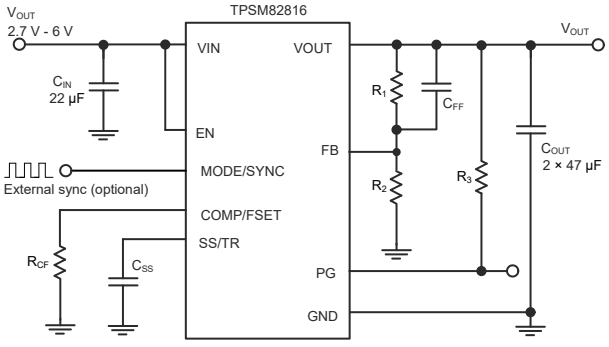
TPSM82816 具有集成电感器和频率同步功能的 2.7V 至 6V 输入 6A 降压 MicroSiP™ 电源模块

1 特性

- 可调和可同步开关频率为 1.8MHz 至 4MHz
- 展频时钟（可选）
- 可选强制 PWM 或 PFM/PWM 运行
- 输出电压精度为 ±1%（PWM 运行）
- 输入电压范围：2.7V 至 6V
- 输出电压范围：0.6V 至 5.5V
- 可调软启动或跟踪
- 具有窗口比较器的电源正常输出
- 精密使能输入可实现
  - 用户定义的欠压锁定
  - 准确排序
- 100% 占空比
- 输出放电
- 26μA 静态电流（典型值）
- 与 TPSM82813 (3A) 和 TPSM82810 (4A) 引脚对引脚兼容
- 优异的热性能
- –40°C 至 125°C 工作温度范围

2 应用

- 光学模块、数据中心互连
- 信号测量、源生成、仪表
- 患者监护和诊断
- 无线基础设施
- 加固型通信：传感器、成像和雷达



原理图

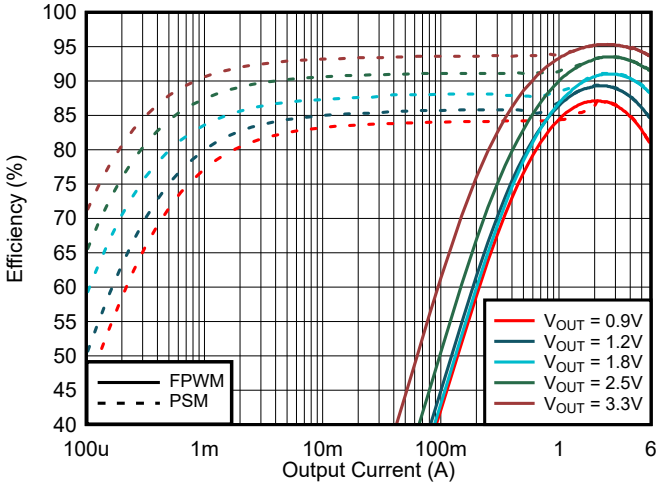
3 说明

TPSM82816 是具有集成电感器、引脚对引脚兼容的 3A、4A 和 6A 高效、易于使用的同步直流/直流降压电源模块系列中的一款产品。这些器件基于固定频率峰值电流模式控制拓扑，用于具有高功率密度和易用性要求的电信、测试和测量以及医疗应用领域。低阻开关可在高温环境下支持高达 6A 的持续输出电流。用户可通过外部方式在 1.8MHz 至 4MHz 范围内调节开关频率，亦可在该频率范围内将其同步至外部时钟。在省电模式下，TPSM82816 会在轻负载时自动进入 PFM，从而可在整个负载范围内保持高效率。TPSM82816 可在 PWM 模式下提供 1% 的输出电压精度，这有助于实现具有高输出电压精度的电源设计。SS/TR 引脚可设置启动时间或跟踪向外部源提供的输出电压。此特性可实现不同电源轨的外部定序并限制启动期间的浪涌电流。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
TPSM82816	SIE（uSiP，14）	3.0mm × 4.0mm × 1.6mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



效率与输出电流间的关系；V_{IN} = 5V；f_{SW} = 1.8MHz；T_A = 25°C

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	SPREAD SPECTRUM CLOCKING
TPSM82816SIER	6 A	Set by COMP / FSET pin

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6 Pin Configuration and Functions

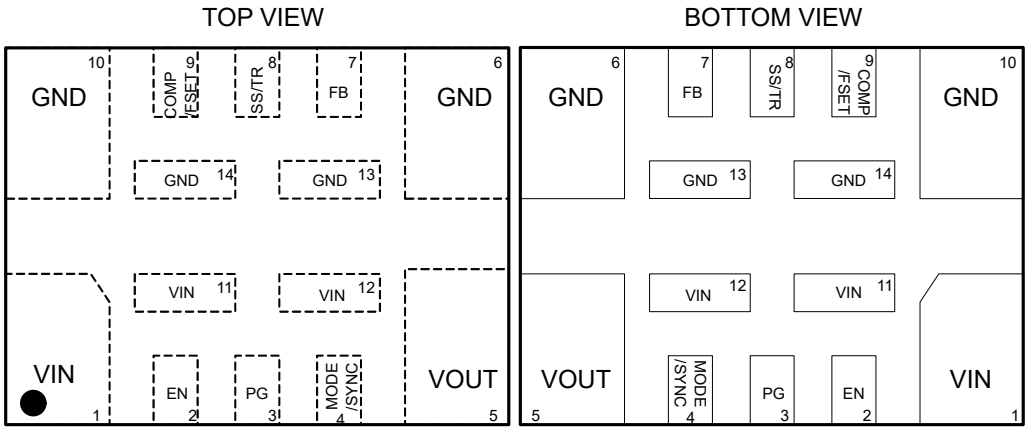


图 6-1. uSiP 14-pin SIE Package

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	This pin is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB	7	I	Voltage feedback input. Connect the output voltage resistor divider to this pin.
GND	6, 10, 13, 14		Ground pin
MODE/SYNC	4	I	The device runs in PSM (auto PFM/PWM transition) mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The MODE/SYNC pin can also be used to synchronize the device to an external frequency. See *Synchronizing to an External Clock*.
COMP/FSET	9	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized. The switching frequency is set to 2.25 MHz if the pin is tied to GND or VIN. Spread spectrum is also enabled and disabled by this pin. See *COMP/FSET*. Do not leave this pin unconnected.
PG	3	O	Open-drain power-good output with window comparator. This pin is pulled to GND while VOUT is outside the power-good threshold. This pin can be left open or tied to GND if not used. A pullup resistor can be connected to any voltage not larger than VIN.
SS/TR	8	I	Soft-start, tracking pin. A capacitor connected from this pin to GND defines the output voltage rise time. The pin can also be used as an input for tracking and sequencing - see *Voltage Tracking*.
VOUT	5		Output voltage pin. This pin is internally connected to the integrated inductor.
VIN	1, 11, 12		Power supply input. Connect the input capacitor as close as possible between the VIN and GND pins.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN, EN, MODE/SYNC	–0.3	6.5	V
Pin voltage(2)	FB	–0.3	4	V
Pin voltage(2)	COMP/FSET, PG, SS/TR, VOUT	–0.3	V_{IN} + 0.3	V
I_{SINK_PG}	Sink Current at PG pin		10	mA
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–40	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		6	V
V_{OUT}	Output voltage range	0.6		5.5	V
I_{OUT}	Output current	0		6	A
C_{OUT}	Effective output capacitance(1)	32 × V / V_{OUT}		470	µF
C_{IN}	Effective input capacitance(1)	5	10		µF
R_{CF}		4.5		100	kΩ
I_{SINK_PG}	Sink current at PG pin	0		2	mA
T_J	Junction temperature	–40		125	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied. Please see the feature description for COMP/FSET about the output capacitance vs compensation setting and output voltage.

7.4 Thermal Information

THERMAL METRIC(1)		TPSM82816		UNIT
		14 PINS		
		JEDEC 51-5	EVM	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	45.3	32.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29	n/a (2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	n/a (2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5.7	7.2	°C/W

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7.4 Thermal Information (continued)

THERMAL METRIC(1)		TPSM82816		UNIT
		14 PINS		
		JEDEC 51-5	EVM	
Ψ_{JB}	Junction-to-board characterization parameter	16.2	12.7	°C/W

(1) For more information about thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM.

7.5 Electrical Characteristics

Over operating junction remperature range (T_J = –40°C to +125°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device not switching, MODE/SYNC = GND, V_{OUT} = 0.6 V		18	36	µA
I_{SD}	Shutdown current	EN = GND		0.15	90	µA
V_{UVLO}	Undervoltage lock out threshold	V_{IN} rising	2.45	2.6	2.7	V
		V_{IN} falling	2.1	2.5	2.6	V
T_{JSD}	Thermal shutdown threshold	T_J rising		180		°C
	Thermal shutdown hysteresis	T_J falling		15		°C
CONTROL and INTERFACE						
$V_{IH,EN}$	Input threshold voltage	EN rising	1.05	1.1	1.15	V
$V_{IL,EN}$	Input threshold voltage	EN falling	0.96	1.0	1.05	V
$I_{IH,EN}$	Input leakage current into EN	EN = VIN or GND			125	nA
V_{IH}	Input-threshold voltage at MODE/SYNC		1.1			V
V_{IL}	Input-threshold voltage at MODE/SYNC				0.3	V
I_{IH}	Input leakage current into MODE/SYNC				250	nA
f_{SW}	PWM Switching frequency range	MODE/SYNC = high	1.8	2.25	4	MHz
f_{SW}	PWM Switching frequency	COMP/FSET = GND or V_{IN}	2.08	2.25	2.4	MHz
f_{SW}	PWM Switching frequency tolerance	using a resistor from COMP/FSET to GND	–12 %		12 %	
f_{SYNC}	Frequency range on MODE/SYNC pin for synchronization		1.8		4	MHz
t_{Sync_lock}	Time to lock to external frequency			50		µs
	Duty cycle of synchronization signal at MODE/SYNC		20 %		80 %	
t_{Delay}	Enable delay time	Time from EN high to device starts switching; V_{IN} applied already	135	270	520	µs
t_{Ramp}	Output voltage ramp time, SS/TR pin open	I_{OUT} = 0 mA, time from device starts switching to power good; device not in current limit	90	150	220	µs
$I_{SS/TR}$	SS/TR source current		8	10	12	µA
$R_{DIS,SS/TR}$	Internal discharge resistance on SS/TR	EN = low	0.7	1.1	1.5	kΩ
	Tracking gain	V_{FB} / $V_{SS/TR}$		1		
	Tracking offset	V_{FB} when $V_{SS/TR}$ = 0 V		±1		mV
V_{TH_PG}	UVP power good threshold voltage; dc level	V_{OUT} rising (%V_{FB})	92 %	95 %	98 %	
V_{TH_PG}	UVP power good threshold voltage; dc level	V_{OUT} falling (%V_{FB})	87 %	90 %	93 %	

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7.5 Electrical Characteristics (continued)

Over operating junction remperature range (T_J = –40°C to +125°C) and V_{IN} = 2.7 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25°C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{TH_PG}	OVP power good threshold voltage; dc level	V_{OUT} rising (%V_{FB})	107 %	110 %	113 %	
	OVP power good threshold voltage; dc level	V_{OUT} falling (%V_{FB})	104 %	107 %	111 %	
$V_{OL,PG}$	Low-level output voltage at PG	I_{SINK_PG} = 2 mA		0.01	0.3	V
$I_{IH,PG}$	Input leakage current into PG	V_{PG} = 5 V			100	nA
$t_{PG,DLY}$	PG deglitch time	for a high level to low level transition on the power good output		40		µs
OUTPUT						
V_{FB}	Feedback voltage			0.6		V
V_{FB}	Feedback voltage accuracy	PWM mode, $V_{IN} \geqslant V_{OUT}$ + 1 V	–1 %		1 %	
V_{FB}	Feedback voltage accuracy	PFM mode, $V_{IN} \geqslant V_{OUT}$ + 1 V, $V_{OUT} \geqslant$ 1.5 V, Co,eff ⩾ 47 µF	–1 %		2 %	
V_{FB}	Feedback voltage accuracy	PFM mode, $V_{IN} \geqslant V_{OUT}$ + 1 V, V_{OUT} < 1.5 V, Co,eff ⩾ 68 µF	–1 %		2.5 %	
V_{FB}	Feedback voltage accuracy with voltage tracking	$V_{IN} \geqslant V_{OUT}$ + 1 V, $V_{SS/TR}$ = 0.3 V, PWM mode	–5 %		5 %	
$I_{IH,FB}$	Input leakage current into FB	V_{FB} = 0.6 V		1	70	nA
	Load regulation	PWM mode		0.05		%/A
R_{DIS}	Output discharge resistance			30	50	Ω
$t_{on,min}$	Minimum on-time of high-side FET	$V_{IN} \geqslant$ 3.3 V		45	67	ns
R_{DP}	Dropout Resistance	100% mode		27		mΩ
I_{LIMH}	High-side FET switch current limit	DC value, V_{IN} = 3 V to 6 V	7.3	9.2	10.4	A
I_{LIMNEG}	Low-side FET negative current limit	DC value, MODE/SYNC = high		–3		A

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7.6 Typical Characteristics

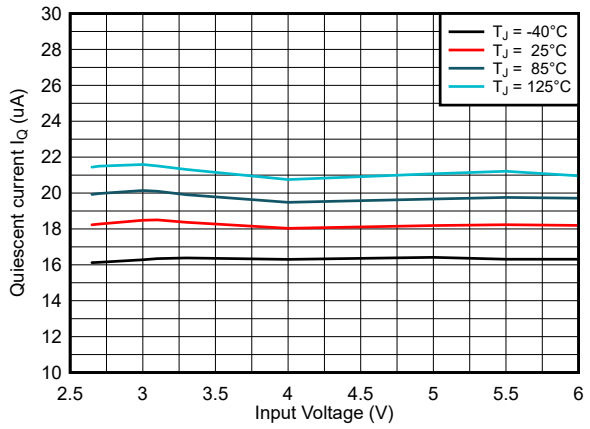


图 7-1. Quiescent Current

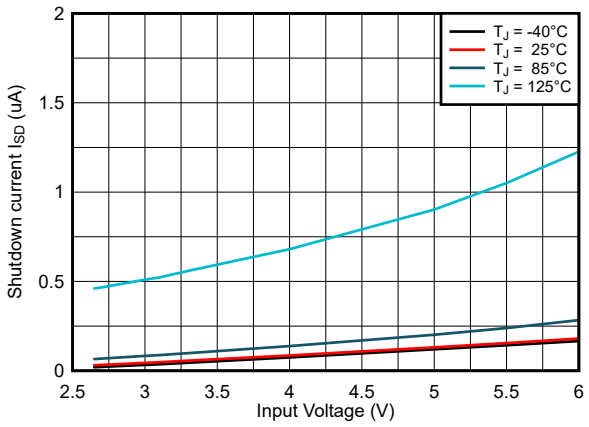


图 7-2. Shutdown Current

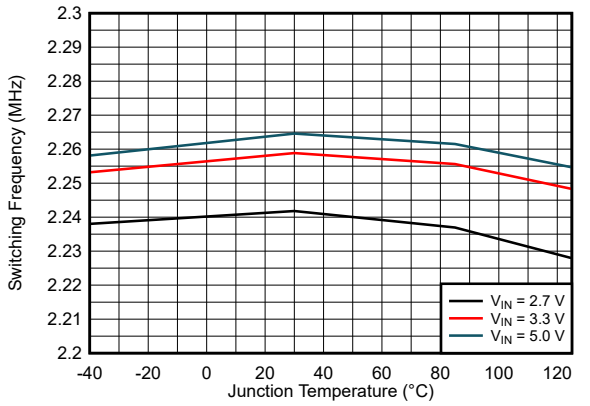


图 7-3. Oscillator Frequency (COMP/FSET = VIN)

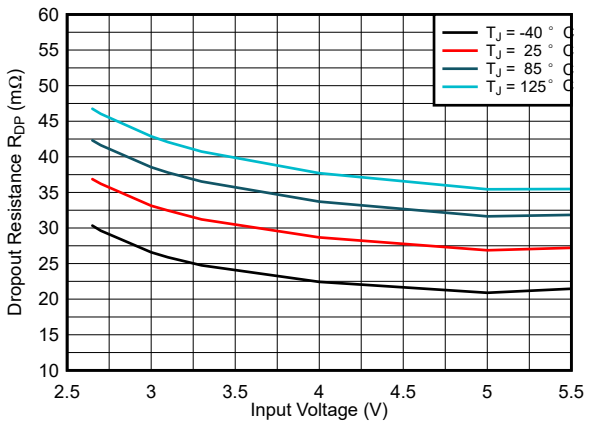


图 7-4. Dropout Resistance

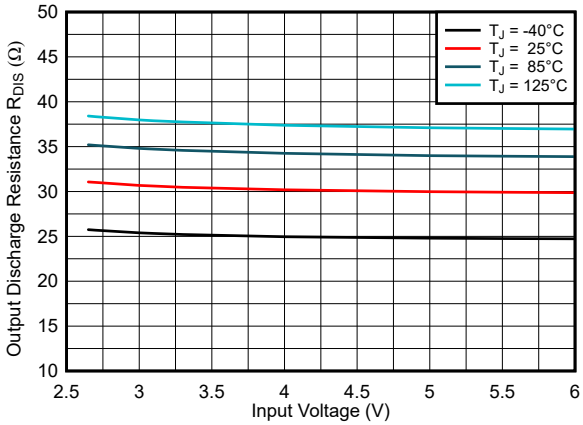


图 7-5. Discharge Resistance

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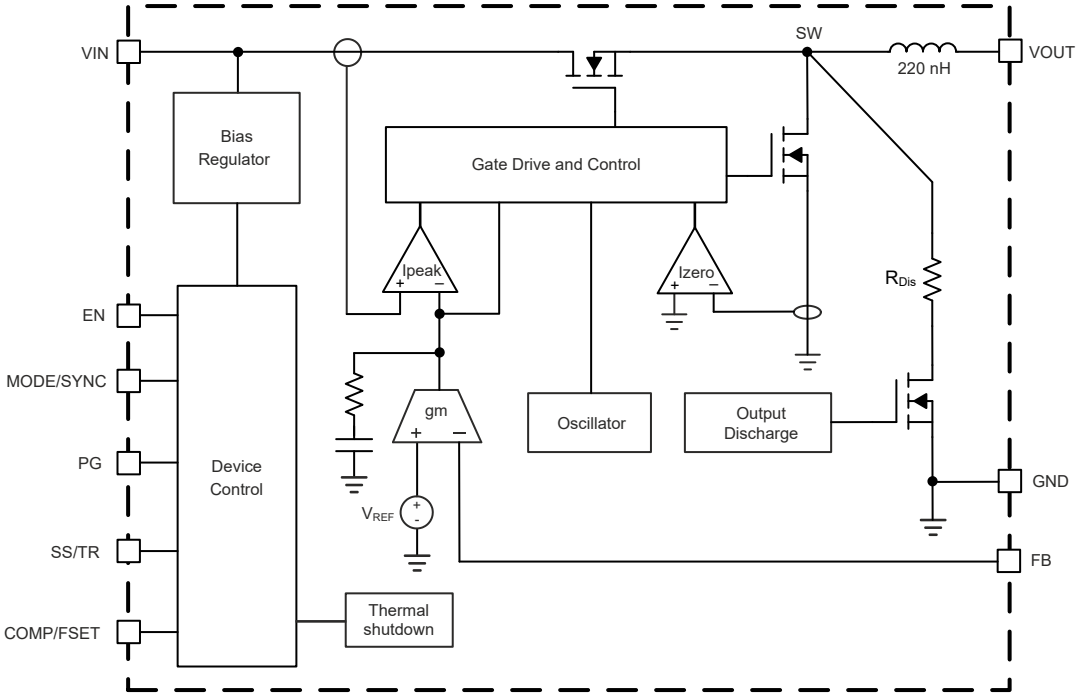
8 Detailed Description

8.1 Overview

The TPSM82816 synchronous switch mode DC/DC converter power modules are based on a fixed-frequency peak current-mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with the TPSM82816, one of two internal compensation settings can be selected. See *COMP/FSET*. The compensation setting is selected either by a resistor from COMP/FSET to GND or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors.

The device supports forced fixed frequency operation (FPWM) with the MODE/SYNC pin tied to a logic high level. The frequency is defined as either 2.25 MHz (internally fixed when COMP/FSET is tied to GND or VIN) or in a range of 1.8 MHz to 4 MHz (defined by a resistor from COMP/FSET to GND). Alternatively, the device can be synchronized to an external clock signal in a range from 1.8 MHz to 4 MHz, applied to the MODE/SYNC pin with no need for additional passive components. An internal PLL allows the device to change from internal clock to external clock during operation. The synchronization to the external clock is done on the falling edge of the clock applied at MODE/SYNC to the rising edge on the internal SW node. When the MODE/SYNC pin is set to a logic low level, the device operates in power save mode (PSM). At low output current, the device operates in PFM mode and automatically transitions to fixed-frequency PWM mode at higher output current. In PFM operation, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output current (see *Power Save Mode Operation (PSM)* for more details).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Precise Enable (EN)

The TPSM82816 starts operation when the rising EN threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off. The voltage applied at the EN pin of the TPSM82816 is compared to a fixed threshold of 1.1 V for a rising voltage.

The enable input threshold for a falling edge is typically 100 mV lower than the rising edge threshold. The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the

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input of the EN pin. The Precise Enable input also allows you to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. See the *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold Technical Brief* for more details.

8.3.2 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is being disabled, but also to keep the output voltage close to 0 V when the device is off. The output discharge feature is only active after the TPSM82816 has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active is typically 2 V. Output discharge is not activated during a current limit event.

8.3.3 COMP/FSET

This pin allows the user to set three different parameters independently:

- Internal compensation settings for the control loop (two settings available)
- The switching frequency in PWM mode from 1.8 MHz to 4 MHz
- Enable / disable spread spectrum clocking (SSC)

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation allows the user to adopt the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is sampled at the start-up of the converter, so a change in the resistor during operation only has an effect on the switching frequency, but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined switching frequency or compensation. Do not leave the pin floating.

The switching frequency has to be selected based on the maximum input voltage in the application and the output voltage to meet the specifications for the minimum on time.

Example: V_{IN} = 5.5 V, V_{OUT} = 1 V

$$f_{Sw,max} = \frac{V_{OUT}}{V_{IN} \times t_{ON,min}} = \frac{1\,V}{5.5\,V \times 67\,ns} = 2.71\,MHz \quad (1)$$

The compensation range has to be chosen based on the effective minimum capacitance used. The capacitance can be increased from the minimum value as given in 表 8-1, up to the maximum of 470 µF in both compensation ranges. If the capacitance of an output changes during operation, for example when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. If the output capacitance exceeds 72 µF × V / VOUT[V], use the second compensation setting to get the best load transient response. If the output capacitance only exceeds 32 µF × V / VOUT[V], use the first compensation setting. Compensating for large output capacitance but having too little effective capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1 with spread spectrum clocking (SSC) disabled:

$$R_{CF}\left[k\Omega\right] = \frac{18\,MHz \times k\Omega}{f_S[MHz]} \quad (2)$$

For compensation (comp) setting 1 with spread spectrum clocking (SSC) enabled:

$$R_{CF}\left[k\Omega\right] = \frac{60\,MHz \times k\Omega}{f_S[MHz]} \quad (3)$$

For compensation (comp) setting 2 with spread spectrum clocking (SSC) disabled:

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$$R_{CF}\left[k\Omega\right] = \frac{180\ MHz \times k\Omega}{f_S[MHz]} \quad (4)$$

表 8-1. Switching Frequency and Compensation

COMPENSATION	R_{CF}	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE
For smallest output capacitance (comp setting 1) SSC disabled	10 kΩ ... 4.5 kΩ	1.8 MHz (10 kΩ) ... 4 MHz (4.5 kΩ) according to 方程式 2	32 µF × V / V_{OUT}[V]
For smallest output capacitance (comp setting 1) SSC enabled	33 kΩ ... 15 kΩ	1.8 MHz (33 kΩ) ... 4 MHz (15 kΩ) according to 方程式 3	32 µF × V / V_{OUT}[V]
For best transient response (larger output capacitance) (comp setting 2) SSC disabled	100 kΩ ... 45 kΩ	1.8 MHz (100 kΩ) ... 4 MHz (45 kΩ) according to 方程式 4	72 µF × V / V_{OUT}[V]
For smallest output capacitance (comp setting 1) SSC disabled	Tied to GND	Internally fixed 2.25 MHz	32 µF × V / V_{OUT}[V]
For best transient response (larger output capacitance) (comp setting 2) SSC enabled	Tied to V_{IN}	Internally fixed 2.25 MHz	72 µF × V / V_{OUT}[V]

The minimum output capacitance required for stability depends on the output voltage as stated in 表 8-1. Refer to *Output Capacitor* for further details on the output capacitance required depending on the output voltage.

A too-high resistor value for R_{CF} is decoded as "tied to V_{IN}" and a value below the lowest range is decoded as "tied to GND". The minimum output capacitance in 表 8-1 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

8.3.4 MODE/SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin forces PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8 MHz to 4 MHz for external synchronization. When an external clock is applied, the device only operates in PWM mode. As with the switching frequency selection, the specification for the minimum on-time has to be observed when applying the external clock signal. When using external synchronization, TI recommends to set the switching frequency (as set by R_{CF}) to a similar value as the externally applied clock. This ensures that, if the external clock fails, the switching frequency stays in the same range and the settling time to the internal clock is reduced. When there is no resistor from COMP/FSET to GND, but the pin is pulled high or low, external synchronization is not possible. An internal PLL allows you to change from an internal clock to external clock during operation. The synchronization to the external clock is done on the falling edge of the applied clock to the rising edge of the internal SW pin (see *Synchronizing to an External Clock*). The MODE/SYNC pin can be changed during operation.

8.3.5 Spread Spectrum Clocking (SSC)

The device offers spread spectrum clocking as an option, set by the COMP/FSET pin. When SSC is enabled, the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288 kHz above the nominal switching frequency. When the device is externally synchronized, the TPSM82816 follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

8.3.6 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the MOSFETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage goes below the falling threshold.

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8.3.7 Power-Good Output (PG)

The device has a power-good output with window comparator. The PG pin goes high impedance after the FB pin voltage is above 95% and less than 107% of the nominal voltage, and is driven low after the voltage falls below 90% or rises higher than 110% of the nominal voltage (typical). 表 8-2 shows the typical PG pin logic. The PG pin is an open-drain output and is specified to sink up to 2 mA. The power good output requires a pullup resistor connected to any voltage rail less than VIN. The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. If not used, the PG pin can be left floating or connected to GND.

表 8-2. Power-Good Pin Logic

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enabled (EN = High)	$0.95 \times V_{FB_NOM} \leqslant V_{FB} \leqslant 1.07 \times V_{FB_NOM}$	√	
	$V_{FB} < 0.9 \times V_{FB_NOM}$ or $V_{FB} > 1.1 \times V_{FB_NOM}$		√
Shutdown (EN = Low)			√
UVLO	$2\ V \leqslant V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{JSD}$		√
Power Supply Removal	$V_{IN} < 2\ V$	undefined	

The PG pin has a 40- μ s deglitch time on the falling edge. See 图 8-1.

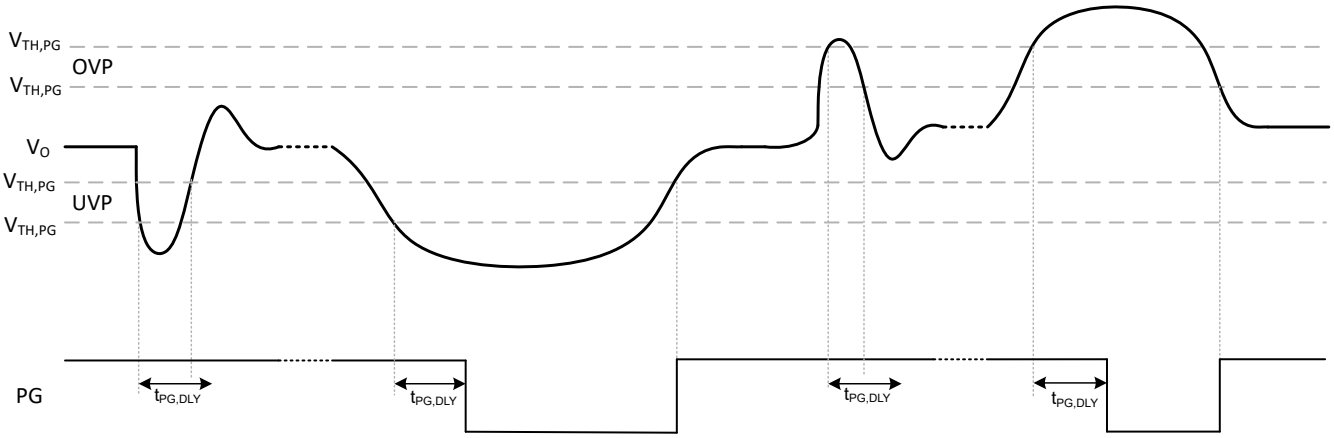


图 8-1. Power-Good Transient and Delay Behavior

8.3.8 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 180°C (typical), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During PFM the thermal shutdown is not active.

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8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TPSM82816 has two operating modes: Forced PWM mode (FPWM) and Power Save Mode (PSM).

With the MODE/SYNC pin set to high, the TPSM82816 operates with pulse width modulation (PWM) in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP/FSET pin to GND or by an external clock signal applied to the MODE/SYNC pin.

With the MODE/SYNC pin set to low, the TPSM82816 operates with pulse frequency modulation (PFM) during light load and will automatically transition into PWM as the load current increases.

8.4.2 Power Save Mode Operation (PSM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 1.8 A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses. The frequency set with the resistor on COMP/FSET must be in a range of 1.8 MHz to 3.5 MHz.

In power save mode, the switching frequency decreases linearly with the load current to maintain high efficiency. The linear behavior of the switching frequency in power save mode is shown in 图 8-2.

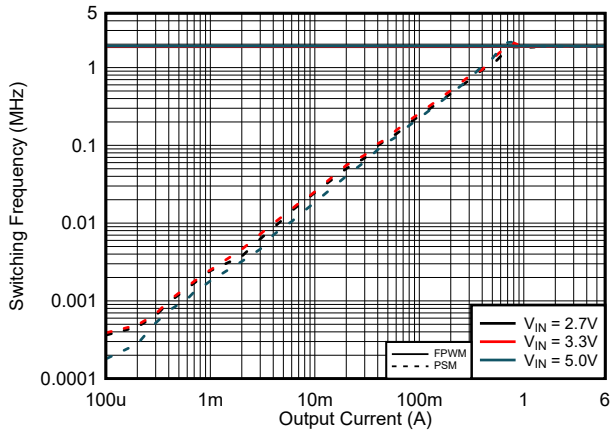


图 8-2. Switching Frequency versus Output Current (V_{OUT} = 1.8 V, R_{CF} = 10 kΩ)

8.4.3 100% Duty-Cycle Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. When the minimum off-time of typically 15 ns is reached, the TPSM82816 skips switching cycles while it approaches 100% mode. In 100% mode, the high-side MOSFET switch is constantly turned on. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP} \quad (5)$$

where:

- R_{DP} is the resistance from VIN to VOUT, which includes the high-side MOSFET on-resistance and DC resistance of the inductor
- $V_{OUT(min)}$ is the minimum output voltage the load can accept

This operation mode is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

8.4.4 Current Limit and Short-Circuit Protection

The TPSM82816 is protected against overload and short circuit events. If the inductor current exceeds the current limit I_{LIMH}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the

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inductor current. The high-side MOSFET turns on again only if the current in the low-side MOSFET has decreased below the low-side current limit. Due to internal propagation delays, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak\ (typ)} = I_{LIMH} + \frac{V_L}{L} \times t_{PD} \quad (6)$$

where

- I_{LIMH} is the static current limit, as specified in the electrical characteristics
- L is the effective inductance (typically 220 nH)
- V_L is the voltage across the inductor (V_{IN} - V_{OUT})
- t_{PD} is the internal propagation delay of typically 50 ns

The dynamic peak current is calculated as follows:

$$I_{peak\ (typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{220\ nH} \times 50\ ns \quad (7)$$

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle. The negative current limit is only active in Forced PWM mode.

8.4.5 Soft Start / Tracking (SS/TR)

The soft-start circuitry controls the output voltage slope during start-up. This action avoids excessive inrush current and ensures a controlled output voltage rise time. This action also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high, the device starts switching after a delay of about 270 μs. Then V_{OUT} rises with a slope controlled by an external capacitor connected to the SS/TR pin.

A capacitor connected from SS/TR to GND is charged with 10 μA by an internal current source during soft start until it reaches the reference voltage of 0.6 V. After reaching 0.6 V, the SS/TR pin voltage is clamped internally while the SS/TR pin voltage keeps rising to a maximum of about 3.3 V. The capacitance required to set a certain ramp-time (t_{ramp}) is:

$$C_{SS}[nF] = \frac{10\mu A \times t_{ramp}[ms]}{0.6\ V} \quad (8)$$

Leaving the SS/TR pin un-connected provides the fastest start-up ramp of 150 μs typically. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor of about 1.1 kΩ pulls the SS/TR pin to GND to ensure a proper low level. Returning from those states causes a new start-up sequence.

A voltage applied at the SS/TR pin can also be used to track a master voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PSM mode, the output voltage decreases based on the load current. An external voltage applied on SS/TR is internally clamped to the feedback voltage (0.6 V). TI recommends to set the final value of the external voltage on SS/TR to be slightly above 0.6 V to make sure the device operates with its internal reference voltage when the power-up sequencing is finished. See *Voltage Tracking*.

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9 Application and Implementation

备注

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9.1 Application Information

The TPSM82816 is a synchronous step-down converter power module. The power inductor is integrated inside the TPSM82816. The inductor is shielded and has an inductance of 220 nH. The TPSM82810, TPSM82813 and TPSM82816 are pin-to-pin compatible.

9.2 Typical Application

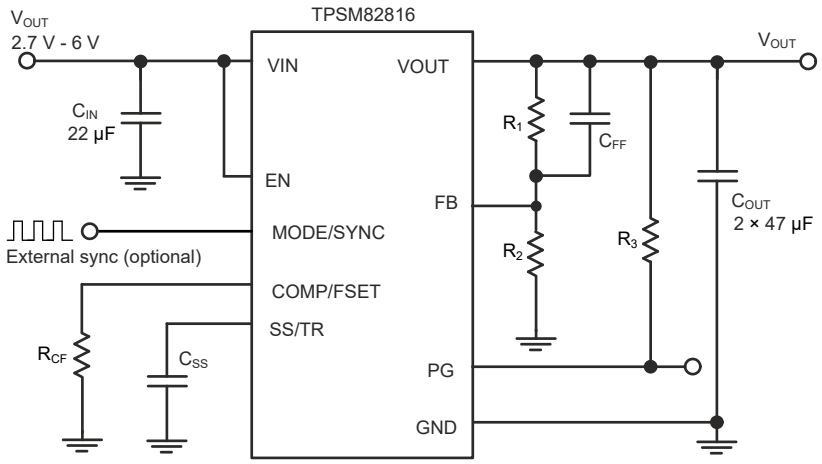


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

表 9-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPSM82816	Texas Instruments
C_{IN}	22 µF / X7R / 6.3 V; GRM21BZ70J226ME44L	Murata
C_{OUT} for V_{OUT} < 1 V	3 × 47 µF / X6S / 6.3 V; JMK212BC6476MG-T	Taiyo Yuden
C_{OUT} for V_{OUT} ⩾ 1 V	2 × 47 µF / X6S / 6.3 V; JMK212BC6476MG-T	Taiyo Yuden
C_{SS}	4.7 nF	Any
R_{CF}	10 kΩ	Any
C_{FF}	10 pF	Any
R_1	Depending on VOUT	Any
R_2	Depending on VOUT	Any
R_3	100 kΩ	Any

(1) See the *Third-party Products Disclaimer*.

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9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Output Voltage

The output voltage of the TPSM82816 is adjustable. Choose resistors R1 and R2 to set the output voltage within a range of 0.6 V to 5.5 V according to 方程式 9. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100 kΩ to have at least 6 µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter Technical Brief*.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R_2 \times \left(\frac{V_{OUT}}{0.6\,V} - 1\right) \quad (9)$$

表 9-2. Examples for setting the Output Voltage

NOMINAL OUTPUT VOLTAGE V_{OUT}	R_1	R_2	Max C_{FF} at min C_{out}	OUTPUT VOLTAGE
0.8 V	16.9 kΩ	51 kΩ	15 pF	0.7988 V
1.0 V	20 kΩ	30 kΩ	13 pF	1.0 V
1.1 V	39.2 kΩ	47 kΩ	6.8 pF	1.101 V
1.2 V	68 kΩ	68 kΩ	3.9 pF	1.2 V
1.5 V	76.8 kΩ	51 kΩ	3.3 pF	1.5 V
1.8 V	80.6 kΩ	40.2 kΩ	3.3 pF	1.803 V
2.5 V	47.5 kΩ	15 kΩ	5.6 pF	2.5 V
3.3 V	88.7 kΩ	19.6 kΩ	3 pF	3.315 V

9.2.2.2 Feedforward Capacitor

A feedforward capacitor (C_{FF}) is required in parallel with R_1 to improve the transient response. The maximum value for the feedforward capacitor C_{FF} at the minimum output capacitance is determined by 方程式 10:

$$C_{ff,\,max}\left[nF\right] = \frac{266.1\,nF \times \Omega}{R_1} \quad (10)$$

For examples of feedforward capacitor values for common output voltages when using the minimum required output capacitance, refer to 表 9-2.

To improve the load transient performance, more output capacitance can be added. Increasing the C_{FF} above values given by 方程式 10 can also improve the response with larger C_{OUT}. The converter's loop response must be evaluated either through a simple load step or by a phase margin measurement. For details, please refer to: *AN-1733 Load Transient Testing Simplified Application Report*.

9.2.2.3 Input Capacitor

For most applications, TI recommends a 22-µF nominal ceramic capacitor. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A X7R or X7T multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For applications with ambient temperatures below 85°C, a capacitor with X5R dielectric can be used. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. The minimum required input capacitance is 5 µF.

9.2.2.4 Output Capacitor

The architecture of the TPSM82816 allows the use of ceramic output capacitors which have low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get a narrow capacitance variation with temperature, TI recommends to use an X7R or X7T dielectric. At temperatures below 85°C, an X5R dielectric can be used.

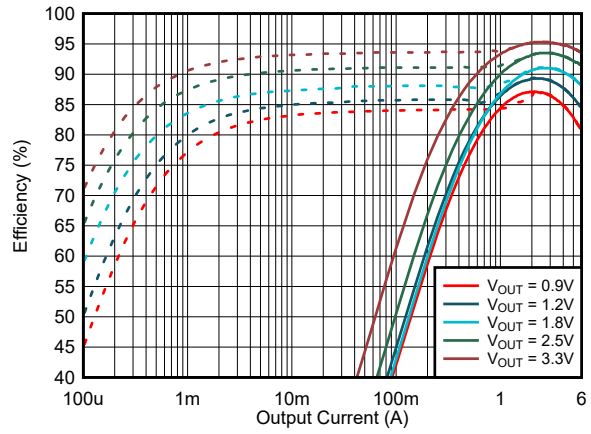
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Using a higher capacitance value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode. By changing the device compensation with a resistor from COMP/FSET to GND, the device can be compensated in two steps based on the minimum capacitance used on the output. The maximum capacitance is 470 µF in any of the compensation settings. The minimum capacitance required on the output depends on the compensation setting and output voltage as shown in 表 8-1. For output voltages below 1 V, the minimum required capacitance increases linearly from 32 µF at 1 V to 53 µF at 0.6 V with the compensation setting for smallest output capacitance. The other compensation setting scales the same. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating.

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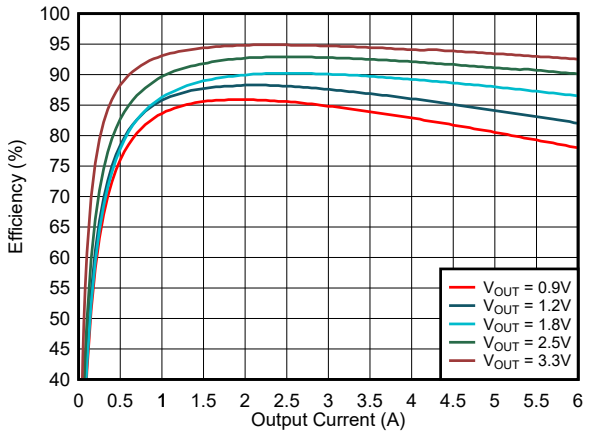
9.2.2.5 Application Curves

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.8 V, 1.8 MHz, PWM mode, BOM = 表 9-1 unless otherwise noted.



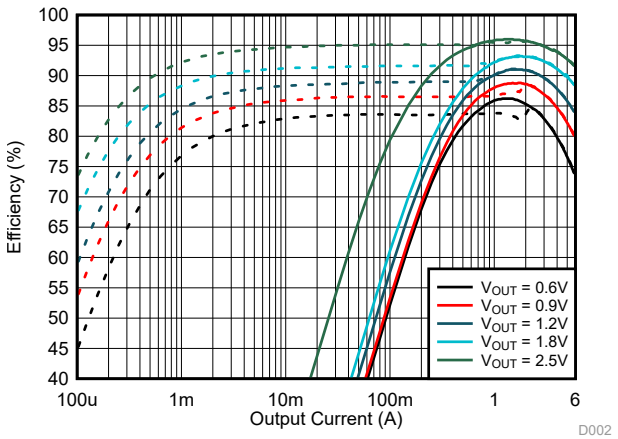
PSM and FPWM

图 9-2. Efficiency V_{IN} = 5.0 V and T_A = 25°C



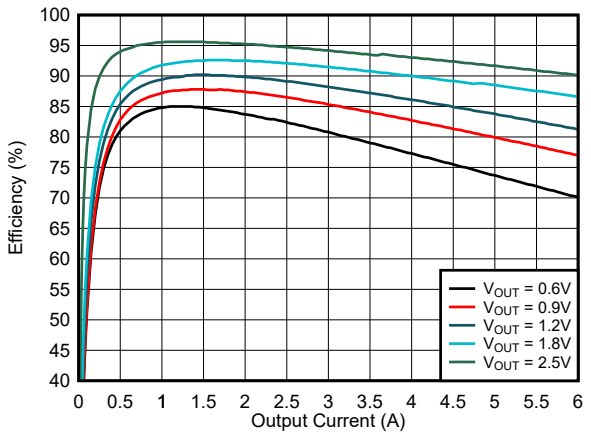
FPWM

图 9-3. Efficiency V_{IN} = 5.0 V and T_A = 85°C



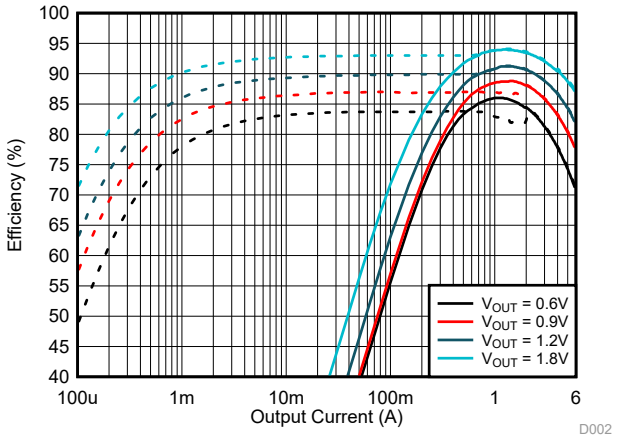
PSM and FPWM

图 9-4. Efficiency V_{IN} = 3.3 V and T_A = 25°C



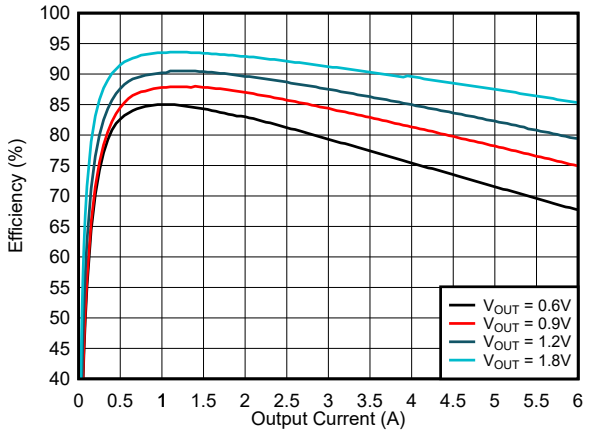
FPWM

图 9-5. Efficiency V_{IN} = 3.3 V and T_A = 85°C



PSM and FPWM

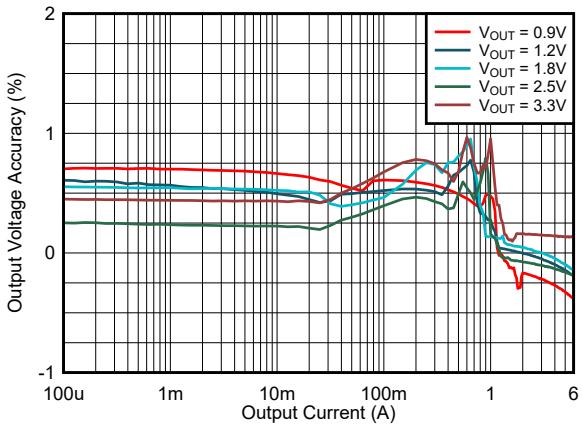
图 9-6. Efficiency V_{IN} = 2.7 V and T_A = 25°C



FPWM

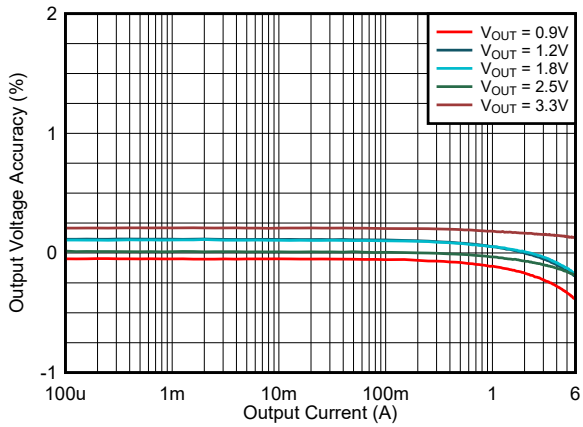
图 9-7. Efficiency V_{IN} = 2.7 V and T_A = 85°C

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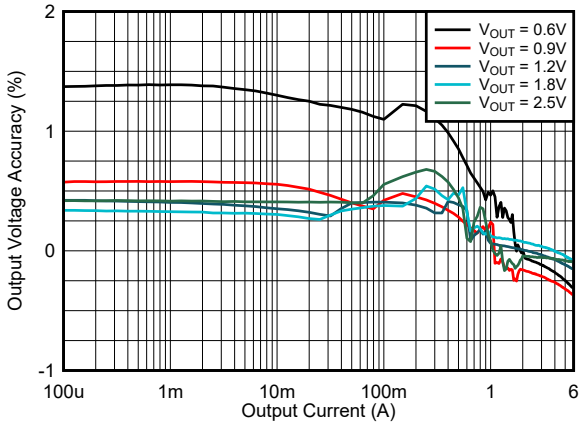
T_A = 25°C

图 9-8. Load Regulation V_{IN} = 5.0 V (PSM)



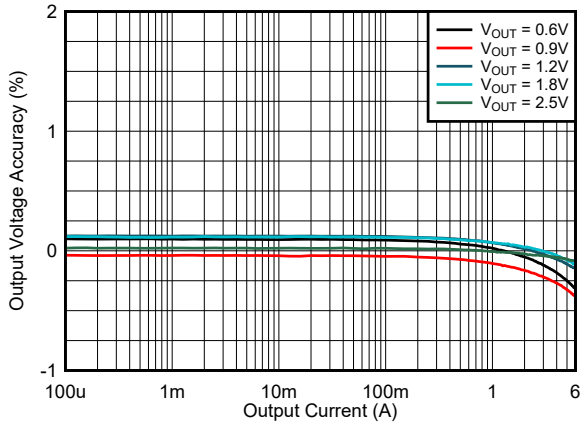
T_A = 25°C

图 9-9. Load Regulation V_{IN} = 5.0 V (FPWM)



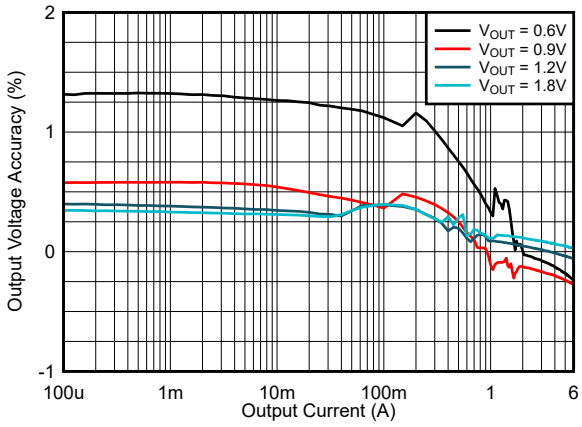
T_A = 25°C

图 9-10. Load Regulation V_{IN} = 3.3 V (PSM)



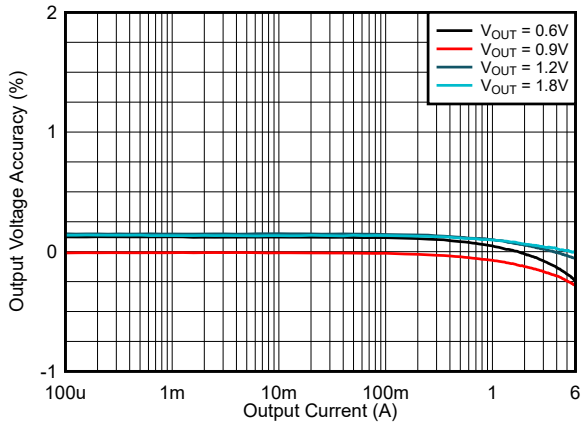
T_A = 25°C

图 9-11. Load Regulation V_{IN} = 3.3 V (FPWM)



T_A = 25°C

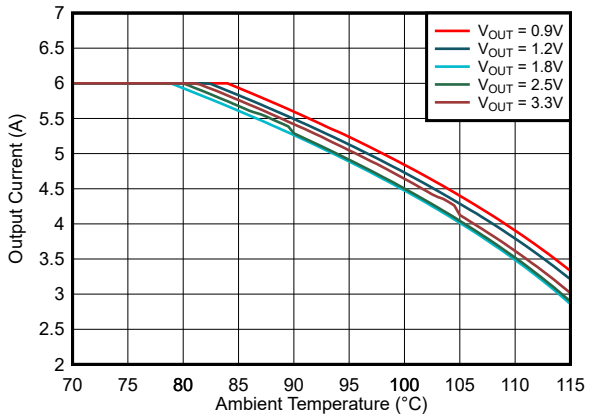
图 9-12. Load Regulation V_{IN} = 2.7 V (PSM)



T_A = 25°C

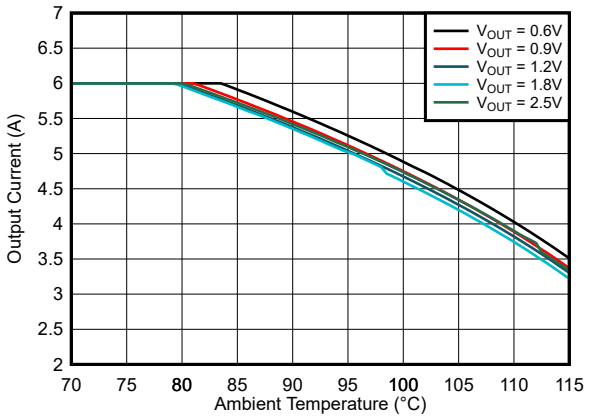
图 9-13. Load Regulation V_{IN} = 2.7 V (FPWM)

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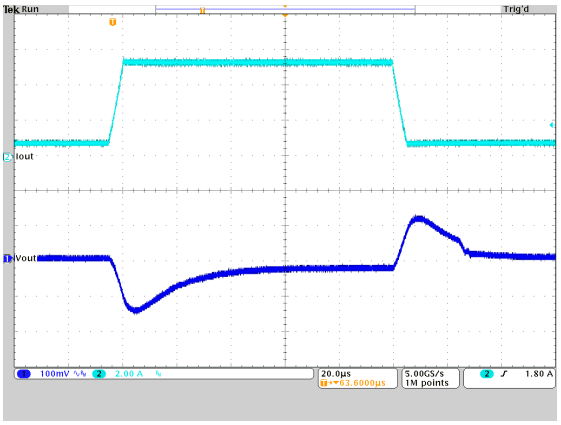
$R_{\theta JA}$ = 32.2 °C/W f_{SW} = 1.8 MHz $T_{J,max}$ = 125 °C

图 9-14. Safe Operating Area V_{IN} = 5.0 V



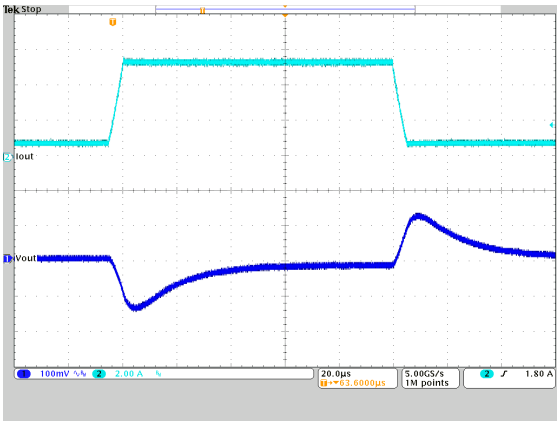
$R_{\theta JA}$ = 32.2 °C/W f_{SW} = 1.8 MHz $T_{J,max}$ = 125 °C

图 9-15. Safe Operating Area V_{IN} = 3.3 V



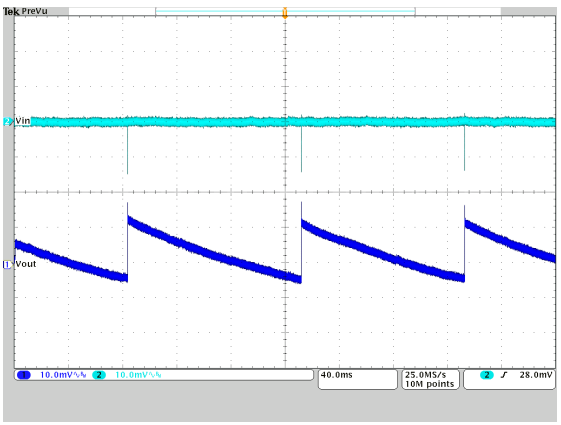
V_{OUT} = 1.8 V PSM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

图 9-16. Load Transient Response



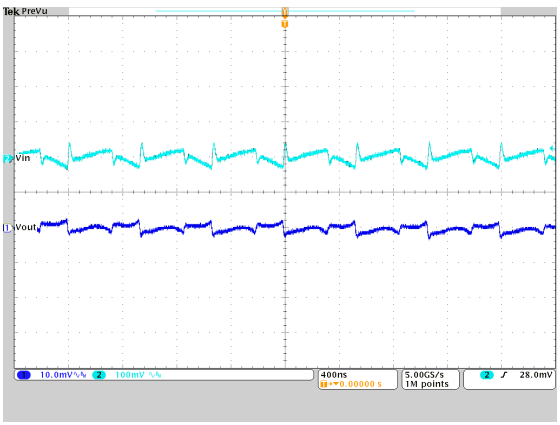
V_{OUT} = 1.8 V FPWM T_A = 25°C
V_{IN} = 5.0 V I_{OUT} = 0.6 A to 5.4 A to 0.6 A

图 9-17. Load Transient Response



V_{OUT} = 1.8 V PSM T_A = 25 °C
I_{OUT} = 0 A V_{IN} = 5.0 V BW = 20 MHz

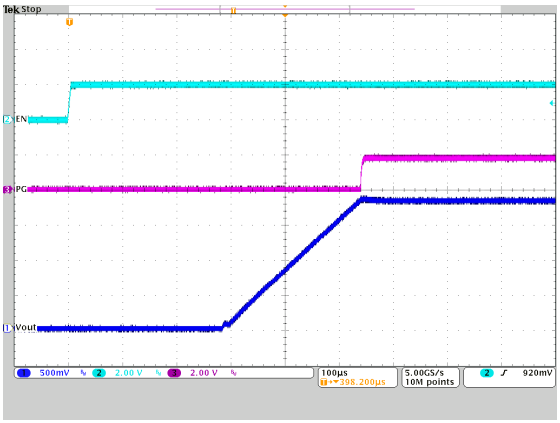
图 9-18. Output and Input Voltage Ripple



V_{OUT} = 1.8 V PWM T_A = 25°C
I_{OUT} = 4 A V_{IN} = 5.0 V BW = 20 MHz

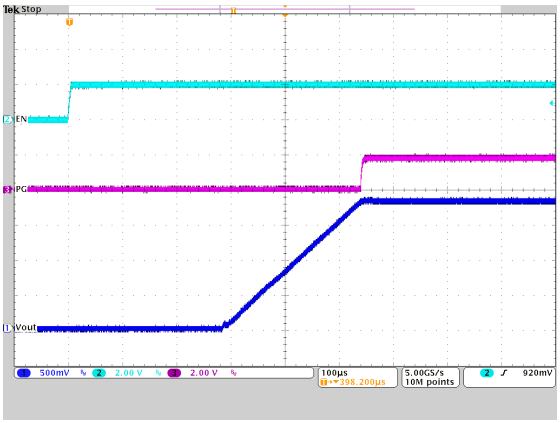
图 9-19. Output and Input Voltage Ripple

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V_{OUT} = 1.8 V　　PSM　　T_A = 25°C
I_{OUT} = 0 A　　V_{IN} = 5 V　　C_{SS} = 4.7 nF

图 9-20. Start-Up Timing



V_{OUT} = 1.8 V　　FPWM　　T_A = 25°C
I_{OUT} = 4 A　　V_{IN} = 5 V　　C_{SS} = 4.7 nF

图 9-21. Start-Up Timing

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9.3 System Examples

9.3.1 Voltage Tracking

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 图 9-22. From 0 V to 0.6 V, the internal reference voltage to the internal error amplifier follows the SS/TR pin voltage. When the SS/TR pin voltage is above 0.6 V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.6 V. The device achieves ratiometric, as shown in 图 9-23 or coincidental (simultaneous) output tracking, as shown in 图 9-23.

The R_2 value must be set properly to achieve accurate voltage tracking by taking the 10-μA charging current into account. 1 kΩ or smaller is a sufficient value for R_2. For decreasing SS/TR pin voltage, the device does not sink current from the output when the device is in PSM. The resulting decrease of the output voltage can be slower than the SS/TR pin voltage if the load is light.

In case both devices need to run in forced PWM mode after start-up, TI recommends to tie the MODE/SYNC pin of the secondary device to the output voltage or the power good signal of the primary device. The TPSM82816 has a duty cycle limitation defined by the minimum on time. For tracking down to low output voltages, the secondary device cannot follow after the minimum duty cycle is reached. Enabling FPWM mode while tracking is in progress allows the user to ramp down the output voltage close to 0 V.

When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin.

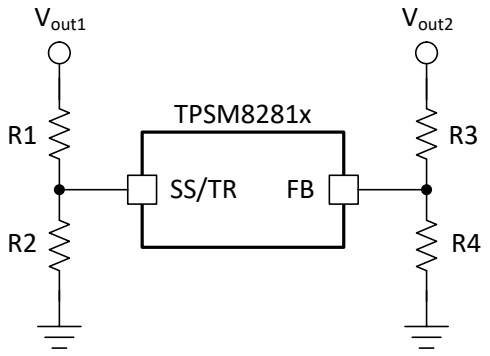


图 9-22. Schematic for Output Voltage Tracking

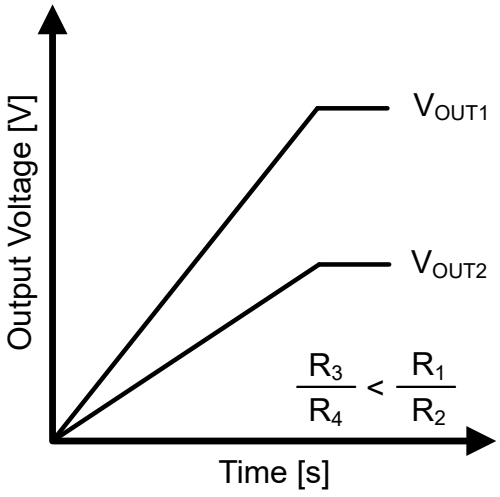


图 9-23. Ratiometric Voltage Tracking

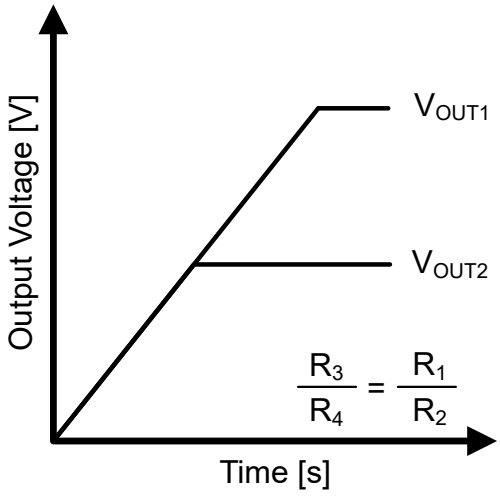


图 9-24. Coincidental Voltage Tracking

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9.3.2 Synchronizing to an External Clock

The TPSM82816 can be synchronized by applying a clock on the MODE/SYNC pin. There is no need for any additional circuitry as long as the input signal meets the requirements given in the electrical specifications. See 图 9-25. The clock can be applied, changed, and removed during operation. The value of the R_{CF} resistor is recommended to be chosen such that the internally defined frequency and the externally-applied frequency are close to each other to have a fast settling time to the external clock. Synchronizing to a clock is not possible if the COMP/FSET pin is connected to Vin or GND. 图 9-26 and 图 9-27 show the external clock being applied and removed. When an external clock is applied, the device operates in PWM mode.

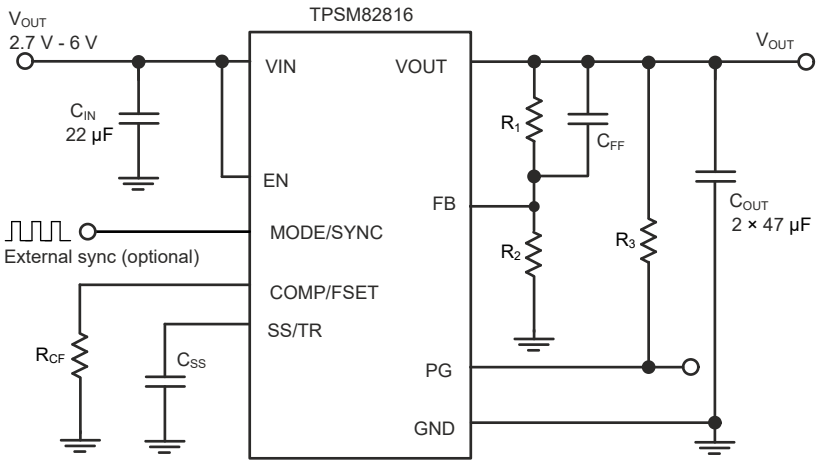
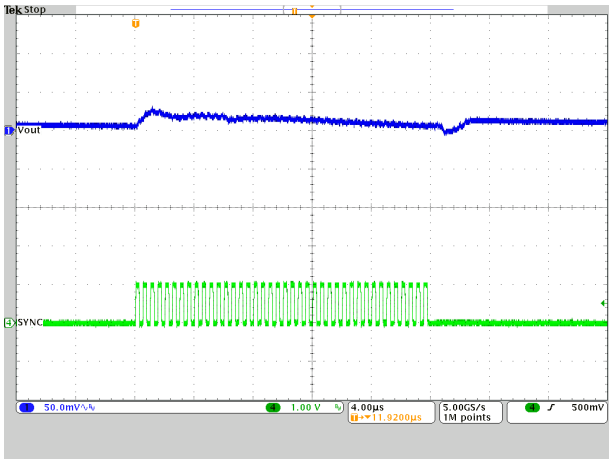
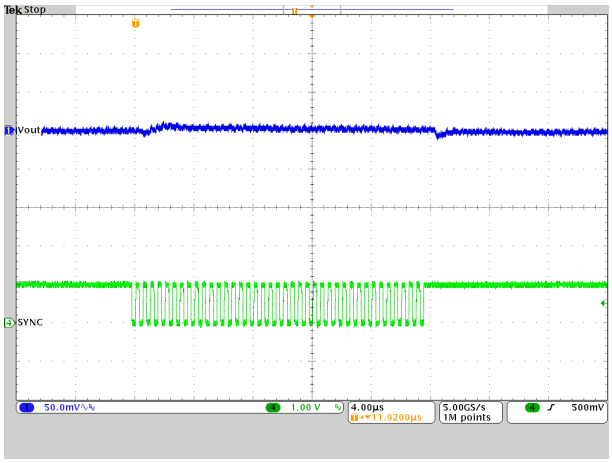


图 9-25. Frequency Synchronization



V_{IN} = 5 V R_{CF} = 10 kΩ I_{OUT} = 0.01 A
V_{OUT} = 1.8 V f_{EXT} = 2.0 MHz

图 9-26. Applying and Removing the Synchronization Signal (PSM)



V_{IN} = 5 V R_{CF} = 10 kΩ I_{OUT} = 1 A
V_{OUT} = 1.8 V f_{EXT} = 2.0 MHz

图 9-27. Applying and Removing the Synchronization Signal (FPWM)

9.4 Power Supply Recommendations

The TPSM82816 device family has no special requirements for the input power supply. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPSM82816.

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9.5 Layout

9.5.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM82816 demands careful attention to ensure best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter Technical Brief* for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- The input capacitor must be placed as close as possible to the VIN and GND pins of the device. This placement is the most critical component placement. Route the input capacitor directly to the VIN and GND pins avoiding vias.
- Place the output capacitor ground close to the VOUT and GND pins and route it directly avoiding vias.
- Place the FB resistors, R1 and R2, and the feedforward capacitor C_{FF} close to the FB pin and place C_{SS} close to the SS/TR pin to minimize noise pickup.
- Place the R_{CF} resistor close to the COMP/FSET pin to minimize the parasitic capacitance.
- The recommended layout is implemented on the EVM and shown in its *TPSM8281xEVM-089 Evaluation Module User's Guide* and in *Layout Example*.
- The recommended land pattern for the TPSM82816 is shown at the end of this data sheet. For best manufacturing results, create the pads as solder mask defined (SMD), when some pins (such as VIN, VOUT, and GND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

9.5.2 Layout Example

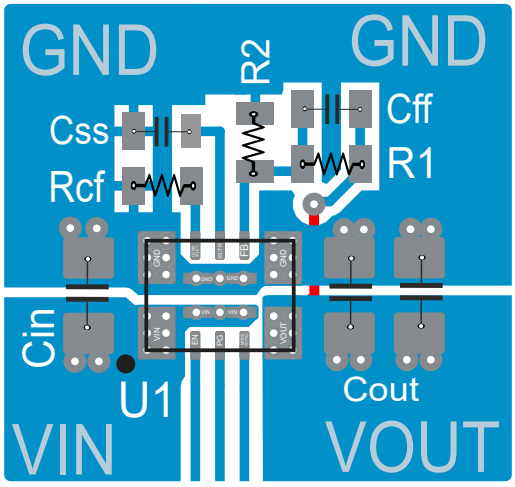


图 9-28. Example Layout

9.5.2.1 Thermal Consideration

The TPSM82816 module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM82816, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

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The thermal values in *Thermal Information* used the recommended land pattern, shown at the end of this data sheet, including the 30 vias as they are shown. The TPSM82816 was simulated on a PCB defined by JEDEC 51-7. The 15 vias on the GND pins were connected to copper on other PCB layers, while the remaining 15 vias were not connected to other layers.

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10 Device and Documentation Support

10.1 Device Support

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPSM8281xEVM-089 Evaluation Module User's Guide*
- Texas Instruments, *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold Technical Brief*
- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter Technical Brief*
- Texas Instruments, *AN-1733 Load Transient Testing Simplified Application Report*
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter Technical Brief*
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*

10.3 接收文档更新通知

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10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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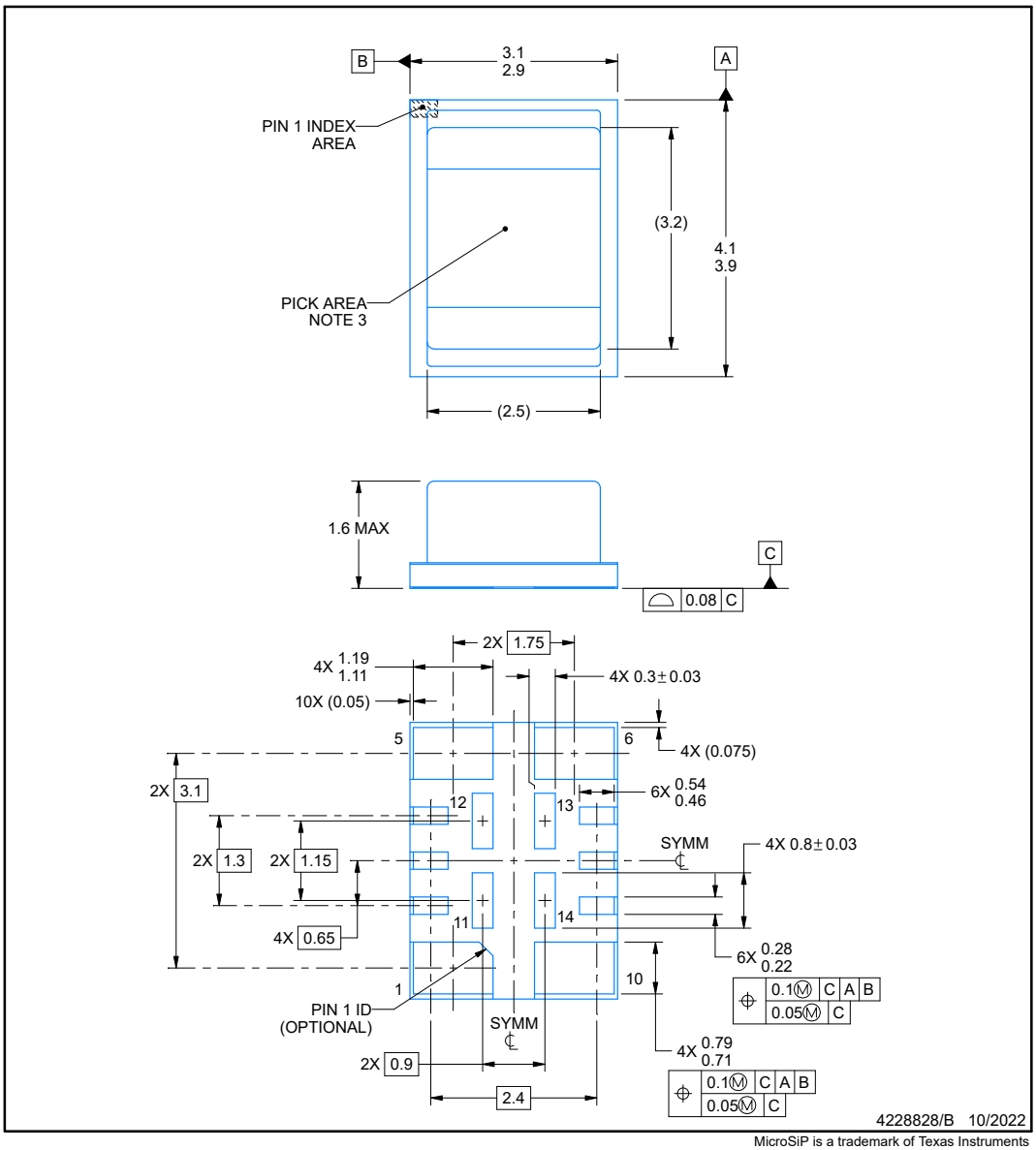
PACKAGE OUTLINE

SIE0014A-C01



uSIP™ - 1.6 mm max height

MICRO SYSTEM IN PACKAGE



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

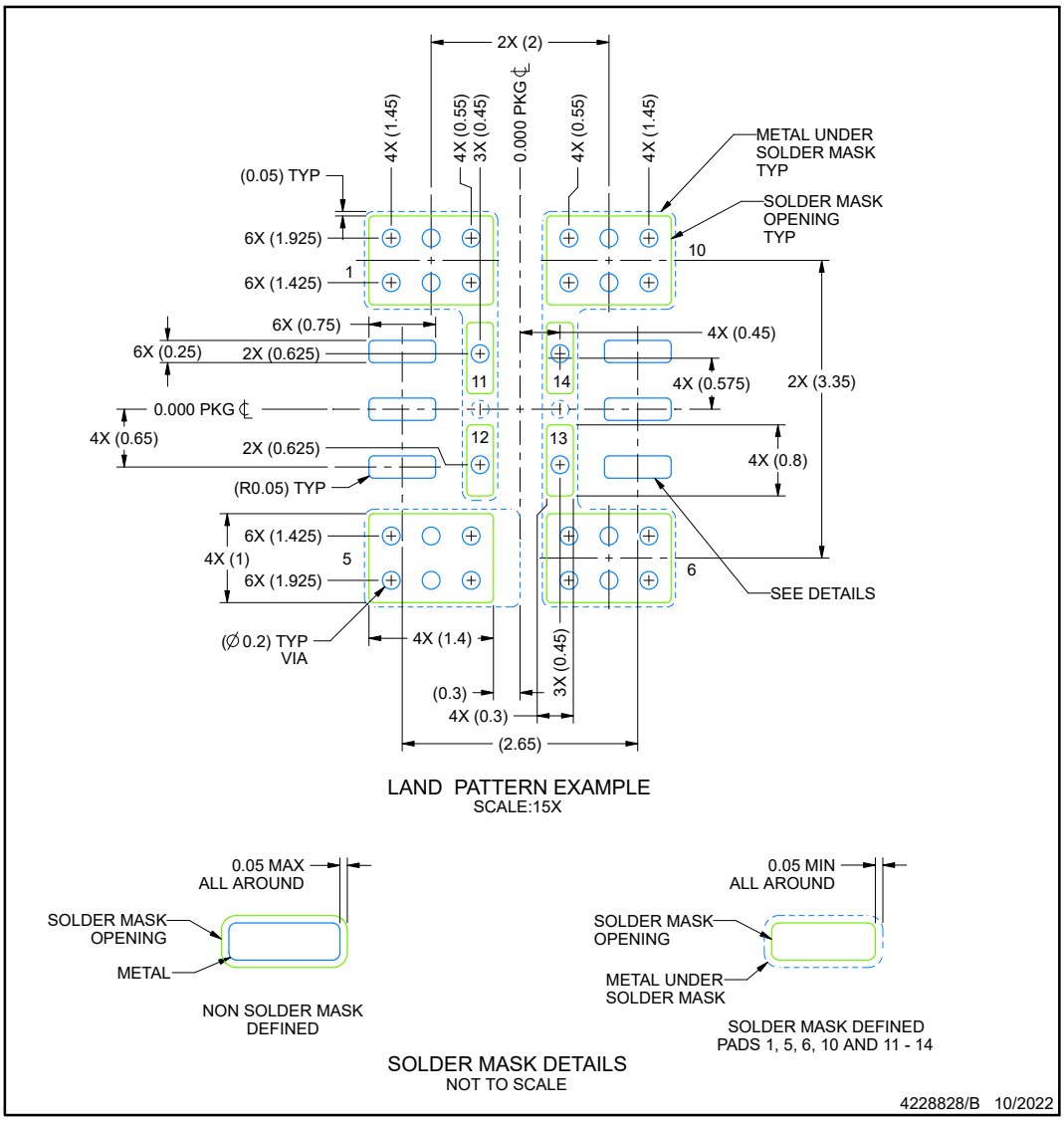
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EXAMPLE BOARD LAYOUT

SIE0014A-C01

uSIP™ - 1.6 mm max height

MICRO SYSTEM IN PACKAGE



NOTES: (continued)

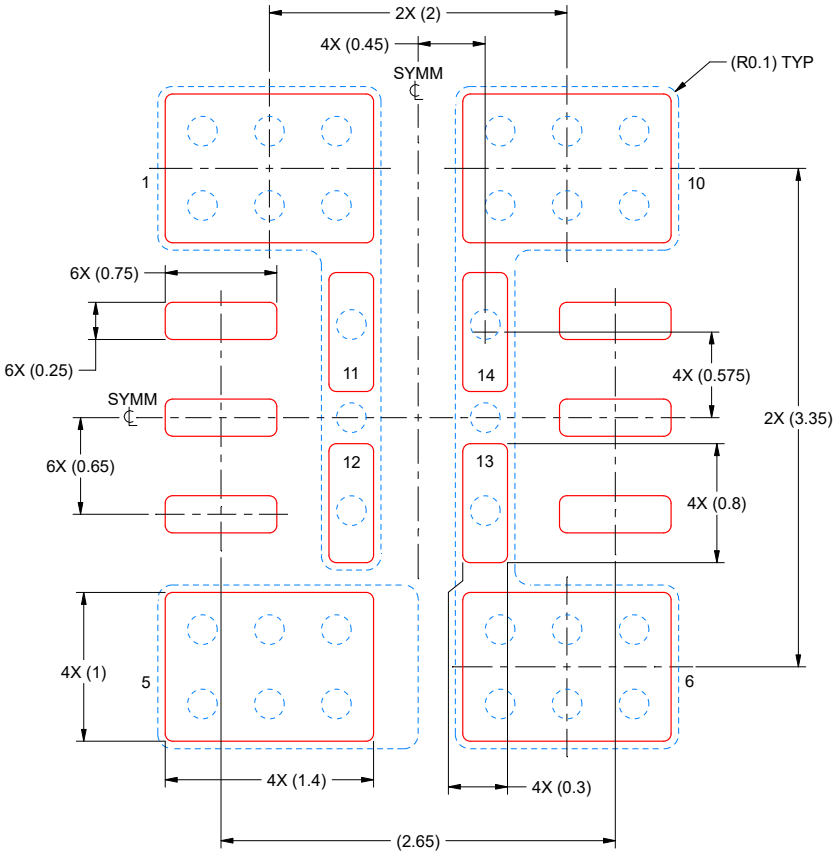
5. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

SIE0014A-C01 — **uSIP™ - 1.6 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM82816SIER	ACTIVE	uSiP	SIE	14	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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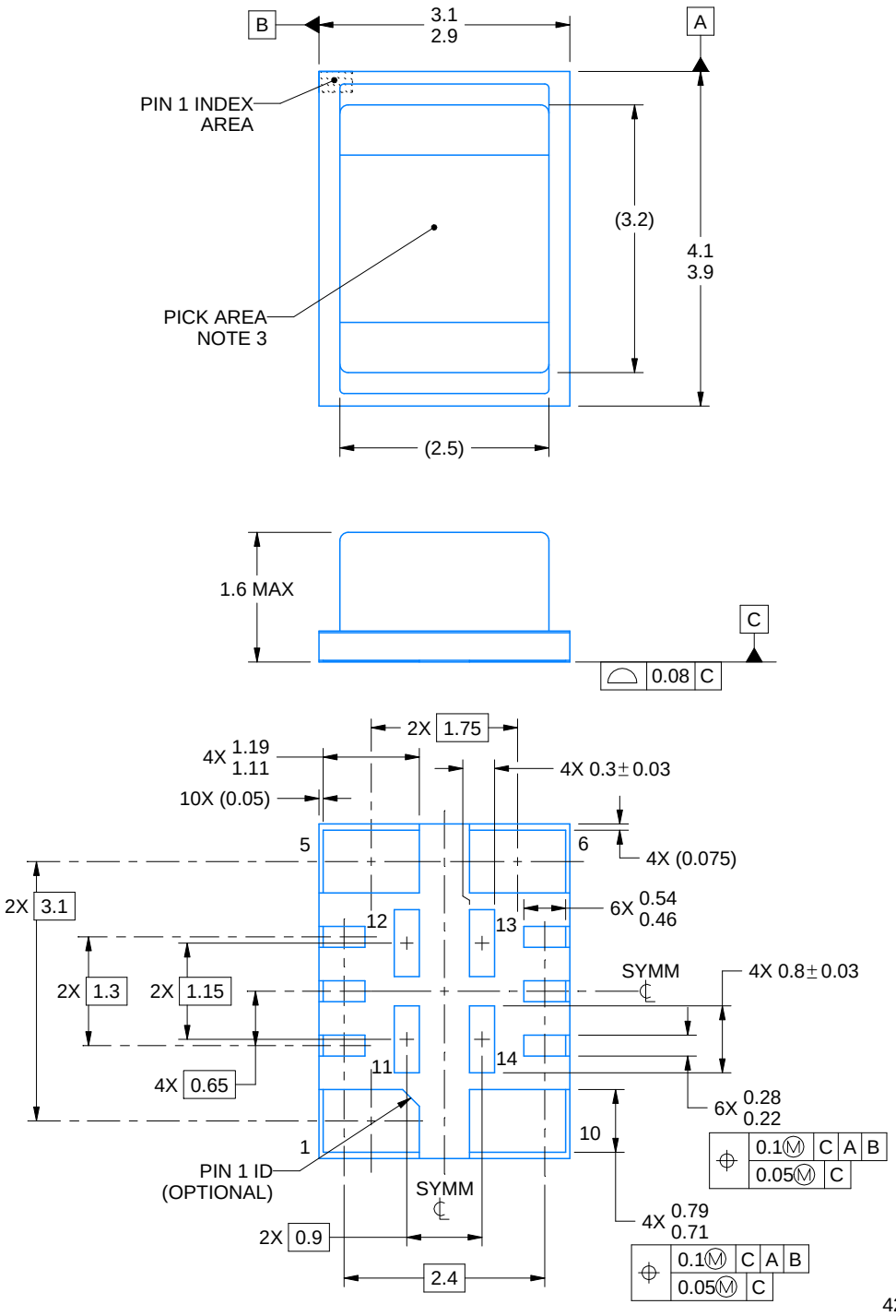
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

SIE0014A

uSIP™ - 1.6 mm max height

MICRO SYSTEM IN PACKAGE

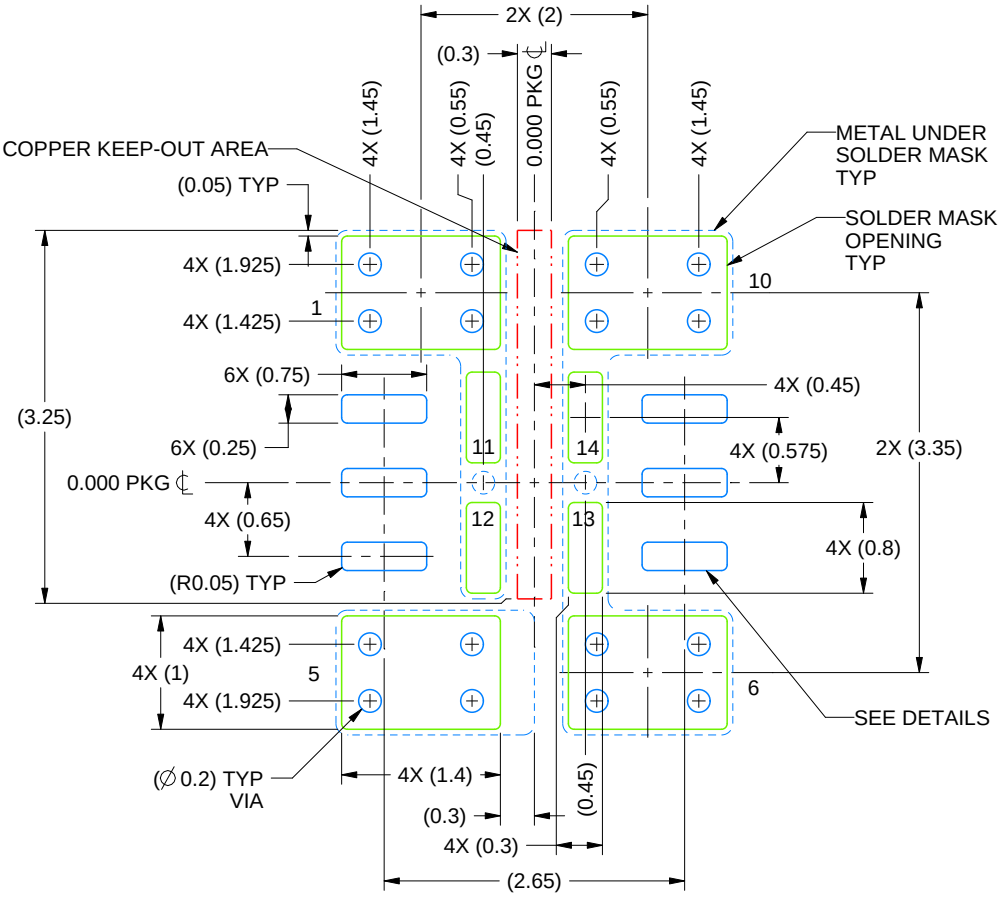


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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 1.3 mm or smaller recommended.
4. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

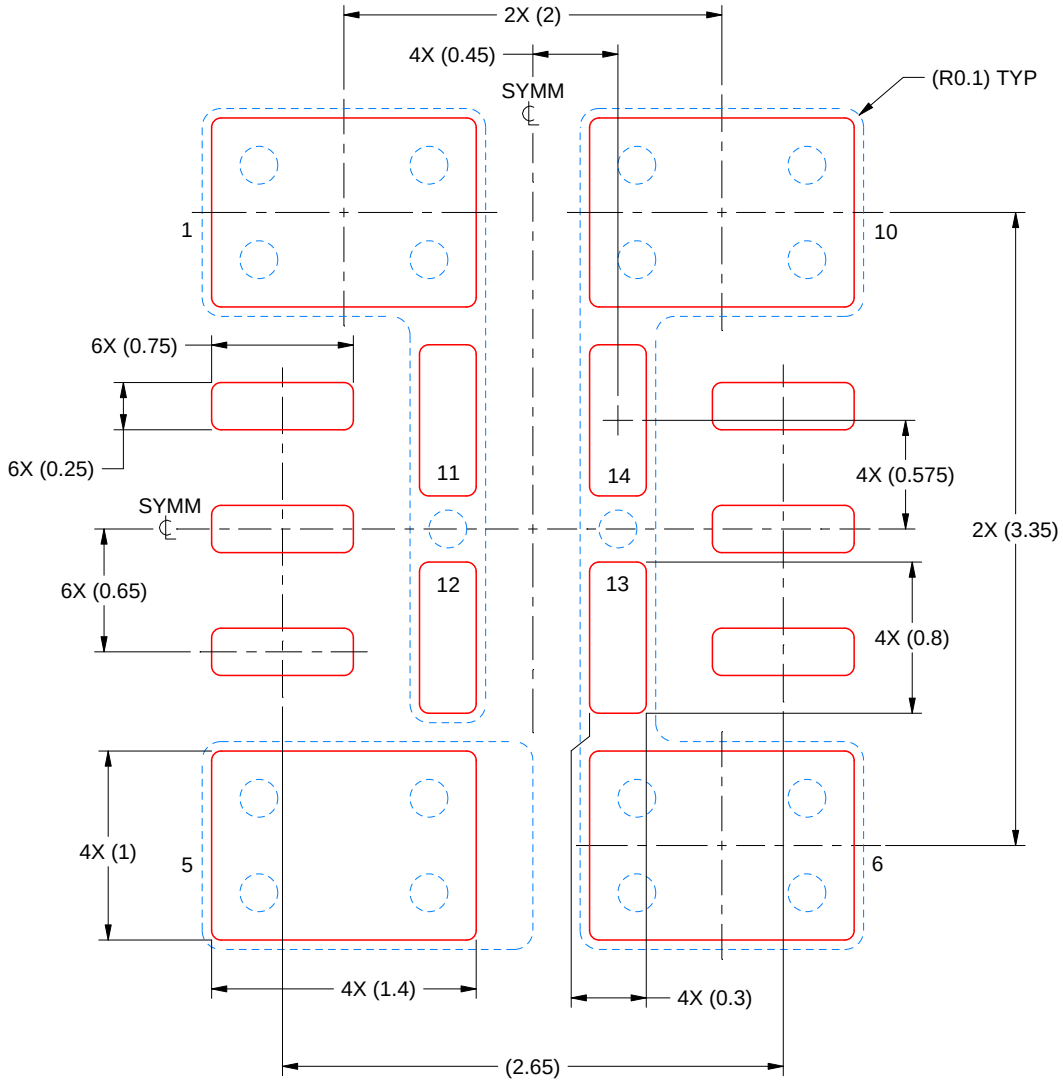


SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

5. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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