TPS8268x 1600mA 高效 MicroSiP™ 降压转换器模块（厚度 < 1.0mm）

1 特性

- 2.5V 至 5.5V 的宽 V_{IN} 范围
- 总体解决方案尺寸 < 6.7mm^2
- 厚度小于 1mm 的解决方案
- DC 电压精度为 ±1.5%
- 负载电流高达 1600mA
- 效率高达 88%
- 固定输出电压：
  - TPS8268150：1.50V
  - TPS8268105：1.05V
  - TPS8268090：0.9V
- 扩展频谱，PWM 频率抖动可降低电磁干扰 (EMI)
- *同类产品中最佳的*负载和线路瞬态响应
- 内部软启动
- 电流过载和热关断保护

2 应用

- 光模块
- 手机、智能电话
- 固态硬盘驱动应用
- 要求高效和极小解决方案尺寸的空间受限应用

3 说明

TPS8268x 器件是一款针对小型解决方案尺寸优化的完整 DC/DC 降压电源。 封装中包含开关稳压器、电感器和输入/输出电容器。 集成所有无源元件后仍属于微型尺寸解决方案，仅为 6.7mm^2。

TPS8268x 基于高频同步降压 dc-dc 转换器，它针对电池供电便携式应用进行了优化，此类应用要求极小的解决方案尺寸和厚度。 TPS8268x 针对高频和低输出电压纹波进行了优化，支持高达 1600mA 的负载电流。 该器件输入电压范围为 2.5V 到 5.5V，支持由锂离子电池及 5V 和 3.3V 电源供电的应用。

TPS8268x 开关频率为 5.5MHz，具有扩展频谱的功能。 对于噪声敏感应用，此特性可降低稳压输出的噪声，并降低输入噪声。 此器件支持固定输出电压，无需外部反馈网络。

凭借这些特性以及高 PSRR 和 AC 负载调节性能，此器件可以替代线性稳压器在相同尺寸条件下获得更高的功率转换效率。

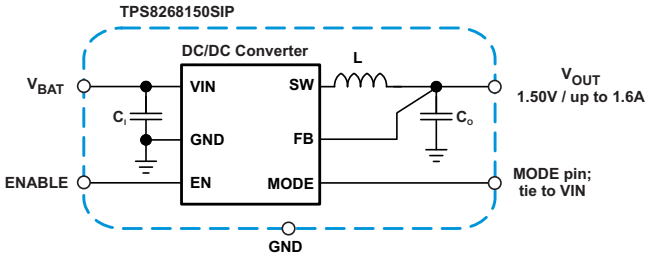
TPS8268x 采用紧凑的 (2.3mm x 2.9mm) 薄型 BGA 封装，适合通过标准表面贴装设备自动组装。

器件信息(1)

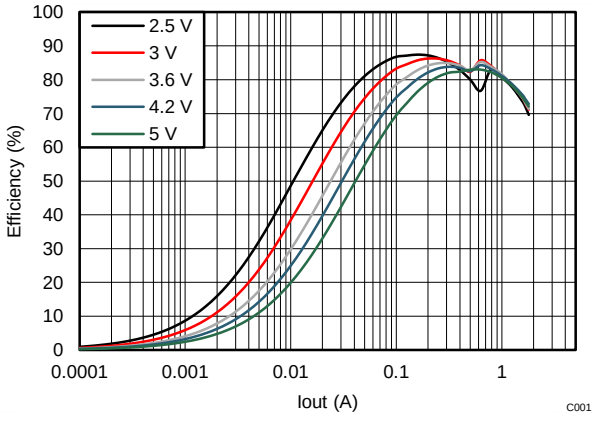
器件型号	封装	封装尺寸（标称值）
TPS8268150	µSIP	2.30mm x 2.90mm
TPS8268105	µSIP	2.30mm x 2.90mm
TPS8268090	µSIP	2.30mm x 2.90mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

典型应用



TPS8268150 的效率与负载电流间的关系



目录

4 修订历史记录

Changes from Original (October 2014) to Revision A **Page**

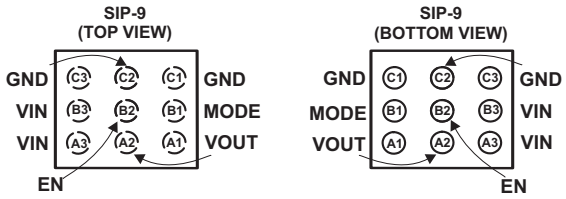
- 已更改 产品预览至生产数据 ... 1

5 Device Comparison Table (1)

DEVICE NUMBER	FEATURES	OUTPUT VOLTAGE	Marking
TPS8268150	PWM Spread Spectrum Modulation Output Capacitor Discharge	1.50V	YR
TPS8268105	PWM Spread Spectrum Modulation Output Capacitor Discharge	1.05V	YO
TPS8268090	PWM Spread Spectrum Modulation Output Capacitor Discharge	0.9V	YP

(1) For other voltage options please contact a TI sales representative.

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VOUT	A1, A2	O	Power output pin. Apply output load between this pin and GND.
VIN	A3, B3	I	Supply voltage connection
EN	B2	I	This is the enable pin of the device. Connecting this pin low forces the device into shutdown mode. Pulling this pin high enables the device. This pin must not be left floating and must be terminated.
MODE	B1	I	This pin must be tied to the input supply voltage VIN.
GND	C1, C2, C3	–	Ground pin.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_I	Voltage at VIN(2)	–0.3	6	V
	Voltage at VOUT(2)	–0.3	3.6	
	Voltage at EN, MODE(2)	–0.3	V_{IN} + 0.3	
	Peak output current		1600	mA
T_J	Operating internal junction temperature range	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	–55	125	°C
ESD rating (1) (2) (3)	Human body model	–2	2	kV
	Charge device model	–500	500	V
	Machine model	–100	100	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
VIN	Input voltage range		2.5		5.5	V
I_{OUT}	Peak output current for TPS8268090, TPS8268105	VIN ≥ 2.8V	0		1600(1)	mA
	Peak output current for TPS8268150	VIN ≥ 3.2V				
I_{OUT}	Average output current for TPS8268090, TPS8268105	VIN ≥ 2.7V	0		1200(1)	mA
	Average output current for TPS8268150	VIN ≥ 2.9V				
I_{OUT}	Average output current during soft-start	Vout ≤ 0.9 x $V_{OUT,nom}$	0		1000(1)	mA
	Additional effective input capacitance		0			µF
	Additional effective output capacitance		0		30(2)	µF
T_A	Operating ambient temperature range		–40		85	°C

(1) See Thermal and Reliability Information for additional details
(2) Due to the dc bias effect of ceramic capacitors, the effective capacitance is lower then the nominal value when a voltage is applied.

7.4 Thermal Information

THERMAL METRIC(1)		TPS8268x SIP 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22	
$R_{\theta JB}$	Junction-to-board thermal resistance	25	
ψ_{JT}	Junction-to-top characterization parameter	11	
ψ_{JB}	Junction-to-board characterization parameter	25	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	

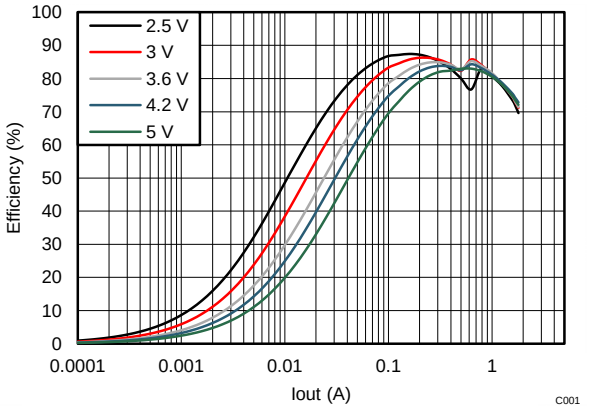
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Minimum and maximum values are at VIN = 2.5V to 5.5V, EN = VIN and T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at VIN = 3.6V, EN = VIN and T_A = 25°C (unless otherwise noted).

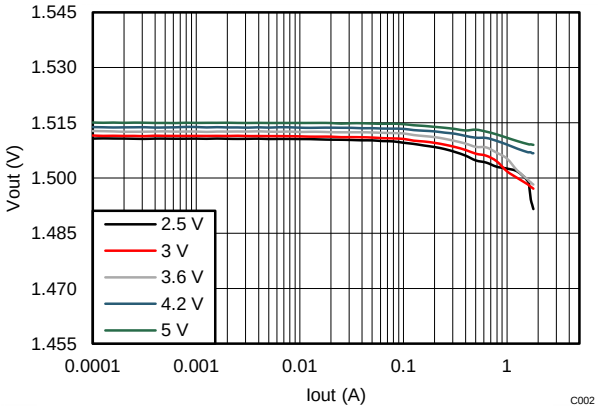
PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_Q	Operating quiescent current		I_{OUT} = 0mA		7		mA
I_{SD}	Shutdown current		EN = low		0.5	5	µA
UVLO	Undervoltage lockout threshold		VIN rising		2.1	2.3	V
			VIN falling		1.95	2.25	V
ENABLE, MODE							
V_{IH}	High-level input voltage			0.9			V
V_{IL}	Low-level input voltage					0.4	V
I_{lkg}	Input leakage current		Input connected to GND or VIN; T_J = –40°C to 85°C		0.01	1.5	µA
PROTECTION							
	Thermal shutdown		Temperature rising		140		°C
	Thermal shutdown hysteresis		Temperature falling		10		°C
I_{LIM}	Average output current limit				2100		mA
I_{SC}	Input current limit under short-circuit condition		V_{OUT} shorted to ground		150		mA
OUTPUT							
$V_{OUT,NOM}$	Nominal output voltage	TPS8268150			1.50		V
		TPS8268105			1.05		V
		TPS8268090			0.9		V
	Output voltage accuracy	TPS8268105, TPS8268090	2.8V ≤ VIN ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 1600 mA T_J = –40°C to 85°C	0.985×$V_{OUT,NOM}$	$V_{OUT,NOM}$	1.015×$V_{OUT,NOM}$	V
		TPS8268150	3.2V ≤ VIN ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 1600 mA T_J = –40°C to 85°C				
		TPS8268105, TPS8268090	2.7V ≤ VIN ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 1200 mA T_J = –40°C to 125°C	0.98×$V_{OUT,NOM}$	$V_{OUT,NOM}$	1.025×$V_{OUT,NOM}$	V
		TPS8268150	2.9V ≤ VIN ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 1200 mA T_J = –40°C to 125°C				
	Line regulation		VIN = 2.5V to 5.5V, I_{OUT} = 200 mA		0.2		%/V
	Load regulation		I_{OUT} = 0mA to 1600 mA		–0.85		%/A
f_{SW}	Nominal oscillator frequency		I_{OUT} = 0mA		5.5		MHz
	Start-up delay time		Time from EN = high to start switching		120	300	µs
t_{RAMP}	Ramp time		I_{OUT} = 0mA, Time from start switching until 95% of nominal output voltage		150		µs
R_{DIS}	VOUT discharge resistor				12		Ω

7.6 Typical Characteristics



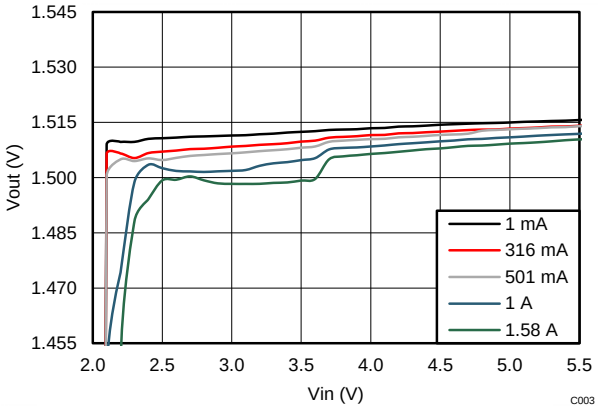
V_{OUT} = 1.50V 25°C

Figure 1. Efficiency vs Output Current



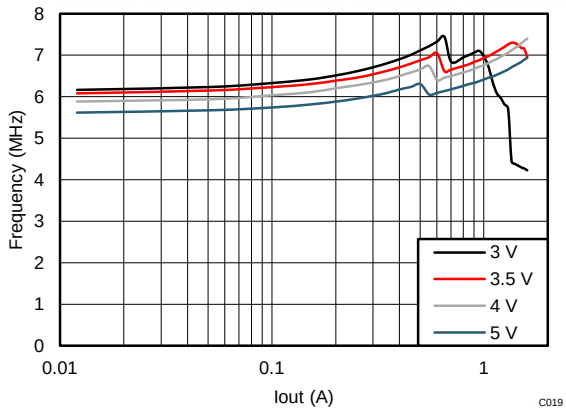
V_{OUT} = 1.50 V 25°C

Figure 2. Output Voltage vs Output Current



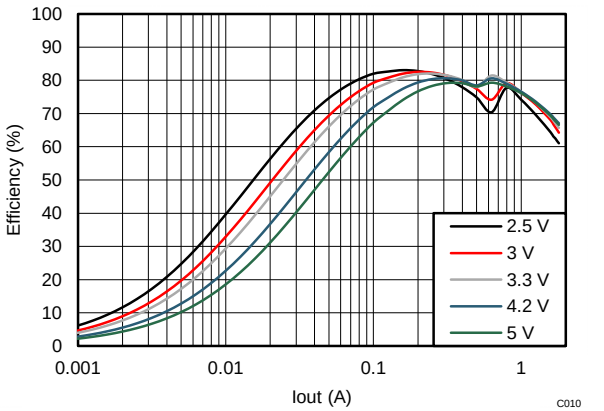
V_{OUT} = 1.50 V 25°C

Figure 3. Output Voltage vs Input Voltage



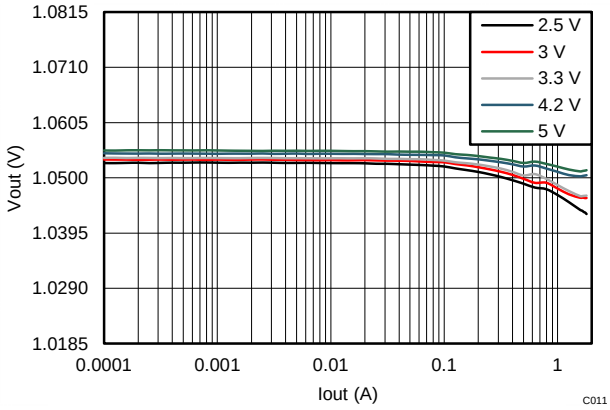
V_{OUT} = 1.50 V 25°C

Figure 4. Switching Frequency vs Output Current



V_{OUT} = 1.05V 25°C

Figure 5. Efficiency vs Output Current



V_{OUT} = 1.05 V 25°C

Figure 6. Output Voltage vs Output Current

Typical Characteristics (continued)

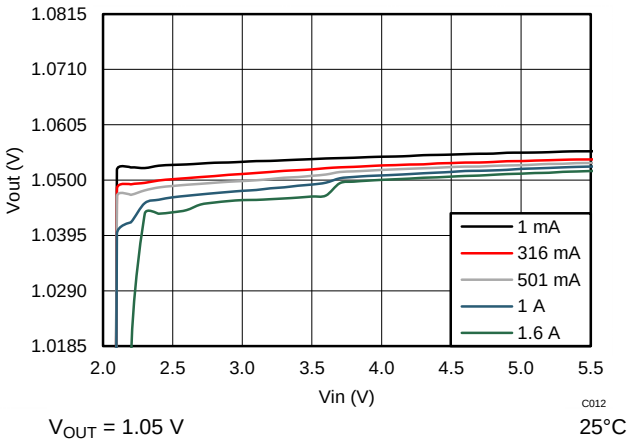


Figure 7. Output Voltage vs Input Voltage

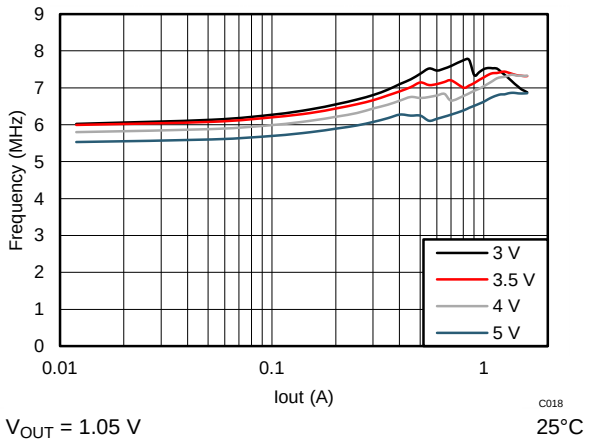


Figure 8. Switching Frequency vs Output Current

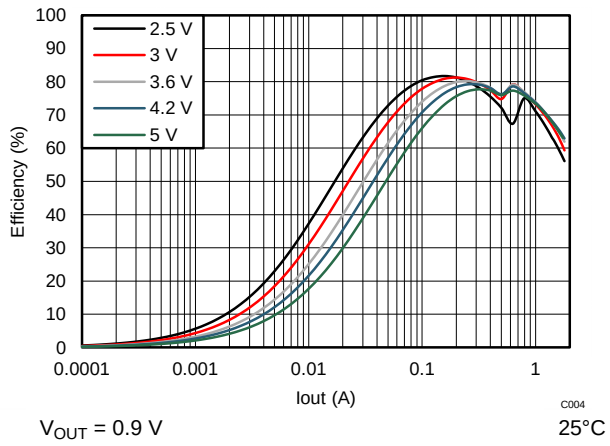


Figure 9. Efficiency vs Output Current

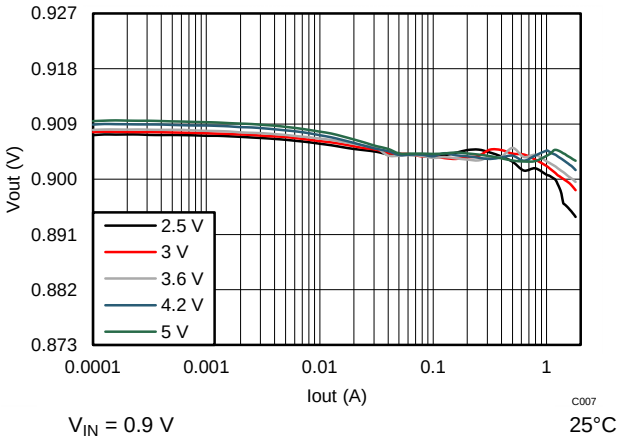


Figure 10. Output Voltage vs Output Current

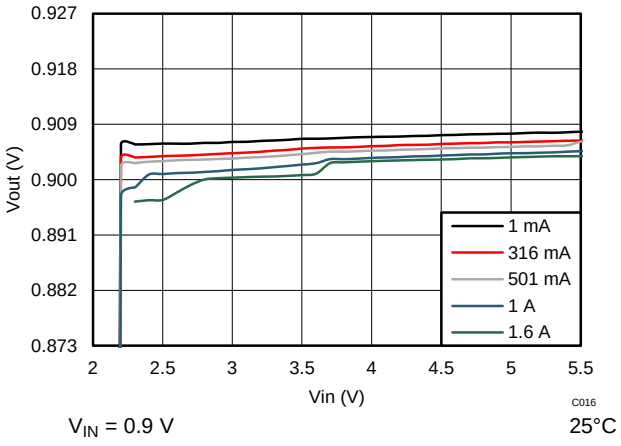


Figure 11. Output Voltage vs Input Voltage

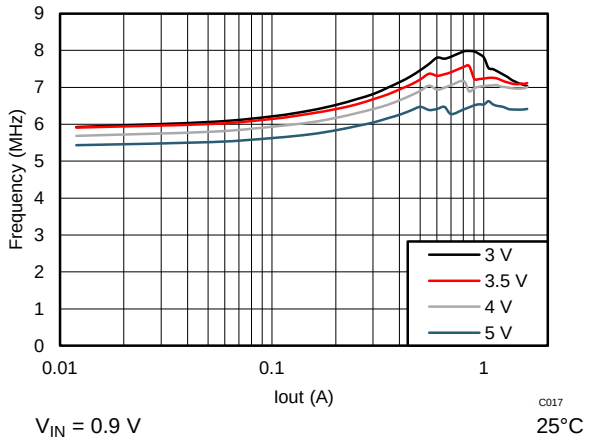
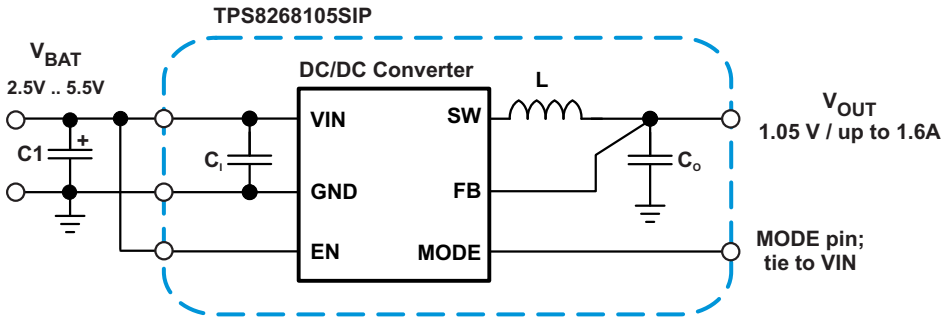


Figure 12. Switching Frequency vs Output Current

8 Parameter Measurement Information

8.1 Schematic



Reference	Description	Manufacturer
IC1	MicroSIP Module TPS8268xSIP	Texas Instruments
C1	Tantalum Capacitor; T520B157M006ATE025; 150uF/6.3V	Kemet

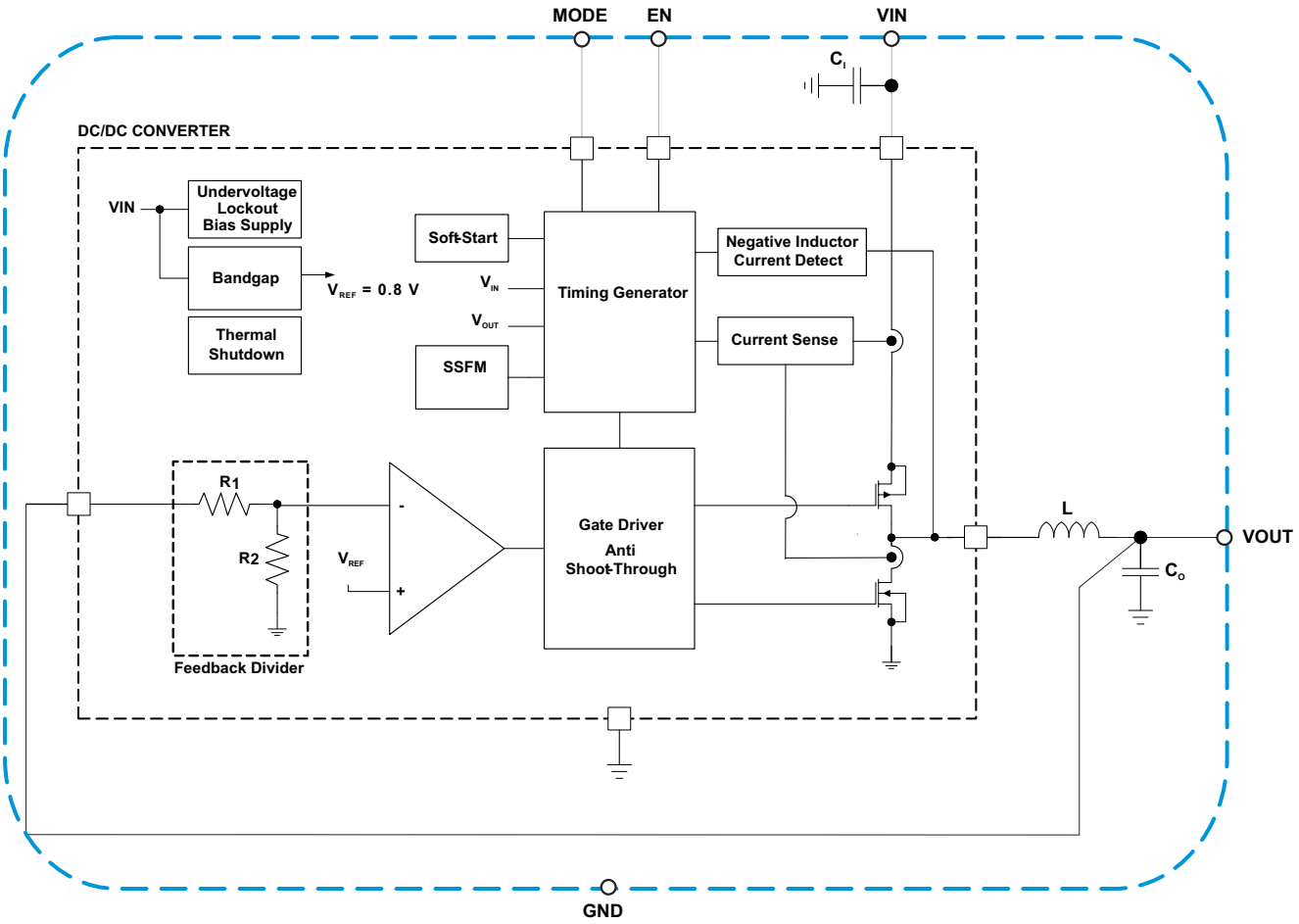
9 Detailed Description

9.1 Overview

The TPS8268x is a complete DC/DC step-down power supply intended for small size and low profile applications. Included in the package are the switching regulator, inductor and input/output capacitors. It is a complete Plug & Play Solution, meaning typically no additional components are required to finish the design. Integration of all required passive components enables a tiny solution size of only 6.7mm^2. The converter operates with fixed frequency pulse width modulation (PWM).

The TPS8268x integrates an input current limit to protect the device against heavy load or short circuits and features an undervoltage lockout circuit to prevent the device from misoperation at low input voltages.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Soft Start

The TPS8268x has an internal soft start circuit that controls the ramp up of the output voltage. Once the converter is enabled and the input voltage is above the undervoltage lockout threshold V_{UVLO}, the output voltage ramps up to 95% of its nominal value within t_{Ramp} of typ. 150µs. This ensures a controlled ramp up of the output voltage and limits the input voltage drop when a battery or a high-impedance power source is connected to the input of the DC/DC converter.

The inrush current during start-up is directly related to the effective capacitance and load present at the output of the converter.

Feature Description (continued)

During soft start, the current limit is reduced to 2/3 of its nominal value. The maximum load current during soft start should be less than 1A. Once the internal reference voltage has reached 90% of its target value, the current limit is set to its nominal target value.

9.3.2 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from misoperation at low input voltages. It prevents the converter from turning on either MOSFET under undefined conditions. The TPS8268x has a rising UVLO threshold of 2.1V (typical).

9.3.3 Short-Circuit Protection

The TPS8268x integrates current limit circuitry to protect the device against heavy load or short circuits. When the average current in the high-side MOSFET reaches its current limit, the high-side MOSFET is turned off and the low-side MOSFET is turned on ramping down the inductor current.

As soon as the converter detects a short circuit condition, it shuts down. After a delay of approximately 20 µs, the converter restarts. In case the short circuit condition remains, the converter shuts down again after hitting the current limit threshold. In case the short circuit condition remains present on the converters output, the converter periodically re-starts with a small duty cycle and shuts down again, thereby limiting the current drawn from the input.

9.3.4 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds typically 140°C, the device goes into thermal shutdown. In this mode, the power stage is turned off. The device continues its operation when the junction temperature falls below typically 130°C.

9.3.5 Enable

The TPS8268x device starts operation when EN is set high. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device into shutdown, with a shutdown current of typically 0.5µA. In this mode, the internal high-side and low-side MOSFETs are turned off, the internal resistor feedback divider is disconnected, and the entire internal control circuitry is switched off. The TPS8268x device actively discharges the output capacitor when it turns off. The integrated discharge resistor has a typical resistance of 12Ω. This internal discharge transistor is only turned on after the device had been enabled at least once. The required time to discharge the output capacitor at the output node depends on load current and the effective output capacitance.

The TPS8268x is designed such that it can start into a pre-biased output, in case the output discharge circuit was active for too short a time to fully discharge the output capacitor. In this case, the converter starts switching as soon as the internal reference has approximately reached the equivalent voltage to the output voltage present. It then ramps the output from that voltage level to its target value.

9.3.6 MODE Pin

This pin must be tied to the input voltage VIN and must not be left floating.

9.4 Device Functional Modes

9.4.1 Spread Spectrum, PWM Frequency Dithering

The goal is to spread out the emitted RF energy over a larger frequency range, so that the resulting EMI is similar to white noise. The end result is a spectrum that is continuous and lower in peak amplitude, making it easier to comply with electromagnetic interference (EMI) standards and with power supply ripple requirements in cellular and non-cellular wireless applications. Radio receivers are typically susceptible to narrowband noise that is focused on specific frequencies.

Device Functional Modes (continued)

Switching regulators can be particularly troublesome in applications where electromagnetic interference (EMI) is a concern. Switching regulators operate on a cycle-by-cycle basis to transfer power to their output. In most cases, the frequency of operation is either fixed or regulated, based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

The spread spectrum architecture varies the switching frequency by around ±10% of the nominal switching frequency, thereby significantly reducing the peak radiated and conducted noise on both the input and output supplies. The frequency dithering scheme is modulated with a triangle profile and a modulation frequency f_m.

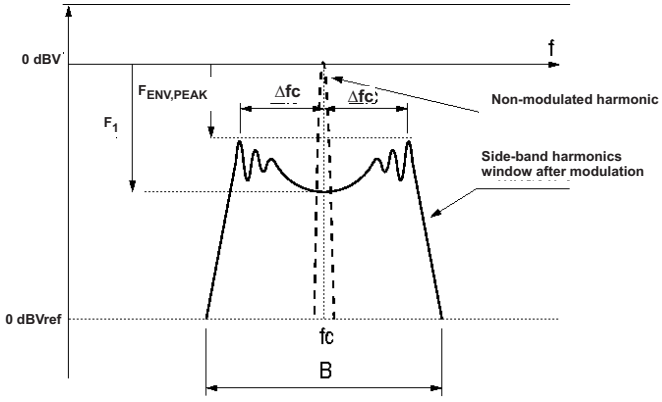


Figure 13. Spectrum Of A Frequency Modulated Sin. Wave With Sinusoidal Variation In Time

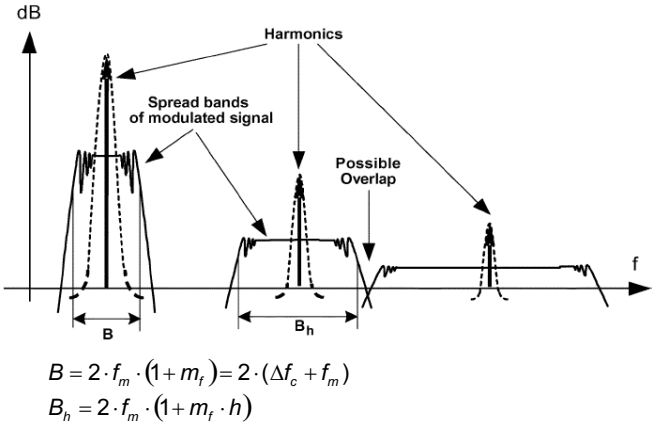


Figure 14. Spread Bands Of Harmonics In Modulated Square Signals (1)

The above figures show that after modulation the side-band harmonic is attenuated compared to the non-modulated harmonic, and the harmonic energy is spread into a certain frequency band. The higher the modulation index (m_f), the larger the attenuation.

$$m_f = \frac{\delta \times f_c}{f_m} \tag{1}$$

where:

- f_c is the carrier frequency (5.5MHz)
- f_m is the modulating frequency (approx. 0.008*f_c)
- δ is the modulation ratio (approx 0.1)

$$\delta = \frac{\Delta f_c}{f_c} \tag{2}$$

The maximum switching frequency f_c is limited by the device and finally the parameter modulation ratio (δ), together with f_m , which is the side-band harmonic´s bandwidth around the carrier frequency f_c . The bandwidth of a frequency modulated waveform is approximately given by Carson's rule and is summarized as:

$$B = 2 \times f_m \times (1 + m_f) = 2 \times (\Delta f_c + f_m) \tag{3}$$

f_m < RBW (resolution bandwidth): The receiver is not able to distinguish individual side-band harmonics, so, several harmonics are added in the input filter and the measured value is higher than expected in theoretical calculations.

f_m > RBW: The receiver is able to properly measure each individual side-band harmonic separately, so the measurements match with the theoretical calculations.

(1) Spectrum illustrations and formulae (Figure 13 and Figure 14) copyright *IEEE TRANSACTIONS ON ELECTROMAGNETIC COMPATIBILITY*, VOL. 47, NO.3, AUGUST 2005. See References Section for full citation.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS8268x device is a complete DC/DC step-down power supply optimized for small solution size. Included in the package are the switching regulator, inductor and input/output capacitors. Integration of passive components enables a tiny solution size of only 6.7mm^2.

10.2 Typical Application

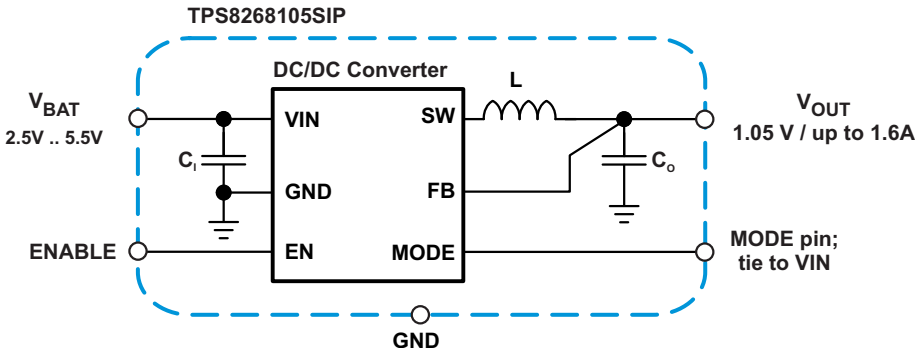


Figure 15. Typical Application Schematic

10.2.1 Design Requirements

Figure 15 shows the schematic of the typical application. The following design guidelines provide all information to operate the device within the recommended operating conditions.

10.2.2 Detailed Design Procedure

The TPS8268x allows the design of a complete power supply with no additional external components. The input capacitance can be increased in case the source impedance is large or if there are high load transients expected at the output. The dc bias effect of the input and output capacitors must be taken into account and the total capacitance on the output must not exceed the value given in the recommended operating conditions.

10.2.2.1 Input Capacitor Selection

Because the nature of the buck converter has a pulsating input current, a low ESR input capacitor is required.

For most applications, the input capacitor that is integrated into the TPS8268x is sufficient. If the application exhibits a noisy or erratic switching frequency, experiment with additional input ceramic capacitance to find a remedy.

The TPS8268x uses a tiny ceramic input capacitor. When a ceramic capacitor is combined with trace or cable inductance, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part. In this circumstance, additional "bulk" capacitance, such as electrolytic or tantalum, should be placed between the input of the converter and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_I.

Typical Application (continued)

10.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the TPS8268x allows the use of tiny ceramic output capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. For most applications, the output capacitor integrated in the TPS8268x is sufficient. An additional output capacitor may be used for the purpose of improving AC voltage accuracy during large load transients.

To further reduce the voltage drop during load transients, additional external output capacitance up to 30µF can be added. A low ESR multilayer ceramic capacitor (MLCC) is suitable for most applications. The total effective output capacitance must remain below 30µF.

As the device operates in PWM mode, the overall output voltage ripple is the sum of the voltage step that is caused by the output capacitor´s ESL and the ripple current that flows through the output capacitor´s impedance.

Because the damping factor in the output path is directly related to several resistive parameters (e.g. inductor DCR, power-stage $r_{DS(on)}$, PCB DC resistance, load switches $r_{DS(on)}$ …) that are temperature dependant, the converter´s small and large signal behavior should be checked over the input voltage range, load current range and temperature range.

The easiest test is to evaluate, directly at the converter's output, the following items:

- efficiency
- load transient response
- output voltage ripple

During the recovery time from a load transient, the output voltage can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop typically has more than 45° of phase margin.

10.2.3 Application Curves

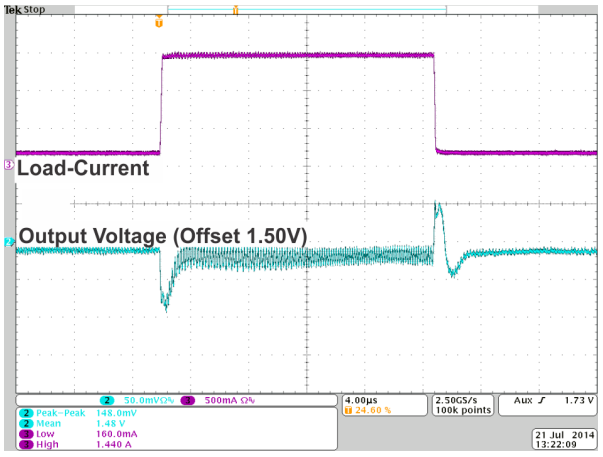


Figure 16. Load Transient Response for TPS8268150 (Vout = 1.5V, Iout = 160mA to 1.44A to 160mA, Vin = 5V)

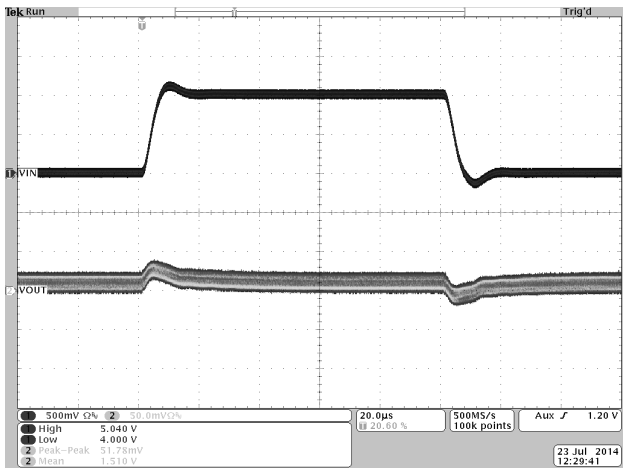


Figure 17. Line Transient Response for TPS8268150 (Vout = 1.5V, Iout = 800mA, Vin = 4V to 5V to 4V)

Typical Application (continued)

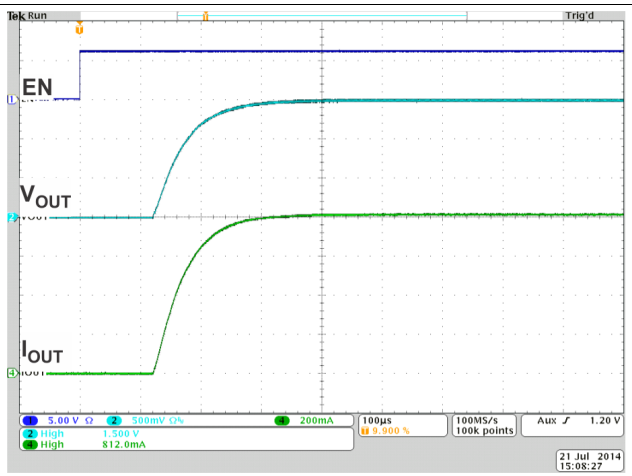


Figure 18. Startup for TPS8268150 (Vin = 5V, Vout = 1.5V)

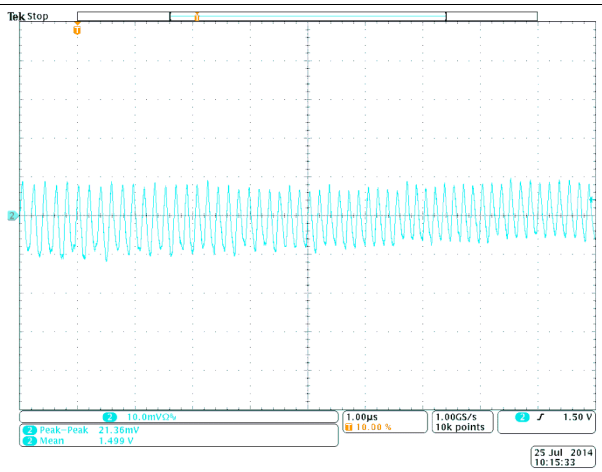


Figure 19. Output Voltage Ripple for TPS8268150 (Vin = 5V, Vout = 1.5V, Iout = 900mA)

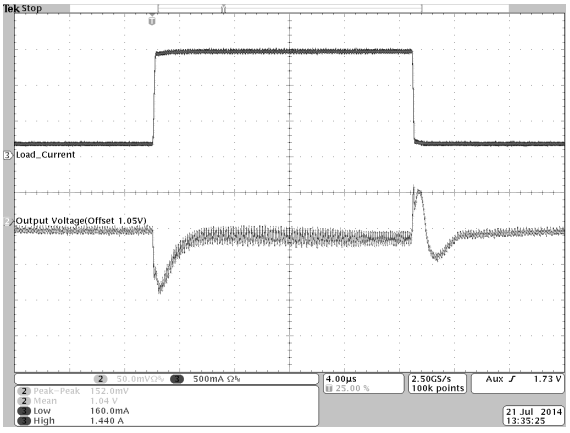


Figure 20. Load Transient Response for TPS8268105 (Vout = 1.05V, Iout = 160mA to 1.44A to 160mA, Vin = 5V)

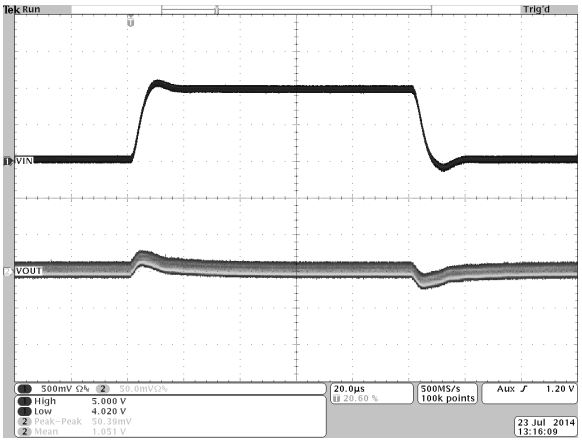


Figure 21. Line Transient Response for TPS8268105 (Vout = 1.05V; Iout = 900mA, Vin = 4V to 5V to 4V)

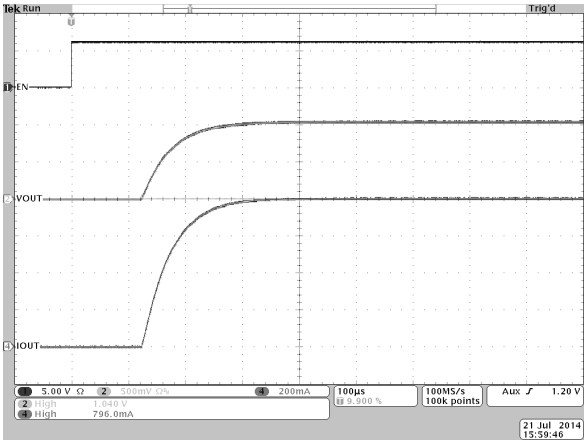


Figure 22. Startup for TPS8268105 (Vin = 5V, Vout = 1.05V)

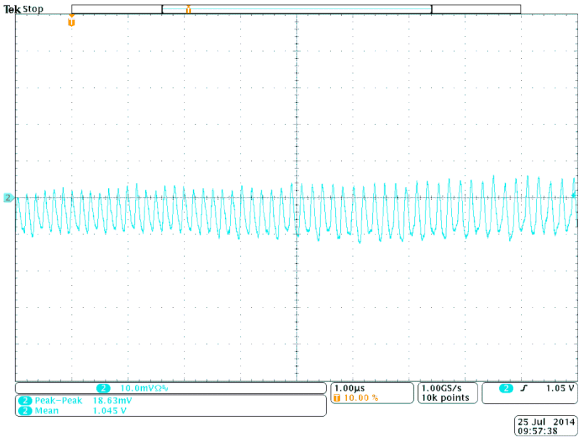


Figure 23. Output Voltage Ripple for TPS8268105 (Vin = 5V, Vout = 1.05V, Iout = 900mA)

Typical Application (continued)

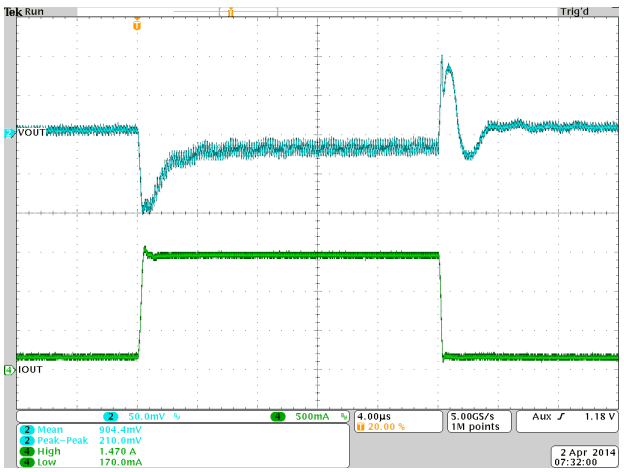


Figure 24. Load Transient Response for TPS8268090 (Vout = 0.9V, Iout = 170mA to 1.47A to 170mA, Vin = 5V)

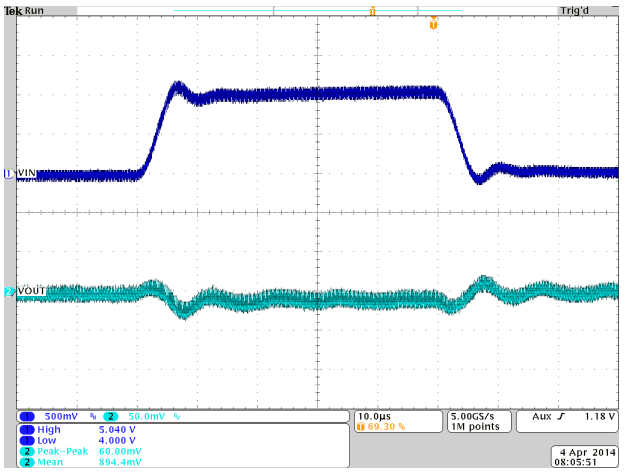


Figure 25. Line Transient Response for TPS8268090 (Vout = 0.90V; Iout = 900mA, Vin = 4V to 5V to 4V)

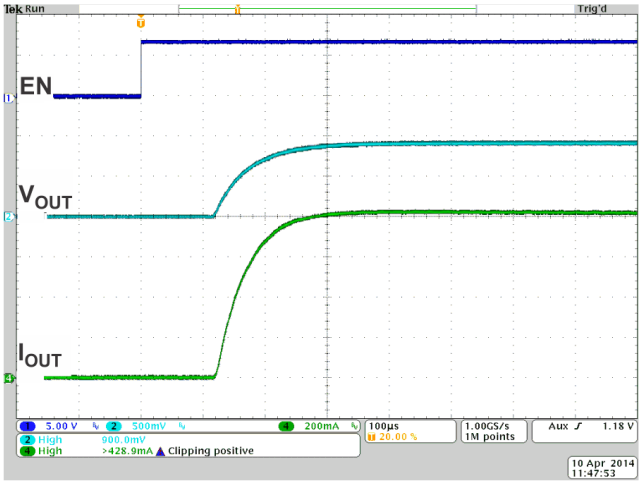


Figure 26. Startup for TPS8268090 (Vin = 5V, Vout = 0.9V)

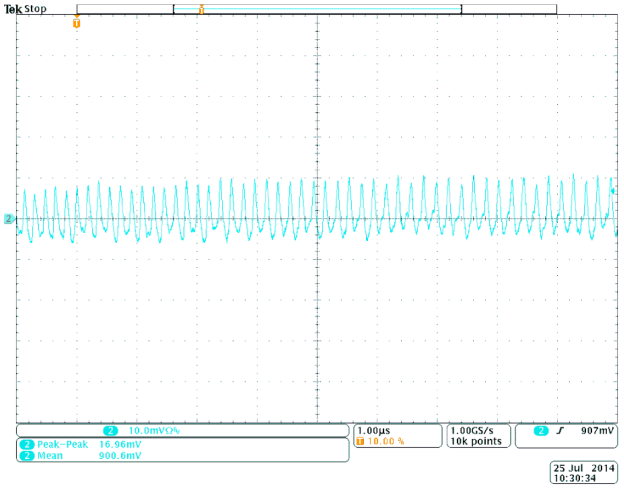


Figure 27. Output Voltage Ripple for TPS8268090 (Vin = 5V, Vout = 0.9V, Iout = 900mA)

11 Power Supply Recommendations

The TPS8268x has no special requirements for its input power supply. The input power supply to the TPS8268x must have a current rating according to the supply voltage and output current of the TPS8268x.

12 Layout

12.1 Layout Guidelines

TPS8268x allows the design of a power supply with small solution size. In order to properly dissipate the heat, wide copper traces for the power connections should be used to distribute the heat across the PCB. If possible, a GND plane should be used as it provides a low impedance connection as well as serves as a heat sink.

In making the pad size for the SiP LGA balls, it is recommended that the layout use a non-solder-mask defined (NSMD) land. With this method, the solder mask opening is made larger than the desired land area, and the opening size is defined by the copper pad width. Figure 28 shows the appropriate diameters for a MicroSiP™ layout.

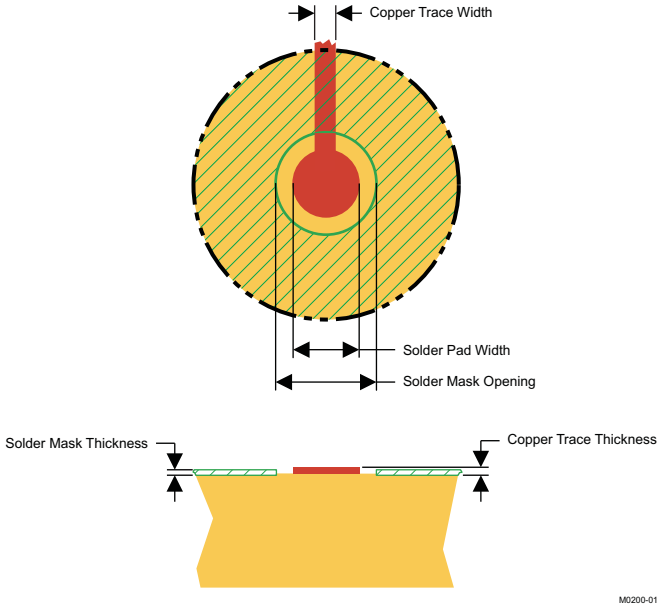


Figure 28. Recommended Land Pattern Image and Dimensions

SOLDER PAD DEFINITIONS (1)(2)(3)(4)	COPPER PAD	SOLDER MASK (5) OPENING	COPPER THICKNESS	STENCIL (6) OPENING	STENCIL THICKNESS
Non-solder-mask defined (NSMD)	0.30mm	0.360mm	1oz max (0.032mm)	0.34mm diameter	0.1mm thick

(1) Circuit traces from non-solder-mask defined PCB lands should be 75µm to 100µm wide in the exposed area inside the solder mask opening. Wider trace widths reduce device stand off and slightly reduce reliability. However, wider traces may be used to improve the thermal relief of the device as well as to provide sufficient current handling.
(2) Best reliability results are achieved when the PCB laminate glass transition temperature is above the operating the range of the intended application.
(3) Recommend solder paste is Type 3 or Type 4.
(4) For a PCB using a Ni/Au surface finish, the gold thickness should be less than 0.5mm to avoid a reduction in thermal fatigue performance.
(5) Solder mask thickness should be less than 20 µm on top of the copper circuit pattern.
(6) For best solder stencil performance use laser cut stencils with electro polishing. Chemically etched stencils give inferior solder paste volume control.

12.2 Layout Example

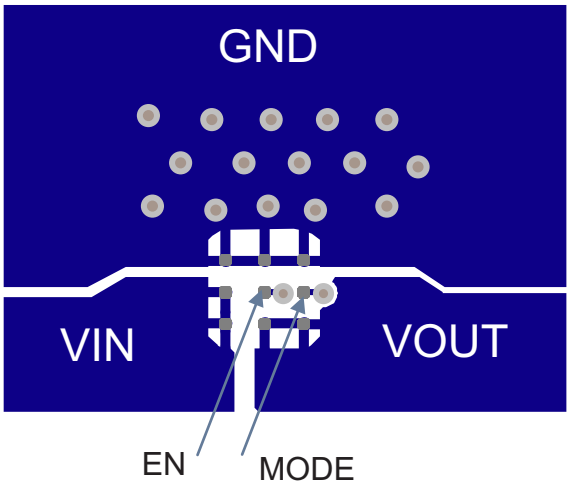


Figure 29. Recommended PCB Layout

12.3 Surface Mount Information

The TPS8268x MicroSiP™ DC/DC converter uses an open frame construction that is designed for a fully automated assembly process and that features a large surface area for pick and place operations. See the "Pick Area" in the package drawings.

Package height and weight have been kept to a minimum to allow the MicroSiP™ device to be handled similarly to a 0805 component.

See JEDEC/IPC standard J-STD-20b for reflow recommendations.

12.4 Thermal and Reliability Information

The TPS8268x´s output current may need to be de-rated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. The amount of current de-rating is dependent upon the input voltage, output power and environmental thermal conditions. Care should especially be taken in applications where the localized PCB temperature exceeds 65°C.

The TPS8268x die and inductor temperature should be kept lower than the maximum rating of 125°C, so care should be taken in the circuit layout to ensure good heat sinking. Sufficient cooling should be provided to ensure reliable operation.

Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the junction temperature, approximate the power dissipation within the TPS8268x by applying the typical efficiency stated in this datasheet to the desired output power; or, by taking an actual power measurement. Then, calculate the internal temperature rise of the TPS8268x above the surface of the printed circuit board by multiplying the TPS8268x´s power dissipation by its thermal resistance.

The thermal resistance numbers listed in the Thermal Information table are based on modeling the MicroSiP™ package mounted on a high-K test board specified per the JEDEC standard. For increased accuracy and fidelity to the actual application, it is recommended to run a thermal image analysis of the actual system.

Thermal measurements have been taken on the EVM to give a guideline on what temperature can be expected when the device is operated in free air at 25°C ambient under a certain load. The temperatures have been checked at 4 different spots as listed below:

- Spot1: temperature of the input capacitor
- Spot2: temperature of the output capacitor
- Spot3: temperature of the inductor
- Spot4: temperature on the main pcb next to the module

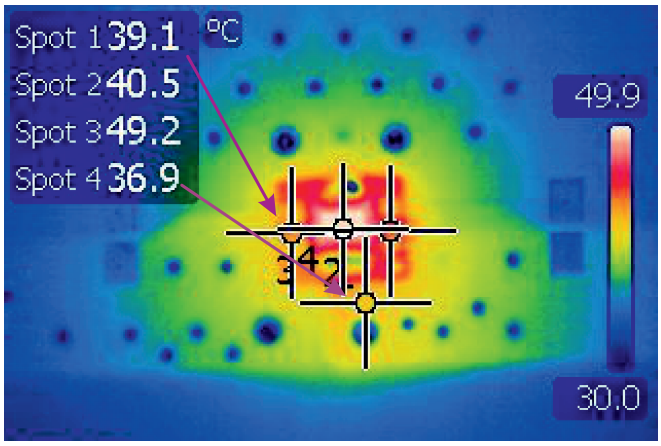


Figure 30. V_{IN}= 5V, V_{OUT}=1.05V, I_{OUT}= 1A 388mW Power Dissipation

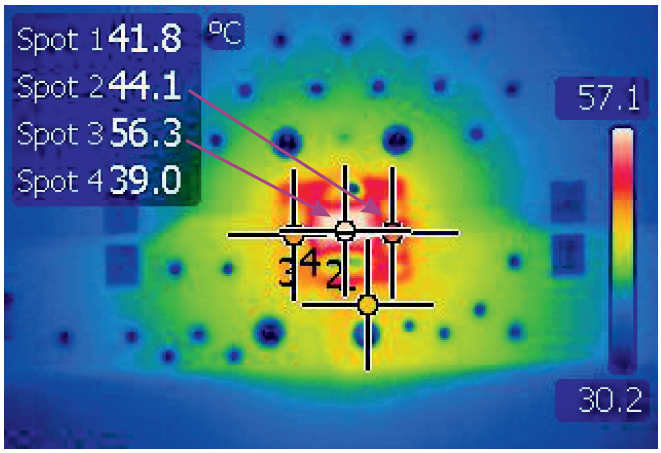


Figure 31. V_{IN}= 5V, V_{OUT}= 1.05V, I_{OUT}= 1.2A 466mW Power Dissipation

The TPS8268x contains a thermal shutdown that inhibits switching at high junction temperatures. The activation threshold of this function, however, is above 125°C to avoid interfering with normal operation. Thus, prolonged or repetitive operation under a condition in which the thermal shutdown activates necessarily means that the components internal to the MicroSiP™ package are subjected to high temperatures for prolonged or repetitive intervals, which may decrease the reliability of the device.

Thermal and Reliability Information (continued)

MLCC capacitor reliability/lifetime depends on temperature and applied voltage. At higher temperatures, MLCC capacitors are subject to stronger stress. On the basis of frequently evaluated failure rates determined with standardized test conditions, the reliability of all MLCC capacitors can be calculated for their actual operating temperature and voltage.

Failures caused by systematic degradation are described by the Arrhenius model. The most critical parameter (IR) is the Insulation Resistance (i.e. leakage current). The drop of IR below a lower limit (e.g. 1 MΩ) is used as the failure criterion. See Figure 32 and Figure 33. Note that the wear-out mechanisms occurring in the MLCC capacitors are not reversible but cumulative over time.

Input Capacitor Lifetime vs Temperature and Voltage

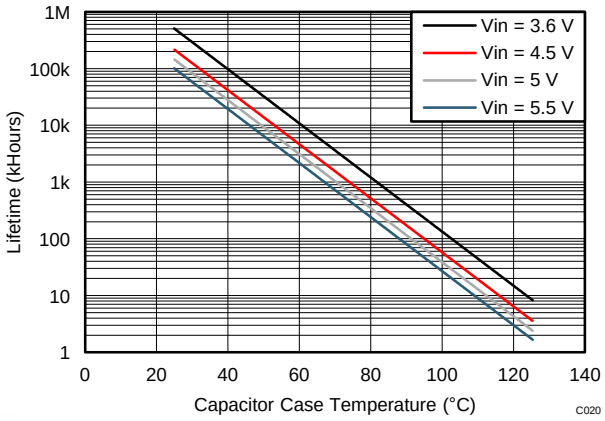


Figure 32. Input Capacitor Lifetime

Output Capacitor Lifetime vs Temperature and Voltage

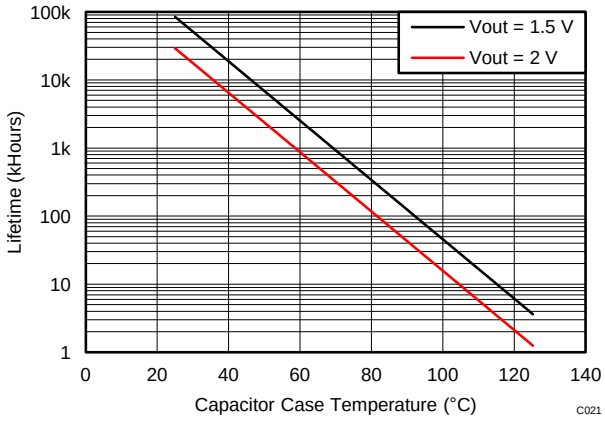


Figure 33. Output Capacitor Lifetime

13 器件和文档支持

13.1 文档支持

13.1.1 参考书目

“使用频率调制技术的开关电源转换器中的电磁干扰 (EMI) 减少”，*《电气与电子工程师协会 (IEEE) 电磁兼容性汇刊》，卷4，NO.3，2005 年 8 月，第 569-576 页* 作者 Josep Balcells，Alfonso Santolaria，Antonio Orlandi，David González，Javier Gago。

13.2 相关链接

以下表格列出了快速访问链接。 范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **1.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS8268150	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS8268105	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS8268090	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.3 商标

MicroSiP is a trademark of Texas Instruments.

13.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.5 术语表

SLYZ022 — *TI 术语表*。

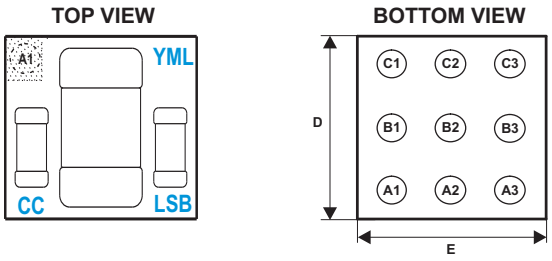
这份术语表列出并解释术语、首字母缩略词和定义。

14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

14.1 封装概要

SIP 封装



代码：

- CC - 客户代码（特定器件/电压）
- YML—Y：年，M：月，L：批次跟踪码
- LSB—L：批次跟踪码，S：地点代码，B：主板定位器

14.2 MicroSiP™ DC/DC 模块封装尺寸

TPS8268x 采用 9 凸点球状引脚栅格阵列 (BGA) 封装。 封装尺寸为：

- D = 2.30 ± 0.05mm
- E = 2.90 ± 0.05mm

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS8268090SIPR	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YP
TPS8268090SIPT	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YP
TPS8268090SIPT.B	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 125	YP
TPS8268105SIPR	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YO
TPS8268105SIPT	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YO
TPS8268150SIPR	Active	Production	uSiP (SIP) | 9	3000 | LARGE T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YR
TPS8268150SIPT	Active	Production	uSiP (SIP) | 9	250 | SMALL T&R	Yes	SNAGCU	Level-2-260C-1 YEAR	-40 to 85	YR

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

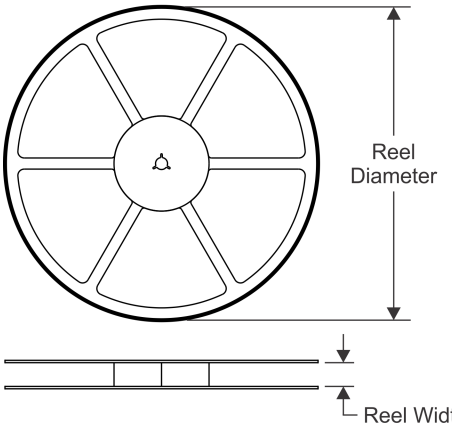
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

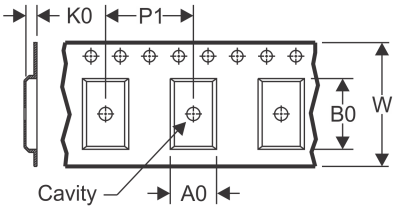
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

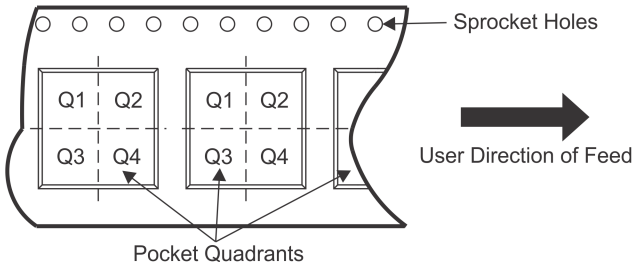


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

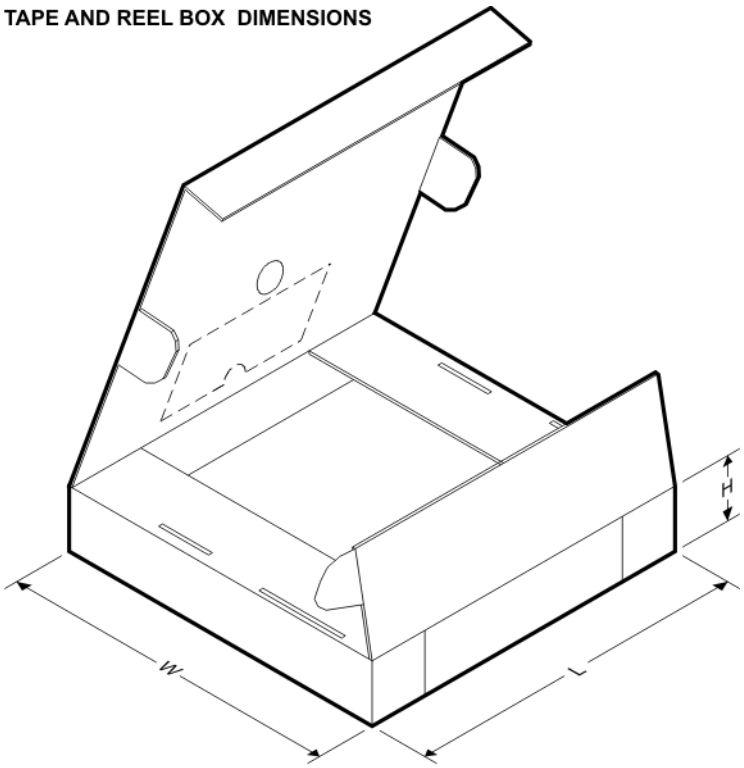
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS8268090SIPR	uSiP	SIP	9	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268090SIPT	uSiP	SIP	9	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268105SIPR	uSiP	SIP	9	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268105SIPT	uSiP	SIP	9	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268150SIPR	uSiP	SIP	9	3000	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2
TPS8268150SIPT	uSiP	SIP	9	250	178.0	9.0	2.45	3.05	1.1	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

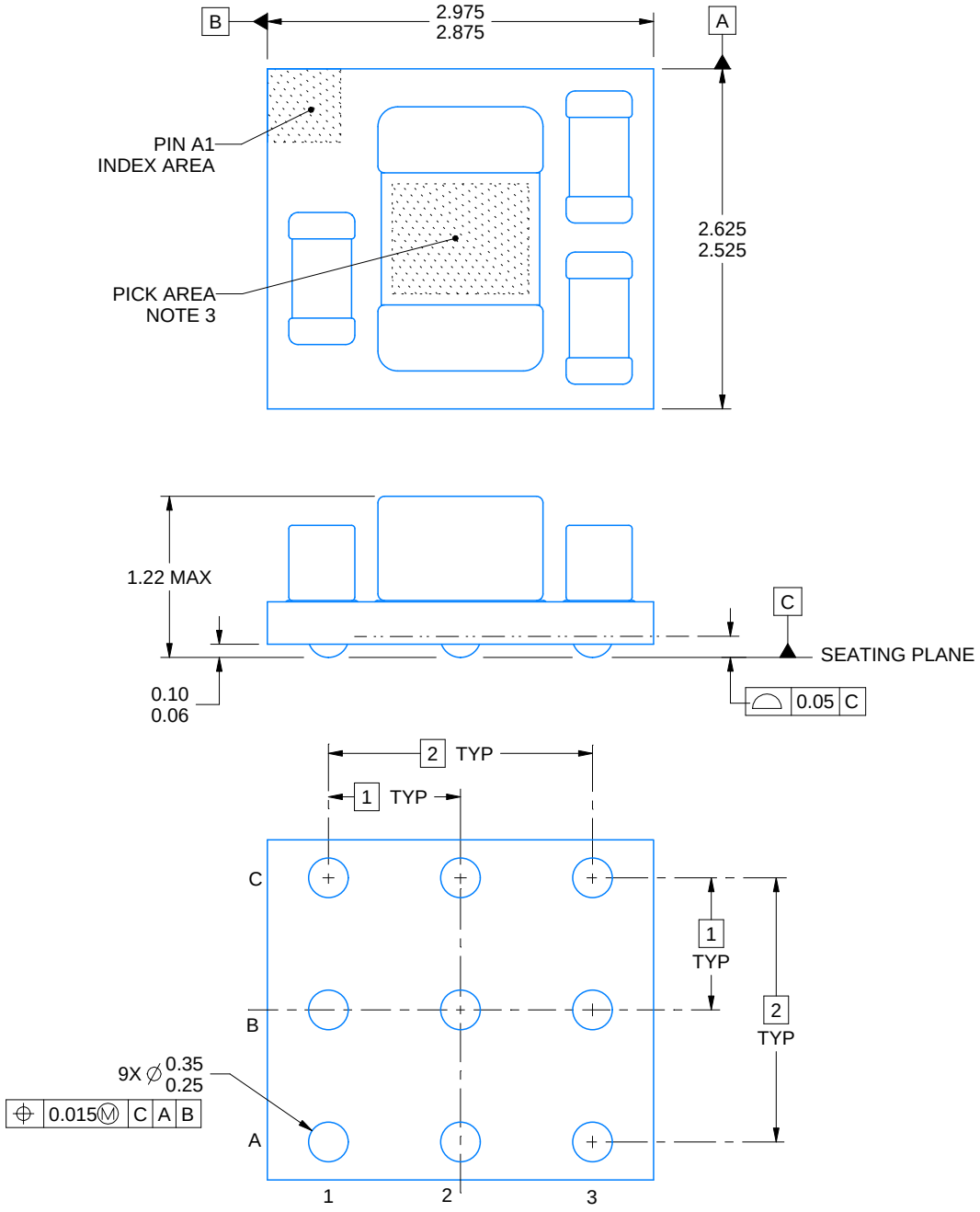
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS8268090SIPR	uSiP	SIP	9	3000	223.0	194.0	35.0
TPS8268090SIPT	uSiP	SIP	9	250	223.0	194.0	35.0
TPS8268105SIPR	uSiP	SIP	9	3000	223.0	194.0	35.0
TPS8268105SIPT	uSiP	SIP	9	250	223.0	194.0	35.0
TPS8268150SIPR	uSiP	SIP	9	3000	223.0	194.0	35.0
TPS8268150SIPT	uSiP	SIP	9	250	223.0	194.0	35.0

PACKAGE OUTLINE

SIP0009A

MicroSiP™ - 1.22 mm max height

MICRO SYSTEM IN PACKAGE



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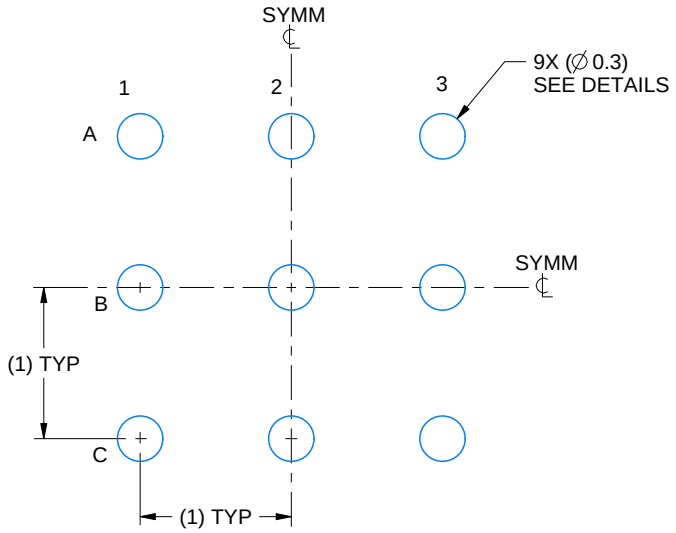
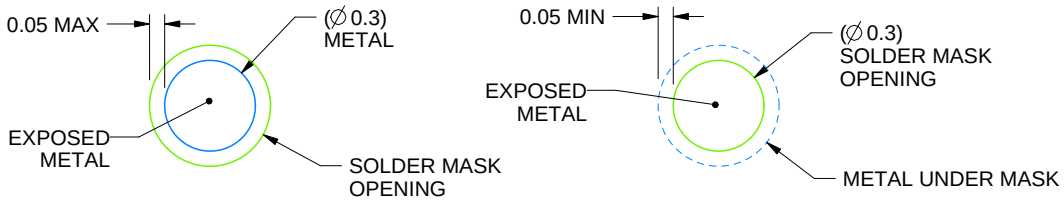
MicroSiP is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. For pick and place nozzle recommendation, see product datasheet.
4. Location, size and quantity of each component are for reference only and may vary.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS
NOT TO SCALE

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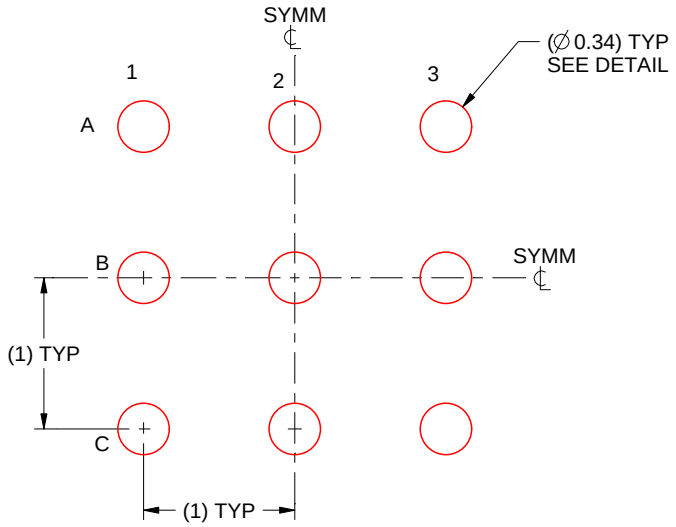
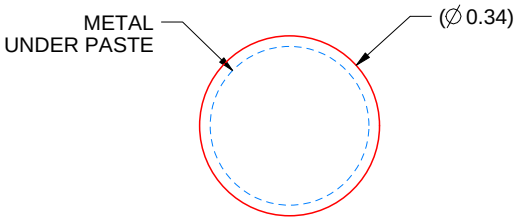
NOTES: (continued)

5. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:20X



SOLDER PASTE DETAIL
TYPICAL

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月