TPS7H3301-SP 内置 VREF 的灌电流/拉电流抗辐射加固型 3A DDR 终端稳压器

1 特性

- QML V 类符合 5962-14228(1)(2)
  - 总电离剂量为 100krad (Si)
    - 高剂量率 (HDR) (50-100 rad(Si)/s)
    - 低剂量率 (LDR) (0.01 rad(Si)/s)
  - 单粒子锁定 (SEL)、单粒子栅穿 (SEGR)、单粒子烧毁 (SEB) 对于线性能量传输 (LET) 的抗扰度 = 65MeV-cm^2/mg
  - 单粒子瞬变 (SET)、单粒子功能中断 (SEFI)、单粒子翻转 (SEU) 的抗扰度为 65MeV-cm^2/mg（详细信息请参见*辐射报告*）
- 支持 DDR、DDR2、DDR3、DDR3LP 和 DDR4 终端 应用 并兼容 JEDEC 标准
- 输入电压：支持 2.5V 和 3.3V 电源轨(3)
- 独立低电压输入 (VLDOIN) 降至 0.9V 以改善电源效率(3)
- 具有压降补偿功能的 3A 灌电流/拉电流终端稳压器
- 用于电源排序的使能输入和电源正常输出
- VTT 终端稳压器
  - 输出电压范围：0.5V 至 1.75V
  - 3A 灌电流和拉电流
  - 精度为 ±20mV
- 具有感测输入的精密集成分压器网络
- 远程感测 (VOSNS)
- VTTREF 缓冲参考输出
  - 精度为 VDDQ/2 ± 1%
  - ±10mA 灌/拉电流
- 集成了内置软启动 (SS)、欠压锁定 (UVLO) 以及过流限制 (OCL) 功能

2 应用

- 采用 DDR、DDR2、DDR3 和低功耗 DDR3 和 DDR4 存储器的 单电路板计算机、固态记录器和载荷 应用
- 超快速瞬态电源 应用
- 支持军用温度范围（-55°C 至 125°C）
- 提供工程评估 (/EM) 组件(4)

3 说明

TPS7H3301-SP 是一款内置 VREF 的 TID 和单粒子效应 (SEE) 抗辐射加固型双倍数据速率 (DDR) 3A 终端稳压器。该稳压器专门用于为空间 DDR 终端应用（如单电路板计算机、固态记录器和载荷处理应用）提供一套完整的紧凑型、低噪声解决方案。

TPS7H3301-SP 支持并兼容 DDR、DDR2、DDR3、DDR4 以及相关的低功耗 JEDEC 规范。凭借快速瞬态响应，TPS7H3301-SP VTT 稳压器可在读取/写入状态下提供稳定性较高的电源。TPS7H3301-SP 还包含一个内置的 VREF 电源。该电源可跟踪 VTT 以进一步缩减解决方案尺寸。在瞬态变化过程中，VREF 电源的快速跟踪功能能够最大限度地降低 VTT 和 VREF 之间的电压偏移。请参见*说明（续）*。

器件信息(1)(2)

器件型号	封装	封装尺寸（标称值）
TPS7H3301-SP	CFP (16)	9.60mm x 11.00mm

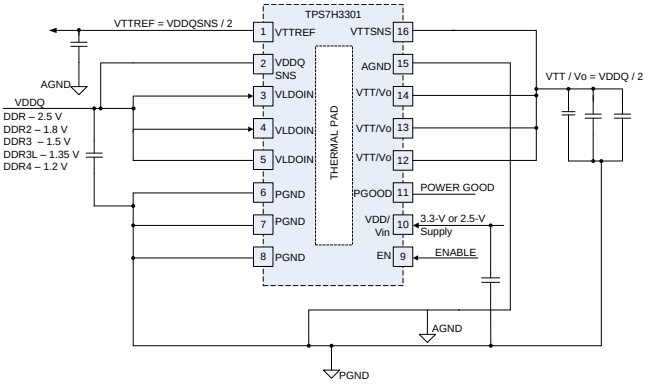
(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

(2) 抗辐射加固保障 (RHA) 当前可达 100krad；详细信息请联系制造商。

(3) 适用于 DDR2、DDR3、DDR3L 和 DDR4 DDR 的标称输入电压 = 3.3V。V_{INDDR1} 的 为 2.95V 至 3.5V，所有 DDR 的 V_{LDOIN} > V_{TT}。
DDR2 3A 负载条件下的 Vin 为 2.45V 至 3.5V。
Vin 余量：$V_{in\_min} \geq V_{TT}$ + 1.5V

(4) 这些部件仅用于工程评估。以非合规性流程对其进行了处理（即未进行老化处理等操作）并且仅在 25°C 的额定温度下进行了测试。这些部件不适用于质检、生产、辐射测试或飞行。这些零部件无法在 –55°C 至 125°C 的完整 MIL 额定温度范围内或运行寿命中保证其性能。

标准 DDR 应用



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4 修订历史记录

日期	修订版本	注释
2015 年 12 月	*	最初发布版本

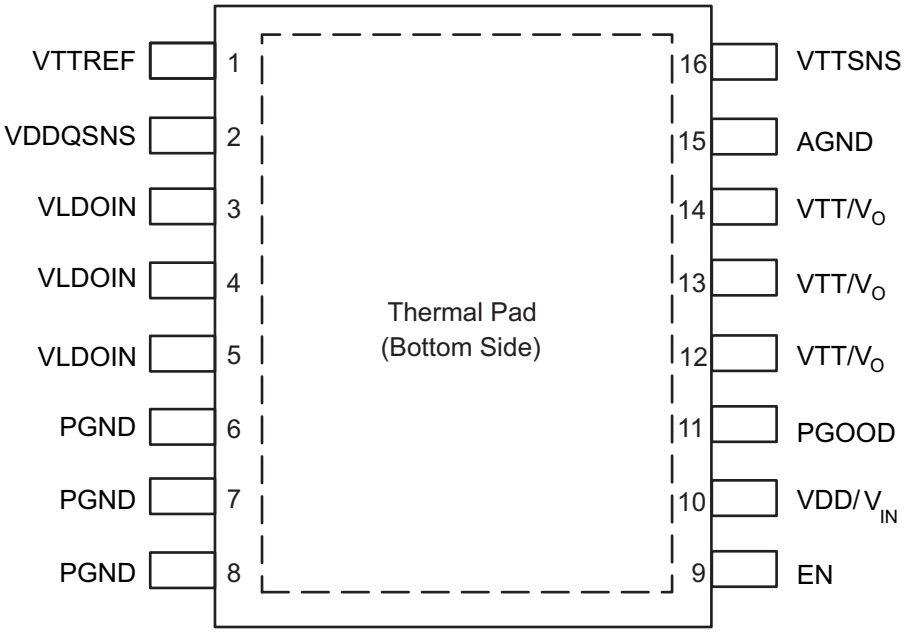
5 说明 （续）

为了简单的启用电源排序，使能输入和电源正常输出 (PGOOD) 已在 TPS7H3301-SP 中集成。PGOOD 输出是开漏输出，因此可在所有电源进入稳压状态时将其与多个开漏输出相连来进行监控。使能信号还可用于在挂起至 RAM (S3) 断电模式时使 VTT 放电。

TPS7H3301-SP 采用 TI 常用的 16 引脚耐热增强型双陶瓷扁平封装 (HKR)，TPS7H1101-SP 同样采用这种封装。

6 Pin Configuration and Functions

HKR Package
16-Pin CFP
Top View - Live Bug



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VTTREF	1	O	Reference output. Connect to GND through 0.1-µF ceramic capacitor.
VDDQSNS	2	I	VDDQ sense input. Reference input for VTTREF.
VLDOIN	3	I	Supply voltage for the LDO. Connect to VDDQ voltage or an alternate voltage source.
	4		
	5		
PGND	6	—	Power ground. Connect output for the VTT/ V_O LDO to negative pin of the output capacitor.
	7		
	8		
EN	9	I	Enable pin. Driving this pin to logic high enables the device; driving this pin to logic low disables the device.
VDD/V_{IN}	10	I	2.5- or 3.3-V power supply. A ceramic decoupling capacitor with a value between 1 and 10 µF is required.
PGOOD	11	O	PGOOD output pin. PGOOD pin is an open drain output to indicate the output voltage is within specification.
VTT/V_O	12	O	Power output for VTT LDO
	13		
	14		
AGND	15	—	Signal ground. Connect to negative pin of output capacitors.(1)
VTTSNS	16	I	VDDQ sense input, reference input for VTTREF. Voltage sense for VTT/ V_O . Connect to positive pin of the output capacitor or the load.

(1) Thermal pad must be connected to GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature, unless otherwise noted(1)

			MIN	MAX	UNIT
	Input voltage (2)	V_{IN} /VDD, VLDOIN, VTTSNS, VDDQSNS	–0.36	3.6	V
		EN	–0.3	6.5	
		PGND to AGND	–0.3	0.3	
	Output voltage (2)	V_O /VTT, VTTREF	–0.3	3.6	V
		PGOOD	–0.3	3.6	
	Peak output current		Internally limited		A
	PG pin sink current			5	mA
T_J	Maximum operating junction temperature		–55	150	°C
T_{stg}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground pin unless otherwise noted.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage	V_{IN} / VDD	2.375		3.5	V
Voltage	VLDOIN	0.9		3.5	
	EN, VTTSNS	–0.1		3.5	
	VDDQSNS	1.0		3.5	
	V_O / VTT, PGOOD	–0.1		3.5	
	VTTREF	–0.1		1.8	
	PGND	–0.1		0.1	
T_J	Operating junction temperature	–55		125	°C

7.4 Thermal Information

THERMAL METRIC (1) (2) (3)		TPS7H3301-SP HKR (CFP) 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Do not allow package body temperature to exceed 265°C at any time or permanent damage may result.
(3) Maximum power dissipation may be limited by overcurrent protection.

7.5 Electrical Characteristics

Over full temperature range, –55°C to 125°C, $V_{IN/VDD}$ = 3.3 V and 2.375V,V_{VLDOIN} = 1.8 V, $V_{VDDQSNS}$ = 1.8 V, $V_{VOSNS/VTTSNS}$ = 0.9 V, V_{EN} = $V_{VIN/VDD}$, *标准 DDR 应用* (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN} /I_{VDD}	Supply current	V_{EN} = 3.3 V, No Load		18	30	mA
$I_{VDD(SDN)}$	Shutdown current	V_{EN} = 0 V, VDDQSNS = 0, No Load		3	5	mA
		V_{EN} = 0 V, VDDQSNS > 0.78 V, No Load		6.5	8	
I_{LDOIN}	Supply current of VLDOIN	V_{EN} = 3.3 V, No Load		575	1200	µA
$I_{LDOIN(SDN)}$	Shutdown current of VLDOIN	V_{EN} = 0 V, No Load		50	100	µA
INPUT CURRENT						
$I_{VDDQsns}$	Input current, VDDQsns	V_{EN} = 3.3 V		4	6	µA
V_O / V_{TT} OUTPUT						
$V_{VOSNS/VTTSNS}$	Output DC voltage, VO	V_{LDOIN} = 2.5 V, V_{VTTREF} = 1.25 V (DDR1), I_O = 0 A		1.25		V
			–6		6	mV
		V_{LDOIN} = 1.8 V, V_{VTTREF} = 0.9 V (DDR2), I_O = 0 A		0.9		V
			–6		6	mV
		V_{LDOIN} = 1.5 V, V_{VTTREF} = 0.75 V (DDR3), I_O = 0 A		0.75		V
			–6		6	mV
		V_{LDOIN} = 1.35 V, V_{VTTREF} = 0.675 V (DDR3L), I_O = 0 A		0.675		V
			–6		6	mV
		V_{LDOIN} = 1.20 V, V_{VTTREF} = 0.60 V (DDR4), I_O = 0 A		0.60		V
			–6		6	mV
$V_{LODIN} – V_{TT}$ (1)	$V_{LODIN} > V_{TT}$	V_{IN} / V_{DD} = 2.95 V, $V_{VDDQSNS}$ = 2.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR1), I_O = 0.5 A		50	230	mV
		V_{IN} / V_{DD} = 2.95 V, $V_{VDDQSNS}$ = 2.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR1), I_O = 1 A		101	300	
		V_{IN} / V_{DD} = 2.95 V, $V_{VDDQSNS}$ = 2.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR1), I_O = 2.0 A(2)		209	400	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.80 V, V_{TT} = V_{VTTREF} – 50 mV (DDR2), I_O = 0.5 A(2)		54	230	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.80 V, V_{TT} = V_{VTTREF} – 50 mV (DDR2), I_O = 1 A(2)		108	300	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.80 V, V_{TT} = V_{VTTREF} – 50 mV (DDR2), I_O = 2.0 A(2)		228	400	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3), I_O = 0.5 A		52	230	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3), I_O = 1 A		104	300	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.50 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3), I_O = 2.0 A(2)		216	400	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.35 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3L), I_O = 0.5 A		50	230	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.35 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3L), I_O = 1 A		102	300	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.35 V, V_{TT} = V_{VTTREF} – 50 mV (DDR3L), I_O = 2.0 A(2)		212	400	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.20 V, V_{TT} = V_{VTTREF} – 50 mV (DDR4), I_O = 0.5 A		50	230	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.20 V, V_{TT} = V_{VTTREF} – 50 mV (DDR4), I_O = 1 A		102	300	
		V_{IN} / V_{DD} = 2.375 V, $V_{VDDQSNS}$ = 1.20 V, V_{TT} = V_{VTTREF} – 50 mV (DDR4), I_O = 2.0 A(2)		210	400	
$V_{VOTOL/VTTTOL}$	Output voltage tolerance to V_{VTTREF}	I_{VO} = –3 A, across V_{IN} voltage range(2)	12	25	34	mV
		I_{VO} = 3 A, across V_{IN} voltage range(2)	-34	–25	-12	
I_{VOSRCL}	VO/VTT source current limit	With reference to V_{VTTREF}, V_{VTTSNS} = 90% × V_{VTTREF}	3.25		8	A

(1) Dropout / Headroom information provided to help designer in optimizing system efficiency
(2) Specified by characterization and not production tested

Electrical Characteristics (continued)

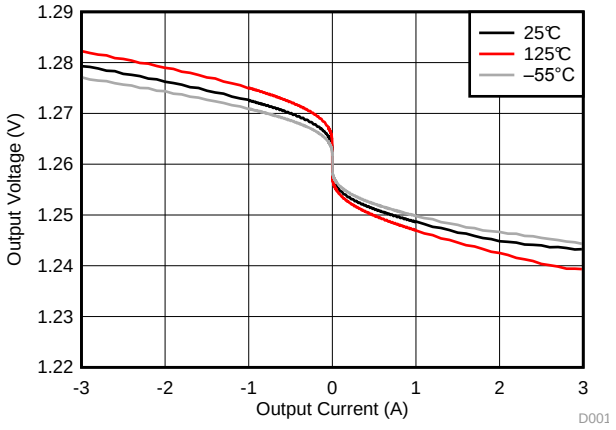
Over full temperature range, –55°C to 125°C, $V_{IN/VDD}$ = 3.3 V and 2.375V,V_{VLDOIN} = 1.8 V, $V_{VDDQSNS}$ = 1.8 V, $V_{VOSNS/VTTSNS}$ = 0.9 V, V_{EN} = $V_{VIN/VDD}$, *标准 DDR 应用* (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VOSNCL}	VO/VTT sink current limit	With reference to V_{VTTREF}, V_{VTTSNS} = 110% × V_{VTTREF}	3.5		5.5	A
R_{DSCHRG}	Discharge impedance, Ω	V_{DDQSNS} = 0 V, V_{VO} = 0.3 V, V_{EN} = 0 V, T_A = 25°C		18	25	Ω
POWERGOOD COMPARATOR						
$V_{TH(PG)}$	VO/VTT PGOOD threshold	PGOOD window lower threshold with respect to V_{VTTREF}	–23.5%	–20%	–17.5%	
		PGOOD window upper threshold with respect to V_{VTTREF}	17.5%	20%	23.5%	
		PGOOD hysteresis		5%		
$T_{PGSTUPDLY}$	PGOOD startup delay	Startup rising edge, VOSNS within 15% of V_{VTTREF}		2		ms
$V_{PGOODLOW}$	Output low voltage	I_{SINK} = 4 mA			0.4	V
$T_{PBADDLY}$	PGOOD bad delay	V_{OSNS} is outside of the ±20% PGOOD window		1		µs
$I_{PGOODLK}$	Leakage current	V_{OSNS} = V_{REFIN} (PGOOD high impedance), PGOOD = V_{IN} + 0.2 V			1	µA
V_{DDQSNS} AND V_{VTTREF} OUTPUT						
V_{DDQSNS}	V_{DDQSNS} voltage range		1.0		2.80	V
V_{DDQSNS_UVLO}	V_{DDQSNS} undervoltage lockout	V_{DDQSNS} rising		780		mV
$V_{DDQSNSUVHYS}$	V_{DDQSNS} undervoltage lockout hysteresis			20		mV
V_{VTTREF}	V_{VTTREF} voltage			V_{DDQSNS} / 2		V
V_{VTTREF}	V_{VTTREF} voltage tolerance to $V_{VDDQSNS}$	–10 mA < I_{VTTREF} <10 mA, $V_{VDDQSNS}$ = 2.5 V	–15		15	mV
		–10 mA <I_{VTTREF} <10 mA, $V_{VDDQSNS}$ = 1.8 V	–15		15	
		–10 mA <I_{VTTREF} <10 mA, $V_{VDDQSNS}$ = 1.5 V	–15		15	
		–10 mA <I_{VTTREF} <10 mA, $V_{VDDQSNS}$ = 1.35 V	–15		15	
		–10 mA <I_{VTTREF} <10 mA, $V_{VDDQSNS}$ = 1.2 V	–15		15	
$I_{VTTREFSRCL}$	V_{VTTREF} source current limit	VTTREF = 0 V	10	40		mA
$I_{VTTREFSNCCL}$	V_{VTTREF} sink current limit	VTTREF = 0 V	6	40		mA
$I_{VTTREFDIS}$	V_{VTTREF} discharge current	EN = 0 V, V_{DDQSNS} = 0 V, V_{VTTREF} = 0.5 V		1.3		mA
UVLO/EN LOGIC THRESHOLD						
$V_{VINUVVIN}$	UVLO threshold	Wake up, T_A = 25°C		2.18	2.25	V
		Hysteresis		50		mV
V_{ENIH}	High-level input voltage	Enable	1.7			V
V_{ENIL}	Low-level input voltage	Enable			0.3	
V_{ENYST}	Hysteresis voltage	Enable		0.5		
I_{ENLEAK}	Logic input leakage current	EN, T_A = 25°C	–1		1	µA
THERMAL SHUTDOWN						
T_{SON}	Thermal shutdown threshold (3)	Shutdown temperature		210		°C
		Hysteresis		12		

(3) Ensured by design, not production tested

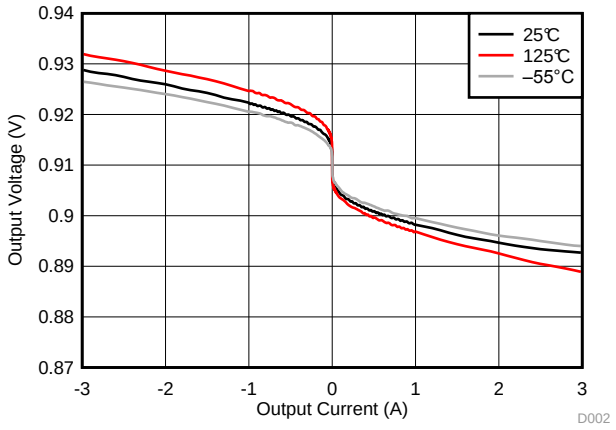
7.6 Typical Characteristics

For Figure 1 through Figure 15, (3 × 150 µF T530D157M010ATE005 tantalum + 4 × 4.7 µF MLCC) or equivalent capacitance/ESR are used on the output.



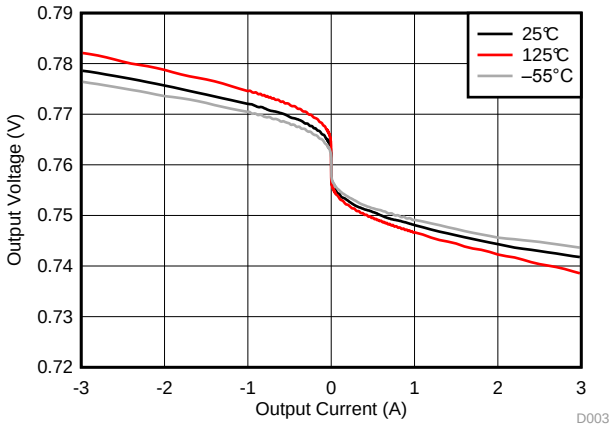
V_{VIN} = 3.3 V VDDQSNS = 2.5 V

Figure 1. Output Voltage vs Output Current



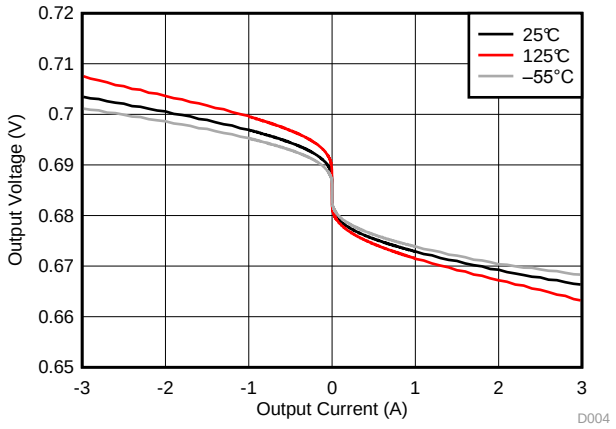
V_{VIN} = 3.3 V VDDQSNS = 1.8 V

Figure 2. Output Voltage vs Output Current



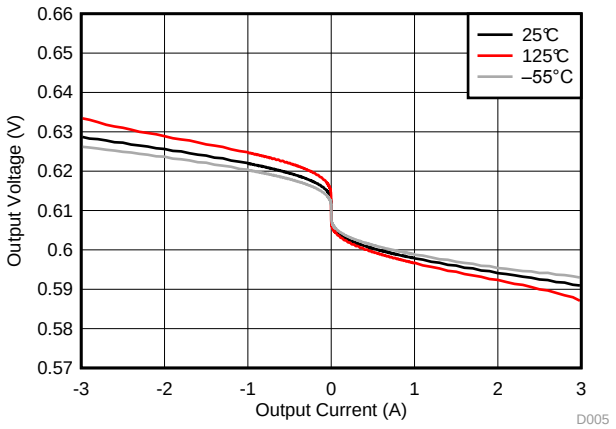
V_{VIN} = 3.3 V VDDQSNS = 1.5 V

Figure 3. Output Voltage vs Output Current



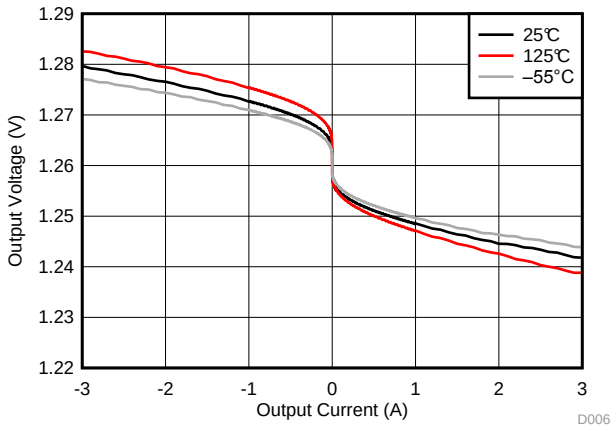
V_{VIN} = 3.3 V VDDQSNS = 1.35 V

Figure 4. Output Voltage vs Output Current



V_{VIN} = 3.3 V VDDQSNS = 1.2 V

Figure 5. Output Voltage vs Output Current

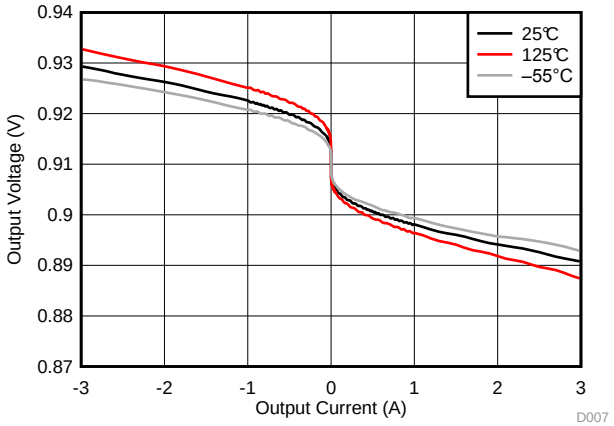


V_{VIN} = 2.95 V VDDQSNS = 2.5 V

Figure 6. Output Voltage vs Output Current

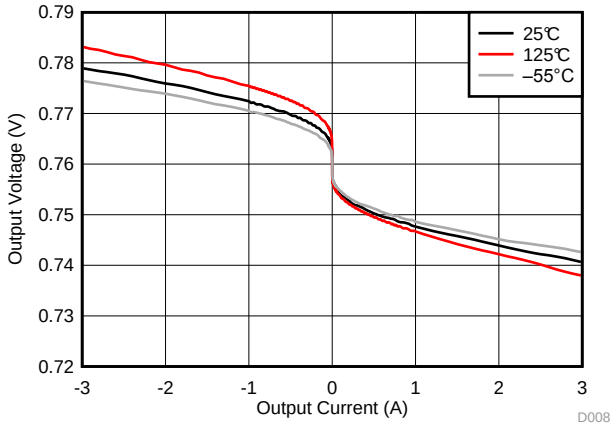
Typical Characteristics (continued)

For Figure 1 through Figure 15, (3 × 150 µF T530D157M010ATE005 tantalum + 4 × 4.7 µF MLCC) or equivalent capacitance/ESR are used on the output.



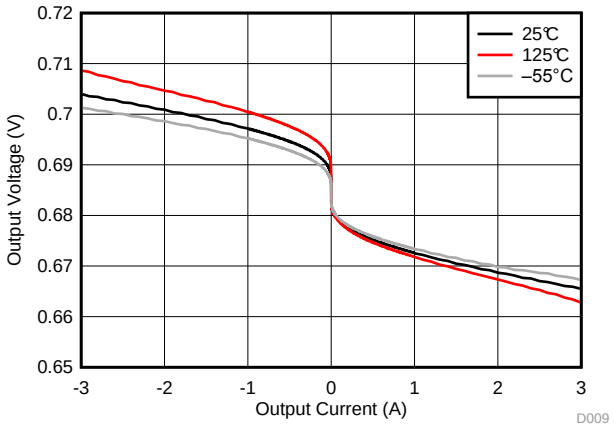
V_{VIN} = 2.95 V VDDQSNS = 1.8 V

Figure 7. Output Voltage vs Output Current



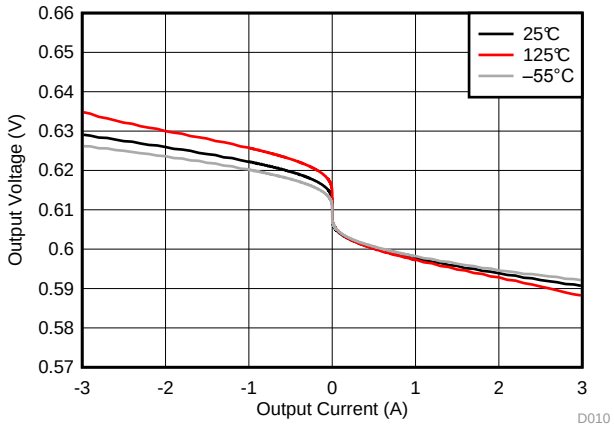
V_{VIN} = 2.375 V VDDQSNS = 1.5 V

Figure 8. Output Voltage vs Output Current



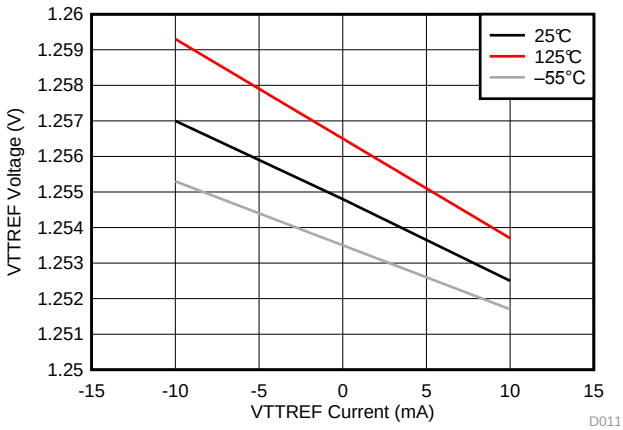
V_{VIN} = 2.375 V VDDQSNS = 1.35 V

Figure 9. Output Voltage vs Output Current



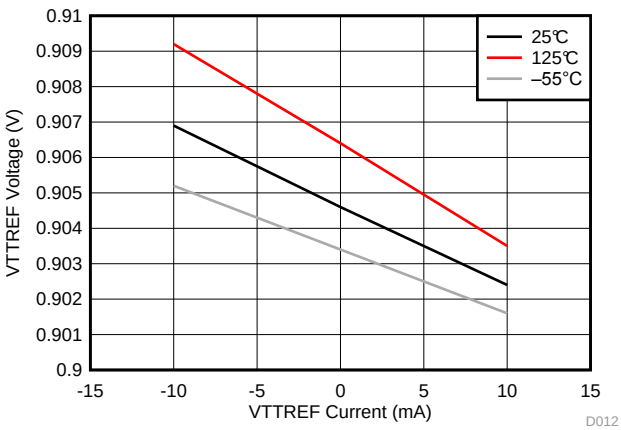
V_{VIN} = 2.375 V VDDQSNS = 1.2 V

Figure 10. Output Voltage vs Output Current



VDDQSNS = 2.5 V

Figure 11. RF Voltage vs REFOUT Current

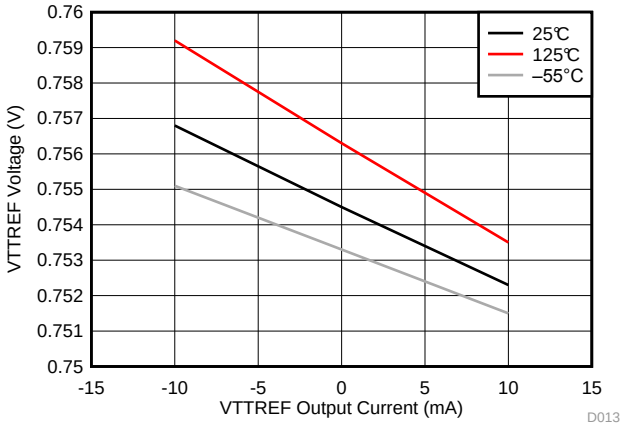


VDDQSNS = 1.8 V

Figure 12. RF Voltage vs REFOUT Current

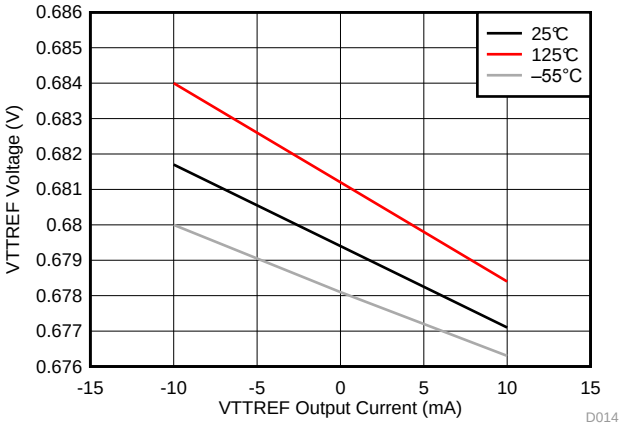
Typical Characteristics (continued)

For Figure 1 through Figure 15, (3 × 150 µF T530D157M010ATE005 tantalum + 4 × 4.7 µF MLCC) or equivalent capacitance/ESR are used on the output.



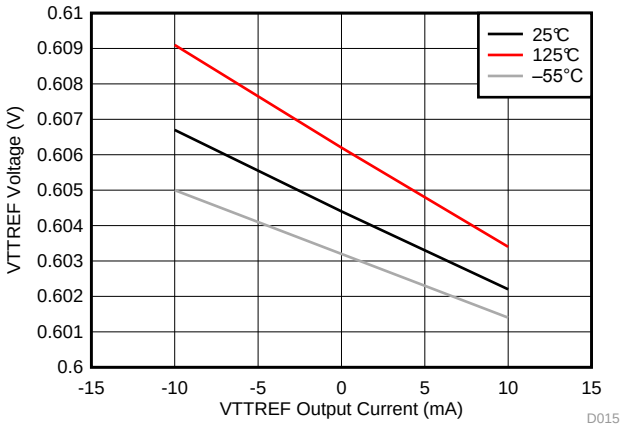
VDDQSNS = 1.5 V

Figure 13. RF Voltage vs REFOUT Current



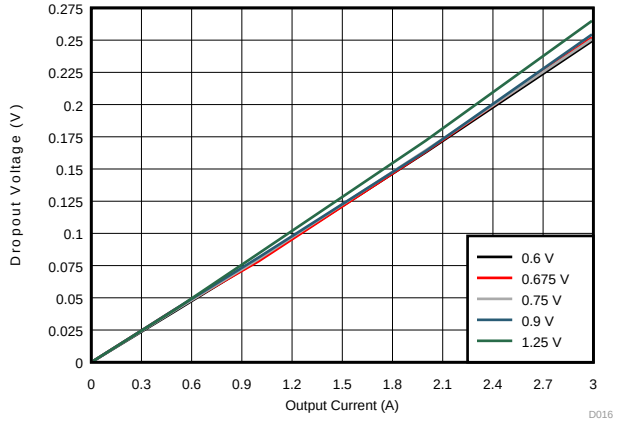
VDDQSNS = 1.35 V

Figure 14. RF Voltage vs REFOUT Current



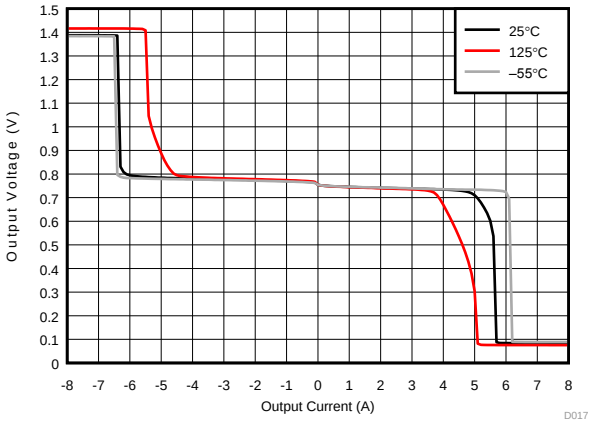
VDDQSNS = 1.2 V

Figure 15. RF Voltage vs REFOUT Current



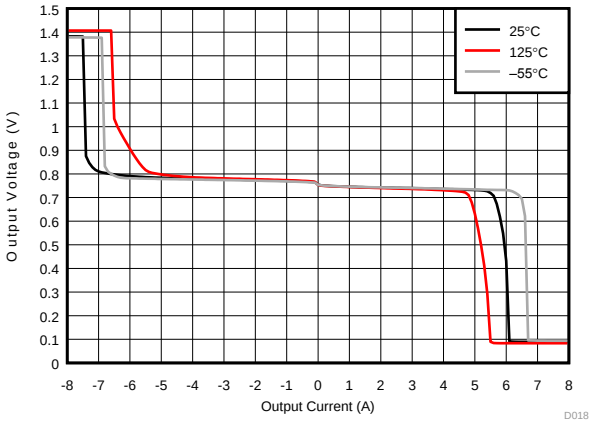
V_{VIN} = 3.6 V

Figure 16. Dropout Voltage vs Output Current



V_{IN} = 2.375 V VDDQSNS = 1.5 V

Figure 17. Output Voltage vs Output Current, DDR3

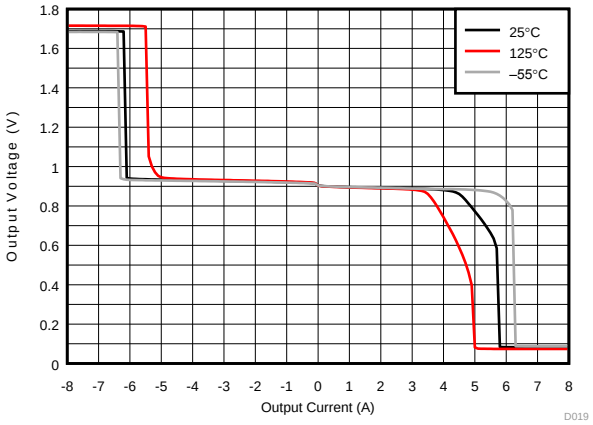


V_{IN} = 3.5 V VDDQSNS = 1.5 V

Figure 18. Output Voltage vs Output Current, DDR3

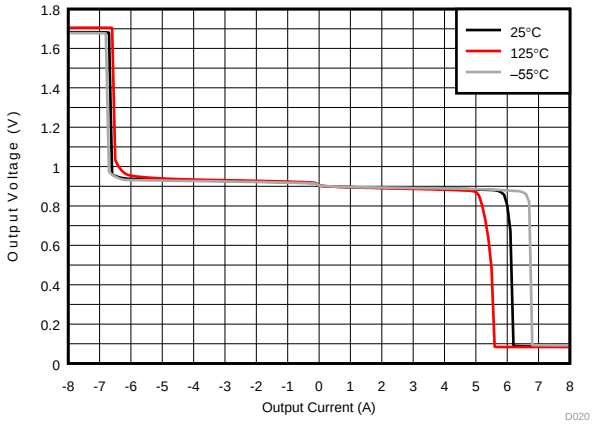
Typical Characteristics (continued)

For Figure 1 through Figure 15, (3 × 150 µF T530D157M010ATE005 tantalum + 4 × 4.7 µF MLCC) or equivalent capacitance/ESR are used on the output.



V_{IN} = 2.375 V VDDQSNS = 1.8 V

Figure 19. Output Voltage vs Output Current, DDR2



V_{IN} = 3.5 V VDDQSNS = 1.8 V

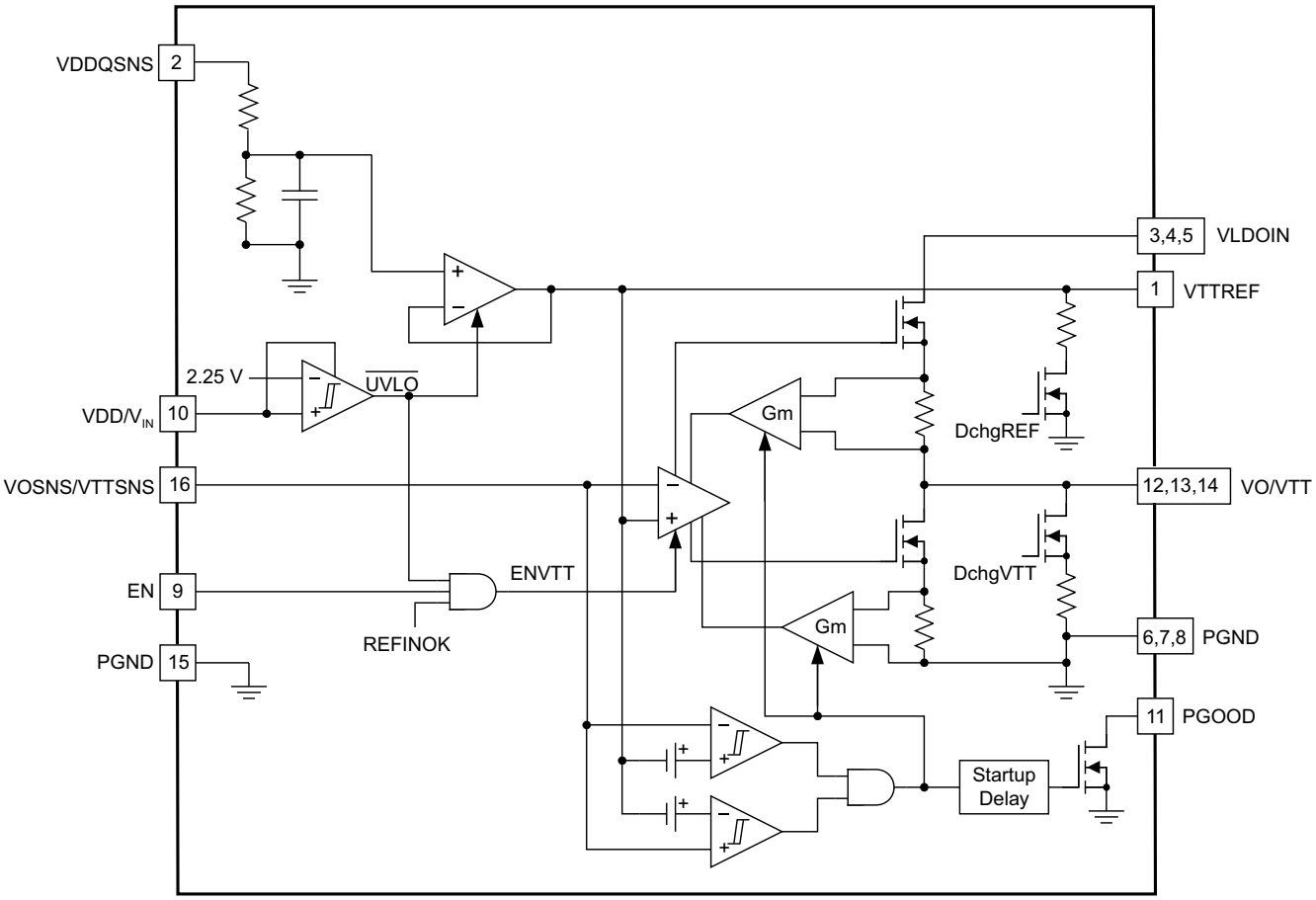
Figure 20. Output Voltage vs Output Current, DDR2

8 Detailed Description

8.1 Overview

The TPS7H3301-SP device is a sink and source double data rate (DDR) termination regulator specifically designed for low input voltage, low-cost, low-noise systems where space and weight is a key consideration.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 VO Sink/Source Regulator

The TPS7H3301-SP is a 3A sink/source tracking termination regulator specifically designed for low input voltage, low-cost, and low external component count systems where space is a key application parameter. The TPS7H3301-SP integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that ceramic capacitors can be used to support the fast load transient response. To achieve tight regulation with minimum effect of trace resistance, a remote sensing pin, VOSNS/VTTSNS, should be connected to the positive pin of the output capacitor(s) as a separate trace from the high current path from Vo/VTT.

The TPS7H3301-SP has a dedicated pin VLDOIN, for VTT power supply to minimize the LDO power dissipation on user application. The minimum VLDOIN voltage is 400mV above the 1/2 VDDQSNS voltage or as highlighted in electrical table VLDOIN to VTT headroom for various load conditions.

Feature Description (continued)

8.3.2 Reference Input (VDDQSNS)

The output voltage, Vo/VTT, is regulated to VTTREF. VDDQSNS incorporates integrated resistor divider network. VDDQSNS can be connected to memory supply bus (VDDQ). VDDQSNS should be connected to the memory supply bus (VDDQ). The TPS7H3301-SP supports VDDQSNS voltage from 1.0 V to 3.5 V, making it versatile and ideal for many types of low-power LDO applications.

8.3.3 Reference Output (VTTREF)

When it is configured for DDR termination applications, VTTREF generates the DDR VTT reference voltage for the memory application. VTTREF block consists of an on-chip 1/2 divider and a low-pass filter (LPF). VTTREF tracks 1/2 of VDDQSNS with 1% accuracy. It is capable of supporting both a sourcing and sinking load of 10 mA. VTTREF becomes active when VDDQSNS voltage rises to 0.78 V and Vin/VDD is above the UVLO threshold. When VTTREF is less than 0.375 V, VTTREF is disabled and subsequently discharges to GND through an internal MOSFET. VO/ VTT is also dicharged following discharge of VTTREF. VTTREF is independent of the EN pin state. To meet stability criteria, a capacitor of 0.1 µF min must be installed close to VTTREF (pin1). Capacitor value at VTTREF (pin 1) must not exceed 2.2 µF.

8.3.4 EN ControL (EN)

When EN is driven high, the TPS7H3301-SP Vo/ VTT regulator begins normal operation. When EN is driven low, Vo/VTT is discharges to GND through an internal 18-Ω MOSFET. VTTREF remains on when EN is driven low. EN is not tied high internally to prevent power sequencing issues with an external signal that may be controlling the enable. EN is floating input and not internally tied, thus the user can have complete control over where and when the EN signal is generated. EN feeds directly into PowerGood (PGOOD). When enable is low Pgood is low.

8.3.5 PowerGood Function (PGOOD)

The TPS7H3301-SP provides an open-drain PGOOD output that goes high when the Vo/VTT output is within 20% of VTTREF (typ). PGOOD deasserts within 1 µs after the output exceeds the size of the powergood window. During initial Vo/VTT startup, PGOOD asserts high 2 ms (typ) after the Vo/ VTT enters power good window. Because PGOOD is an open-drain output, a 100-kΩ, pullup resistor between PGOOD and a stable active supply voltage rail is required.

8.3.6 VO Current Protection

The LDO has a constant OCL.

8.3.7 VIN UVLO Protection

For VIN/ VDD undervoltage lockout (UVLO) protection, the TPS7H3301-SP monitors VIN/ VDD voltage. When the VIN/ VDD voltage is lower than the UVLO threshold voltage, both the VTT nd VTTREF regulators are powered off. This shutdown is a non-latch protection.

8.3.8 Thermal Shutdown

The TPS7H3301-SP monitors its junction temperature. If the device junction temperature exceeds its threshold value, (typically 210°C), the VO/VTT and VTTREF regulators are both shut off, discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

8.4 Device Functional Modes

TPS7H3301-SP a 3-A source-sink LDO provides low output noise to meet system needs. In order to improve efficiency in the LDO, TPS7H3301-SP LDO can operate from low VLDOIN voltage rail, thus using dual voltage source one for the VLDOIN that supports high current and an alternate voltage source that provides voltage for VDDQSNS pin.

Typcically VLDOIN and VDDQSNS pins are tied together. In the memory system VDDQ is a high-current supply that powers the core, the I/O, and the logic of the memory, VTTREF is a low-current, precision reference voltage that provides a threshold between a logic high (one) and a logic low (zero) that adapts to changes in the I/O supply voltage. By providing a precision threshold that adapts to the supply voltage, VTTREF realizes wider noise margins than those possible with a fixed threshold and normal variations in termination and drive impedance. Specifications vary from device manufacturer to manufacturer, but the most common specification is 0.49 to 0.51 times VDDQ and draws only tens to hundreds of microamps. For TPS7H3301-SP VTTREF is desinged to source / sink 10 mA.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H3301-SP device is a highly-integrated source sink LDO. The device is targeted to support VTT voltage for DDR memory applications and is capable of sourcing and sinking 3-A load current. The TPS7H3301-SP user's guide is available on www.ti.com, SLVUAK2. The guide highlights standard EVM test results, schematic, and bill of materials (BOM) for reference.

9.2 Typical Application

The design example describes a 2.5-V Vin, DDR3 configuration.

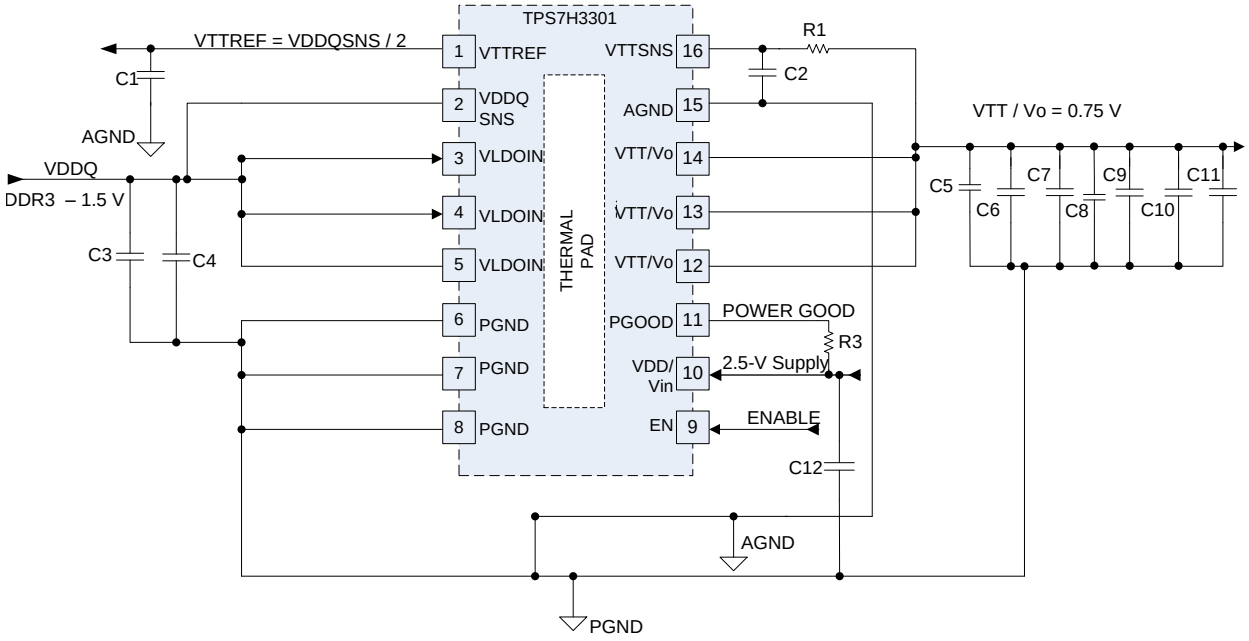


Figure 21. Typical Application Circuit

9.2.1 Design Requirements

See the *Recommended Operating Conditions* for recommended limits.

Typical Application (continued)

9.2.2 Detailed Design Procedure

Table 1. Design Example 1 List of Materials

REFERENCE DESIGNATOR	DESCRIPTION	SPECIFICATION	PART NUMBER	MANUFACTURER
R1	Resistor	392 Ω	CRCW0603392RFKEA	
R3		100 kΩ	CRCW0603100KJNEA	
C3, C5, C6, C7	Capacitor	150 µF, 10 V	T530D157M010ATE005	Kemet
C2		1000 pF	GRM188R71H102KA01D	MuRata
C1		0.1 µF	08053C104KAT2A	AVX
C4, C8, C9, C10, C11		4.7 µF, 10 V	1210ZC475KAT2A	Murata
C12		10 µF, 10 V	GRM21BR71A106KE51L	Murata

9.2.2.1 VIN/VDD Capacitor

Add a ceramic capacitor, with a value between 1- and 10-µF, placed close to the VIN/VDD pin, to stabilize the bias supply (2.5-V rail or 3.3-V rail) from any parasitic impedance from the supply.

9.2.2.2 VLDO Input Capacitor

Depending on the trace impedance between the VLDOIN/ VDDQ bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VLDOIN/ VDDQ input capacitor. Use a 150-µF (or greater) tantalum capacitor in parallel with 4.7uf ceramic capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VO. In general, use one-half of the C_{OUT} value for input. One can also determine the input capacitance based upon headroom between VLDOIN and VTT/ Vo voltage differential in the application.

9.2.2.3 VTT Output Capacitor

For stable operation, the total capacitance of the VTT/ Vo output pin must be greater than 470 µF. Attach three, 3 x 150-µF low esr tantalum capacitors in parallel with ceramic capacitors to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL). If the ESR is greater than 2 mΩ, insert an R-C filter between the output and the VTTSNS input to achieve loop stability. The R-C filter time constant should be almost the same as or slightly lower than the time constant of the output capacitor and its ESR.

9.2.2.4 VTTSNS Connection

To achieve tight regulation with minimum effect of trace resistance, a remote sensing pin, the VTTSNS pin should be connected to the positive pin of the VTT pin output capacitor or capacitors as a separate trace from the high-current path from VTT. Consider adding a low-pass R-C filter at the VTTSNS pin in case the ESR of the VTT output capacitor or capacitors is larger than 2 mΩ. The R-C filter time constant should be approximately the same or slightly lower than the time constant of the VTT output capacitance and ESR.

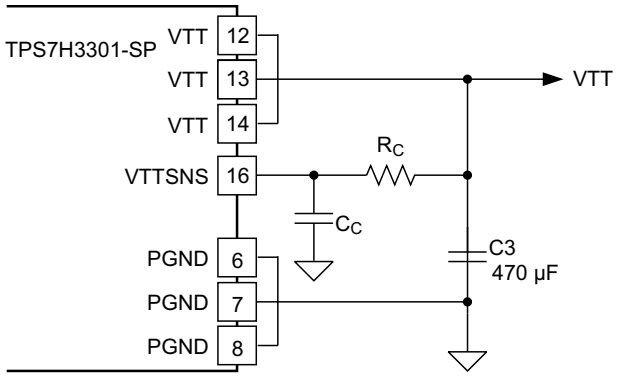


Figure 22. R-C Filter for VTTSNS

9.2.2.5 Low VIN Applications

TPS7H3301-SP can be used in an application system where either a 2.5-V rail or a 3.3-V rail is available. The TPS7H3301-SP minimum input voltage requirement is 2.375 V. If a 2.5-V rail is used, ensure that the absolute minimum voltage (both DC and transient) at the device pin is be 2.375 V or greater. The voltage tolerance for a 2.5-V rail input is between –5% and 5% accuracy, or better.

9.2.2.6 S3 and Pseudo-S5 Support

The TPS7H3301-SP provides S3 support by an EN function. The EN pin could be connected to an SLP_S3 signal in the end application. Both VTTREF and Vo/VTT are on when EN = high (S0 state). VTTREF is maintained while Vo/ VTT is turned off and discharged via an internal discharge MOSFET when EN = low (S3 state). When EN = low and the VDDQSNS voltage is less than 0.780 V, TPS7H3301-SP enters pseudo-S5 state. Both VTTREF and VTTREF outputs are turned off and discharged to GND through internal MOSFETs when pseudo-S5 support is engaged (S4/S5 state). Figure 23 shows a typical startup and shutdown timing diagram for an application that uses S3 and pseudo-S5 support.

9.2.2.7 Tracking Startup and Shutdown

The TPS7H3301-SP also supports tracking startup and shutdown when EN is tied directly to the system bus and not used to turn on or turn off the device. During tracking startup, VO/VTT follows VTTREF once VDDQSNS voltage is greater than 0.78 V. VDDQSNS incorporates the resistor divider network. The typical soft-start time for the VDDQ rail is approximately 3 ms, however it may vary depending on the system configuration. The SS time of the VO/VTT output no longer depends on the OCL setting, but it is a function of the SS time of the VDDQ rail. PGOOD is asserted 2 ms after VO/VTT is within ±20% of VTTREF. During tracking shutdown, VO/VTT falls following VTTREF until VTTREF reaches 0.37 V. Once VTTREF falls below 0.37 V, the internal discharge MOSFETs are turned on and quickly discharge both VTTREF and VO/VTT to GND. PGOOD is deasserted once VO/VTT is beyond the ±20% range of VTTREF. Figure 24 shows the typical timing diagram for an application that uses tracking startup and shutdown.

There are no sequencing requirements between Vin/VDD and VLDOIN. If VLDOIN is applied first followed by VDD/Vin there is no issue. Vin UVLO protection monitors Vin/VDD voltage, when Vin/Vdd is lower than UVLO threshold both VTT and VTTREF regulators are powered off.

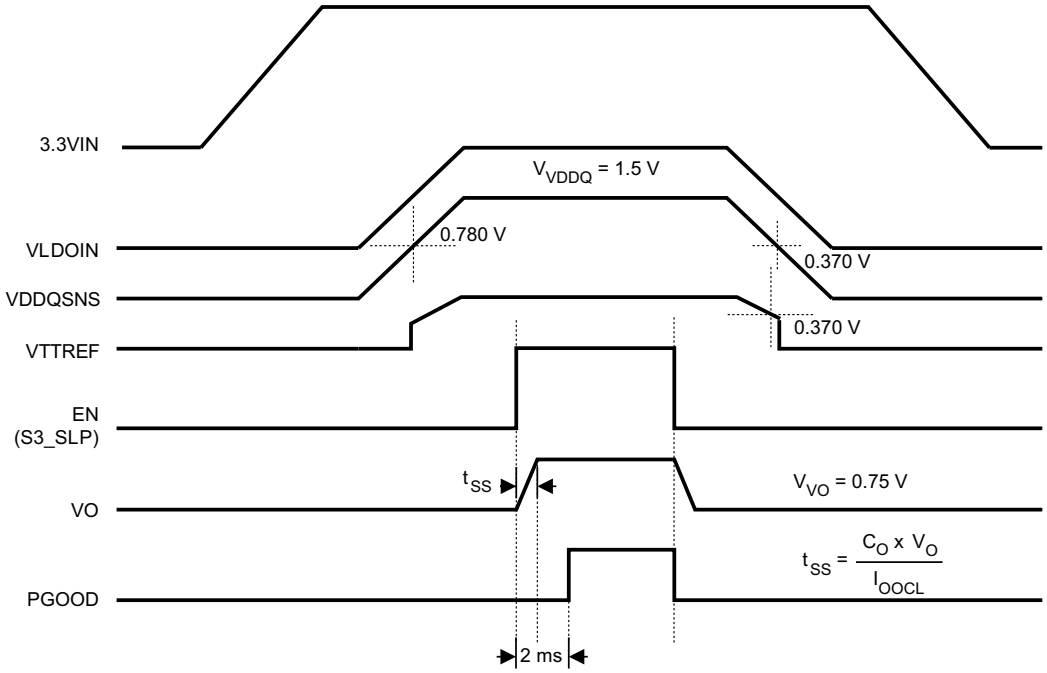


Figure 23. Typical Timing Diagram for S3 and Pseudo-S5 Support

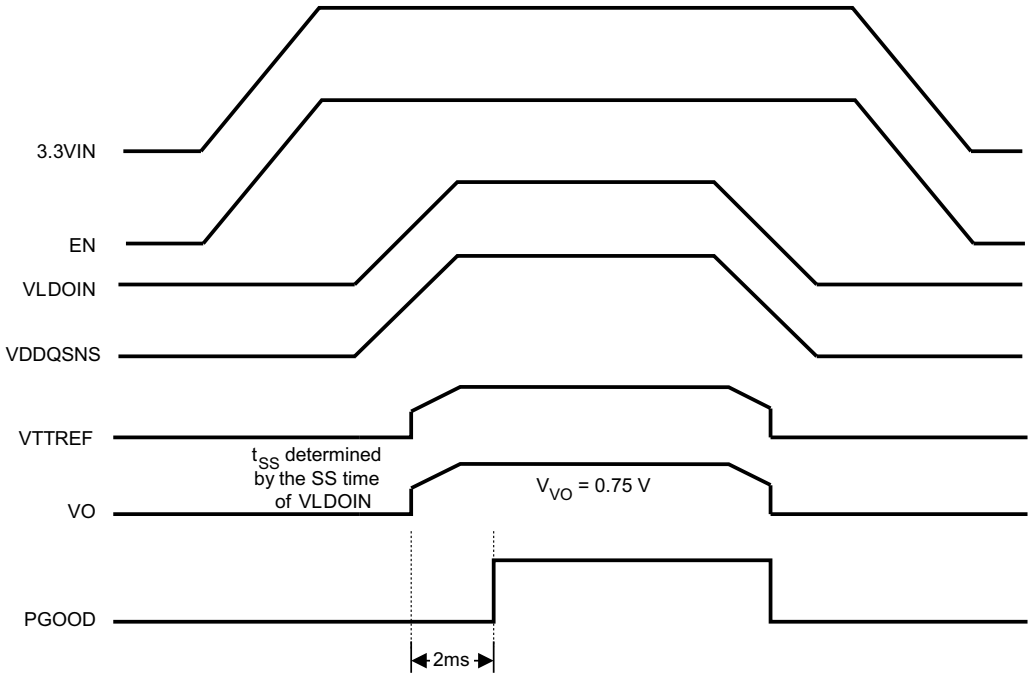


Figure 24. Typical Timing Diagram of Tracking Startup and Shutdown

9.2.2.8 Output Tolerance Consideration for VTT DIMM Applications

The TPS7H3301-SP is specifically designed to power up the memory termination rail (as shown in Figure 25). The DDR memory termination structure determines the main characteristics of the VTT rail, which is to be able to sink and source current while maintaining acceptable VTT tolerance. See Figure 26 for typical characteristics for a single memory cell.

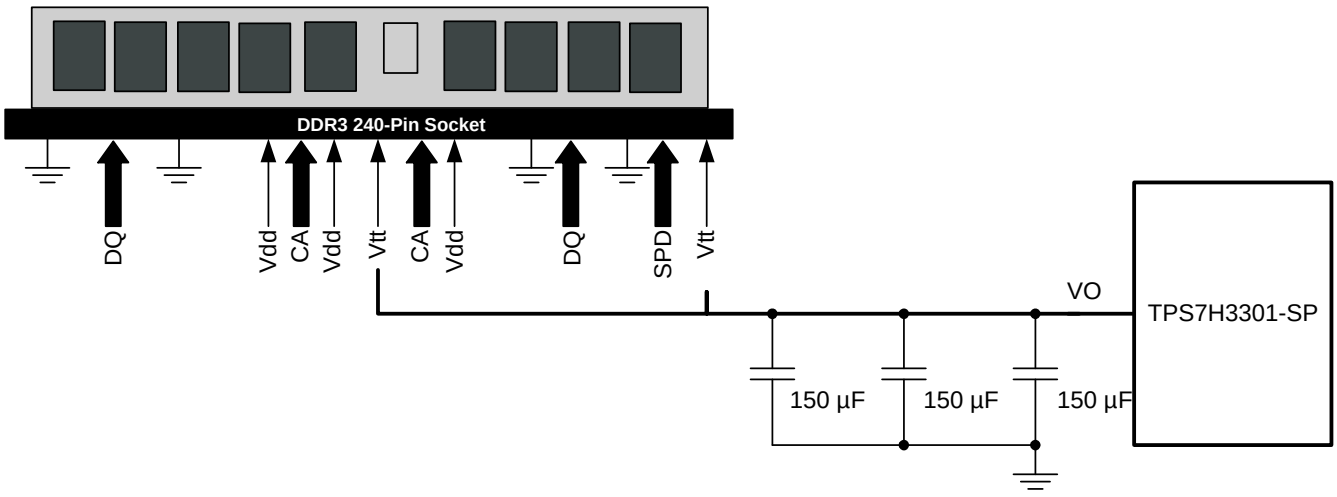


Figure 25. Typical Application Diagram for DDR3 VTT DIMM using TPS7H3301-SP

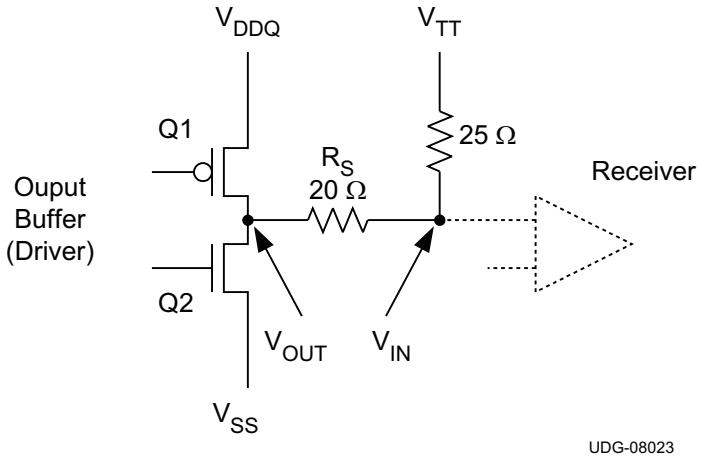


Figure 26. DDR Physical Signal System Bidirectional SSTL Signaling

In Figure 26, when Q1 is on and Q2 is off:

- Current flows from VDDQ via the termination resistor to VTT
- VTT sinks current

In Figure 26, when Q2 is on and Q1 is off:

- Current flows from VTT via the termination resistor to GND
- VTT sources current

Because VTT accuracy has a direct impact on the memory signal integrity, it is imperative to understand the tolerance requirement on VTT. Based on JEDEC VTT specifications for DDR and DDR2 (JEDEC standard: DDR JESD8-9B May 2002; DDR2 JESD8-15A Sept 2003).

VTTREF – 40 mV <VTT <VTTREF + 40 mV, for both dc and ac conditions

The specification itself indicates that VTT must keep track of VTTREF for proper signal conditioning.

The TPS7H3301-SP ensures the regulator output voltage to be:

VTTREF –34 mV <VTT <VTTREF + 34mV, for both DC and AC conditions and –3 A <I_{VTT} <3 A

The regulator output voltage is measured at the regulator side, not the load side. The tolerance is applicable to DDR, DDR2, DDR3 and Low Power DDR3/DDR4 applications (see Table 2 for detailed information). To meet the stability requirement, a minimum output capacitance of 470 µF is needed, combination of both Tantalum and ceramic capacitors. Considering the actual tolerance on the MLCC capacitors, four or higher 4.7-µF ceramic capacitors in parallel with 3 × 150 µF low esr tantalum capacitor are sufficient to meet the above requirement. For higher esr tantalum capacitors it will require multiple tantalum capacitors in parallel with ceramic capacitors to meet system needs.

Table 2. DDR, DDR2, DDR3, and LP DDR3 Termination Technology and Their Differences

	DDR	DDR2	DDR3	LOW POWER DDR3 (DDR3L)
FSB Data Rates	200, 266, 333 and 400 MHz	400, 533, 677 and 800 MHz	800, 1066, 1330 and 1600 MHz	Same as DDR3
Termination	Motherboard termination to VTT for all signals	On-die termination for data group. VTT termination for address, command and control signals	On-die termination for data group. VTT termination for address, command and control signals	Same as DDR3
Termination Current Demand	Max source/sink transient currents of up to 2.6 A to 2.9 A	Not as demanding • Only 34 signals (address, command, control) tied to VTT • ODT handles data signals Less than 1 A of burst current	Not as demanding • Only 34 signals (address, command, control) tied to VTT • ODT handles data signals Less than 1 A of burst current	Same as DDR3
Voltage Level	2.5-V Core and I/O 1.25-V VTT	1.8-V Core and I/O 0.9-V VTT	1.5-V Core and I/O 0.75-V VTT	1.35-V Core and I/O 0.68-V VTT

The TPS7H3301-SP is designed as a Gm driven LDO. The voltage droop between the reference input and the output regulator is determined by the transconductance and output current of the device. The typical Gm is 250 S at 3 A and changes with respect to the load in order to conserve the quiescent current (that is, the Gm is very low at no load condition). The Gm LDO regulator is a single pole system. Its unity gain bandwidth for the voltage loop is only determined by the output capacitance, as a result of the bandwidth nature of the Gm (see Equation 1).

$$F_{UGBW} = \frac{Gm}{2 \times \pi \times C_{OUT}} \quad (1)$$

where

- F_{UGBW} is the unity gain bandwidth
- Gm is transconductance
- C_{OUT} is the output capacitance

There are two limitations to this type of regulator when it comes to the output bulk capacitor requirement. To maintain stability, the zero location contributed by the ESR of the output capacitors should be greater than the –3-dB point of the current loop. This constraint means that higher ESR capacitors should not be used in the design. In addition, the impedance characteristics of the ceramic capacitor should be well understood in order to prevent the gain peaking effect around the Gm –3-dB point because of the large ESL, the output capacitor and parasitic inductance of the VO trace.

Figure 27 shows the bode plot simulation for a typical DDR3 configuration of the TPS7H3301-SP, where:

- V_{IN} = 2.4 V
- V_{VLDOIN} = 1.5 V
- V_{VO} = 0.75 V
- I_{IO} = 2 A
- 3 × 150-µF low-ESR tantalum capacitors (T530D157M010ATE005) in parallel with 4 × 4.7-µF ceramic capacitor include
- ESR = 1.66 mΩ
- ESL = 800 pH

The unity-gain bandwidth is approximately 87.3 kHz and the phase margin is 82°. The 0-dB level is crossed, the gain peaks because of the ESL effect. However, the peaking is kept well below 0 dB.

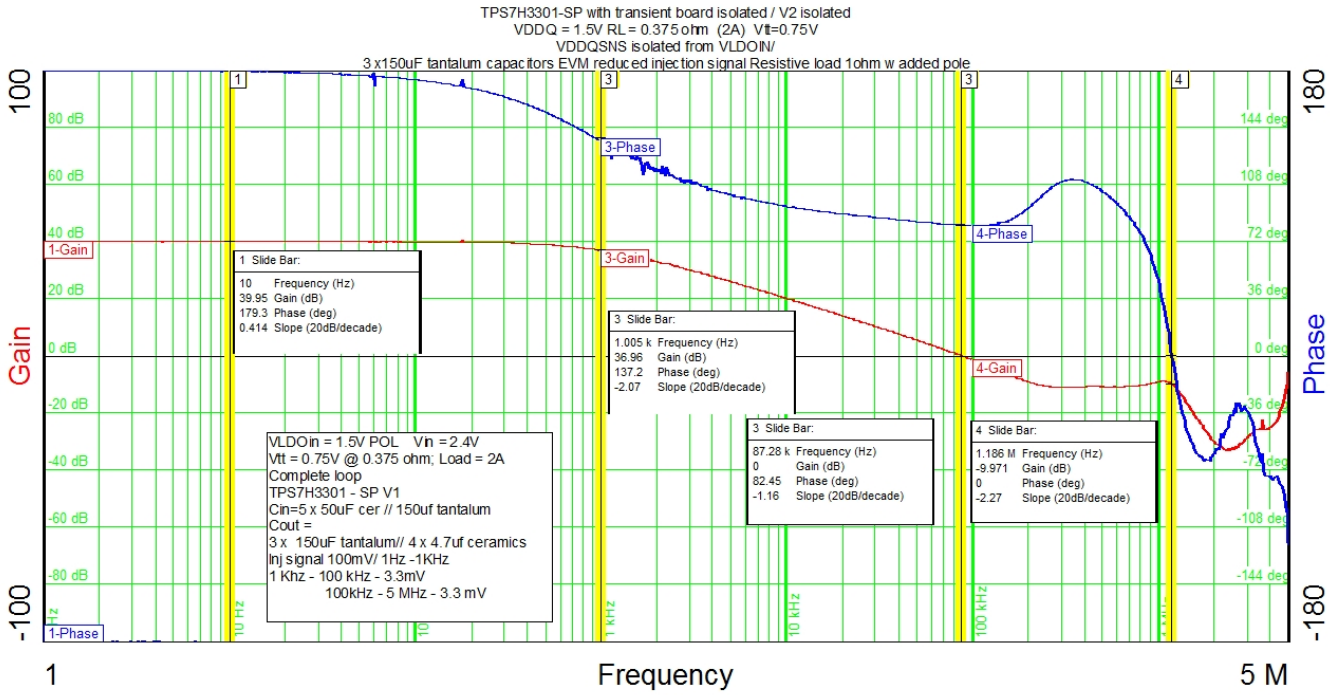


Figure 27. Bode Plot for a Typical DDR3 Configuration

Figure 8 shows the load regulation and Figure 28 shows the transient response for a typical DDR3 configuration. When the regulator is subjected to ±1.5-A load step and release, the output voltage measurement shows no difference between the DC and AC conditions.

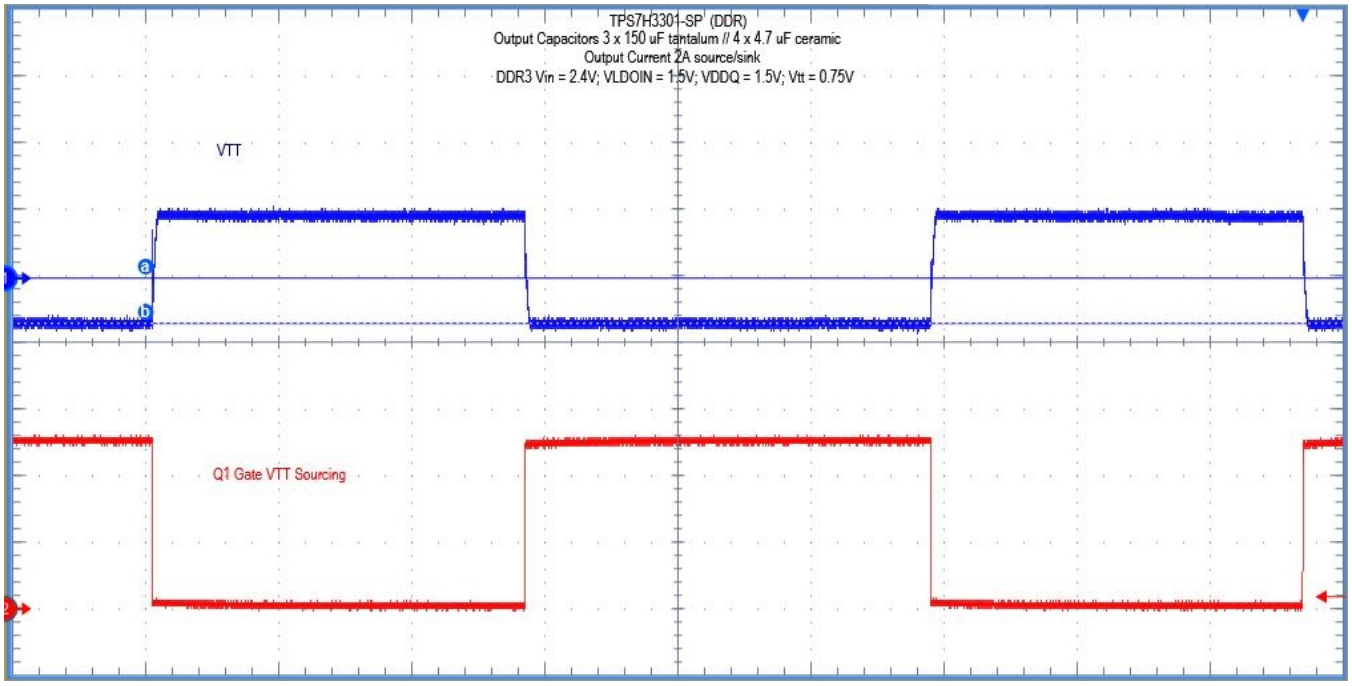


Figure 28. Transient Plot

9.2.2.9 LDO Design Guidelines

The minimum input (VLDOIN) to output voltage (V_O/V_{tt}) difference (headroom) decides the lowest usable supply voltage Gm-driven to drive a certain load. For TPS7H3301-SP, a minimum of 300 mV ($VLDOIN_{MIN} – VO_{MAX}$) is needed in order to support a Gm driven sourcing current of 3 A based on a design of V_{IN} = 3.3 V and C_{OUT} = 470 µF. Because the TPS7H3301-SP is essentially a Gm driven LDO, its impedance characteristics are both a function of the 1/Gm and $R_{DS(on)}$ of the sourcing MOSFET (see Figure 29). The current inflection point of the design is between 3 A and 4 A. When I_{SRC} is less than the inflection point, the LDO is considered to be operating in the Gm region; when I_{SRC} is greater than the inflection point but less than the overcurrent limit point, the LDO is operating in the $R_{DS(on)}$ region. The typical sourcing $R_{DS(on)}$ is 154 mΩ with V_{IN} = 3.0 V and T_J = 125°C.

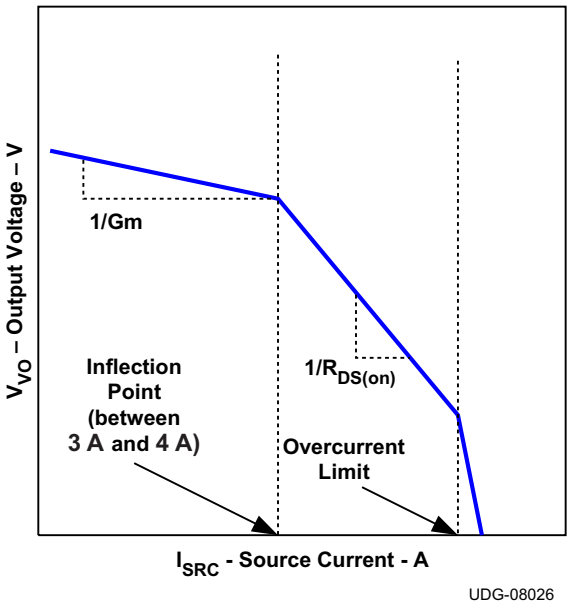


Figure 29. TPS7H3301-SP Impedance Characteristics

9.2.3 Application Curve

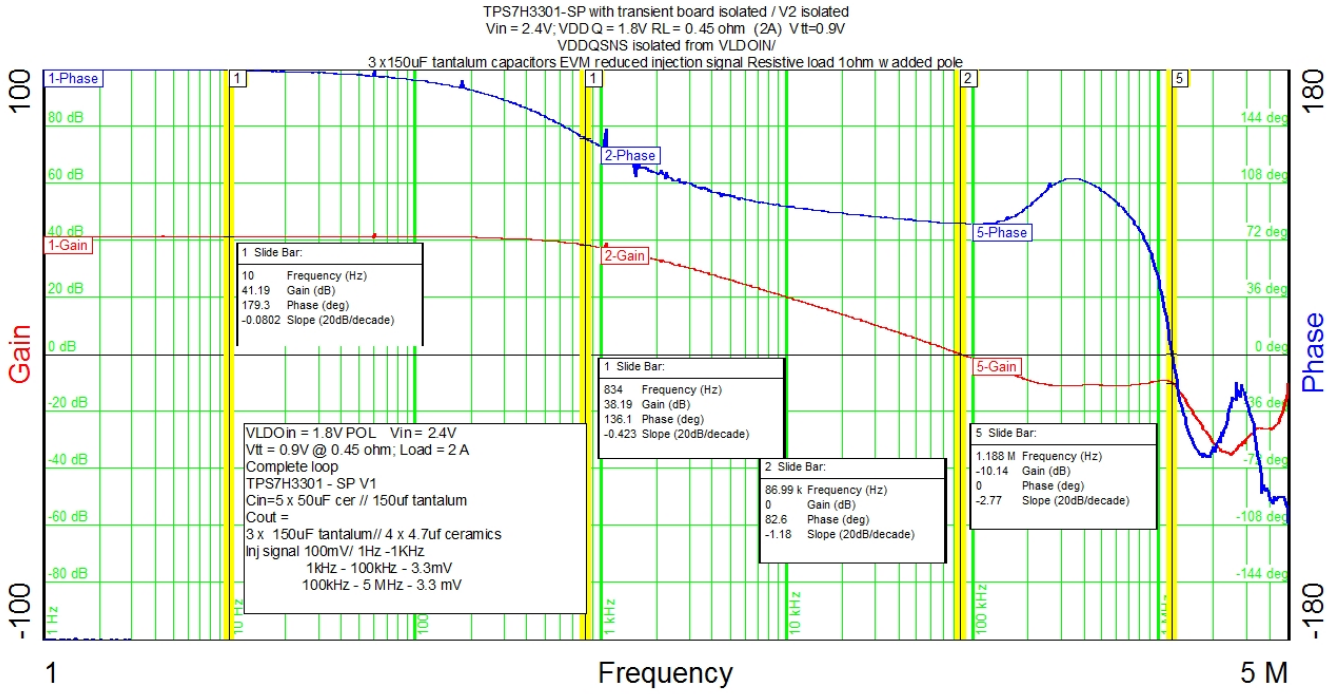


Figure 30. DDR2 2-A Load Vin 2.4 V 0.9 Vtt

10 Power Supply Recommendations

TPS7H3301-SP is designed to support DDR, DDR2, DDR3, DDR3L, and DDR4 VTT applications. TPS7H3301-SP VLDOIN supports voltage range from 0.9 V to 3.5 V. The supply must be well regulated. Having a separate VLDOIN and VDDQSNS allows designer to optimize system efficiency. Vin/VDD is used to bias the TPS7H3301-SP IC and its voltage range is from 2.375 V to 3.5 V. This supply must be well regulated and bypassed with a ceramic capacitor with a value of 1 µF and 10 µF. TI recommends that VLDOIN and VDDQSNS be isolated from each other. If this is not possible then an RC filter must be used to isolated VLDOIN and VDDQNSS. However, in so doing the dynamic tracking of VTT and VTTREF will be lost. See the user's guide SLVUAK2 for additional details.

11 Layout

11.1 Layout Guidelines

Consider the following points before starting the TPS7H3301-SP layout design.

- The input bypass capacitor for VLDOIN should be placed as close as possible to the pin with short and wide connections.
- The output capacitor for VO/VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL trace inductance.
- VOSNS should be connected to the positive node of VO/VTT output capacitors as a separate trace from the high current power line. This configuration is strongly recommended to avoid additional ESR and/or ESL. If sensing the voltage at the point of the load is required, it is recommended to attach the output capacitor or capacitors at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between the GND pin and the output capacitor or capacitors.
- Consider adding low-pass filter at VOSNS if the ESR of the VO/VTT output capacitor or capacitors is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise-generating lines.
- The negative node of the VO/VTT output capacitor or capacitors and the VTTREF capacitor should be tied together by avoiding common impedance to the high current path of the VO/VTT source/sink current.
- The GND and PGND pins should be connected to the thermal land underneath the die pad with multiple vias connecting to the internal system ground planes (for better result, use at least two internal ground planes). Use as many vias as possible to reduce the impedance between PGND/GND and the system ground plane. Also, place bulk caps close to the DIMM load point, route the VOSNS to the DIMM load sense point.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package's thermal pad. The wide traces of the component and the side copper connected to the thermal land pad help to dissipate heat. Numerous vias 0.33 mm in diameter connected from the thermal land to the internal/solder side ground plane or planes should also be used to help dissipation.

11.2 Layout Example

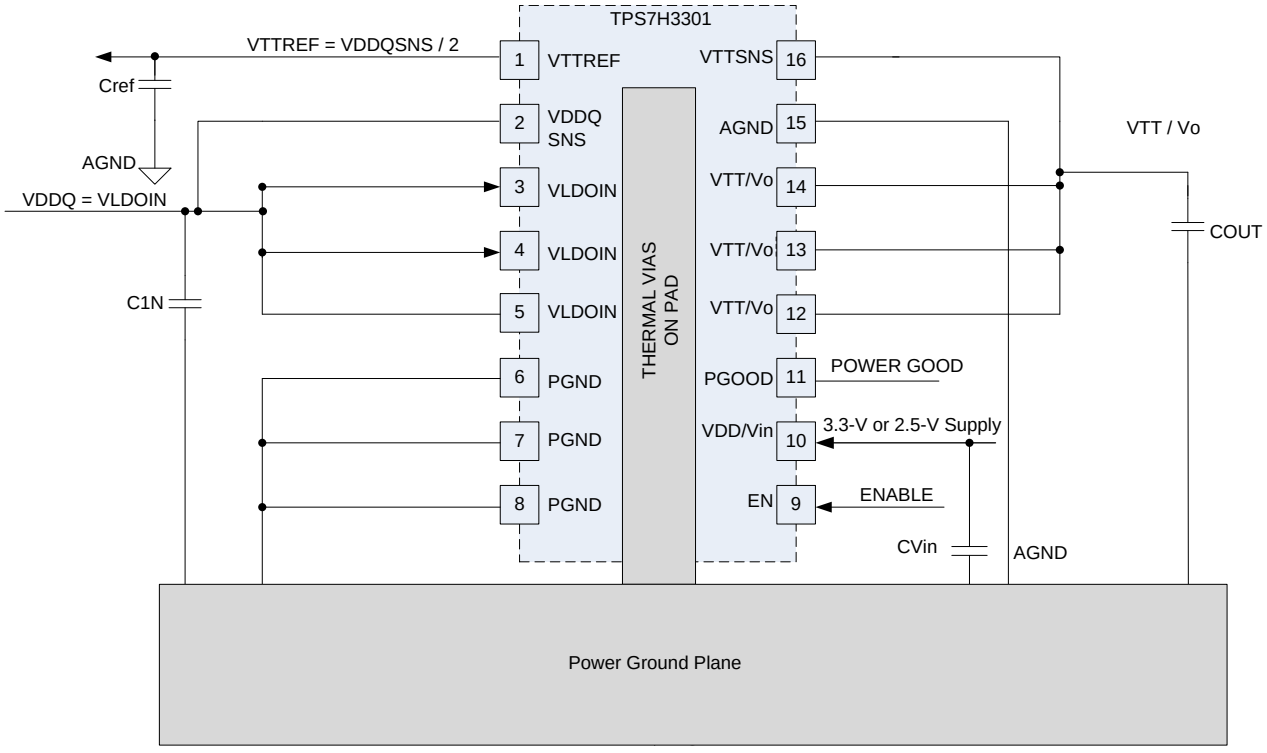


Figure 31. Layout Recommendation

11.3 Thermal Considerations

Because the TPS7H3301-SP is a linear regulator, the VO current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the voltage difference between VLDOIN and VO times IO (I_{IO}) current becomes the power dissipation as shown in Equation 2.

$$P_{DISS\_SRC} = (V_{VLDOIN} - V_{VO}) \times I_{O\_SRC} \quad (2)$$

In this case, if VLDOIN is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VO voltage is applied across the internal LDO regulator, and the power dissipation, P_{DISS_SNK} can be calculated by Equation 3.

$$P_{DISS\_SNK} = V_{VO} \times I_{O\_SNK} \quad (3)$$

Because the device does not sink and source current at the same time and the IO current may vary rapidly with time, the actual power dissipation should be the time average of the above dissipations over the thermal relaxation duration of the system. Another source of power consumption is the current used for the internal current control circuitry from the VIN supply and the VLDOIN supply. This can be estimated as 5 mW or less during normal operating conditions. This power must be effectively dissipated from the package.

The thermal performance of an LDO depends on the printed circuit board (PCB) layout. Because the TPS7H3301-SP device is shipped unformed, only the recommended heat pad pattern is shown. Lead pad placement depends on final form factor.

To further improve the thermal performance of this device, using a larger than recommended thermal land as well as increasing the number of vias helps lower the thermal resistance from junction to heat slug. TI recommends that up to 48 (0.01 inch) thermal vias can be located under the device package.

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-1422801VXC	ACTIVE	CFP	HKR	16	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962-1422801VXC TPS7H3301-SP	Samples
5962R1422801VXC	ACTIVE	CFP	HKR	16	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R1422801VXC TPS7H3301-RHA	Samples
TPS7H3301HKR/EM	ACTIVE	CFP	HKR	16	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	TPS7H3301HKREM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

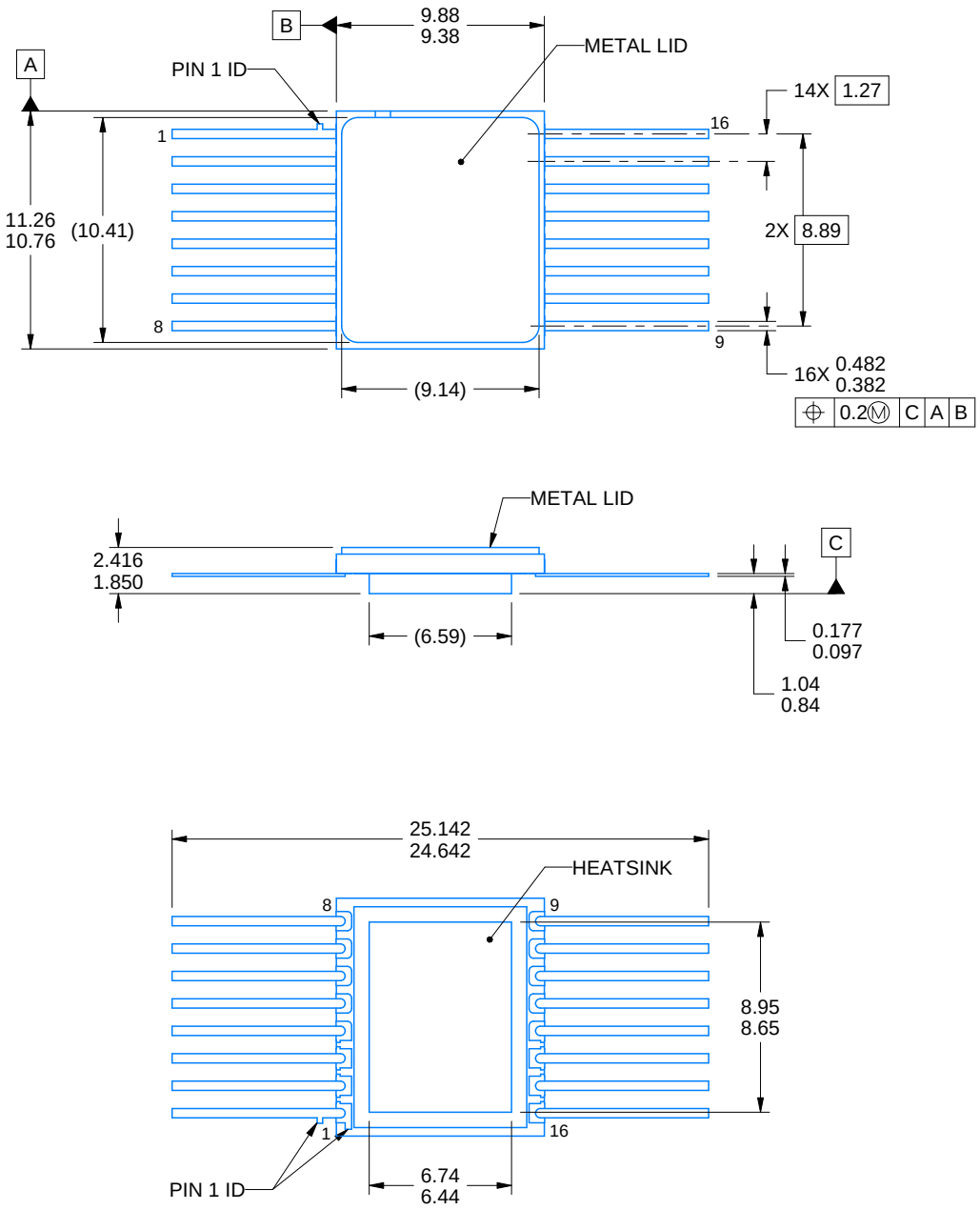
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

HKR0016A

CFP - 2.416 mm max height

CERAMIC DUAL FLATPACK



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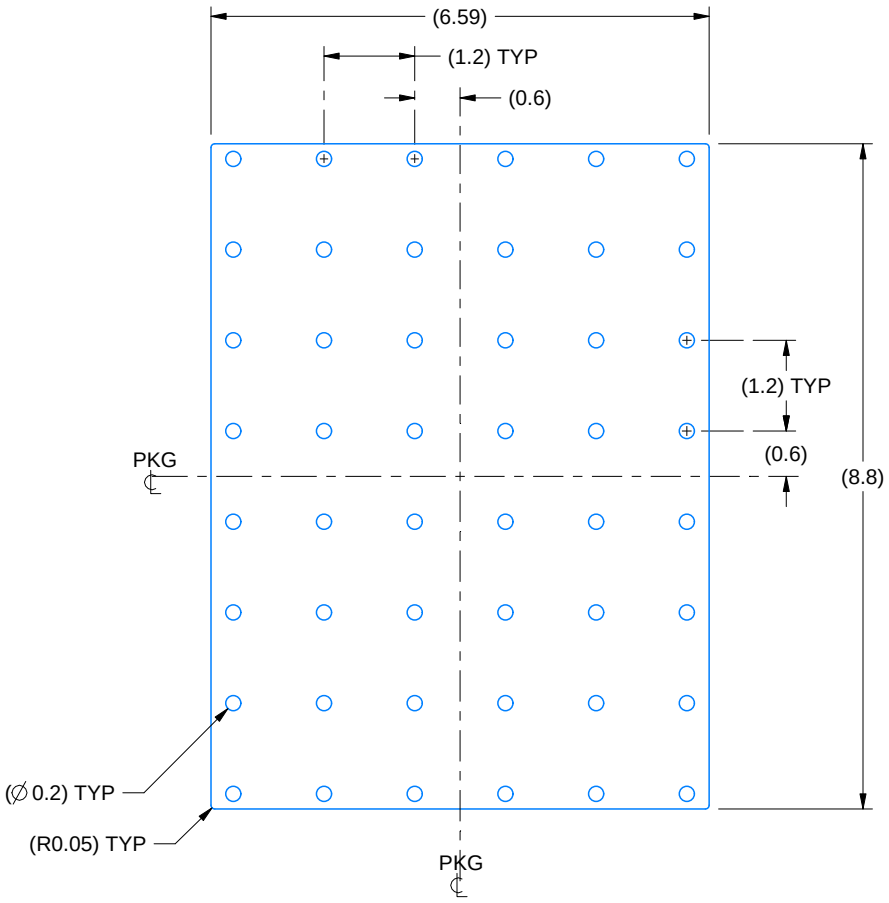
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid is connected to Heatsink.
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X

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