TPS7B63-Q1 汽车、300mA、40V 高压超低静态电流看门狗 LDO

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 温度等级 1：–40°C 至 125°C，T_A
- 最大输出电流：300mA
- 4V 至 40V 宽 V_{IN} 输入电压范围，瞬态电压高达 45V
- 固定 3.3V 和 5V 输出
- 最大压降电压：400mV (300mA)
- 在宽电容（4.7µF 至 500µF）和 ESR（0.001Ω 至 20Ω）范围内，与输出电容器搭配使用时可保持稳定
- 低静态电流 ($I_{(Q)}$)：
  - EN 为低电平时 < 4µA（关断模式）
  - 轻负载（$\overline{WD\_EN}$ 为高电平）时具有 19µA 的典型值（看门狗禁用）
- 可配置为窗口看门狗或标准看门狗
- 开闭窗口比率可配置为 1:1 或 8:1
- 完全可调的看门狗周期（从 10ms 至 500ms）
- 看门狗周期精度为 10%
- 专用 $\overline{WD\_EN}$ 引脚，用于控制看门狗开关
- 完全可调的电源正常阈值和电源正常延迟周期
- 针对 UVLO 的低输入电压跟踪功能
- 集成故障保护
  - 过载电流限制保护
  - 热关断
- 功能安全型
  - 提供协助功能安全系统设计的文件
- 16 引脚 HTSSOP 封装

2 应用

- 汽车 MCU 电源
- 车身控制模块 (BCM)
- 座椅舒适模块
- EV 和 HEV 电池管理系统 (BMS)
- 电子换挡器
- 变速箱
- 电动助力转向 (EPS)

3 说明

在汽车微控制器或微处理器电源应用中，看门狗用于监测微控制器的工作状态，以防止软件失控。确保系统的可靠性，必须使看门狗与微控制器彼此独立。

TPS7B63-Q1 是 300mA 看门狗低压降稳压器 (LDO)，额定工作电压高达 40V，轻负载条件下的典型静态电流仅为 19µA。该器件集成了可编程功能，用于选择窗口看门狗或标准看门狗，并使用外部电阻设置看门狗时间，精度在 10% 以内。

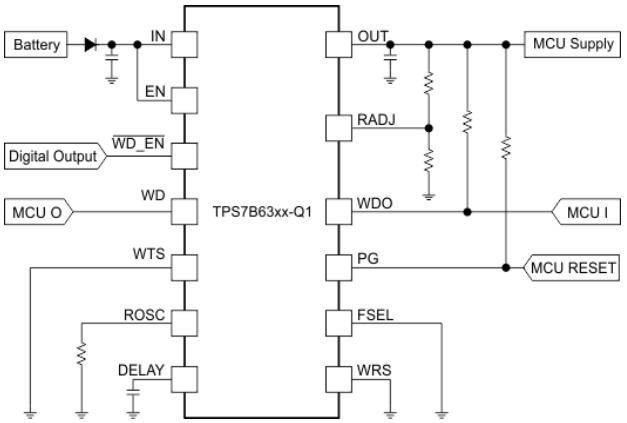
封装信息

器件型号	封装(1)	封装尺寸(2)
TPS7B63-Q1	PWP（HTSSOP，16）	5mm × 6.4mm

(1) 如需更多信息，请参阅*机械、封装和可订购信息*。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

器件信息

器件型号	输出电压	封装
TPS7B6333-Q1	固定 3.3V	HTSSOP (16)
TPS7B6350-Q1	固定 5V	



典型应用原理图

TPS7B63-Q1 上的 PG 引脚指示输出电压何时达到稳定且处于稳压状态。电源正常延迟周期和电源正常阈值可通过选择外部元件进行调整。这些器件还具有集成的短路和过流保护功能。上述特性组合使得该器件极具灵活性，旨在为汽车应用中的微控制器供电。

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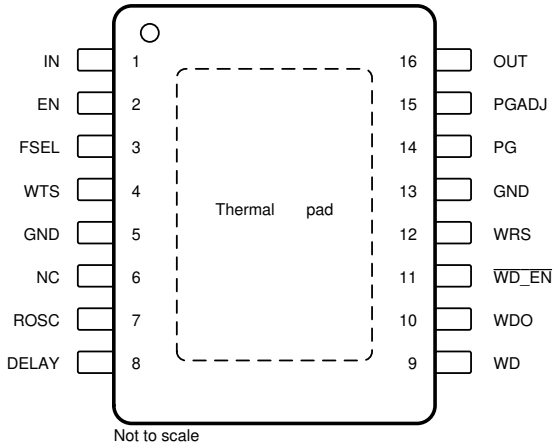
4 Pin Configuration and Functions



NC - No internal connection

图 4-1. PWP PowerPAD™ Package, 16-Pin HTSSOP With Exposed Thermal Pad (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
DELAY	8	O	Power-good delay period adjustment pin. Connect this pin with a capacitor to ground to adjust the power-good delay time.
EN	2	I	Device enable pin. Pull this pin down to low-level voltage to disable the device. Pull this pin up to high-level voltage to enable the device.
FSEL	3	I	Internal oscillator frequency selection pin. Pull this pin down to low-level voltage to select the high-frequency oscillator. Pull this pin up to high-level voltage to select the low-frequency oscillator.
GND	5, 13	—	Ground reference
IN	1	I	Device input power-supply pin
NC	6	—	Not connected
OUT	16	O	Device 3.3-V or 5-V regulated output voltage pin
PG	14	O	Power-good pin. Open-drain output pin. Pull this pin up to V_{OUT} or to a reference through a resistor. When the output voltage is not ready, this pin is pulled down to ground.
PGADJ	15	I	Power-good threshold adjustment pin. Connect a resistor divider between the PGADJ and OUT pins to set the power-good threshold. Connect this pin to ground to set the threshold to 91.6% of output voltage V_{OUT}.
ROSC	7	O	Watchdog timer adjustment pin. Connect a resistor between the ROSC pin and the GND pin to set the duration of the watchdog monitor. Leaving this pin open or connecting this pin to ground results in the watchdog reporting a fault at the watchdog output (WDO).
WD	9	I	Watchdog service-signal input pin.
WDO	10	O	Watchdog status pin. Open-drain output pin. Pull this pin up to OUT or a reference voltage through a resistor. When watchdog fault occurs, this pin is pulled down to a low-level voltage.
$\overline{\text{WD\_EN}}$	11	I	Watchdog enable pin. Pull this pin down to a low level to enable the watchdog. Pull this pin up to a high level to disable the watchdog.
WRS	12	I	Window ratio selection pin (only applicable for the window watchdog). Pull this pin down to a low level to set the open:closed window ratio to 1:1. Pull this pin up to high level to set the open:closed window ratio to 8:1.
WTS	4	I	Watchdog type-selection pin. To set the window watchdog, connect this pin to the GND pin. To set the standard watchdog, pull this pin high.
Thermal pad	—	—	Solder to board to improve the thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
Unregulated input	IN, EN	–0.3	45	V
Internal oscillator reference voltage	ROSC	–0.3	7	V
Power-good delay-timer output	DELAY	–0.3	7	V
Regulated output	OUT	–0.3	7	V
Power-good output voltage	PG	–0.3	7	V
Watchdog status output voltage	WDO	–0.3	7	V
Watchdog frequency selection, watchdog-type selection	FSEL, WTS	–0.3	45	V
Watchdog enable	$\overline{\text{WD\_EN}}$	–0.3	7	V
Watchdog service signal voltage	WD	–0.3	7	V
Window ratio selection	WRS	–0.3	7	V
Power-good threshold-adjustment voltage	PGADJ	–0.3	7	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), device HBM ESD classification level 2		±2000	V
		Charged-device model (CDM), per AEC Q100-011, device CDM ESD classification level C4B	All pins	±500	
			Corner pins (1, 14, 15, and 28)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

Over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Unregulated input	IN	4	40	V
40-V pins	EN, FSEL, WTS	0	V_{IN}	V
Regulated output	OUT	0	5.5	V
Power good, watchdog status, reference oscillator	PG, WDO, ROSC	0	5.5	V
Low voltage pins	WD, $\overline{\text{WD\_EN}}$, PGADJ, DELAY, WRS	0	5.5	V
Output current		0	300	mA
Ambient temperature, T_A		–40	125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS7B63-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

V_{IN} = 14 V, $C_{OUT} \geq$ 4.7 µF, 1 mΩ < ESR < 20 Ω, and T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
V_{IN}	Input voltage		4		40	V
$I_{(SLEEP)}$	Input sleep current	EN = OFF			4	µA
$I_{(Q)}$	Input quiescent current	V_{IN} = 5.6 V to 40 V for fixed 5-V V_{OUT}; V_{IN} = 4 V to 40 V for fixed 3.3-V V_{OUT}; EN = ON; watchdog disabled; I_{OUT} < 1 mA; T_J < 80°C		19	29.6	µA
		V_{IN} = 5.6 V to 40 V for fixed 5-V V_{OUT}; V_{IN} = 4 V to 40 V for fixed 3.3-V V_{OUT}; EN = ON; watchdog enabled; I_{OUT} < 1 mA		28	42	
		V_{IN} = 5.6 V to 40 V for fixed 5-V V_{OUT}; V_{IN} = 4 V to 40 V for fixed 3.3-V V_{OUT}; EN = ON; watchdog enabled; I_{OUT} < 100 mA		78	98	
$V_{(UVLO)}$	Undervoltage lockout, falling	Ramp V_{IN} down until output is turned off			2.6	V
$V_{(UVLO\_HYST)}$	UVLO hysteresis			0.5		V
ENABLE INPUT, WATCHDOG TYPE SELECTION AND FSEL (EN, WTS, AND FSEL)						
V_{IL}	Low-level input voltage				0.7	V
V_{IH}	High-level input voltage		2			V
V_{hys}	Hysteresis			150		mV
WATCHDOG ENABLE ($\overline{WD\_EN}$ PIN)						
V_{IL}	Low-level input threshold voltage for watchdog enable pin	Watchdog enabled			0.7	V
V_{IH}	High-level input threshold voltage for watchdog enable pin	Watchdog disabled	2			V
I_{WD_EN}	Pulldown current for watchdog enable pin	V_{WD_EN} = 5 V			3	µA
REGULATED OUTPUT (OUT)						
V_{OUT}	Regulated output	V_{IN} = 5.6 V to 40 V for fixed 5-V V_{OUT}, V_{IN} = 4 V to 40 V for fixed 3.3-V V_{OUT}, I_{OUT} = 0 to 300 mA, –40°C ≤ T_J ≤ 125°C	–2%		2%	
		V_{IN} = 5.6 V to 40 V for fixed 5-V V_{OUT}; V_{IN} = 4 V to 40 V for fixed 3.3-V V_{OUT}; I_{OUT} = 0 to 300 mA	–2.5%		2.5%	

5.5 Electrical Characteristics（续）

V_{IN} = 14 V, C_{OUT} ≥ 4.7 µF, 1 mΩ < ESR < 20 Ω, and T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	V_{IN} = 5.6 V to 40 V			10	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	I_{OUT} = 1 mA to 300 mA			20	mV
$V_{(dropout)}$	Dropout voltage (V_{IN} – V_{OUT})	I_{OUT} = 300 mA(2)		300	400	mV
		I_{OUT} = 200 mA(2)		170	325	
I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
$I_{(LIM)}$	Output current limit	V_{OUT} shorted to ground, V_{IN} = 5.6 V to 40 V	301	680	1000	mA
PSRR	Power-supply ripple rejection(1)	I_{OUT} = 100 mA; C_{OUT} = 10 µF; frequency (f) = 100 Hz		60		dB
		I_{OUT} = 100 mA; C_{OUT} = 10 µF; frequency (f) = 100 kHz		40		
POWER-GOOD (PG, PGADJ)						
$V_{OL(PG)}$	PG output, low voltage	I_{OL} = 5 mA, PG pulled low			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	PG pulled to V_{OUT} through a 10-kΩ resistor			1	µA
$V_{(PG\_TH)}$	Default power-good threshold	V_{OUT} powered above the internally set tolerance, PGADJ pin shorted to ground	89.6	91.6	93.6	% of V_{OUT}
$V_{(PG\_HYST)}$	Power-good hysteresis	V_{OUT} falling below the internally set tolerance hysteresis		2		% of V_{OUT}
PGADJ						
$V_{(PGADJ\_TH)}$	Switching voltage for the power-good adjust pin	V_{OUT} is falling	1.067	1.1	1.133	V
POWER-GOOD DELAY						
$I_{(DLY\_CHG)}$	DELAY capacitor charging current		3	5	10	µA
$V_{(DLY\_TH)}$	DELAY pin threshold to release PG high	Voltage at DELAY pin is ramped up	0.95	1	1.05	V
$I_{(DLY\_DIS)}$	DELAY capacitor discharging current	V_{DELAY} = 1 V	0.5			mA
CURRENT VOLTAGE REFERENCE (ROSC)						
V_{ROSC}	Voltage reference		0.95	1	1.05	V
WATCHDOG (WD, WDO, WRS)						
V_{IL}	Low-level threshold voltage for the watchdog input and window-ratio select	For WD and WRS pins			30	% of V_{OUT}
V_{IH}	High-level threshold voltage for the watchdog input and window-ratio select	For WD and WRS pins	70			% of V_{OUT}
$V_{(HYST)}$	Hysteresis			10		% of V_{OUT}
I_{WD}	Pulldown current for the WD pin	V_{WDO} = 5 V		2	4	µA
V_{OL}	Low-levlel watchdog output	I_{WDO} = 5 mA			0.4	V
I_{lkg}	WDO pin leakage current	WDO pin pulled to V_{OUT} through 10-kΩ resistor			1	µA
OPERATING TEMPERATURE RANGE						
T_J	Junction temperature		–40		150	°C
$T_{(SD)}$	Junction shutdown temperature			175		°C

5.5 Electrical Characteristics（续）

V_{IN} = 14 V, C_{OUT} ≥ 4.7 µF, 1 mΩ < ESR < 20 Ω, and T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{(HYST)}$	Hysteresis of thermal shutdown			25		°C

(1) Design information – not tested, determined by characterization.
(2) This test is done with V_{OUT} in regulation, measuring the V_{IN} – V_{OUT} when V_{OUT} drops by 100 mV from the rated output voltage at the specified load.

5.6 Switching Characteristics

V_I = 14 V, $C_O \geq$ 4.7 µF, 1 mΩ < ESR < 20 Ω, and T_J = –40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-GOOD DELAY (DELAY)						
$t_{(DEGLITCH)}$	Power-good deglitch time		50	180	250	µs
$t_{(DLY\_FIX)}$	Fixed power-good delay	No capacitor connect at DELAY pin		248	900	µs
$t_{(DLY)}$	Power-on-reset delay	Delay capacitor value: $C_{(DELAY)}$ = 100 nF		20		ms
WATCHDOG (WD, WDO, WRS)						
$t_{(WD)}$	Watchdog window duration	$R_{(ROSC)}$ = 20 kΩ ±1%, FSEL = LOW	9	10	11	ms
		$R_{(ROSC)}$ = 20 kΩ ±1%, FSEL = HIGH	45	50	55	
$t_{(WD\_TOL)}$	Tolerance of watchdog window duration using external resistor	Excludes tolerance of $R_{(ROSC)}$ = 20 kΩ to 100 kΩ	–10%		10%	
$t_{p(WD)}$	Watchdog service-signal duration		100			µs
$t_{(WD\_HOLD)}$	Watchdog output resetting time (percentage of settled watchdog window duration)			20		% of $t_{(WD)}$
$t_{(WD\_RESET)}$	Watchdog output resetting time	$R_{(ROSC)}$ = 20 kΩ ± 1%, FSEL = LOW	1.8	2	2.2	ms
		$R_{(ROSC)}$ = 20 kΩ ± 1%, FSEL = HIGH	9	10	11	

5.7 Typical Characteristics

at V_{IN} = 14 V, V_{EN} ≥ 2 V, and T_J = –40°C to +150°C (unless otherwise noted)

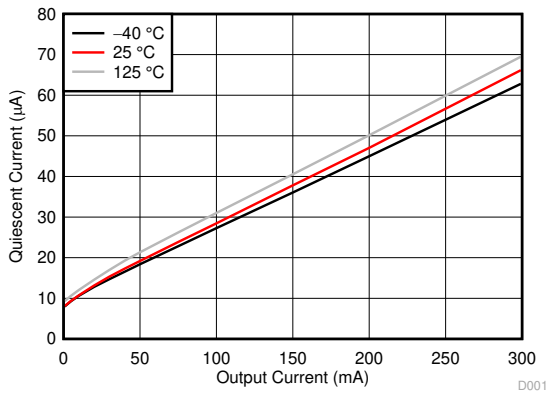


图 5-1. Quiescent Current vs Output Current

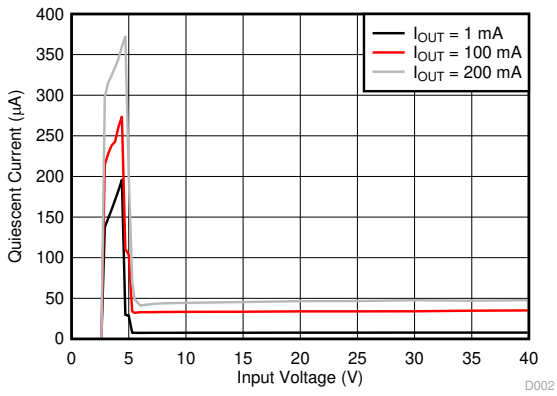


图 5-2. Quiescent Current vs Input Voltage

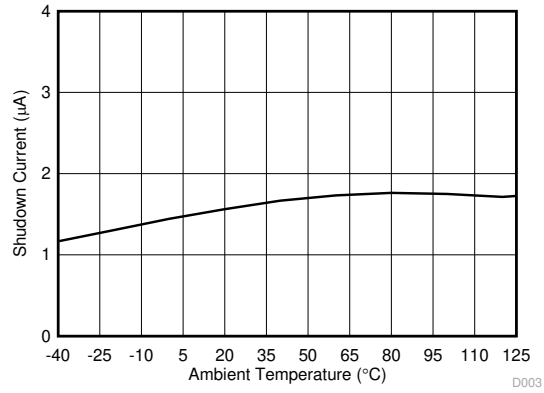


图 5-3. Shutdown Current vs Ambient Temperature

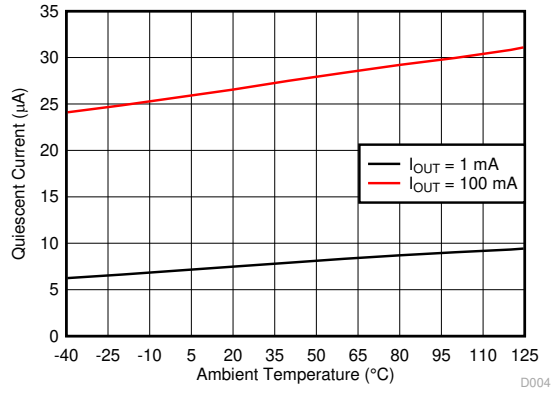


图 5-4. Quiescent Current vs Ambient Temperature

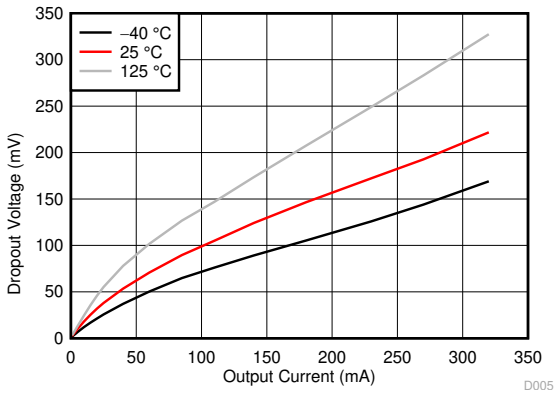
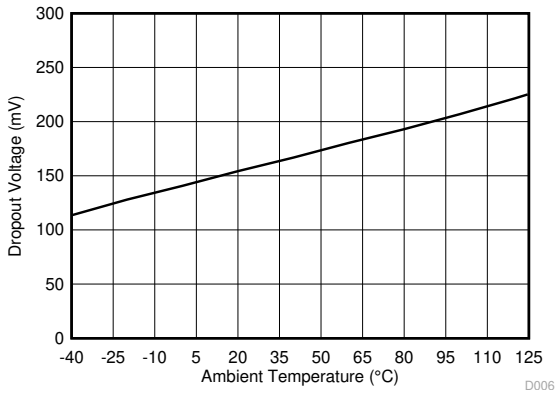


图 5-5. Dropout Voltage vs Output Current

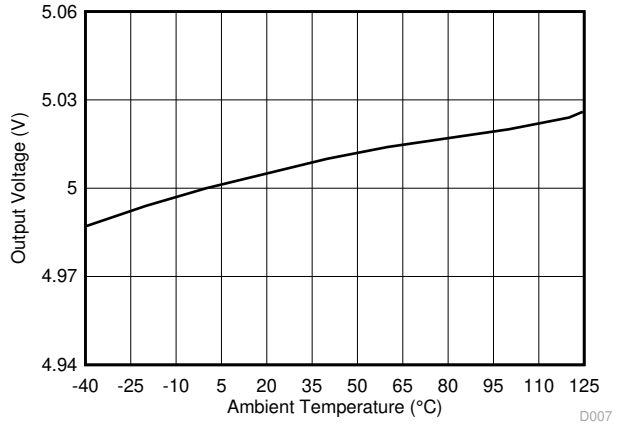


I_{OUT} = 200 mA

图 5-6. Dropout Voltage vs Ambient Temperature

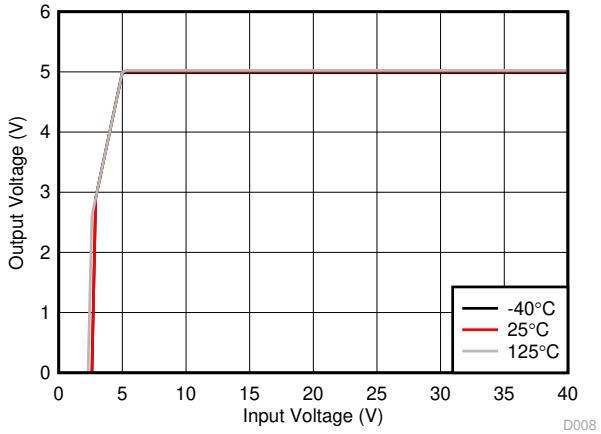
5.7 Typical Characteristics (continued)

at V_{IN} = 14 V, $V_{EN} \geq$ 2 V, and T_J = –40°C to +150°C (unless otherwise noted)



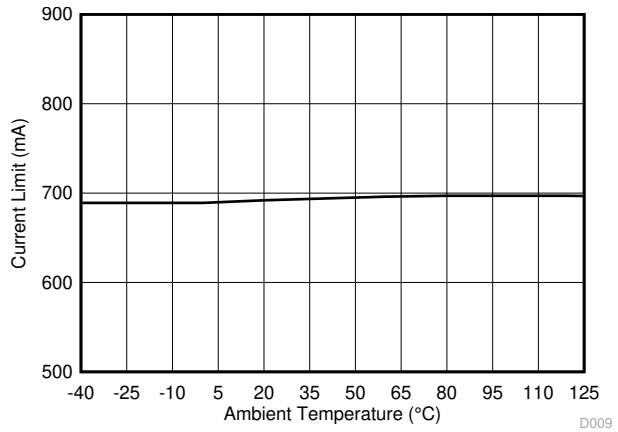
V_{OUT} = 5 V

图 5-7. Output Voltage vs Ambient Temperature



V_{OUT} = 5 V

图 5-8. Output Voltage vs Input Voltage



V_{IN} = 5.6 V

图 5-9. Output Current Limit (I_{LIM}) vs Ambient Temperature

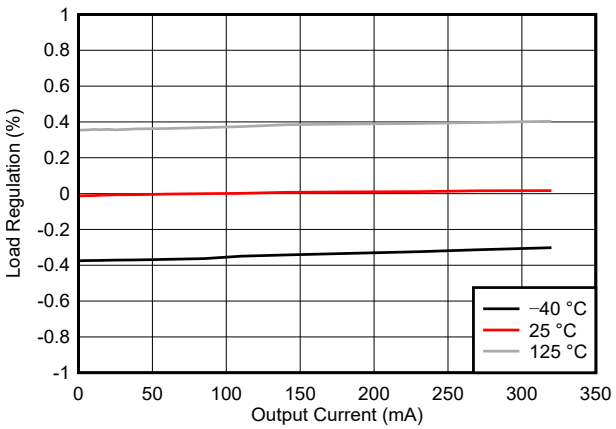


图 5-10. Load Regulation

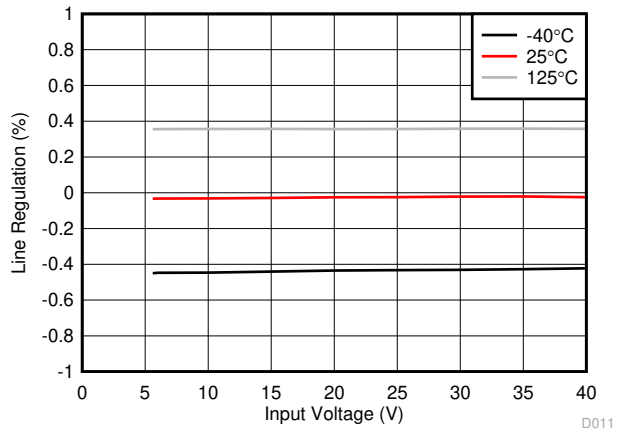
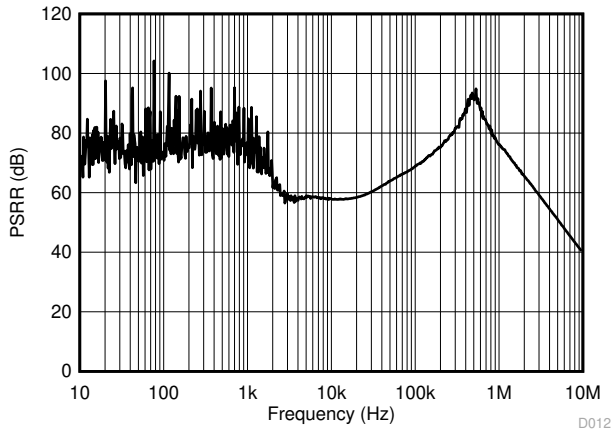


图 5-11. Line Regulation

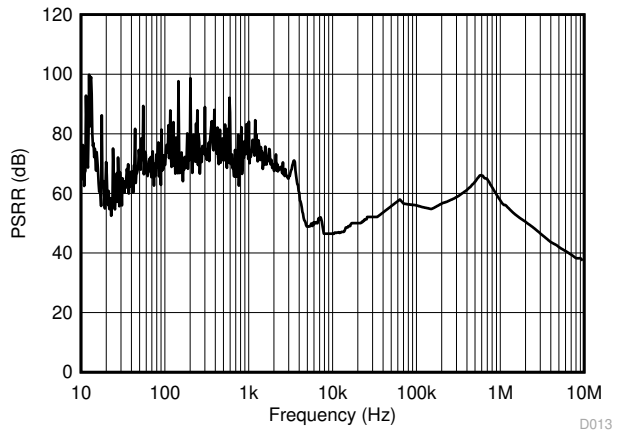


C_{OUT} = 10 µF, I_{OUT} = 1 mA, T_A = 25°C

图 5-12. PSRR vs Frequency

5.7 Typical Characteristics (continued)

at V_{IN} = 14 V, $V_{EN} \geq$ 2 V, and T_J = –40°C to +150°C (unless otherwise noted)



C_{OUT} = 10 µF, I_{OUT} = 100 mA, T_A = 25°C

图 5-13. PSRR vs Frequency

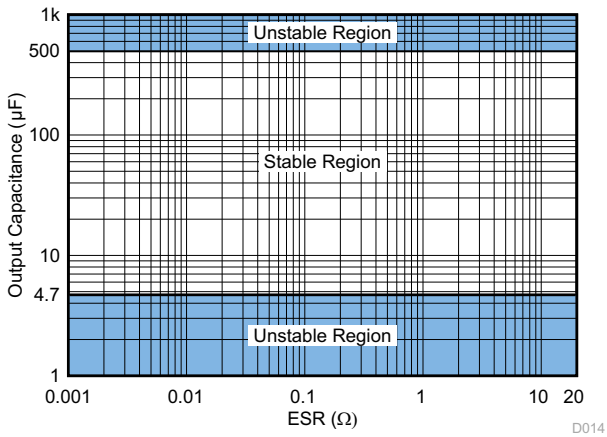
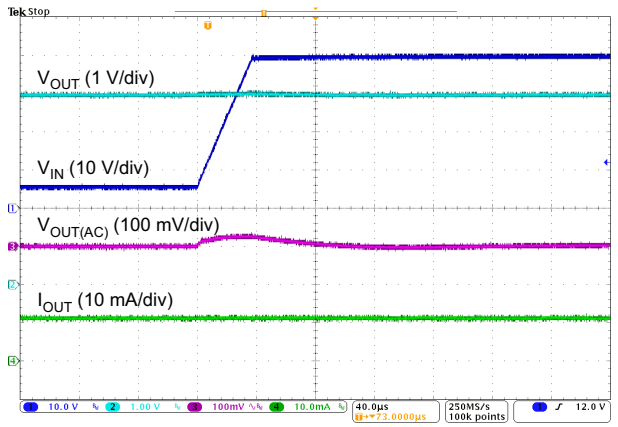
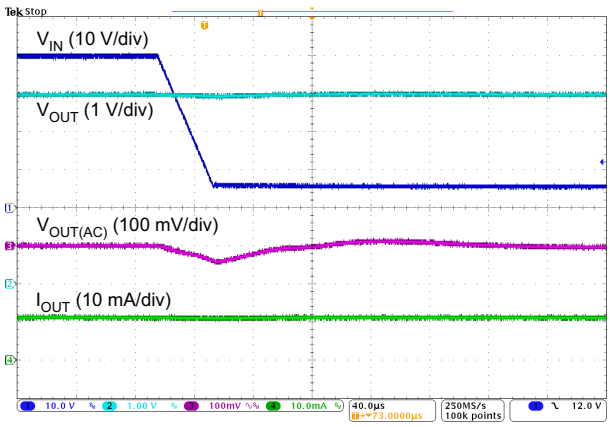


图 5-14. ESR Stability vs Output Capacitance



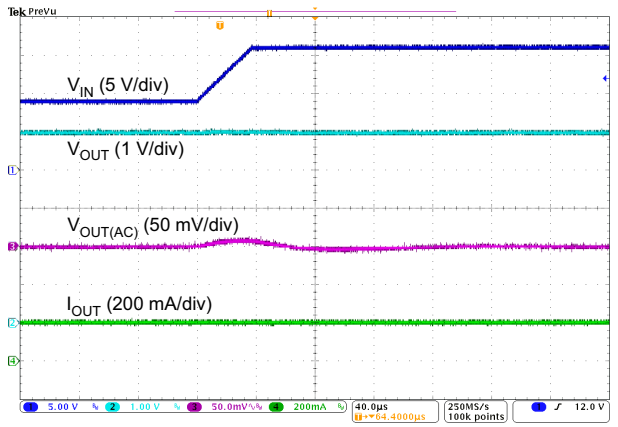
V_{IN} = 6 V to 40 V, V_{OUT} = 5 V, C_{OUT} = 10 µF, I_{OUT} = 1 mA

图 5-15. Line Transient



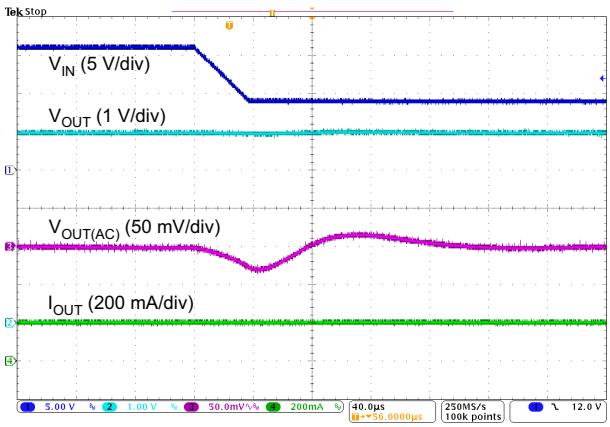
V_{IN} = 40 V to 6 V, V_{OUT} = 5 V, C_{OUT} = 10 µF, I_{OUT} = 1 mA

图 5-16. Line Transient



V_{IN} = 9 V to 16 V, V_{OUT} = 5 V, C_{OUT} = 10 µF, I_{OUT} = 200 mA

图 5-17. Line Transient

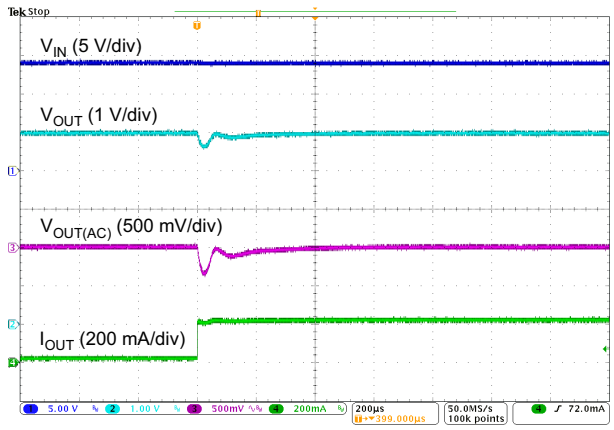


V_{IN} = 16 V to 9 V, V_{OUT} = 5 V, C_{OUT} = 10 µF, I_{OUT} = 200 mA

图 5-18. Line Transient

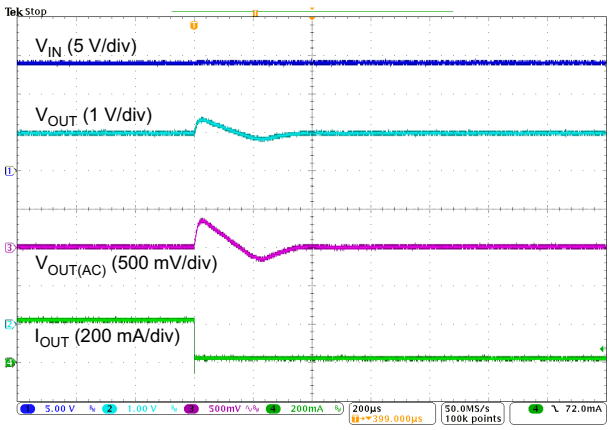
5.7 Typical Characteristics (continued)

at V_{IN} = 14 V, $V_{EN} \geqslant$ 2 V, and T_J = –40°C to +150°C (unless otherwise noted)



V_{OUT} = 5 V, C_{OUT} = 10 µF, I_{OUT} = 1 mA to 200 mA

图 5-19. Load Transient



V_{OUT} = 5 V, C_{OUT} = 10 µF, I_{OUT} = 200 mA to 1 mA

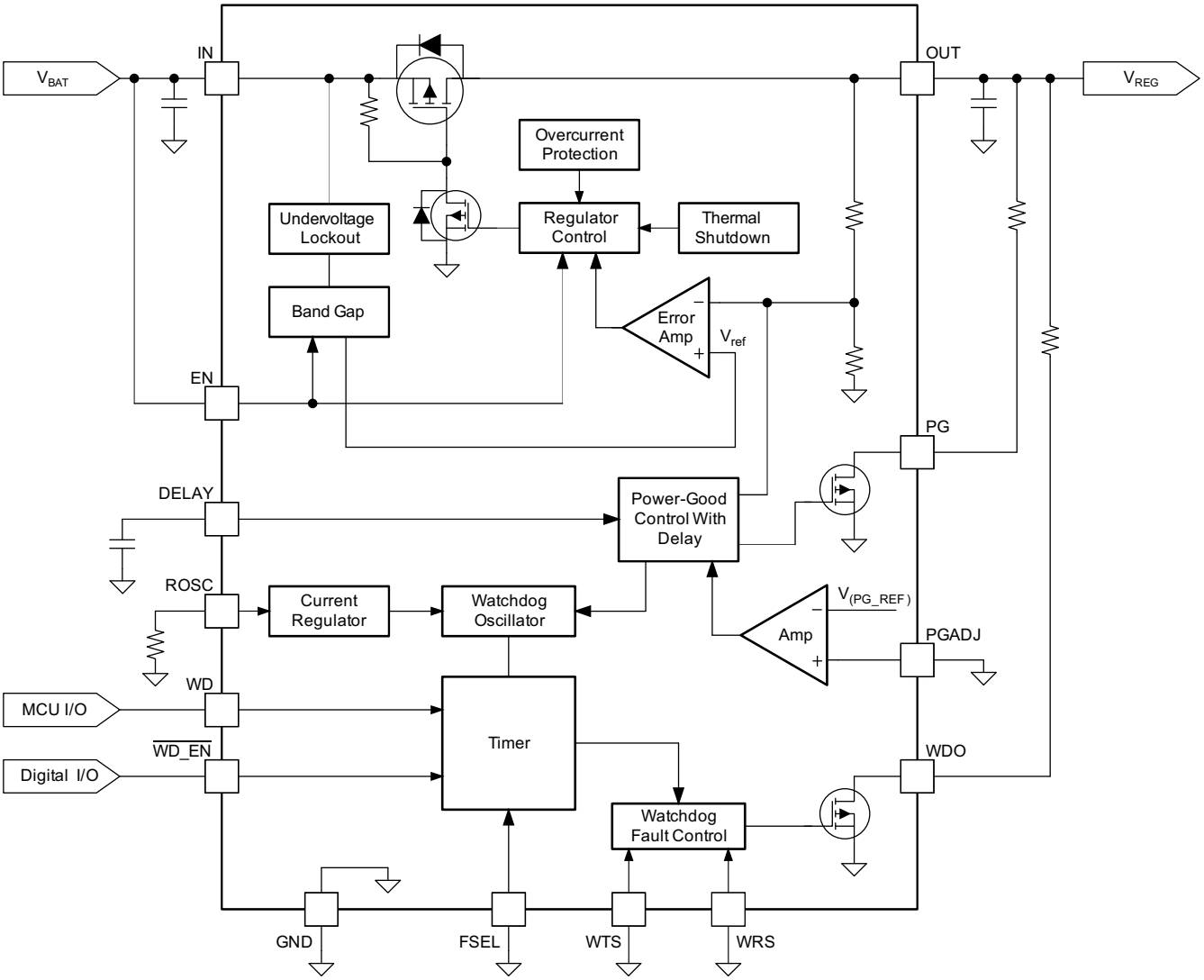
图 5-20. Load Transient

6 Detailed Description

6.1 Overview

The TPS7B63-Q1 is a 300-mA, 40-V monolithic low-dropout linear voltage regulator with integrated watchdog and adjustable power-good threshold functionality. This voltage regulator consumes only 19-µA quiescent current in light-load applications. Because of the adjustable power-good delay (also called power-on-reset delay) and the adjustable power-good threshold, this device is designed as a power supply for microprocessors and microcontrollers in automotive applications.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulator ON. Connect this input pin to an external microcontroller or a digital control circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

6.3.2 Adjustable Power-Good Threshold (PG, PGADJ)

The PG pin is an open-drain output with an external pullup resistor to the regulated supply, and the PGADJ pin is a power-good threshold adjustment pin. Connecting the PGADJ pin to GND sets the power-good threshold value to the default, $V_{(PG\_TH)}$. When V_{OUT} exceeds the default power-good threshold, the PG output turns high after the power-good delay period has expired. When V_{OUT} falls below $V_{(PG\_TH)} - V_{(PG\_HYST)}$, the PG output turns low after a short deglitch time.

The power-good threshold is also adjustable from 1.1 V to 5 V by using an external resistor divider between PGADJ and OUT. The threshold can be calculated using 方程式 1:

$$V_{(PG\_ADJ)\,falling} = V_{(PGADJ\_TH)\,falling} \times \frac{R1 + R2}{R2}$$
$$V_{(PG\_ADJ)\,risng} = \left[V_{(PGADJ\_TH)\,falling} + 26\ mV\ (typ) \right] \times \frac{R1 + R2}{R2} \quad (1)$$

where

- $V_{(PG\_ADJ)}$ is the adjustable power-good threshold
- $V_{(PG\_REF)}$ is the internal comparator reference voltage of the PGADJ pin, 1.1 V typical, 2% accuracy specified under all conditions

By setting the power-good threshold $V_{(PG\_ADJ)}$, when V_{OUT} exceeds this threshold, the PG output turns high after the power-good delay period has expired. When V_{OUT} falls below $V_{(PG\_ADJ)} - V_{(PG\_HYST)}$, the PG output turns low after a short deglitch time. 图 6-1 shows typical hardware connections for the PGADJ pin and DELAY pin.

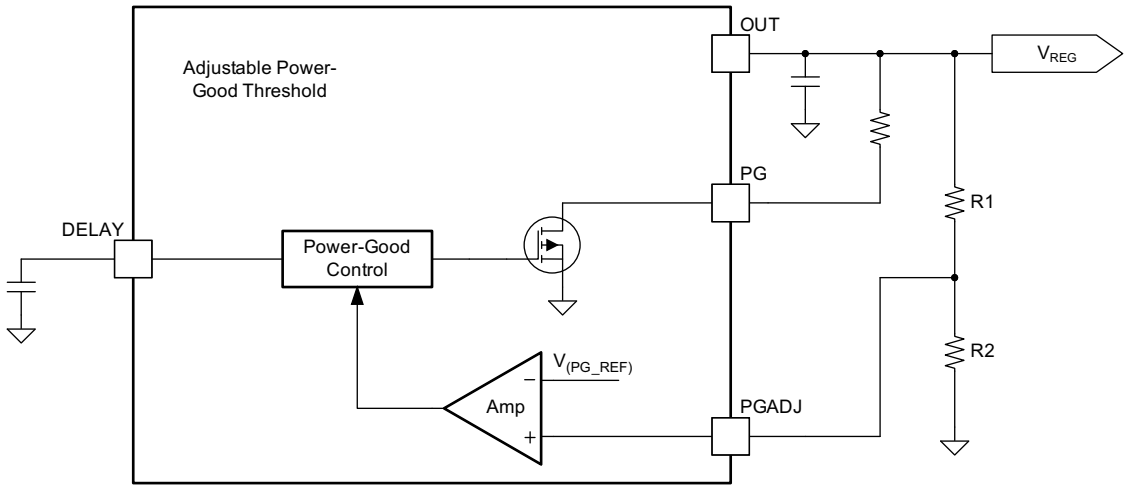


图 6-1. Adjustable Power-Good Threshold

6.3.3 Adjustable Power-Good Delay Timer (DELAY)

The power-good delay period is a function of the value set by an external capacitor on the DELAY pin before turning the PG pin high. 图 6-2 illustrates typical power-good and delay behavior. Connecting an external capacitor from this pin to GND sets the power-good delay period. The constant current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator, and 方程式 2 determines the power-good delay period:

$$t_{(DLY)} = t_{dly\_fix} + \frac{C_{DELAY} \; x \; 1V}{5 \; \mu A} \tag{2}$$

where

- $t_{(DLY)}$ is the adjustable power-good delay period
- C_{DELAY} is the value of the power-good delay capacitor

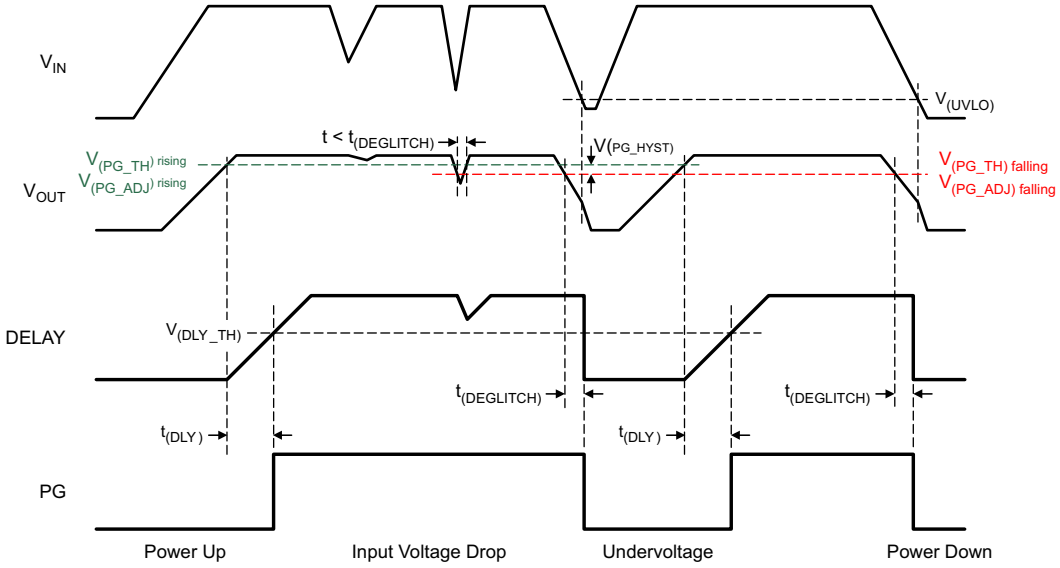


图 6-2. Power Up and Conditions for Activating Power-Good

If the DELAY pin is open, the default delay time is $t_{(DLY\_FIX)}$.

6.3.4 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit to shut down the output if the input voltage falls below an internal UVLO threshold, $V_{(UVLO)}$. This ensures that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient which drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence once the input voltage is above the required level.

6.3.5 Current Limit

This device features current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This feature protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

6.3.6 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. The junction temperature

exceeding the TSD trip point causes the output to turn off. When the junction temperature falls below the $T_{(SD)}$ – $T_{(HYST)}$, the output turns on again.

6.3.7 Integrated Watchdog

This device has an integrated watchdog with fault (WDO) output option. Both window watchdog and standard watchdog are available in one device. The watchdog operation, service fault conditions, and differences between window watchdog and standard watchdog are described as follows.

6.3.7.1 Window Watchdog (WTS, ROSC, FSEL and WRS)

This device works in the window watchdog mode when the watchdog type selection (WTS) pin is connected to a to low voltage level. The user can set the duration of the watchdog window by connecting an external resistor (R_{ROSC}) to ground at the ROSC pin and setting the voltage level at the FSEL pin. The current through the R_{ROSC} resistor sets the clock frequency of the internal oscillator. The user can adjust the duration of the watchdog window (the watchdog timer period) by changing the resistor value. A high voltage level at the FSEL pin sets the watchdog window duration to 5 times as long as that of a low voltage level with same external component configuration.

The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency, as shown by the following equations:

FSEL low

$$t_{(WD)} = R_{ROSC} \times 0.5 \times 10^{-6} \quad (3)$$

FSEL high

$$t_{(WD)} = R_{ROSC} \times 2.5 \times 10^{-6} \quad (4)$$

Watchdog initialization

$$t_{(WD\_INI)} = 8 \times t_{(WD)} \quad (5)$$

Open and closed windows

$$t_{(WD)} = t_{(OW)} + t_{(CW)} \quad (6)$$

WRS low

$$t_{(OW)} = t_{(CW)} = 50\% \times t_{(WD)} \quad (7)$$

WRS high

$$t_{(OW)} = 8 \times t_{(CW)} = (8 / 9) \times t_{(WD)} \quad (8)$$

where:

- $t_{(WD)}$ is the duration of the watchdog window
- R_{ROSC} is the resistor connected at the ROSC pin
- $t_{(WD\_INI)}$ is the duration of the watchdog initialization
- $t_{(OW)}$ is the duration of the open watchdog window
- $t_{(CW)}$ is the duration of the closed watchdog window

For all the foregoing items, the unit of resistance is Ω and the unit of time is s.

表 6-1 illustrates several periods of watchdog window with typical conditions.

表 6-1. Several Typical Periods of Watchdog Window

FSEL	$R_{(ROSC)}$ (kΩ)	$I_{(ROSC)}$ (μA)	$t_{(WD)}$ (ms)	WATCHDOG PERIOD TOLERANCE
High	200	5	500	15%
	100	10	250	10%
	50	20	125	
	40	25	100	
	25	40	62.5	
	20	50	50	
Low	100	10	50	10%
	50	20	25	
	40	25	20	
	25	40	12.5	
	20	50	10	

As illustrated in 图 6-3, each watchdog window consists of an open window and a closed window. While the window ratio selection (WRS) pin is low, each open window ($t_{(OW)}$) and closed window ($t_{(CW)}$) has a width approximately 50% of the watchdog window ($t_{(WD)}$). While the WRS pin is high, the ratio between open window and closed window is about 8:1. However, there is an exception to this; the first open window after watchdog initialization ($t_{(WD\_INI)}$) is eight times the duration of the watchdog window. The watchdog must receive the service signal (by software, external microcontroller, and so forth) during this initialization open window.

A watchdog fault occurs when servicing the watchdog during a closed window, or not servicing during an open window.

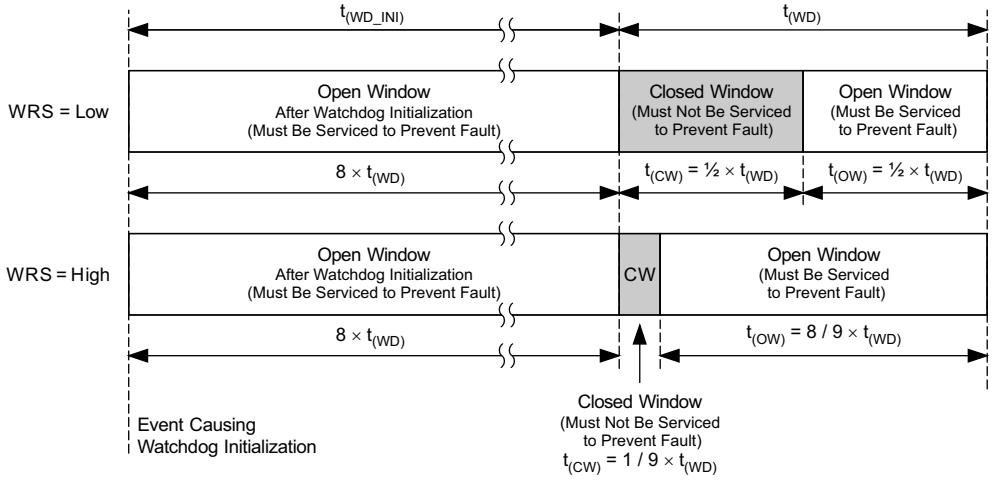


图 6-3. Watchdog Initialization, Open Window and Closed Window

6.3.7.2 Standard Watchdog (WTS, ROSC and FSEL)

This device works in the standard watchdog mode when the watchdog type selection (WTS) pin is connected to a high voltage level. The same as in window watchdog mode, the user can set the duration of the watchdog window by adjusting the external resistor (R_{ROSC}) value at the ROSC pin and setting the voltage level at the FSEL pin. The current through the R_{ROSC} resistor sets the clock frequency of the internal oscillator. The user can adjust the duration of the watchdog window (the watchdog timer period) by changing the resistor value. A high voltage level at the FSEL pin sets the watchdog window duration to 5 times as long as that of a low voltage level with same external component configuration.

The duration of the watchdog window and the duration of the fault output are multiples of the internal oscillator frequency, as shown by the following equations:

FSEL low

$$t_{(WD)} = R_{ROSC} \times 0.5 \times 10^{-6} \quad (9)$$

FSEL high

$$t_{(WD)} = R_{ROSC} \times 2.5 \times 10^{-6} \quad (10)$$

Watchdog initialization

$$t_{(WD\_INI)} = 8 \times t_{(WD)} \quad (11)$$

where:

- $t_{(WD)}$ is the duration of the watchdog window
- R_{ROSC} is the resistor connected at the ROSC pin
- $t_{(WD\_INI)}$ is the duration of the watchdog initialization

For all the foregoing items, the unit of resistance is Ω and the unit of time is s

Compared with window watchdog, there is no closed window in standard watchdog mode. The standard watchdog receives a service signal at any time within the watchdog window. The watchdog fault occurs when not servicing watchdog during the watchdog window.

6.3.7.3 Watchdog Service Signal and Watchdog Fault Outputs (WD and WDO)

The watchdog service signal (WD) must stay high for at least 100 µs. The WDO pin is the fault output terminal and is tied high through a pullup resistor to a regulated output supply. When a watchdog fault occurs, the device momentarily pulls WDO low for a duration of $t_{(WD\_HOLD)}$.

$$t_{(WD\_HOLD)} = 20\% \times t_{(WD)} \quad (12)$$

6.3.7.4 ROSC Status Detection (ROSC)

When a watchdog function is enabled, if the ROSC pin is shorted to GND or open, the watchdog output (WDO) pin remains low, indicating a fault status. If the watchdog function is disabled, ROSC pin status detection does not work.

6.3.7.5 Watchdog Enable (PG and $\overline{\text{WD\_EN}}$)

When PG (power good) is high, an external microcontroller or a digital circuit can apply a high or low logic signal to the $\overline{\text{WD\_EN}}$ pin to disable or enable the watchdog. A low input to this pin turns the watchdog on, and a high input turns the watchdog off. If PG is low, the watchdog is disabled and the watchdog-fault output (WDO) pin stays in the high-impedance state.

6.3.7.6 Watchdog Initialization

On power up and during normal operation, the watchdog initializes under the conditions shown in 表 6-2.

表 6-2. Conditions for Watchdog Initialization

EDGE	WHAT CAUSES THE WATCHDOG TO INITIALIZE
↑	Rising edge of PG (power good) while the watchdog is in the enabled state, for example, during soft power up
↓	Falling edge of $\overline{\text{WD\_EN}}$ while PG is already high, for example, when the microprocessor enables the watchdog after the device is powered up
↑	Rising edge of WDO while PG is already high and the watchdog is in the enabled state, for example, right after a closed window is serviced

6.3.7.7 Window Watchdog Operation (WTS = Low)

The window watchdog is able to monitor whether the frequency of the watchdog service signal (WD) is within certain ranges. A watchdog low-voltage fault is reported when the frequency of the watchdog service signal is out of the setting range. 图 6-4 shows the window watchdog initialization and operation for the TPS7B63-Q1 (WRS is low). After the output voltage is in regulation and PG is high, the window watchdog becomes enabled when an external signal pulls $\overline{WD\_EN}$ (the watchdog enable pin) low. This causes the watchdog to initialize and wait for a service signal during the first initialization window for 8 times the duration of $t_{(WD)}$. A service signal applied to the WD pin during the initialization open window resets the watchdog counter and a closed window starts. To prevent a fault condition from occurring, watchdog service must not occur during the closed window. Watchdog service must occur during the following open window to prevent a fault condition from occurring. The fault output (WDO), externally pulled up to V_{OUT} (typical), stays high as long as the watchdog receives a proper service signal and there is no other fault condition.

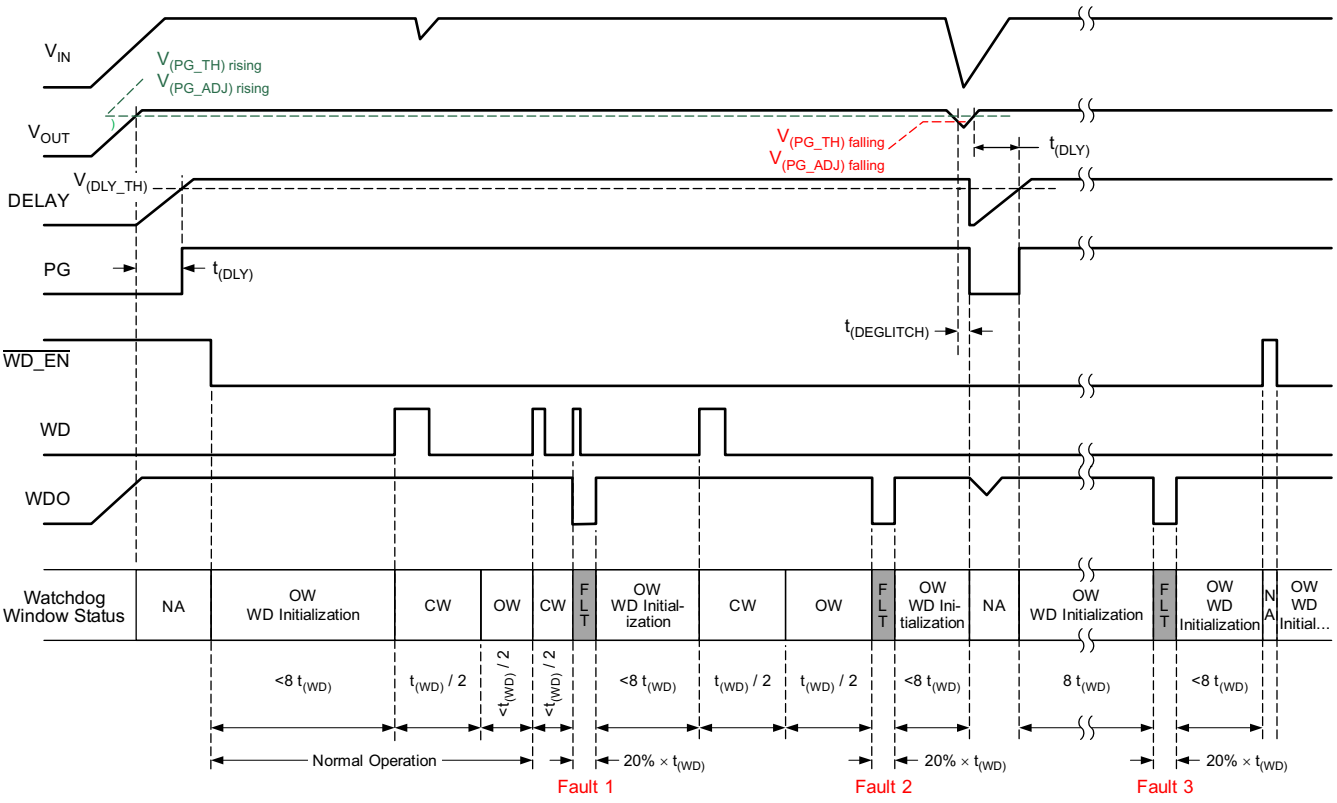


图 6-4. Window Watchdog Operation

Three different fault conditions occur in 图 6-4:

- Fault 1: The watchdog service signal is received during the closed window. The WDO is triggered once, receiving a WD rising edge during the closed window.
- Fault 2: The watchdog service signal is not received during the open window. WDO is triggered after the maximum open-window duration $t_{(WD)}$ / 2.
- Fault 3: The watchdog service signal is not received during the WD initialization. WDO is triggered after the maximum initialization window duration 8 × $t_{(WD)}$.

6.3.7.8 Standard Watchdog Operation (WTS = High)

The standard watchdog is able to monitor whether the frequency of the watchdog service signal (WD) is lower than a certain value. A watchdog low-voltage fault is reported when the frequency of the watchdog service signal is lower than the set value.

图 6-5 shows the standard watchdog initialization and operation for the TPS7B63-Q1. Similar to the window watchdog, after output the voltage is in regulation and PG asserts high, the standard watchdog becomes enabled when an external signal pulls $\overline{WD\_EN}$ low. This causes the standard watchdog to initialize and wait for a service signal during the first initialization window for 8 times the duration of $t_{(WD)}$. A service signal applied to the WD pin during the first open window resets the watchdog counter and another open window starts. To prevent a fault condition from occurring, watchdog service must occur during the every open window to prevent a fault condition from occurring. The fault output (WDO), externally pulled up to V_{OUT} (typical), stays high as long as the watchdog receives proper service and there is not fault condition.

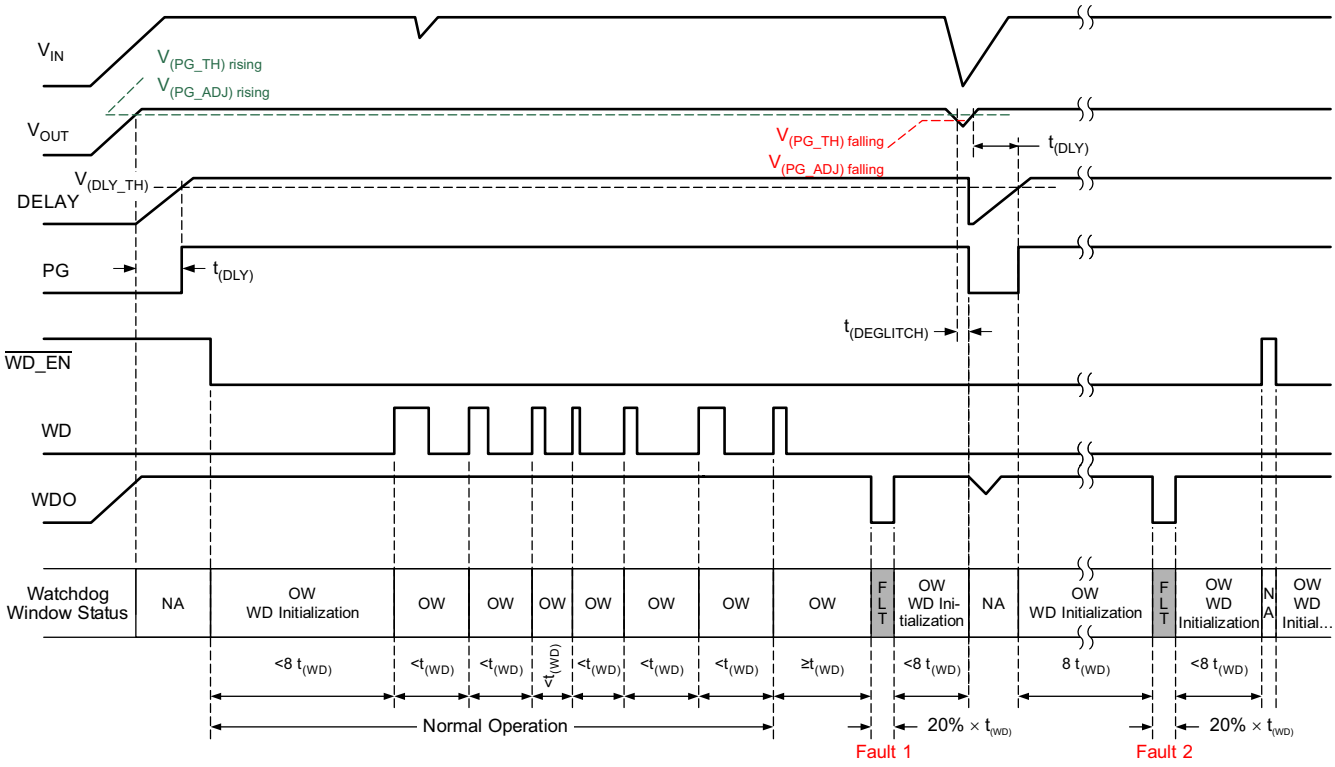


图 6-5. Standard Watchdog Operation

Two different fault conditions occur in 图 6-5:

- Fault 1: The watchdog service signal is not received during the open window. WDO is triggered after the maximum open-window duration $t_{(WD)}$.
- Fault 2: The watchdog service signal is not received during the WD initialization. WDO is triggered after the maximum initialization window duration 8 × $t_{(WD)}$.

6.4 Device Functional Modes

6.4.1 Operation With Input Voltage Lower Than 4 V

The device normally operates with input voltages above 4 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.6 V. At input voltages below the actual UVLO voltage, the device does not operate.

6.4.2 Operation With Input Voltage Higher Than 4 V

When the input voltage is greater than 4 V, if the input voltage is higher than the output set value plus the device dropout voltage, then the output voltage is equal to the set value. Otherwise, the output voltage is equal to the input voltage minus the dropout voltage.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TPS7B63-Q1 is a 300-mA low-dropout watchdog linear regulator with ultralow quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

7.2 Typical Application

图 7-1 shows a typical application circuit for the TPS7B63-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. TI recommends using a low-ESR ceramic capacitor with a dielectric of type X7R.

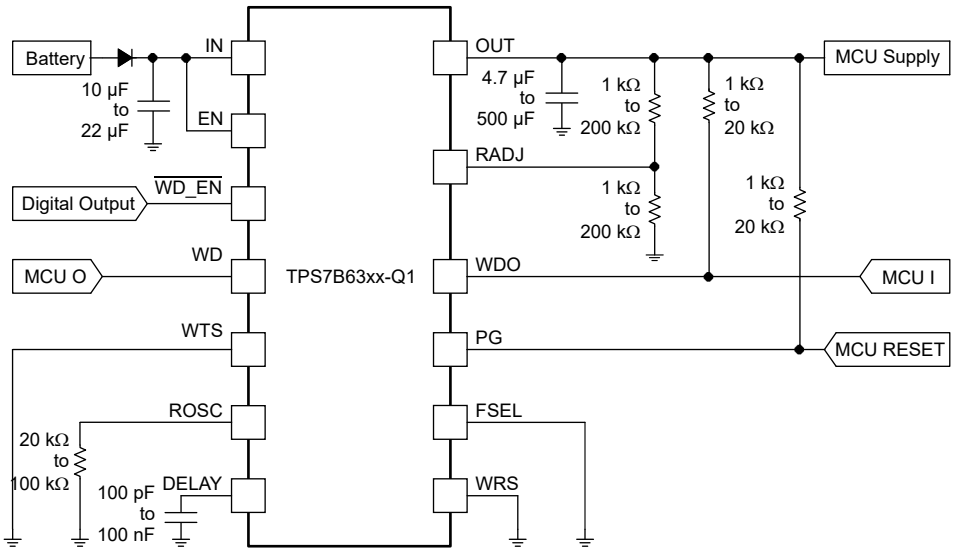


图 7-1. TPS7B63-Q1 Typical Application Schematic

7.2.1 Design Requirements

For this design example, use the parameters listed in 表 7-1.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	4 V to 40 V for TPS7B6333-Q1 5.6 V to 40 V for TPS7B6350-Q1
Input capacitor range	10 µF to 22 µF
Output voltage	3.3 V, 5 V
Output current rating	300 mA maximum
Output capacitor range	4.7 µF to 500 µF
Power-good threshold	Adjustable or fixed
Power-good delay capacitor	100 pF to 100 nF
Watchdog type	Standard watchdog or window watchdog
Watchdog window periods	10 ms to 500 ms

7.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output voltage
- Output current
- Power-good threshold
- Power-good delay capacitor
- Watchdog type
- Watchdog window period

7.2.2.1 Input Capacitor

When using a TPS7B63-Q1, TI recommends adding a 10-µF to 22-µF capacitor with a 0.1 µF ceramic bypass capacitor in parallel at the input to keep the input voltage stable. The voltage rating must be greater than the maximum input voltage.

7.2.2.2 Output Capacitor

Ensuring the stability of the TPS7B63-Q1 requires an output capacitor with a value in the range from 4.7 µF to 500 µF and with an ESR range from 0.001 Ω to 20 Ω. TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

7.2.2.3 Power-Good Threshold

The power-good threshold is set by connecting PGADJ to GND or to a resistor divider from OUT to GND. The *Adjustable Power-Good Threshold (PG, PGADJ)* section provides the method for setup of the power-good threshold.

7.2.2.4 Power-Good Delay Period

The power-good delay period is set by an external capacitor (C_{DELAY}) to ground, with a typical capacitor value from 100 pF to 100 nF. Calculate the correct capacitance for the application using 方程式 2.

7.2.2.5 Watchdog Setup

The *Integrated Watchdog* section discusses the watchdog type selection and watchdog window-period setup method.

7.2.3 Application Curves

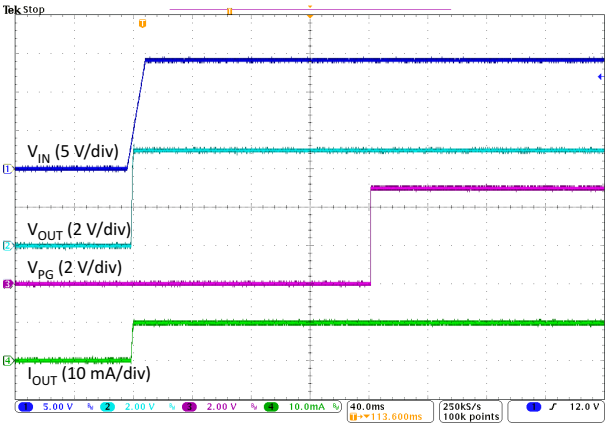


图 7-2. TPS7B6350-Q1 Power-Up Waveform

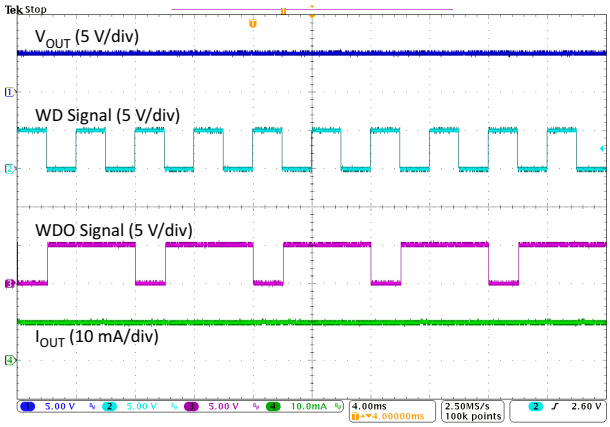


图 7-3. TPS7B6350-Q1 Watchdog Fault (High-Frequency Watchdog Service Signal)

7.3 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 4 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B63-Q1, TI recommends adding a capacitor with a value of ⩾10 µF with a 0.1 µF ceramic bypass capacitor in parallel at the input.

7.4 Layout

7.4.1 Layout Guidelines

For LDO power supplies, especially high-voltage and high-current ones, layout is an important step. If layout is not carefully designed, the regulator could not deliver enough output current because of thermal limitation. To improve the thermal performance of the device and maximize the current output at high ambient temperature, TI recommends spreading the thermal pad as much as possible and putting enough thermal vias on the thermal pad. 图 7-4 shows an example layout.

7.4.2 Layout Example

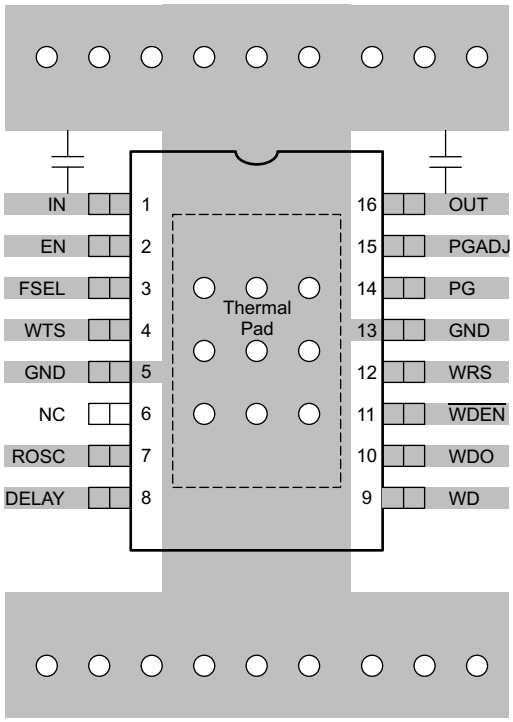


图 7-4. Layout Recommendation

8 器件和文档支持

8.1 文档支持

8.1.1 相关文档

请参阅以下相关文档：

德州仪器 (TI)，*TPS7B63xx-Q1 评估模块* 用户指南

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (December 2022) to Revision D (June 2025)	Page
• 向 *说明* 部分添加了 *封装信息* 表	1

Changes from Revision B (September 2020) to Revision C (December 2022)	Page
• Changed PADJ and WTS pins to inputs instead of outputs	4
• Changed *Load Regulation* graph and changed VIN condition for I_{OUT} = 200 mA *Line Transient* graphs	10
• Changed resistor values in *TPS7B63xx-Q1 Typical Application Schematic* figure	22

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B6333QPWPRQ1	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6333Q
TPS7B6333QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6333Q
TPS7B6350QPWPRQ1	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6350Q
TPS7B6350QPWPRQ1.A	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B6350Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

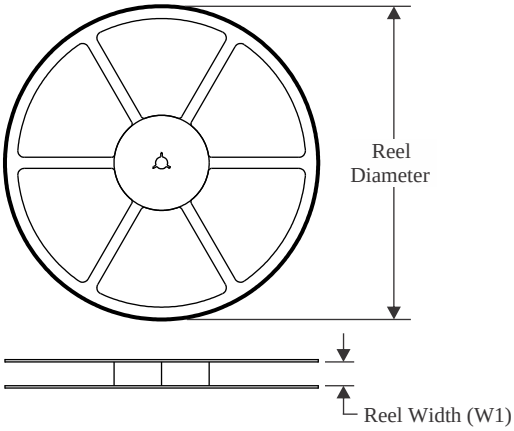
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

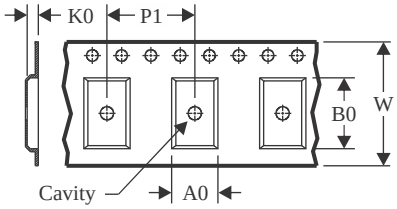
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

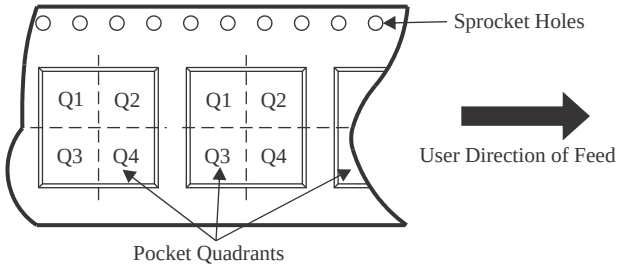


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

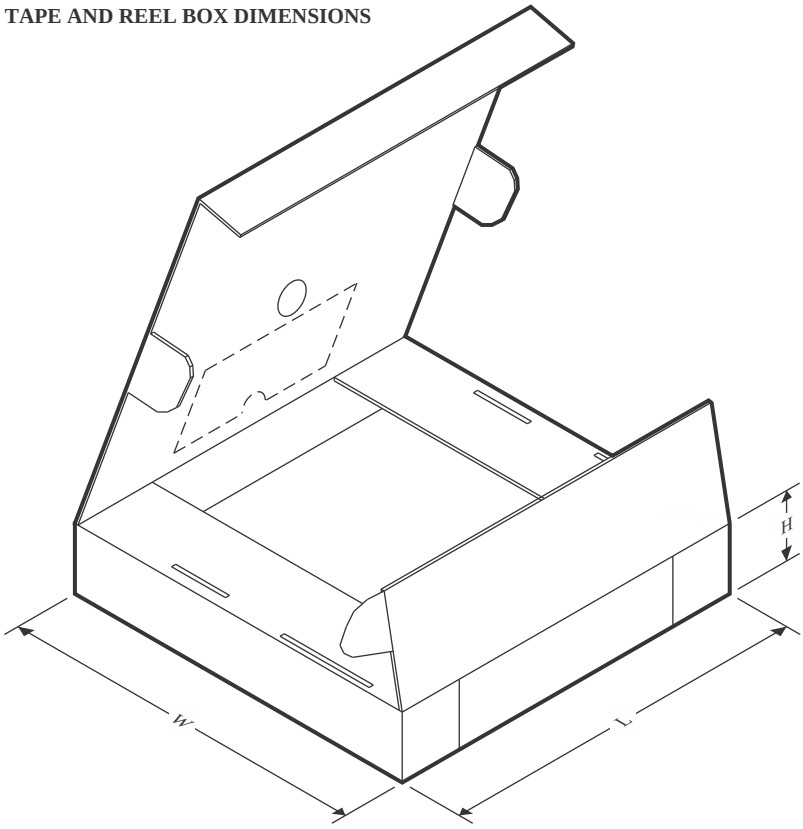
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B6333QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B6350QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

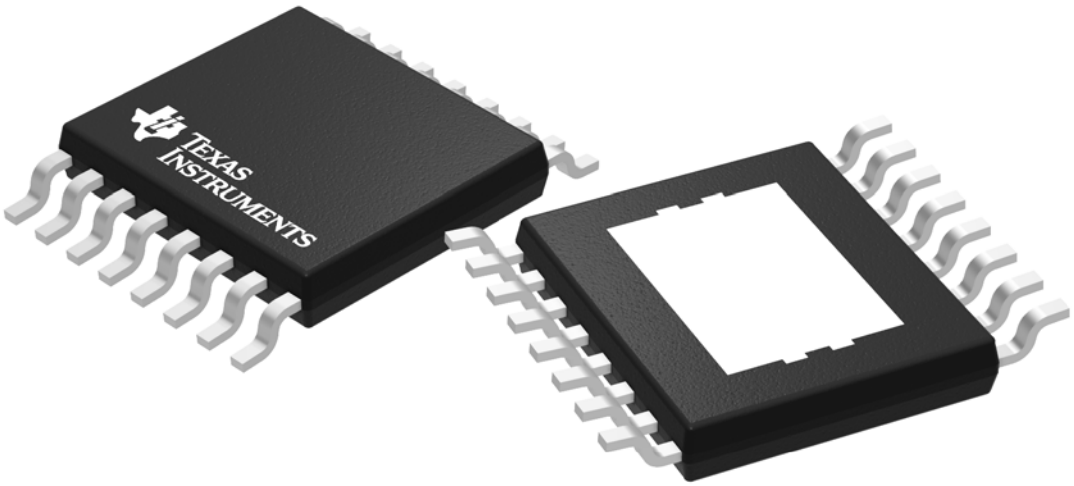


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B6333QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS7B6350QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

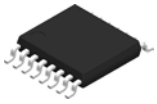
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

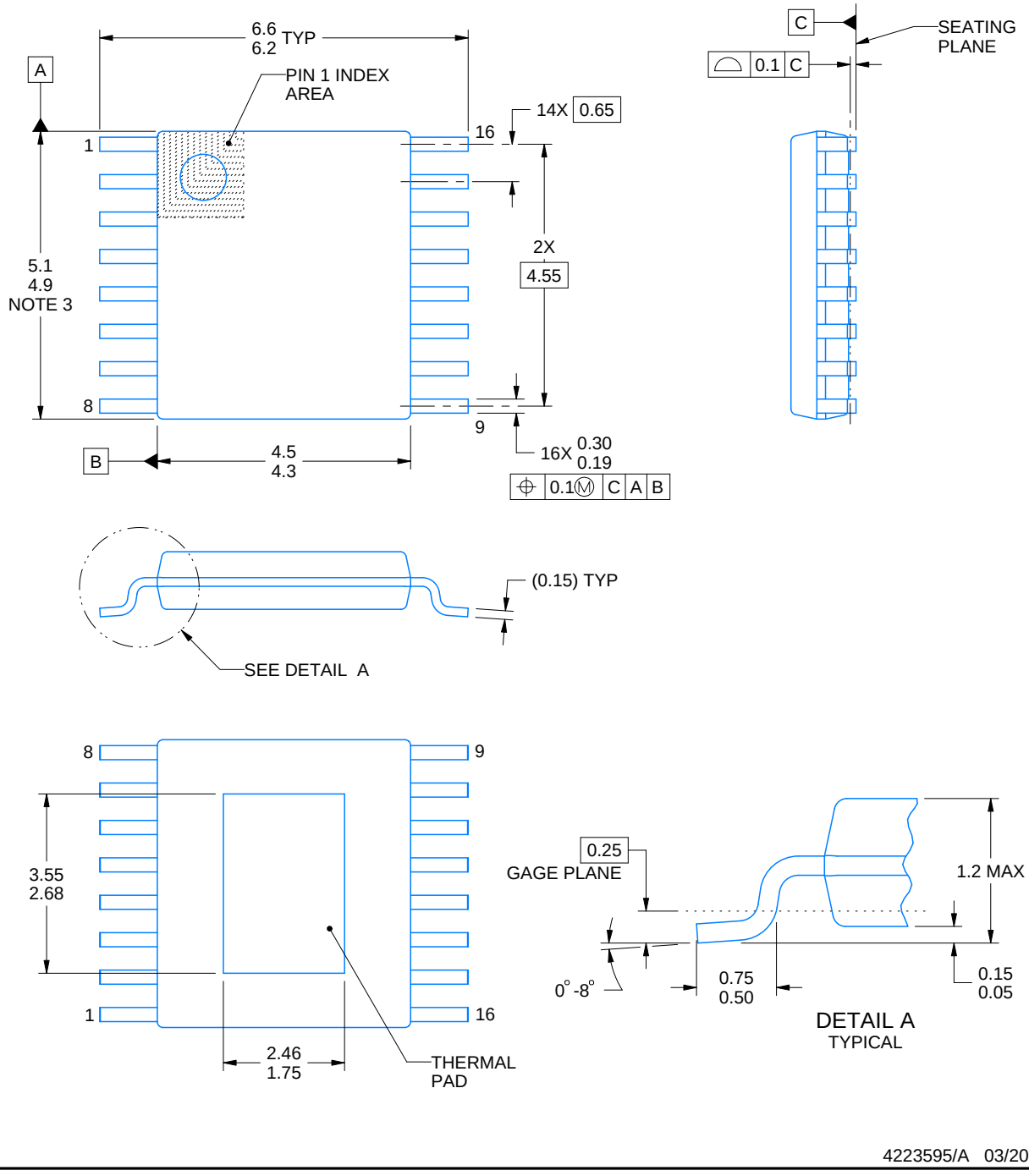
PACKAGE OUTLINE

PWP0016J



PowerPAD™ TSSOP - 1.2 mm max height

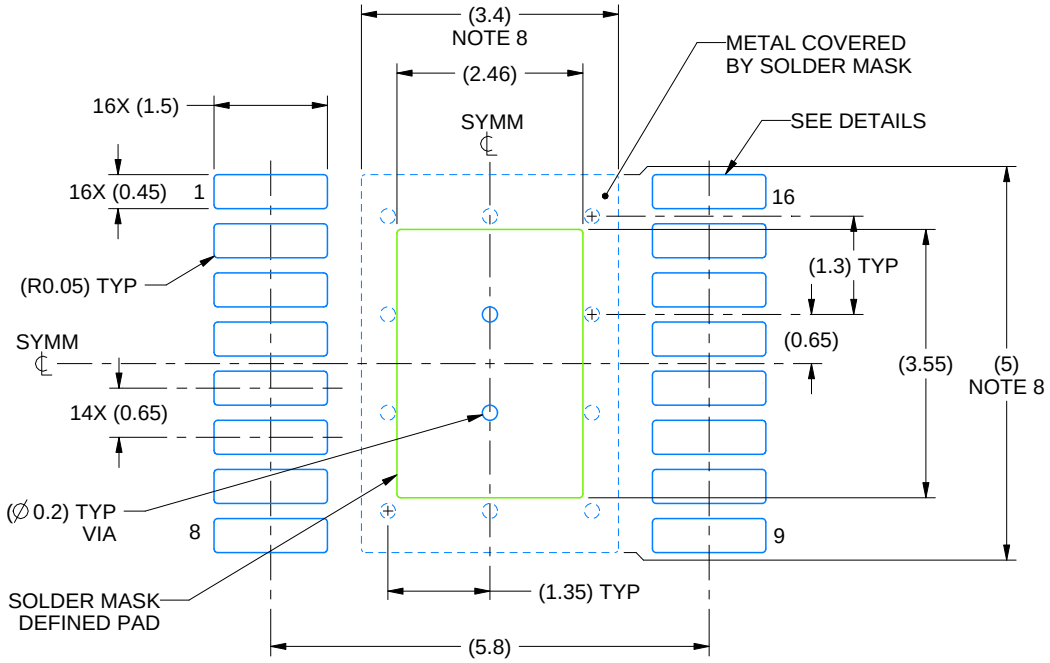
SMALL OUTLINE PACKAGE



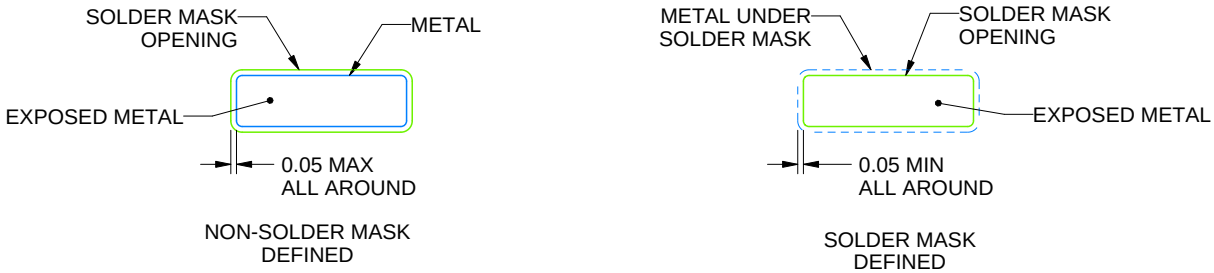
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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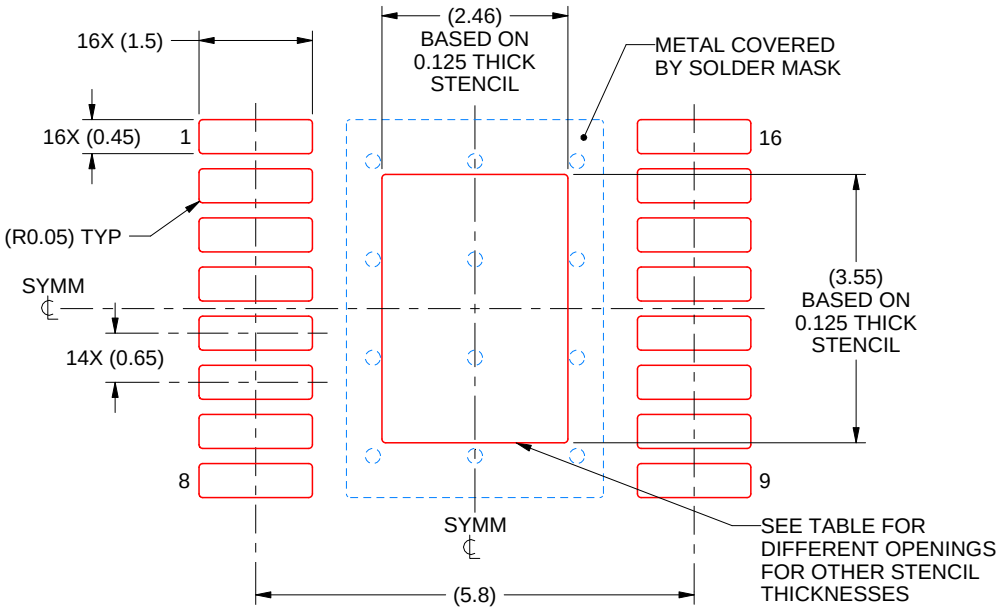
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月