

用于紧凑型摄像机模块 (CCM) 应用且具有 LED 闪存驱动器和参考时钟生成功能的 TPS68470 电源管理 单元

1 特性

- 高效降压转换器
 - 输出电流高达 500mA
 - 输出电压可选范围: 0.9V 至 1.95V
- 双闪存发光二极管 (LED) 驱动器
 - 高效升压转换器
 - 基于 LED 基准电压 (Vf) 的自适应输出电压调节
 - 低侧 LED 电流驱动器
 - 两个 1A 电流驱动器
 - LED 温度监视
 - 开路/短路 LED 检测/保护
 - 受控 LED 电流斜升/斜降
- 传感器模拟电源的线性稳压器
 - 输出电压可编程范围是 0.875V 到 3.1V (17.8mV 步长)
 - 输出电流高达 200mA
- IO 电源的线性稳压器
 - 输出电压可编程范围是 0.875V 到 3.1V (17.8mV 步长)
 - 输出电流高达 50mA
- VCM (音圈电机) 驱动器电源的线性稳压器
 - 输出电压可编程范围是 0.875V 到 3.1V (17.8mV 步长)
 - 输出电流高达 500mA
- 辅助电源的线性稳压器
 - 输出电压可编程范围是 0.875V 到 3.1V (17.8mV 步长)
 - 输出电流高达 150mA
- 辅助电源的线性稳压器
 - 输出电压可编程范围是 0.875V 到 3.1V (17.8mV 步长)
 - 输出电流高达 50mA
- 传感器 IO 电源的线性稳压器
 - 输出电压可编程范围是 0.875V 到 3.1V (17.8mV 步长)
 - 输出电流高达 150mA
- 时钟发生
 - 可编程锁相环 (PLL)
 - 晶振
- I²C 接口
- 7 个通用输入输出 (GPIO)
- 系统复位

- 工作温度范围: 0°C 至 85°C
- 封装厚度 0.625mm 的芯片级球状引脚栅格阵列 (DSBGA)

2 应用

- 可拆卸式超级本
- 平板电脑
- 智能手机
- 紧凑型摄像机模块 (CCM)

3 说明

TPS68470 器件是高级电源管理单元, 可为紧凑型摄像机模块 (CCM) 供电、为图像传感器生成时钟、驱动闪存的双 LED 并集成两个用于通用指示器的 LED 驱动器。TPS68470 能够生成 CCM 中所需的全部电源轨。

CORE 电压稳压器是目前最先进的降压转换器, 可用于图像传感器数字电源。线性稳压器 (LDO) (LDO_ANA) 可用于图像传感器模拟电源。

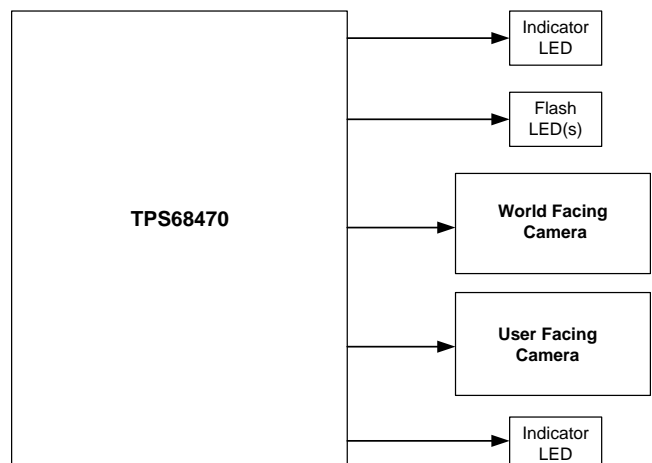
TPS68470 还具有一个高效的升压转换器, 可支持两个 1A LED 闪光灯驱动器。并且可通过低侧稳压电流源来控制 LED 电流。

器件信息⁽¹⁾

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|----------|------------|-------------------|
| TPS68470 | DSBGA (56) | 3.325mm x 2.930mm |

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

应用图



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4 修订历史记录

Changes from Revision A (March 2015) to Revision B Page

| | | |
|---|---|----|
| • | Changed LDO_AUX2 Max output current from 50 mA to 80 mA | 11 |
|---|---|----|

Changes from Original (September 2014) to Revision A Page

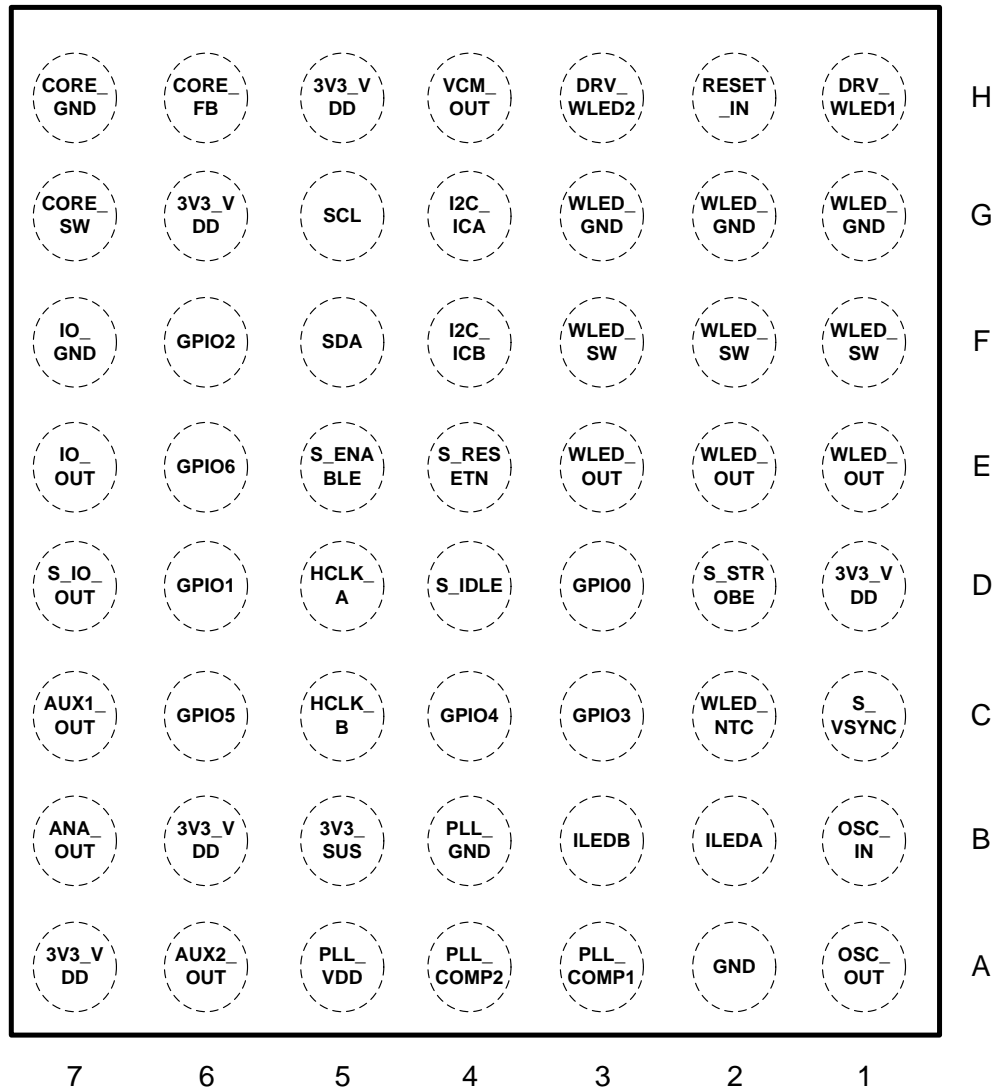
| | | |
|---|---|---|
| • | Added Storage temperature to Absolute Maximum Ratings | 5 |
| • | Changed Handling Ratings to ESD Ratings | 5 |
| • | Deleted Storage temperature from ESD Ratings | 5 |

5 说明（续）

TPS68470 还有五个 LDO。其中两个可用于通用电源电压生成及传感器 IO 电源电压生成（LDO_IO 和 LDO_S_IO）。其中一个可专门用于 VCM 驱动器电源（LDO_VCM）。其余两个是辅助 LDO（LDO_AUX1 和 LDO_AUX2）。

6 Pin Configuration and Functions

**56-Pin DSBGA
YFF Package
(Top View)**



Pin Functions

| PIN | | I/O | DESCRIPTION |
|---------|--------|-----|--|
| NAME | NUMBER | | |
| I2C_ICA | G4 | I | TPS68470 I ² C Address select pin A |
| I2C_ICB | F4 | I | TPS68470 I ² C Address select pin B |
| SDA | F5 | I/O | I ² C data |
| SCL | G5 | I | I ² C clk |
| GPIO0 | D3 | I/O | GPIO |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|-----------|--------------------|-----|--|
| NAME | NUMBER | | |
| GPIO1 | D6 | I/O | GPIO (sensor SDA in daisy chain mode) |
| GPIO2 | F6 | I/O | GPIO (sensor SCL in daisy chain mode) |
| GPIO3 | C3 | I/O | GPIO or External Reference Clock when XTAL is disabled |
| GPIO4 | C4 | I/O | GPIO |
| GPIO5 | C6 | I/O | GPIO |
| GPIO6 | E6 | I/O | GPIO |
| S_RESETN | E4 | O | Sensor reset |
| S_ENABLE | E5 | O | Sensor power enable / power down |
| S_IDLE | D4 | O | Sensor power down mode |
| S_VSYNC | C1 | I | Sensor activity indication enable |
| RESET_IN | H2 | I | Platform reset input (active low) |
| S_STROBE | D2 | I | White LED trigger input |
| OSC_IN | B1 | I | XTAL input |
| OSC_OUT | A1 | O | XTAL output |
| HCLK_A | D5 | O | Sensor Clock |
| HCLK_B | C5 | O | Alternate Sensor Clock |
| PLL_COMP1 | A3 | O | PLL compensation |
| PLL_COMP2 | A4 | O | SS PLL compensation |
| VCM_OUT | H4 | O | VCM LDO output |
| ANA_OUT | B7 | O | Analog LDO output |
| IO_OUT | E7 | O | IO LDO output |
| S_IO_OUT | D7 | O | Sensor IO LDO output |
| IO_GND | F7 | - | IO and digital GND |
| AUX1_OUT | C7 | O | Auxiliary LDO1 output |
| AUX2_OUT | A6 | O | Auxiliary LDO2 output |
| CORE_SW | G7 | O | Core Buck SW |
| CORE_FB | H6 | I | Core Buck feedback |
| CORE_GND | H7 | - | Core Buck GND |
| WLED_SW | F3, F2, F1 | O | White LED Boost SW |
| WLED_OUT | E3, E2, E1 | O | White LED Boost output, connect 2 x 10uF capacitors to this output |
| WLED_GND | G3, G2, G1 | - | White LED Boost GND |
| WLED_NTC | C2 | I | White LED Temperature sensor feedback |
| DRV_WLED1 | H1 | I | White LED 1 current sink (the source of current is from WLED_OUT) |
| DRV_WLED2 | H3 | I | White LED 2 current sink (the source of current is from WLED_OUT) |
| ILED A | B2 | O | Indicator LED A driver |
| ILED B | B3 | O | Indicator LED B driver |
| PLL_VDD | A5 | O | PLL internal regulator (connect a 1μF capacitor to this pin) |
| PLL_GND | B4 | - | PLL GND |
| 3V3_VDD | H5, G6, D1, B6, A7 | I | 3.3V input * H5 - LDO_VCM * G6 - CORE Buck Converter * D1 - WLED Boost Converter * B6 - LDO_PLL * A7 - LDO_AUX1, LDO_ANA, LDO_IO, LDO_SIO |
| 3V3_SUS | B5 | I | 3.3V Auxiliary sustaining rail input (LDO_AUX2) |
| GND | A2 | - | Ground |

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

| | | MIN | MAX | UNIT |
|--|--|------|------|------|
| Voltage | 3V3_VDD, 3V3_SUS | –0.3 | 3.96 | V |
| | DRV_WLED1, DRV_WLED2 | –0.3 | 7.0 | |
| | WLED_SW, WLED_OUT | –0.3 | 7.0 | |
| | CORE_SW | –0.3 | 7.0 | |
| | I2C_ICA, I2C_ICB, SDA, SCL | –0.3 | 3.96 | |
| | GPIO0-6 | –0.3 | 3.96 | |
| | S_RESETN, S_ENABLE, S_IDLE, S_VSYNC, S_STROBE | –0.3 | 3.96 | |
| | RESET_IN | –0.3 | 3.96 | |
| | OSC_IN, OSC_OUT | –0.3 | 3.96 | |
| | HCLK_A, HCLK_B | –0.3 | 3.96 | |
| | PLL_COMP1, PLL_COMP2 | –0.3 | 3.96 | |
| | VCM_OUT, ANA_OUT, IO_OUT, S_IO_OUT, AUX1_OUT, AUX2_OUT | –0.3 | 3.96 | |
| | CORE_FB | –0.3 | 3.96 | |
| | WLED_NTC | –0.3 | 3.96 | |
| | ILED _A , ILED _B | –0.3 | 3.96 | |
| | PLL_VDD | –0.3 | 3.96 | |
| Continuous power dissipation, P _D | | | 1.6 | W |
| Operating junction temperature, T _J | | –30 | 125 | °C |
| Storage temperature, T _{stg} | | –65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.

7.2 ESD Ratings

| | | VALUE | UNIT |
|---|--|-------|------|
| V _(ESD) ⁽¹⁾ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽²⁾ | 2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽³⁾ | 500 | |

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|--|------|-----|--------------------|------|
| Voltage | 3V3_VDD, 3V3_SUS | 2.97 | 3.3 | 3.63 | V |
| | DRV_WLED1, DRV_WLED2 | | | Setting Depend ent | |
| | WLED_SW, WLED_OUT | | | Setting Depend ent | |
| | CORE_SW | | | Setting Depend ent | |
| | I2C_ICA, I2C_ICB | | | 3.3 | |
| | SDA, SCL | 1.8 | | 3.3 | |
| | GPIO0-6 | | | 3.3 | |
| | S_RESETN, S_ENABLE, S_IDLE, S_VSYNC, S_STROBE | | | 3.3 | |
| | RESET_IN | | | 3.3 | |
| | OSC_IN, OSC_OUT | | | 3.3 | |
| | HCLK_A, HCLK_B | | | 3.3 | |
| | PLL_COMP1, PLL_COMP2 | | | 3.3 | |
| | VCM_OUT, ANA_OUT, IO_OUT, S_IO_OUT, AUX1_OUT, AUX2_OUT | | | 3.1 | |
| | CORE_FB | | | 1.95 | |
| | WLED_NTC | | | 3.3 | |
| | ILED_A, ILED_B | | | 3.3 | |
| | PLL_VDD | | | 3.3 | |
| Operating ambient temperature, T _A | | 0 | | 85 | °C |

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | YFF (DSBGA) 56 PINS | UNIT |
|-------------------------------|--|------------------------|------|
| R _{θJA} | Junction-to-ambient thermal resistance | 39.8 | °C/W |
| R _{θJctop} | Junction-to-case (top) thermal resistance | 0.2 | |
| R _{θJB} | Junction-to-board thermal resistance | 6.6 | |
| ψ _{JT} | Junction-to-top characterization parameter | 0.5 | |
| ψ _{JB} | Junction-to-board characterization parameter | 6.5 | |
| R _{θJcbot} | Junction-to-case (bottom) thermal resistance | n/a | |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.5 Electrical Characteristics

Over recommended free-air temperature and over recommended input voltage (typical at an ambient temperature range of 27°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|--|--|------|-------|------|------|
| SUPPLY VOLTAGE and UVLO | | | | | | |
| $V_{I(3V3_VDD)}$ | Operating input voltage | | 2.97 | 3.3 | 3.63 | V |
| $V_{I(3V3_SUS)}$ | Operating input voltage | | 2.97 | 3.3 | 3.63 | V |
| $I_{Q(3V3_VDD)}$ | 3V3_VDD quiescent current | In ACTIVE mode, $V_{I(3V3_VDD)} = V_{I(3V3_SUS)} = 3.3$ V, LDO_IO enabled and with no load, LDO_PLL, LDO_ANA, LDO_S_IO, LDO_AUX1, LDO_VCM, CORE and WLED_OUT disabled and with no load LDO_AUX2 disabled and with no load | 65 | 100 | 145 | μA |
| | | In ACTIVE mode, $V_{I(3V3_VDD)} = V_{I(3V3_SUS)} = 3.3$ V, LDO_IO enabled and with no load, LDO_PLL, LDO_ANA, LDO_S_IO, LDO_AUX1, LDO_VCM, CORE and WLED_OUT disabled and with no load LDO_AUX2 enabled and with no load - LDO_AUX2 current comes from 3V3_SUS | 65 | 100 | 145 | μA |
| | | In ACTIVE mode, $V_{I(3V3_VDD)} = V_{I(3V3_SUS)} = 3.3$ V, LDO_ANA, LDO_IO, LDO_S_IO, LDO_AUX1, LDO_VCM, CORE and WLED_OUT enabled (default voltage settings) and with no load, LDO_PLL disabled, CORE and WLED_OUT running on internal oscillator LDO_AUX2 disabled and with no load | | 5 | | mA |
| | | In ACTIVE mode, $V_{I(3V3_VDD)} = V_{I(3V3_SUS)} = 3.3$ V, LDO_IO enabled and with no load, LDO_PLL enabled, BUCKDIV [3:0] set to 5.2 MHz, BOOSTDIV [4:0] set to 2 MHz, POSTDIV for HCLK_A and HCLK_B set to 18 MHz LDO_ANA, LDO_S_IO, LDO_AUX1, LDO_VCM, CORE and WLED_OUT disabled and with no load LDO_AUX2 disabled and with no load | | 0.91 | | mA |
| $I_{Q(3V3_SUS)}$ | 3V3_SUS quiescent current | In ACTIVE mode, $V_{I(3V3_VDD)} = V_{I(3V3_SUS)} = 3.3$ V, LDO_AUX2 disabled and with no load | 25 | 35 | 50 | μA |
| | | In ACTIVE mode, $V_{I(3V3_VDD)} = V_{I(3V3_SUS)} = 3.3$ V, LDO_AUX2 enabled and with no load | 70 | 102 | 130 | μA |
| | | In ACTIVE mode, $V_{I(3V3_VDD)} = V_{I(3V3_SUS)} = 3.3$ V, LDO_ANA, LDO_IO, LDO_S_IO, LDO_AUX1, LDO_VCM, CORE and WLED_OUT enabled (default voltage settings) and with no load, LDO_PLL disabled, CORE and WLED_OUT running on internal oscillator LDO_AUX2 disabled and with no load | | 255 | | μA |
| | | In ACTIVE mode, $V_{I(3V3_VDD)} = V_{I(3V3_SUS)} = 3.3$ V, LDO_IO enabled and with no load, LDO_PLL enabled, BUCKDIV [3:0] set to 5.2 MHz, BOOSTDIV [4:0] set to 2 MHz, POSTDIV for HCLK_A and HCLK_B set to 18 MHz LDO_ANA, LDO_S_IO, LDO_AUX1, LDO_VCM, CORE and WLED_OUT disabled and with no load LDO_AUX2 disabled and with no load | | 1.367 | | mA |
| | | In SLEEP mode, $V_{I(3V3_VDD)} = 0$ V, $V_{I(3V3_SUS)} = 3.3$ V, LDO_AUX2 disabled and with no load | | 0.3 | 1.1 | μA |
| | | In SLEEP mode, $V_{I(3V3_VDD)} = 0$ V, $V_{I(3V3_SUS)} = 3.3$ V, LDO_AUX2 enabled and with no load | 75 | 100 | 125 | μA |
| $UVLO_{3V3_VDD}$ | Under voltage lockout threshold at 3V3_VDD pin | $V_{I(3V3_VDD)}$ going up | 2.6 | 2.75 | 2.85 | V |
| | | $V_{I(3V3_VDD)}$ going down | 2.55 | 2.65 | 2.75 | |
| | | Hysteresis | | 0.1 | | |

Electrical Characteristics (continued)

Over recommended free-air temperature and over recommended input voltage (typical at an ambient temperature range of 27°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---|--|-------|------|------|------|
| UVLO _{3V3_SUS} | Under voltage lockout threshold at 3V3_SUS pin | V _{I(3V3_SUS)} going up | 2.6 | 2.75 | 2.85 | V |
| | | V _{I(3V3_SUS)} going down | 2.55 | 2.65 | 2.75 | |
| | | Hysteresis | 0.1 | | | |
| BOOST CONVERTER (WLED_OUT) | | | | | | |
| VI(3V3_VDD) | Input Voltage | | 2.97 | 3.3 | 3.63 | V |
| V _{O(WLED_OUT)} | Output voltage range | Current regulation mode | VIN | | 5.5 | V |
| | | Voltage regulation mode | 3.68 | | 5.48 | V |
| | Internal feedback voltage accuracy | Boost mode, PWM voltage regulation | −2% | | 2% | |
| V _{OVP} | Output overvoltage protection | V _{O(WLED_OUT)} rising | 5.7 | 6.0 | 6.25 | V |
| | Output overvoltage protection hysteresis | V _{O(WLED_OUT)} falling | 100 | | | mV |
| t _{start} | Start-up time | | 1 | | | ms |
| D _{WLED_SW} | Minimum duty cycle | | 7.5% | | | |
| R _{DS(ON)} | Switch MOSFET on-resistance | V _{O(WLED_OUT)} = V _{gs} = 3.6 V | 40 | | | mΩ |
| | Rectifier MOSFET on-resistance | | 40 | | | mΩ |
| I _{LK(WLED_SW)} | Switch MOSFET leakage | V _{WLED_SW} = 3.6 V, T _A = 85°C | 0.22 | | 1.2 | μA |
| I _{LIM} | Switch current limit | ILIM[3:0] = '1010' | 4.0 | | | A |
| | | Selectable range ⁽¹⁾ | 2.0 | | 5.0 | |
| C _{IN} | External Input capacitor | | 4.7 | | | μF |
| C _{LC} | External LC capacitance | | 10 | 20 | 26 | μF |
| L _{LC} | External LC inductance | | 1.3 | 2.2 | 2.9 | μH |
| LED DRIVER | | | | | | |
| I _{DRV_WLEDx} | Maximum operating current per driver | Driver on | | | 1 | A |
| | DRV_WLEDx current accuracy | 0.4 V ≤ V _{DRV_WLEDx} ≤ 2.0 V, 0 mA ≤ I _{DRV_WLEDx} ≤ 300 mA | −10% | | 10% | |
| | | 0.4 V ≤ V _{DRV_WLEDx} ≤ 2.0 V, 300 mA ≤ I _{DRV_WLEDx} ≤ 1000 mA | −7.5% | | 7.5% | |
| | DRV_WLED1 and DRV_WLED2 current matching | | −10% | | 10% | |
| I _{ILEDx} | Indicator LEDx driver maximum operating current | | | | 16 | mA |
| | ILEDx current accuracy | V _{ILEDx} = 1.0 V at I _{ILEDx} = 16 mA | −10% | | 10% | |
| V _{SENSE(DRV_WLEDx)} | DRV_WLEDx sense voltage | I _{DRV_WLEDx} = full-scale current | 400 | | | mV |
| I _{ILK(DRV_WLEDx)} | DRV_WLEDx input leakage current | V _{DRV_WLEDx} = 3.6 V, T _A = 85°C | | | 5 | μA |
| I _{ILK(ILEDx)} | ILEDx input leakage current | V _{ILEDx} = 0 V, T _A = 85°C | | | 1 | μA |
| LED TEMPERATURE MONITORING | | | | | | |
| I _{O(WLED_NTC)} | Temperature sense current source | Thermistor bias current | 23.8 | | | μA |
| | TS resistance (warning temperature) | LEDWARN bit = 1 | 0.92 | 1.05 | 1.19 | V |
| | TS resistance (hot temperature) | LEDHOT bit = 1 | 0.29 | 0.35 | 0.4 | V |

(1) Boost current limit is selectable from register VWLEDILIM with 4-bits

Electrical Characteristics (continued)

Over recommended free-air temperature and over recommended input voltage (typical at an ambient temperature range of 27°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|--|---|-------|------|------|------|
| BUCK CONVERTER (CORE) | | | | | | |
| $V_{I(3V3_VDD)}$ | Input voltage | | 2.97 | 3.3 | 3.63 | V |
| $V_{O(CORE)}$ | Regulated DC output voltage | $0\text{ mA} \leq I_O \leq 500\text{ mA}$, DVOLT[5:0] = 0x0D | 1.15 | 1.2 | 1.25 | V |
| | Output voltage range | Range selectable with 25-mV steps | 0.9 | 1.2 | 1.95 | V |
| $R_{DS(ON)}$ | High-Side MOSFET on resistance | $V_{I(3V3_VDD)} = V_{(GS)} = 3.3\text{ V}$, 100% Duty Cycle | | 180 | | mΩ |
| | Low-Side MOSFET on resistance | $V_{I(3V3_VDD)} = V_{(GS)} = 3.3\text{ V}$, 0% Duty Cycle | | 150 | | mΩ |
| V_{SHORT} | Output short detection comparator | $V_{O(CORE)} < V_{SHORT}$ for greater than 10 ms | | 0.5 | | V |
| R_{DIS} | Discharge resistor for power down sequence | Core Disabled | | 190 | 375 | Ω |
| $I_{O(CORE)}$ | Output operating current | | | | 500 | mA |
| | P-MOS current limit | | | 1000 | | mA |
| f_{SW} | Clock frequency range | | 3 | 5.2 | 6 | MHz |
| R_{FB} | Feedback input resistance | | | 500 | | kΩ |
| t_{Ramp} | $V_{O(CORE)}$ ramp up time | Time to ramp from 5% to 95% of V_{OUT} ($V_{O(CORE)} = 1.2\text{ V}$) ,no load, typical C_{OUT} | | 85 | 200 | μs |
| C_{IN} | External input capacitor | | | 4.7 | | μF |
| C_{LC} | External LC capacitance | | 2.35 | 4.7 | 6.11 | μF |
| L_{LC} | External LC inductance | | 0.5 | 1.0 | 1.3 | μH |
| LDO_ANA | | | | | | |
| $V_{I(3V3_VDD)}$ | Input voltage | | | 3.3 | | V |
| $V_{O(ANA_OUT)}$ | Output voltage | See ⁽²⁾ | 0.875 | 2.8 | 3.1 | V |
| | Output DC accuracy | $V_{I(3V3_VDD)} - V_{O(ANA_OUT)} > 200\text{ mV}$ | -2% | | 2% | |
| | Dropout voltage | $V_{3V3_VDD} = 0.975 \times V_{OUT(NOM)}$, $I_{OUT} = 200\text{ mA}$ | | 100 | 150 | mV |
| | Load regulation | $0\text{ mA} \leq I_{out} \leq 200\text{ mA}$ | | | 15 | mV |
| | Line regulation | $V_{OUT(NOM)} + 0.3\text{ V} \leq V_{3V3_VDD} \leq 3.63\text{ V}$, $I_{OUT} = 10\text{ mA}$ | | | 5 | mV |
| I_{max} | Max output current | | | | 200 | mA |
| PSRR | Power supply rejection ratio | $f = 1\text{ kHz}$, $V_I = 3.3\text{ V}$, $V_O = 2.8\text{ V}$, $I_{OUT} = 0.75 \times 200\text{ mA}$ | 50 | 56 | | dB |
| | | $f = 10\text{ kHz}$, $V_I = 3.3\text{ V}$, $V_O = 2.8\text{ V}$, $I_{OUT} = 0.75 \times 200\text{ mA}$ | 30 | 38 | | |
| V_{SHORT} | Output short detection comparator | $V_{O(ANA_OUT)} < V_{SHORT}$ for greater than 10ms | | 0.5 | | V |
| T_{start} | Startup time | $C_{OUT} = 1.0\text{ μF}$, $V_{O(ANA_OUT)}$ from 0 V to 2.8 V | | 100 | | μs |
| R_{DIS} | Discharge resistor in power down | | | 100 | 200 | Ω |
| C_{OUT} | Output capacitance | | 0.5 | 1.0 | 1.3 | μF |

(2) All LDO output voltages are selectable through a specific voltage adjustment register xVAL bits xVOLT[6:0] and can be adjusted from 0.875 V up to 3.1 V with steps of 17.8 mV. Output voltage register setting xVOLT[6:0] values (dec) can be calculated with the below formula:

$$xVOLT(DEC) = \text{round}[(V_{out} - 0.875\text{ V})/0.0178\text{ V}]$$

Electrical Characteristics (continued)

Over recommended free-air temperature and over recommended input voltage (typical at an ambient temperature range of 27°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------------|---|-------|-----|-----|---------------|
| LDO_VCM | | | | | | |
| $V_{I(3V3_VDD)}$ | Input Voltage | | | 3.3 | | V |
| $V_{O(VCM_OUT)}$ | Output voltage | See ⁽²⁾ | 0.875 | 2.8 | 3.1 | V |
| | Output DC accuracy | $V_{I(3V3_VDD)} - V_{O(VCM_OUT)} > 200 \text{ mV}$ | -2% | | 2% | |
| | Dropout voltage | $V_{3V3_VDD} = 0.975 \times V_{OUT(NOM)}$, $I_{OUT} = 500 \text{ mA}$ | | 100 | 150 | mV |
| | Load regulation | $0 \text{ mA} \leq I_{out} \leq 500 \text{ mA}$ | | | 15 | mV |
| | Line regulation | $V_{OUT(NOM)} + 0.3 \text{ V} \leq V_{3V3_VDD} \leq 3.63 \text{ V}$, $I_{OUT} = 10 \text{ mA}$ | | | 5 | mV |
| I_{max} | Max output current | | | | 500 | mA |
| PSRR | Power supply rejection ratio | $f = 1 \text{ kHz}$, $V_I = 3.3 \text{ V}$, $V_O = 2.8 \text{ V}$, $I_{OUT} = 0.75 \times 500 \text{ mA}$ | 50 | 60 | | dB |
| | | $f = 10 \text{ kHz}$, $V_I = 3.3 \text{ V}$, $V_O = 2.8 \text{ V}$, $I_{OUT} = 0.75 \times 500 \text{ mA}$ | 30 | 40 | | |
| V_{SHORT} | Output short detection comparator | $V_{O(VCM_OUT)} < V_{SHORT}$ for greater than 10ms | | 0.5 | | V |
| T_{start} | Startup time | $C_{OUT} = 1.0 \mu\text{F}$, V_{out} from 0 V to 2.8 V | | 100 | | μs |
| R_{DIS} | Discharge resistor in power down | | | 100 | 200 | Ω |
| C_{OUT} | Output capacitance | | 0.5 | 1.0 | 1.3 | μF |
| LDO_AUX1 | | | | | | |
| $V_{I(3V3_VDD)}$ | Input voltage | | | 3.3 | | V |
| $V_{O(AUX1_OUT)}$ | Output voltage | See ⁽²⁾ | 0.875 | 1.2 | 3.1 | V |
| | Output accuracy | $V_{I(3V3_VDD)} - V_{O(AUX1_OUT)} > 200 \text{ mV}$ | -2% | | 2% | |
| | Dropout voltage | $V_{3V3_VDD} = 0.975 \times V_{OUT(NOM)}$, $I_{OUT} = 150 \text{ mA}$ | | 100 | 150 | mV |
| | Load regulation | $0 \text{ mA} \leq I_{out} \leq 150 \text{ mA}$ | | | 15 | mV |
| | Line regulation | $V_{OUT(NOM)} + 0.3 \text{ V} \leq V_{3V3_VDD} \leq 3.63 \text{ V}$, $I_{OUT} = 10 \text{ mA}$ | | | 5 | mV |
| I_{max} | Max output current | | | | 150 | mA |
| PSRR | Power supply rejection ratio | $f = 1 \text{ kHz}$, $V_I = 3.3 \text{ V}$, $V_O = 1.2 \text{ V}$, $I_{OUT} = 0.75 \times 150 \text{ mA}$ | 50 | 56 | | dB |
| | | $f = 10 \text{ kHz}$, $V_I = 3.3 \text{ V}$, $V_O = 1.2 \text{ V}$, $I_{OUT} = 0.75 \times 150 \text{ mA}$ | 30 | 38 | | |
| V_{SHORT} | Output short detection comparator | $V_{O(AUX1_OUT)} < V_{SHORT}$ for greater than 10 ms | | 0.5 | | V |
| T_{start} | Startup time | $C_{OUT} = 1.0 \mu\text{F}$, V_{out} from 0 V to 1.2 V | | 100 | | μs |
| R_{DIS} | Discharge resistor in power down | | | 100 | 200 | Ω |
| C_{OUT} | Output capacitance | | 0.5 | 1.0 | 1.3 | μF |

Electrical Characteristics (continued)

Over recommended free-air temperature and over recommended input voltage (typical at an ambient temperature range of 27°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|-----------------------------------|--|-------|-----|-----|---------------|
| LDO_AUX2 | | | | | | |
| $V_{I(3V3_SUS)}$ | Input voltage | | | 3.3 | | V |
| $V_{O(AUX2_OUT)}$ | Output voltage | See (2) | 0.875 | 1.8 | 3.1 | V |
| | Output accuracy | $V_{I(3V3_SUS)} - V_{O(AUX2_OUT)} > 200 \text{ mV}$ | -2% | | 2% | |
| | Dropout voltage | $V_{3V3_SUS} = 0.975 \times V_{OUT(NOM)}$, $I_{OUT} = 50 \text{ mA}$ | | 100 | 150 | mV |
| | Load regulation | $0 \text{ mA} \leq I_{OUT} \leq 50 \text{ mA}$ | | | 15 | mV |
| | Line regulation | $V_{OUT(NOM)} + 0.3 \text{ V} \leq V_{3V3_VDD} \leq 3.63 \text{ V}$, $I_{OUT} = 10 \text{ mA}$ | | | 5 | mV |
| I_{max} | Max output current | | | | 80 | mA |
| PSRR | Power supply rejection ratio | $f = 1 \text{ kHz}$, $V_I = 3.3 \text{ V}$, $V_O = 1.8 \text{ V}$, $I_{OUT} = 0.75 \times 50 \text{ mA}$ | 50 | 53 | | dB |
| | | $f = 10 \text{ kHz}$, $V_I = 3.3 \text{ V}$, $V_O = 1.8 \text{ V}$, $I_{OUT} = 0.75 \times 50 \text{ mA}$ | 30 | 38 | | dB |
| V_{SHORT} | Output short detection comparator | $V_{O(AUX2_OUT)} < V_{SHORT}$ for greater than 10 ms | | 0.5 | | V |
| T_{start} | Startup time | $C_{OUT} = 1.0 \mu\text{F}$, V_{out} from 0 V to 1.8 V | | 100 | | μs |
| R_{DIS} | Discharge resistor in power down | | | 100 | 200 | Ω |
| C_{OUT} | Output capacitance | | 0.5 | 1.0 | 1.3 | μF |
| LDO_IO | | | | | | |
| $V_{I(3V3_VDD)}$ | Input voltage | | | 3.3 | | V |
| $V_{O(IO_OUT)}$ | Output voltage | See (2) and (3) | 1.6 | 1.8 | 3.1 | V |
| | Output DC accuracy | $V_{I(3V3_VDD)} - V_{O(IO_OUT)} > 200 \text{ mV}$ | -2% | | 2% | |
| | Dropout voltage | $V_{3V3_VDD} = 0.975 \times V_{OUT(NOM)}$, $I_{OUT} = 50 \text{ mA}$ | | 100 | 150 | mV |
| | Load regulation | $0 \text{ mA} \leq I_{out} \leq 50 \text{ mA}$ | | | 15 | mV |
| | Line regulation | $V_{OUT(NOM)} + 0.3 \text{ V} \leq V_{3V3_VDD} \leq 3.63 \text{ V}$, $I_{OUT} = 10 \text{ mA}$ | | | 5 | mV |
| I_{max} | Max output current | | | | 50 | mA |
| PSRR | Power supply rejection ratio | $f = 1 \text{ kHz}$, $V_I = 3.3 \text{ V}$, $V_O = 1.8 \text{ V}$, $I_{OUT} = 0.75 \times 50 \text{ mA}$ | 50 | 56 | | dB |
| | | $f = 10 \text{ kHz}$, $V_I = 3.3 \text{ V}$, $V_O = 1.8 \text{ V}$, $I_{OUT} = 0.75 \times 50 \text{ mA}$ | 30 | 38 | | dB |
| V_{SHORT} | Output short detection comparator | $V_{O(IO_OUT)} < V_{SHORT}$ for greater than 10 ms | | 0.5 | | V |
| T_{start} | Startup time | $C_{OUT} = 1.0 \mu\text{F}$, V_{out} from 0 V to 1.8 V | | 100 | | μs |
| R_{DIS} | Discharge resistor in power down | | | 100 | 200 | Ω |
| C_{OUT} | Output capacitance | | 0.5 | 1.0 | 1.3 | μF |

(3) LDO_IO should never be set below 1.6 V, otherwise I²C communication is not functional.

Electrical Characteristics (continued)

Over recommended free-air temperature and over recommended input voltage (typical at an ambient temperature range of 27°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------------------------|---|-------|-----|------|---------------|
| LDO_S_IO | | | | | | |
| $V_{I(3V3_VDD)}$ | Input Voltage | | | 3.3 | | V |
| $V_{O(S_IO_OUT)}$ | Output voltage | See ⁽²⁾ | 0.875 | 1.8 | 3.1 | V |
| | Output DC accuracy | $V_{I(3V3_VDD)} - V_{O(S_IO_OUT)} > 200\text{ mV}$ | -2% | | 2% | |
| | Dropout voltage | $V_{3V3_VDD} = 0.975 \times V_{OUT(NOM)}$, $I_{OUT} = 150\text{ mA}$ | | 100 | 150 | mV |
| | Load regulation | $0\text{ mA} \leq I_{OUT} \leq 150\text{ mA}$ | | | 15 | mV |
| | Line regulation | $V_{OUT(NOM)} + 0.3\text{ V} \leq V_{3V3_VDD} \leq 3.63\text{ V}$, $I_{OUT} = 10\text{ mA}$ | | | 5 | mV |
| I_{max} | Max output current | | | | 150 | mA |
| PSRR | Power supply rejection ratio | $f = 1\text{ kHz}$, $V_I = 3.3\text{ V}$, $V_O = 1.8\text{ V}$, $I_{OUT} = 0.75 \times 150\text{ mA}$ | 50 | 53 | | dB |
| | | $f = 10\text{ kHz}$, $V_I = 3.3\text{ V}$, $V_O = 1.8\text{ V}$, $I_{OUT} = 0.75 \times 150\text{ mA}$ | 30 | 38 | | dB |
| V_{SHORT} | Output short detection comparator | $V_{O(S_IO_OUT)} < V_{SHORT}$ for greater than 10 ms | | 0.5 | | V |
| T_{start} | Startup time | $C_{OUT} = 1.0\text{ }\mu\text{F}$, V_{out} from 0 V to 1.8 V | | 100 | | ms |
| R_{DIS} | Discharge resistor in power down | | | 100 | 200 | Ω |
| C_{OUT} | Output capacitance | | 0.5 | 1.0 | 1.3 | μF |
| LDO_PLL (For Internal Use Only) | | | | | | |
| $V_{I(3V3_VDD)}$ | Input voltage | | | 3.3 | | V |
| $V_{O(PLL_VDD)}$ | Output voltage | See ⁽²⁾ | 2.55 | 2.7 | 2.75 | V |
| | Output DC accuracy | $V_{I(3V3_VDD)} - V_{O(PLL_VDD)} > 200\text{ mV}$ | -2% | | 2% | |
| | Dropout voltage | $V_{3V3_VDD} = 0.975 \times V_{OUT(NOM)}$, $I_{OUT} = 50\text{ mA}$ | | 150 | 200 | mV |
| | Load regulation | $0\text{ mA} \leq I_{OUT} \leq 50\text{ mA}$ | | | 15 | mV |
| | Line regulation | $V_{OUT(NOM)} + 0.3\text{ V} \leq V_{3V3_VDD} \leq 3.63\text{ V}$, $I_{OUT} = 10\text{ mA}$ | | | 5 | mV |
| I_{max} | Max output current | | | | 50 | mA |
| PSRR | Power supply rejection ratio | $f = 1\text{ kHz}$, $V_I = 3.3\text{ V}$, $V_O = 2.7\text{ V}$, $I_{OUT} = 0.75 \times 50\text{ mA}$ | 50 | 57 | | dB |
| | | $f = 10\text{ kHz}$, $V_I = 3.3\text{ V}$, $V_O = 2.7\text{ V}$, $I_{OUT} = 0.75 \times 50\text{ mA}$ | 30 | 40 | | dB |
| V_{SHORT} | Output short detection comparator | $V_{O(PLL_VDD)} < V_{SHORT}$ for greater than 10 ms | | 0.5 | | V |
| T_{start} | Startup time | $C_{OUT} = 1.0\text{ }\mu\text{F}$, V_{out} from 0 V to 2.7 V | | 100 | | μs |
| R_{DIS} | Discharge resistor in power down | | | 100 | 200 | Ω |
| C_{OUT} | Output capacitance | | 0.5 | 1.0 | 1.3 | μF |

Electrical Characteristics (continued)

Over recommended free-air temperature and over recommended input voltage (typical at an ambient temperature range of 27°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---------------------------------------|--|---------------------------|-----|------|------|
| CLOCK GENERATION | | | | | | |
| f _{XTAL} | External reference clock | | 3 | 24 | 27 | MHz |
| t _{start} | PLL start-up time | With FL2000044 crystal to 0.1% accuracy of the target frequency | 1 | | | ms |
| XTAL ESR | | | 50 | 150 | | Ω |
| f _{HCLK} | Output clock | minimum programmable frequency | 3.8 | 4 | 4.2 | MHz |
| | | maximum programmable frequency | 63.8 | 64 | 64.2 | MHz |
| D _{HCLK} | HCLKx duty cycle driven by PLL output | | 45% | 55% | | |
| t _{rise} | HCLKx rise time | Measured from 10% to 90%, DRV_STR_x[1:0] = 2 mA | 2 | | 5 | ns |
| t _{fall} | HCLKx fall time | Measured from 90% to 10%, DRV_STR_x[1:0] = 2 mA | 2 | | 5 | ns |
| T | HCLKx jitter | 3σ cycle-to-cycle. Greater than 1000 cycles. Difference between two consecutive cycles | | | 600 | ps |
| C _{load} | HCLKx load | maximum load capacitance for frequencies between 4 MHz and 32 MHz | | | 10 | pF |
| | | maximum load capacitance for frequencies up to 64 MHz | | | 5 | |
| V _{OH} | HCLKx output high voltage | I _{OH} = 8 mA | 0.7*V _{S_IO_OUT} | | | V |
| V _{OL} | HCLKx output low voltage | I _{OL} = 8 mA | 0.2*V _{S_IO_OUT} | | | V |
| THERMAL SHUTDOWN | | | | | | |
| | WLED BOOST thermal shutdown | Trip temperature | 140 | 160 | | °C |
| | | Hysteresis | 20 | | | |
| | Core buck thermal shutdown | Trip temperature | 140 | 160 | | °C |
| | | Hysteresis | 20 | | | |
| | LDO thermal shutdown | Trip temperature | 140 | 160 | | °C |
| | | Hysteresis | 20 | | | |
| OSCILLATOR (for digital core) | | | | | | |
| f _{osc} | Oscillator frequency | | 1.8 | 2 | 2.2 | MHz |
| S_VSYNC | | | | | | |
| V _{IH} | Input high level | | 1.0 | | | V |
| V _{IL} | Input low level | | 0.4 | | | V |
| R _{PD (S_VSYNC)} | S_VSYNC internal pull-down | Only present when V _{S_VSYNC} is below V _{IL} threshold | 5 | 10 | kΩ | |

Electrical Characteristics (continued)

Over recommended free-air temperature and over recommended input voltage (typical at an ambient temperature range of 27°C) (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|---------------------------|-------|---------------------------|------|
| I²C I/Os (SDA, SCL) (IO_OUT voltage) | | | | | | |
| I _{LK} | Input leakage current | Clamped to GND or 3.3 V | –1 | | 1 | μA |
| V _{IH} | Input high level | | 0.7*V _{IO_OUT} | | | V |
| V _{IL} | Input low level | | | | 0.3*V _{IO_OUT} | V |
| V _{OL(SDA)} | Output low level (SDA) | I _{OL} = 3 mA | | | 0.2*V _{IO_OUT} | V |
| f _{SCL} | I ² C clock frequency | | | | 400 | kHz |
| GPIOs (GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5 and GPIO6) | | | | | | |
| V _{IH} | Input high level | Configured as Input | 1.2 | | | V |
| V _{IL} | Input low level | Configured as Input | | | 0.4 | V |
| I _{LK} | Input leakage current | Configured as input, clamped to GND or 3.3 V | –1 | | 1 | μA |
| V _{OH_PP} | Output high level for push-pull configuration | V _{O(IO_OUT)} = 1.8 V or V _{I(3V3_SUS)} = 3.3 V, I _{OH} = 8 mA | 0.8*VDD | | | V |
| V _{OL_PP} | Output low level for push-pull configuration | V _{O(IO_OUT)} = 1.8 V or V _{I(3V3_SUS)} = 3.3 V, I _{OL} = 8 mA | | | 0.2*VDD | V |
| V _{OL_OD} | Output low level for open-drain configuration | V _{O(IO_OUT)} = 1.8 V or V _{I(3V3_SUS)} = 3.3 V, I _{OL} = 8 mA | | | 0.2*VDD | V |
| I _{LK_OD} | Output leakage current for open-drain configuration | V _{O(IO_OUT)} = 1.8 V or V _{I(3V3_SUS)} = 3.3 V | | | 1 | μA |
| R _{PU} | GPIOs pull-up resistance if enabled | | | 50 | | kΩ |
| C _{IN} | Internal pin capacitance | | | 3.19 | 3.21 | pF |
| SENSOR PASS GATES (GPIO1 to SDA and GPIO2 to SCL) | | | | | | |
| R _{DS} | SDA and SCL to GPIO1 and GPIO2 daisy chain switch on resistance | | | | 25 | Ω |
| LOGIC INPUTS (S_STROBE, I2C_ICA, I2C_ICB) (S_IO_OUT voltage dependent - 3.3-V Tolerant) | | | | | | |
| I _{LK} | Input leakage current (does not apply to S_STROBE) | Clamped to GND or 3.3 V | –1 | | 1 | μA |
| V _{IH} | Input high level | | 1.2 | | | V |
| V _{IL} | Input low level | | | | 0.4 | V |
| R _{PD} (S_STROBE) | S_STROBE pull-down | | | 50 | | kΩ |
| C _{IN} | Input pin capacitance | | | 1.257 | 5.57 | pF |
| LOGIC OUTPUTS (S_RESETN, S_ENABLE, S_IDLE) | | | | | | |
| V _{OH} | Output high level | I _{OH} = 8 mA | 0.8*V _{S_IO_OUT} | | | V |
| V _{OL} | Output low level | I _{OL} = 8 mA | | | 0.2*V _{S_IO_OUT} | V |
| LOGIC I/Os (RESET_IN) (3V3_SUS voltage) | | | | | | |
| I _{LK} | Input leakage current | Clamped to GND or 3.3 V | –1 | | 1 | μA |
| V _{IH} | Input high level | | 0.9 | | | V |
| V _{IL} | Input low level | | | | 0.5 | V |
| R _{PU} | RESET_IN pull-up resistance | | | 50 | | kΩ |

7.6 Timing Requirements - Data Transmission

VDD = 1.8 ± 5%, T_A = 25°C, C_L = 100 pF (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--------------------------------|------------|-----|-------------|------------|
| f _(SCL) Serial clock frequency | | | | 100 400 | kHz kHz |
| t _(BUF) Bus free time between stop and start condition | SCL = 100 kHz SCL = 400 kHz | 4.7 1.3 | | | μs μs |
| t _(SP) Tolerable spike width on bus | SCL = 100 kHz SCL = 400 kHz | | | 50 | ns |
| t _{LOW} SCL low time | SCL = 100 kHz SCL = 400 kHz | 4.7 1.3 | | | μs μs |
| t _{HIGH} SCL high time | SCL = 100 kHz SCL = 400 kHz | 4.0 600 | | | μs ns |
| t _{S(DAT)} SDA → SCL setup time | SCL = 100 kHz SCL = 400 kHz | 250 100 | | | ns ns |
| t _{S(STA)} Start condition setup time | SCL = 100 kHz SCL = 400 kHz | 4.7 600 | | | μs ns |
| t _{S(STO)} Stop condition setup time | SCL = 100 kHz SCL = 400 kHz | 4.0 600 | | | μs ns |
| t _{H(DAT)} SDA → SCL hold time | SCL = 100 kHz SCL = 400 kHz | 0 0 | | 3.45 0.9 | μs μs |
| t _{H(STA)} Start condition hold time | SCL = 100 kHz SCL = 400 kHz | 4.0 600 | | | μs ns |
| t _{r(SCL)} Rise time of SCL signal | SCL = 100 kHz SCL = 400 kHz | | | 1000 300 | ns ns |
| t _{f(SCL)} Fall time of SCL signal | SCL = 100 kHz SCL = 400 kHz | | | 300 300 | ns ns |
| t _{r(SDA)} Rise time of SDA signal | SCL = 100 kHz SCL = 400 kHz | | | 1000 300 | ns ns |
| t _{f(SDA)} Fall time of SDA signal | SCL = 100 kHz SCL = 400 kHz | | | 300 300 | ns ns |

7.7 Typical Characteristics

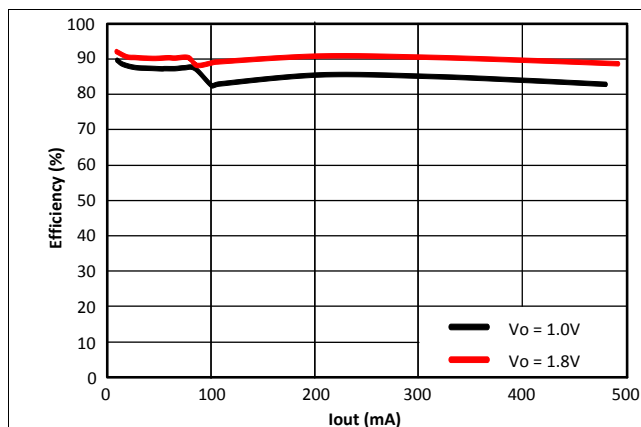


Figure 1. Buck Efficiency vs. Output Current

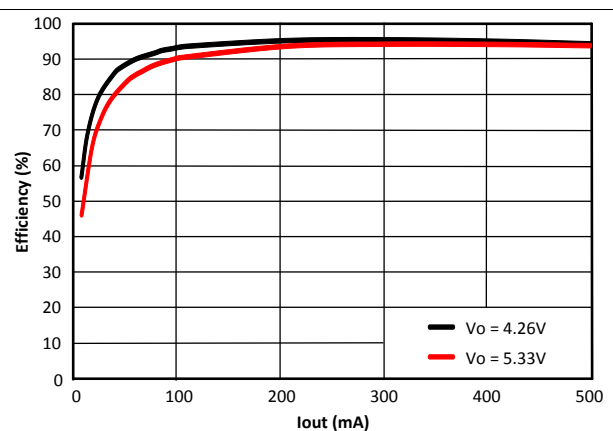


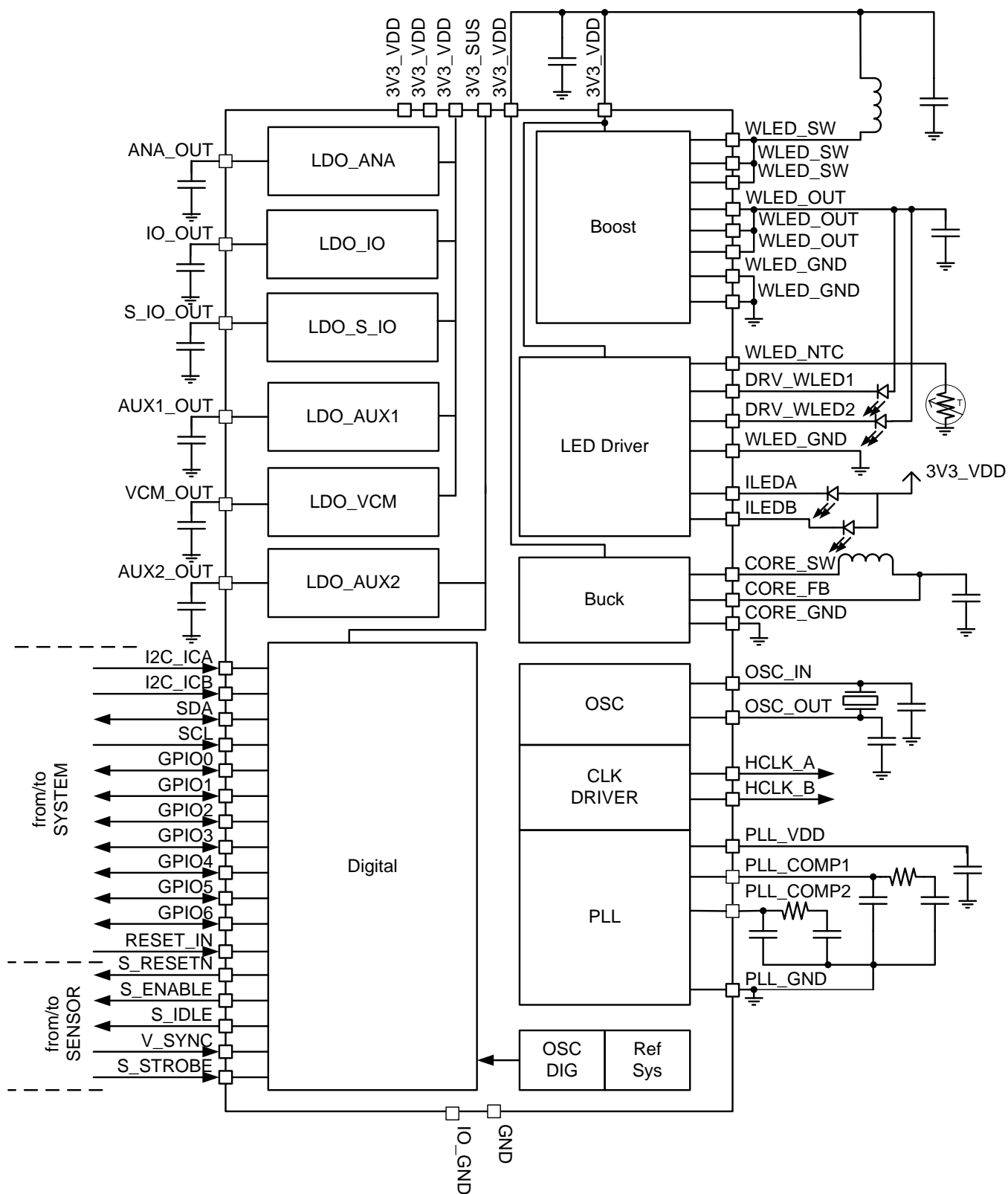
Figure 2. Boost Efficiency vs. Output Current

8 Detailed Description

8.1 Overview

The TPS68470 device is an advanced power management unit that powers a Compact Camera Module (CCM), generates the clock, and drives a dual LED Flash. The TPS68470 is capable of generating all power rails required by a CCM. It has a high efficiency, state of the art buck converter for the image sensor digital supply (CORE Voltage Regulator). An analog voltage rail for the image sensor analog supply is generated with an LDO (LDO_ANA). A Phase Locked Loop (PLL) generates the clock with an option to introduce spread spectrum by enabling a secondary integrated PLL. The TPS68470 also has a high efficiency, state of the art boost converter to support two 1A LED flash drivers. The LED currents are controlled with a regulated low side current source. Additional LDOs are also integrated in the TPS68470: two IO supply voltage generation LDOs (LDO_IO and LDO_S_IO), two auxiliary LDOs (LDO_AUX1 and LDO_AUX2), and a VCM driver supply LDO (LDO_VCM).

8.2 Functional Block Diagram



8.3 Feature Description

The following sections describe the specific features of the TPS68470 device.

8.3.1 Power-Up Sequence and Modes

The TPS68470 receives power from the 3V3_VDD and 3V3_SUS pins. Power to all voltage regulators except for LDO_AUX2 comes from the 3V3_VDD pin. In order for this device to remain partially functional during a system-standby mode, the 3V3_SUS pin powers LDO_AUX2, the internal digital logic circuitry and the generic GPIOs (when configured for 3.3V operation).

The power-up sequence is shown in Figure 3. Applying 3V3_SUS and 3V3_VDD for the first time starts the internal power-up sequence. Upon completion of the internal power-up sequence, the TPS68470 enters the active state. A detection of the 3V3_VDD voltage enables LDO_IO so as to power up the I²C bus during the active state which allows the programming of the I²C registers. If the 3V3_VDD rail drops below its UVLO voltage threshold and the 3V3_SUS rail remains above its UVLO voltage threshold, all active blocks will be turned off and the TPS68470 enters its sleep state. In the sleep state, the device consumes a minimal amount of power and all registers hold their values since the digital core is powered from the 3V3_SUS rail. When the 3V3_VDD is once again applied, the device will enter the active state and LDO_IO is enabled. If both the 3V3_SUS and 3V3_VDD rails drop below their UVLO voltage thresholds, the TPS68470 will shutdown.

NOTE: If 3V3_VDD is present, then 3V3_SUS must also be present. Otherwise a leakage current from 3V3_VDD to ground will exist.

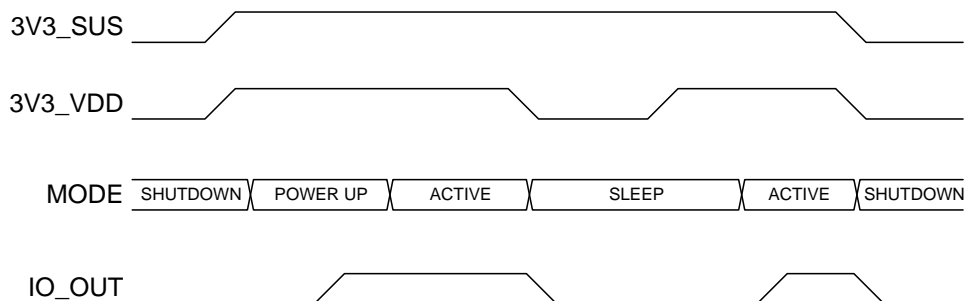


Figure 3. Power-Up Sequence and Modes of Operation

TPS68470 modes:

| | |
|----------|---|
| SHUTDOWN | When 3V3_SUS and 3V3_VDD are both below the power on reset (POR) voltage levels, the device is in shutdown. |
| POWER UP | When the TPS68470 is powered the first time by pulling 3V3_SUS and 3V3_VDD high, an internal state machine performs a power-up sequence. During the power-up sequence, the TPS68470 reads all factory trim values into the digital core registers after which it automatically enters the active state. The oscillator is turned off after the power up sequence in order to reduce power consumption. |
| ACTIVE | The TPS68470 enters the active state from the power up or sleep mode. The TPS68470 is in the active mode when 3V3_SUS and 3V3_VDD are above UVLO levels. When the TPS68470 is in the active mode, the reference, UVLO of 3V3_SUS and 3V3_VDD, and LDO_IO are always powered up. The oscillator is enabled automatically if timing is needed by any function. When in active mode, the I ² C registers can be accessed and any function in the TPS68470 can be enabled. |
| SLEEP | The TPS68470 will enter the sleep mode from the active mode if 3V3_VDD is pulled low and 3V3_SUS is kept high. This is the lowest power mode where register values are kept. In sleep mode, the I ² C is not active since LDO_IO is not enabled. The TPS68470 can exit from sleep mode by pulling 3V3_VDD high. |

Feature Description (continued)

8.3.2 Clock Generation

The TPS68470 has a built in crystal oscillator driver, a phase lock loop, and clock dividers for clock generation to the sensor and internal switching converters. To reduce possible noise coupling to other parts in the system, a spread spectrum PLL can be enabled to drive the HCLK_A and HCLK_B outputs.

Internal switching regulator clocks are generated from the PLL output and the dividers for the Boost and Buck need to be set accordingly. Since the Boost is switching at 2 MHz, the clock to the Boost regulator must also be set as close as possible to 2 MHz. This is accomplished by configuring the BOOSTDIV [4:0] bits in the BOOSTDIV register such that the clock to the Boost regulator is set as close as possible to 2 MHz.

The Buck clock should be set as close as possible to 5.2 MHz. This is accomplished by configuring the BUCKDIV [3:0] bits in the BUCKDIV register such that the clock to the Buck regulator is set as close as possible to 5.2 MHz. Shown in Figure 4 is the block diagram of the clock generation with control bits from the digital core to set the wanted clock at the HCLK_A and HCLK_B output pins.

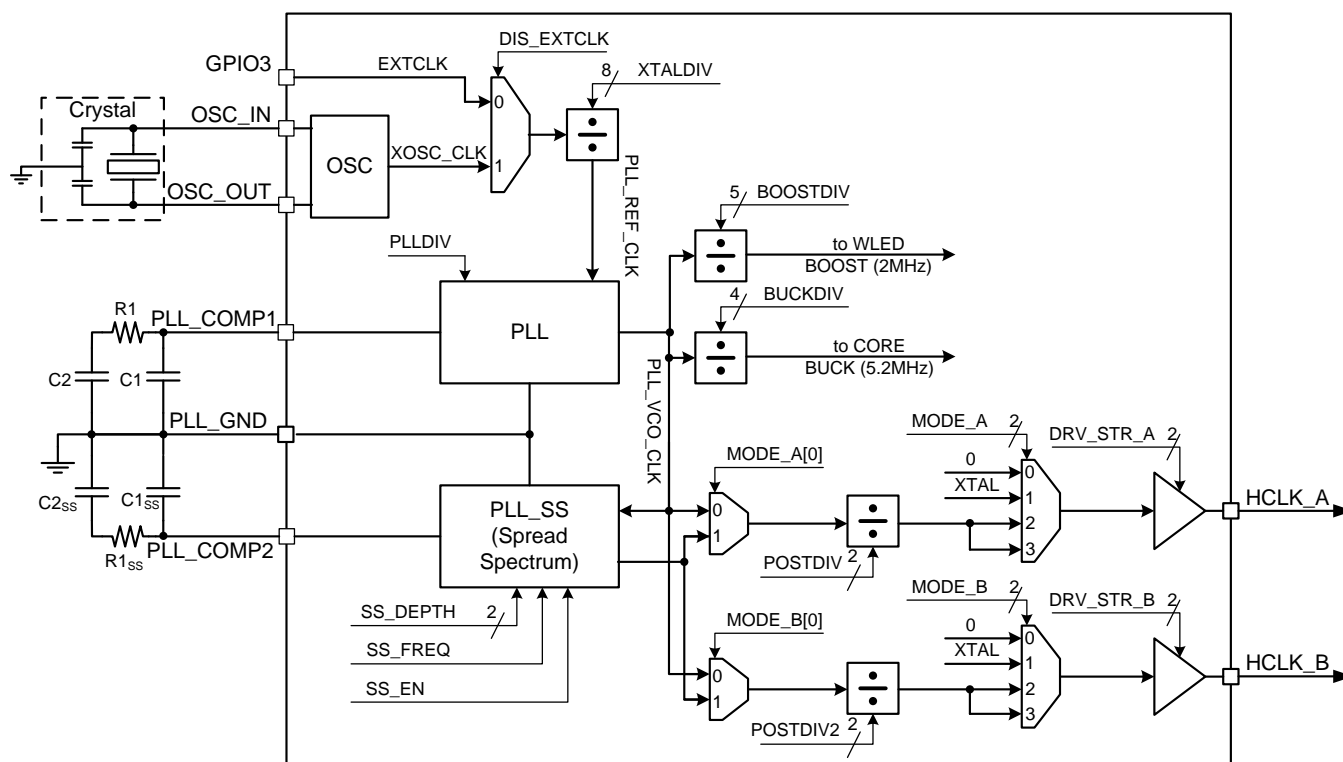


Figure 4. TPS68470 Clock Generation Block Diagram

8.3.2.1 Crystal Oscillator

The input range of the crystal can be anything from 3 MHz up to 27 MHz allowing usage of a wide range of crystal resonators. The oscillator is enabled if either EN_PLL (PLLCTL register) or EN_PLL_SS (PLLCTL2 register) is enabled, or MODE_A or MODE_B (CLKCFG1 register) are selected to '01'. The oscillator is disabled when an external clock is selected to the PLLs by writing the DIS_EXTCLK (PLLCTL register) bit low. In this case, the PLL reference clock is driven by the GPIO3 pin. The oscillator output is divided down before the PLL and can be controlled using the XTALDIV register. To channel the oscillator output to the HCLK_A or HCLK_B pins, set the MODE_A or MODE_B control bits in the CLKCFG1 register to '01'. The crystal oscillator input amplifier has tunable capacitors for the OSC_IN and OSC_OUT pins. The pin capacitance can be controlled using the CON_XTAL_C[2:0] bits in the PLLCTL register.

Feature Description (continued)

8.3.2.2 Phase Locked Loop (PLL)

The PLL is powered by the PLL_VDD LDO and it is automatically enabled when the EN_PLL bit is set high in the PLLCTL register or when the MODE_A and/or MODE_B control bits in the CLKCFG1 register are set to '01'. The PLL is used to multiply the crystal oscillator frequency range of 3 MHz to 27 MHz by a programmable factor of $F = (M/N) \cdot (1/P)$ such that the output available at the HCLK_A or HCLK_B pins are in the range of 4 MHz to 64 MHz in increments of 0.1 MHz.

M is controlled by the PLLDIV register and N by the XTALDIV register. The effective value of N is d'30 + XTALDIV [7:0]. The effective value of the M is d'320 + PLLDIV [8:0]. The value of P is controlled by the POSTDIV register 2-bit field and allows the PLL raw output, denoted as PLL_VCO_CLK, to be divided down by factors of 1, 2, 4 or 8 before exiting the IC. The PLL frequency should be set during the TPS68470 power up. The PLL is enabled with the register bit EN_PLL after both dividers described above have been configured.

Note: The XTALDIV and PLLDIV settings should not be modified while the PLL is in operation. The POSTDIV settings may be modified in operation if a finite changeover time can be tolerated by the application.

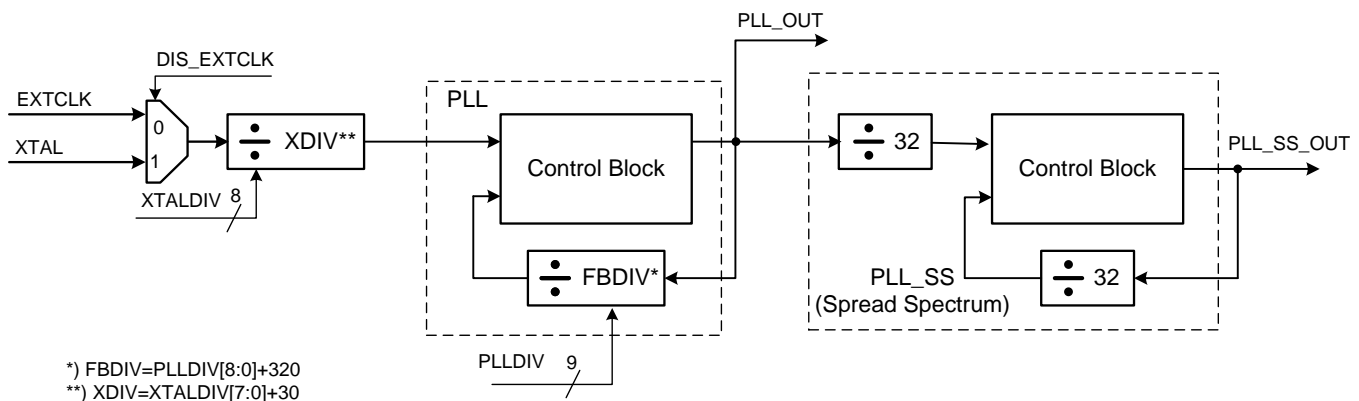


Figure 5. PLL Block Diagram

The correct programming of the XTALDIV, PLLDIV and POSTDIV registers is essential for proper operation of the PLL. The crystal oscillator output, XOSC_CLK, is first divided by a programmable 8 bit divider (XTALDIV) and used as the reference clock (PLL_REF_CLK) to the PLL. Choose the XTALDIV such that the PLL_REF_CLK is exactly 100 kHz. If an exact 100 kHz is not achievable, set it as close to 100 kHz as possible. If there is a choice between values lower than 100 kHz or higher, it is recommended to pick the higher value. The PLL has a programmable 9 bit feedback loop divider (PLLDIV). The PLLDIV value is set so as to multiply PLL_REF_CLK to a PLL_VCO_CLK value in the range of 32 MHz to 64 MHz. Since more than one PLLDIV value will satisfy this last criterion, it is recommended to choose the smallest value possible, such that when followed by POSTDIV of 1, 2, 4, or 8, the final desired output clock on the HCLK_A or HCLK_B pins is obtained. The use of PLLDIV and POSTDIV allows the VCO frequency range to be narrow to achieve a more linear transfer characteristic for the VCO and simultaneously allows a wide final output frequency range by configuring POSTDIV appropriately.

Gain of the Voltage Controlled Oscillator (VCO) inside the PLL is normally set internally by the value of the PLLDIV register according to Table 1. The purpose of the automatic control is to center the VCO control voltage denoted by the PLL_COMP1/PLL_COMP2 pins well within the supply range and achieve the most linear VCO transfer function denoted as MHz/V. The VCO gain can be overridden using the VCOSPEED register under special circumstances. To do so the OVR bit must be set and a SPEED [2:0] is to be programmed in lieu of the automatic setting. A rule of thumb in choosing the SPEED [2:0] value to avoid saturating the PLL_COMP voltage at either GND or VDD potential is to set it manually to within ± 2 codes of the value in Table 1. For example for PLLDIV 0...31, default SPEED [2:0] value is 000. So do not exceed 010 or else the PLL_COMP voltage will be too low since the VCO gain will be increased at setting 010 vs 000. Similarly for PLLDIV values 288...511, default SPEED [2:0] bits are 111. So do not go below 101 or the VCO gain will be too low to achieve the required frequency.

Feature Description (continued)

NOTE

It is highly recommended not to modify VCOSPEED as it can have adverse consequences for PLL stability and ability to meet the desired target frequency.

The PLL is equipped with a timer based lock signal that is asserted after the start-up timer has reached its maximum value. The timer delay is set via I²C in the PLLSWR register using the SWR [1:0] bits. It is to be noted that the true lock time of the PLL is set by the loop characteristics. The timer is intended to provide a reasonable indicator of when the PLL has locked. The LOCK time should be set to its maximum value in order to avoid a situation where the LOCK signal goes high well before the actual VCO locks to the target frequency. The LOCK timing does not affect the actual PLL operation. It is simply provided as an indicator to external circuits that may need the PLL output on the HCLK_A and HCLK_B pins to be stable before being used.

The PLL uses an external loop filter which should be connected between PLL_COMP1 and PLL_GND to avoid noise coupling to the VCO. The recommended filter components are shown in Figure 4. The component values of C1 = 2.2 nF, C2 = 10 nF, R1 = 8.2 kΩ are recommended. These values are designed to work across the entire input and output frequency ranges of the PLL for optimal performance of stability, loop bandwidth and lock time.

Table 1. Internally Defined VCOSPEED Settings

| PLLDIV VALUE [dec] | M (=PLLDIV+320) [dec] | SPEED BITS ⁽¹⁾ [bin] |
|-----------------------|--------------------------|------------------------------------|
| 0...31 | 320...351 | 000 |
| 32...63 | 352...383 | 001 |
| 64...95 | 384...415 | 010 |
| 96...143 | 416...463 | 011 |
| 144...191 | 464...511 | 100 |
| 192...223 | 512...543 | 101 |
| 224...287 | 544...607 | 110 |
| 288...511 | 608...831 | 111 |

(1) LSB and MSB of the SPEED bits are crossed silicon version 1p0

NOTE

Boost and Buck clock dividers are not glitchless so clock divider controls should be set before enabling PLL.

8.3.2.3 Spread Spectrum Modulator

The TPS68470 has a separate PLL for generating a clock signal with spread spectrum. This PLL_SS is enabled using the register bit EN_PLL_SS. The PLL_SS is designed to have fixed reference divider of 32 and fixed feedback divider of 32. Hence it functions as a 1:1 ratio PLL. SS_FREQ and SS_DEPTH bits can be used to control spread spectrum options. SS_FREQ controls the triangular spreading frequency either to 15 kHz or 30 kHz and the SS_DEPTH control bit can be used to change modulation depth in percentage. The SS_DEPTH is the peak \pm change in frequency vs. time resulting from the modulation. If the PLL_SS frequency is plotted vs. time, it would be a triangular waveform whose peak deviation from the mean would be equal to SS_DEPTH. The SS_FREQ is the periodicity of the modulation i.e., if the PLL_SS frequency is plotted vs. time, the period of the triangular modulation would be the reciprocal of SS_FREQ. The PLL_SS will similarly give a lock signal after the start-up timer has reached its maximum value, set by the SWR_SS bits. Spread spectrum PLL output has an output divider that can be controlled from the POSTDIV and POSTDIV2 control registers. Clock driver for HCLK_A and HCLK_B bits can be driven with or without spread spectrum and can be controlled by the MODE_A and MODE_B bits.

8.3.2.4 Clock Drivers

A clock is driven out from the HCLK_A and HCLK_B pins provided LDO_S_IO is enabled. The output signal to these pins can be selected from the MODE_A [1:0] and MODE_B [1:0] control bits in the CLKCFG1 register. The HCLK_A and HCLK_B outputs can be either disabled, XTAL, PLL, or PLL spread spectrum per [Table 2](#). Their output drive strengths can be controlled with the DRV_STR_A [1:0] and DRV_STR_B [1:0] bits in the CLKCFG2 register.

If both HCLK_A and HCLK_B are to be used, both must be configured using the CLKCFG1 register using a single write command. In order to enable one of the clocks after the other clock is already enabled, both must be disabled before an enable write command is accepted. In addition, if either or both are enabled, they must be disabled prior to turning off the PLL.

Table 2. HCLK_A and HCLK_B Clock Source Selection

| MODE_A [bin] | MODE_B [bin] | HCLK_A SIGNAL | HCLK_B SIGNAL |
|-----------------|-----------------|----------------------|-----------------------|
| 00 | 00 | No Output | No Output |
| 01 | 01 | XTAL | XTAL |
| 10 | 10 | PLL after POSTDIV | PLL after POSTDIV2 |
| 11 | 11 | PLL_SS after POSTDIV | PLL_SS after POSTDIV2 |

NOTE

When only one clock output is needed, the unused output pin should be left as not connected.

8.3.3 GPIO and Interrupt Generation

The TPS68470 has 7 GPIO pins that can be configured as inputs or outputs along with other features using the GPCTLxA and GPCTLxB registers.

As Inputs, they can be configured with the following options (defaults are shown in bold).

- Voltage (**LDO_IO level** or 3V3_SUS level)
- Hysteresis (**yes**, no)
- 50-kΩ pull-up (**yes**, no)
- Polarity (**normal**, Inverted)
- Edge / level detection (level, negative edge, **positive edge**)

As outputs, they can be configured as voltage or current drivers with the following options (defaults are shown in bold).

- Voltage mode (**LDO_IO level** or 3V3_SUS level)
- Current mode driver topology (open drain) and drive strength (**1**, 2, 4, or 8 mA)
- Polarity (**normal**, Inverted)

When configured to LDO_IO level, the GPIO input/output buffer is powered from the LDO_IO supply. When configured to 3V3_SUS level, it is powered from the 3V3_SUS input rail.

8.3.3.1 I²C Daisy Chain

Some image sensors do not allow for the IO line to be powered before the other power rails are up. This limitation prevents the main I²C bus on the TPS68470 and the host processor from being directly connected to the sensor I²C since this needs to be active before any output power from the TPS68470 is being generated.

The TPS68470 has a dedicated sensor IO LDO (LDO_S_IO) and two GPIOs (GPIO 1 and GPIO 2) that can be controlled using the S_I2C_CTL register. The S_EN_IO bit in the S_I2C_CTL register enables/disables the sensor IO LDO. The S_EN_I2C bit in the S_I2C_CTL register configures GPIO1 (SDA) and GPIO2 (SCL) as pass gates for the sensor I²C signals. This way the host processor can enable all sensor power rails before enabling the sensor IO supply (LDO_S_IO) and opening the pass gates from SDA to GPIO1 and SCL to GPIO2.

During I²C communications, the TPS68470 will never show an incomplete I²C transaction.

NOTE

When SDA and SCL are routed to GPIO1 and GPIO2, the mode for these GPIOs must be configured using their respective GPCTLxA registers as inputs with no pull-ups.

8.3.3.2 Programmable Interrupt Trigger

The Programmable Interrupt Trigger (PIT) feature can be used to trigger an external event such as an Interrupt or a Wake-up. The configuration for the PIT is accomplished using the WAKECFG register and controlled using the PITCTL register. The inputs to the PIT include the following:

- The value of each generic GPIO pin that is configured as an Input
- The value of the WAKE bit in the TPS68470 global status register (GSTAT)

Using the WAKECFG register, the WAKE bit in the GSTAT register can be routed to any GPIO pin that is configured as an output. Likewise, any GPIO configured as an input can be used to trigger the Wake-up event provided the GPIO wake control is enabled using the PITCTL register. The polarity of the GPIO input and GPIO output is controlled using the respective GPCTLxB register. The same register can be used to define whether the input is edge or level sensitive. If a level sensitive trigger is used, the Wake signal is cleared when the input state becomes inactive. In the case of an edge sensitive input, the state is held until it is cleared by writing a '1' to the respective bit in the IOWAKESTAT register.

The above mentioned description for the Wake signal also applies if the GPIO is configured as an Interrupt output. In the case where the same GPIO pin is configured for both a Wake and Interrupt event, the PIT performs a logical OR between the two events.

NOTE

The PIT block is powered from the 3V3_SUS rail, such that it remains fully functional when the main 3V3_VDD rail is absent.

8.3.3.3 Internal Interrupt Signals

Internally, the TPS68470 generates numerous types of different status information which can be used to generate an interrupt to an external controller. The user can select which events will generate an interrupt by either masking or unmasking a specific status in the INTMASK register. The INT_CONF[2:0] bits in the WAKECFG register can be used to select which of the GPIOs will be used as an interrupt output.

8.3.4 Sensor GPO Signals

The TPS68470 has three dedicated discrete signals (S_ENABLE, S_IDLE and S_RESETN) to support an Image sensor. These signals have a direct connection to the image sensor inside the Compact Camera Module. All three signals are permanently configured as LDO_S_IO level outputs. Drive strength of these output buffers can be configured using the SGPO register. The level on each signal (Low or High) reflects the value written to bits in the SGPO register (0 or 1). These signals are used to manage the Sensor Reset, Power Up and Power Down mode change operation.

8.3.5 Power-Up and Software Reset

The TPS68470 power-up-reset unit generates an internal reset event when the sustaining supply (3V3_SUS) powers up. Asserting RESET_IN low after 3V3_SUS is within regulation limits will also generate an internal reset event. Following a reset event, the TPS68470 state is initialized as follows:

- All internal registers are set to their default state
- All external voltage regulator outputs are connected to GND with internal pull-down resistor, except for the WLED Boost which has a diode between WLED_SW and WLED_OUT, anode and cathode respectively
- All GPIOs are configured as input with internal pull-up to IO_OUT
- All sensor outputs (S_ENABLE, S_IDLE and S_RESETN) are driven to an output low level voltage

The TPS68470 can also be reset by writing 0xFF to the RESET register. This software reset will initialize the device in the same manner as a power-up reset. Since all internal registers are set to a default state following a reset event, it is recommended that all interrupts be serviced prior to initiating a software reset. Otherwise, if the source of the interrupt is no longer present, the interrupt status flag will no longer provide information on the source of the interrupt. However, if the source of the interrupt is still present, the interrupt status flag will once again report the status after the device initialization is complete.

The RESET register is self clearing so it is not necessary to go back and write to the register once the initialization is complete.

8.3.6 Core Buck

The TPS68470 has a synchronous step-down converter which operates at a maximum frequency of 6-MHz pulse width modulation (PWM) at moderate to heavy load currents.

The converter uses a unique frequency locked ring oscillating modulator to achieve best-in-class load and line response which allows the use of tiny inductors and small ceramic input and output capacitors. At the beginning of each switching cycle, the high-side MOSFET switch is turned on and the inductor current ramps up raising the output voltage until the main comparator trips. Once the main comparator trips, the control logic turns off the high side MOSFET switch.

A key advantage of this non-linear architecture is that there is no traditional loop compensation. The loop response to a change in the output voltage (CORE_FB) is essentially instantaneous. As a result, an excellent load transient response is achieved. The absence of a traditional, high-gain compensated linear loop means that the buck converter is inherently stable over a wide range of Inductors and output capacitor values. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, the architecture of this converter uses an internal Frequency Lock Loop (FLL) which holds the switching frequency constant over a wide range of operating conditions.

8.3.6.1 Buck Converter Switching Frequency

The magnitude of the internal ramp, which is generated from the duty cycle (D), reduces for duty cycles on either side of $D = 50\%$. Thus, there is less overdrive on the main comparator inputs which would normally tend to slow the conversion down. The intrinsic maximum operating frequency of the converter is about 10 MHz to 12 MHz, which is controlled to approximately 5.2 MHz by the integrated frequency locked loop.

When high or low duty cycles are encountered, the loop runs out of range and the conversion frequency falls below 5.2 MHz. The tendency is for the converter to operate more towards a "constant inductor peak current" rather than a "constant frequency". In addition to this behavior which is observed at high duty cycles, it is also noted at low duty cycles.

When the converter is required to operate towards the nominal 5.2 MHz at extreme duty cycles, the application can be assisted by decreasing the ratio of inductance (L) to the output capacitor's equivalent serial inductance (ESL). This increases the ESL step seen at the main comparator's feed-back input thus decreasing its propagation delay which increases the switching frequency. These factor help to implement a high performance camera module in a very small solution size.

8.3.6.2 Buck Converter Internal Current Limit and Short Detection

The Buck converter has an internal current limit and a thermal shutdown circuit to protect the device during fault conditions. If the maximum current is reached, the output voltage will drop since the load can no longer be supplied with sufficient power. If the thermal shutdown is triggered, the converter is turned off and the TSD bit in the VDCTL register is set . It is important to note that the thermal shutdown and subsequent setting of the TSD bit only occurs when the converter is operating in the PWM mode. During light loads, when the converter is operating in PFM mode, heat dissipation is non existent.

The Buck converter also has a short detection comparator that is triggered if the output, during normal operation, is below 0.5 V. An internal timer is triggered when Vout droops below 0.5V and after 10ms, the converter is turned off.

8.3.7 Low Dropout Voltage Regulators (LDOs)

All LDOs in the TPS68470 use the same topology where only the pass transistor is scaled based on the voltage and current requirements described in the [Electrical Characteristics](#). Each LDO has its own independent current limit. The LDOs have low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise and good PSRR with little ($V_{IN} - V_{OUT}$) headroom, make these LDOs ideal for compact camera module applications.

8.3.7.1 LDO Output Capacitor Requirements

Ceramic capacitors are recommended, because these capacitors have minimal variation in capacitance value and equivalent series resistance (ESR) over temperature. Based on the temperature expected on the board, X5R or X7R type capacitors should be used.

However, the LDOs in the TPS68470 are designed to be stable with minimum effective capacitance at the output that is stated in the electrical characteristics table of each LDO. Thus, the LDOs are stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than stated in the electrical characteristics table. This effective capacitance refers to the capacitance that the LDO sees under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature de-rating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with stated effective capacitance also enables the use of smaller footprint capacitors that have higher de-rating in size and space constrained applications.

Using a capacitor rated at the minimum stable value at the output of the LDO does not ensure stability because the effective capacitance under the specified operating conditions would be less than specified. From an ESR perspective, the recommendation is to use capacitors with a maximum ESR less than 200 mΩ.

8.3.7.2 LDO Internal Current Limit and Short Detection

All LDOs have internal current limit to protect the device during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} - V_{OUT}) \times I_{LIMIT}$ until thermal shutdown is triggered. If the thermal shutdown is triggered, all power rails except LDO_IO are turned off .

All LDO outputs also have a short detection comparator that is triggered if the output, during normal operation, is below 0.5 V. An internal timer is triggered when Vout droops below 0.5V and after 10 ms, the LDO is turned off. If a short is detected, the enable bit for the shorted LDO is cleared and if an interrupt is generated due to the short condition, the VRSHORT register can be used to determine which LDO has a shorted output.

8.3.7.3 Dropout Voltage

All LDOs use a PMOS pass transistor to achieve a low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

As with any linear regulator, PSRR and transient responses are degraded as $(V_{IN} - V_{OUT})$ approaches dropout.

8.3.8 WLED Boost Converter and WLED Drivers

The TPS68470 employs a 2-MHz constant-frequency, current-mode boost converter to generate the output voltage required to drive high-power LEDs. The device integrates a power stage based on an NMOS switch and a synchronous NMOS rectifier. The device also implements two linear low-side current regulators to control the LED currents when the WLED voltages are higher than the diode forward voltage.

The duty cycle of the converter is set by the error amplifier and the saw-tooth ramp applied to the comparator. Because the control architecture is based on a current-mode control, a compensation ramp is added to allow stable operation at duty cycles larger than 50%. The converter is a fully-integrated synchronous-boost converter, always operating in continuous-conduction mode. This allows low-noise operation, and avoids ringing on the switch pin, which would be seen on a converter when entering discontinuous-conduction mode.

The boost converter of the TPS68470 not only operates as a regulated current sink but also as a standard voltage-boost regulator. In the device, the voltage-mode operation can be activated by a software command using the VMODE bit in the VWLEDCTL register. The output must be enabled using the ENABLE bit in the VWLEDCTL register. This additional operating mode can be useful when supplying other high-power devices in the system, such as a hands-free audio power amplifier, or any other component requiring a supply voltage higher than the system supply voltage.

The WLED Boost power stage is capable of supplying a maximum total output current of 2 A. The TPS68470 provides two constant-current sinks, one on the DRV_WLED1 pin and the other on the DRV_WLED2 pin, such that each is capable of sinking up to 1000 mA while in flash mode. In order to keep track of LED operation, the LEDs are monitored using the WLEDSTAT register. Additionally, the WLED Boost die temperature is monitored using the WLED_T[1:0] bits in the VWLEDCTL register.

Control of the WLED Boost and WLED drivers is done using the I²C interface. Some of the features are listed below.

- The WLED Boost can be set in constant output voltage mode using the VMODE bit in the VWLEDCTL register
- The WLED Boost output voltage can be adjusted while in constant output voltage mode with the VWLEDVAL register
- The WLEDs can be set to one of four modes (Flash, Torch/Video Light, Red-Eye Reduction and Focus Assist) by using the MODE[1:0] bits in the WLEDCTL register
- The brightness of the external WLEDs can be controlled with the WLEDMAXF (Flash), WLEDMAXT (Torch/Video Light), WLEDMAXRER (Red-Eye Reduction), and WLEDMAXAF (Focus Assist) registers
- Safety timers can be programmed using the WLEDTO and WLEDTIMER_MSB/WLEDTIMER_LSB registers.

8.3.8.1 WLED Driver Operation

The TPS68470 device can drive one or two LEDs for applications that require Flash, Torch/Video Light, Red-Eye Reduction, or Focus Assist functions. The TPS68470 device utilizes LED forward-voltage sensing circuitry on the DRV_WLED1 and DRV_WLED2 pins to optimize the power-stage boost ratio for maximum power efficiency. Due to the nature of the sensing circuitry, it is not recommended to leave any of the DRV_WLEDx pins unused if the operation has not been disabled via the DISLED1 or DISLED2 bits in the WLEDCTL register. Leaving the DRV_WLEDx pins unconnected, without disabling the respective LED driver output, forces the control loop into high gain, and eventually trips the output overvoltage protection. The DRV_WLEDx pins may be connected together to drive one or two LEDs at higher currents. Connecting the current sink inputs in parallel does not affect the internal operation of the TPS68470. For additional information on the proper operation, reference the DISLED1 and DISLED2 bits in the WLEDCTL register.

8.3.8.2 WLED Modes

For a more flexible system integration, the TPS68470 offers several options for activating the WLEDs. The WLEDs can be programmed to four different modes of operation by using the MODE[1:0] bits in the WLEDCTL register.

8.3.8.2.1 FLASH: MODE[1:0] = '00'

The flash operation can be triggered either by an I²C software command (START bit in the WLEDCTL register) or by means of a dedicated S_STROBE signal. To simplify flash synchronization with the camera module, the TPS68470 uses the S_STROBE input pin to turn on the WLED current with zero latency. In Flash mode, the S_STROBE input is always enabled. However, operation using the S_STROBE input requires that the S_IO_LDO be enabled. If the WLEDC1 and/or WLEDC2 register bits are set to a higher current than is set in the WLEDMAXF register, the current in flash mode will be limited by the WLEDMAXF register settings.

Regardless of whether the flash is operated using the S_STROBE signal or the I²C command, the maximum duration of the flash pulse is controlled by means of internal user-programmable safety timers configured using the WLEDTO register and the WLEDTIMER_MSB/WLEDTIMER_LSB registers.

The Flash trigger can be set to either edge or level sensitive. If set to edge sensitive, the WLED will turn on for the amount of time programmed by the FLASH[2:0] bits in the WLEDTO register or by the settings in the WLEDTIMER_MSB/WLEDTIMER_LSB registers, whichever time is less. If the trigger is set to level sensitive, the WLED will turn on and remain on for as long as the hardware signal (S_STROBE) or software command (START bit) is set to a logic high provided the total time is less than the time set by the FLASH[2:0] bits in the WLEDTO register.

NOTE

The WLEDTO register cannot be programmed while the WLED boost is enabled.

8.3.8.2.2 TORCH: MODE[1:0] = '01'

The Torch mode is enabled immediately once the MODE[1:0] bits in the WLEDCTL register are set to '01' and then the EN bit is set to a '1'. The torch mode is disabled by writing a '0' to the EN bit in the WLEDCTL register. In this mode, the S_STROBE input is disabled. The device regulates the LED current in torch/video light mode regardless of the S_STROBE input and the START bit. If the WLEDC1 and/or WLEDC2 register bits are set to a higher current than is set in the WLEDMAXT register, the current in torch mode will be limited by the WLEDMAXT register settings. A watchdog timer is present when the WLED mode is set to Torch/Video Light mode. In order to avoid the WLEDs from turning off as a result of the torch/video light safety timeout of 13 seconds, the MODE[1:0] must be refreshed within the 13 second window.

NOTE

The Torch timeout counter is based on the 2-MHz clock coming to the Boost regulator which may change depending on the clock generated from the PLL.

8.3.8.2.3 RED-EYE REDUCTION: MODE[1:0] = '10'

In this mode, the S_STROBE input is enabled. The flash pulse can be triggered by the S_STROBE synchronization signal, or by a software command (START bit in WLEDCTL register). If the WLEDC1 and/or WLEDC2 register bits are set to a higher current than is set in the WLEDMAXRER register, the current in the Red-Eye Reduction mode will be limited by the WLEDMAXRER register settings. When using the software command or edge trigger, the pulse length is determined by the WLEDTIMER_MSB and WLEDTIMER_LSB registers. The register bit settings in the WLEDTO safety timer limits the max pulse length in both S_STROBE and software mode and is calculated based on the RER[1:0] control bits.

8.3.8.2.4 FOCUS ASSIST: MODE[1:0] = '11'

In this mode, the S_STROBE input is disabled. The device regulates the LED current in focus assist light mode regardless of the S_STROBE inputs and the START bit. This mode is enabled immediately once the MODE[1:0] bits in the WLEDCTL register are set to '11' and then the EN bit is set to a '1'. If the WLEDC1 and/or WLEDC2 register bits are set to a higher current than is set in the WLEDMAXAF register, the current in the Focus Assist mode will be limited by the WLEDMAXAF register settings. The register bit settings in the WLEDTO safety timer limits the max pulse length and is calculated based on the FA[1:0] control bits.

8.3.8.3 WLED Trigger Options

If the MODE[1:0] bits in the WLEDCTL register are set to Flash or Red-Eye Reduction, the TPS68470 offers a couple of WLED trigger options.

8.3.8.3.1 Level-Sensitive Flash Trigger (TRIG = 0)

If the TRIG bit in the WLEDCTL register is set to 'Level Sensitive', the flash pulse is started either by a leading edge on the synchronization source (S_STROBE) or by a positive transition on the START bit. The polarity of the S_STROBE edge is set by the TRIG_POL bit in the WLEDCTL register. This bit does not have any effect on the polarity of the START bit. The internal safety timer defined by the settings in the WLEDTO register is triggered on the leading edge and stopped by a trailing edge of either the S_STROBE pin or the START bit. However, if the S_STROBE or START bit pulse width is greater than the time defined in the WLEDTO register, the WLEDTO register settings will dominate such that a timeout will occur reducing the flash pulse.

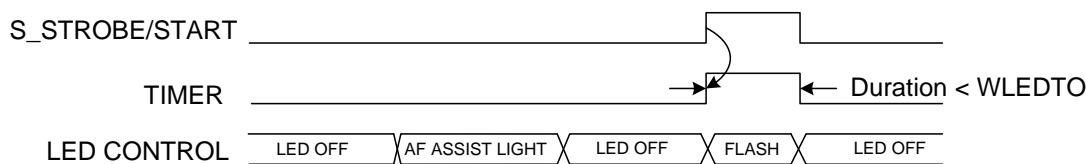


Figure 6. Level Sensitive Timer

8.3.8.3.1.1 Edge Trigger Flash (TRIG = 1)

If the TRIG bit in the WLEDCTL register is set to 'Edge Sensitive', the duration of the flash pulse is defined by the WLEDTIMER_MSB and WLEDTIMER_LSB registers provided that the duration is less than the register settings in the WLEDTO safety timer. The flash pulse is started either by a leading edge on the synchronization source (S_STROBE) or by a positive transition on the START bit. The polarity of the S_STROBE edge is set by the TRIG_POL bit in the WLEDCTL register. This bit does not have any effect on the polarity of the START bit. Once running, the timer ignores both types of triggering signals and only stops after the time set in the WLEDTIMER_MSB and WLEDTIMER_LSB registers expires. The START bit is reset by the timeout signal.

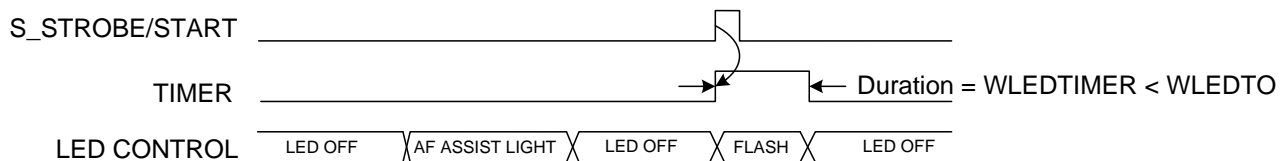


Figure 7. Edge Sensitive Timer (Single Trigger Event)

8.3.8.4 Blanking (Tx-Mask) for Instantaneous Flash-Current Reduction

The TPS68470 device has the capability of using GPIO2, GPIO3, or GPIO4 as a Tx-Mask hardware signal. The Tx-Mask signal can be used to reduce the overall current drawn from the battery if other system components require high energy at the same time. This dedicated hardware signal input can be configured using the TXMASK_CONF[1:0] bits in the WAKECFG register. When the Tx-Mask input signal is driven high, the WLED current in flash, red-eye reduction or focus assist mode is immediately reduced to the programmed torch mode level. The Tx-Mask function has no influence on the pulse duration set by the WLEDTO, WLEDTIMER_MSB and WLEDTIMER_LSB registers.

8.3.8.5 Voltage Mode

In this mode, the TPS68470 boost operates as a standard voltage-boost regulator. The voltage-mode operation is enabled by setting both the VMODE bit to a '1' and the ENABLE bit to a '1' in the VWLEDCTL register. The device regulates a constant output voltage between 3.68 V and 5.48 V based on the OV[3:0] bit settings in the VWLEDVAL register.

8.3.9 Indicator LED Operation

The TPS68470 device has dedicated pins for driving two indicator LEDs (ILED_A and ILED_B) which can be used for visual feedback to the camera operation mode or a Privacy Warning indicator. The indicator LED drivers are low-side constant current sources which drive low V_F LEDs. The ILED_A current is constant at 16mA. The ILED_B current is regulated directly from the 3V3_VDD input voltage and is programmed using the CTRLB[1:0] bits in the ILEDCTL register.

8.3.9.1 Retriggerable Pulse Extender

The Retriggerable Pulse Extender (RPE) block is enabled whenever the CORE buck is enabled. If S_VSYNC is driven high (3.3-V logic), the ILED_A output drive current is set to a max current of 16 mA regardless of the ENA bit setting in the ILEDCTL register. There is no dependency on any other register bit value.

The operation is as follows:

- If S_VSYNC is connected to GND (a logic low), the ILED_A ENA bit does not follow the state of the CORE enable
- If S_VSYNC is connected to 3.3V (logic high), the ILED_A ENA bit follows the state of the CORE enable
- The ILED_A can also be enabled via an I²C write
- S_VSYNC has an internal 10-k Ω pull-down resistor. If S_VSYNC is connected to 3.3 V, the 10-K pull-down path is removed to reduce leakage current

NOTE

When the RPE function is not used, S_VSYNC should be connected to GND. In this mode, the ILED_A driver enable does not depend on the state of the CORE buck enable. However, the ILED_A driver can still be enabled via the ENA bit in the ILEDCTL register.

8.3.10 Safe Operation and Protection Features

8.3.10.1 LED Temperature Monitoring (Finger-Burn Protection)

The TPS68470 LED temperature monitoring feature is enabled using the ENTMON bit in the WLEDSTAT register. The ENTMON bit must be enabled prior to enabling the WLEDs via the EN bit in the WLEDCTL register. If the WLEDs are enabled first, it is possible that the TSD bit in the WLEDSTAT register will be set keeping the WLED driver from being enabled. Critical temperatures are handled in two stages reflected by two bits in the WLEDSTAT register: LEDWARN provides an early warning to the camera engine, LEDHOT immediately halts the flash operation.

The LED temperature is sensed by measuring the voltage drop of a negative-temperature-coefficient resistor connected between the WLED_NTC and GND pins. An internal current source provides a bias of 24 μ A for the NTC and the WLED_NTC pin voltage is compared to internal thresholds (1.05 V and 0.345 V) to protect the LEDs against overheating.

The LEDWARN and LEDHOT bits reflect the LED temperature. The LEDWARN bit is set when the voltage at the WLED_NTC pin is lower than 1.05 V. This threshold corresponds to an LED warning temperature value; device operation is still permitted. While regulating LED current (i.e., torch light or flash modes), the LEDHOT bit is latched when the voltage at the WLED_NTC pin is lower than 0.345 V. This threshold corresponds to an excessive LED temperature value; device operation is immediately halted and the MODE[1:0] bits are reset.

The LEDWARN and LEDHOT bits will generate an interrupt and also report a status via the WLEDF bit in the GSTAT register unless the WLEDF bit is masked in the INTMASK register. The LEDWARN and LEDHOT bits are cleared by writing a '1' to the WLEDF bit in the GSTAT register provided the EN bit in the WLEDCTL register is set to 'disabled'. Masking the WLEDF bit in the INTMASK register will also clear the WLEDF bit in the GSTAT register.

8.3.10.2 LED Failure Modes (Open/Short Detection) and Overvoltage Protection

The TPS68470 devices incorporate protection features to indicate if the connected LED(s) are failing. These protections cover overvoltage conditions, which are caused by a failing LED showing open circuit behavior, as well as short circuit conditions caused by a failing LED or further reasons causing a short circuit condition. If such failure conditions occur, these are indicated by setting a failure detection flag. The overvoltage protection of ILEDA is disabled to allow setting of the LED current also with a serial resistor. Furthermore, the maximum current drawn from the boost output is limited by the low side WLED drivers.

8.3.10.3 WLED Open Circuit Detection/Over Voltage Protection

If the connected LED(s) fail showing an open circuit behavior or are disconnected, the WLED_OUT output voltage must be limited to prevent the step-up converter from exceeding critical values. An overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. For this protection the TPS68470 output voltage is monitored internally. The TPS68470 device limits WLED_OUT to 6.0 V (typ) and the boost OVP flag is set in the GSTAT register.

8.3.10.4 LED Current Ramp-Up/Down

To achieve smooth LED current waveforms and avoid excessive input voltage drop, the TPS68470 device actively controls the LED current ramp-up / down sequence.

The WLED enable (bit 0 of the VWLEDCTL register) must be set high when enabling the WLED module in order for the RAMP DOWN functionality to be operational. Bit 2 of the WLEDCTL register must also be set to high for a functional RAMP DOWN. If only bit 2 of the WLEDCTL register is set to a high, the RAMP DOWN function will not be operational once disabled by setting bit 2 of the WLEDCTL register to a low state.

In the case of a die temperature shutdown (TSD) or WLED thermal shutdown (LEDHOT), the RAMP DOWN feature is disabled so that the Boost and Flash modules turn off immediately.

Table 3. LED Current Ramp-Up/Down Control vs Operating Mode

| RAMP DIRECTION | FLASH AND FOCUS ASSIST MODE | TORCH AND RED EYE REDUCTION |
|-----------------------|--|--|
| LED CURRENT RAMP-UP | I _{STEP} = 32.5 mA per LED | I _{STEP} = 32.5 mA per LED |
| | T _{STEP} = 12 μs (single LED) T _{STEP} = 24 μs (dual LED) | T _{STEP} = 0.5 μs (single LED) T _{STEP} = 1 μs (dual LED) |
| | Slew-rate = 2.71 mA/μs | Slew-rate = 65 mA/μs |
| LED CURRENT RAMP-DOWN | I _{STEP} = 32.5 mA per LED | I _{STEP} = 32.5 mA per LED |
| | T _{STEP} = 0.5 μs (single LED) T _{STEP} = 1 μs (dual LED) | T _{STEP} = 0.5 μs (single LED) T _{STEP} = 1 μs (dual LED) |
| | Slew-rate = 65 mA/μs | Slew-rate = 65 mA/μs |

8.3.10.5 Short Circuit Protection

The TPS68470 incorporates protection to the LED short by the WLED drivers but cannot protect against a short at WLED_OUT.

If a short circuit condition occurs while the WLED(s) are operated, the low side current sinks DRV_WLED1, DRV_WLED2 limit the maximum output current as programmed for the respective operation mode. If a short circuit condition occurs, the current sinks increase their input resistance to prevent excessive current to be drawn. Furthermore, the WLED Failure flag (WLEDF) is set to indicate the short circuit condition. WLEDF is triggered if the LED forward voltage drops below 1.23 V typically. The second protection is the current limit which generally limits the current drawn from WLED_OUT.

8.3.10.6 Hot Die Detection and Thermal Shutdown

The TPS68470 device offers two levels of die temperature monitoring and protection, which are hot die detection and thermal shutdown functionality. The hot die detector WLED_T[1:0] reflects the instantaneous junction temperature when the Boost is enabled. The hot die detector monitors the junction temperature but does not shut down the device. It provides an early warning to the camera host processor to avoid excessive power dissipation thus preventing from thermal shutdown during the next high-power flash strobe.

As soon as the junction temperature T_J exceeds 160°C typical, the device goes into a global thermal shutdown. In this mode, all LDOs except for LDO_IO are disabled. If the buck converter and the boost are operating based on the PLL clock, they will also be turned off as a result of disabling the LDO_PLL. The ILEDA, ILEDB, HCLK_A and HCLK_B are also turned off. The WLED_T[1:0] bits will be set only if the Boost is enabled and the TSD bit in the VACTL register will be set to indicate an LDO Thermal shutdown has occurred.

The TSD bit in the VACTL register can be cleared by either a hardware reset or a software reset. The TSD bit in the VACTL register will also be cleared if the TSD_FLAG bit in the INTMASK register is changed from 'Not Masked' to 'Masked'.

Table 4. Die Temperature Bits

| WLED_T[1:0] | T_J |
|-------------|---------------------|
| 00 | <55°C |
| 01 | 55°C ≤ T_J ≤ 70°C |
| 11 | >70°C |
| 10 | Illegal state |

8.3.11 WLED Boost Inductor Selection

A boost converter requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. The TPS68470 device integrates a current limit protection circuitry. The peak current of the low-side NMOS switch is sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit (2000 mA ... 5000 mA) is user selectable via the I²C interface.

In order to optimize solution size the TPS68470 device has been designed to operate with inductance values between a minimum of 1.3 µH and maximum of 2.9 µH. In typical high-current white LED applications a 2.2-µH inductance is recommended.

To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the power switch depends on the output load, the input and output voltages. Estimation of the maximum average inductor current and the maximum inductor peak current can be done using [Equation 1](#) and [Equation 2](#):

$$I_L \sim I_{OUT} = \frac{V_{WLED_OUT}}{n \times V_{3V3_VDD}} \quad (1)$$

$$I_{L(PEAK)} = \frac{V_{3V3_VDD} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1-D) \times n} \quad \text{with } D = \frac{V_{WLED_OUT} - V_{3V3_VDD}}{V_{WLED_OUT}} \quad (2)$$

where:

f = switching frequency

L = inductance value

n = estimated efficiency

The losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

8.3.12 I²C Bus Operation

The I²C Bus is a communications link between a master and a series of slave pins. The link is established using a two-wired bus consisting of a Serial Clock signal (SCL) and a Serial Data signal (SDA). The serial clock is sourced by the master. The serial data line is bi-directional for data communication between the master and the slave pins. Each device has an open drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

The TPS68470 hosts a slave I²C interface that is compliant to the 3.0 I²C standard. The TPS68470 supports data rates up to 400 kbit/s and auto-increment addressing.

The TPS68470 supports four different read and two different write operations; single read from a defined location, single read from a current location, sequential read starting from a defined location, sequential read from current location, single write to a defined location, sequential write starting from a defined location.

All of the supported read and write operations are described in the following sections.

8.3.12.1 Single Write to a Defined Location

Figure 8 shows the format of a single write to a defined location. First, the master issues a start condition, followed by a seven-bit I²C address. Next, the master writes a zero to signify that it wishes to conduct a write operation. Upon receiving an acknowledge from the slave, the master writes the eight-bit register number across the bus. Following a second acknowledge, the TPS68470 sets the I²C register to a defined value and the master writes the eight-bit data value across the bus. Upon receiving a third acknowledge, the TPS68470 auto increments the internal I²C register number by one and the master issues a stop condition. This action concludes the register write.

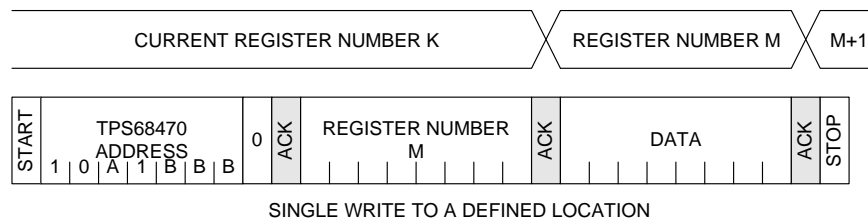


Figure 8. Single Write to a Defined Location

8.3.12.2 Single Read From a Defined Location and Current Location

Figure 9 shows the format of a single read from a defined location. First, the master issues a start condition followed by a seven-bit I²C address. Next, the master writes a zero to signify that it conducts a write operation. Upon receiving an acknowledge from the slave, the master writes the eight-bit register number across the bus. Following a second acknowledge, the TPS68470 sets the internal I²C register number to a defined value. Then the master issues a repeat start condition and a seven-bit I²C address followed by a one to signify that it conducts a read operation. Upon receiving a third acknowledge, the master releases the bus to the TPS68470. The TPS68470 then writes the eight-bit data value from the register across the bus. The master acknowledges receiving this byte and issues a stop condition. This action concludes the register read.

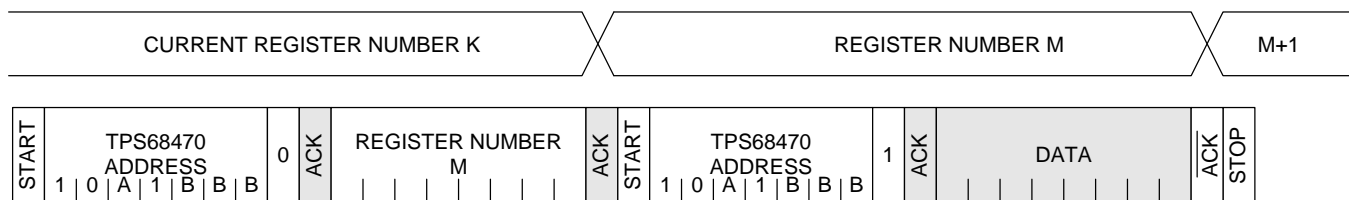


Figure 9. Single Read From a Defined Location

Shown in Figure 10 is the single read from the current location. If the read command is issued without defining the register number first, the TPS68470 writes out the data from the current register from the device memory.

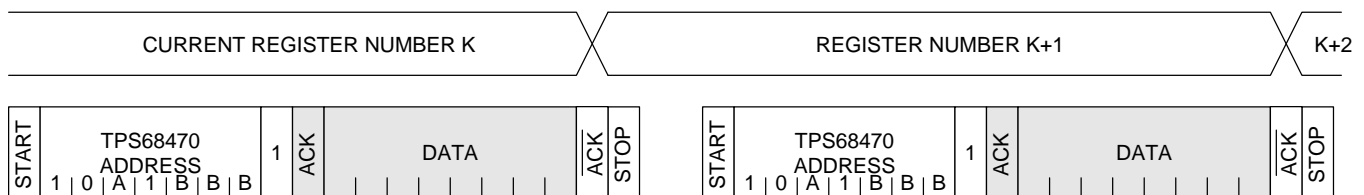


Figure 10. Single Read From the Current Location

8.3.12.3 Sequential Read and Write

Sequential read and write allows simple and fast access to the TPS68470 registers. Figure 11 shows a sequential read from a defined location. If the master does not issue a stop condition after providing the ACK, the TPS68470 auto increments the register number and writes the data from the next register.

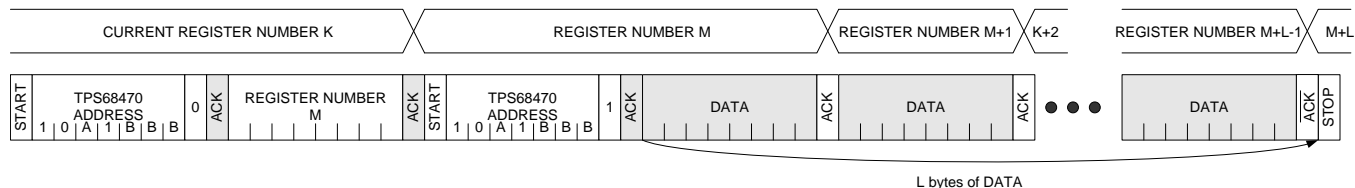


Figure 11. Sequential Read from a Defined Location

Figure 12 shows a sequential write. If the I²C master does not provide a stop condition after the TPS68470 has issued an ACK, the TPS68470 will auto increment its address register by 1 so that the master can write to the next register.

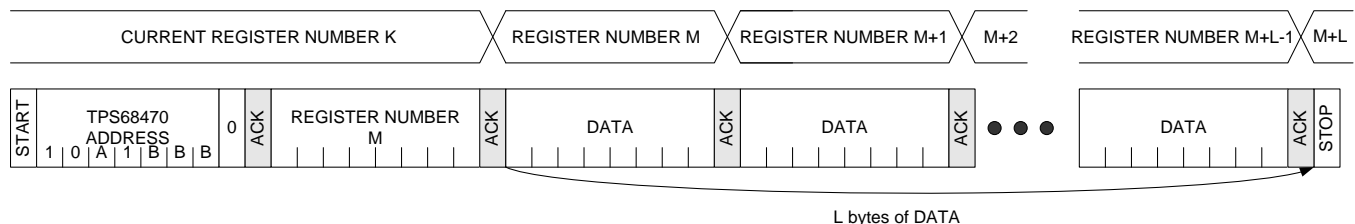


Figure 12. Sequential Write

If a read is started without writing the register value first, the TPS68470 writes out data from the current location. If the master does not issue a STOP condition after ACK, the TPS68470 auto increments the I²C register and writes out the data. This continues until the master issues a STOP condition. This is shown in Figure 13.

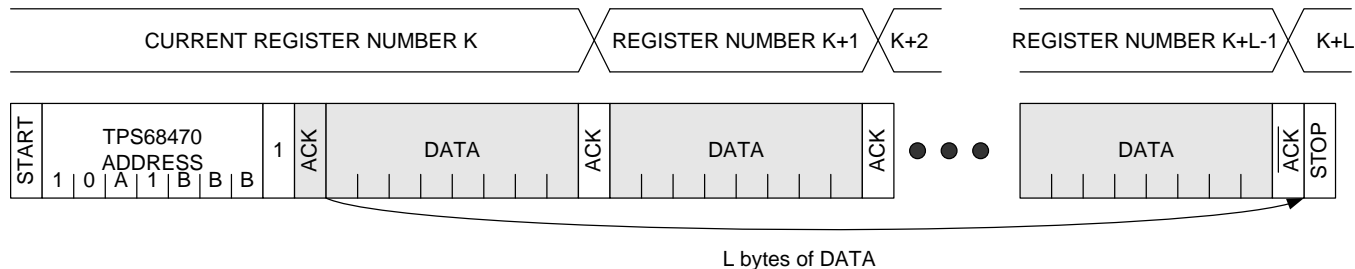


Figure 13. Sequential Read Starting From a Current Location

8.3.13 Subaddress Definition

The address bits used in the slave address portion of the I²C transaction are defined by the device pins I2C_ICA and I2C_ICB. The I2C_ICA and I2C_ICB pins can be tied to either GND, VDD (LDO_IO), SDA, or SCL. Figure 14 shows the derivation of the I²C sub address based on the I2C_ICA and I2C_ICB connections. Table 5 shows the values of the address bits for all combinations of I2C_ICA and I2C_ICB.

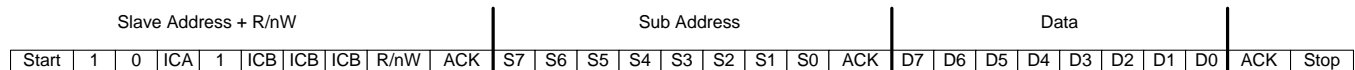


Figure 14. Sub Address in I²C Transmission

Start – Start Condition

ACK – Acknowledge

ICA, ICB – Device Address: Device address is selectable via I2C_ICA and I2C_ICB input pin.

S(7:0) – Sub address: defined per register map.

R/nW – Read / not Write Select Bit

D(7:0) – Data; Data to be loaded into the device

Stop – Stop Condition

Table 5. ICA and ICB(2:0) Sub Address Bits with Different I2C_ICA and I2C_ICB Pin Configurations

| I2C_ICA and I2C_ICB PIN CONNECTIONS | | ICA | ICB(2:0) | WRITE ADDRESS | READ ADDRESS |
|-------------------------------------|---------|-----|----------|---------------|--------------|
| I2C_ICA | I2C_ICB | | | | |
| VDD | VDD | 0 | 000 | 0x90 | 0x91 |
| VDD | GND | 0 | 001 | 0x92 | 0x93 |
| VDD | SDA | 0 | 010 | 0x94 | 0x95 |
| VDD | SCL | 0 | 011 | 0x96 | 0x97 |
| GND | VDD | 0 | 100 | 0x98 | 0x99 |
| GND | GND | 0 | 101 | 0x9A | 0x9B |
| GND | SDA | 0 | 110 | 0x9C | 0x9D |
| GND | SCL | 0 | 111 | 0x9E | 0x9F |
| SDA | VDD | 1 | 000 | 0xB0 | 0xB1 |
| SDA | GND | 1 | 001 | 0xB2 | 0xB3 |
| SDA | SDA | 1 | 010 | 0xB4 | 0xB5 |
| SDA | SCL | 1 | 011 | 0xB6 | 0xB7 |
| SCL | VDD | 1 | 100 | 0xB8 | 0xB9 |
| SCL | GND | 1 | 101 | 0xBA | 0xBB |
| SCL | SDA | 1 | 110 | 0xBC | 0xBD |
| SCL | SCL | 1 | 111 | 0xBE | 0xBF |

8.3.13.1 I²C Device Address, Start and Stop Condition

Data transmission is initiated with a start bit from the master as shown in Figure 15. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. SDA data is latched by the TPS68470 on the rising edge of the SCL line. If the appropriate device address bits are set for the device, the TPS68470 issues the ACK by pulling the SDA line low on the next falling edge after 8th bit is latched. SDA is kept low until the next falling edge of the SCL line.

Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. (See Figure 16.)

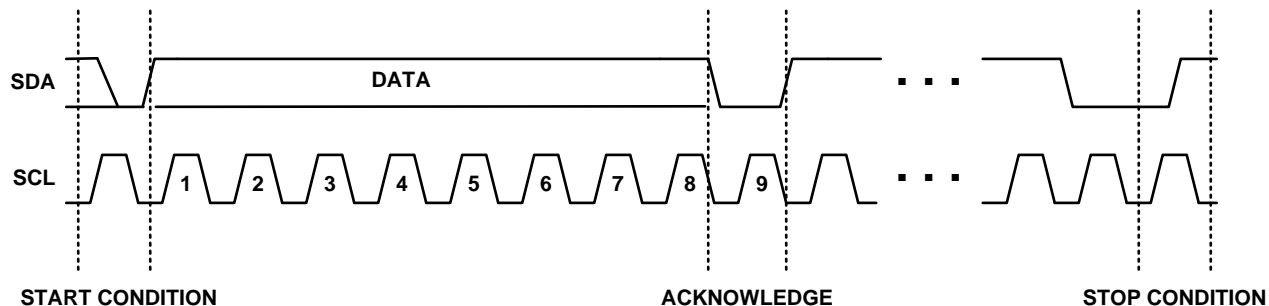


Figure 15. I²C Start / Stop / Acknowledge Protocol

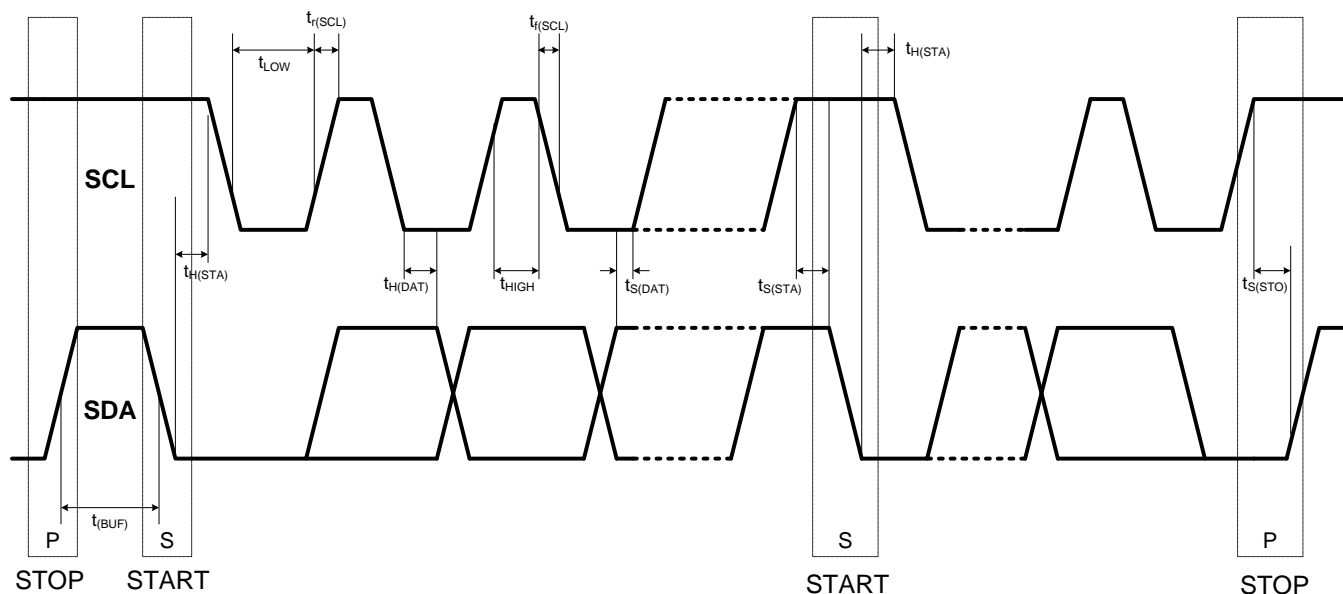


Figure 16. I²C Data Transmission Timing

8.4 Device Functional Modes

8.4.1 Operation with a Single Input Power Rail

The TPS68470 was designed such that both the 3V3_SUS and 3V3_VDD pins can be sourced from the same supply. However, if both pins are connected together, the device will never enter the 'Sleep' mode.

8.4.2 Sequencing the Input Power Rails

If the input power rails have to be sequenced, the recommendation is to turn on the power to the 3V3_SUS pin first and then to the 3V3_VDD pin. On power down, the recommendation is to remove power from the 3V3_VDD pin first.

8.5 Register Map

| REGISTER ADDRESS | REGISTER NAME | REGISTER GROUP | FUNCTION |
|------------------|---------------|----------------|---|
| 0x00 | RESERVED | - | Reserved |
| 0x01 | GSTAT | Status | Global status |
| 0x02 | VRSTAT | Status | VR status |
| 0x03 | VRSHORT | Status | VR short status |
| 0x04 | INTMASK | Configuration | Interrupt mask |
| 0x05 | VCOSPEED | Configuration | PLL VCO speed control |
| 0x06 | POSTDIV2 | Configuration | HCLK_B PLL output divider |
| 0x07 | BOOSTDIV | Configuration | PLL output divider for boost clock |
| 0x08 | BUCKDIV | Configuration | PLL output divider for buck clock |
| 0x09 | PLL_SWR | Configuration | PLL lock timer controls |
| 0x0A | XTALDIV | Configuration | PLL reference divider for sensor |
| 0x0B | PLLDIV | Configuration | PLL feedback divider |
| 0x0C | POSTDIV | Configuration | HCLK_A PLL output divider |
| 0x0D | PLLCTL | Configuration | PLL control |
| 0x0E | PLLCTL2 | Configuration | Spread spectrum PLL control |
| 0x0F | CLKCFG1 | Configuration | HCLK_A and HCLK_B configuration |
| 0x10 | CLKCFG2 | Configuration | HCLK_A and HCLK_B drive strengths |
| 0x11 - 0x13 | RESERVED | - | Reserved |
| 0x14 | GPCTL0A | GPIO | GPIO 0 control |
| 0x15 | GPCTL0B | GPIO | GPIO 0 control |
| 0x16 | GPCTL1A | GPIO | GPIO 1 control |
| 0x17 | GPCTL1B | GPIO | GPIO 1 control |
| 0x18 | GPCTL2A | GPIO | GPIO 2 control |
| 0x19 | GPCTL2B | GPIO | GPIO 2 control |
| 0x1A | GPCTL3A | GPIO | GPIO 3 control |
| 0x1B | GPCTL3B | GPIO | GPIO 3 control |
| 0x1C | GPCTL4A | GPIO | GPIO 4 control |
| 0x1D | GPCTL4B | GPIO | GPIO 4 control |
| 0x1E | GPCTL5A | GPIO | GPIO 5 control |
| 0x1F | GPCTL5B | GPIO | GPIO 5 control |
| 0x20 | GPCTL6A | GPIO | GPIO 6 control |
| 0x21 | GPCTL6B | GPIO | GPIO 6 control |
| 0x22 | SGPO | GPIO | Sensor general purpose output |
| 0x23 | PITCTL | Configuration | Programmable interrupt trigger control |
| 0x24 | WAKECFG | Configuration | Wake and interrupt output configuration |
| 0x25 | IOWAKESTAT | Status | GPIO interrupt status |
| 0x26 | GPDI | GPIO | GPIO Data in |
| 0x27 | GPDO | GPIO | GPIO Data out |
| 0x28 | ILEDCTL | GPIO | ILED output control |
| 0x29 | WLEDSTAT | WLED | White LED status |
| 0x2A | VWLEDILIM | WLED | WLED coil current limit setting |
| 0x2B | VWLEDVAL | WLED | WLED voltage adjustment |
| 0x2C | WLEDMAXRER | WLED | White LED max current in red-eye-reduction mode |
| 0x2D | WLEDMAXT | WLED | White LED max current in torch/video light mode |
| 0x2E | WLEDMAXAF | WLED | White LED max current in autofocus mode |
| 0x2F | WLEDMAXF | WLED | White LED max current in flash mode |

Register Map (continued)

| REGISTER ADDRESS | REGISTER NAME | REGISTER GROUP | FUNCTION |
|------------------|---------------|----------------|---|
| 0x30 | WLEDTO | WLED | Flash LED timeout configuration |
| 0x31 | VWLEDCTL | WLED | WLED VR control |
| 0x32 | WLEDTMR_MSB | WLED | Flash pulse duration MSB |
| 0x33 | WLEDTMR_LSB | WLED | Flash pulse duration LSB |
| 0x34 | WLEDC1 | WLED | Flash LED 1 current setting |
| 0x35 | WLEDC2 | WLED | Flash LED 2 current setting |
| 0x36 | WLEDCTL | WLED | White LED control |
| 0x37 - 0x3B | RESERVED | - | Reserved |
| 0x3C | VCMVAL | Regulator | VCM voltage adjustment |
| 0x3D | VAUX1VAL | Regulator | AUX1 voltage adjustment |
| 0x3E | VAUX2VAL | Regulator | AUX2 voltage adjustment |
| 0x3F | VIOVAL | Regulator | IO voltage adjustment |
| 0x40 | VSIOVAL | Regulator | S_IO voltage adjustment |
| 0x41 | VAVAL | Regulator | ANA voltage adjustment |
| 0x42 | VDVAL | Regulator | CORE voltage adjustment |
| 0x43 | S_I2C_CTL | Control | Sensor I ² C interface control |
| 0x44 | VCMCTL | Regulator | VCM VR control |
| 0x45 | VAUX1CTL | Regulator | AUX1 VR control |
| 0x46 | VAUX2CTL | Regulator | AUX2 VR control |
| 0x47 | VACTL | Regulator | ANA VR control |
| 0x48 | VDCTL | Regulator | CORE VR control |
| 0x49 - 0x4F | RESERVED | - | Reserved |
| 0x50 | RESET | Control | Soft reset |
| 0x51 - 0x7F | RESERVED | - | Reserved |
| 0x80 - 0xEF | RESERVED | - | Reserved |
| 0xFF | REVID | ID | Silicon Revision Identification |

8.5.1 GSTAT Register (address = 0x01) [reset = 00000000]

Figure 17. GSTAT Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----------|-------|-------|-------|-------|----------|------|
| Field Name | SHORT_FLAG | PWR_FLAG | ILEDf | WLEDf | OVP | UVLO | TSD_FLAG | WAKE |
| Read/Write | R/W1C | R/W1C | R/W1C | R/W1C | R/W1C | R/W1C | R/W1C | R |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only; R/W1C = Read/Write 1 to Clear

Table 6. GSTAT Register Description

| Bit | Field | Type | Reset | Description |
|-------|-------------------------|-------|-------|---|
| Bit 0 | WAKE | R | 0 | Status of Wake Event external interrupt if GPIO inputs are configured in the IOWAKESTAT[6:0] as active 0: Not detected 1: Wake Event detected |
| Bit 1 | TSD_FLAG ⁽¹⁾ | R/W | 0 | Status of Max Die Temperature interrupt for WLED Boost converter (VWLEDCTL[1]), Core Buck converter (VDCTL[3]) or all LDOs (VACTL[1]) 0: Not detected 1: Max Die Temperature exceeded |
| Bit 2 | 3V3_VDD_UVLO | R/W | 0 | Status of 3V3_VDD undervoltage lockout (UVLO) interrupt 0: Not detected 1: UVLO detected |
| Bit 3 | OVP | R/W | 0 | Status of WLED Boost converter (WLED_OUT) over voltage protection interrupt 0: Not detected 1: Overvoltage detected |
| Bit 4 | WLEDf ⁽²⁾ | R/W | 0 | Status of the WLED interrupt defined by the WLEDSTAT [5,4,2 and 1] register bits (LEDf, TO, LEDHOT and LEDWARN) 0: Not detected 1: LEDf, TO, LEDHOT and/or LEDWARN detected |
| Bit 5 | ILEDf | R/W | 0 | Status of ILEDB or ILEDA interrupt defined by the ILEDCTL[7,3] register bits 0: Not detected 1: ILEDA and/or ILEDB failure detected |
| Bit 6 | PWR_FLAG | R/W | 0 | Status of any Voltage Regulator (VR) power good output defined by the VRSTAT[7:0] and PLLCTL[2] register bits 0: Not detected 1: A transition of 'not detected' to 'detected' has occurred on at least one of the VRs |
| Bit 7 | SHORT_FLAG | R/W1C | 0 | Status of any Voltage Regulator (VR) short circuit detection defined by the VRSHORT[7:0] and PLLCTL[3] register bits 0: Not detected 1: A short circuit has been detected |

(1) If the TSD_FLAG is masked in the INTMASK register, the device will not protect itself with the Thermal Shutdown and the TSD_FLAG bit in the GSTAT register will not indicate a Max Die Temperature. status

(2) The WLEDf bit can only be reset if the Boost and WLED driver control bit (bit D1 - EN) in the WLEDCTL register is disabled.

8.5.2 VRSTAT Register (address = 0x02) [reset = –]

Figure 18. VRSTAT Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|-----------|-----------|-----------|-----------|----------|---------|----------|
| Field Name | AUX2_GOOD | AUX1_GOOD | WLED_GOOD | S_IO_GOOD | CORE_GOOD | ANA_GOOD | IO_GOOD | VCM_GOOD |
| Read/Write | R | R | R | R | R | R | R | R |
| Reset Value | - | - | - | - | - | - | - | - |

LEGEND: R = Read only

Table 7. VRSTAT Register Description

| Bit | Field | Type | Reset | Description |
|-------|-----------|------|-------|---|
| Bit 0 | VCM_GOOD | R | – | Status of VCM_OUT voltage rail 0: Output below power good threshold 1: Output above power good threshold |
| Bit 1 | IO_GOOD | R | – | Status of IO_OUT voltage rail 0: Output below power good threshold 1: Output above power good threshold |
| Bit 2 | ANA_GOOD | R | – | Status of ANA_OUT voltage rail 0: Output below power good threshold 1: Output above power good threshold |
| Bit 3 | CORE_GOOD | R | – | Status of CORE_OUT voltage rail 0: Output below power good threshold 1: Output above power good threshold |
| Bit 4 | S_IO_GOOD | R | – | Status of S_IO_OUT voltage rail 0: Output below power good threshold 1: Output above power good threshold |
| Bit 5 | WLED_GOOD | R | – | Status of WLED_OUT voltage rail 0: Output below power good threshold 1: Output above power good threshold |
| Bit 6 | AUX1_GOOD | R | – | Status of AUX1_OUT voltage rail 0: Output below power good threshold 1: Output above power good threshold |
| Bit 7 | AUX2_GOOD | R | – | Status of AUX2_OUT voltage rail 0: Output below power good threshold 1: Output above power good threshold |

8.5.3 VRSHORT Register (address = 0x03) [reset = 00000000]

Figure 19. VRSHORT Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------|------|------|------|------|-----|----|-----|
| Field Name | AUX2 | AUX1 | RSVD | S_IO | CORE | ANA | IO | VCM |
| Read/Write | R | R | R | R | R | R | R | R |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R = Read only

Table 8. VRSHORT Register Description

| Bit | Field | Type | Reset | Description |
|-------|-------|------|-------|---|
| Bit 0 | VCM | R | 0 | Status of the VCM_OUT voltage rail 0: No short 1: Short (output below 0.5 V) |
| Bit 1 | IO | R | 0 | Status of the IO_OUT voltage rail 0: No short 1: Short (output below 0.5 V) |
| Bit 2 | ANA | R | 0 | Status of the ANA_OUT voltage rail 0: No short 1: Short (output below 0.5 V) |
| Bit 3 | CORE | R | 0 | Status of the CORE_OUT voltage rail 0: No short 1: Short (output below 0.5 V) |
| Bit 4 | S_IO | R | 0 | Status of the S_IO_OUT voltage rail 0: No short 1: Short (output below 0.5 V) |
| Bit 5 | RSVD | R | 0 | Reserved |
| Bit 6 | AUX1 | R | 0 | Status of the AUX1_OUT voltage rail 0: No short 1: Short (output below 0.5V) |
| Bit 7 | AUX2 | R | 0 | Status of the AUX2_OUT voltage rail 0: No short 1: Short (output below 0.5 V) |

8.5.4 INTMASK Register (address = 0x04) [reset = 00000000]

Figure 20. INTMASK Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|----------|--------|--------|-----|------|----------|--------------|
| Field Name | SHORT_FLAG | PWR_FLAG | ILEDIF | WLEDIF | OVP | RSVD | TSD_FLAG | 3V3_VDD_UVLO |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write

Table 9. INTMASK Register Description

| Bit | Field | Type | Reset | Description |
|-------|--------------|------|-------|--|
| Bit 0 | 3V3_VDD_UVLO | R/W | 0 | 3V3_VDD UVLO interrupt mask 0: Not Masked 1: Masked |
| Bit 1 | TSD_FLAG | R/W | 0 | Max Die Temperature interrupt mask for WLED Boost converter (VWLEDCTL[1]), Core Buck converter (VDCTL[3]) or LDOs (VACTL[1]) 0: Not Masked 1: Masked |
| Bit 2 | RSVD | R/W | 0 | Reserved Bit - Do not set to '1' 0: Default Setting |
| Bit 3 | OVP | R/W | 0 | WLED Boost converter (WLED_OUT) over voltage protection interrupt mask 0: Not Masked 1: Masked |
| Bit 4 | WLEDIF | R/W | 0 | WLED interrupt mask defined by the WLEDSTAT [5,4,2, and 1] register bits (LEDIF, TO, LEDHOT and LEDWARN) 0: Not Masked 1: Masked |
| Bit 5 | ILEDIF | R/W | 0 | ILEDIF or ILEDA interrupt mask defined by the ILEDCTL[7,3] register bits 0: Not Masked 1: Masked |
| Bit 6 | PWR_FLAG | R/W | 0 | Voltage Regulator (VR) power good output interrupt mask defined by the VRSTAT[7:0] and PLLCTL[2] register bits 0: Not Masked 1: Masked |
| Bit 7 | SHORT_FLAG | R/W | 0 | Voltage Regulator (VR) short circuit detection interrupt mask defined by the VRSHORT[7:0] and PLLCTL[3] register bits 0: Not Masked 1: Masked |

8.5.5 VCOSPEED Register (address = 0x05) [reset = 00000000]

Figure 21. VCOSPEED Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|-----|------------|-----|-----|
| Field Name | Not used | Not used | Not used | Not used | OVR | SPEED[2:0] | | |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 10. VCOSPEED Register Description

| Bit | Field | Type | Reset | Description |
|------------|------------|------|-------|---|
| Bits [2:0] | SPEED[2:0] | R/W | 000 | VCO gain setting, normally defined by the value of the PLLDIV register 000: 50 MHz/V 001: 56 MHz/V 010: 63 MHz/V 011: 73 MHz/V 100: 78 MHz/V 101: 87 MHz/V 110: 96 MHz/V 111: 105 MHz/V |
| Bit 3 | OVR | R/W | 0 | Override the internal, PLLDIV setting which is dependent on the VCO gain setting (MHz/V) (sets the gain to the approximate value stored in the SPEED[2:0] register bits) 0: Do not override 1: Override |
| Bits [7:4] | Not used | R | 0000 | |

8.5.6 POSTDIV2 Register (address = 0x06) [reset = 00000000]

Figure 22. POSTDIV2 Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|----------|---------------|-----|
| Field Name | Not used | Not used | Not used | Not used | Not used | Not used | POSTDIV2[1:0] | |
| Read/Write | R | R | R | R | R | R | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 11. POSTDIV2 Register Description

| Bit | Field | Type | Reset | Description |
|------------|---------------|------|--------|---|
| Bits [1:0] | POSTDIV2[1:0] | R/W | 00 | PLL output divider for HCLK_B Divider = POSTDIV FACTOR = $2^{\text{POSTDIV2[1:0]}}$ HCLK_B Desired Frequency = PLL_VCO_CLK / POSTDIV FACTOR 00: POSTDIV FACTOR = $2^0 = 1$ 01: POSTDIV FACTOR = $2^1 = 2$ 10: POSTDIV FACTOR = $2^2 = 4$ 11: POSTDIV FACTOR = $2^3 = 8$ |
| Bits [7:2] | Not used | R | 000000 | |

8.5.7 BOOSTDIV Register (address = 0x07) [reset = 00000000]

Figure 23. BOOSTDIV Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|---------------|-----|-----|-----|-----|
| Field Name | Not used | Not used | Not used | BOOSTDIV[4:0] | | | | |
| Read/Write | R | R | R | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 12. BOOSTDIV Register Description

| Bit | Field | Type | Reset | Description |
|------------|------------------------------|------|-------|--|
| Bits [4:0] | BOOSTDIV[4:0] ⁽¹⁾ | R/W | 00000 | PLL output divider for boost clock Divider = BOOSTDIV[4:0] + 16 BOOST = PLL_VCO_CLK / (BOOSTDIV[4:0] + 16) |
| Bits [7:5] | Not used | R | 000 | |

(1) As a default, select BOOSTDIV[4:0] to achieve BOOST = 2 MHz as closely as possible.

8.5.8 BUCKDIV Register (address = 0x08) [reset = 00000000]

Figure 24. BUCKDIV Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|--------------|-----|-----|-----|
| Field Name | Not used | Not used | Not used | Not used | BUCKDIV[3:0] | | | |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 13. BUCKDIV Register Description

| Bit | Field | Type | Reset | Description |
|------------|-----------------------------|------|-------|--|
| Bits [3:0] | BUCKDIV[3:0] ⁽¹⁾ | R/W | 0000 | PLL output divider for buck clock Divider = BUCKDIV[3:0] + 5 BUCK = PLL_VCO_CLK / (BUCKDIV[3:0] + 5) |
| Bits [7:4] | Not used | R | 0000 | |

(1) As a default, select BUCKDIV[3:0] to achieve BUCK = 5.2 MHz as closely as possible.

8.5.9 PLLSWR Register (address = 0x09) [reset = 00000000]

Figure 25. PLLSWR Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------|------|------|--------|------|------|----------|-----|
| Field Name | RSVD | RSVD | RSVD | SWR_SS | RSVD | RSVD | SWR[1:0] | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write

Table 14. PLLSWR Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|-------|--|
| Bits [1:0] | SWR[1:0] | R/W | 00 | LOCK timer setting for the PLL sets the number of PLL_REF_CLK cycles where $PLL_REF_CLK = F_{Input\ Clock} / (XTALDIV[7:0] + 30) = 100\text{ KHz}$: $LOCK\ time = ((2^{SWR[1:0]}) * 50) / (PLL_REF_CLK) + \text{settling time}$ Example for an SWR[1:0]='11' = 3 setting: $(2^3) * 50 = 400$ divided by 100 KHz (the LOCK time for $F_{Input\ Clock} = 24\text{MHz}$ and $XTALDIV[7:0] + 30 = 240$) results in a 4-ms LOCK time. 00: Reserved 01: Reserved 10: 2 ms 11: 4 ms |
| Bits [3:2] | RSVD | R/W | 00 | |
| Bit 4 | SWR_SS | R/W | 0 | LOCK timer setting for SS PLL sets the number of PLL REFCLK ($= f_{XCLK} / XTALDIV$) cycles: 0: 58 * PLL_SS_REFCLK cycles 1: 78 * PLL_SS_REFCLK cycles |
| Bits [7:5] | RSVD | R/W | 000 | |

8.5.10 XTALDIV Register (address = 0x0A) [reset = 00000000]

Figure 26. XTALDIV Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|-----|-----|-----|-----|-----|-----|-----|
| Field Name | XTALDIV[7:0] | | | | | | | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write

Table 15. XTALDIV Register Description

| Bit | Field | Type | Reset | Description |
|------------|-----------------------------|------|----------|---|
| Bits [7:0] | XTALDIV[7:0] ⁽¹⁾ | R/W | 00000000 | Reference crystal divider $Divider = (XTALDIV[7:0] + 30)$ $PLL_REF_CLK = 100\text{ KHz} = F_{Input\ Clock} / (XTALDIV[7:0] + 30)$ |

(1) The intent is to divide the input clock (crystal or external clock) down to PLL_REF_CLK=100kHz as precisely as possible.

8.5.11 PLLDIV Register (address = 0x0B) [reset = 00000000]

Figure 27. PLLDIV Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Field Name | PLLDIV[8:1] | | | | | | | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write

Table 16. PLLDIV Register Description

| Bit | Field | Type | Reset | Description |
|------------|-------------------------------|------|----------|---|
| Bits [7:0] | PLLDIV[8:1] ⁽¹⁾⁽²⁾ | R/W | 00000000 | PLL feedback divider, 8 highest bits, LSB in POSTDIV Divider = (PLLDIV[8:0] + 320) PLL_REF_CLK = PLL_VCO_CLK / (PLLDIV[8:0] + 320) The PLLDIV[8:0] result will require the LSB to be stored in the PLLDIV[0] location and the upper 8 bits to be stored in the PLLDIV[8:1] location. |

(1) The intent is to divide PLL_VCO_CLK down to PLL_REF_CLK=100 KHz as precisely as possible.

(2) The PLL_REF_CLK value should match the frequency value obtained from XTALDIV.

8.5.12 POSTDIV Register (address = 0x0C) [reset = 00000000]

Figure 28. POSTDIV Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-----------|----------|----------|----------|----------|----------|--------------|-----|
| Field Name | PLLDIV[0] | Not used | Not used | Not used | Not used | Not used | POSTDIV[1:0] | |
| Read/Write | R/W | R | R | R | R | R | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 17. POSTDIV Register Description

| Bit | Field | Type | Reset | Description |
|------------|--------------|------|-------|--|
| Bits [1:0] | POSTDIV[1:0] | R/W | 00 | PLL output divider for HCLK_A Divider = POSTDIV FACTOR = 2 ^{POSTDIV[1:0]} HCLK_A Desired Frequency = PLL_VCO_CLK / POSTDIV FACTOR 00: POSTDIV FACTOR = 2 ⁰ = 1 01: POSTDIV FACTOR = 2 ¹ = 2 10: POSTDIV FACTOR = 2 ² = 4 11: POSTDIV FACTOR = 2 ³ = 8 |
| Bits [6:2] | Not used | R | 00000 | |
| Bit 7 | PLLDIV[0] | R/W | 0 | LSB for PLL feedback divider (See PLLDIV Register at address 0x0B) |

8.5.13 PLLCTL Register (address = 0x0D) [reset = 10000000]

Figure 29. PLLCTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|-----------------|-----|-----|-----------|-----------|------|--------|
| Field Name | DIS_EXTCLK | CON_XTAL_C[2:0] | | | SHORT_LDO | VGOOD_LDO | LOCK | EN_PLL |
| Read/Write | R/W | R/W | R/W | R/W | R | R/W1C | R | R/W |
| Reset Value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only; R/W1C = Read/Write 1 to Clear

Table 18. PLLCTL Register Description

| Bit | Field | Type | Reset | Description |
|------------|-----------------|------|-------|---|
| Bit 0 | EN_PLL | R/W | 0 | PLL Enable Control 0: Disable PLL 1: Enable PLL |
| Bit 1 | LOCK | R | 0 | PLL Lock Control status 0: PLL Lock timer has not expired 1: PLL Lock timer has expired |
| Bit 2 | VGOOD_LDO | R/W | 0 | PLL LDO output status 0: PLL LDO is below power good threshold 1: PLL LDO is above power good threshold |
| Bit 3 | SHORT_LDO | R | 0 | PLL LDO short status 0: PLL output is not shorted 1: PLL output is shorted |
| Bits [6:4] | CON_XTAL_C[2:0] | R/W | 000 | Crystal oscillator amp input capacitance control. OSC_IN and OSC_OUT pins have a fixed 7 pF of capacitance. Additional capacitance is added based on the CON_XTAL_C[2:0] register bit settings 000 : 0 pF 001 : 2 pF 010 : 4 pF 011 : 6 pF 100 : 8 pF 101 : 10 pF 110 : 12 pF 111 : 14 pF |
| Bit 7 | DIS_EXTCLK | R/W | 1 | Clock source control 0: External CLK source comes from GPIO3 1: XTAL oscillator enabled as clock source |

8.5.14 PLLCTL2 Register (address = 0x0E) [reset = 00000000]

Figure 30. PLLCTL2 Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|---------|---------------|-----|-------|----------|----------|------|-----------|
| Field Name | SS_FREQ | SS_DEPTH[1:0] | | SS_EN | Not used | Not used | LOCK | EN_PLL_SS |
| Read/Write | R/W | R/W | R/W | R/W | R | R | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 19. PLLCTL2 Register Description

| Bit | Field | Type | Reset | Description |
|------------|---------------|------|-------|--|
| Bit 0 | EN_PLL_SS | R/W | 0 | PLL_SS Enable Control 0: Disable PLL_SS 1: Enable PLL_SS |
| Bit 1 | LOCK | R | 0 | PLL_SS Lock Control status 0: PLL_SS Lock timer has not expired 1: PLL_SS Lock timer has expired |
| Bits [3:2] | Not used | R | 00 | |
| Bit 4 | SS_EN | R/W | 0 | Spread Spectrum Modulation Control 0: Disable spread spectrum modulation 1: Enable spread spectrum modulation |
| Bits [6:5] | SS_DEPTH[1:0] | R/W | 00 | Modulation depth at $f_{VCO} = 32 \text{ MHz}$ 00: 0.75% 01: 1.2% 10: 1.5% 11 : 2% Modulation depth at $f_{VCO}=64\text{MHz}$ 00 : 0.64% 01 : 0.9% 10 : 1.15% 11 : 1.5% |
| Bit 7 | SS_FREQ | R/W | 0 | Modulation frequency 0: 30 kHz 1: 15 kHz |

8.5.15 CLKCFG1 Register (address = 0x0F) [reset = 00000000]

Figure 31. CLKCFG1 Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|-------------|-----|-------------|-----|
| Field Name | Not used | Not used | Not used | Not used | MODE_B[1:0] | | MODE_A[1:0] | |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 20. CLKCFG1 Register Description

| Bit | Field | Type | Reset | Description |
|------------|-------------|------|-------|---|
| Bits [1:0] | MODE_A[1:0] | R/W | 00 | Output selection for HCLK_A 00: Output disabled 01: Buffered version of the crystal oscillator input 10: PLL output ⁽¹⁾ 11: PLL output with SS modulation ⁽¹⁾ |
| Bits [3:2] | MODE_B[1:0] | R/W | 00 | Output selection for HCLK_B 00: Output disabled 01: Buffered version of the crystal oscillator input 10: PLL output ⁽¹⁾ 11: PLL output with SS modulation ⁽¹⁾ |
| Bits [7:4] | Not used | R | 0000 | |

(1) The HCLK_A and HCLK_B outputs are gated by the Lock signal in the PLLCTL register.

8.5.16 CLKCFG2 Register (address = 0x10) [reset = 00000000]

Figure 32. CLKCFG2 Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------------|-----|----------------|-----|
| Field Name | Not used | Not used | Not used | Not used | DRV_STR_B[1:0] | | DRV_STR_A[1:0] | |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 21. CLKCFG2 Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------------|------|-------|---|
| Bits [1:0] | DRV_STR_A[1:0] | R/W | 00 | HCLK_A drive strength value 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |
| Bits [3:2] | DRV_STR_B[1:0] | R/W | 00 | HCLK_B drive strength value 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |
| Bits [7:4] | Not used | R | 0000 | |

8.5.17 GPCTL0A Register (address = 0x14) [reset = 00000001]

Figure 33. GPCTL0A Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|-----|----------|----------|-------|-------|----------------|-----|
| Field Name | DRV_STR[1:0] | | Not used | Not used | LEVEL | DMODE | MODE_CTRL[1:0] | |
| Read/Write | R/W | R/W | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

LEGEND: R/W = Read/Write; R = Read only

Table 22. GPCTL0A Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------------|------|-------|---|
| Bits [1:0] | MODE_CTRL[1:0] | R/W | 01 | GPIO0 operation mode: 00: GPIO input 01: GPIO input, pull-up 10: GPIO output, CMOS (push-pull) 11: GPIO output, open-drain pull-down |
| Bit 2 | DMODE | R/W | 0 | GPIO0 drive mode when configured as an output (CMOS or open-drain) via the MODE_CTRL[1:0] bits: 0: Voltage mode (only CMOS is supported) 1: Current mode (only open-drain is supported) |
| Bit 3 | LEVEL | R/W | 0 | GPIO0 voltage level (applies to any of the MODE_CTRL[1:0] bit settings): 0: LDO_IO level 1: 3V3_SUS level |
| Bits [5:4] | Not used | R | 00 | |
| Bits [7:6] | DRV_STR[1:0] | R/W | 00 | GPIO0 current sink/drive strength value (applies to any of the MODE_CTRL[1:0] bit settings): 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |

8.5.18 GPCTL0B Register (address = 0x15) [reset = 00001000]

Figure 34. GPCTL0B Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|------|----------|----------|------|
| Field Name | Not used | Not used | Not used | Not used | HYST | POLARITY | Not used | TRIG |
| Read/Write | R | R | R | R | R/W | R/W | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 23. GPCTL0B Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|-------|--|
| Bit 0 | TRIG | R/W | 0 | GPIO0 sensitivity control in WAKE operation (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: Edge sensitive (Polarity normal - rising edge, polarity invert - falling edge) 1: Level sensitive (interrupt is cleared when trigger condition is removed) |
| Bit 1 | Not used | R | 0 | |
| Bit 2 | POLARITY | R/W | 0 | GPIO0 polarity control (applies to any of the MODE_CTRL[1:0] bit settings): 0: Normal 1: Inverted |
| Bit 3 | HYST | R/W | 1 | GPIO0 hysteresis control (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: No hysteresis 1: Hysteresis |
| Bits [7:4] | Not used | R | 0000 | |

8.5.19 GPCTL1A Register (address = 0x16) [reset = 00000001]

Figure 35. GPCTL1A Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|-----|----------|----------|-------|-------|----------------|-----|
| Field Name | DRV_STR[1:0] | | Not used | Not used | LEVEL | DMODE | MODE_CTRL[1:0] | |
| Read/Write | R/W | R/W | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

LEGEND: R/W = Read/Write; R = Read only

Table 24. GPCTL1A Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------------|------|-------|---|
| Bits [1:0] | MODE_CTRL[1:0] | R/W | 01 | GPIO1 operation mode: 00: GPIO input 01: GPIO input, pull-up 10: GPIO output, CMOS (push-pull) 11: GPIO output, open-drain pull-down |
| Bit 2 | DMODE | R/W | 0 | GPIO1 drive mode when configured as an output (CMOS or open-drain) via the MODE_CTRL[1:0] bits: 0: Voltage mode (only CMOS is supported) 1: Current mode (only open-drain is supported) |
| Bit 3 | LEVEL | R/W | 0 | GPIO1 voltage level (applies to any of the MODE_CTRL[1:0] bit settings): 0: LDO_IO level 1: 3V3_SUS level |
| Bits [5:4] | Not used | R | 00 | |
| Bits [7:6] | DRV_STR[1:0] | R/W | 00 | GPIO1 current sink/drive strength value (applies to any of the MODE_CTRL[1:0] bit settings): 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |

8.5.20 GPCTL1B Register (address = 0x17) [reset = 00001000]

Figure 36. GPCTL1B Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|------|----------|----------|------|
| Field Name | Not used | Not used | Not used | Not used | HYST | POLARITY | Not used | TRIG |
| Read/Write | R | R | R | R | R/W | R/W | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 25. GPCTL1B Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|-------|--|
| Bit 0 | TRIG | R/W | 0 | GPIO1 sensitivity control in WAKE operation (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: Edge sensitive (Polarity normal - rising edge, polarity invert - falling edge) 1: Level sensitive (interrupt is cleared when trigger condition is removed) |
| Bit 1 | Not used | R | 0 | |
| Bit 2 | POLARITY | R/W | 0 | GPIO1 polarity control (applies to any of the MODE_CTRL[1:0] bit settings): 0: Normal 1: Inverted |
| Bit 3 | HYST | R/W | 1 | GPIO1 hysteresis control (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: No hysteresis 1: Hysteresis |
| Bits [7:4] | Not used | R | 0000 | |

8.5.21 GPCTL2A Register (address = 0x18) [reset = 00000001]

Figure 37. GPCTL2A Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|-----|----------|----------|-------|-------|----------------|-----|
| Field Name | DRV_STR[1:0] | | Not used | Not used | LEVEL | DMODE | MODE_CTRL[1:0] | |
| Read/Write | R/W | R/W | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

LEGEND: R/W = Read/Write; R = Read only

Table 26. GPCTL2A Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------------|------|-------|---|
| Bits [1:0] | MODE_CTRL[1:0] | R/W | 01 | GPIO2 operation mode: 00: GPIO input 01: GPIO input, pull-up 10: GPIO output, CMOS (push-pull) 11: GPIO output, open-drain pull-down |
| Bit 2 | DMODE | R/W | 0 | GPIO2 drive mode when configured as an output (CMOS or open-drain) via the MODE_CTRL[1:0] bits: 0: Voltage mode (only CMOS is supported) 1: Current mode (only open-drain is supported) |
| Bit 3 | LEVEL | R/W | 0 | GPIO2 voltage level (applies to any of the MODE_CTRL[1:0] bit settings): 0: LDO_IO level 1: 3V3_SUS level |
| Bits [5:4] | Not used | R | 00 | |
| Bits [7:6] | DRV_STR[1:0] | R/W | 00 | GPIO2 current sink/drive strength value (applies to any of the MODE_CTRL[1:0] bit settings): 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |

8.5.22 GPCTL2B Register (address = 0x19) [reset = 00001000]

Figure 38. GPCTL2B Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|------|----------|----------|------|
| Field Name | Not used | Not used | Not used | Not used | HYST | POLARITY | Not used | TRIG |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 27. GPCTL2B Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|-------|--|
| Bit 0 | TRIG | R/W | 0 | GPIO2 sensitivity control in WAKE operation (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: Edge sensitive (Polarity normal - rising edge, polarity invert - falling edge) 1: Level sensitive (interrupt is cleared when trigger condition is removed) |
| Bit 1 | Not used | R/W | 0 | |
| Bit 2 | POLARITY | R/W | 0 | GPIO2 polarity control (applies to any of the MODE_CTRL[1:0] bit settings): 0: Normal 1: Inverted |
| Bit 3 | HYST | R/W | 1 | GPIO2 hysteresis control (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: No hysteresis 1: Hysteresis |
| Bits [7:4] | Not used | R | 0000 | |

8.5.23 GPCTL3A Register (address = 0x1A) [reset = 00000001]

Figure 39. GPCTL3A Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|-----|----------|----------|-------|-------|----------------|-----|
| Field Name | DRV_STR[1:0] | | Not used | Not used | LEVEL | DMODE | MODE_CTRL[1:0] | |
| Read/Write | R/W | R/W | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

LEGEND: R/W = Read/Write; R = Read only

Table 28. GPCTL3A Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------------|------|-------|---|
| Bits [1:0] | MODE_CTRL[1:0] | R/W | 01 | GPIO3 operation mode: 00: GPIO input 01: GPIO input, pull-up 10: GPIO output, CMOS (push-pull) 11: GPIO output, open-drain pull-down |
| Bit 2 | DMODE | R/W | 0 | GPIO3 drive mode when configured as an output (CMOS or open-drain) via the MODE_CTRL[1:0] bits: 0: Voltage mode (only CMOS is supported) 1: Current mode (only open-drain is supported) |
| Bit 3 | LEVEL | R/W | 0 | GPIO3 voltage level (applies to any of the MODE_CTRL[1:0] bit settings): 0: LDO_IO level 1: 3V3_SUS level |
| Bits [5:4] | Not used | R | 00 | |
| Bits [7:6] | DRV_STR[1:0] | R/W | 00 | GPIO3 current sink/drive strength value (applies to any of the MODE_CTRL[1:0] bit settings): 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |

8.5.24 GPCTL3B Register (address = 0x1B) [reset = 00001000]

Figure 40. GPCTL3B Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|------|----------|----------|------|
| Field Name | Not used | Not used | Not used | Not used | HYST | POLARITY | Not used | TRIG |
| Read/Write | R | R | R | R | R/W | R/W | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 29. GPCTL3B Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|-------|--|
| Bit 0 | TRIG | R/W | 0 | GPIO3 sensitivity control in WAKE operation (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: Edge sensitive (Polarity normal - rising edge, polarity invert - falling edge) 1: Level sensitive (interrupt is cleared when trigger condition is removed) |
| Bit 1 | Not used | R | 0 | |
| Bit 2 | POLARITY | R/W | 0 | GPIO3 polarity control (applies to any of the MODE_CTRL[1:0] bit settings): 0: Normal 1: Inverted |
| Bit 3 | HYST | R/W | 1 | GPIO3 hysteresis control (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: No hysteresis 1: Hysteresis |
| Bits [7:4] | Not used | R | 0000 | |

8.5.25 GPCTL4A Register (address = 0x1C) [reset = 00000001]

Figure 41. GPCTL4A Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|-----|----------|----------|-------|-------|----------------|-----|
| Field Name | DRV_STR[1:0] | | Not used | Not used | LEVEL | DMODE | MODE_CTRL[1:0] | |
| Read/Write | R/W | R/W | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

LEGEND: R/W = Read/Write; R = Read only

Table 30. GPCTL4A Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------------|------|-------|---|
| Bits [1:0] | MODE_CTRL[1:0] | R/W | 01 | GPIO4 operation mode: 00: GPIO input 01: GPIO input, pull-up 10: GPIO output, CMOS (push-pull) 11: GPIO output, open-drain pull-down |
| Bit 2 | DMODE | R/W | 0 | GPIO4 drive mode when configured as an output (CMOS or open-drain) via the MODE_CTRL[1:0] bits: 0: Voltage mode (only CMOS is supported) 1: Current mode (only open-drain is supported) |
| Bit 3 | LEVEL | R/W | 0 | GPIO4 voltage level (applies to any of the MODE_CTRL[1:0] bit settings): 0: LDO_IO level 1: 3V3_SUS level |
| Bits [5:4] | Not used | R | 00 | |
| Bits [7:6] | DRV_STR[1:0] | R/W | 00 | GPIO4 current sink/drive strength value (applies to any of the MODE_CTRL[1:0] bit settings): 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |

8.5.26 GPCTL4B Register (address = 0x1D) [reset = 00001000]

Figure 42. GPCTL4B Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|------|----------|----------|------|
| Field Name | Not used | Not used | Not used | Not used | HYST | POLARITY | Not used | TRIG |
| Read/Write | R | R | R | R | R/W | R/W | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 31. GPCTL4B Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|-------|--|
| Bit 0 | TRIG | R/W | 0 | GPIO4 sensitivity control in WAKE operation (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: Edge sensitive (Polarity normal - rising edge, polarity invert - falling edge) 1: Level sensitive (interrupt is cleared when trigger condition is removed) |
| Bit 1 | Not used | R | 0 | |
| Bit 2 | POLARITY | R/W | 0 | GPIO4 polarity control (applies to any of the MODE_CTRL[1:0] bit settings): 0: Normal 1: Inverted |
| Bit 3 | HYST | R/W | 1 | GPIO4 hysteresis control (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: No hysteresis 1: Hysteresis |
| Bits [7:4] | Not used | R | 0000 | |

8.5.27 GPCTL5A Register (address = 0x1E) [reset = 00000001]

Figure 43. GPCTL5A Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|-----|----------|----------|-------|-------|----------------|-----|
| Field Name | DRV_STR[1:0] | | Not used | Not used | LEVEL | DMODE | MODE_CTRL[1:0] | |
| Read/Write | R/W | R/W | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

LEGEND: R/W = Read/Write; R = Read only

Table 32. GPCTL5A Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------------|------|-------|---|
| Bits[1:0] | MODE_CTRL[1:0] | R/W | 01 | GPIO5 operation mode: 00: GPIO input 01: GPIO input, pull-up 10: GPIO output, CMOS (push-pull) 11: GPIO output, open-drain pull-down |
| Bit 2 | DMODE | R/W | 0 | GPIO5 drive mode when configured as an output (CMOS or open-drain) via the MODE_CTRL[1:0] bits: 0: Voltage mode (only CMOS is supported) 1: Current mode (only open-drain is supported) |
| Bit 3 | LEVEL | R/W | 0 | GPIO5 voltage level (applies to any of the MODE_CTRL[1:0] bit settings): 0: LDO_IO level 1: 3V3_SUS level |
| Bits [5:4] | Not used | R | 00 | |
| Bits [7:6] | DRV_STR[1:0] | R/W | 00 | GPIO5 current sink/drive strength value (applies to any of the MODE_CTRL[1:0] bit settings): 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |

8.5.28 GPCTL5B Register (address = 0x1F) [reset = 00001000]

Figure 44. GPCTL5B Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|------|----------|----------|------|
| Field Name | Not used | Not used | Not used | Not used | HYST | POLARITY | Not used | TRIG |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 33. GPCTL5B Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|-------|--|
| Bit 0 | TRIG | R/W | 0 | GPIO5 sensitivity control in WAKE operation (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: Edge sensitive (Polarity normal - rising edge, polarity invert - falling edge) 1: Level sensitive (interrupt is cleared when trigger condition is removed) |
| Bit 1 | Not used | R/W | 0 | |
| Bit 2 | POLARITY | R/W | 0 | GPIO5 polarity control (applies to any of the MODE_CTRL[1:0] bit settings): 0: Normal 1: Inverted |
| Bit 3 | HYST | R/W | 1 | GPIO5 hysteresis control (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: No hysteresis 1: Hysteresis |
| Bits [7:4] | Not used | R | 0000 | |

8.5.29 GPCTL6A Register (address = 0x20) [reset = 00000001]

Figure 45. GPCTL6A Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|--------------|-----|----------|----------|-------|-------|----------------|-----|
| Field Name | DRV_STR[1:0] | | Not used | Not used | LEVEL | DMODE | MODE_CTRL[1:0] | |
| Read/Write | R/W | R/W | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

LEGEND: R/W = Read/Write; R = Read only

Table 34. GPCTL6A Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------------|------|-------|---|
| Bits [1:0] | MODE_CTRL[1:0] | R/W | 01 | GPIO6 operation mode: 00: GPIO input 01: GPIO input, pull-up 10: GPIO output, CMOS (push-pull) 11: GPIO output, open-drain pull-down |
| Bit 2 | DMODE | R/W | 0 | GPIO6 drive mode when configured as an output (CMOS or open-drain) via the MODE_CTRL[1:0] bits: 0: Voltage mode (only CMOS is supported) 1: Current mode (only open-drain is supported) |
| Bit 3 | LEVEL | R/W | 0 | GPIO6 voltage level (applies to any of the MODE_CTRL[1:0] bit settings): 0: LDO_IO level 1: 3V3_SUS level |
| Bits [5:4] | Not used | R | 00 | |
| Bits [7:6] | DRV_STR[1:0] | R/W | 00 | GPIO6 current sink/drive strength value (applies to any of the MODE_CTRL[1:0] bit settings): 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |

8.5.30 GPCTL6B Register (address = 0x21) [reset = 00001000]

Figure 46. GPCTL6B Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|------|----------|----------|------|
| Field Name | Not used | Not used | Not used | Not used | HYST | POLARITY | Not used | TRIG |
| Read/Write | R | R | R | R | R/W | R/W | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 35. GPCTL6B Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|-------|--|
| Bit 0 | TRIG | R/W | 0 | GPIO6 sensitivity control in WAKE operation (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: Edge sensitive (Polarity normal - rising edge, polarity invert - falling edge) 1: Level sensitive (interrupt is cleared when trigger condition is removed) |
| Bit 1 | Not used | R | 0 | |
| Bit 2 | POLARITY | R/W | 0 | GPIO6 polarity control (applies to any of the MODE_CTRL[1:0] bit settings): 0: Normal 1: Inverted |
| Bit 3 | HYST | R/W | 1 | GPIO6 hysteresis control (applies only to the input modes set via the MODE_CTRL[1:0] bits): 0: No hysteresis 1: Hysteresis |
| Bits [7:4] | Not used | R | 0000 | |

8.5.31 SGPO Register (address = 0x22) [reset = 00000000]

Figure 47. SGPO Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|--------------|-----|----------|----------|--------|----------|
| Field Name | Not used | Not used | DRV_STR[1:0] | | Not used | S_RESETN | S_IDLE | S_ENABLE |
| Read/Write | R | R | R/W | R/W | R | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 36. SGPO Register Description

| Bit | Field | Type | Reset | Description |
|------------|--------------|------|-------|--|
| Bit 0 | S_ENABLE | R/W | 0 | Control of S_ENABLE pin 0: Low 1: High |
| Bit 1 | S_IDLE | R/W | 0 | Control of S_IDLE pin 0: Low 1: High |
| Bit 2 | S_RESETN | R/W | 0 | Control of S_RESETN pin 0: Low 1: High |
| Bit 3 | Not used | R | 0 | |
| Bits [5:4] | DRV_STR[1:0] | R/W | 00 | Sensor output drive strength control 00 : 1 mA 01 : 2 mA 10 : 4 mA 11 : 8 mA |
| Bits [7:6] | Not used | R | 00 | |

8.5.32 PITCTL Register (address = 0x23) [reset = 00000000]

Figure 48. PITCTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|-----|-----|-----|-----|-----|-----|-----|
| Field Name | Not used | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 37. PITCTL Register Description

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| Bit 0 | GP0 | R/W | 0 | GPIO0 Wake control (GPIO0 must be set as an input via the MODE_CTRL[1:0] bits): 0: Wake disabled 1: Wake enabled |
| Bit 1 | GP1 | R/W | 0 | GPIO1 Wake control (GPIO1 must be set as an input via the MODE_CTRL[1:0] bits): 0: Wake disabled 1: Wake enabled |
| Bit 2 | GP2 | R/W | 0 | GPIO2 Wake control (GPIO2 must be set as an input via the MODE_CTRL[1:0] bits): 0: Wake disabled 1: Wake enabled |
| Bit 3 | GP3 | R/W | 0 | GPIO3 Wake control (GPIO3 must be set as an input via the MODE_CTRL[1:0] bits): 0: Wake disabled 1: Wake enabled |
| Bit 4 | GP4 | R/W | 0 | GPIO4 Wake control (GPIO4 must be set as an input via the MODE_CTRL[1:0] bits): 0: Wake disabled 1: Wake enabled |
| Bit 5 | GP5 | R/W | 0 | GPIO5 Wake control (GPIO5 must be set as an input via the MODE_CTRL[1:0] bits): 0: Wake disabled 1: Wake enabled |
| Bit 6 | GP6 | R/W | 0 | GPIO6 Wake control (GPIO6 must be set as an input via the MODE_CTRL[1:0] bits): 0: Wake disabled 1: Wake enabled |
| Bit 7 | Not used | R | 0 | |

8.5.33 WAKECFG Register (address = 0x24) [reset = 00000000]

Figure 49. WAKECFG Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------------|-----|---------------|-----|-----|----------------|-----|-----|
| Field Name | TXMASK_CONF[1:0] | | INT_CONF[2:0] | | | WAKE_CONF[2:0] | | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write

Table 38. WAKECFG Register Description

| Bit | Field | Type | Reset | Description |
|------------|-------------------------------------|------|-------|---|
| Bits [2:0] | WAKE_CONF[2:0] ⁽¹⁾⁽²⁾⁽³⁾ | R/W | 000 | Wake output configuration 000: No output, only GSTAT flag 001: Routed to GPIO0 010: routed to GPIO1 011: Routed to GPIO2 100: Routed to GPIO3 101: Routed to GPIO4 110: routed to GPIO5 111: Routed to GPIO6 |
| Bits [5:3] | INT_CONF[2:0] ⁽¹⁾⁽³⁾ | R/W | 000 | Interrupt output configuration ⁽⁴⁾ 000: No output 001: Routed to GPIO0 010: Routed to GPIO1 011: Routed to GPIO2 100: routed to GPIO3 101: Routed to GPIO4 110: routed to GPIO5 111: Routed to GPIO6 |
| Bits [7:6] | TXMASK_CONF[1:0] | R/W | 00 | Txmask input configuration 00: TX masking disabled 01: Routed from GPIO2 10: Routed from GPIO3 11: Routed from GPIO4 |

- (1) GPIOs configured by the WAKE_CONF[2:0] or INT_CONF[2:0] bits must be programmed as outputs in the respective GPCTLxA registers.
- (2) Setting the WAKE_CONF[2:0] bits creates an external interrupt signal (Wake) generated by the PIT block.
- (3) If both the WAKE_CONF[2:0] and INT_CONF[2:0] bits are configured for the same pin, the signals will be ORed before exiting the device.
- (4) Interrupt is an internal event (e.g., TSD tripping).

8.5.34 IOWAKESTAT Register (address = 0x25) [reset = 00000000]

Figure 50. IOWAKESTAT Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|-------|-------|-------|-------|-------|-------|-------|
| Field Name | Not used | GP6 | GP5 | GP4 | GP3 | GP2 | GP1 | GP0 |
| Read/Write | R | R/W1C | R/W1C | R/W1C | R/W1C | R/W1C | R/W1C | R/W1C |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R = Read only; R/W1C = Read/Write 1 to Clear

Table 39. IOWAKESTAT Register Description⁽¹⁾

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| Bit 0 | GP0 | R/W | 0 | GPIO0 Wake status 0: Wake inactive 1: Wake active |
| Bit 1 | GP1 | R/W | 0 | GPIO1 Wake status 0: Wake inactive 1: Wake active |
| Bit 2 | GP2 | R/W | 0 | GPIO2 Wake status 0: Wake inactive 1: Wake active |
| Bit 3 | GP3 | R/W | 0 | GPIO3 Wake status 0: Wake inactive 1: Wake active |
| Bit 4 | GP4 | R/W | 0 | GPIO4 Wake status 0: Wake inactive 1: Wake active |
| Bit 5 | GP5 | R/W | 0 | GPIO5 Wake status 0: Wake inactive 1: Wake active |
| Bit 6 | GP6 | R/W | 0 | GPIO6 Wake status 0: Wake inactive 1: Wake active |
| Bit 7 | Not used | R | 0 | |

(1) All status bits get ORed depending on the PITCTL register. The result is reflected in GSTAT register.

8.5.35 GPDI Register (address = 0x26) [reset = 00000000]

Figure 51. GPDI Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|-------|-------|-------|-------|-------|-------|-------|
| Field Name | Not used | GPIO6 | GPIO5 | GPIO4 | GPIO3 | GPIO2 | GPIO1 | GPIO0 |
| Read/Write | R | R | R | R | R | R | R | R |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R = Read only

Table 40. GPDI Register Description⁽¹⁾⁽²⁾

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|--|
| Bit 0 | GPIO0 | R | 0 | State of the GPIO0 input (dependent on the polarity settings in the GPCTL0B register) 0: Low 1: High |
| Bit 1 | GPIO1 | R | 0 | State of the GPIO1 input (dependent on the polarity settings in the GPCTL1B register) 0: Low 1: High |
| Bit 2 | GPIO2 | R | 0 | State of the GPIO2 input (dependent on the polarity settings in the GPCTL2B register) 0: Low 1: High |
| Bit 3 | GPIO3 | R | 0 | State of the GPIO3 input (dependent on the polarity settings in the GPCTL3B register) 0: Low 1: High |
| Bit 4 | GPIO4 | R | 0 | State of the GPIO4 input (dependent on the polarity settings in the GPCTL4B register) 0: Low 1: High |
| Bit 5 | GPIO5 | R | 0 | State of the GPIO5 input (dependent on the polarity settings in the GPCTL5B register) 0: Low 1: High |
| Bit 6 | GPIO6 | R | 0 | State of the GPIO6 input (dependent on the polarity settings in the GPCTL6B register) 0: Low 1: High |
| Bit 7 | Not used | R | 0 | |

(1) The bit values reflect the real-time state of the GPIO inputs.

(2) Latched bits are implemented in the IOWAKESTAT register. These bits must be written to be cleared.

8.5.36 GPDO Register (address = 0x27) [reset = 00000000]

Figure 52. GPDO Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|-------|-------|-------|-------|-------|-------|-------|
| Field Name | Not used | GPIO6 | GPIO5 | GPIO4 | GPIO3 | GPIO2 | GPIO1 | GPIO0 |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 41. GPDO Register Description

| Bit | Field | Type | Reset | Description |
|-------|----------|------|-------|---|
| Bit 0 | GPIO0 | R/W | 0 | Control of the GPIO0 output (dependent on the polarity settings in the GPCTL0B register) 0: Low 1: High |
| Bit 1 | GPIO1 | R/W | 0 | State of the GPIO1 output (dependent on the polarity settings in the GPCTL1B register) 0: Low 1: High |
| Bit 2 | GPIO2 | R/W | 0 | State of the GPIO2 output (dependent on the polarity settings in the GPCTL2B register) 0: Low 1: High |
| Bit 3 | GPIO3 | R/W | 0 | State of the GPIO3 output (dependent on the polarity settings in the GPCTL3B register) 0: Low 1: High |
| Bit 4 | GPIO4 | R/W | 0 | State of the GPIO4 output (dependent on the polarity settings in the GPCTL4B register) 0: Low 1: High |
| Bit 5 | GPIO5 | R/W | 0 | State of the GPIO5 output (dependent on the polarity settings in the GPCTL5B register) 0: Low 1: High |
| Bit 6 | GPIO6 | R/W | 0 | State of the GPIO6 output (dependent on the polarity settings in the GPCTL6B register) 0: Low 1: High |
| Bit 7 | Not used | R | 0 | |

8.5.37 ILEDCTL Register (address = 0x28) [reset = 00000000]
Figure 53. ILEDCTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------|-----|------------|-----|-------|-----|----------|----------|
| Field Name | FAILB | ENB | CTRLB[1:0] | | FAILA | ENA | Not used | Not used |
| Read/Write | R | R/W | R/W | R/W | R | R/W | R | R |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 42. ILEDCTL Register Description

| Bit | Field | Type | Reset | Description |
|------------|------------|------|-------|---|
| Bits [1:0] | Not used | R | 00 | |
| Bit 2 | ENA | R/W | 0 | ILED_A driver status 0: Disabled 1: Enabled, 16mA |
| Bit 3 | FAILA | R | 0 | ILED_A driver output failure mode 0: Open 1: Shorted |
| Bits [5:4] | CTRLB[1:0] | R/W | 00 | Controls ILED_B current sink value 00 : 2 mA 01 : 4 mA 10 : 8 mA 11 : 16 mA |
| Bit 6 | ENB | R/W | 0 | ILED_B driver status 0: Disabled 1: Enabled |
| Bit 7 | FAILB | R | 0 | ILED_B driver output failure mode 0: Open 1: Shorted |

8.5.38 WLEDSTAT Register (address = 0x29) [reset = 00000000]

Figure 54. WLEDSTAT Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|-----|------|----|----------|--------|---------|--------|
| Field Name | S_STROBE | TSD | LEDF | TO | Not used | LEDHOT | LEDWARN | ENTMON |
| Read/Write | R | R | R | R | R | R | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 43. WLEDSTAT Register Description

| Bit | Field | Type | Reset | Description |
|-------|------------------------|------|-------|--|
| Bit 0 | ENTMON | R/W | 0 | Enable LED temperature monitoring (LEDHOT, LEDWARN) |
| Bit 1 | LEDWARN ⁽¹⁾ | R | 0 | LED Temperature warning flag 0 : TS input voltage > 1.05 V 1 : TS input voltage <1.05 V |
| Bit 2 | LEDHOT ⁽¹⁾ | R | 0 | LED Excessive temperature flag ⁽²⁾ 0 : TS input voltage > 0.345 V 1 : TS input voltage <0.345 V |
| Bit 3 | Not used | R | 0 | |
| Bit 4 | TO ⁽¹⁾ | R | 0 | Flash LED time out 0 : No time-out event 1. Time-out event occurred. Flag is reset at re-start of the safety timer |
| Bit 5 | LEDF ⁽¹⁾ | R | 0 | Flash LED short 0 : No failure 1 : Failure |
| Bit 6 | TSD | R | 0 | Flash Overtemperature Status Bit 0 : No failure 1 : Thermal shutdown tripped |
| Bit 7 | S_STROBE | R | 0 | Reflects the state of the S_STROBE signal |

(1) LEDF, TO, LEDHOT and LEDWARN will each generate an interrupt and report status via the WLEDF bit in the GSTAT register unless masked in the INTMASK register. These status bits (except for the TO bit and provided the condition is no longer present) are cleared by writing a '1' to the WLEDF bit in the GSTAT register or by masking the WLEDF bit in the INTMASK register.

(2) With 220-kΩ NTC (Eg. MURATA NCP18WM224J03RB) the valid temperature window is between 60°C and 90°C.

8.5.39 VWLEDILIM Register (address = 0x2A) [reset = 00001010]
Figure 55. VWLEDILIM Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|-----------|-----|-----|-----|
| Field Name | Not used | Not used | Not used | Not used | ILIM[3:0] | | | |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 44. VWLEDILIM Register Description

| Bit | Field | Type | Reset | Description |
|------------|-----------|------|-------|--|
| Bits [3:0] | ILIM[3:0] | R/W | 1010 | Boost current limit setting 0000 : 2 A 0001 : 2.2 A 0010 : 2.4 A 0011 : 2.6 A 0100 : 2.8 A 0101 : 3.0 A 0110 : 3.2 A 0111 : 3.4 A - 1000 : 3.6 A 1001 : 3.8 A 1010 : 4.0 A 1011 : 4.2 A 1100 : 4.4 A 1101 : 4.6 A 1110 : 4.8 A 1111 : 5 A |
| Bits [7:4] | Not used | R | 0000 | |

8.5.40 VWLEDVAL Register (address = 0x2B) [reset = 00000000]
Figure 56. VWLEDVAL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|---------|-----|-----|-----|
| Field Name | Not used | Not used | Not used | Not used | OV[3:0] | | | |
| Read/Write | R | R | R | R | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 45. VWLEDVAL Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|-------|---|
| Bits [3:0] | OV[3:0] | R/W | 0000 | Boost output voltage in voltage mode, 120-mV steps 0000 : 3.68 V 0001 : 3.80 V 0010 : 3.92 V 0011 : 4.04 V 0100 : 4.16 V 0101 : 4.28 V 0110 : 4.40 V 0111 : 4.52 V - 1000 : 4.64 V 1001 : 4.76 V 1010 : 4.88 V 1011 : 5.00 V 1100 : 5.12 V 1101 : 5.24 V 1110 : 5.36 V 1111 : 5.48 V |
| Bits [7:4] | Not used | R | 0000 | |

8.5.41 WLEDMAXRER Register (address = 0x2C) [reset = 00000000]

Figure 57. WLEDMAXRER Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|--------------|-----|-----|-----|-----|
| Field Name | Not used | Not used | Not used | MAX_CUR[4:0] | | | | |
| Read/Write | R | R | R | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 46. WLEDMAXRER Register Description⁽¹⁾

| Bit | Field | Type | Reset | Description |
|------------|--------------|------|-------|--|
| Bits [3:0] | MAX_CUR[4:0] | R/W | 0000 | WLED RER Mode max current setting (in 32.5-mA steps) 00000 : 0 mA 00001 : 32.5 mA 00010 : 65 mA 00011 : 97.5 mA 00100 : 130.0 mA 00101 : 162.5 mA 00110 : 195.0 mA 00111 : 227.5 mA 01000 : 260.0 mA 01001 : 292.5 mA 01010 : 325.0 mA 01011 : 357.5 mA 01100 : 390.0 mA 01101 : 422.5 mA 01110 : 455.0 mA 01111 : 487.5 mA 10000 : 520.0 mA 10001 : 552.5 mA 10010 : 585.0 mA 10011 : 617.5 mA 10100 : 650.0 mA 10101 : 682.5 mA 10110 : 715.0 mA 10111 : 747.5 mA 11000 : 780.0 mA 11001 : 812.5 mA 11010 : 845.0 mA 11011 : 877.5 mA 11100 : 910.0 mA 11101 : 942.5 mA 11110 : 975.0 mA 11111 : 1007.5 mA |
| Bits [7:4] | Not used | R | 0000 | |

(1) WLEDMAXRER register cannot be written when WLED is enabled.

8.5.42 WLEDMAXT Register (address = 0x2D) [reset = 00000000]

Figure 58. WLEDMAXT Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|--------------|-----|-----|
| Field Name | Not used | Not used | Not used | Not used | Not used | MAX_CUR[2:0] | | |
| Read/Write | R | R | R | R | R | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 47. WLEDMAXT Register Description⁽¹⁾

| Bit | Field | Type | Reset | Description |
|------------|--------------|------|-------|---|
| Bits [2:0] | MAX_CUR[2:0] | R/W | 000 | WLED Torch Mode max current setting (in 32.5-mA steps) 000 : 0 mA 001 : 32.5 mA 010 : 65 mA 011 : 97.5 mA 100 : 130.0 mA 101 : 162.5 mA 110 : 195.0 mA 111 : 227.5 mA |
| Bits [7:3] | Not used | R | 00000 | |

(1) WLEDMAXT register cannot be written when WLED is enabled.

8.5.43 WLEDMAXAF Register (address = 0x2E) [reset = 00000000]

Figure 59. WLEDMAXAF Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|--------------|-----|-----|-----|-----|
| Field Name | Not used | Not used | Not used | MAX_CUR[4:0] | | | | |
| Read/Write | R | R | R | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 48. WLEDMAXAF Register Description⁽¹⁾

| Bit | Field | Type | Reset | Description |
|------------|--------------|------|-------|---|
| Bits [4:0] | MAX_CUR[4:0] | R/W | 00000 | WLED Focus Assist Mode max current setting (in 32.5-mA steps) 00000 : 0 mA 00001 : 32.5 mA 00010 : 65 mA 00011 : 97.5 mA 00100 : 130.0 mA 00101 : 162.5 mA 00110 : 195.0 mA 00111 : 227.5 mA 01000 : 260.0 mA 01001 : 292.5 mA 01010 : 325.0 mA 01011 : 357.5 mA 01100 : 390.0 mA 01101 : 422.5 mA 01110 : 455.0 mA 01111 : 487.5 mA 10000 : 520.0 mA 10001 : 552.5 mA 10010 : 585.0 mA 10011 : 617.5 mA 10100 : 650.0 mA 10101 : 682.5 mA 10110 : 715.0 mA 10111 : 747.5 mA 11000 : 780.0 mA 11001 : 812.5 mA 11010 : 845.0 mA 11011 : 877.5 mA 11100 : 910.0 mA 11101 : 942.5 mA 11110 : 975.0 mA 11111 : 1007.5 mA |
| Bits [7:5] | Not used | R | 000 | |

⁽¹⁾ WLEDMAXAF register cannot be written when WLED is enabled.

8.5.44 WLEDMAXF Register (address = 0x2F) [reset = 00000000]

Figure 60. WLEDMAXF Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|--------------|-----|-----|-----|-----|
| Field Name | Not used | Not used | Not used | MAX_CUR[4:0] | | | | |
| Read/Write | R | R | R | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 49. WLEDMAXF Register Description⁽¹⁾

| Bit | Field | Type | Reset | Description |
|------------|--------------|------|-------|--|
| Bits [4:0] | MAX_CUR[4:0] | R/W | 00000 | WLED Flash Mode max current setting (in 32.5-mA steps) 00000 : 0 mA 00001 : 32.5 mA 00010 : 65 mA 00011 : 97.5 mA 00100 : 130.0 mA 00101 : 162.5 mA 00110 : 195.0 mA 00111 : 227.5 mA 01000 : 260.0 mA 01001 : 292.5 mA 01010 : 325.0 mA 01011 : 357.5 mA 01100 : 390.0 mA 01101 : 422.5 mA 01110 : 455.0 mA 01111 : 487.5 mA 10000 : 520.0 mA 10001 : 552.5 mA 10010 : 585.0 mA 10011 : 617.5 mA 10100 : 650.0 mA 10101 : 682.5 mA 10110 : 715.0 mA 10111 : 747.5 mA 11000 : 780.0 mA 11001 : 812.5 mA 11010 : 845.0 mA 11011 : 877.5 mA 11100 : 910.0 mA 11101 : 942.5 mA 11110 : 975.0 mA 11111 : 1007.5 mA |
| Bits [7:5] | Not used | R | 000 | |

⁽¹⁾ WLEDMAXF register cannot be written when WLED is enabled.

8.5.45 WLEDTO Register (address = 0x30) [reset = 00000000]

Figure 61. WLEDTO Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|---------|-----|----------|-----|----------|------------|-----|-----|
| Field Name | FA[1:0] | | RER[1:0] | | Not used | FLASH[2:0] | | |
| Read/Write | R/W | R/W | R/W | R/W | R | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write

Table 50. WLEDTO Register Description⁽¹⁾⁽²⁾

| Bit | Field | Type | Reset | Description |
|------------|------------|------|-------|--|
| Bits [2:0] | FLASH[2:0] | R/W | 000 | 000 : 37.3 ms 001 : 71.5 ms 010 : 102.2 ms 011 : 136.3 ms 100 : 204 ms 101 : 340 ms 110 : 579 ms 111 : 852 ms |
| Bit 3 | Not used | R | 0 | |
| Bits [5:4] | RER[1:0] | R/W | 00 | 00 : 37.3 ms 01 : 71.5 ms 10 : 102.2 ms 11 : 136.3 ms |
| Bits [7:6] | FA[1:0] | R/W | 00 | 00 : 204.5 ms 01 : 340.8 ms 10 : 579.3 ms 11 : 852 ms |

(1) Torch/video light has a fixed 13s timeout. This is based on an assumed 2-MHz clock and the time will vary depending on the boost clock generated from PLL.

(2) The WLEDTO register cannot be written when WLED is enabled.

8.5.46 VWLEDCTL Register (address = 0x31) [reset = 00111000]
Figure 62. VWLEDCTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|---------------|-----|------------|-------|-----|--------|
| Field Name | WLED_T[1:0] | | HEADROOM[1:0] | | EN_PLL_CLK | VMODE | TSD | ENABLE |
| Read/Write | R | R | R/W | R/W | R/W | R/W | R | R/W |
| Reset Value | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 51. VWLEDCTL Register Description⁽¹⁾⁽²⁾⁽³⁾

| Bit | Field | Type | Reset | Description |
|------------|---------------|------|-------|---|
| Bit 0 | ENABLE | R/W | 0 | WLED Enable Control 0: Output disabled 1: Output enabled |
| Bit 1 | TSD | R | 0 | WLED thermal shutdown status 0 : Boost thermal shutdown not active. 1 : Boost thermal shutdown active. |
| Bit 2 | VMODE | R/W | 0 | WLED mode control 0 : Boost regulates the headroom over flash LED current sources 1 : Boost regulates the output voltage according to setting in OV[3:0] register bits (Voltage Mode) |
| Bit 3 | EN_PLL_CLK | R/W | 1 | WLED clock control 0 : Internal oscillator 1 : PLL clock |
| Bits [5:4] | HEADROOM[1:0] | R/W | 11 | Flash current sink headroom voltage setting. Must always be set to the default setting of '11'. 00 : Reserved 01 : Reserved 10 : Reserved 11 : 400 mV (Default Setting) |
| Bits [7:6] | WLED_T[1:0] | R | 00 | WLED boost die temperature monitor (Status is only valid when the ENABLE bit is set) 00 : T _j < +55°C 01 : +55°C < T _j < +70°C 10 : Illegal state 11 : T _j > +70°C |

- (1) Boost can be enabled either with VWLEDCTL or WLEDCTL register.
 (2) Enabling the boost in this register should only be done when the boost is being operated as a generic voltage regulator.
 (3) CLK muxing is not glitchless and should be done prior to starting the boost.

8.5.47 WLEDTIMER_MSB Register (address = 0x32) [reset = 00000000]

Figure 63. WLEDTIMER_MSB Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|----------|-------------|-----|
| Field Name | Not used | Not used | Not used | Not used | Not used | Not used | TPULSE[9:8] | |
| Read/Write | R | R | R | R | R | R | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 52. WLEDTIMER_MSB Register Description

| Bit | Field | Type | Reset | Description |
|------------|-------------|------|--------|---|
| Bits [1:0] | TPULSE[9:8] | R/W | 00 | Flash pulse duration (in 1-ms increments) 0x000 : 1 ms 0x001 : 2 ms ... 0x3FF: 1023 ms ⁽¹⁾ |
| Bits [7:3] | Not used | R | 000000 | |

(1) Maximum allowed pulse length depends on the WLED mode and on the WLEDTO register.

8.5.48 WLEDTIMER_LSB Register (address = 0x33) [reset = 00000000]

Figure 64. WLEDTIMER_LSB Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|-----|-----|-----|-----|-----|-----|-----|
| Field Name | TPULSE[7:0] | | | | | | | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write

Table 53. WLEDTIMER_LSB Register Description

| Bit | Field | Type | Reset | Description |
|-----------|-------------|------|----------|---|
| Bits 7:0] | TPULSE[7:0] | R/W | 00000000 | Flash pulse duration (in 1-ms increments) 0x000 : 1 ms 0x001 : 2 ms ... 0x3FF: 1023 ms ⁽¹⁾ |

(1) Maximum pulse length depends on the WLED mode and on the WLEDTO register.

8.5.49 WLEDC1 Register (address = 0x34) [reset = 00000000]
Figure 65. WLEDC1 Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|-----------|-----|-----|-----|-----|
| Field Name | Not used | Not used | Not used | ILED[4:0] | | | | |
| Read/Write | R | R | R | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 54. WLEDC1 Register Description

| Bit | Field | Type | Reset | Description |
|------------|-----------|------|-------|--|
| Bits [4:0] | ILED[4:0] | R/W | 00000 | WLED1 current setting (in 32.5-mA steps) 00000 : 0 mA 00001 : 32.5 mA 00010 : 65 mA 00011 : 97.5 mA 00100 : 130.0 mA 00101 : 162.5 mA 00110 : 195.0 mA 00111 : 227.5 mA 01000 : 260.0 mA 01001 : 292.5 mA 01010 : 325.0 mA 01011 : 357.5 mA 01100 : 390.0 mA 01101 : 422.5 mA 01110 : 455.0 mA 01111 : 487.5 mA 10000 : 520.0 mA 10001 : 552.5 mA 10010 : 585.0 mA 10011 : 617.5 mA 10100 : 650.0 mA 10101 : 682.5 mA 10110 : 715.0 mA 10111 : 747.5 mA 11000 : 780.0 mA 11001 : 812.5 mA 11010 : 845.0 mA 11011 : 877.5 mA 11100 : 910.0 mA 11101 : 942.5 mA 11110 : 975.0 mA 11111 : 1007.5 mA |
| Bits [7:5] | Not used | R | 000 | |

8.5.50 WLEDC2 Register (address = 0x35) [reset = 00000000]
Figure 66. WLEDC2 Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|-----------|-----|-----|-----|-----|
| Field Name | Not used | Not used | Not used | ILED[4:0] | | | | |
| Read/Write | R | R | R | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 55. WLEDC2 Register Description

| Bit | Field | Type | Reset | Description |
|------------|-----------|------|-------|--|
| Bits [4:0] | ILED[4:0] | R/W | 00000 | WLED2 current setting (in 32.5-mA steps) 00000 : 0 mA 00001 : 32.5 mA 00010 : 65 mA 00011 : 97.5 mA 00100 : 130.0 mA 00101 : 162.5 mA 00110 : 195.0 mA 00111 : 227.5 mA 01000 : 260.0 mA 01001 : 292.5 mA 01010 : 325.0 mA 01011 : 357.5 mA 01100 : 390.0 mA 01101 : 422.5 mA 01110 : 455.0 mA 01111 : 487.5 mA 10000 : 520.0 mA 10001 : 552.5 mA 10010 : 585.0 mA 10011 : 617.5 mA 10100 : 650.0 mA 10101 : 682.5 mA 10110 : 715.0 mA 10111 : 747.5 mA 11000 : 780.0 mA 11001 : 812.5 mA 11010 : 845.0 mA 11011 : 877.5 mA 11100 : 910.0 mA 11101 : 942.5 mA 11110 : 975.0 mA 11111 : 1007.5 mA |
| Bits [7:5] | Not used | R | 000 | |

8.5.51 WLEDCTL Register (address = 0x36) [reset = 00000000]

Figure 67. WLEDCTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|------|-------|---------|---------|-----|-----------|-----|
| Field Name | TRIG_POL | TRIG | START | DISLED2 | DISLED1 | EN | MODE[1:0] | |
| Read/Write | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write

Table 56. WLEDCTL Register Description⁽¹⁾⁽²⁾

| Bit | Field | Type | Reset | Description |
|------------|----------------------------|------|-------|---|
| Bits [1:0] | MODE[1:0] | R/W | 00 | WLED Mode Control 00 : Flash 01 : Torch / video light 10 : Red-eye reduction 11 : Focus assist |
| Bit 2 | EN | R/W | 0 | Boost and WLED driver control 0: Disabled 1: Enables Boost and the WLED driver according to the setting in MODE[1:0] |
| Bit 3 | DISLED1 | R/W | 0 | Disable LED1. Set this to '1' before enabling the WLED driver in current mode if the LED1 is not assembled 0: Enables LED1 1: Disables LED1 |
| Bit 4 | DISLED2 | R/W | 0 | Disable LED2. Set this to '1' before enabling the WLED driver in current mode if the LED2 is not assembled 0: Enables LED2 1: Disables LED2 |
| Bit 5 | START | R/W | 0 | WLED Start bit control 0: No change in flash LED current 1: flash LED current ramps up to preset level and back down after preset pulse length Note: A read of this bit reflects the state of the flash LED current pulse regardless of how the pulse was started Note: If the trigger is level sensitive, the pulse will continue until START is written to '0' or time-out has occurred |
| Bit 6 | TRIG ⁽³⁾⁽⁴⁾ | R/W | 0 | WLED Trigger configuration 0: Level sensitive 1: Edge sensitive |
| Bit 7 | TRIG_POL ⁽³⁾⁽⁵⁾ | R/W | 0 | WLED Trigger polarity 0: Rising edge / trigger when high 1: Falling edge / trigger when low |

(1) Torch and focus assist will immediately begin driving current when enabled. Other modes need START bit to be set (or external S_STROBE).

(2) Torch mode needs to be written repeatedly to avoid 13s watchdog from triggering.

(3) TRIG_POL and TRIG only applies to Flash and Red-Eye reduction.

(4) TRIG applies to both S_STROBE and SW trigger.

(5) TRIG_POL applies only for S_STROBE.

8.5.52 VCMVAL Register (address = 0x3C) [reset = 00000000]
Figure 68. VCMVAL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|-------------|-----|-----|-----|-----|-----|-----|
| Field Name | Not used | VCVOLT[6:0] | | | | | | |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 57. VCMVAL Register Description

| Bit | Field | Type | Reset | Description |
|------------|-------------|------|---------|--|
| Bits [6:0] | VCVOLT[6:0] | R/W | 0000000 | The VR output voltage range is from 875 mV to 3.1 V for codes 0x00 to 0x7D in increments of 17.8 mV 0x00 : 0.875 V 0x01 : 0.8928 V ... 0x7C : 3.082 V 0x7D : 3.10 V 0x7E: Not Supported 0x7F: Not Supported |
| Bit 7 | Not used | R | 0 | |

8.5.53 VAUX1VAL Register (address = 0x3D) [reset = 00000000]
Figure 69. VAUX1VAL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|---------------|-----|-----|-----|-----|-----|-----|
| Field Name | Not used | AUX1VOLT[6:0] | | | | | | |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 58. VAUX1VAL Register Description

| Bit | Field | Type | Reset | Description |
|------------|---------------|------|---------|--|
| Bits [6:0] | AUX1VOLT[6:0] | R/W | 0000000 | The VR output voltage range is from 875 mV to 3.1 V for codes 0x00 to 0x7D in increments of 17.8 mV 0x00 : 0.875 V 0x01 : 0.8928 V ... 0x7C : 3.082 V 0x7D : 3.10 V 0x7E: Not Supported 0x7F: Not Supported |
| Bit 7 | Not used | R | 0 | |

8.5.54 VAUX2VAL Register (address = 0x3E) [reset = 00000000]

Figure 70. VAUX2VAL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|---------------|-----|-----|-----|-----|-----|-----|
| Field Name | Not used | AUX2VOLT[6:0] | | | | | | |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 59. VAUX2VAL Register Description

| Bit | Field | Type | Reset | Description |
|------------|---------------|------|---------|--|
| Bits [6:0] | AUX2VOLT[6:0] | R/W | 0000000 | The VR output voltage range is from 875 mV to 3.1 V for codes 0x00 to 0x7D in increments of 17.8 mV 0x00 : 0.875 V 0x01 : 0.8928 V ... 0x7C : 3.082 V 0x7D : 3.10 V 0x7E: Not Supported 0x7F: Not Supported |
| Bit 7 | Not used | R | 0 | |

8.5.55 VIOVAL Register (address = 0x3F) [reset = 00110100]

Figure 71. VIOVAL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|-------------|-----|-----|-----|-----|-----|-----|
| Field Name | Not used | IOVOLT[6:0] | | | | | | |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 60. VIOVAL Register Description

| Bit | Field | Type | Reset | Description |
|------------|-------------|------|---------|--|
| Bits [6:0] | IOVOLT[6:0] | R/W | 0110100 | The VR output voltage range is from 875 mV to 3.1 V for codes 0x00 to 0x7D in increments of 17.8 mV 0x00 : 0.875 V 0x01 : 0.8928 V ... 0x7C : 3.082 V 0x7D : 3.10 V 0x7E: Not Supported 0x7F: Not Supported |
| Bit 7 | Not used | R | 0 | |

8.5.56 VSIOVAL Register (address = 0x40) [reset = 00110100]
Figure 72. VSIOVAL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|-------------|-----|-----|-----|-----|-----|-----|
| Field Name | Not used | IOVOLT[6:0] | | | | | | |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 61. VSIOVAL Register Description⁽¹⁾⁽²⁾

| Bit | Field | Type | Reset | Description |
|------------|-------------|------|---------|--|
| Bits [6:0] | IOVOLT[6:0] | R/W | 0110100 | The VR output voltage range is from 875 mV to 3.1 V for codes 0x00 to 0x7D in increments of 17.8 mV 0x00 : 0.875 V 0x01 : 0.8928 V ... 0x7C : 3.082 V 0x7D : 3.10 V 0x7E: Not Supported 0x7F: Not Supported |
| Bit 7 | Not used | R | 0 | |

(1) This register must have same setting as VIOVAL if S_IO LDO is used to power daisy chained IOs in the receive side.

 (2) If there is no I²C daisy chain it can be set freely.

8.5.57 VAVAL Register (address = 0x41) [reset = 00000000]
Figure 73. VAVAL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|------------|-----|-----|-----|-----|-----|-----|
| Field Name | Not used | AVOLT[6:0] | | | | | | |
| Read/Write | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 62. VAVAL Register Description

| Bit | Field | Type | Reset | Description |
|------------|------------|------|---------|--|
| Bits [6:0] | AVOLT[6:0] | R/W | 0000000 | The VR output voltage range is from 875 mV to 3.1 V for codes 0x00 to 0x7D in increments of 17.8 mV 0x00 : 0.875 V 0x01 : 0.8928 V ... 0x7C : 3.082 V 0x7D : 3.10 V 0x7E: Not Supported 0x7F: Not Supported |
| Bit 7 | Not used | R | 0 | |

8.5.58 VDVAL Register (address = 0x42) [reset = 00000000]

Figure 74. VDVAL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|------------|-----|-----|-----|-----|-----|
| Field Name | Not used | Not used | DVOLT[5:0] | | | | | |
| Read/Write | R | R | R/W | R/W | R/W | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 63. VDVAL Register Description

| Bit | Field | Type | Reset | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------|----------------|----------------|--------|---|--------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|-----|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|--|
| Bits [5:0] | DVOLT[5:0] | R/W | 000000 | <p>The VR output voltage range is from 0.9 V to 1.95 V for codes 0x00 to 0x2A in increments of 25 mV. Codes above 0x2A will yield a 1.95-V output.</p> <table><tr><td>0x00 : 0.9 V</td><td>0x10 : 1.295 V</td><td>0x20 : 1.695 V</td></tr><tr><td>0x01 : 0.922 V</td><td>0x11 : 1.322 V</td><td>0x21 : 1.726 V</td></tr><tr><td>0x02 : 0.949 V</td><td>0x12 : 1.350 V</td><td>0x22 : 1.742 V</td></tr><tr><td>0x03 : 0.973 V</td><td>0x13 : 1.369 V</td><td>0x23 : 1.774 V</td></tr><tr><td>0x04 : 0.999 V</td><td>0x14 : 1.399 V</td><td>0x24 : 1.790 V</td></tr><tr><td>0x05 : 1.025 V</td><td>0x15 : 1.420 V</td><td>0x25 : 1.824 V</td></tr><tr><td>0x06 : 1.048 V</td><td>0x16 : 1.452 V</td><td>0x26 : 1.842 V</td></tr><tr><td>0x07 : 1.071 V</td><td>0x17 : 1.474 V</td><td>0x27 : 1.878 V</td></tr><tr><td>0x08 : 1.096 V</td><td>0x18 : 1.497 V</td><td>0x28 : 1.897 V</td></tr><tr><td>0x09 : 1.121 V</td><td>0x19 : 1.521 V</td><td>0x29 : 1.915 V</td></tr><tr><td>0x0A : 1.148 V</td><td>0x1A : 1.545 V</td><td>0x2A : 1.954 V</td></tr><tr><td>0x0B : 1.176 V</td><td>0x1B : 1.571 V</td><td>0x2B : 1.954 V</td></tr><tr><td>0x0C : 1.198 V</td><td>0x1C : 1.597 V</td><td>...</td></tr><tr><td>0x0D : 1.221 V</td><td>0x1D : 1.624 V</td><td>0x3E : 1.954 V</td></tr><tr><td>0x0E : 1.245 V</td><td>0x1E : 1.652 V</td><td>0x3F : 1.954 V</td></tr><tr><td>0x0F : 1.269 V</td><td>0x1F : 1.666 V</td><td></td></tr></table> | 0x00 : 0.9 V | 0x10 : 1.295 V | 0x20 : 1.695 V | 0x01 : 0.922 V | 0x11 : 1.322 V | 0x21 : 1.726 V | 0x02 : 0.949 V | 0x12 : 1.350 V | 0x22 : 1.742 V | 0x03 : 0.973 V | 0x13 : 1.369 V | 0x23 : 1.774 V | 0x04 : 0.999 V | 0x14 : 1.399 V | 0x24 : 1.790 V | 0x05 : 1.025 V | 0x15 : 1.420 V | 0x25 : 1.824 V | 0x06 : 1.048 V | 0x16 : 1.452 V | 0x26 : 1.842 V | 0x07 : 1.071 V | 0x17 : 1.474 V | 0x27 : 1.878 V | 0x08 : 1.096 V | 0x18 : 1.497 V | 0x28 : 1.897 V | 0x09 : 1.121 V | 0x19 : 1.521 V | 0x29 : 1.915 V | 0x0A : 1.148 V | 0x1A : 1.545 V | 0x2A : 1.954 V | 0x0B : 1.176 V | 0x1B : 1.571 V | 0x2B : 1.954 V | 0x0C : 1.198 V | 0x1C : 1.597 V | ... | 0x0D : 1.221 V | 0x1D : 1.624 V | 0x3E : 1.954 V | 0x0E : 1.245 V | 0x1E : 1.652 V | 0x3F : 1.954 V | 0x0F : 1.269 V | 0x1F : 1.666 V | |
| 0x00 : 0.9 V | 0x10 : 1.295 V | 0x20 : 1.695 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x01 : 0.922 V | 0x11 : 1.322 V | 0x21 : 1.726 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x02 : 0.949 V | 0x12 : 1.350 V | 0x22 : 1.742 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x03 : 0.973 V | 0x13 : 1.369 V | 0x23 : 1.774 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x04 : 0.999 V | 0x14 : 1.399 V | 0x24 : 1.790 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x05 : 1.025 V | 0x15 : 1.420 V | 0x25 : 1.824 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x06 : 1.048 V | 0x16 : 1.452 V | 0x26 : 1.842 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x07 : 1.071 V | 0x17 : 1.474 V | 0x27 : 1.878 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x08 : 1.096 V | 0x18 : 1.497 V | 0x28 : 1.897 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x09 : 1.121 V | 0x19 : 1.521 V | 0x29 : 1.915 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0A : 1.148 V | 0x1A : 1.545 V | 0x2A : 1.954 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0B : 1.176 V | 0x1B : 1.571 V | 0x2B : 1.954 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0C : 1.198 V | 0x1C : 1.597 V | ... | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0D : 1.221 V | 0x1D : 1.624 V | 0x3E : 1.954 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0E : 1.245 V | 0x1E : 1.652 V | 0x3F : 1.954 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0F : 1.269 V | 0x1F : 1.666 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Bits [7:6] | Not used | R | 00 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

8.5.59 S_I2C_CTL Register (address = 0x43) [reset = 00000000]

Figure 75. S_I2C_CTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|----------|---------|----------|
| Field Name | Not used | Not used | Not used | Not used | Not used | Not used | S_EN_IO | S_EN_I2C |
| Read/Write | R | R | R | R | R | R | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 64. S_I2C_CTL Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|--------|--|
| Bit 0 | S_EN_I2C | R/W | 0 | Connects SDA and SCL pins to GPIO1 and GPIO2 pins ⁽¹⁾ |
| Bit 1 | S_EN_IO | R/W | 0 | <p>Enables S_IO_OUT LDO</p> <p>0: Output disabled</p> <p>1: Output enabled</p> |
| Bits [7:2] | Not used | R | 000000 | |

(1) GPIO1 and GPIO2 IOs should be set to 'inputs, no pull-up'.

8.5.60 VCMCTL Register (address = 0x44) [reset = 00000000]
Figure 76. VCMCTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|----------|----------|--------|
| Field Name | Not used | Not used | Not used | Not used | Not used | Not used | Not used | ENABLE |
| Read/Write | R | R | R | R | R | R | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 65. VCMCTL Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|---------|--|
| Bit 0 | ENABLE | R/W | 0 | Enables VCM_OUT LDO 0: Output disabled 1: Output enabled |
| Bits [7:1] | Not used | R | 0000000 | |

8.5.61 VAUX1CTL Register (address = 0x45) [reset = 00000000]
Figure 77. VAUX1CTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|----------|----------|--------|
| Field Name | Not used | Not used | Not used | Not used | Not used | Not used | Not used | ENABLE |
| Read/Write | R | R | R | R | R | R | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 66. VAUX1CTL Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|---------|---|
| Bit 0 | ENABLE | R/W | 0 | Enables AUX1_OUT LDO 0: Output disabled 1: Output enabled |
| Bits [7:1] | Not used | R | 0000000 | |

8.5.62 VAUX2CTL Register (address = 0x46) [reset = 00000000]
Figure 78. VAUX2CTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|----------|----------|--------|
| Field Name | Not used | Not used | Not used | Not used | Not used | Not used | Not used | ENABLE |
| Read/Write | R | R | R | R | R | R | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 67. VAUX2CTL Register Description

| Bit | Field | Type | Reset | Description |
|------------|----------|------|---------|---|
| Bit 0 | ENABLE | R/W | 0 | Enables AUX2_OUT LDO 0: Output disabled 1: Output enabled |
| Bits [7:1] | Not used | R | 0000000 | |

8.5.63 VACTL Register (address = 0x47) [reset = 00000000]

Figure 79. VACTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|----------|----------|-----|--------|
| Field Name | Not used | Not used | Not used | Not used | Not used | Not used | TSD | ENABLE |
| Read/Write | R | R | R | R | R | R | R | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 68. VACTL Register Description

| Bit | Field | Type | Reset | Description |
|------------|--------------------|------|--------|---|
| Bit 0 | ENABLE | R/W | 0 | Enables ANA_OUT LDO 0: Output disabled 1: Output enabled |
| Bit 1 | TSD ⁽¹⁾ | R | 0 | Global Thermal Shutdown status (a combination of all the LDOs) 0 : LDO thermal shutdown not active. 1: LDO thermal shutdown active. |
| Bits [7:2] | Not used | R | 000000 | |

(1) The TSD bit is a latched status signal. If the thermal shutdown event is no longer present, this bit can be cleared by either a reset or by masking the TSD_FLAG in the INTMASK register .

8.5.64 VDCTL Register (address = 0x48) [reset = 00000100]

Figure 80. VDCTL Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|----------|----------|----------|----------|-----|------------|------------|--------|
| Field Name | Not used | Not used | Not used | Not used | TSD | EN_PLL_CLK | FORCED_PWM | ENABLE |
| Read/Write | R | R | R | R | R | R/W | R/W | R/W |
| Reset Value | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

LEGEND: R/W = Read/Write; R = Read only

Table 69. VDCTL Register Description⁽¹⁾

| Bit | Field | Type | Reset | Description |
|------------|------------|------|-------|---|
| Bit 0 | ENABLE | R/W | 0 | CORE VR Enable Control 0: Output disabled 1: Output enabled |
| Bit 1 | FORCED_PWM | R/W | 0 | CORE VR PWM/PFM Control 0: Regulator operates in low power drive mode 1: Regulator operates in nominal power mode |
| Bit 2 | EN_PLL_CLK | R/W | 1 | CORE VR Clock Control 0: Internal oscillator 1: PLL clock |
| Bit 3 | TSD | R | 0 | CORE VR thermal shutdown status (this bit will only be set when the max temperature is exceed and the converter is in PWM mode) 0: Buck thermal shutdown not active. 1: Buck thermal shutdown active. |
| Bits [7:4] | Not used | R | 0000 | |

(1) CLK control is not glitchless and should be done before enabling buck.

8.5.65 RESET Register (address = 0x50) [reset = N/A]

Figure 81. RESET Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|------------|-----|-----|-----|-----|-----|-----|-----|
| Field Name | RESET[7:0] | | | | | | | |
| Read/Write | W | W | W | W | W | W | W | W |
| Reset Value | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

LEGEND: W = Write

Table 70. RESET Register Description

| Bit | Field | Type | Reset | Description |
|------------|------------|------|-------|---|
| Bits [7:0] | RESET[7:0] | W | N/A | Force software reset when FF is writtern. Self clearing register. |

8.5.66 REVID Register (address = 0xFF) [reset = 00100000]

Figure 82. REVID Register Format

| Data Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------------|-------------|----|----|----------|----|----------|----|----|
| Field Name | VENDOR[2:0] | | | MRV[1:0] | | LRV[2:0] | | |
| Read/Write | R | R | R | R | R | R | R | R |
| Reset Value | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

LEGEND: R = Read only

Table 71. REVID Register Description

| Bit | Field | Type | Reset | Description |
|------------|-------------|------|-------|---|
| Bits [2:0] | LRV[2:0] | R | 001 | Minor revision number : 000 = xp0 where x = MRV[1:0] 001 = xp1 where x = MRV[1:0] 010 = xp2 where x = MRV[1:0] 011 = xp3 where x = MRV[1:0] |
| Bits [4:3] | MRV[1:0] | R | 00 | Major revision number : 00 = 1py where y = LRV[2:0] 01 = 2py where y = LRV[2:0] 10 = 3py where y = LRV[2:0] 11 = 4py where y = LRV[2:0] |
| Bits [7:5] | VENDOR[2:0] | R | 001 | Vendor code : 001=TI |

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The target application for this device is to power a camera module in portable computers and tablets. The recommendations given in the following section are based on the target application.

9.2 Typical Application

The following figure shows the application schematic for the TPS68470 PMIC. For recommended component values refer to [Table 73](#).

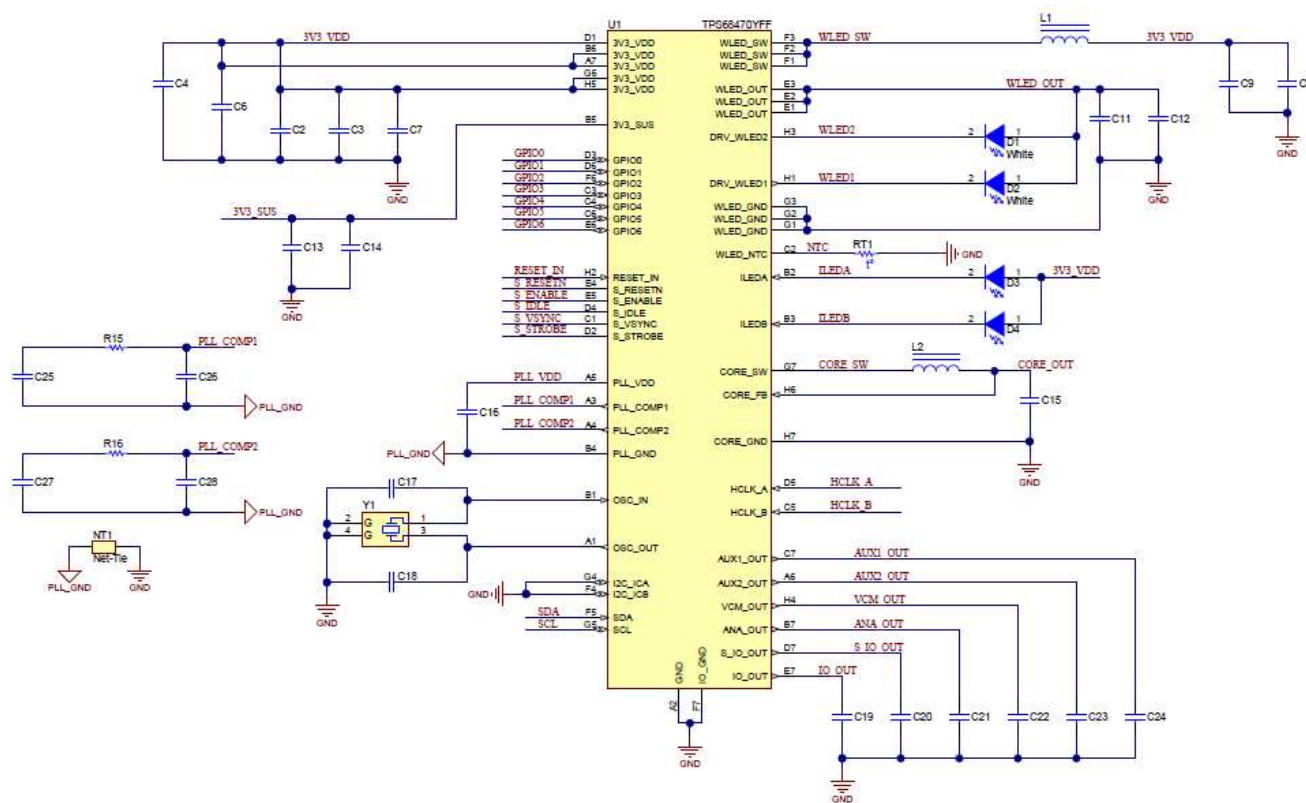


Figure 83. Application Schematic for the TPS68470 (refer to [Table 73](#) for values)

Typical Application (continued)

9.2.1 Design Requirements

Table 72. Design Parameters

| PARAMETER | VOLTAGE |
|---|-----------------------------|
| Input Voltage Range (3V3_VDD and 3V3_SUS) | 3.3V |
| Buck Output Voltage | Default Setting = Off |
| Boost Output Voltage | Default Setting = Off |
| LDO_IO Output Voltage | Default Setting = On (1.8V) |
| LDO_ANA Output Voltage | Default Setting = Off |
| LDO_S_IO Output Voltage | Default Setting = Off |
| LDO_VCM Output Voltage | Default Setting = Off |
| LDO_AUX1 Output Voltage | Default Setting = Off |
| LDO_AUX2 Output Voltage | Default Setting = Off |

9.2.2 Detailed Design Procedure

This section describes the application design procedure for the TPS68470 camera module PMIC. It covers the external component selection for the specified application requirements.

9.2.2.1 Core Buck Design

There are three components required for the buck to operate properly: inductor, output capacitor, and input capacitor. The inductor and output capacitor form an output filter that averages the switch node into a clean regulated supply. The input capacitor supplies the instantaneous current demand of the converter while reducing the noise injected onto the input supply voltage for the other loads.

9.2.2.1.1 Inductor Selection

The CORE_SW pin is the switch node of the converter to which the output inductor is connected. The other end of the inductor connects to the output capacitor.

The inductor value affects the peak-to-peak ripple current, the PFM-to-PWM transition point, the output voltage ripple and the efficiency. In addition, the inductor selected has to be rated for the appropriate saturation current, core losses and DC resistance (DCR). The inductor ripple current decreases with higher inductance and increases with higher V_{IN} . For the CORE buck converter, it is recommended to use an inductor with an inductance range of 1.0 μH to 2.2 μH and with the appropriate current rating for the application.

Use the equation below to calculate the theoretical desired inductance value that fits the application.

$$L_T = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times K_{IND} \times I_{MAX} \times f_{SW}} \quad (3)$$

Where:

I_{MAX} is the maximum DC load current of the application.

V_{OUT} is the typical output voltage of the voltage rail.

V_{IN} is the input voltage to the converter. For this calculation, use the expected maximum input voltage.

f_{sw} is the typical switching frequency of the converter.

K_{IND} is the desired ripple current divided by I_{MAX} . Typically between 0.2 and 0.4.

L_T is the theoretical inductance of the desired inductor.

With the chosen inductance value, the peak current, I_{LMAX} , for the inductor in steady state operation can be calculated using the equations below. The rated saturation current of the inductor must be higher than the I_{LMAX} current.

$$I_{Lmax} = I_{MAX} + \frac{I_{Lripple}}{2} \quad (4)$$

$$I_{L\text{ripple}} = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{V_{\text{IN}} \times f_{\text{SW}} \times L} \quad (5)$$

Where:

$I_{L\text{max}}$ is the maximum current through the inductor.

$I_{L\text{ripple}}$ is the ripple current through the inductor in PWM mode.

L is the typical inductance of the selected inductor.

In DC/DC converter applications, the efficiency is affected by the inductor core losses and by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a low DCR value and low core losses at the typical V_{IN} , V_{OUT} and switching frequency. Increasing the inductor value produces lower ripple and peak currents while increasing efficiency but, degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

At low load currents, the switching and core losses are reduced by the PFM mode feature. The approximate transition point of the converter between PFM and PWM is when the DC load current is equal to 50% of $I_{L\text{ripple}}$.

The table at the end of this section lists the recommended inductors for the CORE buck converter.

9.2.2.1.2 Output Capacitor

The output capacitor completes the LC output filter. It is important to choose an output capacitor that suits the application and inductor selection for stability, output voltage ripple, and specific application requirements such as size and cost. Ceramic capacitors with low ESR values provide the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. In order to achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

For the output capacitor of the CORE buck converter, the use of a small ceramic capacitor placed as close as possible to the inductor and the respective CORE_GND pin of the IC is recommended. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the inductor and the respective CORE_GND pin of the IC.

Refer to [Table 73](#) for recommended values.

Use the equation below to calculate the maximum ESR of the output capacitor allowed in-order to meet the maximum output voltage ripple.

$$R_{\text{ESR}} < \frac{V_{\text{OUTTripple}}}{I_{L\text{ripple}}} \quad (6)$$

Where:

$V_{\text{OUTTripple}}$ is the maximum output voltage ripple allowed by the application.

R_{ESR} is the ESR of the output capacitance.

9.2.2.1.3 Input Capacitor

Due to the nature of the switching converter with a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering. Be sure to size the ceramic capacitor to achieve the recommended input capacitance. Place the ceramic capacitor as close as possible to the respective 3V3_VDD and CORE_GND pins of the IC.

$$C_{IN} > \frac{I_{OUT} \times V_{OUT}}{\Delta V_{IN} \times V_{IN} \times f_{SW}} \quad (7)$$

Where:

ΔV_{IN} is the maximum input voltage ripple allowed by the application.

C_{IN} is the input capacitance.

9.2.2.2 WLED Boost Design

There are three components required for the boost to operate properly: inductor, output capacitor, and input capacitor.

9.2.2.2.1 Inductor Selection

The WLED_SW pin is the switch node of the converter which connects to the inductor of the WLED boost converter. The inductor must be connected between the WLED_SW pin and the input capacitor. Use the equation below to calculate the theoretical desired inductance for the inductor.

$$L_T = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{K_{IND} \times I_{MAX} \times f_{SW} \times V_{OUT}} \quad (8)$$

Where:

I_{MAX} is the maximum DC load current of the application.

V_{OUT} is the typical output voltage of the voltage rail.

V_{IN} is the input voltage to the converter.

f_{SW} is the typical switching frequency of the boost converter.

K_{IND} is the desired ripple current divided by I_{MAX} . Typically between 0.2 and 0.4.

L_T is the theoretical inductance of the desired inductor.

With the chosen inductance value, the peak current, I_{LMAX} , for the inductor in steady state operation can be calculated using the equations below. The rated saturation current of the inductor must be higher than the I_{LMAX} current.

$$I_{Lmax} = \frac{I_{MAX} + V_{OUT}}{V_{IN}} + \frac{I_{Lripple}}{2} \quad (9)$$

$$I_{Lripple} = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT} \times f_{SW} \times L} \quad (10)$$

Where:

I_{Lmax} is the maximum current through the inductor.

$I_{Lripple}$ is the ripple current through the inductor in PWM mode.

L is the typical inductance of the selected inductor.

In DC/DC converter applications, the efficiency is affected by the inductor core losses and by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a low DCR value and low core losses at the typical V_{IN} , V_{OUT} and switching frequency. Increasing the inductor value produces lower ripple and peak currents while increasing efficiency but, degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The table at the end of this section lists the recommended inductors for the WLED boost converter.

9.2.2.2.2 Output Capacitor

It is important to choose an output capacitor that suits the application and inductor selection for stability, output voltage ripple, and specific application requirements such as size and cost. Ceramic capacitors with low ESR values provide the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. In order to achieve specified regulation performance and low output voltage ripple, the DC-bias characteristic of ceramic capacitors must be considered. The effective capacitance of ceramic capacitors drops with increasing DC bias voltage.

For the output capacitor of the boost converter, the use of a small ceramic capacitor placed as close as possible to the inductor and the respective WLED_GND pin of the IC is recommended. If, for any reason, the application requires the use of large capacitors which cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the WLED_OUT pins and the respective WLED_GND pin of the IC.

Use the equation below to calculate the minimum output capacitance with regards to load transient performance.

Refer to [Table 73](#) for recommended values.

9.2.2.2.3 Input Capacitor

Due to the nature of the switching converter with a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. To achieve the low ESR requirement, a ceramic capacitor is recommended. However, the voltage rating and DC bias characteristic of ceramic capacitors need to be considered. The input capacitor can be increased without any limit for better input voltage filtering. Be sure to size the ceramic capacitor to achieve the recommended input capacitance. Place the ceramic capacitor as close as possible to the inductor and WLED_GND pins of the IC.

Refer to [Table 73](#) for recommended values.

9.2.2.3 LDOs Capacitor Selection

It is recommended to use at least 1.0 μF of output capacitance for each LDO output. The input capacitance for each LDO can be combined into one ceramic capacitor of at least 4.7 μF . For both the input and output capacitors, it is recommended to use small ceramic capacitors placed as close as possible to the IC VDD and GND pins. X5R or X7R dielectric capacitors are required for proper operation over temperature.

9.2.2.4 LED Selection

For the indicator LED selection, it is best to choose LEDs with small maximum V_f to maximize LED control head room. A red LED with a maximum V_f of 2.2V is a good choice.

For the WLED selection, it is best to choose a WLED with a maximum current of at least 1A and small to fit the form factor of the application design.

9.2.2.5 Recommended External Components

The following external components are recommended for use with the TPS68470.

Table 73. List of External Components

| BLOCK | COMPONENT | COMPONENT NUMBER | MANUFACTURER | VALUE | SERIES | DIMENSIONS |
|---------------|----------------------|------------------|--------------|----------------|------------------------------|-----------------------|
| CORE BUCK | Inductor | L2 | Toko | 1.0 μ H | 1269AS-H-1R0M | 2.5 x 2.0 x 1.0 mm |
| | | | Taiyo Yuden | 1.5 μ H | CKP2012N1R5M | 2.0 x 1.25 x 1.0 mm |
| | | | | 1.0 μ H | NR3010_1R0 | 3.0 x 3.0 x 1.0 mm |
| | Output capacitor | C15 | | 4.7 μ F | X5R or X7R ceramic capacitor | |
| | Input capacitor | C2 | | 10 μ F | X5R or X7R ceramic capacitor | |
| WLED BOOST | Inductor | L1 | TDK | 2.2 μ H | SMP3012 | 3.2 x 3.0 x 1.2 mm |
| | | | | 2.2 μ H | SMP3015 | 3.2 x 3.0 x 1.5 mm |
| | | | | 2.2 μ H | SMP4012 | 4.4 x 4.1 x 1.2 mm |
| | Output capacitor | C11, C12 | | 10 μ F | X5R or X7R ceramic capacitor | |
| | Input capacitor | C1, C9 | | 10 μ F | X5R or X7R ceramic capacitor | |
| WLED | Flash LEDs | D1, D2 | Everlight | | ELCH08-5070J6J8284110-N0 | 2.04 x 1.64 x 0.75 mm |
| All LDO's | Output capacitor | C19 - C24 | | 1.0 μ F | X5R or X7R ceramic capacitor | |
| CLK generator | XTAL | Y1 | Pericom | | FL2000044 | 3.2 x 2.5 x 0.65mm |
| | | | Epson | 24MHz | FA - 128 | 2.0 x 1.6 x 0.5 mm |
| | | | TXC | | TXC – 7M | 3.2 x 2.5 x 0.7 mm |
| | Comp capacitors | C26, C28 | | 2.2 nF | X5R or X7R ceramic capacitor | |
| | | C25, C27 | | 10 nF | X5R or X7R ceramic capacitor | |
| | Comp resistors | R15, R16 | | 8.2 k Ω | | |
| 3V3_SUS | Supply capacitor | C13 | | 4.7 μ F | X5R or X7R ceramic capacitor | |
| | Decoupling capacitor | C14 | | 0.1 μ F | X5R or X7R ceramic capacitor | |
| 3V3_VDD | Supply capacitors | C3 | | 4.7 μ F | X5R or X7R ceramic capacitor | |
| | Decoupling capacitor | C4, C6, C7 | | 0.1 μ F | X5R or X7R ceramic capacitor | |

9.2.3 Application Performance Graphs

Table 74. Table of Graphs

| DESCRIPTION | | REFERENCE |
|-------------|---|---------------------------|
| Core Buck | Efficiency vs. Output Current | Figure 84 |
| | Load Regulation vs. Output Current | Figure 85 |
| | Output Ripple Voltage, $I_{OUT} = 500$ mA | Figure 86 |
| | Load Transient | Figure 87 |
| WLED Boost | Efficiency vs. Output Current | Figure 88 |
| | Load Regulation vs. Output Current | Figure 89 |
| | Output Ripple Voltage, $I_{OUT} = 500$ mA | Figure 90 |
| | Load Transient | Figure 91 |

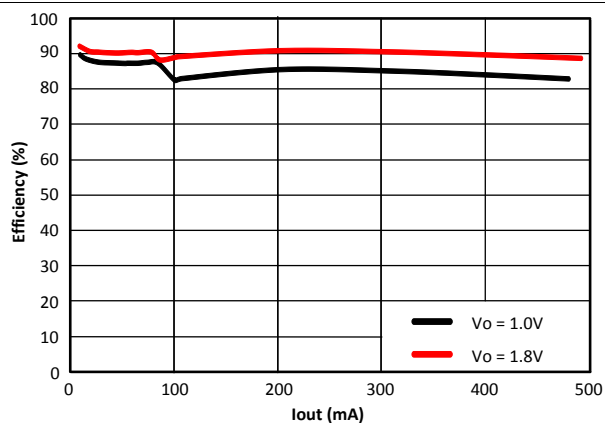


Figure 84. Core Buck Efficiency

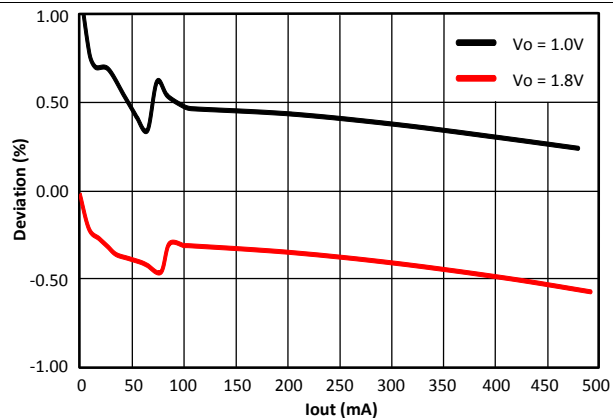


Figure 85. Core Buck Load Regulation

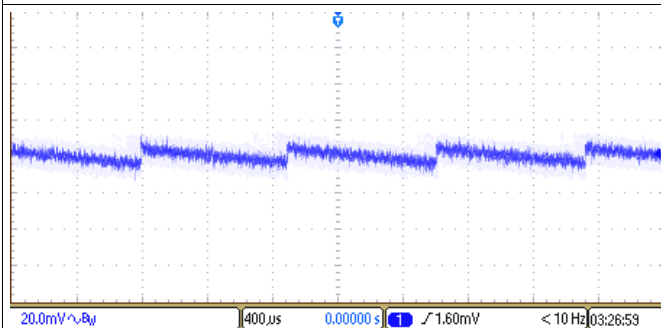


Figure 86. Core Buck Output Ripple

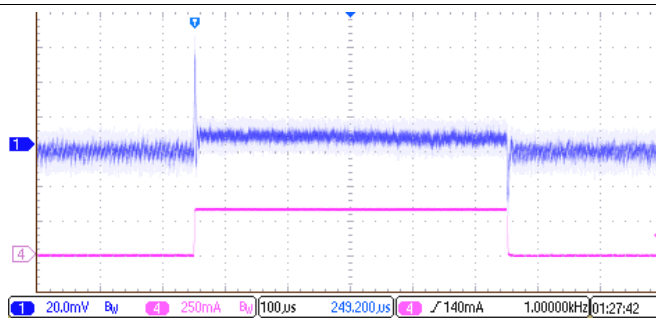


Figure 87. Core Buck Load Transient

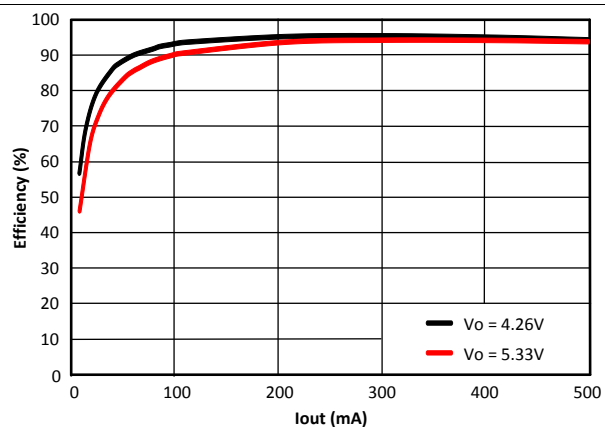


Figure 88. WLED Boost Efficiency

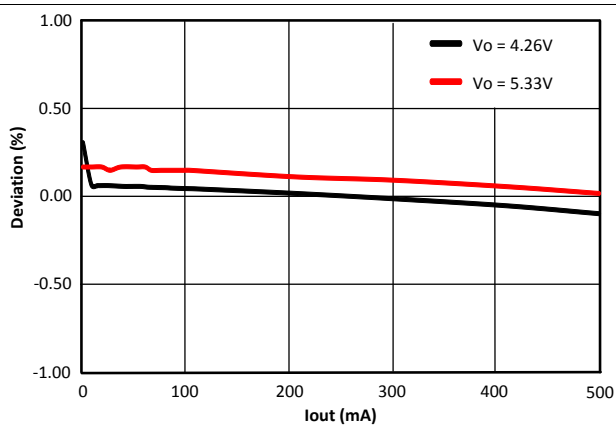


Figure 89. WLED Boost Load Regulation

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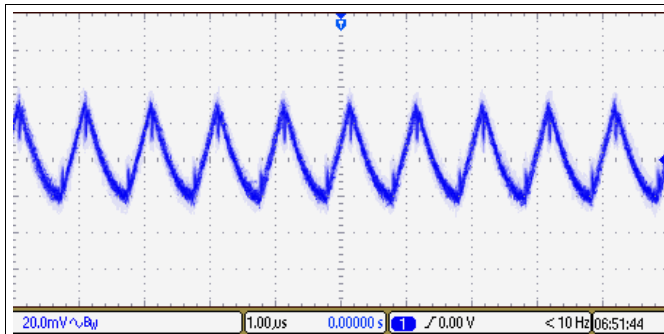


Figure 90. WLED Boost Output Ripple

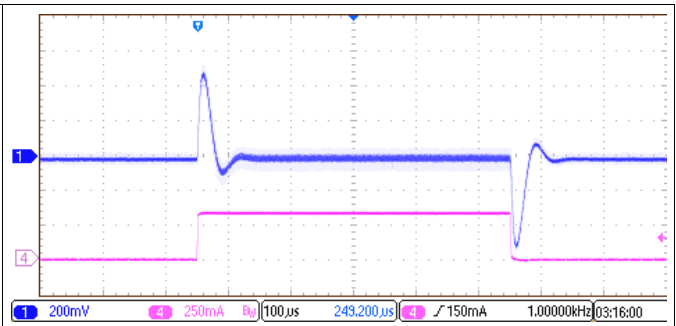


Figure 91. WLED Boost Load Transient

10 Power Supply Recommendations

The TPS68470 has two power supply input pins, 3V3_SUS and 3V3_VDD. Both should be well regulated 3.3-V rails. The 3V3_VDD supply must be able to supply the maximum required input current, typically on the order of 5 A.

11 Layout

11.1 Layout Guidelines

Below is the layout check list.

- All input capacitors are placed as close as possible to the IC VIN and GND pins respectfully.
- A small 0.1- μ F decoupling capacitor is recommended on each of the 3V3_VDD and 3V3_SUS pins.
- The cross sectional area loop from the input capacitor to the CORE input and CORE_GND pins is kept minimal.
- Route the feedback signal for the buck next to the current path of the buck converter. This decreases the cross sectional area of the feedback loop, minimizing noise injection into the loop.
- Ensure large planes for current to flow with minimum parasitics for all output rails and 3V3_VDD. Output rails include all LDOs, CORE_OUT, WLED_OUT and WLEDx.
- Ensure large planes for the ground return path for current to flow with minimum parasitics. Also, ground pours on the external and internal layers for ground improve the thermal performance.
- The PLL compensation components should be grounded to PLL_GND. The PLL ground loop must be kept minimal.
- If the GPIO3 pin is being driven with an external clock source, match the impedance of the GPIO3 trace to 50 Ω for best performance.
- Do not route any noise sensitive signals under or next to the inductor for the boost or buck converters. It is best to have a keepout region directly under the inductors or at least ground shielding.
- It is recommended to have the layer nearest to the side with the IC be a solid copper ground pour.

11.2 Layout Example

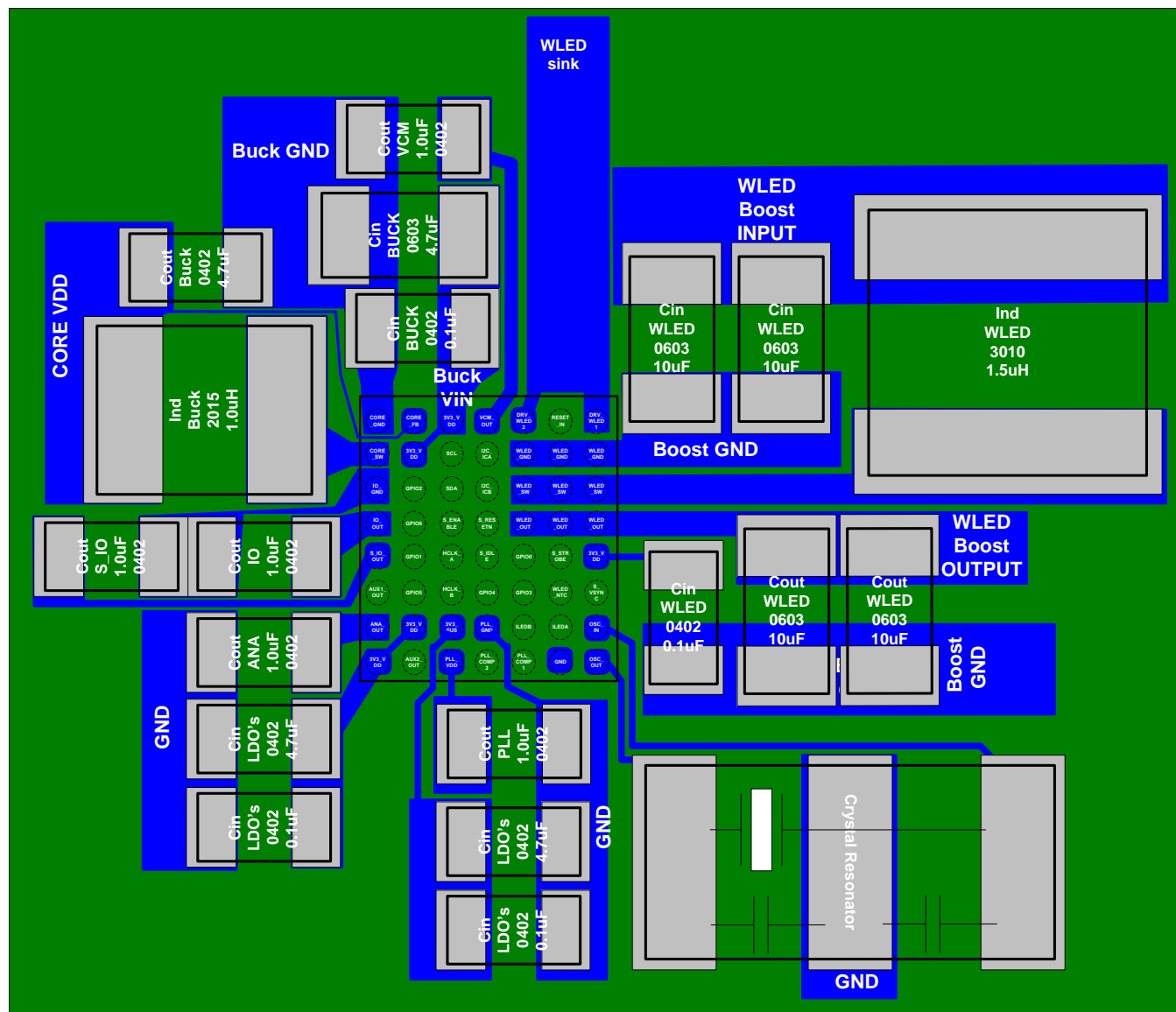


Figure 92. Layout

12 器件和文档支持

12.1 器件支持

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|------------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| TPS68470YFFR | Active | Production | DSBGA (YFF) 56 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | 0 to 85 | TPS68470 |
| TPS68470YFFR.A | Active | Production | DSBGA (YFF) 56 | 3000 LARGE T&R | Yes | SNAGCU | Level-1-260C-UNLIM | 0 to 85 | TPS68470 |
| TPS68470YFFT | Active | Production | DSBGA (YFF) 56 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | 0 to 85 | TPS68470 |
| TPS68470YFFT.A | Active | Production | DSBGA (YFF) 56 | 250 SMALL T&R | Yes | SNAGCU | Level-1-260C-UNLIM | 0 to 85 | TPS68470 |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS68470YFFR | DSBGA | YFF | 56 | 3000 | 330.0 | 12.4 | 3.0 | 3.55 | 0.81 | 8.0 | 12.0 | Q1 |
| TPS68470YFFT | DSBGA | YFF | 56 | 250 | 330.0 | 12.4 | 3.0 | 3.55 | 0.81 | 8.0 | 12.0 | Q1 |

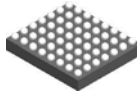
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS68470YFFR | DSBGA | YFF | 56 | 3000 | 335.0 | 335.0 | 25.0 |
| TPS68470YFFT | DSBGA | YFF | 56 | 250 | 335.0 | 335.0 | 25.0 |

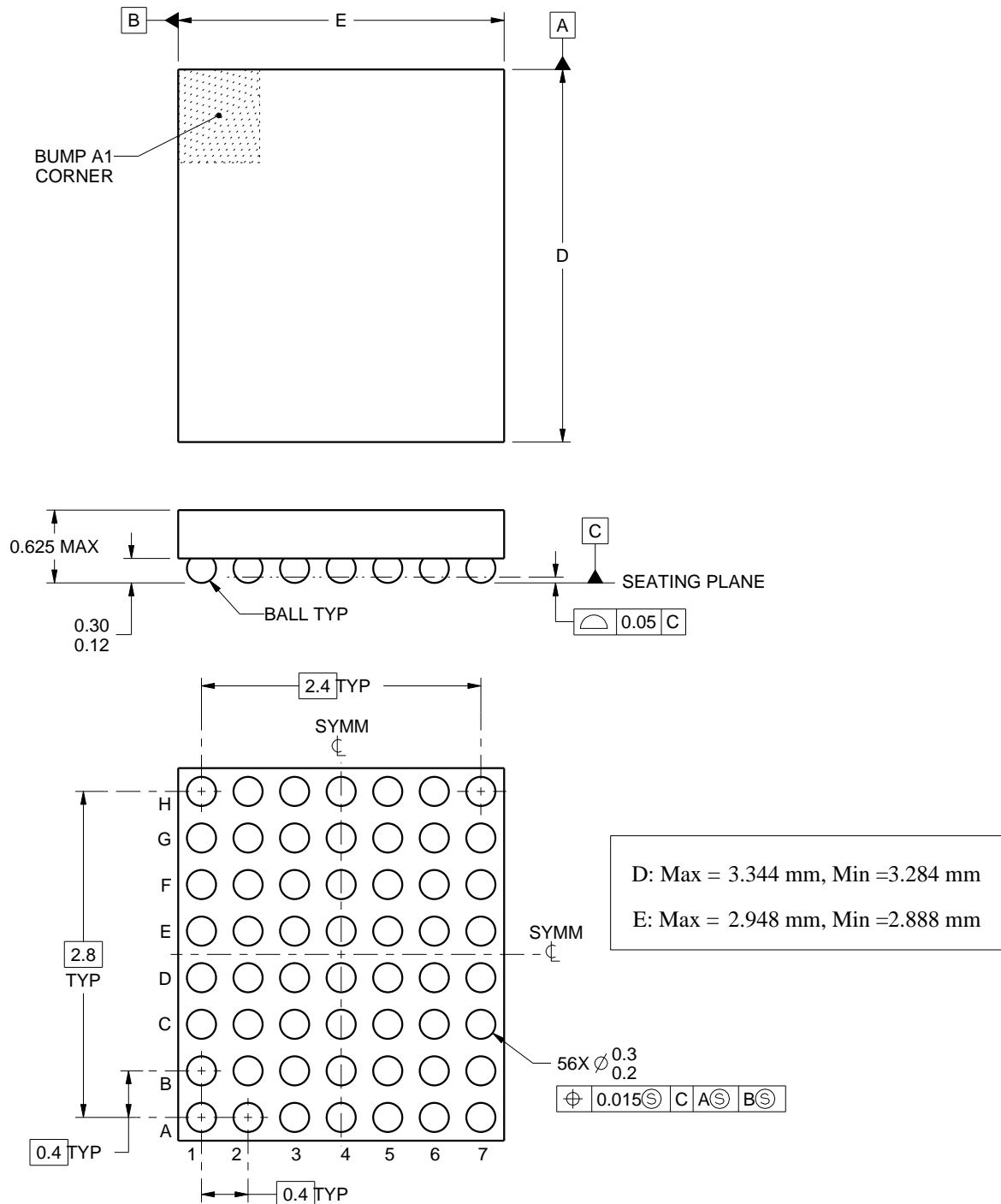
YFF0056



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



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NOTES:

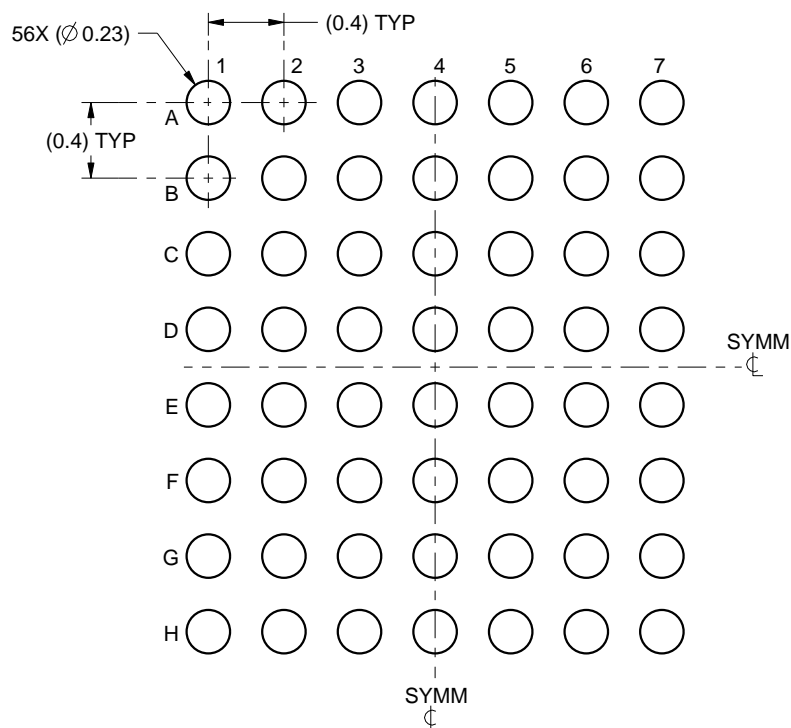
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

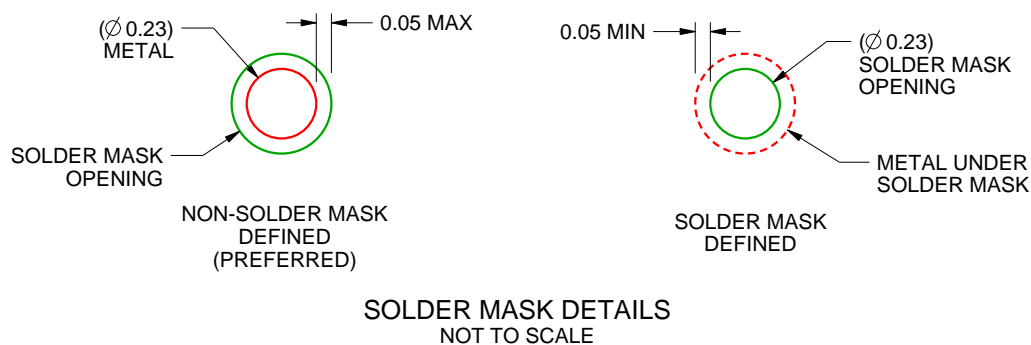
YFF0056

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

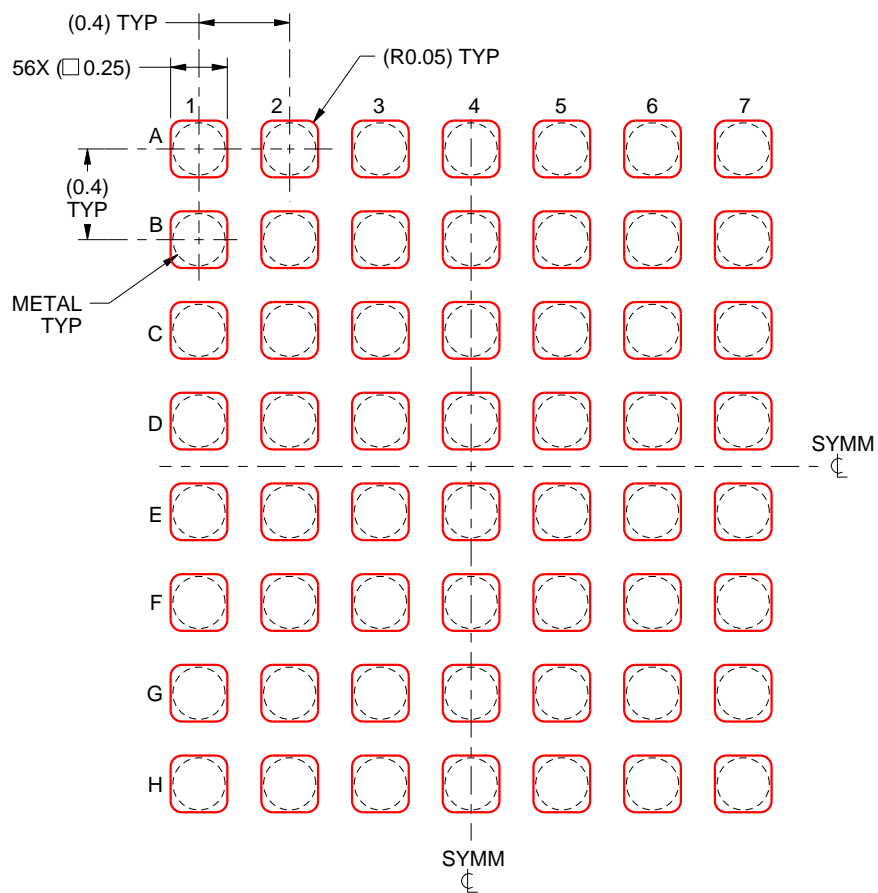
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 (www.ti.com/lit/sbva017).

EXAMPLE STENCIL DESIGN

YFF0056

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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