

## Single-Inductor, Multiple-Output (SIMO) Regulator for AMOLED

### FEATURES

- 2.3-V to 5.5-V Input Voltage Range
- 1% Output Voltage Accuracy
- Low-Noise Operation
- 750-mW Output Power at  $V_{in} = 2.9\text{ V}$
- SIMO Regulator Technology
- Fixed 4.6-V Positive Output Voltage
- Negative Output Voltage Down to  $-6\text{ V}$
- Advanced Power-Save Mode for Light-Load Efficiency

- Out-of-Audio Mode
- Short-Circuit Protection
- Excellent Line Regulation
- Thermal Shutdown
- 3-mm × 3-mm Thin QFN Package

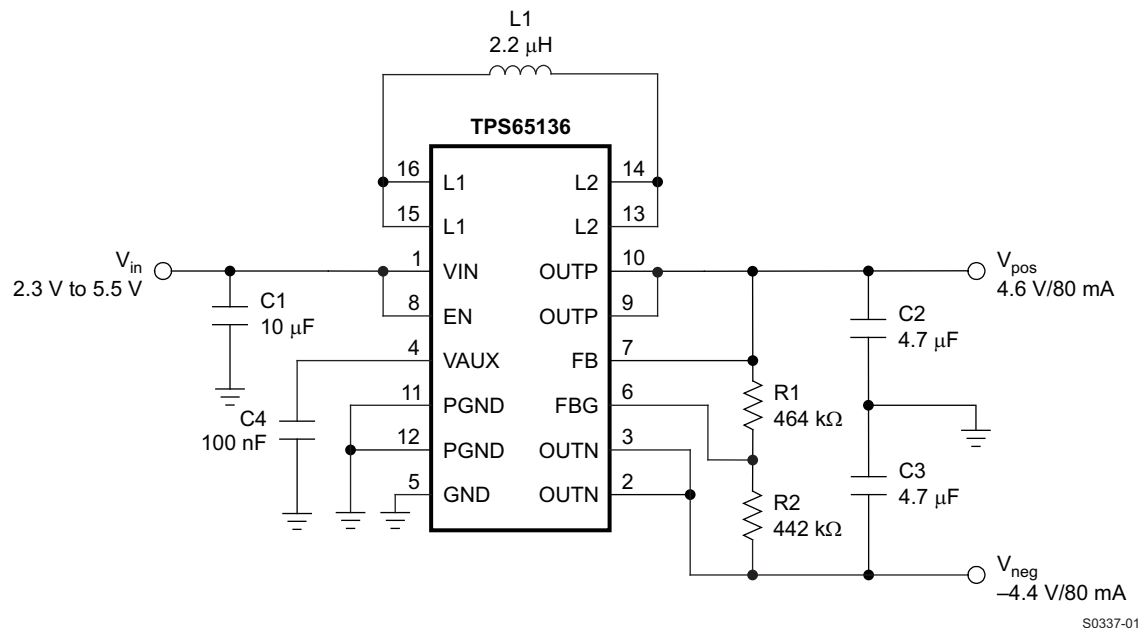
### APPLICATIONS

- Active-Matrix OLED Power Supply

### DESCRIPTION

The TPS65136 is designed to provide best-in-class picture quality for active-matrix OLED (AMOLED) displays that require positive and negative supply rails. With its wide input voltage range, the device is ideally suited for AMOLED displays, which are used in mobile phones or SmartPhone™ devices. With the new single-inductor multiple-output (SIMO) technology, the smallest possible solution size is achieved. The device operates with a buck-boost topology and generates both positive and negative output voltages above or below the input voltage rail. The SIMO technology enables excellent line and load regulation. Excellent line-transient regulation is required to avoid disturbance of the AMOLED display as a result of input voltage variations that occur during transmit periods in mobile communication systems.

### TYPICAL APPLICATION



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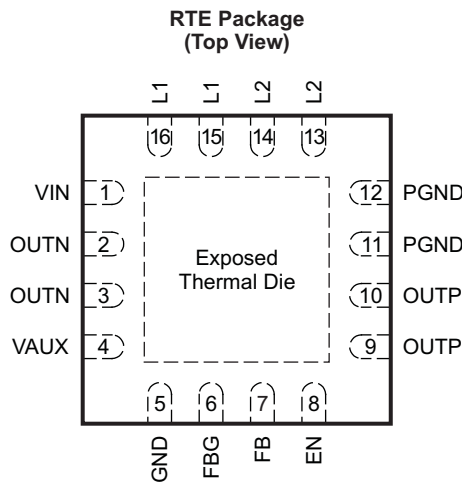
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**ORDERING INFORMATION<sup>(1)</sup>**

T <sub>A</sub>	OPTIONS	ORDERING P/N	PACKAGE	PACKAGE MARKING
–40°C to 85°C	4.6 V fixed <sup>(2)</sup>	TPS65136RTE	RTE	CCO

- (1) The RTE package is available in tape and reel. Add R suffix (TPS65136RTER) to order quantities of 3000 parts per reel. For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at [www.ti.com](http://www.ti.com).
- (2) Contact the factory for other output voltage options.

**16-Terminal TQFN PACKAGE**

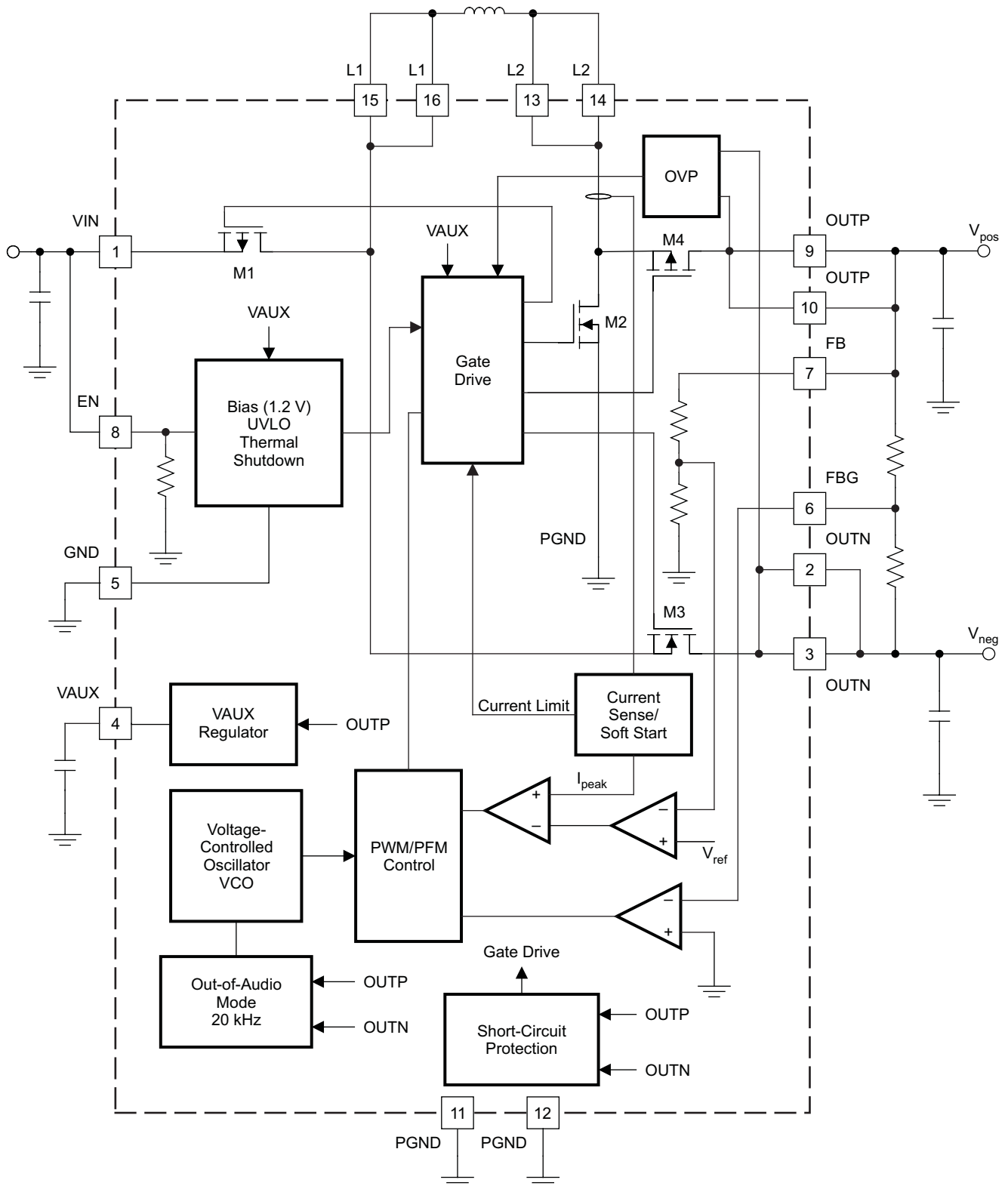


P0081-01

**TERMINAL FUNCTIONS**

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	8	I	Input pin to enable the device. Pulling this pin high enables the device. This pin has an internal 500-kΩ pulldown resistor.
FB	7	I	Feedback regulation input for the positive output voltage rail
FBG	6	I	Feedback regulation input
GND	5	–	Analog ground
L1	13, 14	I/O	Inductor terminal
L2	15, 16	I/O	Inductor terminal
OUTN	2, 3	O	Negative output
OUTP	9, 10	O	Positive output
PGND	11, 12	–	Power GND
VAUX	4	O	Reference voltage output. This pin requires a 100-nF capacitor for stability.
VIN	1	I	Input supply
Exposed thermal die		–	Connect this pad to analog GND.

FUNCTIONAL BLOCK DIAGRAM



B0299-01

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

	VALUE	UNIT
Input voltage range VIN <sup>(2)</sup>	–0.3 to 7	V
Voltage range at EN	–0.3 to 7	V
Voltage range at L1, OUTN	–8 to 7	V
Voltage range at FBG	–0.5 to 0.5	V
Voltage range at L2, OUTP, FB	–0.3 to 7	V
ESD rating, HBM	2	kV
ESD rating, MM	200	V
ESD rating, CDM	1	kV
Continuous total power dissipation	See Dissipation Ratings Table	
T <sub>J</sub> Operating junction temperature range	–40 to 150	°C
T <sub>A</sub> Operating ambient temperature range	–40 to 85	°C
T <sub>stg</sub> Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

## DISSIPATION RATINGS

PACKAGE	R <sub>θJA</sub> <sup>(1)</sup>	T <sub>A</sub> ≤ 25°C POWER RATING	T <sub>A</sub> = 70°C POWER RATING	T <sub>A</sub> = 85°C POWER RATING
RTE	40°C/W	2.5 W	1.37 W	1 W

- (1) Thermal resistance measured on a printed circuit board using thermal vias.

## RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
V <sub>in</sub> Input voltage range	2.3		5.5	V
T <sub>A</sub> Operating ambient temperature	–40		85	°C
T <sub>J</sub> Operating junction temperature	–40		125	°C

## ELECTRICAL CHARACTERISTICS

V<sub>in</sub> = 3.7 V, EN = VIN, OUTP = 4.6 V, OUTN = –5.4 V, T<sub>A</sub> = –40°C to 85°C; typical values are at T<sub>A</sub> = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>					
V <sub>in</sub> Input voltage range		2.3		5.5	V
I <sub>Q</sub> Operating quiescent current into V <sub>in</sub>			1.7		mA
I <sub>SD</sub> Shutdown current into V <sub>in</sub>			0.1	2	μA
V <sub>UVLO</sub> Undervoltage lockout threshold	V <sub>in</sub> falling		1.8	2	V
	V <sub>in</sub> rising		2	2.3	
Thermal shutdown			140		°C
Thermal shutdown hysteresis			5		°C
<b>ENABLE</b>					
V <sub>H</sub> Logic high-level voltage	V <sub>in</sub> = 2.5 V to 5.5 V	1.2			V
V <sub>L</sub> Logic low-level voltage	V <sub>in</sub> = 2.5 V to 5.5 V			0.4	V
R Pulldown resistor			500		kΩ
<b>OUTPUT</b>					
OVP <sub>P</sub> Positive overvoltage protection	I <sub>out</sub> = 10 mA	5.5	7		V

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{in} = 3.7\text{ V}$ ,  $EN = VIN$ ,  $OUTP = 4.6\text{ V}$ ,  $OUTN = -5.4\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ ; typical values are at  $T_A = 25^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{outn}$	Negative output voltage range		-2.5		-6	V
$OVP_N$	Negative overvoltage protection			-7.6	-6	V
$I_{mis}$	Output current mismatch $V_{pos}/V_{neg}$		-30%		30%	
$V_{outp}$	Positive output voltage regulation		4.554	4.6	4.646	V
$t_{dly}$	Sequencing delay	$V_{pos}$ start to $V_{neg}$ start	6	8.7	11	ms
$V_{FBG}$	Feedback ground regulation		-10	0	10	mV
$r_{DS(on)}$	M1 MOSFET on-resistance	$I_{sw} = 100\text{ mA}$		200		m $\Omega$
	M2 MOSFET on-resistance	$I_{sw} = 100\text{ mA}$		400		
	M3 MOSFET on-resistance	$I_{sw} = 100\text{ mA}$		900		
	M4 MOSFET on-resistance	$I_{sw} = 100\text{ mA}$		600		
$I_{SW}$	Switch current limit (M2)	$V_{in} = 3.7\text{ V}$	620	700	940	mA
		$V_{in} = 2.5\text{ V}$	720	830	1120	
$P_{out}$	Output power	$V_{pos} - V_{neg} \leq 10\text{ V}$ ; $V_{in} = 2.9\text{ V}$	750			mW
$f_s$	Switching frequency	$I_{out\ neg} = I_{out\ pos} = 30\text{ mA}$		1		MHz
		$I_{out\ neg} = I_{out\ pos} = 0\text{ mA}$		40		kHz
$Vo_{low}$	Output pulldown voltage <sup>(1)</sup>	$EN = GND$ , $I_{out\ neg} = I_{out\ pos} = 1\text{ mA}$		1		V
	Line regulation positive output OUTP	$I_{out\ neg} = I_{out\ pos} = 5\text{ mA}$		0		%/V
	Line regulation negative output OUTN	$I_{out\ neg} = I_{out\ pos} = 5\text{ mA}$		0.008		%/V
	Load regulation positive output OUTP	$V_{in} = 3.7\text{ V}$		0.27		%/A
	Load regulation negative output OUTN	$V_{in} = 3.7\text{ V}$		0.25		%/A

(1) The device actively pulls down the outputs during shutdown. The value specifies the output voltage as a current is forced into the outputs during shutdown.

**TYPICAL CHARACTERISTICS**
**TABLE OF GRAPHS**

		FIGURE
Efficiency	vs load current (2.2 $\mu\text{H}$ )	<a href="#">Figure 1</a>
Efficiency	vs load current (4.7 $\mu\text{H}$ )	<a href="#">Figure 2</a>
Operation at light load current	DCM operation	<a href="#">Figure 3</a>
Operation at high load current	CCM operation	<a href="#">Figure 4</a>
Line transient response	$I_{out} = 30\text{ mA}$	<a href="#">Figure 5</a>
Line transient response	$I_{out} = 50\text{ mA}$	<a href="#">Figure 6</a>
Start-up		<a href="#">Figure 7</a>
Switching frequency	vs load current	<a href="#">Figure 8</a>
Quiescent current	vs input voltage	<a href="#">Figure 9</a>
Maximum output current	2.2 $\mu\text{H}$ , LPS3008-222	<a href="#">Figure 10</a>
Maximum output current	2.2 $\mu\text{H}$ , LPF3010-2R2	<a href="#">Figure 11</a>
Maximum output current	4.7 $\mu\text{H}$ , LPS3008-472	<a href="#">Figure 12</a>
Maximum output current	4.7 $\mu\text{H}$ , LPF3010-4R7	<a href="#">Figure 13</a>

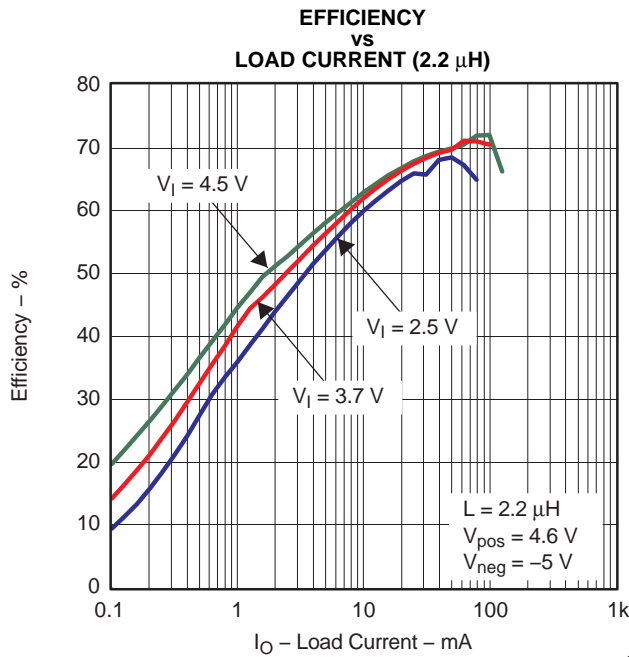


Figure 1.

G001

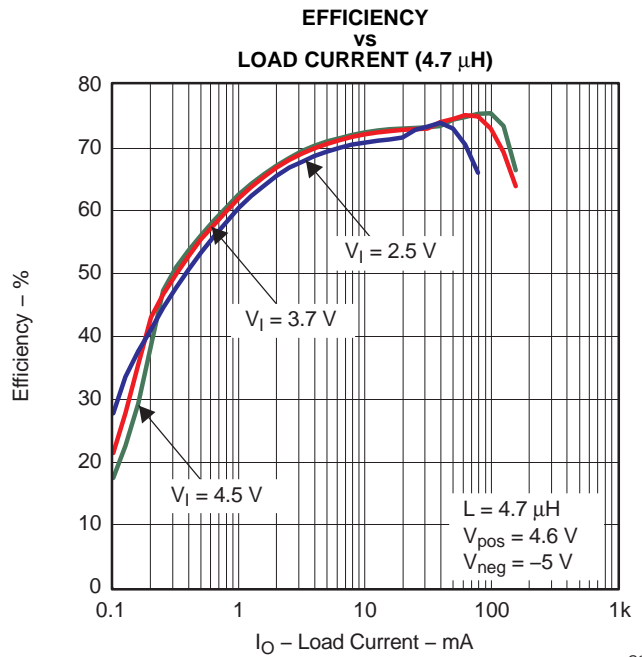


Figure 2.

G002

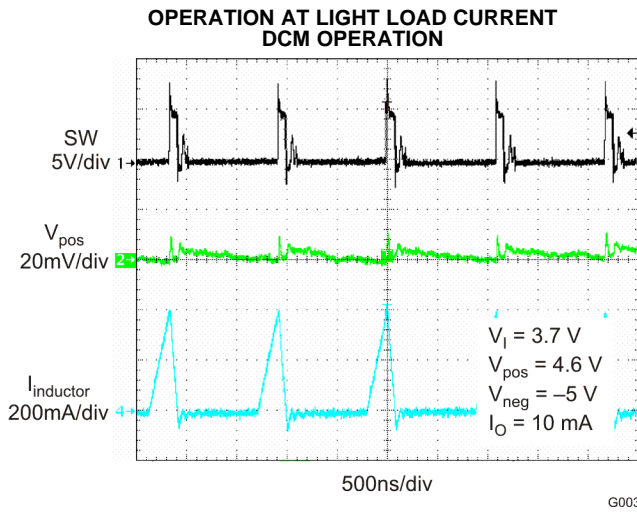


Figure 3.

G003

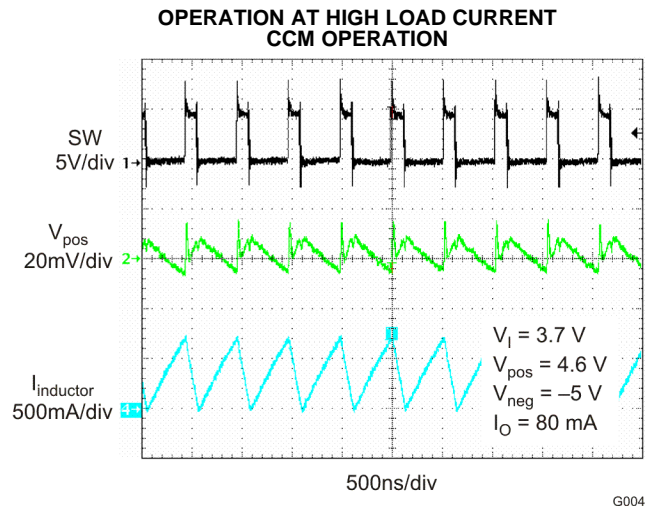


Figure 4.

G004

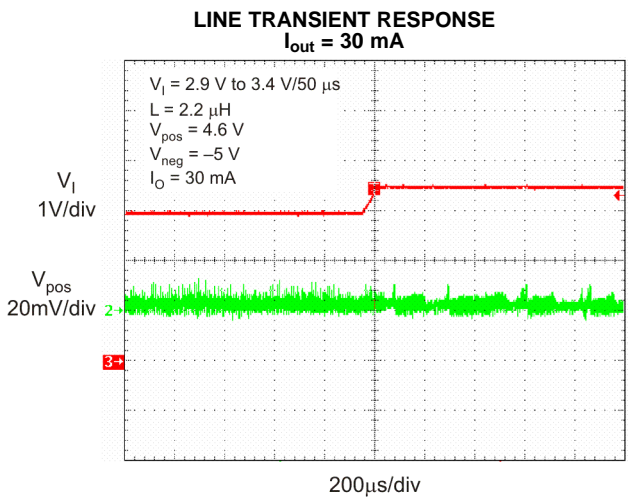


Figure 5.

G005

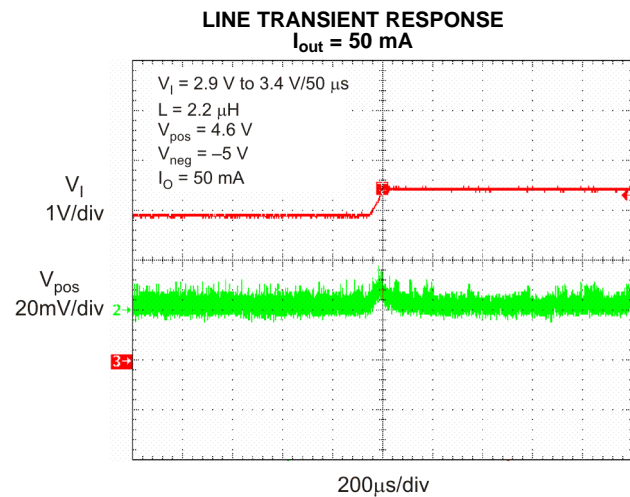


Figure 6.

G006

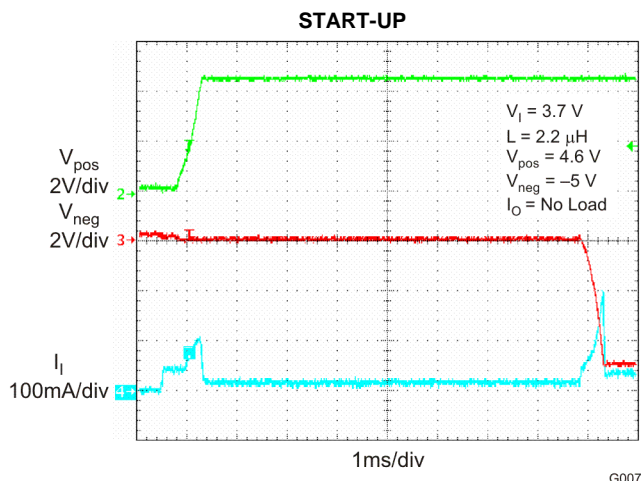


Figure 7.

G007

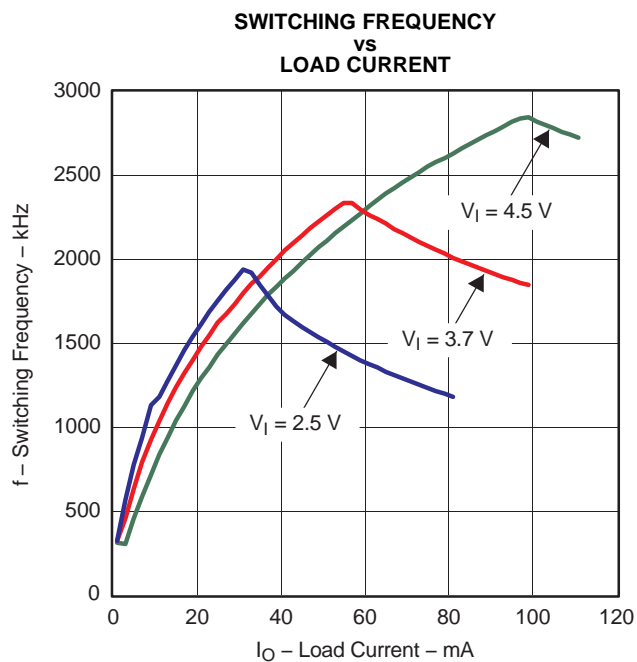


Figure 8.

G008

**QUIESCENT CURRENT  
VS  
INPUT VOLTAGE**

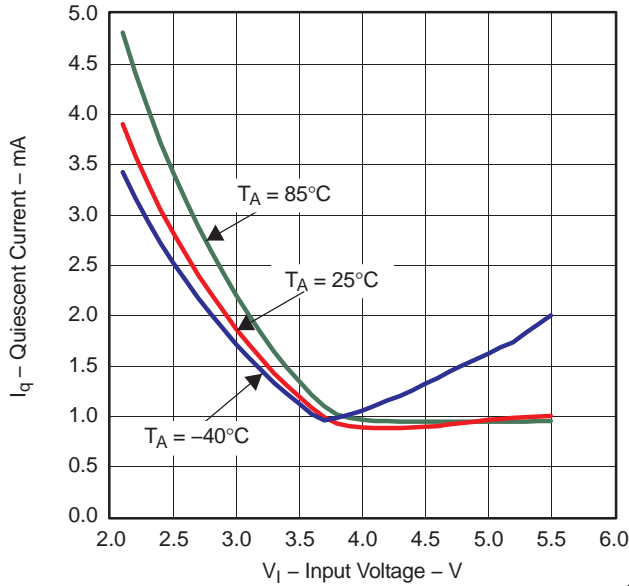


Figure 9.

G009

**MAXIMUM OUTPUT CURRENT  
2.2  $\mu\text{H}$ , LPS3008-222**

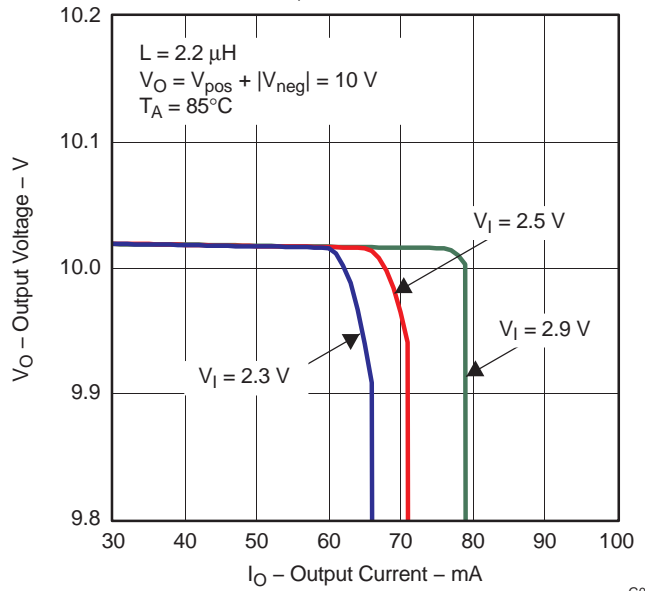


Figure 10.

G010

**MAXIMUM OUTPUT CURRENT  
2.2  $\mu\text{H}$ , LPF3010-2R2**

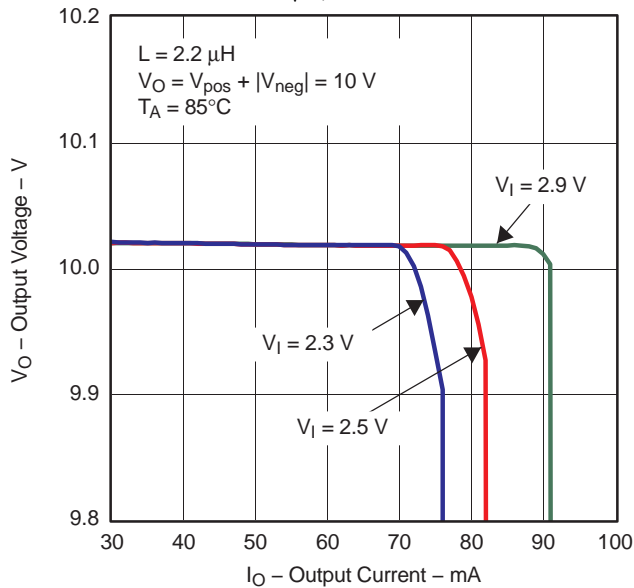


Figure 11.

G011

**MAXIMUM OUTPUT CURRENT  
4.7  $\mu\text{H}$ , LPS3008-472**

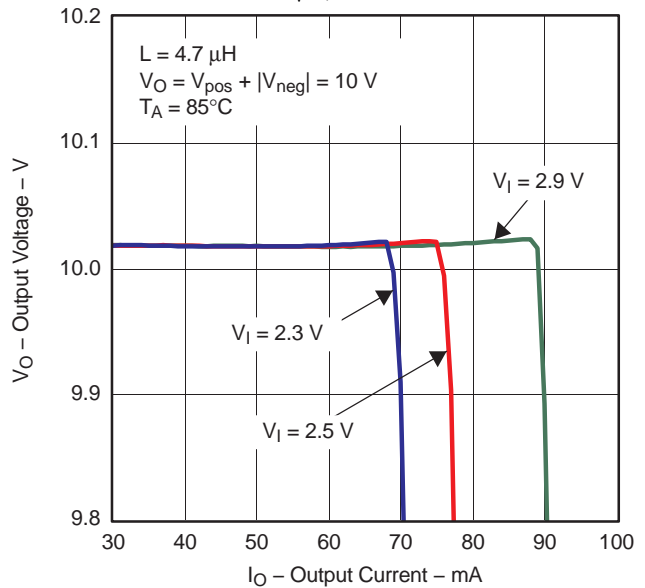
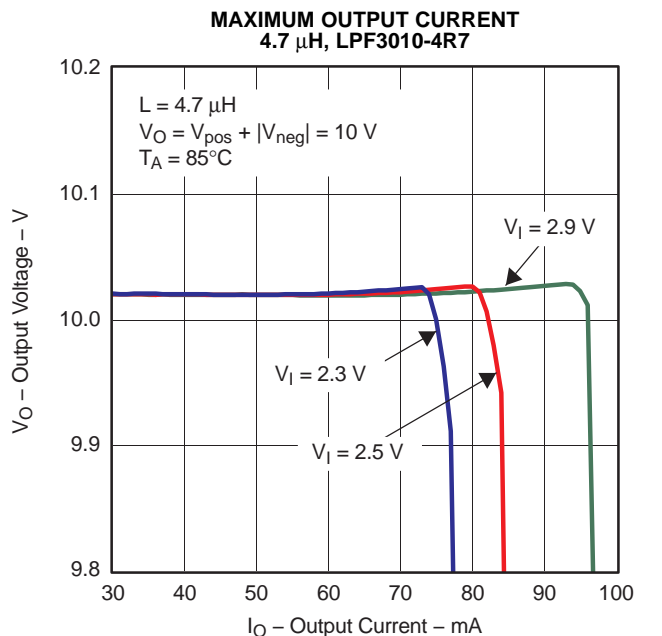


Figure 12.

G012





## DETAILED DESCRIPTION

The TPS65136 operates with a four-switch buck-boost converter topology, generating a negative and a positive output voltage with a single inductor. The device uses the SIMO regulator technology featuring best-in-class line-transient regulation, buck-boost mode for the positive and negative outputs, and highest efficiency over the entire load-current range. High efficiency over the entire load-current range is implemented by reducing the converter switching frequency. Out-of-audio mode avoids the switching frequency going below 20 kHz.

As illustrated in the [functional block diagram](#), the converter operates with two control loops. One error amplifier sets the output voltage for the positive output, OUTP. The ground error amplifier regulates FBG to typically 0 V. Using the external feedback divider allows setting the output voltage of the negative output, OUTN. In principle, the converter topology operates just like any other buck-boost converter topology with the difference that the output voltage across the inductor is the sum of the positive and negative output voltages. With this consideration, all calculations of the buck-boost converter apply for this topology as well. During the first switch cycle, M1 and M2 are closed, connecting the inductor from VIN to GND. During the second switch cycle, the inductor discharges to the positive and negative outputs by closing switches M4 and M3. Because the inductor is discharged to both of the outputs simultaneously, the output voltages can be higher or lower than the input voltage. In addition to that, the converter operates best when the current out of OUTP is equal to the current flowing into OUTN. This is usually the case when driving an AMOLED panel. Any asymmetries in load current can be canceled out by the ground error amplifier connected to FBG. However, this is only possible for current asymmetries of typically 30%. During light load current in discontinuous conduction mode, the converter operates in peak-current-mode control with the switching cycle given by the internal voltage-controlled oscillator (VCO). As the load current increases, the converter operates in continuous-conduction mode. In this mode, the converter moves to peak-current control with the switch cycle given by the fixed off-time. The SIMO regulator topology has excellent line transient regulation when operating in discontinuous conduction mode. As the load current increases, entering continuous conduction mode, the line transient performance is linearly decreased.

## Advanced Power-Save Mode for Light-Load Efficiency

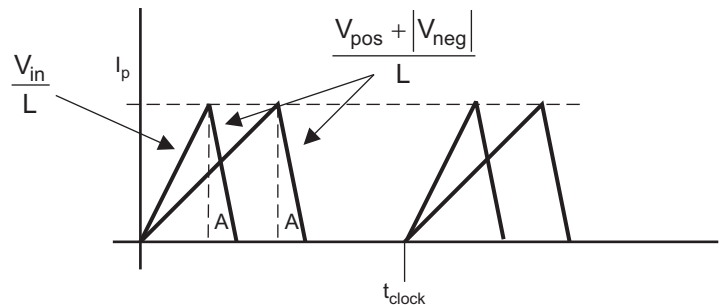
In order to maintain high efficiency over the entire load-current range, the converter reduces its switching frequency as the load current decreases. The advanced power-save mode controls the switching frequency using a voltage-controlled oscillator (VCO). The VCO frequency is proportional to the inductor peak current, with a lower frequency limit of 20 kHz. This avoids disturbance of the audio band and minimizes audible noise coming from the ceramic input and output capacitors. By maintaining a controlled switching frequency, possible EMI is minimized. This is especially important when using the device in mobile phones. See [Figure 8](#) for typical switching frequency versus load current.

## Buck-Boost Mode Operation

Buck-boost mode operation allows the input voltage to be higher than the output voltage. This mode allows the use of batteries and supply voltages that are above the fixed 4.6-V output voltage of OUTP.

## Inherent Excellent Line-Transient Regulation

The SIMO regulator achieves inherent superior line-transient regulation when operating in discontinuous conduction mode, shown in [Figure 5](#) and [Figure 6](#). In discontinuous conduction mode, the current delivered to the output is given by the inductor peak current and falling slope of the inductor current. This is shown in [Figure 14](#), where the output current, given by the area *A*, is the same for different input voltages. Because the converter uses peak-current-mode control, the peak current is fixed as long as the load current is fixed. The falling slope of the inductor current is given by the sum of the output voltage and inductor value. This is also a fixed value and independent of the input voltage. Because of this, any change in input voltage changes the converter duty cycle but does not change the inductor peak current or the falling slope of the inductor current. Therefore, the output current, given by the area *A* ([Figure 14](#)), remains constant over any input voltage variation. Because the area *A* is constant, the converter has an inherently perfect line regulation when operating in discontinuous conduction mode. Entering continuous conduction mode (CCM) linearly decreases the line-transient performance. However, the line-transient response in CCM is still as good as for any standard current-mode-controlled switching converter. The following formulas detail the relations of the TPS65136 converter topology operating in CCM.



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**Figure 14. Inherently Perfect Line-Transient Regulation**

The converter always sees the sum of the negative and positive output voltage, which is calculated as:

$$V_o = V_{\text{outp}} + |V_{\text{outn}}|$$

The converter duty cycle is calculated using the efficiency estimation from the data sheet curves or from real application measurements. A 70% efficiency value is a good value to go through the calculations.

$$D = \frac{V_o}{V_{\text{in}} \cdot \eta + V_o}$$

The output current for entering continuous conduction mode can be calculated. The switching frequency can be obtained from the data sheet graphs. A frequency of 1.5 MHz is usually sufficient for these types of calculations.

$$I_c = \frac{V_o \cdot (1-D)^2}{f_s \cdot 2 \cdot L} \quad (1)$$

The inductor ripple current when operating in CCM can also be calculated.

$$\Delta i_L = \frac{V_{in} \cdot D}{L \cdot f_s}$$

Last but not least, the converter switch peak current is calculated.

$$I_{sw} = \frac{V_{in} \cdot D}{2 \cdot f \cdot L} + \frac{I_{out}}{1-D} \quad (2)$$

## Overvoltage Protection

The device monitors both the positive and negative output voltages. The positive regulator monitors the positive output and reduces the current limit when the output voltage exceeds the overvoltage protection limit. The negative output is clamped using a zener diode, typically to  $-7.6$  V.

## Short-Circuit Protection

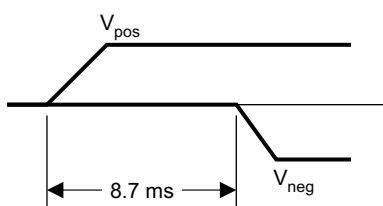
Both outputs are protected against short circuits either to GND or against the other output. For the positive output, the device switching frequency and the current limit are reduced in case of a short circuit.

## Soft-Start Operation

The device increases the current limit during soft-start operation to avoid high inrush currents during start-up. The current limit typically ramps up to its full-current limit within  $100 \mu\text{s}$ .

## Start-Up Sequencing

The TPS65136 includes an internal, fixed start-up sequence, where the negative output voltage rail comes up after the positive output voltage rail. The device starts the positive rail first, and an internal counter delays the start-up of the negative rail, typically by  $8.7$  ms. The negative rail is clamped, typically to  $-0.4$  V, until the internal timer commands the negative rail to start up.



T0298-01

**Figure 15. Start-Up Sequencing**

## Output-Current Mismatch

The device operates best when the current of the positive output is similar to the current of the negative output. However, the device is able to regulate an output-current mismatch between the outputs of up to 30%. If the output-current mismatch becomes much larger, then one of the outputs goes out of regulation.

## Input Capacitor Selection

The device typically requires a  $10\text{-}\mu\text{F}$  ceramic input capacitor. Larger values can be used to lower the input voltage ripple. [Table 1](#) lists capacitors suitable for use on the TPS65136 input.

**Table 1. Input Capacitor Selection**

CAPACITOR	COMPONENT SUPPLIER	SIZE
10 $\mu$ F/10 V	Taiyo Yuden LMK212BJ106	0805
10 $\mu$ F/6.3 V	Taiyo Yuden JMK107BJ106	0603

### Inductor Selection/Efficiency/Line-Transient Response

The device is internally compensated and provides stable operation with either a 4.7- $\mu$ H or 2.2- $\mu$ H inductor. For this type of converter, the inductor selection is a key element in the design process, because it has an impact on several application parameters. The inductor selection influences the converter efficiency, line transient response, and maximum output current. Because the inductor ripple current is fairly large in this type of application, the inductor has a major impact on the overall converter efficiency. Having large inductor ripple current causes the inductor core and magnetizing losses to become dominant. Due to this, an inductor with a larger dc winding resistance can possibly achieve higher converter efficiencies when having lower core and magnetizing losses. Therefore, minimizing inductor ripple current also increases the overall converter efficiency. A 4.7- $\mu$ H inductor achieves a higher efficiency compared to a 2.2- $\mu$ H inductor, due to lower inductor ripple current. The inductor value also influences the line transient regulation. This is because the inductor value influences the current range entering continuous conduction mode (CCM). As discussed, the line transient performance decreases when entering CCM. The larger the inductor value, the lower the load current when entering CCM. The formula to calculate the current entering CCM is shown in [Equation 1](#). The inductors listed in [Table 2](#) achieve a good overall converter efficiency while having a low device profile of just 0,8 mm. The inductor saturation current should be 900 mA, depending on the maximum output current of the application. See [Equation 2](#), where the converter switch current limit is calculated. The converter switch current is equal to the peak inductor current.

**Table 2. Inductor Selection**

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS in mm	$I_{sat}/DCR$
2.2 $\mu$ H	Coilcraft LPS3008-222	2,95 × 2,95 × 0,8	1.1 A/175 m $\Omega$
2.2 $\mu$ H	TOKO FDSE0312-2R2	3,3 × 3,3 × 1,2	1.2 A/160 m $\Omega$
2.2 $\mu$ H	ABCO LPF3010T-2R2	2,8 × 2,8 × 1	1.0A/100 m $\Omega$
2.2 $\mu$ H	Maruwa CXFU0208-2R2	2,65 × 2,65 × 0,8	0.85A/185 m $\Omega$
4.7 $\mu$ H	Maruwa CXFU0208-4R7	2,65 × 2,65 × 0,8	0.51A/440 m $\Omega$
4.7 $\mu$ H	Coilcraft LPS3008-472	2,95 × 2,95 × 0,8	0.8 A/350 m $\Omega$
4.7 $\mu$ H	ABCO LPF3010T-4R7	2,8 × 2,8 × 1	0.7A/280 m $\Omega$

### Output Capacitor Selection

A 4.7- $\mu$ F output capacitor is generally sufficient for most applications, but larger values can be used as well for improved line-transient response at higher load currents. The capacitor of [Table 3](#) is recommended for use with the TPS65136.

**Table 3. Output Capacitor Selection**

CAPACITOR	COMPONENT SUPPLIER	SIZE
4.7 $\mu$ F/10V	Taiyo Yuden LMK107BJ475	0603

### Setting the Negative Output Voltage OUTN

For highest output-voltage accuracy, the TPS65136 has an internally fixed output voltage for the positive output. The negative output voltage is adjustable. Because the feedback FBG is regulated to ground, the voltage across R1 is equal to the positive output voltage of 4.6 V. R1 is selected to have at least 10  $\mu$ A through the feedback divider.

$$R1 = \frac{4.6 \text{ V}}{10 \mu\text{A}} \approx 464 \text{ k}\Omega$$

R2 is then calculated as:

$$R2 = \frac{|V_{\text{neg}}|}{4.6 \text{ V}} \times R1$$

### PCB Layout Guidelines

PCB layout is an important task in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. For the TPS65136, the following PCB layout guidelines are recommended.

Place the power components first. The inductor and the input and output capacitors must be as close as possible to the IC pins. Place the bypass capacitor for the reference output voltage VAUX as close as possible to pin 4. Use bold and wide traces for power traces connecting the inductor and input and output capacitors. Use a common ground plane or a star ground connection.

See the TPS65136EVM-063 user's guide ([SLVU244](#)) and evaluation module for a PCB layout example.

TYPICAL APPLICATION

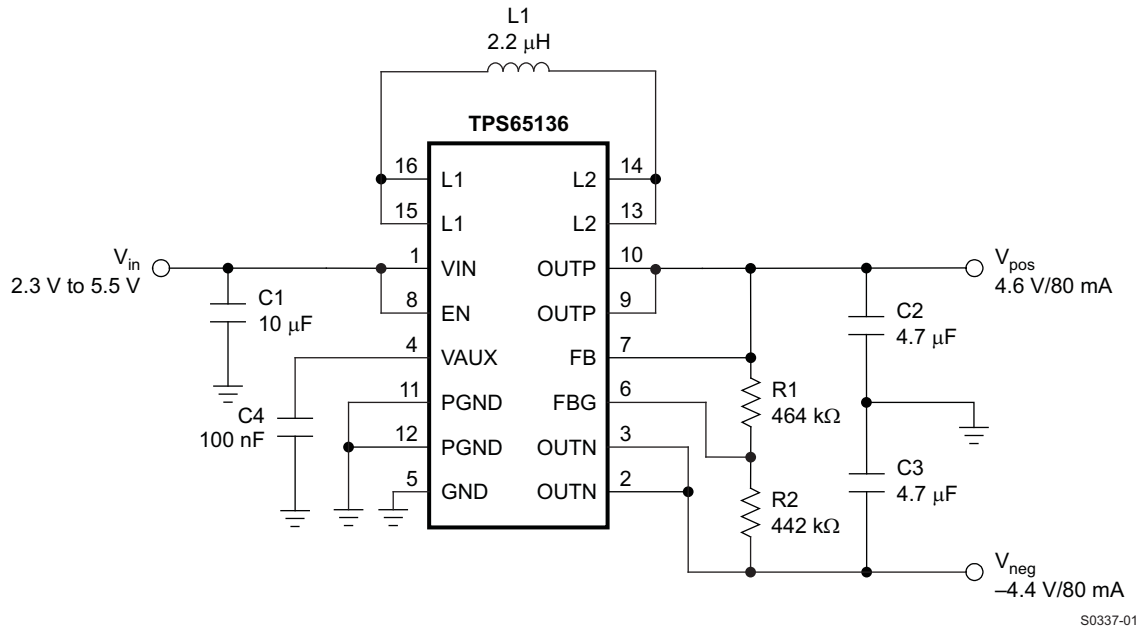


Figure 16. Standard Application AMOLED Supply

S0337-01

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS65136RTER</a>	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CCO
TPS65136RTER.B	Active	Production	WQFN (RTE)   16	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	CCO

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65136RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65136RTER	WQFN	RTE	16	3000	353.0	353.0	32.0

## GENERIC PACKAGE VIEW

**RTE 16**

**WQFN - 0.8 mm max height**

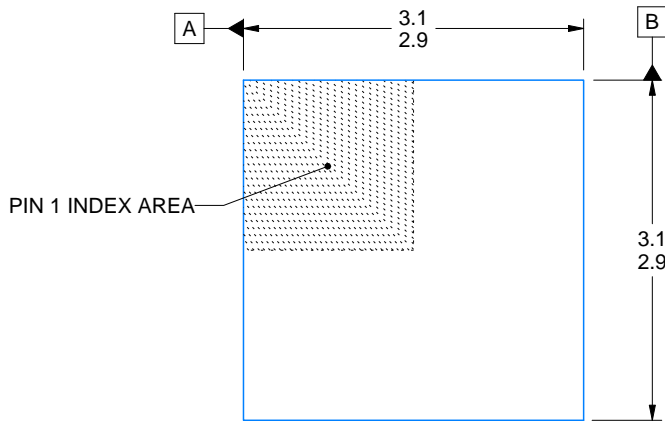
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

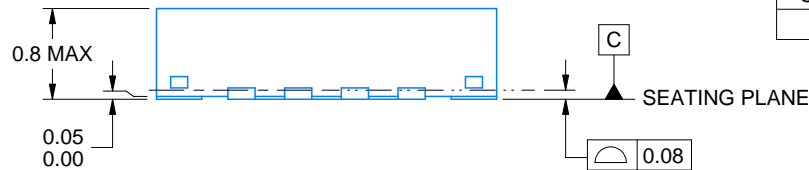
This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4225944/A



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



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NOTES:

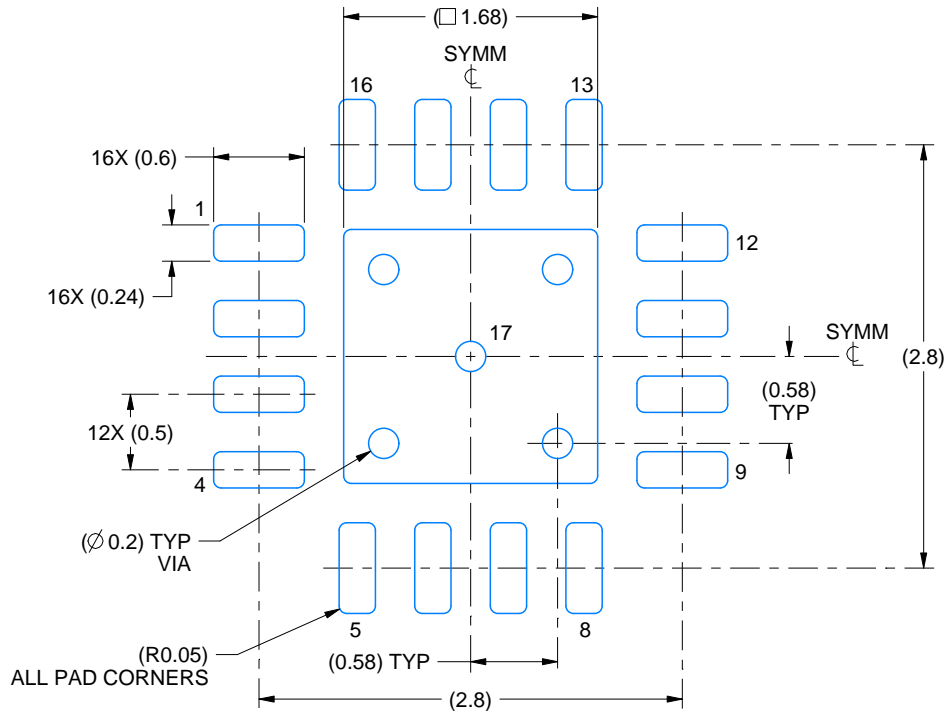
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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