参考文献

TPS61378-Q1 具有负载断开功能的 25μA 静态电流同步升压转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：–40°C 至 125°C 环境工作温度范围
- TPS61378-Q1 可湿性侧面
- TPS61378L-Q1 浸锡
  - 缩短生产周期并延长货架期
- 支持功能安全
  - 可提供用于功能安全系统设计的文档
- 灵活的输入和输出工作范围
  - 输入电压范围：2.3V 至 14V
  - 可编程的输出电压：4.0V 至 18.5V
  - 输入电压范围：2.3V 至 14V
  - 固定输出选项：5V、5.25V 和 5.5V
  - 可编程峰值电流限制：1A 至 4.8A
- 避免 AM 频带干扰和串扰
  - 动态可编程开关频率：200kHz 至 2.2MHz
  - 在 FPWM 模式下支持扩频调频
  - 可选的时钟同步
- 尽量减小解决方案尺寸，用于空间受限型应用
  - 集成式 LS/HS/ISO FET：$R_{DS(ON)}$ 50mΩ/50mΩ/100mΩ
  - 支持高达 2.2MHz，L-C 较小
- 尽量减少轻负载和空闲状态的电流消耗
  - 流入 VIN 引脚的静态电流为 25μA
  - 流入 VIN 引脚的关断电流为 0.5μA
  - 可选择自动 PFM 和强制 PWM 模式
  - 关断期间或出现故障时真正负载断开连接
- 集成保护特性
  - 支持接近 VOUT 运行电压的 VIN
  - 输入欠压锁定和输出过压保护
  - 断续输出短路保护
  - 电源正常状态指示器
  - 165°C 的热关断保护限制
- 0.8A 负载条件下进行 3.3V 至 9V 转换时效率高于 90%

2 应用

- 高级驾驶辅助系统 (ADAS)
- 汽车信息娱乐系统与仪表组
- 车身电子装置和照明
- 紧急呼叫 (eCall)

3 说明

TPS61378-Q1 是一款完全集成的同步升压转换器，集成了负载断开功能。输入电压范围从 2.3V 到 14V，最大输出电压高达 18.5V。开关峰值电流限制的可编程范围为 1A 至 4.8A。该器件从 V_{IN} 端消耗 25μA 的静态电流。

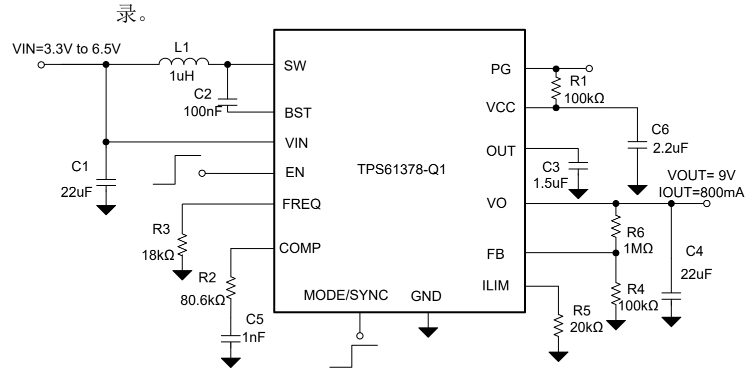
TPS61378-Q1 采用峰值电流模式控制，可编程开关频率范围为 200kHz 到 2.2MHz。在中等到重负载条件下，该器件在固定频率 PWM 模式下运行。在轻负载条件下，通过配置 MODE 引脚可实现两种可选模式：自动 PFM 模式和强制 PWM 模式，以便在轻负载条件下实现效率和抗噪性平衡。可与外部时钟同步开关频率。TPS61378-Q1 使用内部时钟展频在 FPWM 模式下提升 EMI 友好性。此外，还有内部软启动时间来限制浪涌电流。

TPS61378-Q1 有各种固定输出电压版本，可节省外部反馈电阻器。它支持外部环路补偿，在更广泛的 V_{OUT}/V_{IN} 范围内优化稳定性和瞬态响应。它还集成了稳健的保护特性，包括输出短路保护、输出过压保护和热关断保护。TPS61378-Q1 采用具有可湿性侧面的 3mm × 3mm 16 引脚 QFN 封装。

器件信息

器件型号	封装[(1)]	封装尺寸（标称值）
TPS61378-Q1	WQFN-16	3.0mm × 3.0mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用

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4 Device Comparison Table

PART NUMBER	OUTPUT VOLTAGE (V)	OUTPUT VOLTAGE SELECTION RESISTOR (R_{FB})[(2)]	SPREAD SPECTRUM
TPS61378-Q1	5	$0\Omega \leqslant R_{FB} \leqslant 2.4\ k\Omega$	Enable
	5.25	$3.6k\Omega \leqslant R_{FB} \leqslant 4.8\ k\Omega$	
	5.5	$7.2k\Omega \leqslant R_{FB} \leqslant 9.6k\Omega$	
	Adjustable	$R_{FB} \geqslant 14.4k\Omega$	
TPS613781-Q1[(1)]	5.7	$0\Omega \leqslant R_{FB} \leqslant 2.4\ k\Omega$	Enable
	6.2	$3.6k\Omega \leqslant R_{FB} \leqslant 4.8\ k\Omega$	
	7	$7.2k\Omega \leqslant R_{FB} \leqslant 9.6k\Omega$	
	8	$R_{FB} \geqslant 14.4k\Omega$	
TPS613782-Q1[(1)]	9	$0\Omega \leqslant R_{FB} \leqslant 2.4\ k\Omega$	Enable
	10	$3.6k\Omega \leqslant R_{FB} \leqslant 4.8\ k\Omega$	
	11	$7.2k\Omega \leqslant R_{FB} \leqslant 9.6k\Omega$	
	12	$R_{FB} \geqslant 14.4k\Omega$	
TPS613783-Q1	5	$0\Omega \leqslant R_{FB} \leqslant 2.4\ k\Omega$	Disable
	5.25	$3.6k\Omega \leqslant R_{FB} \leqslant 4.8\ k\Omega$	
	5.5	$7.2k\Omega \leqslant R_{FB} \leqslant 9.6k\Omega$	
	Adjustable	$R_{FB} \geqslant 14.4k\Omega$	
TPS613784-Q1[(1)]	5.7	$0\Omega \leqslant R_{FB} \leqslant 2.4\ k\Omega$	Disable
	6.2	$3.6k\Omega \leqslant R_{FB} \leqslant 4.8\ k\Omega$	
	7	$7.2k\Omega \leqslant R_{FB} \leqslant 9.6k\Omega$	
	8	$R_{FB} \geqslant 14.4k\Omega$	
TPS613785-Q1	9	$0\Omega \leqslant R_{FB} \leqslant 2.4\ k\Omega$	Disable
	10	$3.6k\Omega \leqslant R_{FB} \leqslant 4.8\ k\Omega$	
	11	$7.2k\Omega \leqslant R_{FB} \leqslant 9.6k\Omega$	
	12	$R_{FB} \geqslant 14.4k\Omega$	

(1) Product Preview. Contact TI factory for more information.
(2) R_{FB} is the sensed resistor from FB pin. Please refer to *节 8.2.2.1* for details. Avoid using resistors other than the recommended values, otherwise the output voltage value cannot be guaranteed.

5 Pin Configuration and Functions

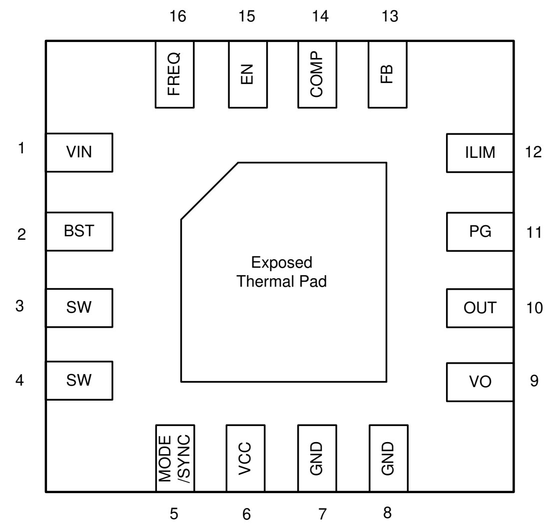


图 5-1. 16-Pin WQFN RTE Package (Transparent Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	IC power supply input
BST	2	I	Power supply for high-side N-MOSFET gate drivers. A capacitor must be connected between this pin and the SW pin.
SW	3, 4	PWR	The switching node pin of the converter. It is connected to the drain of the internal low-side FET and the source of the high-side FET.
MODE/SYNC	5	I	Mode selection pin. MODE = high, forced PWM mode MODE = low or floating, auto PFM mode This pin can also be used to synchronize the external clock. Refer to 表 7-2 for details.
VCC	6	O	Output of internal regulator. A ceramic capacitor with more than 1 µF must be connected between this pin and GND.
GND	7, 8	PWR	Power ground of the IC. It is connected to the source of the low-side FET.
VO	9	PWR	Output of the isolation FET. Connect load to this pin to achieve input/output isolation.
OUT	10	PWR	Output of the drain of the HS FET. Connect this pin because the output can disable the load disconnect/short protection feature (or short this pin with the VO pin).
PG	11	O	Power good indicator and open drain output
ILIM	12	I	Current limit setting pin. Use a resistor to set the desired peak current limit. Refer to 节 7.3.7 for details.
FB	13	I	Feedback pin. Use a resistor divider to set the desired output voltage. Refer to 节 8.2.2.1 for details.
COMP	14	I	Output of the internal transconductance error amplifier. An external RC network is connected to this pin to optimize the loop stability and response time.
EN	15	I	Enable logic input
FREQ	16	I	Frequency setting pin. Connect a resistor between this pin and GND pin to set the desired frequency.
Thermal Pad	-	-	The thermal pad must be connected to the power ground plane for good power dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Voltage range at terminals [(2)]	VIN	-0.3	16	V
Voltage range at terminals [(2)]	VO, SW, OUT	– 0.3	23	V
	BST	– 0.3	SW + 6	V
	MODE/SYNC, FB, FREQ, ILIM, VCC, COMP, EN	– 0.3	6	V
	PG	-0.3	20	V
T_J [(3)]	Operating junction temperature	– 40	150	°C
T_{stg}	Storage temperature	– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) High junction temperatures degrade operating lifetime. Operating lifetime is de-rated for junction temperatures greater than 125°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ [(1)]	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(2)]	±2000	V
		Charged-device model (CDM), per AEC Q100-011, all pins[(3)]	±500	
$V_{(ESD)}$ [(1)]	Electrostatic discharge	Charged-device model (CDM), per AEC Q100-011, corner pins (1,4,5,8,9,12,13,16)[(3)]	±750	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.3		14	V
V_{OUT}	Outputvoltage	4		18.5	V
T_J	Operating junction temperature[(1)]	– 40		150	°C

(1) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125°C.

6.4 Thermal Information

THERMAL METRIC[(1)]		TPS61378-Q1 RTE 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.5	°C/W

THERMAL METRIC(1)		TPS61378-Q1 RTE 16 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	8.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report .

6.5 Electrical Characteristics

T_J = -40 to 125°C, L = 1 µH, V_{IN} = 3.3 V and V_{OUT} = 9 V (VO pin). Typical values are at T_J = 25°C, (unless otherwise noted)

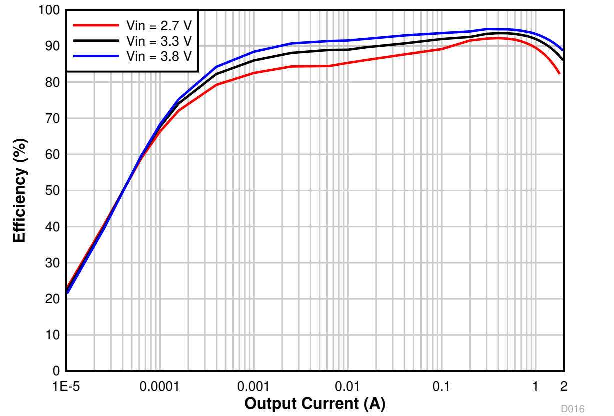
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.3		14	V
V_{IN_UVLO}	VIN under voltage lockout threshold	V_{IN} rising		2.2	2.3	V
		V_{IN} falling		2.04	2.2	V
V_{IN_HYS}	VIN UVLO hysteresis			160		mV
V_{CC_UVLO}	VCC UVLO threshold	V_{CC} rising		2.2		V
V_{CC_HYS}	VCC UVLO hysteresis	V_{CC} hysteresis		150		mV
V_{CC}	VCC regulation	I_{VCC} = 6 mA, V_{OUT} = 9V		4.8		V
I_Q	Quiescent current into V_{IN} pin	IC enabled, no load, V_{IN} = 3.3 V, V_{OUT} = 18.5 V, V_{FB} = V_{REF} + 0.1 V,		25	35	µA
I_Q	Quiescent current into OUT pin	IC enabled, no load, V_{IN} = 3.3 V, V_{OUT} = 18.5 V, V_{FB} = V_{REF} + 0.1 V,		10	20	µA
I_{SD}	Shutdown current into VIN pin	IC disabled, V_{IN} =14 V, EN = GND		0.6	5	µA
I_{SW_LKG}	Leakage current into SW	IC disabled, V_{IN} = OUT = SW =14 V			5	µA
I_{VO_LKG}	Reverse leakage current into VO	IC disabled, OUT= VO = 5 V, SW = 0			5	µA
OUTPUT VOLTAGE						
V_{OVP}	Output over-voltage protection threshold	V_{IN} = 3.3 V, V_{OUT} rising	19.3	20	20.5	V
V_{OVP_HYS}	Output over-voltage protection hysteresis	V_{IN} = 3.3 V, OVP threshold		0.5		V
VOLTAGE REFERENCE						
V_{REF}	Reference Voltage at FB pin	T_J = -40 to 125°C, R_{FB} = 16.0kΩ	0.788	0.800	0.812	V
V_{OUT_5V}		T_J = -40 to 125°C, R_{FB} = 2.0 kΩ	4.85	5.00	5.15	V
$V_{OUT\_5.25V}$		T_J = -40 to 125°C, R_{FB} = 4.0 kΩ	5.10	5.25	5.35	V
$V_{OUT\_5.5V}$		T_J = -40 to 125°C, R_{FB} = 8.0 kΩ	5.35	5.50	5.65	V
V_{OUT_5V}		TPS613783Q1, T_J = -40 to 125°C, R_{FB} = 2.0 kΩ	4.85	5.00	5.15	V
$V_{OUT\_5.25V}$		TPS613783Q1, T_J = -40 to 125°C, R_{FB} = 4.0 kΩ	5.10	5.25	5.35	V
$V_{OUT\_5.5V}$		TPS613783Q1, T_J = -40 to 125°C, R_{FB} = 8.0 kΩ	5.35	5.50	5.65	V
V_{OUT_9V}		TPS613785Q1, T_J = -40 to 125°C, R_{FB} = 2.0 kΩ	8.75	9.00	9.15	V
V_{OUT_10V}		TPS613785Q1, T_J = -40 to 125°C, R_{FB} = 4.0 kΩ	9.75	10.00	10.20	V
V_{OUT_11V}		TPS613785Q1, T_J = -40 to 125°C, R_{FB} = 8.0 kΩ	10.70	11.00	11.20	V
V_{OUT_12V}		TPS613785Q1, T_J = -40 to 125°C, R_{FB} = 16.0 kΩ	11.70	12.00	12.22	V
I_{FB_LKG}	Leakage current into FB pin				50	nA
POWER SWITCH						
$R_{DS(on)}$	Low-side MOSFET on resistance	V_{CC} = 4.85 V		50		mΩ
$R_{DS(on)}$	High-side MOSFET on resistance	V_{CC} = 4.85 V		50		mΩ
$R_{DS(on)}$	Isolation MOSFET on resistance	V_{CC} = 4.85 V		100		mΩ

T_J = -40 to 125°C, L = 1 µH, V_{IN} = 3.3 V and V_{OUT} = 9 V (VO pin). Typical values are at T_J = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT						
I_{LIM_SW}	Peak switching current limit FPWM	R_{LIM} = 20 kΩ , Duty cycle = 65%	4	4.8	5.55	A
I_{LIM_SW}	Peak switching current limit Auto PFM	R_{LIM} = 20 kΩ , Duty cycle = 65%	4	4.8	5.55	A
I_{LIM_SW}	Peak switching current limit FPWM	R_{LIM} = 102 kΩ, Duty cycle = 65%, 4.7uH		0.75		A
I_{LIM_SW}	Peak switching current limit Auto PFM	R_{LIM} = 102 kΩ, Duty cycle = 65%, 4.7uH		0.75		A
$I_{LIM\_SS\_1}$	Peak switching current limit at softstart	V_{IN} = 3.3 V, V_{OUT} = 0 V, R_{LIM} = 20 kΩ	0.9	1.15	1.4	A
SWITCHING FREQUENCY						
Fsw	Switching frequency	R_{FREQ} = 18 kΩ	2050	2200	2400	kHz
Fsw	Switching frequency	R_{FREQ} = 218 kΩ	180	200	230	kHz
D_{max}	Maximum Duty Cycle	R_{FREQ} = 18 kΩ	78			%
t_{ON_min}	Minimal on time			70		ns
F_{DITHER}				10%		Fsw
$F_{pattern}$				0.4%		Fsw
ERROR AMPLIFIER						
I_{SINK}	COMP pin sink current	V_{FB} = V_{REF} + 0.2V		6		µA
I_{SOURCE}	COMP pin source current	V_{FB} = V_{REF} - 0.2V		6		µA
V_{CCLPH}	COMP pin high clamp voltage	V_{FB} = V_{REF} - 0.2V, ILIM = 4.8 A		1.3		V
V_{CCLPL}	COMP pin high low voltage	V_{FB} = V_{REF} + 0.2V,		0.6		V
G_{mEA}	Error amplifier trans conductance	V_{COMP} = 1.0 V		70		µS
POWER GOOD						
V_{PG_TH}	PG threhold for rising FB voltage	Reference to V_{REF}		90%		
V_{PG_HYS}	PG hysteresis	Reference to V_{REF}		5%		
I_{PG_SINK}	PG pin sink current capability	V_{PG} = 0.4 V		20		mA
t_{PG_DELAY}	PG delay time		2.5	3.4	4.3	ms
DOWN MODE						
t_{EN_DELAY}	Delay time between EN high and device working			0.4		ms
t_{SS}	Softstart time			2.5		ms
t_{HCP_ON}	Hiccup on time			1.8		ms
t_{HCP_OFF}	Hiccup off time			67		ms
SYNC TIMING						
f_{SYNC_MIN}				200		kHz
f_{SYNC_MAX}				2200		kHz
EN/SYNC LOGIC						
VI_H	EN, MODE/SYNC pins Logic high threshold				1.2	V
VI_L	EN, MODE/SYNC pins Logic Low threshold		0.4			V
R_{DOWN}	EN, MODE/SYNC pins internal pull down resistor			800		kΩ
THERMAL SHUTDOWN						
t_{SD_R}	Thermal shutdown rising threshold	TJ rising		165		°C
t_{SD_F}	Thermal shutdown falling threshold	TJ falling		145		°C

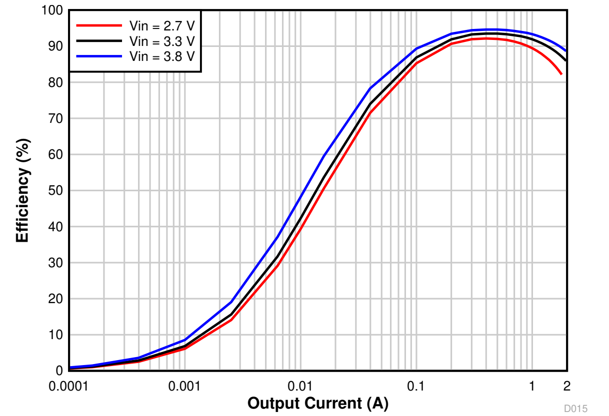
6.6 Typical Characteristics

V_{IN} = 3.3 V, V_{OUT} = 9 V (VO pin), T_A = 25°C, Fsw = 2.2 MHz, unless otherwise noted.



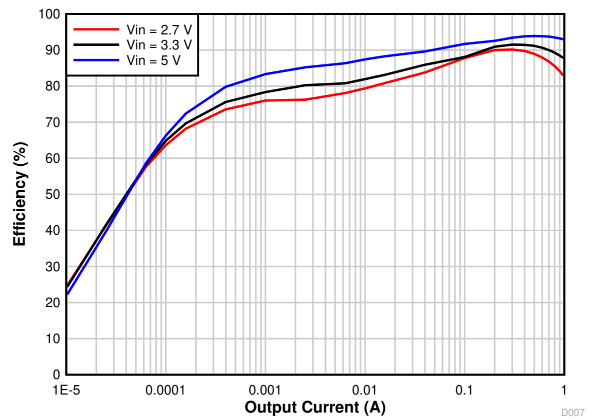
VOUT = 5 V   Auto PFM   Fsw = 2.2 MHz

图 6-1. 5 V_{OUT} Efficiency vs Output Current



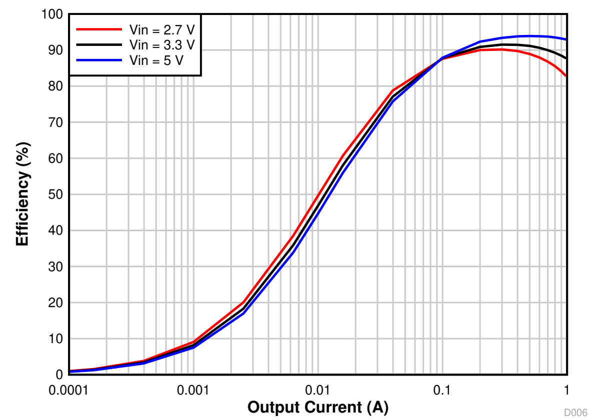
VOUT = 5 V   FPWM   Fsw = 2.2 MHz

图 6-2. 5 V_{OUT} Efficiency vs Output Current



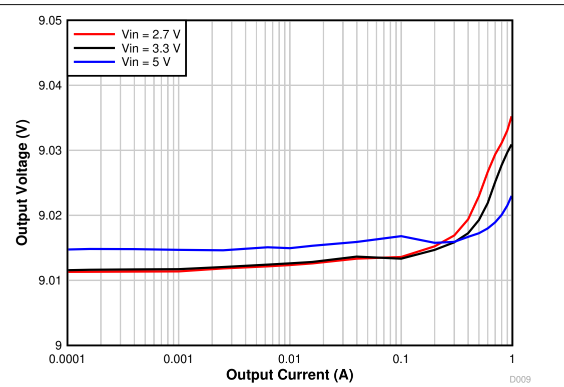
VOUT = 9 V   Auto PFM   Fsw = 2.2 MHz

图 6-3. 9 V_{OUT} Efficiency vs Output Current



VOUT = 9 V   FPWM   Fsw = 2.2 MHz

图 6-4. 9 V_{OUT} Efficiency vs Output Current



VOUT = 9 V   PFM   Fsw = 2.2 MHz

图 6-5. 9 V_{OUT} Regulation vs Output Current

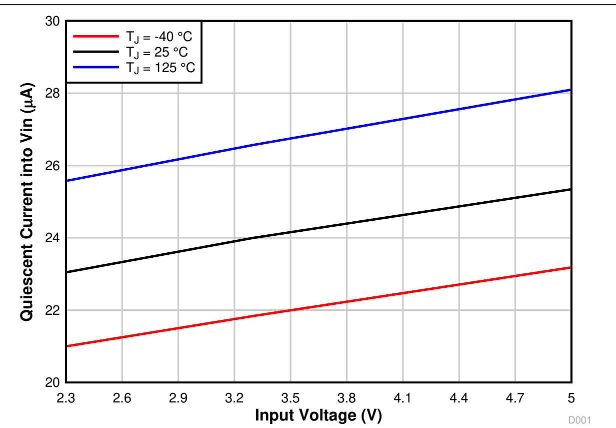


图 6-6. Quiescent Current into V_{IN} vs Input Voltage

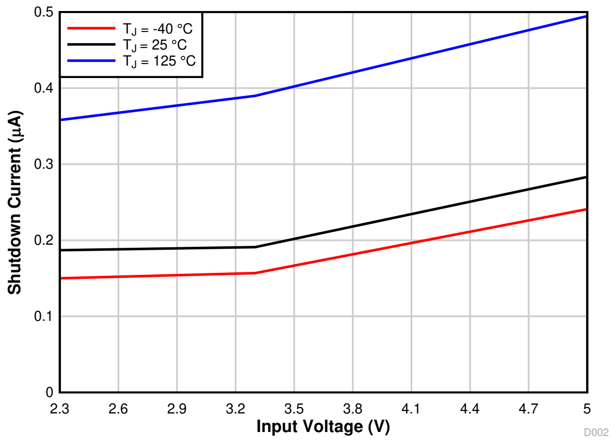


图 6-7. Shutdown Current vs Input Voltage

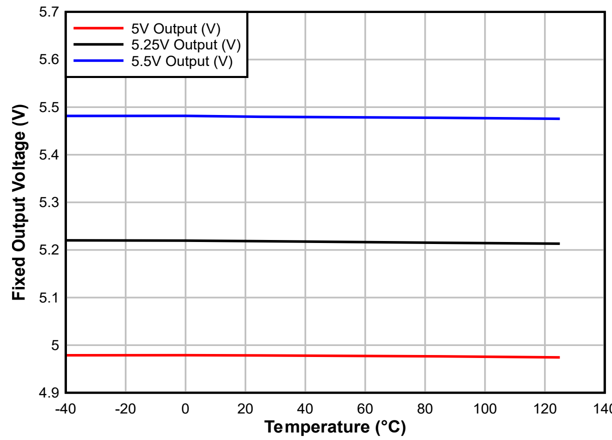


图 6-8. Fixed Output Voltage vs Temperature

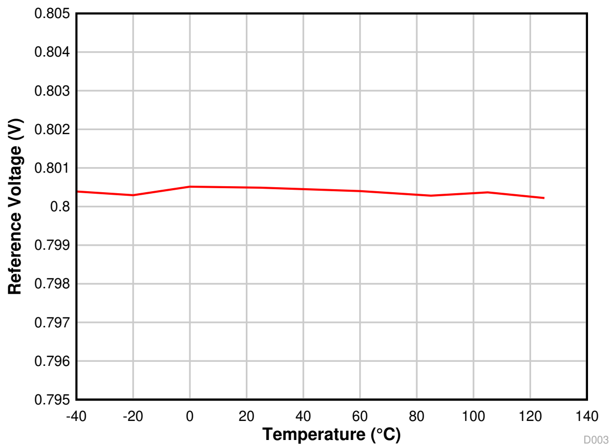


图 6-9. Reference Voltage vs Temperature

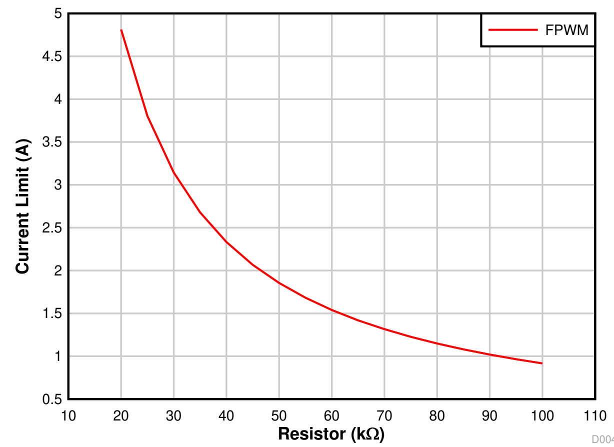


图 6-10. Current Limit vs Setting Resistance

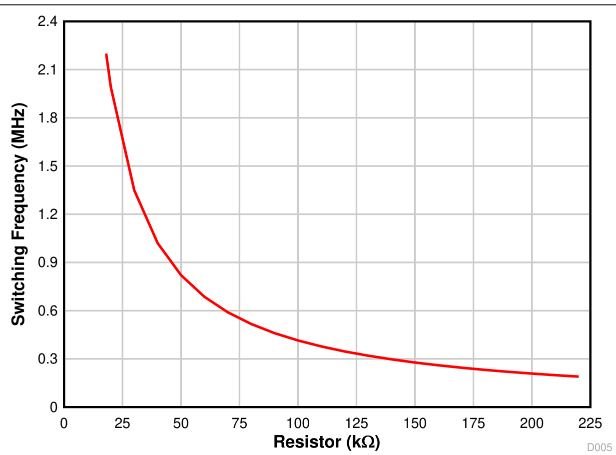


图 6-11. Switching Frequency vs Setting Resistance

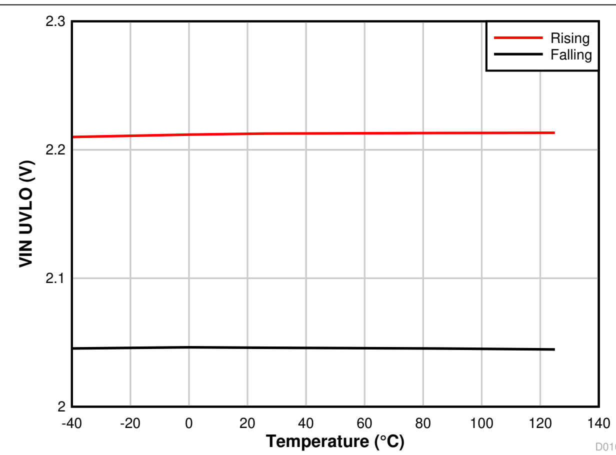


图 6-12. V_{IN} UVLO Threshold Voltage vs Temperature

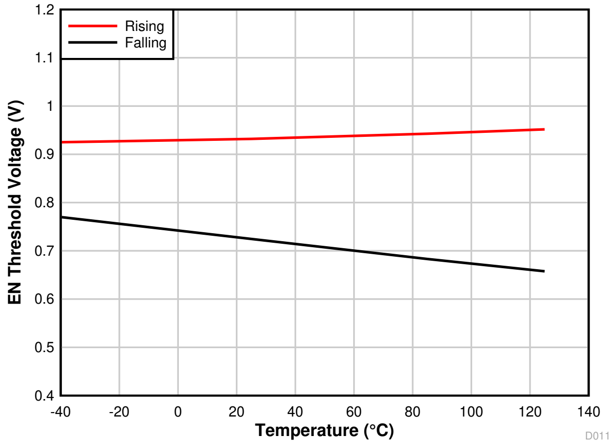


图 6-13. EN Threshold Voltage vs Temperature

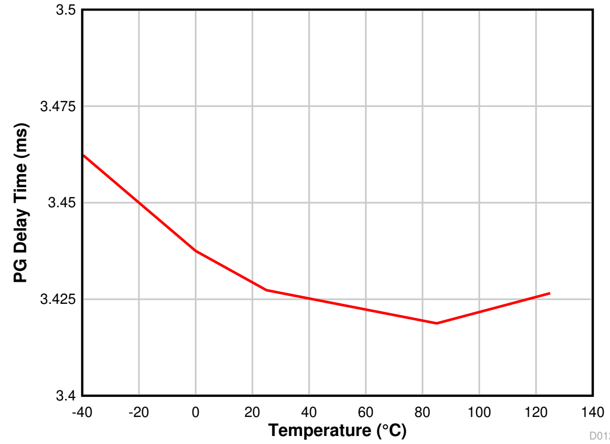


图 6-14. PG Delay Time vs Temperature

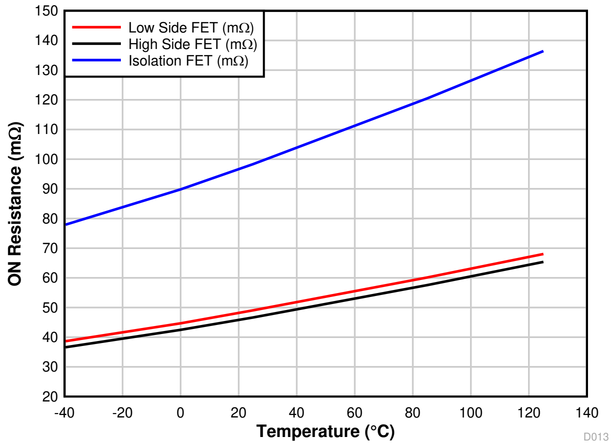


图 6-15. R_{DSON} vs Temperature

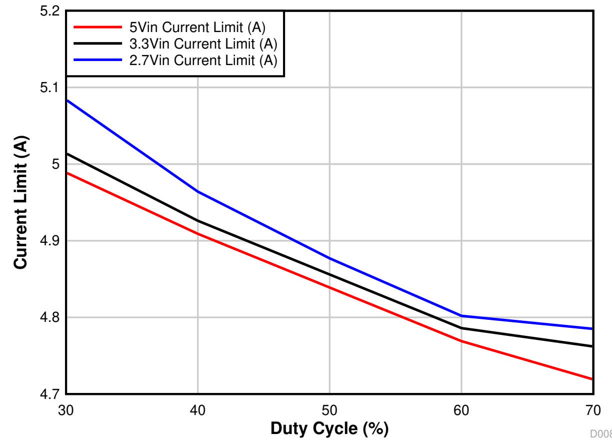


图 6-16. Duty Cycle vs Current Limit

7 Detailed Description

7.1 Overview

The TPS61378-Q1 is a fully-integrated synchronous boost converter with load disconnect function. It supports output voltage up to 18.5 V with a maximum of a 4.8-A programmable switching peak current limit. The input voltage ranges from 2.3 V to 14 V while consuming 25-μA quiescent current.

The TPS61378-Q1 utilizes the fixed-frequency peak current control scheme, which has an internal oscillator and supports adjustable switching frequency from 200 kHz to 2.2 MHz.

The TPS61378-Q1 operates with fixed-frequency pulse width modulation (PWM) from medium to heavy load. At the beginning of each switching cycle, the low-side N-MOSFET switch is turned on. The inductor current ramps up to a peak current that is determined by the output of the internal error amplifier (EA). Once the switching peak current triggers the output of the EA, the low-side N-MOSFET is turned off and the high-side N-MOSFET is turned on after a short dead time. The high-side N-MOSFET switch is not turned off until the next cycle as determined by the internal oscillator. The low-side switch turns on again after a short dead time and the switching cycle is repeated.

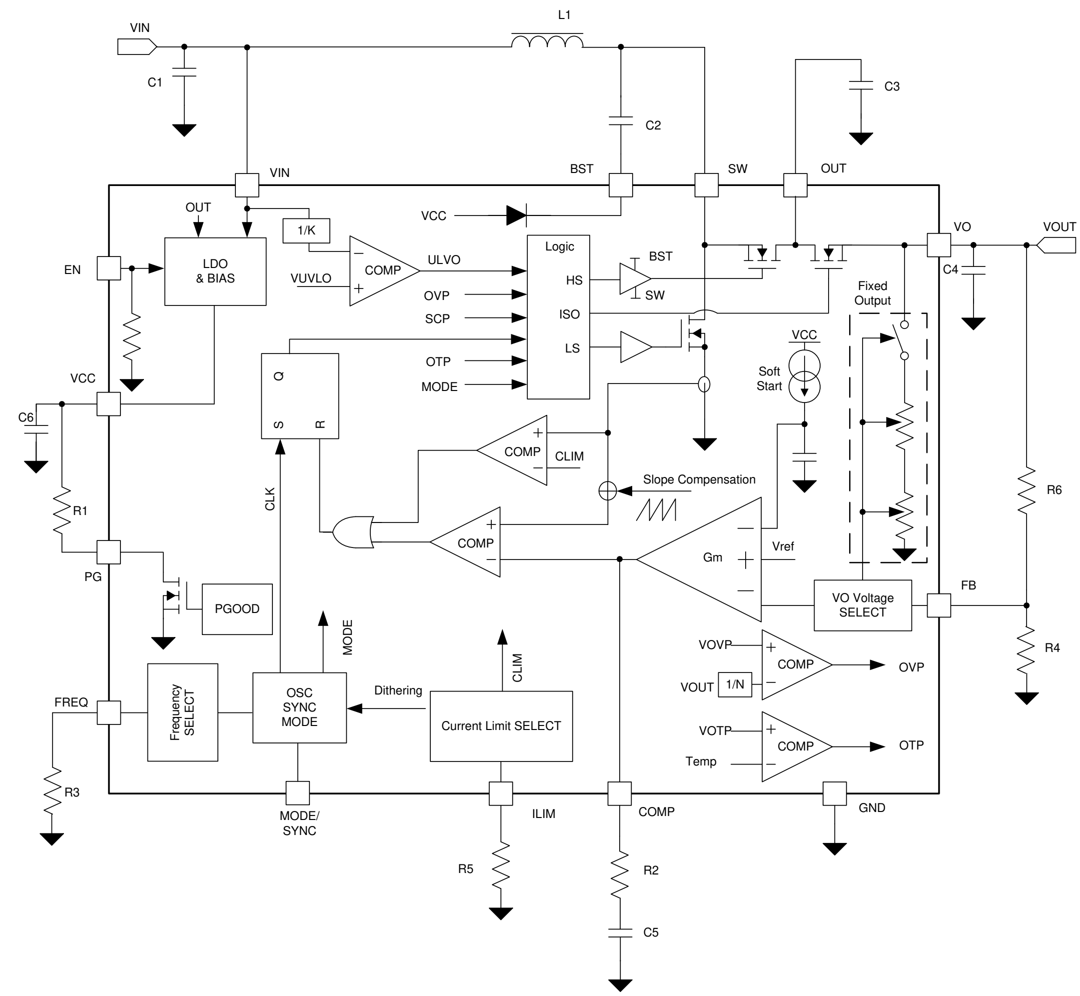
The TPS61378-Q1 provides either auto PFM or forced PWM for the light load operation by configuring the MODE/SYNC pin. In forced PWM mode, the switching frequency remains constant across the entire load range, which helps avoid frequency variation with load. The internal oscillator can be synchronized to an external clock applied on the MODE/SYNC pin. Spread spectrum modulation of the frequency in forced PWM mode helps optimize the EMI performance for automotive applications. In auto PFM mode, the switching frequency can decrease, resulting in higher efficiency.

The TPS61378-Q1 implements a cycle-by-cycle current limit to protect the device from overload during the boost operation phase. If the output current further increases and triggers the output voltage to fall below the input voltage, the TPS61378-Q1 enters into hiccup mode short protection.

There is a built-in soft-start time, which prevents the inrush current during the start-up. The TPS61378-Q1 also provides a power good (PG) indicator to enable the power sequence control for start-up.

The TPS61378-Q1 also has a number of protection features including output short protection, output overvoltage protection (OVP), and thermal shutdown protection (OTP).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VCC Power Supply

The internal LDO in the TPS61378-Q1 outputs a regulated voltage of 4.8 V with 10-mA output current capability. A ceramic capacitor is connected between the VCC pin and GND pin to stabilize the VCC voltage and also decouple the noise on the VCC pin. The value of this ceramic capacitor should be above 1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 10 V is recommended.

7.3.2 Input Undervoltage Lockout (UVLO)

An undervoltage lockout (UVLO) circuit stops the operation of the converter when the input voltage drops below the UVLO threshold of 2.04 V (typical). A hysteresis of 160 mV (typical) is added so that the device cannot be enabled again until the input voltage exceeds 2.2 V (typical). This function is implemented to prevent the device from malfunctioning when the input voltage is between 2.04 V and 2.2 V.

7.3.3 Enable and Soft Start

When the input voltage is above the UVLO threshold and the EN pin is pulled above 1.2 V, the TPS61378-Q1 is enabled. The device starts to monitor the FB pin. With a typical 400-µs delay time after EN is pulled high, the TPS61378-Q1 starts switching. There is an internal built-in start-up time, typically 2.5 ms, to limit the inrush current during start-up.

7.3.4 Shut Down

When the input voltage is below the UVLO threshold or the EN pin is pulled low, The TPS61378-Q1 is in shutdown mode and all the functions are disabled. The input voltage is isolated from the output to minimize the leakage currents.

7.3.5 Switching Frequency Setting

The TPS61378-Q1 uses a fixed-frequency control scheme. The switching frequency can be programmed between 200kHz and 2.2Mhz using a resistor from the FREQ pin to GND. The resistor must be connected when the oscillator is synchronized by external clock. The resistance is defined by 方程式 1.

$$F_{SW}(MHz) = \frac{41.9}{R_{FREQ}(k\Omega) + 1.05} \quad (1)$$

where

- R_{FRQE} is the resistance between the FREQ pin and the GND pin

For example, the switching frequency is 2.2 MHz if the resistance between FREQ pin and GND is 18kΩ. This pin cannot be left floating or tied to VCC.

7.3.6 Spread Spectrum Frequency Modulation

The TPS61378-Q1 uses a triangle waveform to spread the switching frequency with ±10% of normal frequency. The frequency of the triangle waveform is typically 0.4% of the switching frequency. For example, if the normal switching frequency of the TPS61378-Q1 is programmed to 2.2MHz, the spread spectrum function modulates the switching frequency in the range of 1.98MHz to 2.42MHz in a triangle behavior with an 8.8kHz rate.

The spread spectrum is only available while the clock of the TPS61378-Q1 is free running at its natural frequency in FPWM mode. Any of the following conditions overrides spread spectrum, turning it off:

- An external clock is applied to the MODE/SYNC pin.
- The MODE/SYNC pin is configured to be logic low or floating.

7.3.7 Adjustable Peak Current Limit

The TPS61378-Q1 adopts a cycle-by-cycle peak current limit internally and changes its current limit with different working conditions. The low-side switch is turned off immediately as soon as the switch peak current triggers the peak current limit. The peak switch current limit can be set by a resistor from the ILIM pin to ground. The relationship between the peak current limit and the resistor is shown in 方程式 2.

$$R_{LIM}(k\Omega) = 1.184 + \frac{90.56}{I_{LIM}(A)} \quad (2)$$

where

- R_{ILIM} is the resistance between the ILIM pin and the GND. This pin cannot be left floating or connected to VCC.
- I_{LIM} is switch peak current limit

For instance, the current limit is set to 4.8 A if the R_{LIM} is 20 kΩ.

表 7-1 summarizes the peak current limit under various conditions. The current limit applies to the start-up phase.

表 7-1. Switch Peak Current Limit

Behavior	Switch Peak Current Limit
Vin < VO (Not in Down Mode)	I_{LIM} (1)
Vin < VO (In Down Mode)	2/3 I_{LIM}
3V > Vin - VO > 0V	4/9 I_{LIM}

表 7-1. Switch Peak Current Limit （续）

Behavior	Switch Peak Current Limit
6V > Vin - VO > 3V	1/4 I_{LIM}
Vin - VO > 6V	1/4 I_{LIM} & Fsw Clamp to 1.1MHz if FREQ pin setting is > 1.1MHz
FB ⩽ 0.1V	1/5 I_{LIM} & Fsw Clamp to 1.1MHz if FREQ pin setting is > 1.1MHz

(1) I_{LIM} is switch peak current limit programmed in 方程式 2.

7.3.8 Bootstrap

The TPS61378-Q1 has an integrated bootstrap regulator circuit. A small ceramic capacitor is needed between the BST pin and SW pin to provide the gate drive supply voltage for high-side switches. The bootstrap capacitor is charged during the time when the low-side switch is in the ON state. The value of this ceramic capacitor should be above 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating higher than 6.3 V is recommended.

7.3.9 Load Disconnect

The TPS61378-Q1 integrates a load disconnect function when the input source is DC, completely cutting off the path between the input side and output side during shutdown.

The output disconnect function also allows the output short protection and minimizes the inrush current at start-up.

7.3.10 MODE/SYNC Configuration

表 7-2 summarizes the MODE/SYNC function and the entry condition.

表 7-2. MODE/SYNC Configuration

MODE/SYNC PIN CONFIGURATION	MODE
Logic Low or Floating	Auto PFM Mode
Logic High	Forced PWM Mode
External Synchronization	Forced PWM Mode

The TPS61378-Q1 can be synchronized to an external clock applied to the MODE/SYNC pin.

7.3.11 Overvoltage Protection (OVP)

If the output voltage exceeds the OVP threshold (typically 20 V), the TPS61378-Q1 immediately stops switching until the output voltage drops below the recovery threshold (typically 19.5 V). This function protects the device against excessive voltage.

7.3.12 Output Short Protection/Hiccup

In addition to the cycle-by-cycle current limit function, the TPS61378-Q1 also has output short protection.

During normal working condition, when output draws an excessive amount of current, causing the low-side FET to reach peak current limit and the output voltage is pulled below the input voltage, the device enters short circuit protection mode, triggering the hiccup timer. When the hiccup timer is active, the device limits the current for 1.8 ms and then shuts down. After 67 ms, it restarts.

During start-up, whether normal start-up or hiccup restart, the device can trigger short protection. The device has limited loading capacity at start up phase because of smaller peak current limit, which is list in 表 7-1.

Starting up with heavy load or very large capacitors at output side may causes short hiccup protection.

7.3.13 Power-Good Indicator

The TPS61378-Q1 integrates a power-good function. The power-good output consists of an open-drain NMOS, requiring an external pullup resistor connect to a suitable voltage supply like VCC. The PG pin goes high with a typical 3.4-ms delay time after VOUT reaches 90% of the target output voltage. When the output voltage drops below 85% of the target output voltage, the PG pin immediately goes low without delay.

7.3.14 Thermal Shutdown

A thermal shutdown is implemented to prevent damage due to excessive heat and power dissipation. Typically, the thermal shutdown occurs at junction temperatures exceeding 165°C. When the thermal shutdown is triggered, the device stops switching and recovers when the junction temperature falls below 145°C (typical).

7.4 Device Functional Modes

7.4.1 Forced PWM Mode

The TPS61378-Q1 enters forced PWM mode by pulling the MODE/SYNC pin to logic high for more than five switching cycles. In forced PWM mode, the TPS61378-Q1 keeps the switching frequency constant at light load condition. When the load current decreases, the output of the internal error amplifier also decreases to keep the inductor peak current down. When the output current decreases further, the high-side switch is not turned off even if the current of the high-side switch goes negative to keep the frequency constant.

7.4.2 Auto PFM Mode

The TPS61378-Q1 enters auto PFM Mode by pulling the MODE/SYNC pin to logic low for more than five switching cycles or leaving the pin floating. The TPS61378-Q1 improves the efficiency at light load when operating in PFM mode. When the output current decreases to a certain level, the output voltage of the error amplifier is clamped by the internal circuit. If the output current reduces further, the inductor current through the high-side switch will be clamped but not lowered further. Pulses are skipped to improve the efficiency at light load.

7.4.3 External Clock Synchronization

The TPS61378-Q1 supports external clock synchronization with a range of 200 kHz to 2.2 MHz. The external clock needs to be within -+20% of the setting frequency to ensure a reliable synchronization. The TPS61378-Q1 remains in forced PWM mode and operates in CCM across the entire load range if the oscillator is synchronized by an external clock. The spread spectrum feature is disabled when external synchronization is used.

7.4.4 Down Mode

The TPS61378-Q1 features down mode operation when input voltage is close to or higher than output voltage. In down mode, output voltage is regulated at target value, even when V_{IN} > V_O. The TPS61378-Q1 high-side and low-side FETs are switching devices that always work in boost operation, where the isolation FET always works as a linear device.

For boost circuits, on-time or duty cycle is reduced as input voltage approaches output voltage. The TPS61378-Q1 enters down mode when V_{IN} reaches 85% (typical) of V_O voltage at 2.2 MHz. Exiting down mode requires V_{IN} to be reduced below 85% (typical) of V_O voltage at 2.2 MHz.

In normal operation, the isolation FET is fully on.

When down mode is triggered and V_{IN} is less than VO pin voltage, the OUT pin has a fixed 2 V (typical) above VO pin voltage. An isolation FET works in LDO mode to regulate VO pin voltage with a 2-V constant voltage drop.

When down mode is triggered and V_{IN} is 100 mV (typical) higher than VO pin voltage, the OUT pin has an approximated 3 V (typical) above the V_{IN} pin voltage. As V_{IN} keeps rising, the OUT pin continues rising with 3 V on top of V_{IN}. In addition, an isolation FET works in LDO mode to regulate VO pin voltage with a voltage differential of the OUT pin and VO pin.

Refer to 图 7-1.

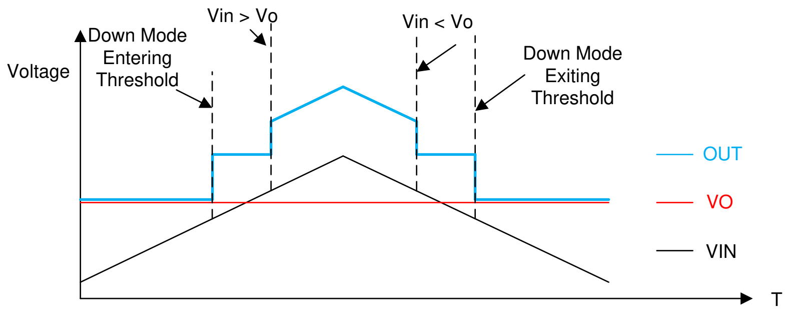


图 7-1. Down Mode

Take care during short-to-ground condition when operation V_{IN} is above 6 V. During hiccup on, the device operates in down mode and the isolation FET voltage drop is V_{IN} + 3 V (OUT pin to VO pin).

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS61378-Q1 is a 25-μA quiescent current boost converter that supports a 2.3-V to 14-V input voltage range. The device also supports load disconnect to minimize the leakage current. The following design procedure can be used to select component values for the TPS61378-Q1.

8.2 Typical Application

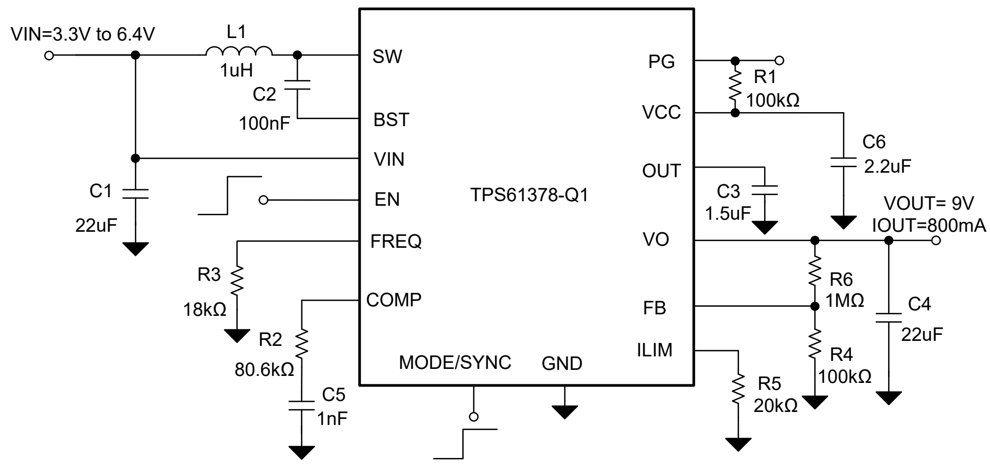


图 8-1. Typical Application

8.2.1 Design Requirements

A typical application example is dual cameras powered through a coax cable, which normally requires 9.0-V output as its bias voltage and consumes less than 600 mA current. 800-mA load current is designed to provide margin. The following design procedure can be used to select external component values for the TPS61378-Q1.

表 8-1. Design Requirements

PARAMETERS	VALUES
Input Voltage	3.3 V to 6.4 V
Output Voltage	9.0 V
Switching Frequency	2.2 MHz
Output Current	800 mA
Output Voltage Ripple	± 25 mV

8.2.2 Detailed Design Procedure

8.2.2.1 Programming the Output Voltage

The output voltage is determined by the resistor sensed from FB pin before device is enabled.

There are two ways to set the output voltage of the TPS61378-Q1, adjustable output voltage(for TPS61378-Q1 and TPS613783-Q1 only) and fixed output voltage.

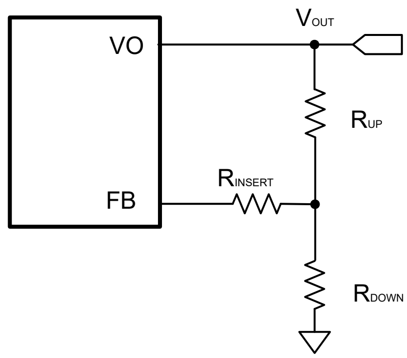


图 8-2. Typical Connection of FB Pin For Adjustable Output Voltage

图 8-2 shows the typical circuit of the FB pin conncetion for adjustable output voltage. The FB resistor R_{FB} is defined as 方程式 3:

$$R_{FB} = R_{INSERT} + \frac{R_{UP} \times R_{DOWN}}{R_{UP} + R_{DOWN}} \tag{3}$$

When selected for adjustable output voltage, R_{FB} must be above 14.4kΩ. The FB pin is connected to the negative input of the internal error amplifier directly. The output voltage can be programmed by adjusting the external resistor divider R_{UP} and R_{DOWN} according to 方程式 4.

$$V_{OUT} = V_{REF} \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}} \tag{4}$$

方程式 4 shows that the output voltage setting is only influenced by R_{UP} and R_{DOWN}. In normal application, R_{INSERT} can be 0Ω, that is, directly connect FB pin to middle point of feedback voltage divider.

For automotive application that do not prefer to use resistors more than 100 kΩ, R_{INSERT} (>15kΩ) can be used so that calculated R_{UP} and R_{DOWN} feedback resistor value could be less than 100kΩ.

When working with adjustable voltage, for the best accuracy, R_{DOWN} is recommended to be smaller than 160 kΩ to ensure that the current flowing through R_{DOWN} is at least 100 times larger than FB pin leakage current. Changing R_{DOWN} towards the lower value increases the robustness against noise injection. Changing R_{DOWN} to higher values reduces the quiescent current to achieve higher efficiency at light load.

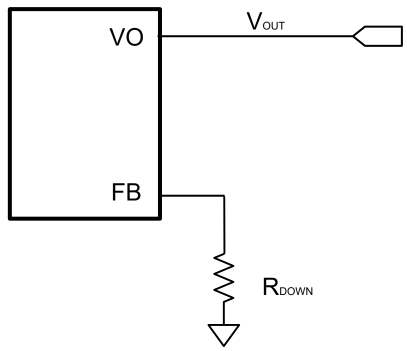


图 8-3. Typical Connection of FB Pin For Fixed Output Voltage

图 8-3 shows the typical circuit of the FB pin conncetion for fixed output voltage.The FB resistor R_{FB} is defined as 方程式 5:

$$R_{FB} = R_{DOWN} \tag{5}$$

When designed for fixed output voltage, the TPS61378-Q1 uses the internal resistor divider and works with fixed output voltage. The TPS61378-Q1 subdivides the voltage due to R_{FB} and device part number. See Device Comparison Table for detailed information.

8.2.2.2 Setting the Switching Frequency

The switching frequency of the TPS61378-Q1 is set at 2.2 MHz. Use 方程式 1 to calculate the required resistor value. The calculated value is 18 kΩ to get the frequency of 2.2 MHz.

8.2.2.3 Setting the Current Limit

The current limit of the TPS61378-Q1 can be programmed by an external resistor. For a target current limit of 4.8 A, use 方程式 2. The calculated resistor value is 20 kΩ.

8.2.2.4 Selecting the Inductor

A boost converter normally requires two main passive components for storing energy during power conversion: an inductor and an output capacitor. The inductor affects the steady state efficiency (including the ripple and efficiency), transient behavior, and loop stability, which makes the inductor the most critical component in application.

When selecting the inductor and the inductance, the other important parameters are:

- The maximum current rating (RMS and peak current should be considered)
- The series resistance
- Operating temperature

The TPS61378-Q1 has built-in slope compensation to avoid subharmonic oscillation associated with current mode control. If the inductor value is too low and makes the inductor peak-to-peak ripple higher than 2 A, the slope compensation may not be adequate, and the loop can be unstable. Therefore, it is recommended to make the peak-to-peak current ripple between 800 mA to 2 A when selecting the inductor.

The inductance can be calculated by 方程式 6, 方程式 7, and 方程式 8:

$$\Delta I_L = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{6}$$

$$\Delta I_{L\_R} = \text{Ripple\%} \times \frac{V_{OUT} \times I_{OUT}}{\eta \times V_{IN}} \tag{7}$$

$$L = \frac{1}{\text{Ripple \%}} \times \frac{\eta \times V_{IN}}{V_{OUT} \times I_{OUT}} \times \frac{V_{IN} \times D}{f_{SW}} \tag{8}$$

where

- Δ_{IL} is the peak-peak inductor current ripple
- V_{IN} is the input voltage
- D is the duty cycle
- L is the inductor
- f_{SW} is the switching frequency
- Ripple % is the ripple ration versus the DC current
- V_{OUT} is the output voltage
- I_{OUT} is the output current
- η is the efficiency

The current flowing through the inductor is the inductor ripple current plus the average input current. During power up, load faults, or transient load conditions, the inductor current can increase above the peak inductor current calculated.

Inductor values can have ±20%, or even ±30%, tolerance with no current bias. When the inductor current approaches the saturation level, the inductance can decrease 20% to 35% from the value at 0-A bias current, depending on how the inductor vendor defines saturation. When selecting an inductor, make sure the rated current, especially the saturation current, is larger than its peak current during the operation.

The inductor peak current varies as a function of the load, switching frequency, and input and output voltages. The peak current can be calculated with 方程式 9 and 方程式 10.

$$I_{PEAK} = I_{IN} + \frac{1}{2} \times \Delta I_L \tag{9}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{IN} is the input average current
- Δ_{IL} is the ripple current of the inductor

The input DC current is determined by the output voltage. The output current can be calculated by:

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{10}$$

where

- I_{IN} is the input current of the inductor
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- η is the efficiency

While the inductor ripple current depends on the inductance, the frequency, the input voltage, and duty cycle are calculated by 方程式 6. Replace 方程式 6 and 方程式 10 into 方程式 9 and get the inductor peak current:

$$I_{PEAK} = \frac{I_{OUT}}{(1-D) \times \eta} + \frac{1}{2} \times \frac{V_{IN} \times D}{L \times f_{SW}} \tag{11}$$

where

- I_{PEAK} is the peak current of the inductor
- I_{OUT} is the output current
- D is the duty cycle
- η is the efficiency
- V_{IN} is the input voltage
- L is the inductor
- f_{SW} is the switching frequency

The heat rating current (RMS) is can be calculated with 方程式 12:

$$I_{L\_RMS} = \sqrt{I_{IN}^2 + \frac{1}{12}(\Delta I_L)^2} \tag{12}$$

where

- I_{L_RMS} is the RMS current of the inductor
- I_{IN} is the input current of the inductor
- Δ_{IL} is the ripple current of the inductor

It is important that the peak current does not exceed the inductor saturation current and the RMS current is not over the temperature-related rating current of the inductors.

For a given physical inductor size, increasing inductance usually results in an inductor with lower saturation current. The total losses of the coil consists of the DC resistance (DCR) loss and the following frequency-dependent loss:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

For a certain inductor, the larger current ripple (smaller inductor) generates the higher DC and also the frequency-dependent loss. An inductor with lower DCR is basically recommended for higher efficiency. However, it is usually a tradeoff between the loss and foot print. 表 8-2 lists some recommended inductors.

表 8-2. Recommended Inductors

PART NUMBER	L (μH)	DCR TYP (mΩ) MAX	SATURATION CURRENT (A)	SIZE (L × W × H mm)	VENDOR[(1)]
XEL4030-471MEB	0.47	4.1	15.5	4 x 4 x 3	Coilcraft
XEL4030-102MEB	1	8.9	9	4 x 4 x 3	Coilcraft
DFE2HCAHR47MJ0L	0.47	25	5.1	2.5 x 2 x 1.2	Murata
DFE322520FD-1R0M	1	22	7.5	3.2 x 2.5 x 2	Murata
TFM322512ALMAR47MTAA	0.47	16	7.6	3.2 x 2.5 x 1.2	TDK
TFM322512ALMA1R0MTAA	1	30	5.1	3.2 x 2.5 x 1.2	TDK

(1) See the *Third-party Products Disclaimer*.

8.2.2.5 Selecting the Output Capacitors

The output capacitor is mainly selected to meet the requirements at load transient or steady state. The loop is compensated for the output capacitor selected. The output ripple voltage is related to the equivalent series resistance (ESR) of the capacitor and its capacitance. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by 方程式 13:

$$C_{OUT} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f_{SW} \times \Delta V \times V_{OUT}} \quad (13)$$

where

- C_{OUT} is the output capacitor
- I_{OUT} is the output current
- V_{OUT} is the output voltage
- V_{IN} is the input voltage
- Δ_V is the output voltage ripple required
- f_{SW} is the switching frequency

The additional output ripple component caused by ESR is calculated by 方程式 14:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (14)$$

where

- ΔV_{ESR} is the output voltage ripple caused by ESR
- R_{ESR} is the resistor in series with the output capacitor

For the ceramic capacitor, the ESR ripple can be neglected. However, for the tantalum or electrolytic capacitors, it must be considered if used.

The minimum ceramic output capacitance needed to meet a load transient requirement can be estimated using 方程式 15:

$$C_{OUT} = \frac{\Delta I_{STEP}}{2\pi \times f_{BW} \times \Delta V_{TRAN}} \tag{15}$$

where

- ΔI_{STEP} is the transient load current step
- ΔV_{TRAN} is the allowed voltage dip for the load current step
- f_{BW} is the control loop bandwidth (that is, the frequency where the control loop gain crosses zero)

For the output capacitor on the OUT pin, the effective capacitance is recommended between 0.22 μF to 1 μF.

Take care when evaluating the derating of a ceramic capacitor under the DC bias. Ceramic capacitors can derate by as much as 70% of the capacitance at the respective rated voltage. Therefore, enough margins on the voltage rating must be considered to ensure adequate capacitance at the required output voltage.

8.2.2.6 Selecting the Input Capacitors

Multilayer ceramic capacitors are an excellent choice for the input decoupling of the step-up converter since they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 22-μF input capacitor or equivalent is sufficient for the most applications, larger values can be used to reduce input current ripple.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the device. Additional "bulk" capacitance (electrolytic or tantalum) in this circumstance, must be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

8.2.2.7 Loop Stability and Compensation

8.2.2.7.1 Small Signal Model

The TPS61378-Q1 uses the fixed frequency peak current mode control. There is an internal adaptive slope compensation to avoid subharmonic oscillation. With the inductor current information sensed, the small-signal model of the power stage reduces from a two-pole system, created by L and C_{OUT}, to a single-pole system, created by R_{OUT} and C_{OUT}. The single-pole system is easily used with the loop compensation. 图 8-4 shows the equivalent small signal elements of a boost converter.

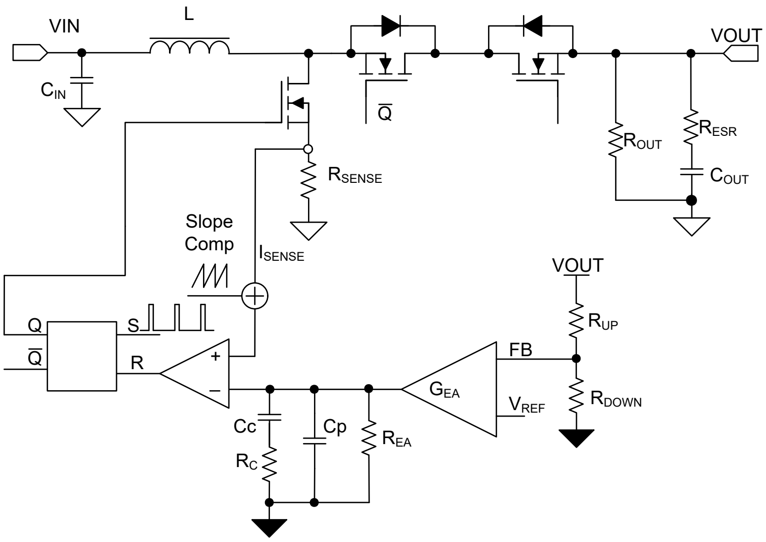


图 8-4. TPS61378-Q1 Control Equivalent Circuitry Model

The small signal of power stage is:

$$K_{PS}(S) = \frac{R_{OUT} \times (1 - D)}{2 \times R_{SENSE}} \times \frac{(1 + \frac{S}{2\pi \times f_{ESR}})(1 - \frac{S}{2\pi \times f_{RHP}})}{(1 + \frac{S}{2\pi \times f_P})} \tag{16}$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- R_{SENSE} is the equivalent internal current sense resistor, which is typically 118 mΩ

The single pole of the power stage is:

$$f_P = \frac{2}{2\pi \times R_{OUT} \times C_{OUT}} \tag{17}$$

where

- C_{OUT} is the output capacitance. For a boost converter having multiple identical output capacitors in parallel, simply combine the capacitors with the equivalent capacitance

The zero created by the ESR of the output capacitor is:

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{18}$$

where

- R_{ESR} is the equivalent resistance in series of the output capacitor

The right-hand plane zero is:

$$f_{RHP} = \frac{R_{OUT} \times (1 - D)^2}{2\pi \times L} \tag{19}$$

where

- D is the duty cycle
- R_{OUT} is the output load resistor
- L is the inductance

方程式 20 shows the equation for feedback resistor network and the error amplifier.

$$H_{EA}(S) = G_{EA} \times R_{EA} \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}} \times \frac{1 + \frac{S}{2 \times \pi \times f_Z}}{(1 + \frac{S}{2 \times \pi \times f_{P1}}) \times (1 + \frac{S}{2 \times \pi \times f_{P2}})} \tag{20}$$

where

- R_{EA} is the output impedance of the error amplifier, typically R_{EA} = 500 MΩ
- f_{P1}, f_{P2} is the pole's frequency of the compensation
- f_Z is the zero’ s frequency of the compensation network

$$f_{P1} = \frac{1}{2\pi \times R_{EA} \times C_c} \tag{21}$$

where

- C_C is the zero capacitor compensation

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \tag{22}$$

where

- C_P is the pole capacitor compensation
- R_C is the resistor of the compensation network

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \tag{23}$$

8.2.2.7.2 Loop Compensation Design Steps

With the small signal models coming out, the next step is to calculate the compensation network parameters with the given inductor and output capacitance.

1. **Set the Crossover Frequency, f_C .**

   The first step is to set the loop crossover frequency, f_C. The higher the crossover frequency, the faster the loop response is. It is generally accepted that the loop gain crosses over no higher than the lower of either 1/10 of the switching frequency, f_{SW}, or 1/5 of the RHPZ frequency, f_{RHPZ}. Then, calculate the loop compensation network values of R_C, C_C, and C_P by the following equations.
2. **Set the Compensation Resistor, R_C .**

   By placing f_Z below f_C, for frequencies above f_C, R_C | | R_{EA} ~ = R_C, so R_C × G_{EA} sets the compensation gain. Setting the compensation gain, $K_{COMP\text{-}dB}$, at f_Z results in the total loop gain, $T_{(s)} = K_{PS(s)} \times H_{EA(s)}$, being zero at f_C.

Therefore, to approximate a single-pole rolloff up to f_{P2}, rearrange 方程式 20 to solve for RC so that the compensation gain, K_{EA}, at f_C is the negative of the gain, K_{PS}. Read at frequency f_C for the power stage bode plot or more simply:

$$K_{EA}(f_C) = 20 \times \log(G_{EA} \times R_C \times \frac{R_{DOWN}}{R_{UP} + R_{DOWN}}) = -K_{PS}(f_C) \tag{24}$$

where

- K_{EA} is gain of the error amplifier network
- K_{PS} is the gain of the power stage
- G_{EA} is the transconductance of the amplifier, the typical value of G_{EA} = 70 µA / V

3. **Set the Compensation Zero capacitor, C_C .**

   Place the compensation zero at the power stage R_{OUT} ,C_{OUT} pole’ s position to get:

$$f_Z = \frac{1}{2\pi \times R_C \times C_C} \tag{25}$$

$$C_C = \frac{R_{OUT} \times C_{OUT}}{2R_C} \tag{26}$$

4. **Set the Compensation Pole Capacitor, C_P .**

   Place the compensation pole at the zero produced by R_{ESR} and C_{OUT}. It is useful for canceling unhelpful effects of the ESR zero.

$$f_{P2} = \frac{1}{2\pi \times R_C \times C_P} \tag{27}$$

$$f_{ESR} = \frac{1}{2\pi \times R_{ESR} \times C_{OUT}} \tag{28}$$

   Set $f_{P2} = f_{ESR}$, and get:

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_C} \tag{29}$$

8.2.2.7.3 Selecting the Bootstrap Capacitor

The bootstrap capacitor between the BST and SW pin supplies the gate current to charge the high-side FET device gate during the turnon of each cycle. The gate current also supplies charge for the bootstrap capacitor. The recommended value of the bootstrap capacitor is 0.1 µF to 1 µF. C_{BST} must be a good quality, low-ESR ceramic capacitor located at the pins of the device to minimize potentially damaging voltage transients caused by trace inductance. A value of 0.1 µF was selected for this design example.

8.2.2.7.4 V_{CC} Capacitor

The primary purpose of the V_{CC} capacitor is to supply the peak transient currents of the driver and bootstrap capacitor and provide stability for the V_{CC} regulator. The value of C_{VCC} must be at least 10 times greater than the value of C_{BST}, and must be a good quality, low-ESR ceramic capacitor. C_{VCC} must be placed close to the pins of the IC to minimize potentially damaging voltage transients caused by the trace inductance. A value of 2.2 µF was selected for this design example.

8.2.3 Application Curves

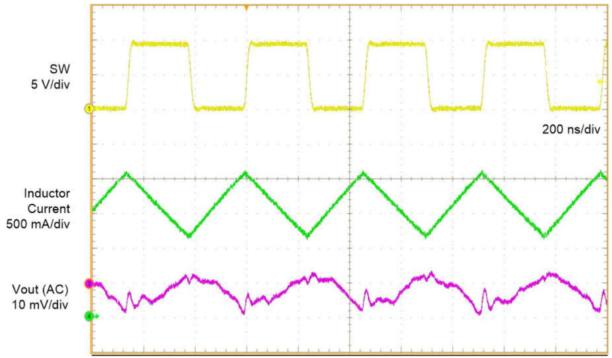


图 8-5. Switching Waveform V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 800 mA, FPWM

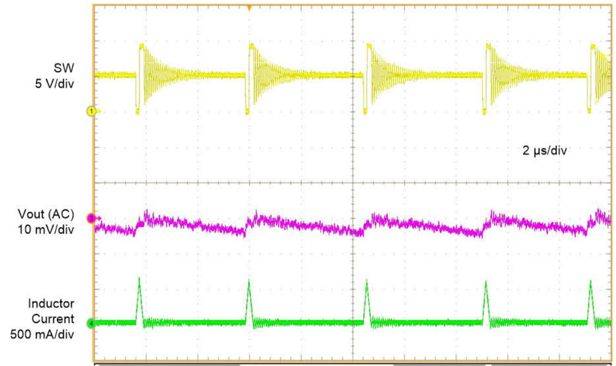


图 8-6. Switching Waveform V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 0 mA, Auto PFM

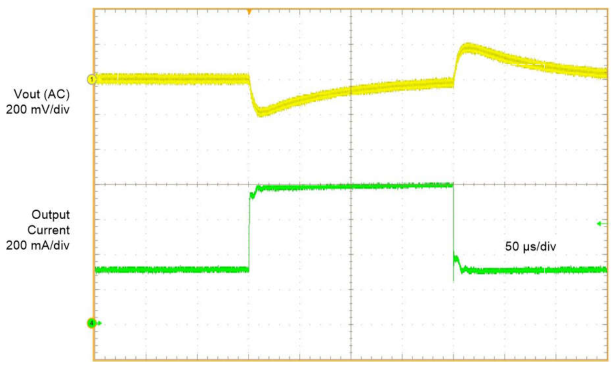


图 8-7. Load Transient V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 300 mA to 800 mA, FPWM

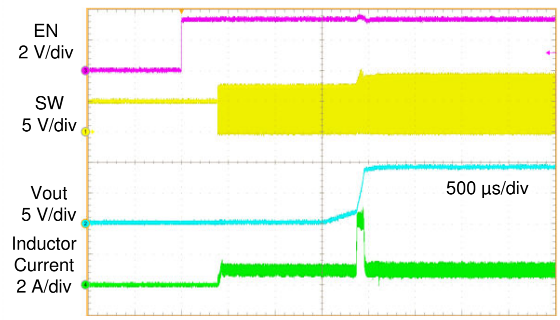


图 8-8. Start-up from EN Waveform V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 500 mA, FPWM

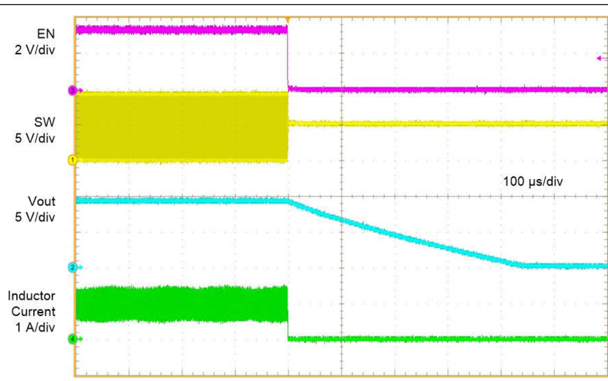


图 8-9. Shutdown from EN Waveforms V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 500 mA, FPWM

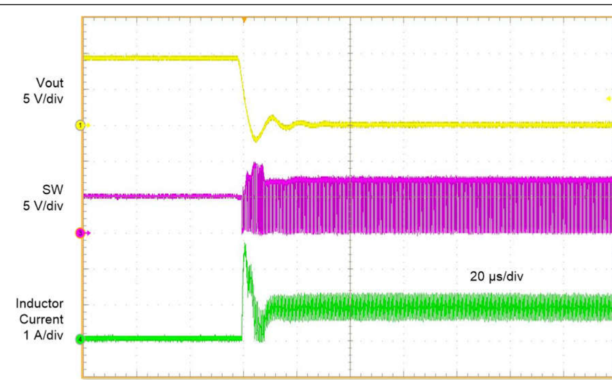


图 8-10. Short Circuit Protection V_{IN} = 5 V, V_{OUT} = 9 V, FPWM

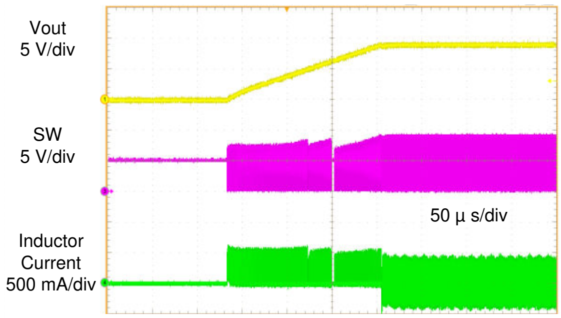


图 8-11. Short Circuit Recovery V_{IN} = 5 V, V_{OUT} = 9 V, I_{OUT} = 0 mA, FPWM

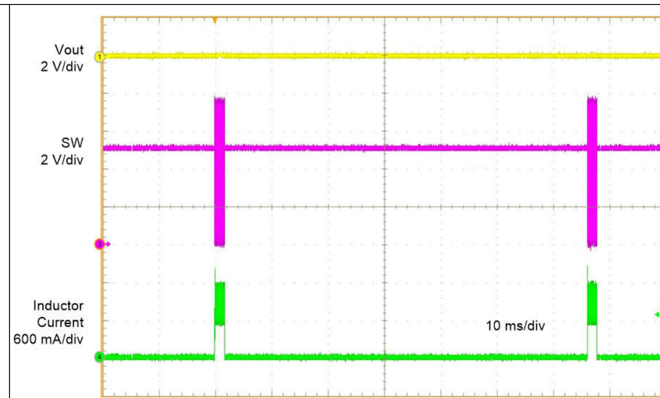


图 8-12. Hiccup Short Circuit Protection V_{IN} = 5 V, V_{OUT} = 9 V, FPWM

9 Power Supply Recommendations

The TPS61378-Q1 is designed to operate from an input voltage supply range between 2.3 V to 14 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device, the bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator can show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor must be placed as close as possible to the IC.

10.2 Layout Example

The bottom layer is a large GND plane connected by vias.

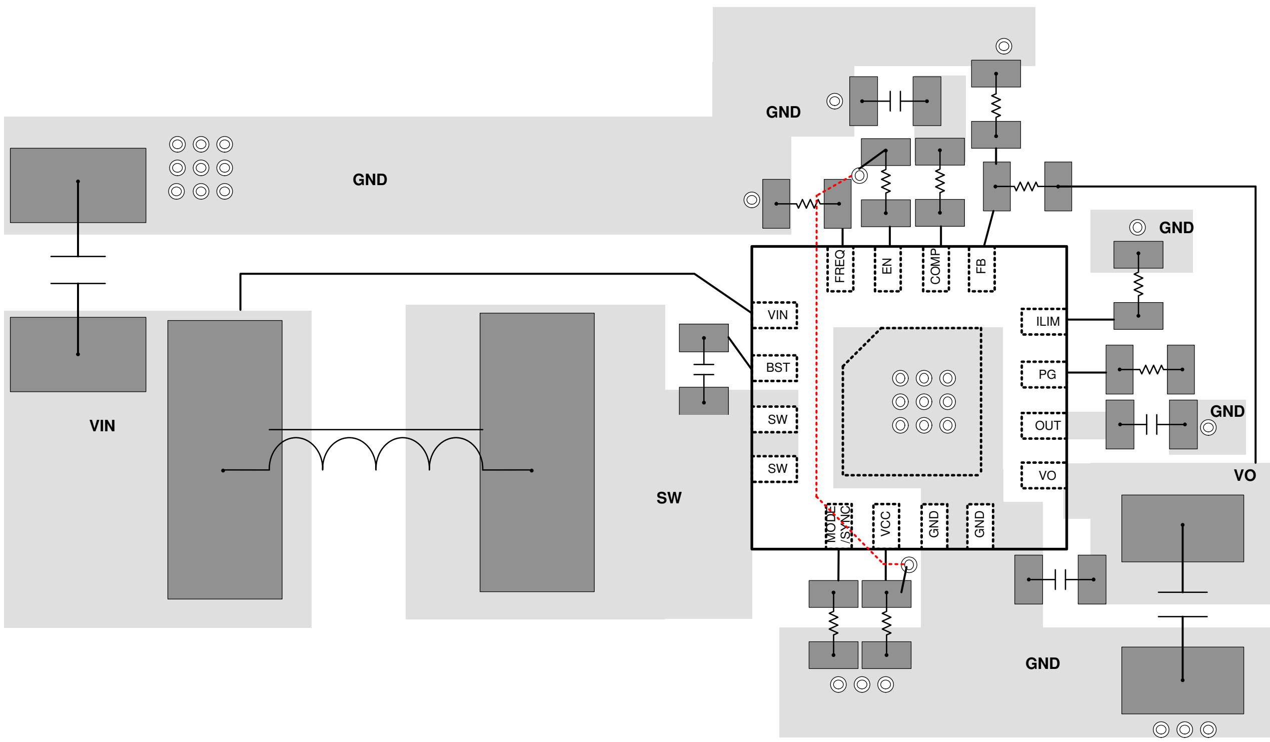


图 10-1. Recommended Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 第三方产品免责声明

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11.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

11.4 Trademarks

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所有商标均为其各自所有者的财产。

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12 Revision History

Changes from Revision D (October 2021) to Revision E (October 2024) — **Page**

- 添加了 TPS61378L....1
- 添加了额外特性....1
- 将封装更新为 WQFN-16....1
- Updated Output Voltage Selection Resistor in the Device Comparison Table....3
- Updated Error Amplifier units....6
- Updated 图 6-8....8
- Added additional information to Spread Spectrum Frequency Modulation....13
- Added 表 7-1....13
- Added additional information to Output Short Protection/Hiccup....14
- Added "The external clock needs to be within -+20% of the setting frequency to ensure a reliable synchronization."....15
- Updated 图 8-1....17
- Added additional information and 图 8-2 and 图 8-3....17

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS613783QWRTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2G8H
TPS613783QWRTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2G8H
TPS613785QWRTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2G9H
TPS613785QWRTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2G9H
TPS61378LQWRTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	61378L
TPS61378LQWRTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	61378L
TPS61378QWRTERQ1	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2ELH
TPS61378QWRTERQ1.A	Active	Production	WQFN (RTE) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2ELH

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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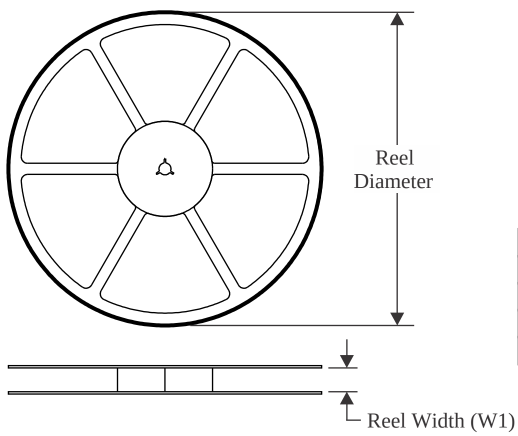
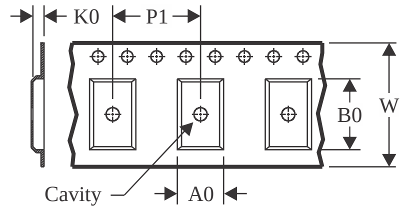
TAPE AND REEL INFORMATION

REEL DIMENSIONS

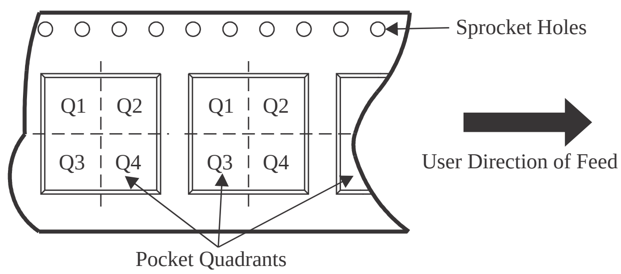


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

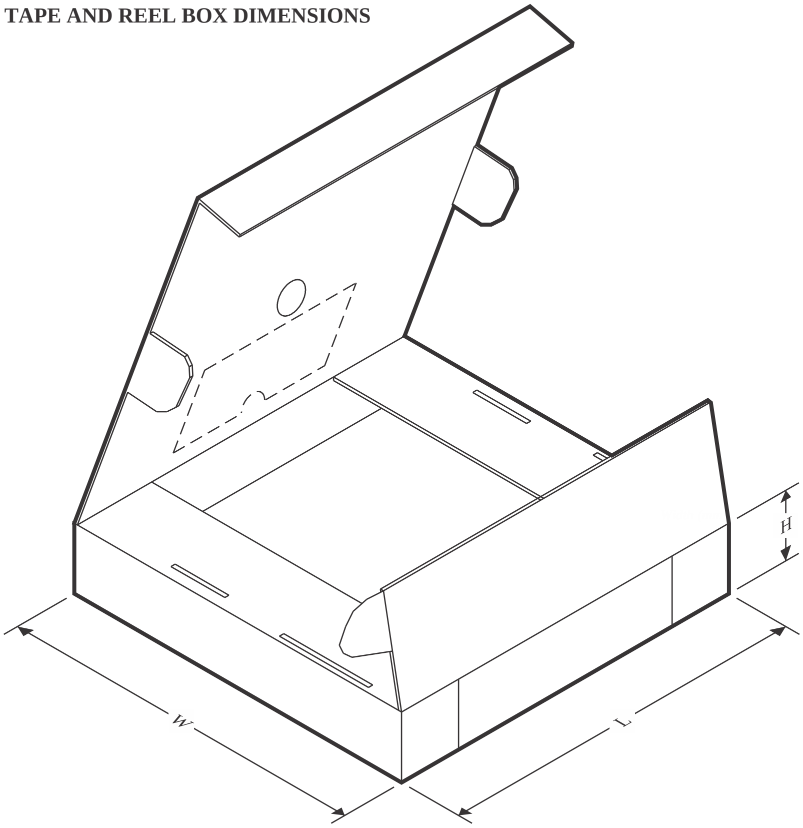
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS613783QWRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS613785QWRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61378LQWRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61378QWRTERQ1	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

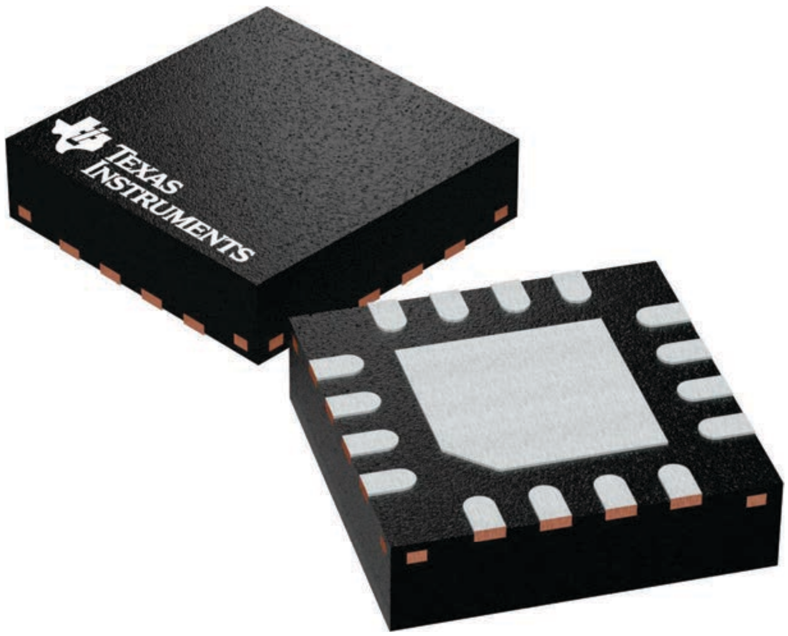
TAPE AND REEL BOX DIMENSIONS



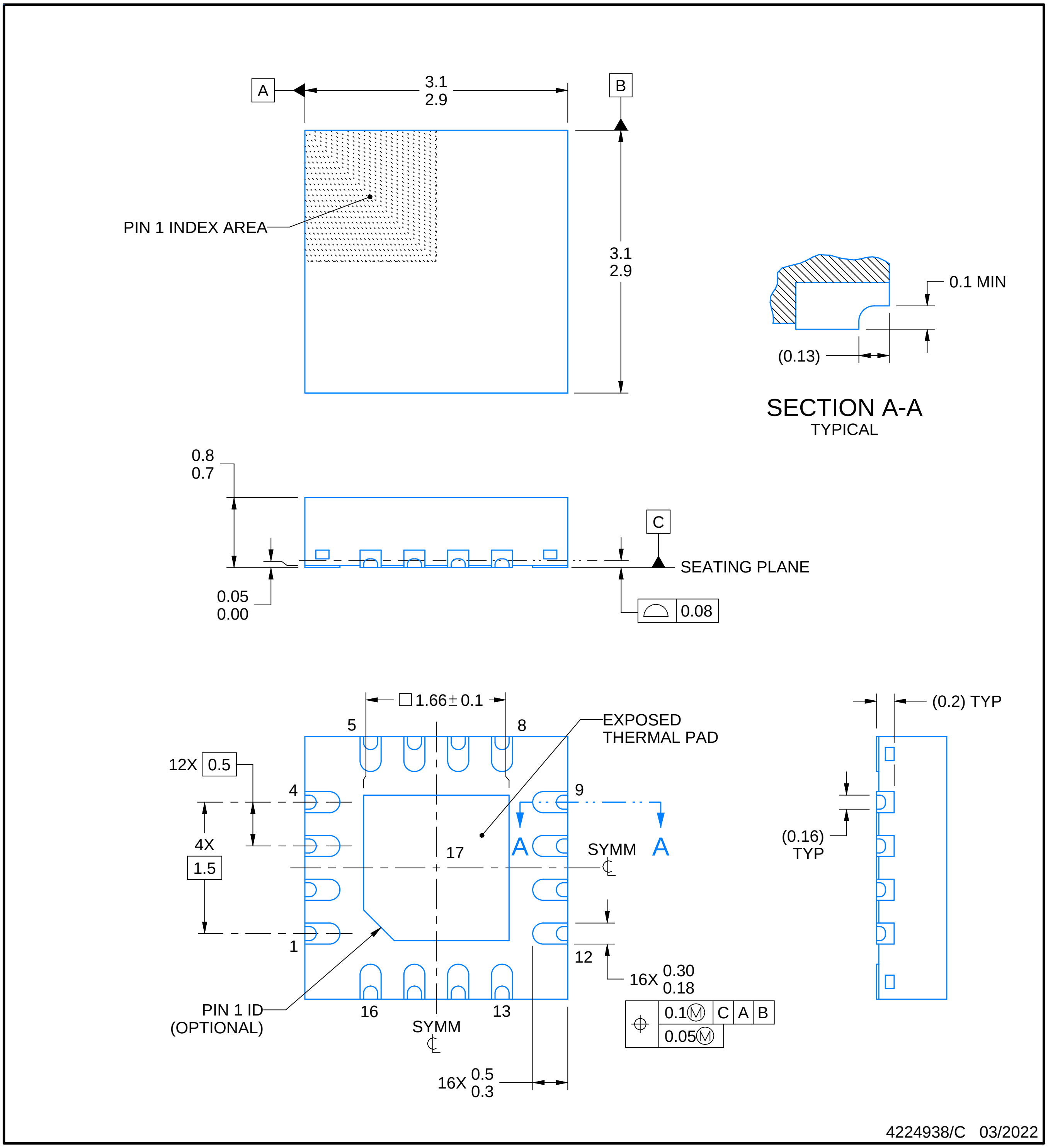
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS613783QWRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS613785QWRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS61378LQWRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0
TPS61378QWRTERQ1	WQFN	RTE	16	3000	367.0	367.0	35.0

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

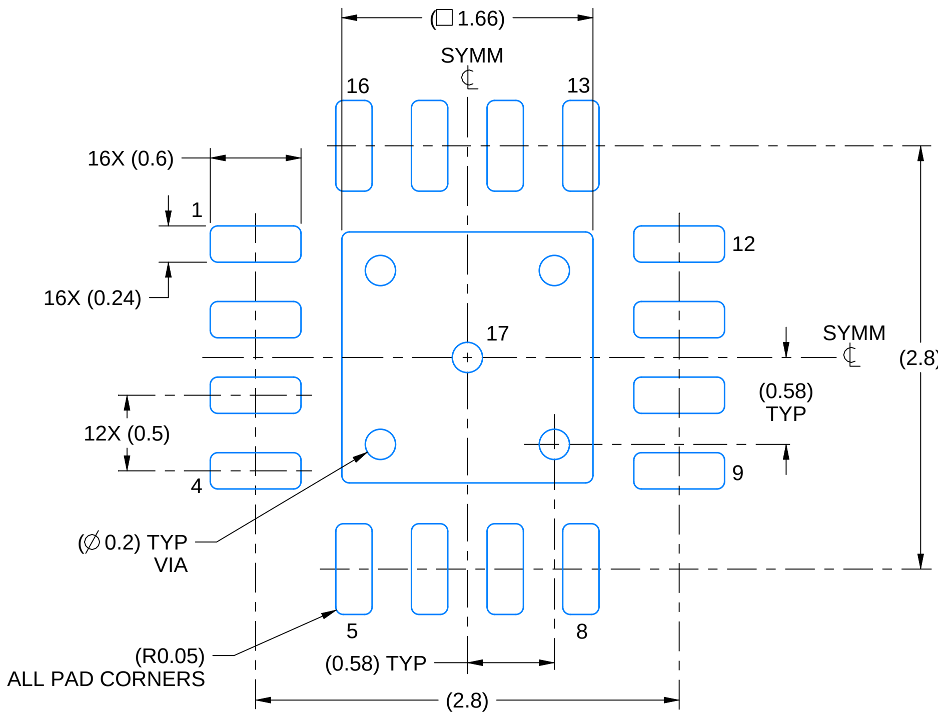


4225944/A

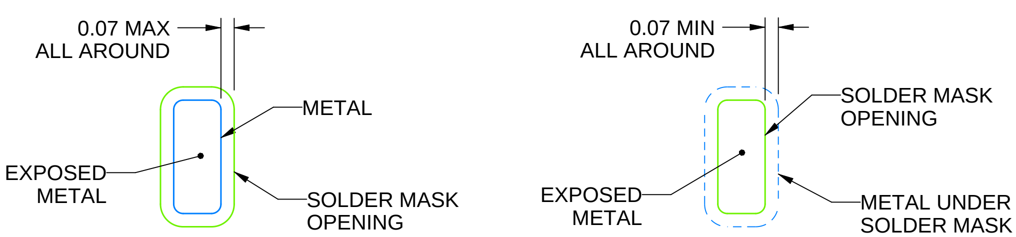


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

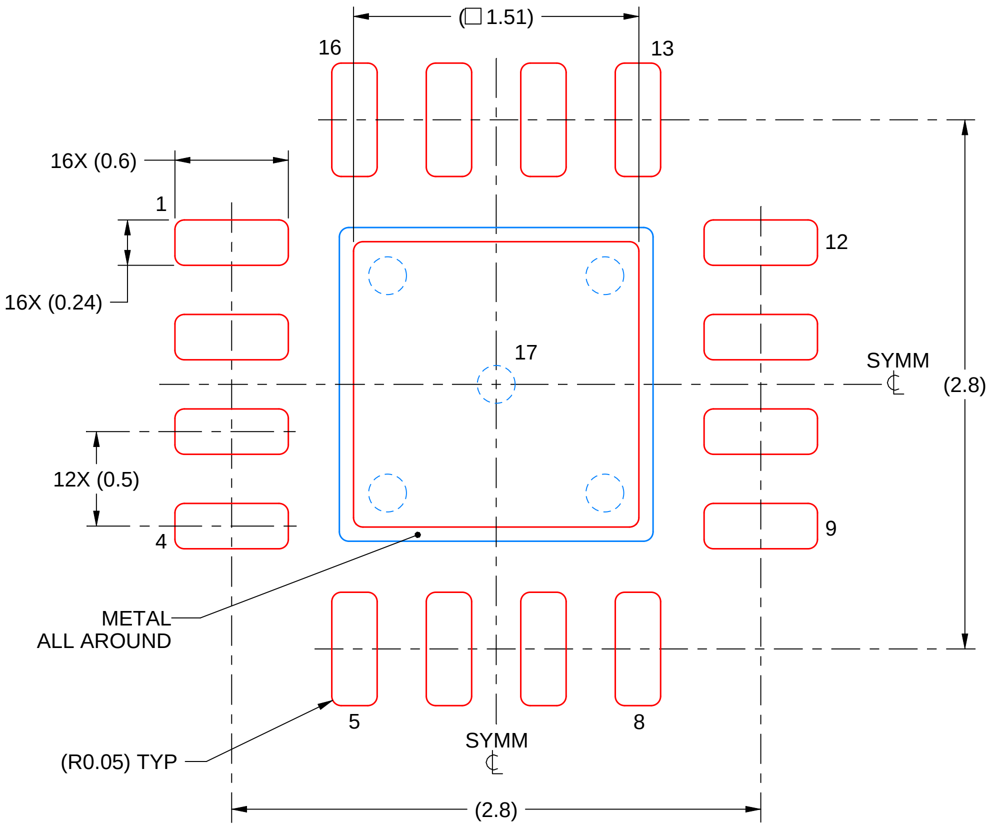
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224938/C 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



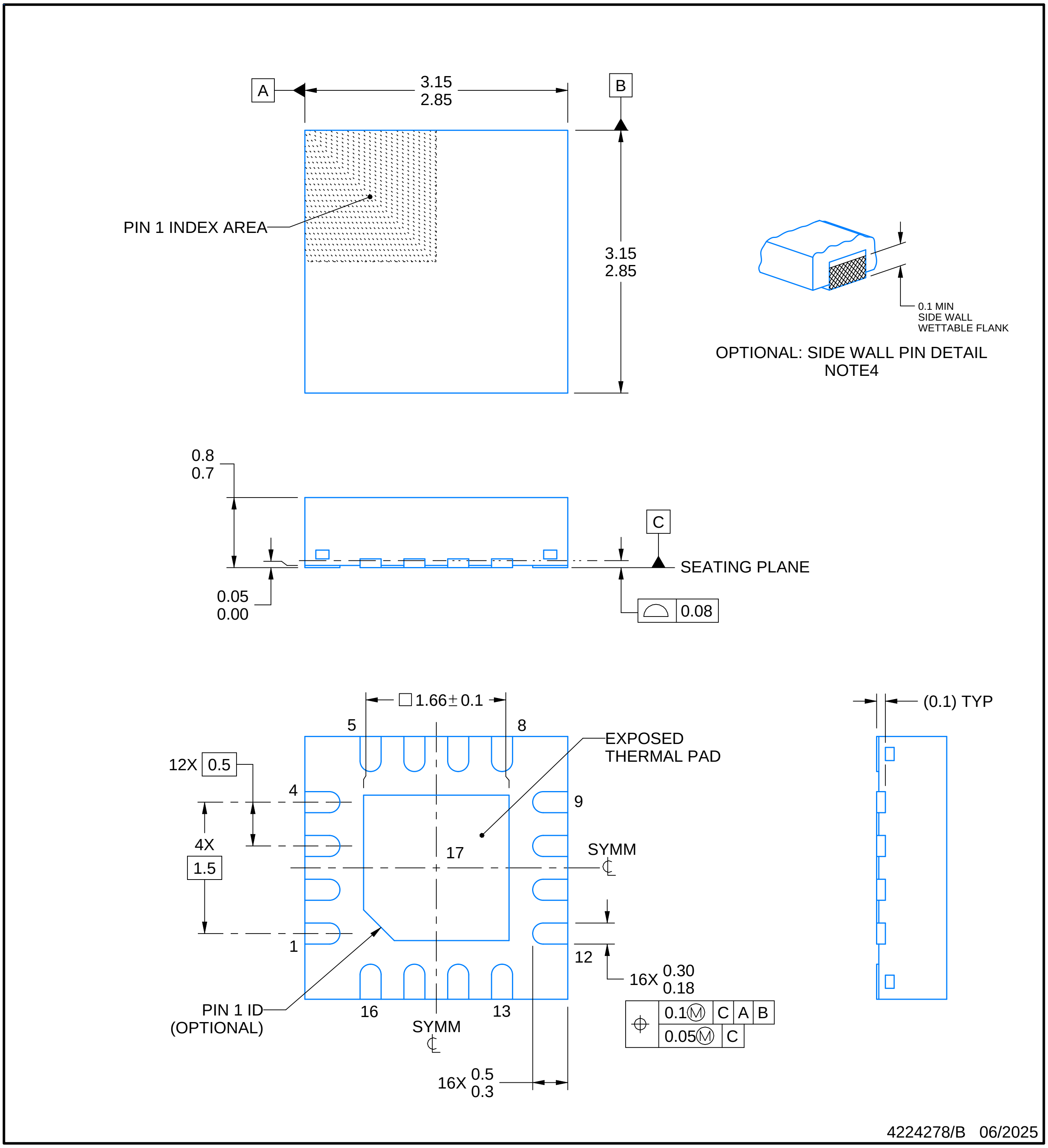
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4224938/C 03/2022

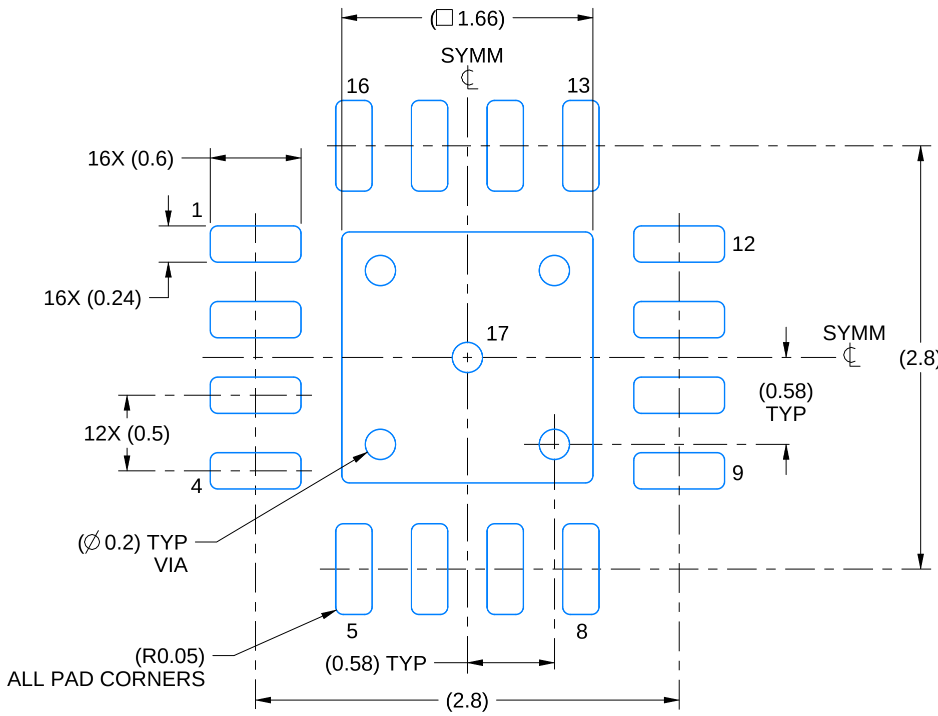
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

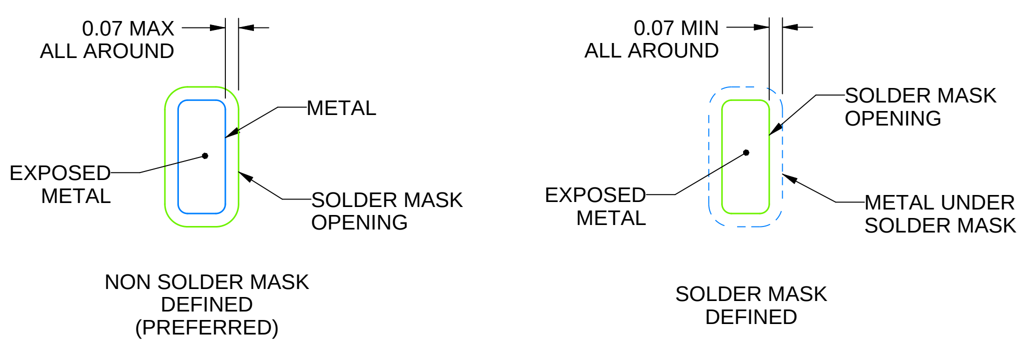


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

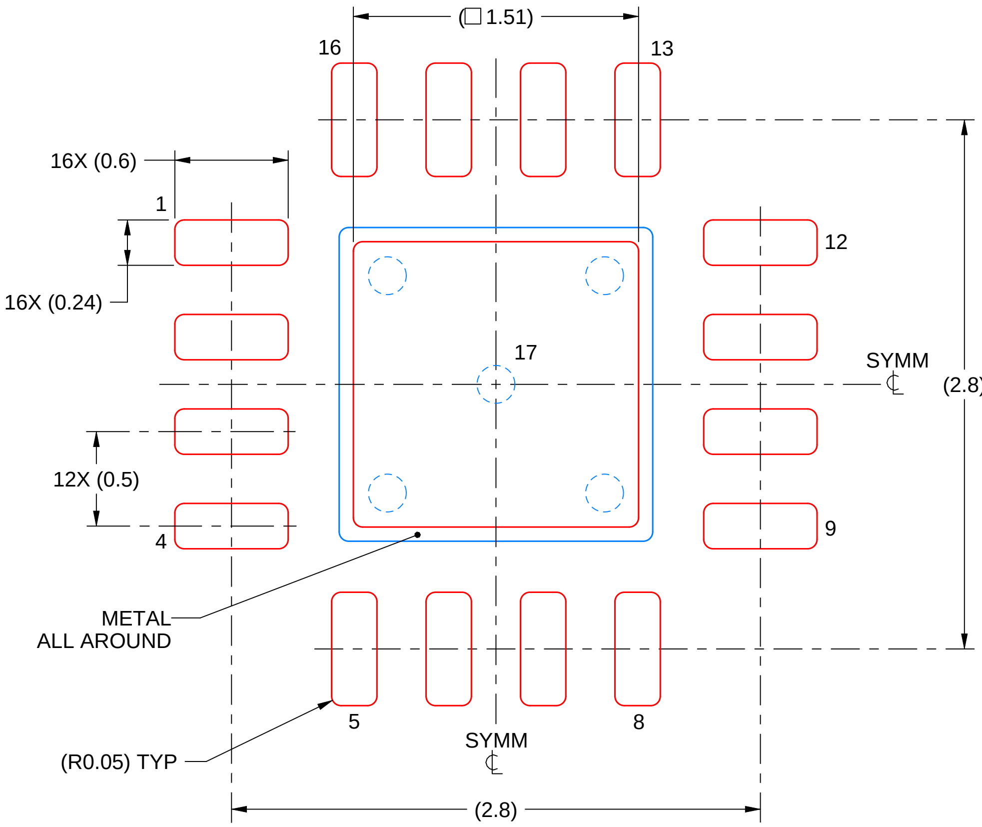


SOLDER MASK DETAILS

4224278/B 06/2025

NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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