TPS6124x 3.5-MHz High Efficiency Step-Up Converter

1 Features

- Efficiency > 90% at Nominal Operating Conditions
- Total DC Output Voltage Accuracy 5.0 V±2%
- Typical 30-µA Quiescent Current
- *Best in Class* Line and Load Transient
- Wide V_{IN} Range From 2.3 V to 5.5 V
- Output Current up to 450 mA
- Automatic PFM/PWM Mode Transition
- Low Ripple Power Save Mode for Improved Efficiency at Light Loads
- Internal Softstart, 250-µs Typical Start-Up Time
- 3.5-MHz Typical Operating Frequency
- Load Disconnect During Shutdown
- Current Overload and Thermal Shutdown Protection
- Three Surface-Mount External Components Required (One MLCC Inductor, Two Ceramic Capacitors)
- Total Solution Size <13 mm^2
- Available in a 6-Pin DSBGA and 2-mm × 2-mm WSON Package

2 Applications

- USB-OTG Applications
- Portable HDMI Applications
- Cell Phones, Smart Phones
- PDAs, Pocket PCs
- Portable Media Players
- Digital Cameras

3 Description

The TPS6124x device is a highly efficient synchronous step-up DC-DC converter optimized for products powered by either a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. The TPS6124x supports output currents up to 450 mA. The TPS61240 has an input valley current limit of 500 mA, and the TPS61241 has an input valley current of 600 mA.

With an input voltage range of 2.3 V to 5.5 V, the device supports batteries with extended voltage range and are ideal to power portable applications like mobile phones and other portable equipment. The TPS6124x boost converter is based on a quasi-constant on-time valley current mode control scheme.

The TPS6124x presents a high impedance at the V_{OUT} pin when shut down. This allows for use in applications that require the regulated output bus to be driven by another supply while the TPS6124x is shut down.

During light loads the device will automatically pulse skip allowing maximum efficiency at lowest quiescent currents. In the shutdown mode, the current consumption is reduced to less than 1 µA.

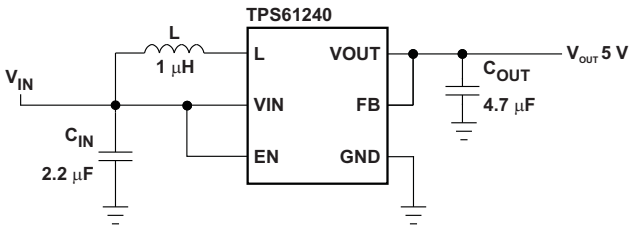
TPS6124x allows the use of small inductors and capacitors to achieve a small solution size. During shutdown, the load is completely disconnected from the battery. The TPS6124x is available in a 6-pin DSBGA and 2-mm × 2-mm WSON package.

Device Information(1)

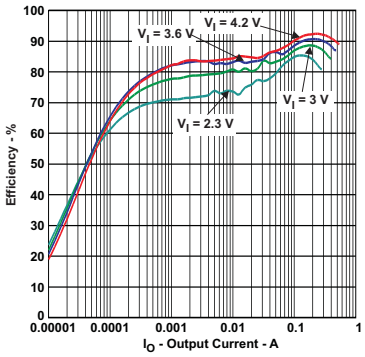
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61240	WSON (6)	2.00 mm × 2.00 mm
	DSBGA (6)	1.25 mm × 0.86 mm
TPS61241	DSBGA (6)	1.25 mm × 0.86 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



Efficiency vs Output Current



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

Changes from Revision C (December 2014) to Revision D **Page**

- Changed V_{IH} Description From: High level input voltage, EN To: High level input voltage threshold, EN in the *Electrical Characteristics* ... 5
- Changed V_{IL} Description From: Low level input voltage, EN To: Low level input voltage threshold, EN in the *Electrical Characteristics* ... 5

Changes from Revision B (February 2012) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

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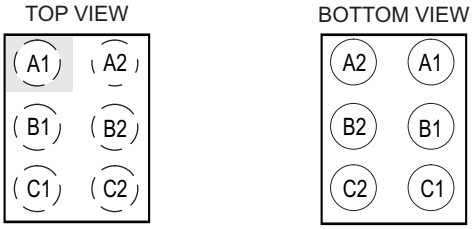
5 Device Options

PART NUMBER(1)	OUTPUT VOLTAGE	DEVICE SPECIFIC FEATURES
TPS61240	5 V	Supports 5 V, up to 250 mA loading down to 3.2 V input voltage
		Supports 5 V, up to 250 mA loading down to 3.2 V input voltage
TPS61241		Supports 5 V, up to 300 mA loading down to 3.2 V input voltage
TPS61242(2)		Optimized to drive an inductive load

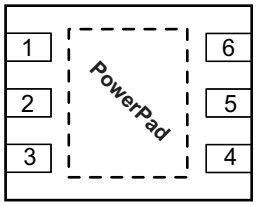
(1) See *Mechanical, Packaging, and Orderable Information* for ordering information.
(2) Product preview. Contact TI factory for more information.

6 Pin Configuration and Functions

DSBGA Package
6 Pins
Top View



WSON Package
6 Pins
Top View



Pin Functions

PIN			I/O	DESCRIPTION	REMARKS
NAME	WSON	DSGBA			
EN	4	C1	I	Enable	Positive polarity. Low = IC shutdown.
FB	3	C2	I	Feedback input	Feedback for regulation.
GND	1	A2	—	Ground	Power ground and IC ground
L	5	B1	I	Boost and rectifying switch input	Inductor connection to FETs
V_{IN}	6	A1	I	Supply voltage	Supply from battery
V_{OUT}	2	B2	O	Output	Connected to load

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7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_I	Input voltage on V_{IN}, L, EN	–0.3	7	V
	Voltage on V_{OUT}	–2.0	7	V
	Voltage on FB	–2.0	14	V
	Peak output current	Internally limited		A
T_J	Maximum operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(3)	±500	
		Machine model (MM)	±200	

(1) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range		2.3		5.5	V
L	Inductance		0.4	1	1.5	µH
C_O	Output capacitance	TPS61240 TPS61241	1		20	µF
		TPS61242	0.8		10	µF
T_A	Operating ambient temperature		–40		85	°C
T_J	Operating junction temperature		–40		125	

7.4 Thermal Information

THERMAL METRIC(1)		TPS6124x		UNIT
		YFF	DRV	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	132.7	104.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.2	97.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	74.0	
ψ_{JT}	Junction-to-top characterization parameter	5.2	4.5	
ψ_{JB}	Junction-to-board characterization parameter	22.4	74.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	48.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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7.5 Electrical Characteristics

Over full operating ambient temperature range, typical values are at T_A = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6V. External components C_{IN} = 2.2µF, C_{OUT} = 4.7µF 0603, L = 1µH, refer to Parameter Measurement Information section.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC-DC STAGE						
V_{IN}	Input voltage range		2.3		5.5	V
V_{OUT}	Fixed output voltage range	2.3 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 200 mA	4.9	5.0	5.1	V
V_{O_Ripple}	Ripple voltage, PWM mode	I_{LOAD} = 150 mA			20	mVpp
I_{SW}	Output current	V_{IN} 2.3 V to 5.5 V	200			mA
	Switch valley current limit	V_{OUT} = V_{GS} = 5.0 V (TPS61240)	500	600		mA
		V_{OUT} = V_{GS} = 5.0 V (TPS61241, TPS61242)	600	700		
	Short circuit current	V_{OUT} = V_{GS} = 5.0 V	200	350		mApk
	High side MOSFET on-resistance(1)	V_{IN} = V_{GS} = 5.0 V, T_A = 25°C(1)		290		mΩ
	Low Side MOSFET on-resistance(1)	V_{IN} = V_{GS} = 5.0 V, T_A = 25°C (1)		250		mΩ
	Operating quiescent current	I_{OUT} = 0 mA, Power save mode		30	40	µA
	Shutdown current	EN = GND			1.5	µA
	Reverse leakage current V_{OUT}	EN = 0, V_{OUT} = 5 V			2.5	µA
	Leakage current from battery to V_{OUT}	EN = GND			2.5	µA
	Line transient response	V_{IN} 600 mVp-p AC square wave, 200 Hz, 12.5% DC at 50/200 mA load		±25	±50	mVpk
	Load transient response	0–50 mA, 50–0 mA V_{IN} = 3.6V T_{Rise} = T_{Fall} = 0.1 µs		50		mVpk
		50–200 mA, 200–50 mA, V_{IN} = 3.6 V, T_{Rise} = T_{Fall} = 0.1 µs		150		
I_{IN}	Input bias current, EN	EN = GND or V_{IN}		0.01	1.0	µA
V_{UVLO}	Undervoltage lockout threshold	Falling		2.0	2.1	V
		Rising		2.1	2.2	V
CONTROL STAGE						
V_{IH}	High level input voltage threshold, EN	2.3 V ≤ V_{IN} ≤ 5.5 V			1.0	V
V_{IL}	Low level input voltage threshold, EN	2.3 V ≤ V_{IN} ≤ 5.5 V	0.4			V
OVC	Input overvoltage threshold	Falling		5.9		V
		Rising		6.0		
t_{Start}	Start-up time	Time from active EN to start switching, no-load until V_{OUT} is stable 5 V			300	µs
DC-DC STAGE						
f		See Figure 7 (Frequency Dependancy vs I_{OUT})		3.5		MHz
T_{SD}	Thermal shutdown	Increasing junction temperature		140		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		20		°C

(1) DRV package has an increased R_{DSon} of about 40mΩ due to bond wire resistance.

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7.6 Typical Characteristics

7.6.1 Table of Graphs

		Figure
Maximum Output Current	vs Input Voltage	Figure 1
Efficiency	vs Output Current, V_{out} = 5V, V_{in} = [2.3 V; 3.0 V; 3.6 V; 4.2 V]	Figure 2
	vs Input Voltage, V_{out} = 5 V, I_{out} = [100 µA; 1 mA; 10 mA; 100 mA; 200 mA]	Figure 3
Input Current	at No Output Load, Device Disabled	Figure 4
Output Voltage	vs Output Current, V_{out} = 5 V, V_{in} = [2.3 V; 3.0 V; 3.6 V; 4.2 V]	Figure 5
	vs Input Voltage	Figure 6
Frequency	vs Output Load, V_{out} = 5 V, V_{in} = [3.0 V; 4.0 V; 5.0 V]	Figure 7

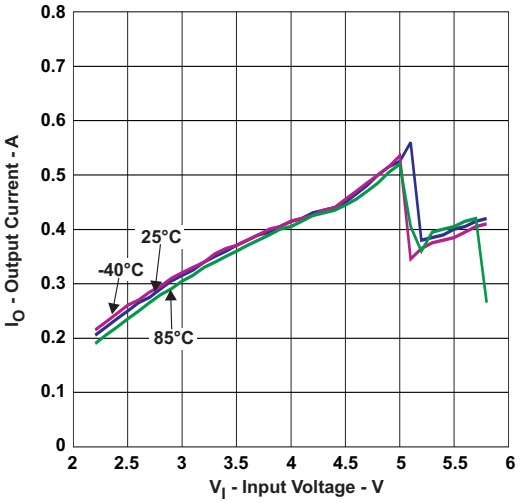


Figure 1. Maximum Output Current vs Input Voltage

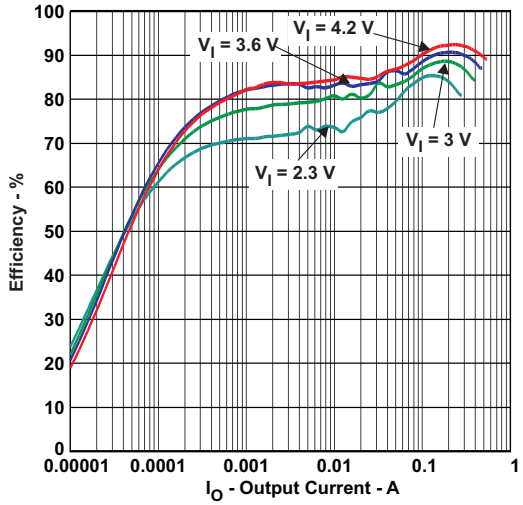


Figure 2. Efficiency vs Output Current

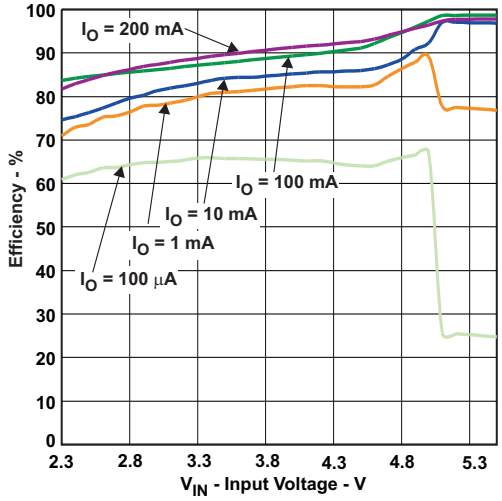


Figure 3. Efficiency vs Input Voltage

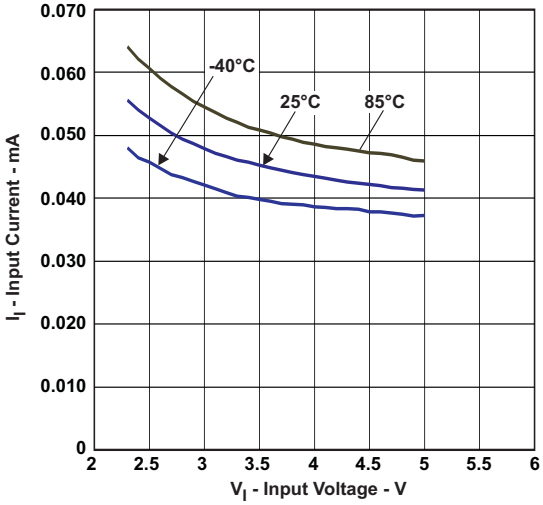


Figure 4. Input at No Output Load

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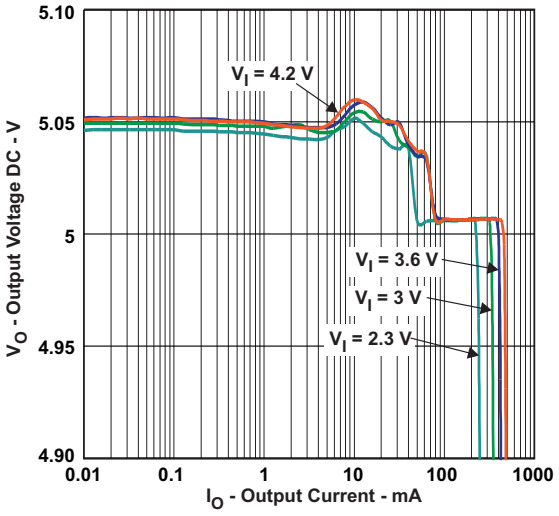


Figure 5. Output Voltage vs Output Current

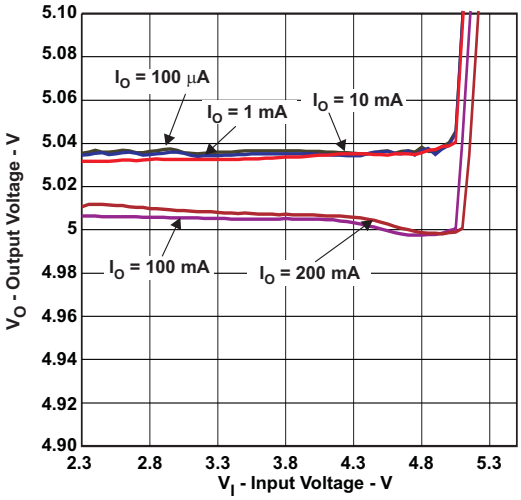


Figure 6. Output Voltage vs Input Voltage

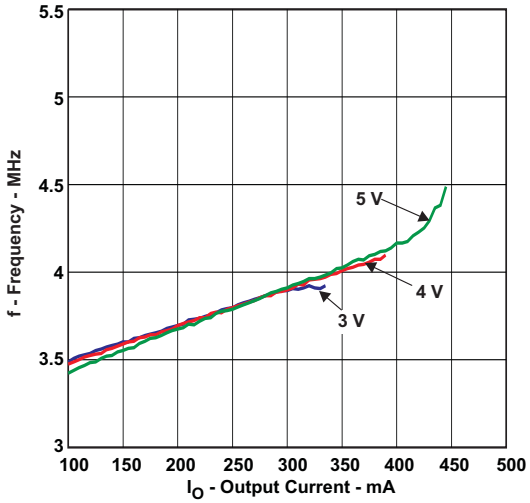


Figure 7. Frequency vs Output Load

8 Parameter Measurement Information

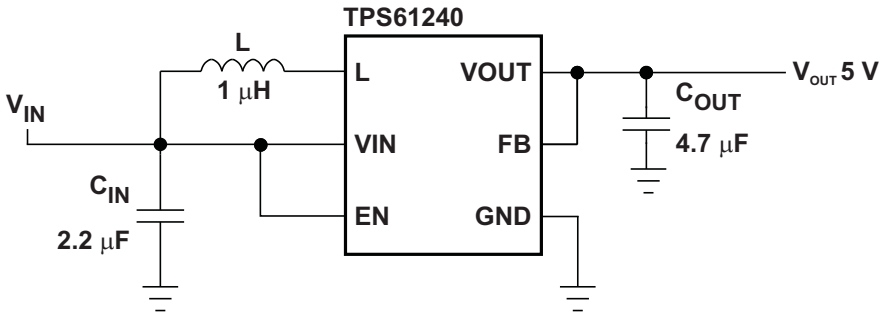


Figure 8. Parameter Measurement Schematic

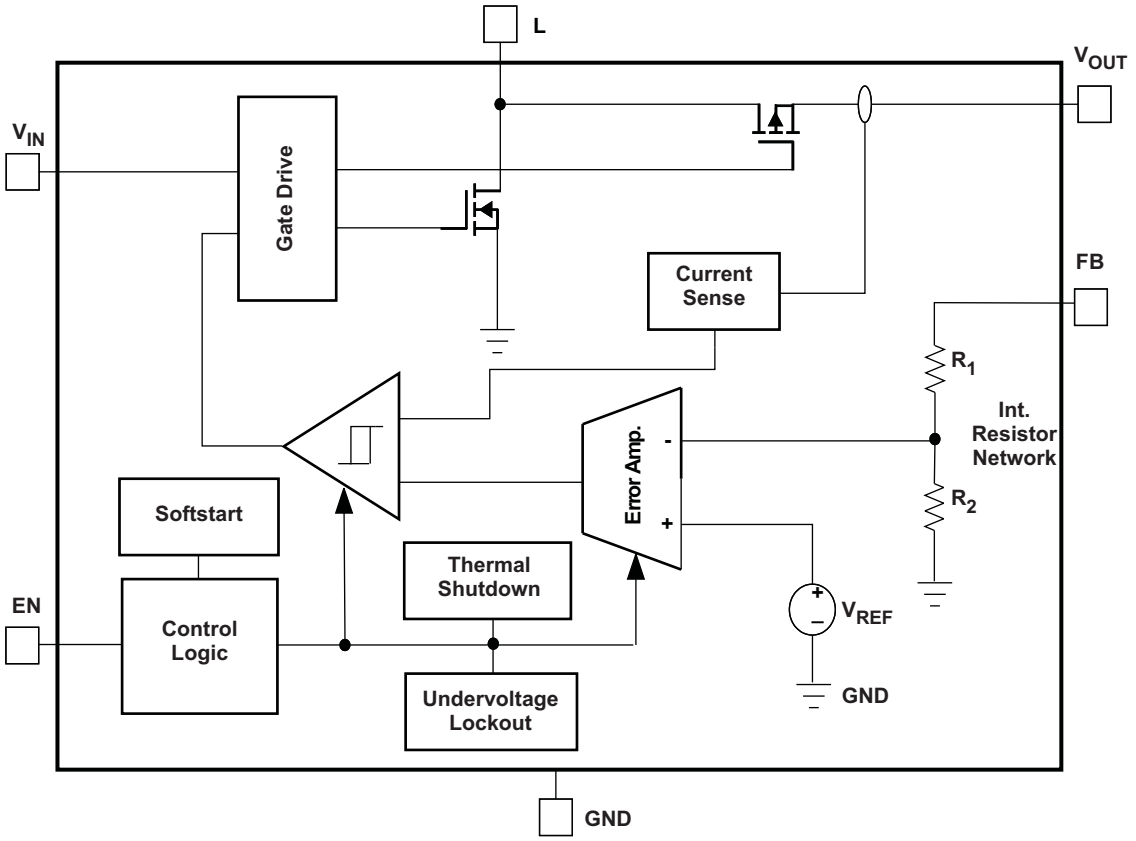
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9 Detailed Description

9.1 Overview

The TPS6124x device is a highly efficient synchronous step-up DC-DC converter optimized for products powered by either a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. The TPS6124x supports output currents up to 450 mA. The TPS61240 has an input valley current limit of 500 mA, and the TPS61241 has an input valley current of 600 mA. The TPS6124x boost converter is based on a quasi-constant on-time valley current mode control scheme. TPS6124x allows the use of small inductors and capacitors to achieve a small solution size. During shutdown, the load is completely disconnected from the battery.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Operation

The TPS6124x boost converter operates with typically 3.5-MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents the converter will automatically enter power save mode and operates then in PFM (Pulse Frequency Modulation) mode. During PWM operation the converter uses a unique fast response quasi-constant on-time valley current mode controller scheme which allows “Best in Class” line and load regulation allowing the use of small ceramic input and output capacitors.

Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time. At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a defined peak current. In the second phase, once the peak current is reached, the current comparator trips, the on-timer is reset turning off the switch, and the current through the inductor then decays to an internally set valley current limit. Once this occurs, the on-timer is set to turn the boost switch back on again and the cycle is repeated.

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Feature Description (continued)

9.3.2 Current Limit Operation

The current limit circuit employs a valley current sensing scheme. Current limit detection occurs during the off time through sensing of the voltage drop across the synchronous rectifier.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit operation, can be defined by Equation 1 as shown.

$$I_{OUT(CL)} = (1 - D) \times \left(I_{VALLEY} + \frac{1}{2} \Delta I_L\right) \quad \text{with } \Delta I_L = \frac{V_{IN}}{L} \times \frac{D}{f} \text{ and } D \approx \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

Figure 9 illustrates the inductor and rectifier current waveforms during current limit operation. The output current, I_{OUT}, is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off time is lengthened to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism).

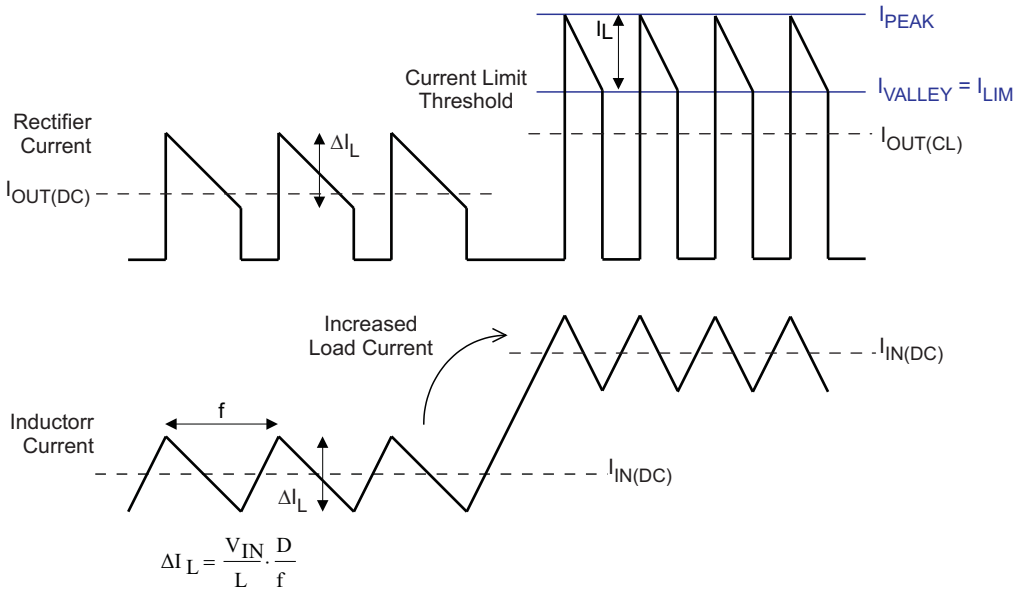


Figure 9. Inductor/Rectifier Currents in Current Limit Operation

9.3.3 Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter once the falling V_{IN} trips the undervoltage lockout threshold V_{UVLO}. The undervoltage lockout threshold V_{UVLO} for falling V_{IN} is typically 2.0 V. The device starts operation once the rising VIN trips undervoltage lockout threshold V_{UVLO} again at typically 2.1 V.

9.3.4 Input Overvoltage Protection

In the event of an overvoltage condition appearing on the input rail, the output voltage will also experience the overvoltage due to being in dropout condition. A input overvoltage protection feature has been implemented into the TPS6124x which has an input overvoltage threshold of 6.0 V. Once this level is triggered, the device will go into a shutdown mode to protect itself. If the voltage drops to 5.9 V or below, the device will startup once more into normal operation.

9.3.5 Enable

The device is enabled setting EN pin to high. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltages reaches its nominal value in typically 250 µs after the device has been enabled.

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Feature Description (continued)

The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can be connected to the output of another converter, to drive the EN pin high and getting a sequencing of supply rails. With EN = GND, the device enters shutdown mode.

9.3.6 Soft Start

The TPS6124x has an internal soft start circuit that controls the ramp up of the output voltage. The output voltages reaches its nominal value within t_{Start} of typically 250µs after EN pin has been pulled to high level. The output voltage ramps up from 5% to its nominal value within t_{RAMP} of typically 300 µs.

This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used.

During soft start, the switch current limit is reduced to 300 mA until the output voltage reaches V_{IN}. Once the output voltage trips this threshold, the device operates with its nominal current limit I_{LIMT}.

9.3.7 Load Disconnect

Load disconnect electrically removes the output from the input of the power supply when the supply is disabled. This is especially important during shutdown. In shutdown of a boost converter, the load is still connected to the input through the inductor and catch diode. Since the input voltage is still connected to the output, a small current continues to flow, even when the supply is disabled. Even small leakage currents significantly reduce battery life during extended periods of off time.

The benefit of this implemented feature for the system design engineer is that the battery is not depleted during shutdown of the converter. No additional components must be added to the design to make sure that the battery is disconnected from the output of the converter.

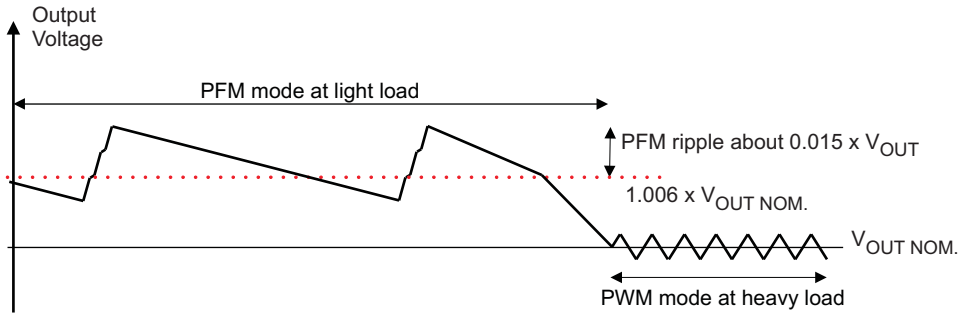
9.3.8 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typical) the device goes into thermal shutdown. In this mode, the High Side and Low Side MOSFETs are turned-off. When the junction temperature falls below the thermal shutdown hysteresis, the device continuous operation.

9.4 Device Functional Modes

9.4.1 Power Save Mode

The TPS6124x family of devices integrates a power save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage.



The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.

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10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS6124x device is optimized for products powered by either a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. With an input voltage range of 2.3 V to 5.5 V, the device supports batteries with extended voltage range and are ideal to power portable applications like mobile phones and other portable equipment. The TPS6124x supports output currents up to 450 mA.

The TPS6124x presents a high impedance at the V_{OUT} pin and the load is completely disconnected from the battery when shut down. This allows for use in applications that require the regulated output bus to be driven by another supply while the TPS6124x is shut down.

10.2 Typical Application

TPS61240 to output fixed 5.0 V for HDMI / USB-OTG applications.

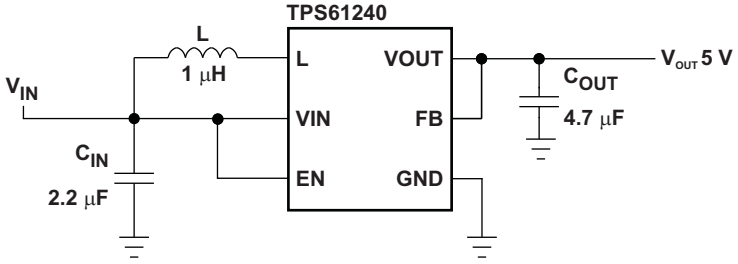


Figure 10. TPS61240 Fixed 5.0 V for HDMI / USB-OTG Applications

10.2.1 Design Requirements

In this example, the TPS61240 is used to design a 5-V output with 100-mA output current capability. The TPS61240 is powered by either a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. In this example, the input voltage range is from 3 V to 4.2 V for a one-cell Li-Ion battery input design.

Table 1. TPS61240 5V Output Design Requirements

Parameters	Value
Input Voltage	3 V to 4.2 V
Output Voltage	5 V
Output Current	100 mA

10.2.2 Detailed Design Procedure

Table 2. List of Components

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_{IN}	JMK105BJ225MV	Taiyo Yuden	2.2 µF, X5R, 6.3 V, 0402
C_{OUT}	JDK105BJ475MV	Taiyo Yuden	4.7 µF, X5R, 6.3 V, 0402
L	MDT2012-CH1R0AN	TOKO	1.0 µH, 900mA, 0805

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10.2.2.1 Programming the Output Voltage

The output voltage is set by a resistor divider internally. The FB pin is used to sense the output voltage. So to configure the output properly, the FB pin needs to be connected directly to the output.

10.2.2.2 Inductor Selection

To make sure that the TPS6124x devices can operate, an inductor must be connected between pin V_{IN} and pin L. A boost converter normally requires two main passive components for storing energy during the conversion. A boost inductor and a storage capacitor at the output are required. To select the boost inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. The highest peak current through the inductor and the switch depends on the output load, the input (V_{IN}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using Equation 2.

$$I_{L_MAX} \approx I_{OUT} \times \frac{V_{OUT}}{\eta \times V_{IN}} \tag{2}$$

For example, for an output current of 200 mA at 5.0 V V_{OUT}, at least 540 mA of average current flows through the inductor at a minimum input voltage of 2.3 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than 20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system size and cost. With these parameters, it is possible to calculate the value of the minimum inductance by using Equation 3.

$$L_{MIN} \approx \frac{V_{IN} \times (V_{OUT} - V_{IN})}{\Delta I_L \times f \times V_{OUT}} \tag{3}$$

Parameter f is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., 20% x I_L. In this example, the desired inductor has the value of 1.7 µH. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. In typical applications a 1.0-µH inductance is recommended. The device has been optimized to operate with inductance values between 1.0 µH and 2.2 µH. It is recommended that inductance values of at least 1.0 µH is used, even if Equation 3 yields something lower. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in Equation 3. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

With the chosen inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 4 shows how to calculate the peak current I.

$$I_{L(peak)} = \frac{V_{IN} \times D}{2 \times f \times L} + \frac{I_{OUT}}{(1 - D) \times \eta} \quad \text{with} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{4}$$

This would be the critical value for the current rating for selecting the inductor. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents.

Table 3. List of Inductors

MANUFACTURER	SERIES	DIMENSIONS
TOKO	MDT2012-CH1R0AN	2.0 x 1.2 x 1.0 max. height
	MDT1608-CH1R0N	1.6 x 0.8 x 0.95 max. height
Hitachi Metals	KSLI-201210AG-1R0	2.0 x 1.2 x 1.0 max. height
	KSLI-201610AG-1R0	2.0 x 1.6 x 1.0 max. height
muRata	LQM21PN1R0MC0	2.0 x 1.2 x 0.55 max. height
FDK	MIPS2012D1R0-X2	2.0 x 1.2 x 1.0 max. height

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10.2.2.3 Input Capacitor

At least 2.2-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. It is recommended to place a ceramic capacitor as close as possible to the VIN and GND pins.

10.2.2.4 Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the V_{OUT} and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the V_{OUT} and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 5 can be used.

$$C_{min} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \quad (5)$$

where

- f is the switching frequency
- ΔV is the maximum allowed ripple

With a chosen ripple voltage of 10 mV, a minimum effective capacitance of 2.7 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using $\Delta V_{ESR} = I_{OUT} \times R_{ESR}$.

A capacitor with a value in the range of the calculated minimum should be used. This is required to maintain control loop stability. There are no additional requirements regarding minimum ESR. There is no upper limit for the output capacitance value. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

Note that ceramic capacitors have a DC Bias effect, which will have a strong influence on the final effective capacitance needed. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and the effective capacitance.

10.2.2.5 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{O(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_O immediately shifts by an amount equal to $\Delta I_{(LOAD)} \times$ ESR, where ESR is the effective series resistance of C_O. $\Delta I_{(LOAD)}$ begins to charge or discharge C_O generating a feedback error signal used by the regulator to return V_O to its steady-state value. The results are most easily interpreted when the device operates in PWM mode. During this recovery time, V_O can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (for example, MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

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10.2.3 Application Curves

	FIGURE
Output Voltage Ripple, PFM Mode, I_{out} = 10 mA	Figure 11
Output Voltage Ripple, PWM Mode, I_{out} = 150 mA	Figure 12
Load Transient Response, V_{in} = 3.6 V, 0 - 50 mA	Figure 13
Load Transient Response, V_{in} = 3.6 V, 50 - 200 mA	Figure 14
Line Transient Response, V_{in} = 3.6 V - 4.2 V, I_{out} = 50 mA	Figure 15
Line Transient Response, V_{in} = 3.6 V - 4.2 V, I_{out} = 200 mA	Figure 16
Startup after Enable, V_{in} = 3.6 V, V_{out} = 5 V, Load = 5 KΩ	Figure 17
Startup after Enable, V_{in} = 3.6 V, V_{out} = 5 V, Load = 16.5 Ω	Figure 18
Startup and Shutdown, V_{in} = 3.6 V, V_{out} = 5 V, Load = 16.5 Ω	Figure 19

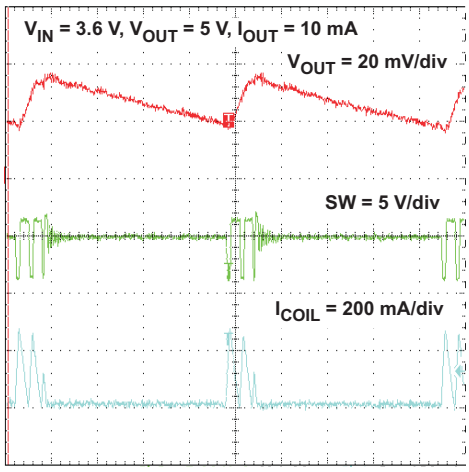


Figure 11. Output Voltage Ripple – PFM Mode

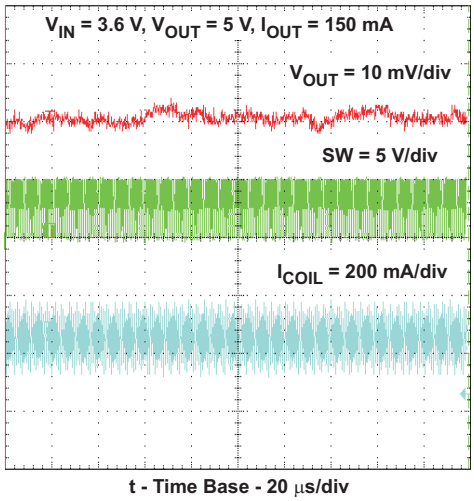


Figure 12. Output Voltage Ripple – PWM Mode

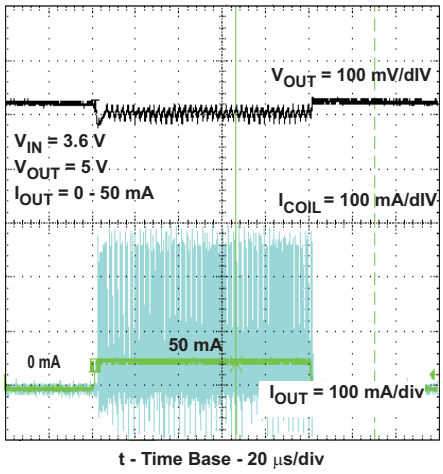


Figure 13. Load Transient Response 0 mA – 50 mA and 50 mA – 0 mA

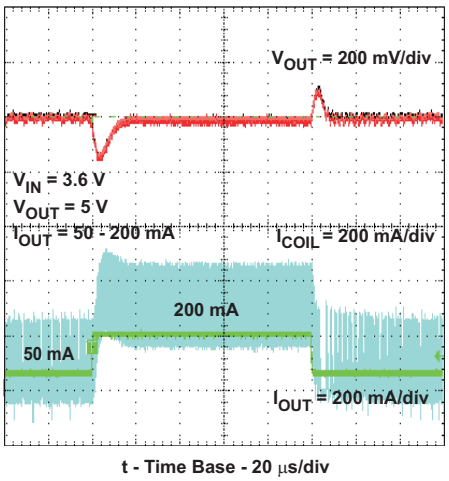


Figure 14. Load Transient Response 0 mA – 200 mA and 200 mA – 0 mA

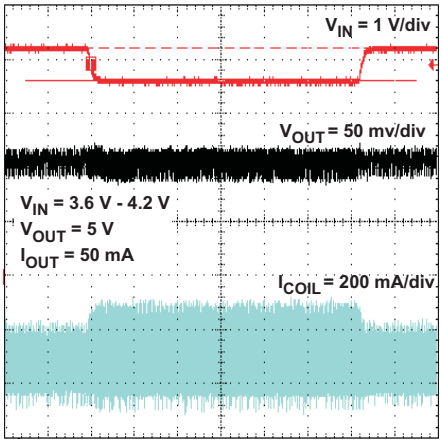


Figure 15. Line Transient Response 3.6 V – 4.2 V at 50 mA Load

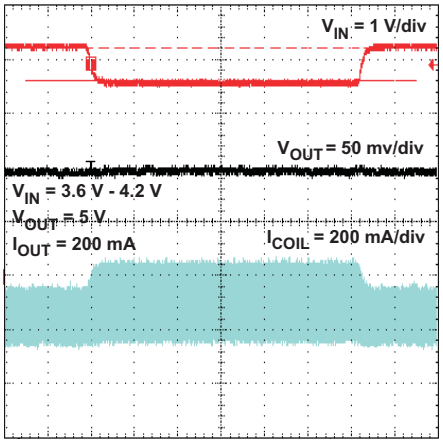


Figure 16. Line Transient Response 3.6 V – 4.2 V at 200 mA Load

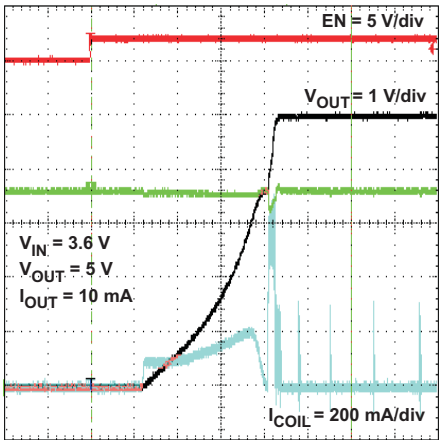


Figure 17. Startup After Enable – No Load

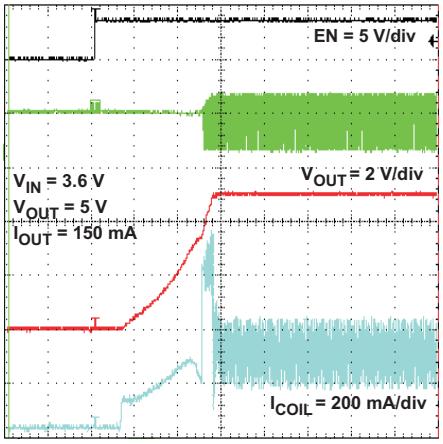


Figure 18. Startup After Enable – With Load

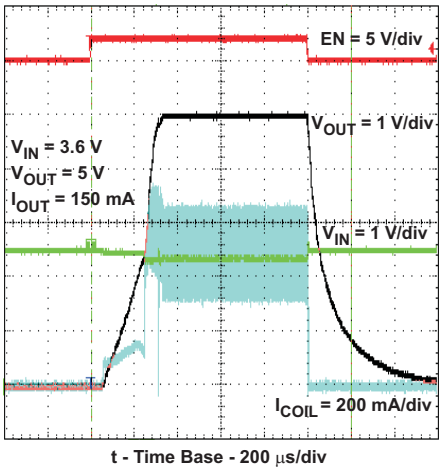


Figure 19. Startup and Shutdown

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10.3 System Examples

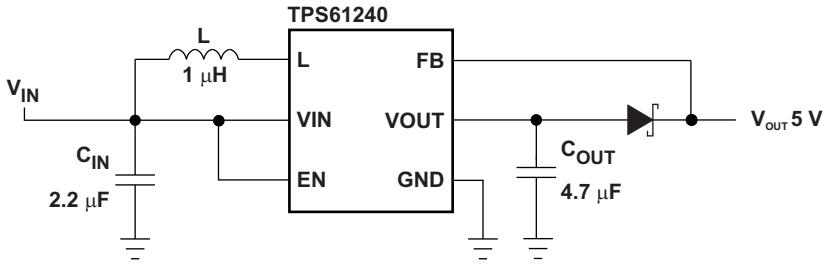


Figure 20. TPS61240 Fixed 5.0 V With Schottky Diode for Output Overvoltage Protection

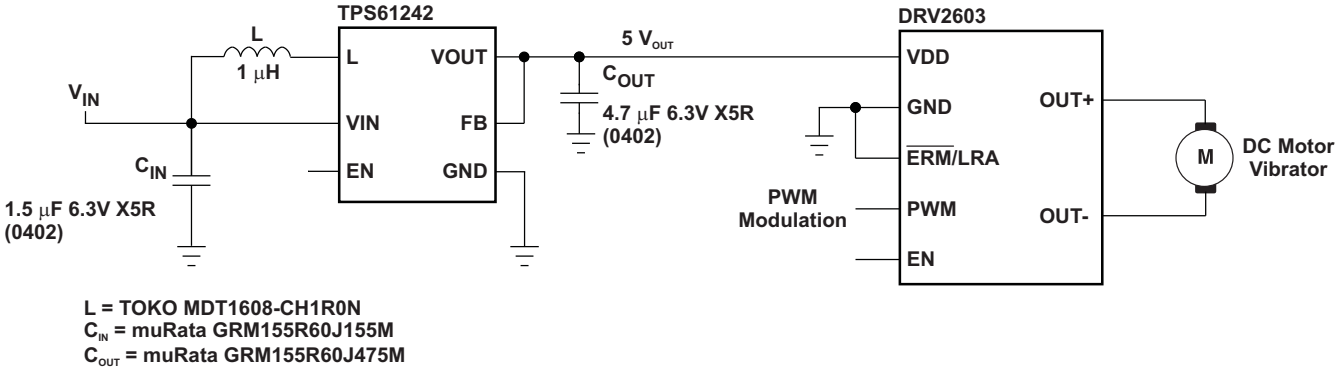


Figure 21. DRV2603 + TPS61242 Haptic Driver Solution featuring PWM Modulation Control

11 Power Supply Recommendations

The power supply can be a three-cell alkaline, NiCd or NiMH, or one-cell Li-Ion or Li-Polymer battery. The input supply should be well regulated with the rating of TPS6124x. If the input supply is located more than a few inches from the device, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

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12 Layout

12.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC. The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

12.2 Layout Example

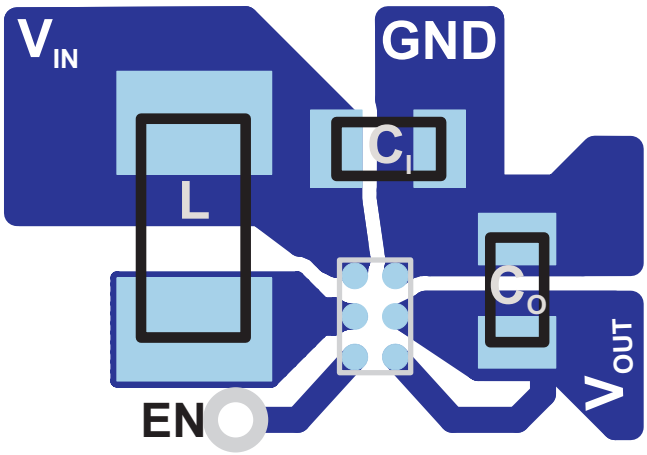


Figure 22. Suggested Layout (Top)

12.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
  - For example, increase of the GND plane on the top layer which is connected to the exposed thermal pad
  - Use thicker copper layer
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS6124x is 105°C. The thermal resistance of the 6-pin CSP package (YFF-6) is $R_{\theta JA}$ = 133 °C/W. Regulator operation is specified to a maximum steady-state ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 150 mW.

$$P_{D(Max)} = [T_{J\ (max)} - T_A\ ] / \theta_{JA} = [105°C - 85°C] / 133\ °C/W = 150\ mW \quad (6)$$

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13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61240	Click here	Click here	Click here	Click here	Click here
TPS61241	Click here	Click here	Click here	Click here	Click here

13.3 Trademarks

NanoFree is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

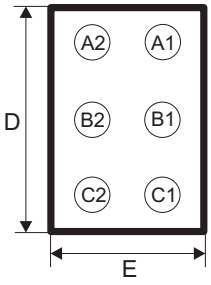
14.1 Chip Scale Package Dimensions

The TPS6124x device is available in a 6-bump chip scale package (YFF, NanoFree™). The package dimensions are given as:

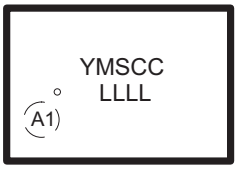
D	E
Max = 1280 µm	Max = 890 µm
Min = 1220 µm	Min = 830 µm

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Chip Scale Package
(Bottom View)



Chip Scale Package
(Top View)



Code:
- YM - Year Month date code
- S - Assembly site code
- CC - Chip Code
- LLLL - Lot trace code

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61240DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCJ	Samples
TPS61240DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCJ	Samples
TPS61240YFFR	ACTIVE	DSBGA	YFF	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GM	Samples
TPS61240YFFT	ACTIVE	DSBGA	YFF	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GM	Samples
TPS61241YFFR	ACTIVE	DSBGA	YFF	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	NF	Samples
TPS61241YFFT	ACTIVE	DSBGA	YFF	6	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	NF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS61240 :

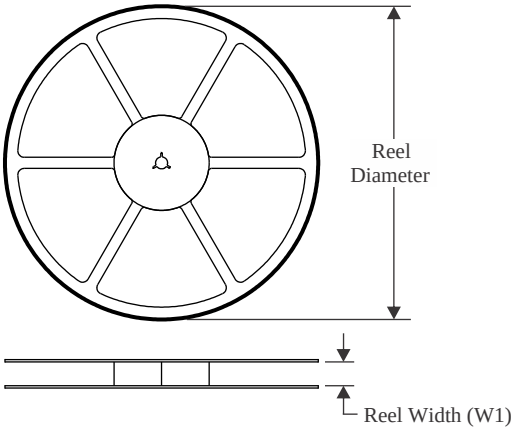
- Automotive : TPS61240-Q1

NOTE: Qualified Version Definitions:

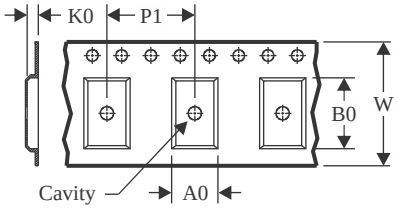
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

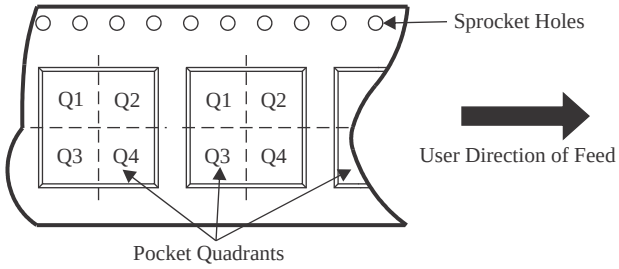


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

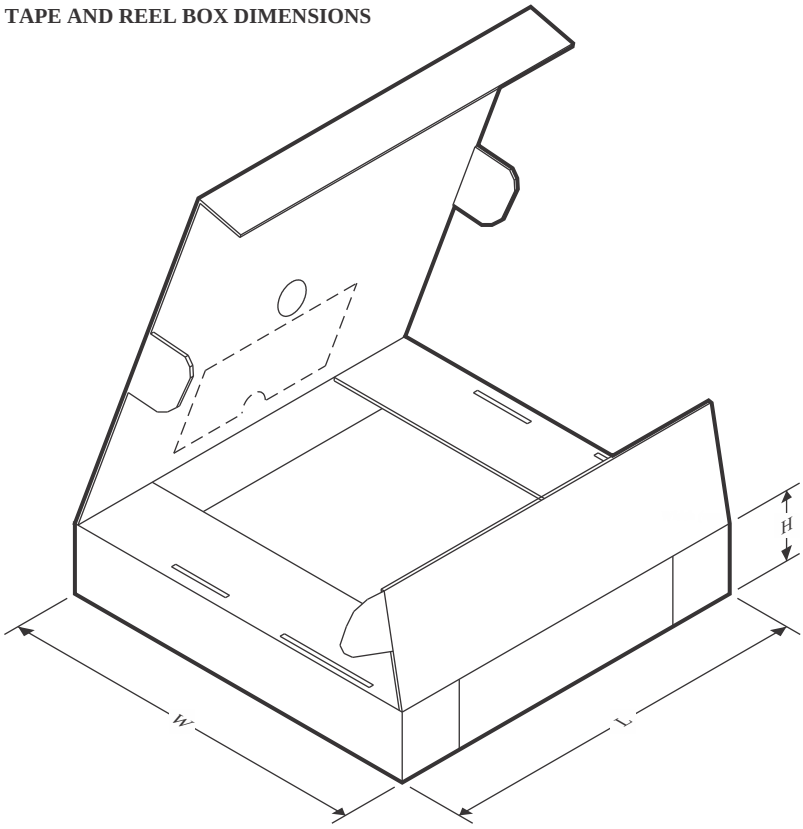
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61240DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61240DRVT	WSON	DRV	6	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
TPS61240DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61240YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.98	1.41	0.69	4.0	8.0	Q1
TPS61240YFFT	DSBGA	YFF	6	250	180.0	8.4	0.98	1.41	0.69	4.0	8.0	Q1
TPS61241YFFR	DSBGA	YFF	6	3000	180.0	8.4	0.98	1.41	0.69	4.0	8.0	Q1
TPS61241YFFT	DSBGA	YFF	6	250	180.0	8.4	0.98	1.41	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

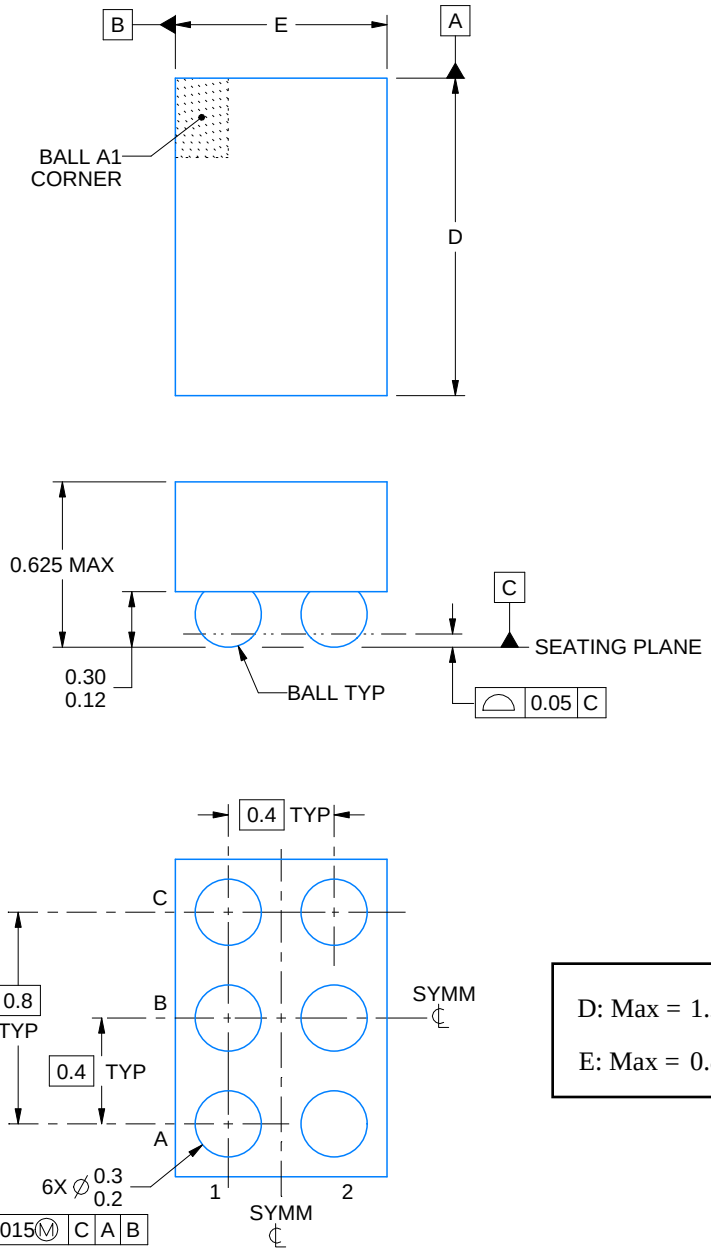
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61240DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS61240DRVT	WSON	DRV	6	250	200.0	183.0	25.0
TPS61240DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS61240YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS61240YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0
TPS61241YFFR	DSBGA	YFF	6	3000	182.0	182.0	20.0
TPS61241YFFT	DSBGA	YFF	6	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0006

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



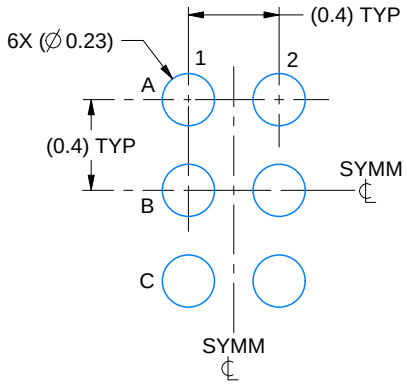
D: Max = 1.288 mm, Min =1.228 mm

E: Max = 0.886 mm, Min =0.826 mm

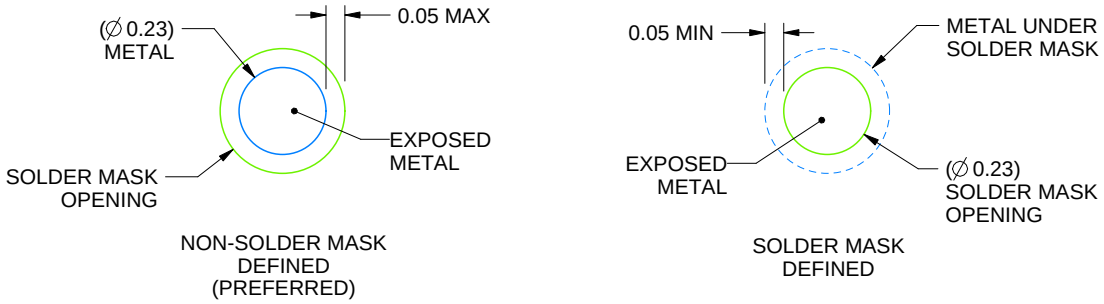
4223785/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X

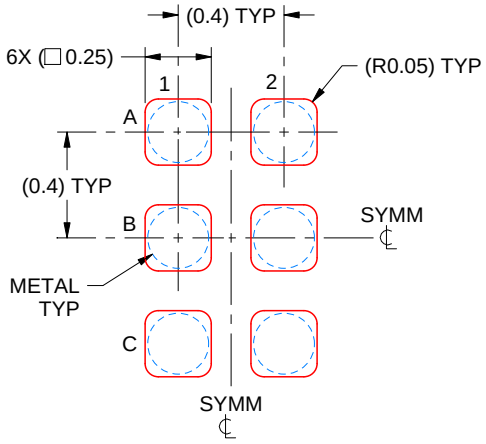


SOLDER MASK DETAILS
NOT TO SCALE

4223785/A 06/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:35X

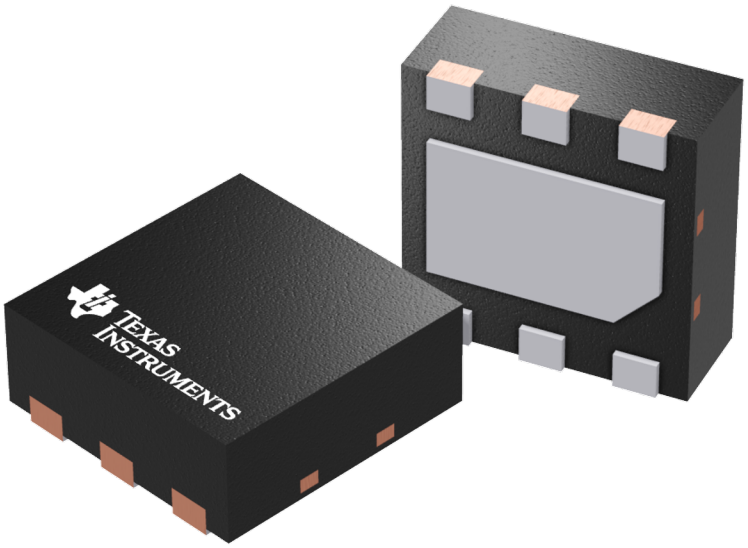
4223785/A 06/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



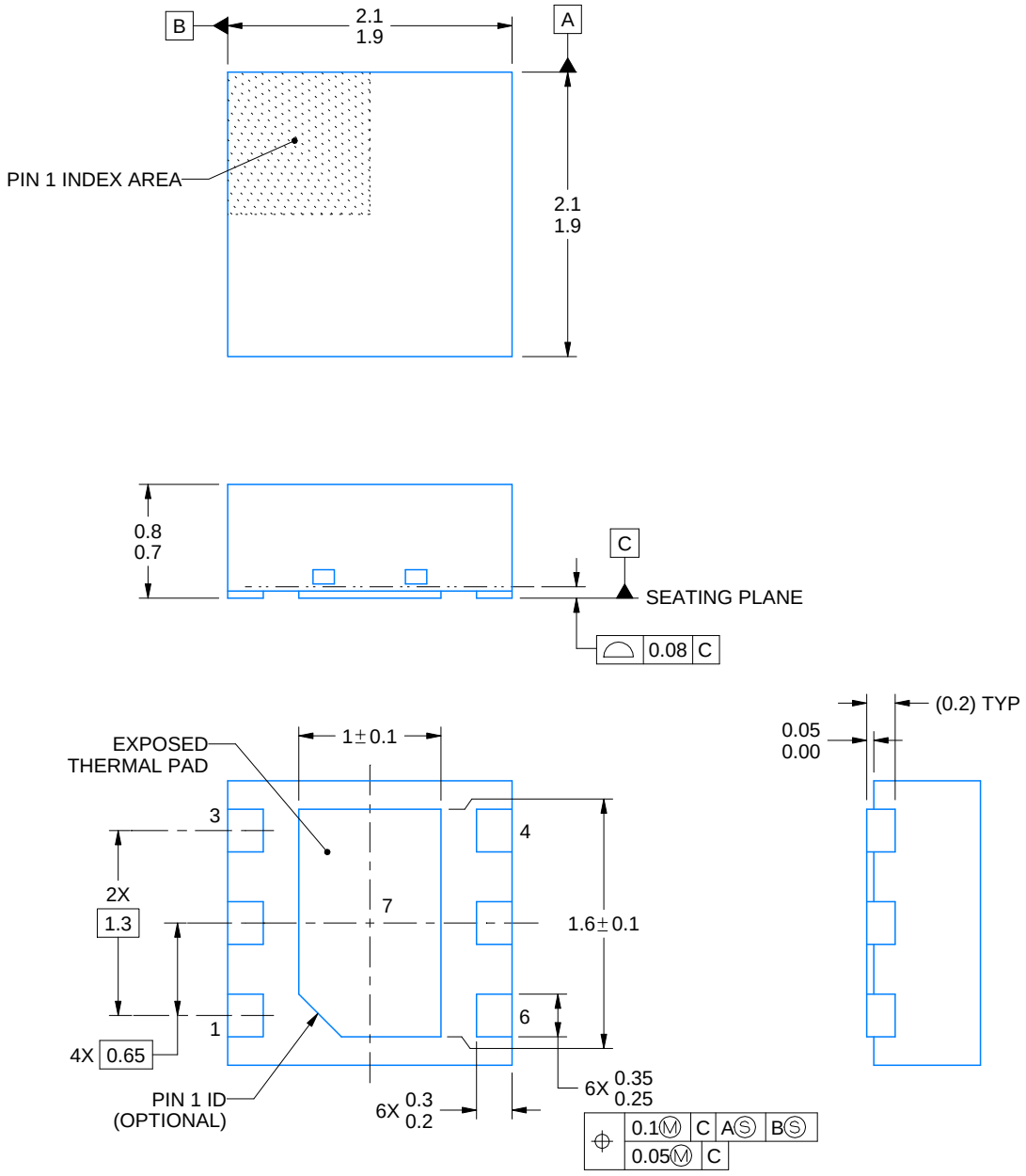
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRV0006A

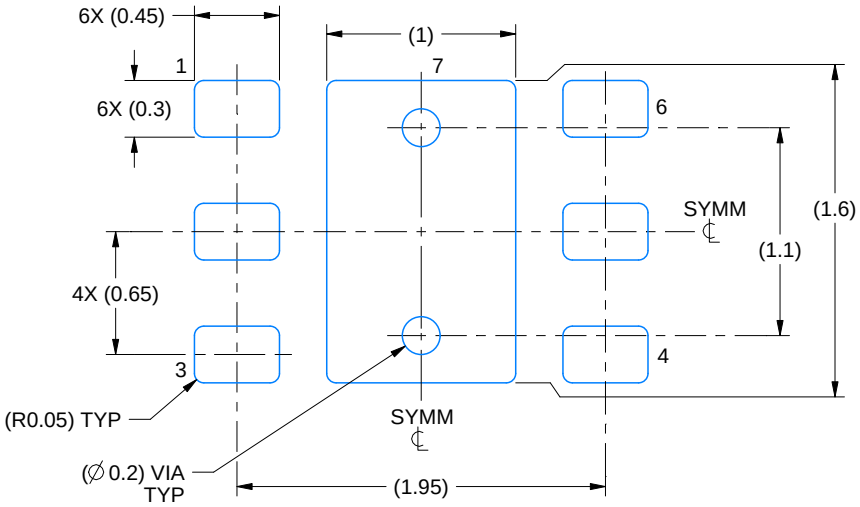
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

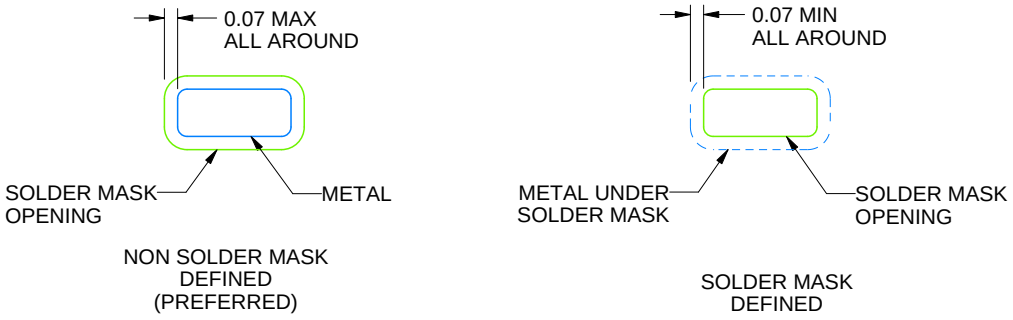


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

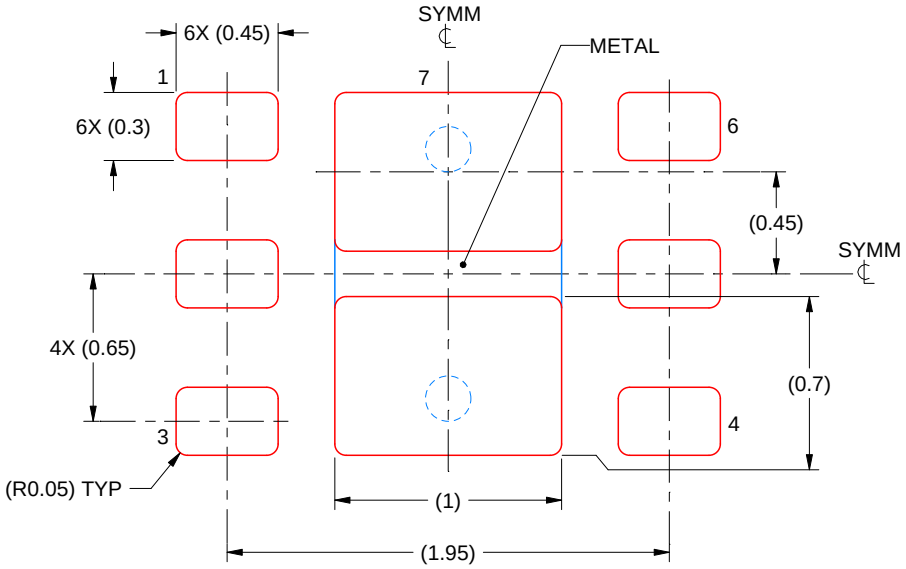
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DRV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

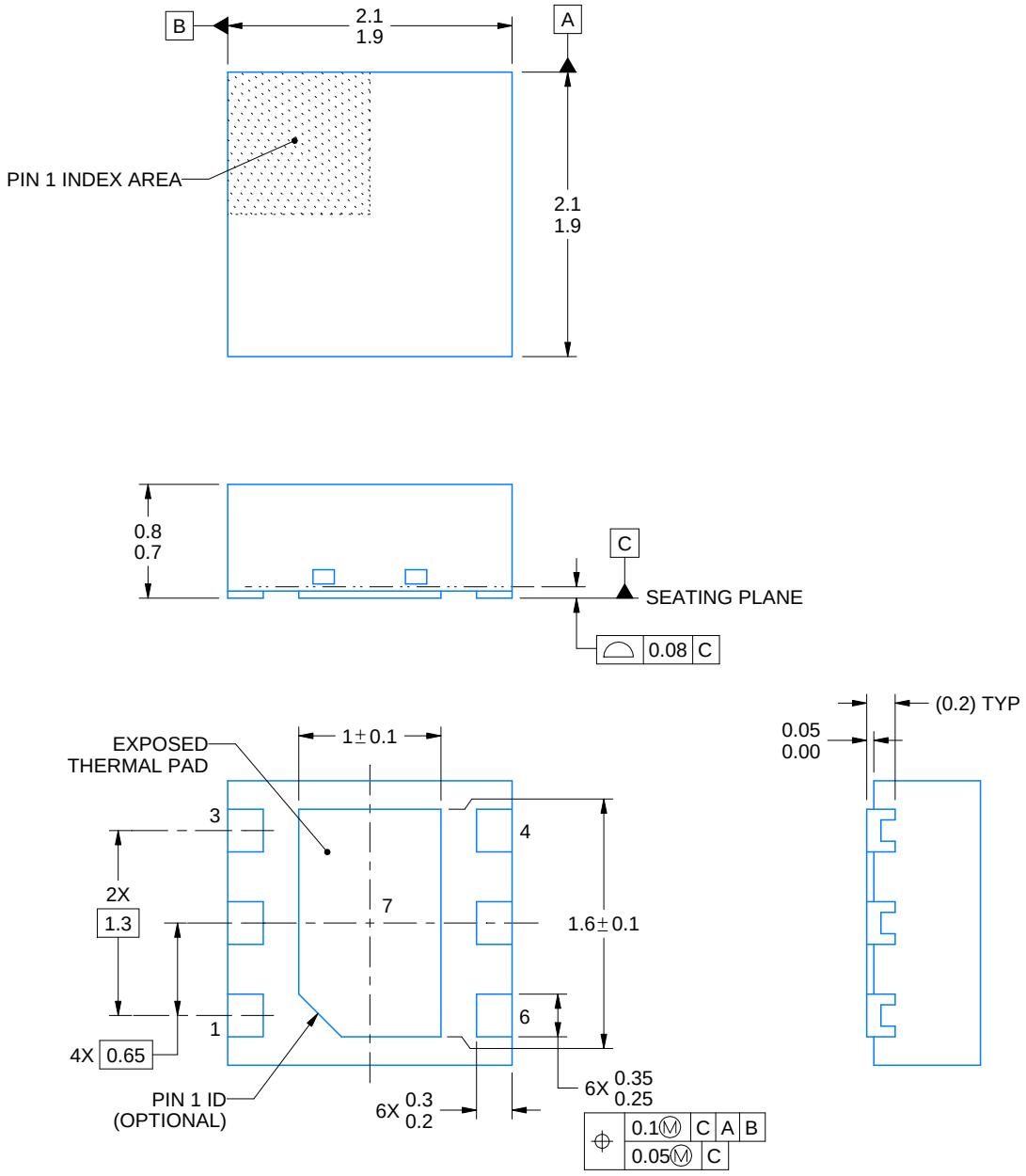
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

DRV0006D

PACKAGE OUTLINE

WSON - 0.8 mm max height

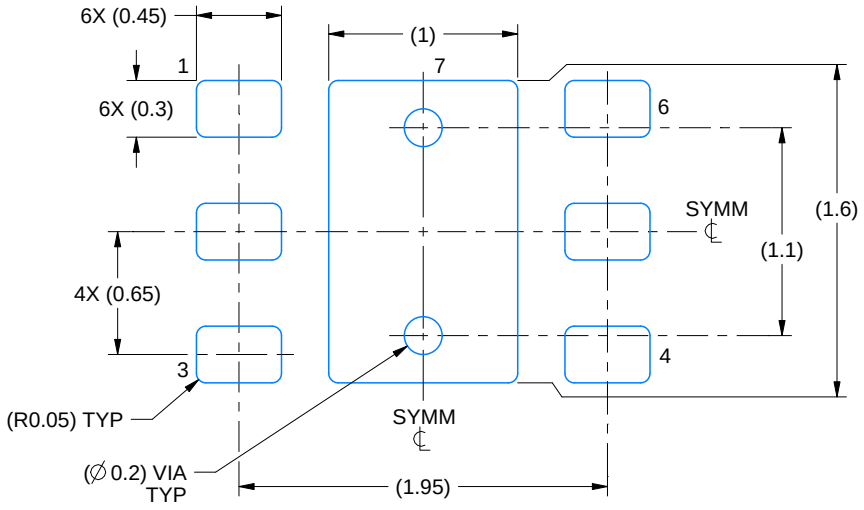
PLASTIC SMALL OUTLINE - NO LEAD



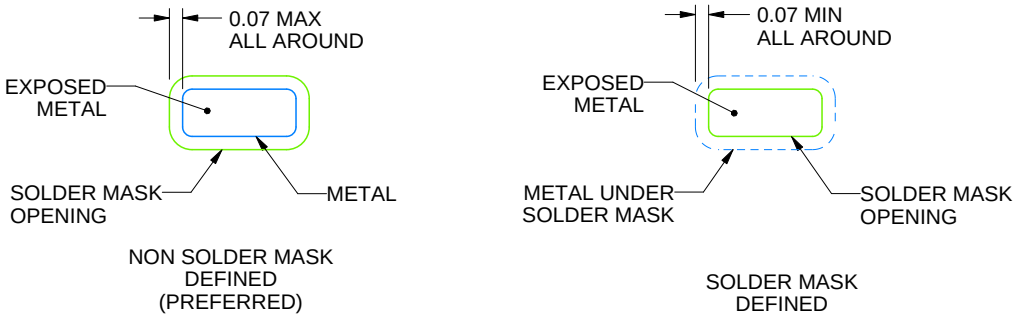
4225563/A 12/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

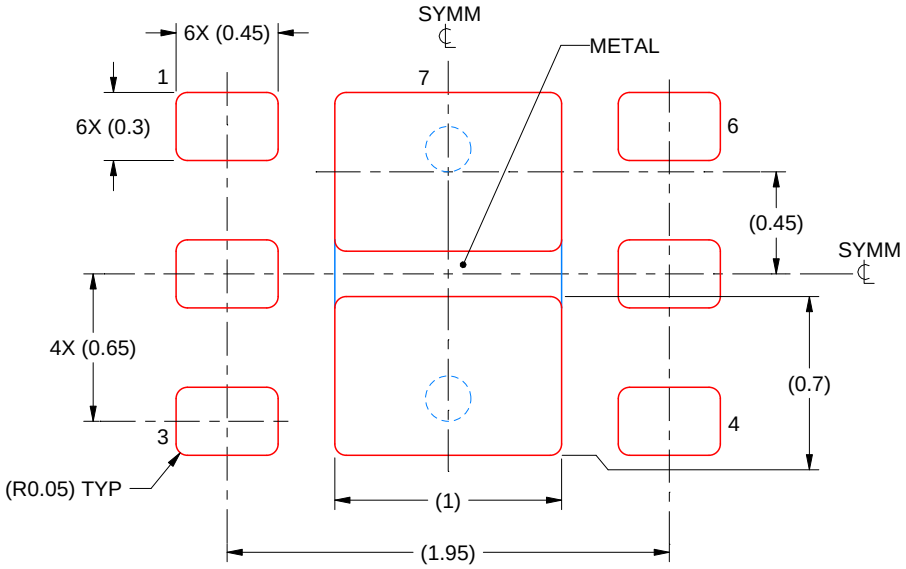


SOLDER MASK DETAILS

4225563/A 12/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4225563/A 12/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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