# 支持单节锂离子电池输入的高效 6 通道白光发光二极管 (WLED) 驱动器

查询样品: TPS61176

## 特性

- **2.7V** 至 **6.5V VIN** 电压范围
- **2.7V** 至 **24V** 升压输入电压范围
- 集成型 **2A/40V** 金属氧化物半导体场效应晶体管 **(MOSFET)**
- **1MHz** 开关频率
- 至 **WLED** 电压的自适应升压输出
- 每个具有 **6** 个 **35mA** 的电流吸收能力
- **±2%**（最大值）电流精度
- **1.3%**（典型值）的电流匹配
- 宽脉宽调制 **(PWM)** 调光频率范围
  - 从 **100Hz** 至 **22kHz**
- 混合调光模式：模拟调光和 **PWM** 调光间的自动切换
  - 可编程切换点：**25%/12.5%**
  - 可编程 **PWM** 调光模式：**22kHz PWM** 调光**/**直接 **PWM** 调光
- 高达 **14** 位的调光分辨率
- 支持低至 **1%** 的调光占空比
- 输入 **PWM** 毛刺脉冲滤波器
- 效率高达 **90%**
- 针对输入**/**输出隔离 **PFET** 的驱动器以实现真关断
- 内置软起动
- 内置 **WLED** 开路**/**短路保护
- 热关断
- 支持 **4.7μH** 电感器
- **16L 3mm x 3mm** 超薄四方扁平无引线 **(WQFN)** 封装

## 应用范围

- 平板电脑背光
- 笔记本电脑背光
- 用于由单节或多节电池输入供电的小型和中等尺寸 **LCD** 显示屏的背光

## 说明

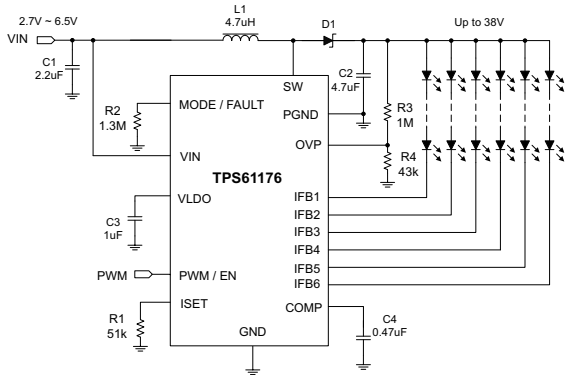
TPS61176 是一款用于平板电脑或笔记本电脑（可支持由单节电池直接供电）的高度集成多通道 WLED 背光驱动器。 它包含一个高效升压转换器，此转换器具有一个集成 2A/40V 功率 MOSFET 和 6 个电流吸收稳压器。 此器件总共能够驱动多达 60 个具有高电流匹配性能的 WLED。 此外，为了提高效率，此升压转换器能够自动调节到 WLED 正向电压的输出电压。

TPS61176 采用混合调光模式。 低调光占空比时的 PWM 调光与高占空比时的模拟调光间的自动切换增加了整体电光转换效率，从而大大减少了背光的功率分配。 切换点可被设定为 25% 或 12.5%，并且 PWM 调光模式可被设定为固定频率调光或直接 PWM 调光。 TPS61176 支持高达 14 位的调光分辨率，这就避免了低亮度调光期间可能发生的视觉闪烁。

通过提供一个用于外部隔离 P 通道 MOSFET 的驱动器，TPS61176 能够支持真关断。 当集成电路 (IC) 被禁用或升压输出被短接至地时，隔离 PFET 可被关闭以切断电池到 WLED 的电源路径，从而防止电池电流泄露。 TPS61176 还集成了软启动，WLED 开路和短路保护以及热关断。

TPS61176 采用 16 引脚 3mm x 3mm WQFN 封装，从而提供了一个节省空间且高性能的 WLED 驱动器解决方案。

## 典型应用

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

| | | VALUE | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Voltage range(2) | VIN, PWM/EN, MODE/FAULT | –0.3 | 7 | V |
| | SW | –0.3 | 40 | V |
| | IFB1 to IFB6 | –0.3 | 20 | V |
| | All other pins | –0.3 | 3.6 | V |
| ESD rating | HBM | | 4 | kV |
| | MM | | 200 | V |
| | CDM | | 2 | kV |
| Continuous power dissipation | | See Thermal Information Table | | |
| Operating junction temperature range | | –40 | 150 | °C |
| Storage temperature range | | –65 | 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS61176 | UNITS |
|---|---|---|---|
| | | RTE (16 PINS) | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance(2) | 43 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance(3) | 44.4 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance(4) | 14.4 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter(5) | 0.6 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter(6) | 14.3 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance(7) | 3.3 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, $\psi_{JT}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, $\psi_{JB}$, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.


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## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Bias voltage to IC (Application as Figure 18) | 2.7 | | 6.5 | V |
| | Input voltage to inductor (Application as Figure 18) | 2.7 | | 24 | V |
| $V_{OUT}$ | Output voltage range | Vin | | 38 | V |
| L | Inductor | 4.7 | 6.8 | 10 | µH |
| $C_I$ | Input capacitor | 1.0 | 2.2 | | µF |
| $C_O$ | Output capacitor | 2.2 | 4.7 | 10 | µF |
| $C_{COMP}$ | COMP capacitor | 0.47 | | 1 | µF |
| $F_{PWM_I}$ | Input PWM signal frequency range | 0.1 | | 22 | KHz |
| $T_A$ | Operating ambient temperature | –40 | | 85 | °C |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

## ELECTRICAL CHARACTERISTICS

$V_{IN}$ = 3.6V, PWM/EN=high, IFB current=20mA, IFB voltage=450mV, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{IN}$ | Input voltage range | | 2.7 | | 6.5 | V |
| $V_{IN_UVLO}$ | VIN under voltage lockout threshold | $V_{IN}$ ramp down | | 2.4 | 2.5 | V |
| | | $V_{IN}$ ramp up | | 2.65 | 2.7 | |
| $V_{IN_HYS}$ | VIN under voltage lockout hysteresis | | | 250 | | mV |
| $I_{q_VIN}$ | Operating quiescent current into VIN | Device enable, switching 1 MHz and no load | | | 3 | mA |
| $I_{SD}$ | Shutdown current | PWM/EN = low | | 1 | 4 | µA |
| | | PWM/EN = low, $T_A$ = 25°C | | 1 | 2 | |
| $V_{LDO}$ | VLDO pin output voltage | $V_{IN}$ = 3.6 V | 3 | 3.3 | 3.5 | V |
| **PWM/EN** | | | | | | |
| $V_H$ | PWM/EN Logic high | | 1.2 | | | V |
| $V_L$ | PWM/EN Logic Low | | | | 0.4 | V |
| $R_{PD}$ | PWM/EN pin internal pull-down resistor | | 400 | 800 | 1600 | kΩ |
| $t_{SD}$ | PWM/EN logic low width to shutdown | PWM/EN from high to low | 20 | | | ms |
| **CURRENT REGULATION** | | | | | | |
| $V_{ISET}$ | ISET pin voltage | PWM/EN logic high | 1.02 | 1.04 | 1.06 | V |
| $K_{ISET}$ | Current multiplier | $I_{ISET}$ = 20 µA | | 1024 | | |
| $I_{FBx}$ | Current accuracy | $I_{ISET}$ = 20 µA, 0°C to 70°C | –2% | | 2% | |
| | | $I_{ISET}$ = 20 µA, –40°C to 85°C | –2.3% | | 2.3% | |
| $K_m$ | $(I_{max} – I_{min}) / (2 \times I_{AVG})$ | $I_{ISET}$ = 20 µA | | 0.65% | | |
| $I_{IFBx_leak}$ | IFBx pin leakage current | $V_{IFBx}$ = 10 V, each pin | | 1.5 | 5 | µA |
| | | $V_{IFBx}$ = 5 V, each pin | | 0.5 | 2 | |
| $I_{IFBx_max}$ | Current sink max output current | $I_{ISET}$ = 35 µA, each pin | 35 | | | mA |
| $T_{FBx_MINON}$ | Current sink minimum on time | $I_{ISET}$ = 20 µA, each pin | | 0.5 | | µs |
| $f_{dim}$ | PWM dimming frequency | Mode 1 / Mode 3, 0°C to 70°C | 20 | 22 | 27 | kHz |
| **BOOST OUTPUT REGULATION** | | | | | | |
| $V_{IFBx_min}$ | IFBx regulation voltage | Measured on $V_{IFB(min)}$, $I_{ISET}$ = 20 µA | | 450 | | mV |

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## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$ = 3.6V, PWM/EN=high, IFB current=20mA, IFB voltage=450mV, $T_A$ = -40°C to +85°C, typical values are at $T_A$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SWITCH** | | | | | | |
| $R_{DS(on)}$ | Switch MOSFET on-resistance | $V_{IN}$ = 3.6 V | | 0.25 | 0.4 | Ω |
| $I_{LEAK_SW}$ | Switch MOSFET leakage current | $V_{SW}$ = 40 V | | | 2 | μA |
| **OSCILLATOR** | | | | | | |
| $f_{SW}$ | Oscillator frequency | | 0.8 | 1 | 1.2 | MHz |
| $D_{max}$ | Maximum boost switch duty cycle | | | 93 | | % |
| **MODE / FAULT** | | | | | | |
| $V_{MODE}$ | MODE/FAULT pin voltage during mode detection period | Tested as $V_{IN}$ - $V_{MODE}$ when mode resistor is connected between VIN pin and MODE/FAULT pin; Tested as $V_{MODE}$ when mode resistor is connected between MODE/FAULT pin and GND | | 0.6 | 0.9 | V |
| $I_{MODE_PD}$ | MODE/FAULT pin pull down current after mode detection | $V_{MODE}$ = 0.5 V, mode resistor is connected between VIN pin and MODE/FAULT pin | 50 | 80 | | μA |
| **OC, SC, OVP and SS** | | | | | | |
| $I_{LIM}$ | Switch MOSFET current limit | | 2 | 2.5 | 3 | A |
| $V_{OVP_clamp}$ | Output over voltage clamp threshold | | 1.47 | 1.5 | 1.53 | V |
| $V_{OVP_sd}$ | Output over voltage shutdown threshold | OVP ramp up | 1.568 | 1.6 | 1.632 | V |
| | | OVP ramp down | 1.519 | 1.55 | 1.581 | |
| $V_{OVP_SC}$ | Output short to GND detection threshold | OVP ramp up | | 90 | | mV |
| | | OVP ramp down | 50 | 70 | | |
| $V_{OVP_IFB}$ | 1st level IFB overvoltage threshold | IFBx current sink on | 7 | 8.5 | 10 | V |
| $V_{OVP2_IFB}$ | 2nd level IFB overvoltage threshold | IFBx current sink on or off | 16 | 18 | 20 | V |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{shutdown}$ | Thermal shutdown threshold | | | 160 | | °C |
| $T_{hys}$ | Thermal shutdown hysteresis | | | 15 | | °C |


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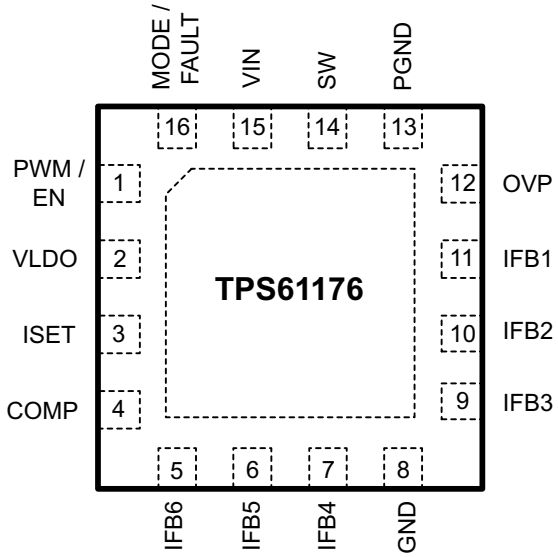
## DEVICE INFORMATION

**PIN ASSIGNMENT**
**16 PIN 3mm × 3mm RTE PACKAGE**
**(TOP VIEW)**




### PIN FUNCTIONS

| PIN | | DESCRIPTION |
|---|---|---|
| NUMBER | NAME | |
| 1 | PWM/EN | PWM dimming signal input and IC enable / disable control(1) |
| 2 | VLDO | Internal pre-regulator output. Connect a 1 µF ceramic capacitor to this pin |
| 3 | ISET | Full-scale LED current setting pin. Connect a resistor to the pin to program the full-scale LED current |
| 4 | COMP | Connect an external 0.47µF ceramic capacitor to this pin for the boost loop compensation. |
| 5~7, 9~11 | IFB4 to IFB6, IFB1 to IFB3 | Regulated current sinks input pins |
| 8 | GND | Analog ground |
| 12 | OVP | This pin monitors the output voltage of the boost converter through external resistor divider |
| 13 | PGND | Power ground |
| 14 | SW | Drain of the internal power MOSFET |
| 15 | VIN | Supply input pin, provides power supply to the IC |
| 16 | MODE/FAULT | Multi-function pin. Use this pin to program the dimming mode. It also functions as a driver for external isolation P-channel MOSFET(1) |

(1) See Detailed Description section for details.

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## TYPICAL CHARACTERISTICS

### Table 1. TABLE OF GRAPHS

| TITLE | DESCRIPTION | FIGURE |
|---|---|---|
| Dimming Efficiency | $V_{BAT}$ = 3V, 3.6V, 4.2V, 5V; $V_O$ = 18V, 6s6p, 20mA/string; PWM Freq = 200Hz; Mode 1; L = 6.8µH | Figure 1 |
| Dimming Efficiency | $V_{BAT}$ = 3V, 3.6V, 4.2V, 5V; $V_O$ = 21V, 7s6p, 20mA/string; PWM Freq = 200Hz; Mode 1; L = 6.8µH | Figure 2 |
| Dimming Efficiency | $V_{BAT}$ = 3V, 3.6V, 4.2V, 5V; $V_O$ = 24V, 8s5p, 20mA/string; PWM Freq = 200Hz; Mode 1; L = 6.8µH | Figure 3 |
| Dimming Efficiency | $V_{BAT}$ = 3V, 3.6V, 4.2V, 5V; $V_O$ = 27V, 9s4p, 20mA/string; PWM Freq = 200Hz; Mode 1; L = 6.8µH | Figure 4 |
| Dimming Efficiency | $V_{IN}$ = 5V; $V_{BAT}$ = 3V, 3.6V, 4.2V, 5V, 7.2V, 9V, 12V, 15V; $V_O$ = 18V, 6s6p, 20mA/string; PWM Freq = 200Hz; Mode 1; L = 6.8µH (refer to Figure 18) | Figure 5 |
| Dimming Linearity | $V_{BAT}$ = 3V, 3.6V, 4.2V, 5V; $V_O$ = 21V, 7s6p; $R_{ISET}$ = 53kΩ ; PWM Freq = 200Hz; Mode 1 | Figure 6 |
| Current Limit vs Input Voltage | $V_O$ = 30V; $T_A$ = 25°C | Figure 7 |
| Switching Waveform | $V_{BAT}$ = 3.6V; $V_O$ = 18V, 6s6p; $R_{ISET}$ = 53kΩ; Duty = 100%; L = 6.8µH | Figure 8 |
| Switching Waveform | $V_{BAT}$ = 3.6V; $V_O$ = 18V, 6s6p; $R_{ISET}$ = 53kΩ; PWM Freq = 200Hz; Duty = 50%; L = 6.8µH; Mode 1 | Figure 9 |
| Switching Waveform | $V_{BAT}$ = 3.6V; $V_O$ = 18V, 6s6p; $R_{ISET}$ = 53kΩ; PWM Freq = 200Hz; Duty = 10%; L = 6.8µH; Mode 1 | Figure 10 |
| Switching Waveform | $V_{BAT}$ = 3.6V; $V_O$ = 18V, 6s6p; $R_{ISET}$ = 53kΩ; PWM Freq = 200Hz; Duty = 50%; L = 6.8µH; Mode 2 | Figure 11 |
| Switching Waveform | $V_{BAT}$ = 3.6V; $V_O$ = 18V, 6s6p; $R_{ISET}$ = 53kΩ; PWM Freq = 200Hz; Duty = 10%; L = 6.8µH; Mode 2 | Figure 12 |
| Startup Waveform | $V_{BAT}$ = 3.6V; $V_O$ = 18V, 6s6p; $R_{ISET}$ = 53kΩ; Duty = 100%; L = 6.8µH | Figure 13 |
| Startup Waveform | $V_{BAT}$ = 3.6V; $V_O$ = 18V, 6s6p; $R_{ISET}$ = 53kΩ; PWM Freq = 200Hz; Duty = 10%; L = 6.8µH; Mode 1 | Figure 14 |

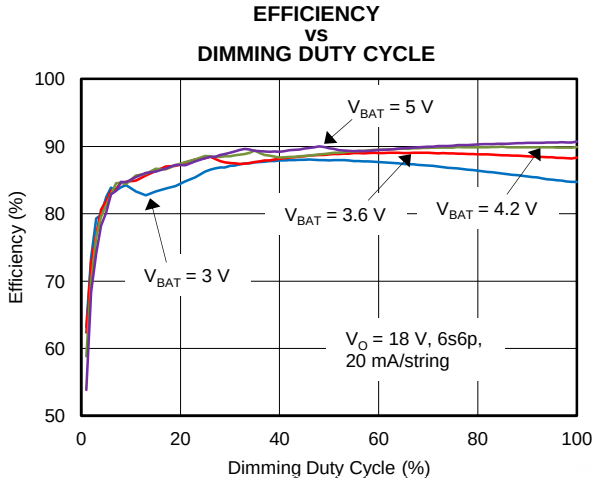


**Figure 1.**

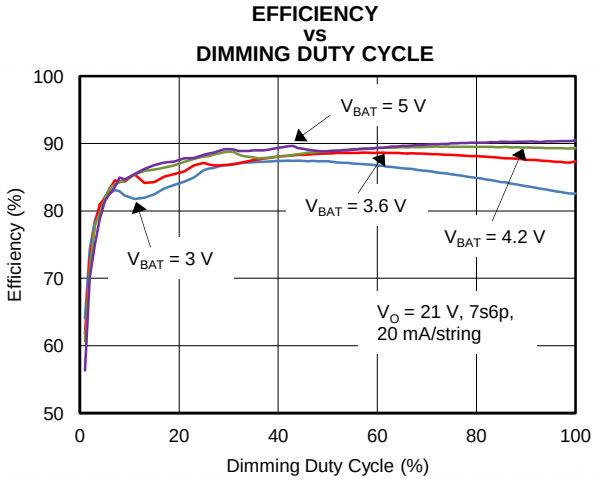


**Figure 2.**


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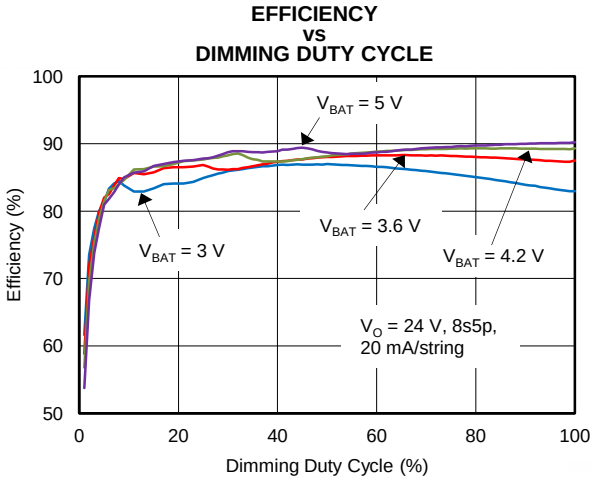



**Figure 3.**

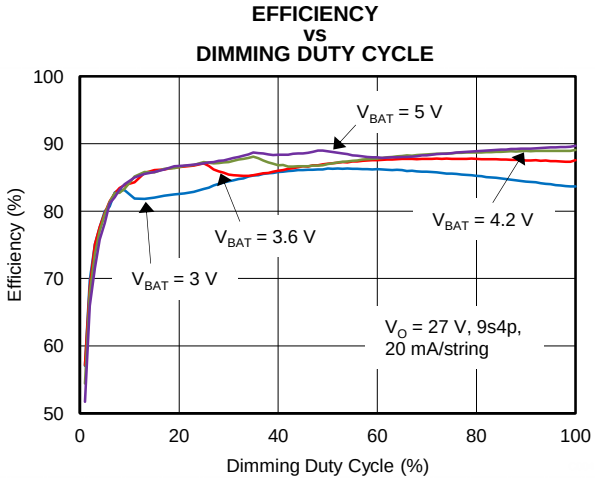
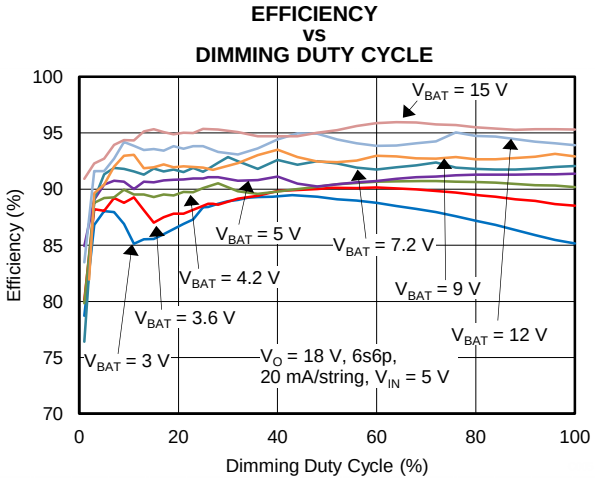



**Figure 4.**

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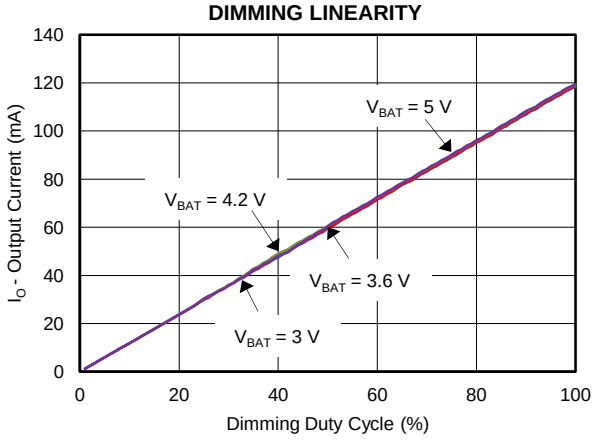


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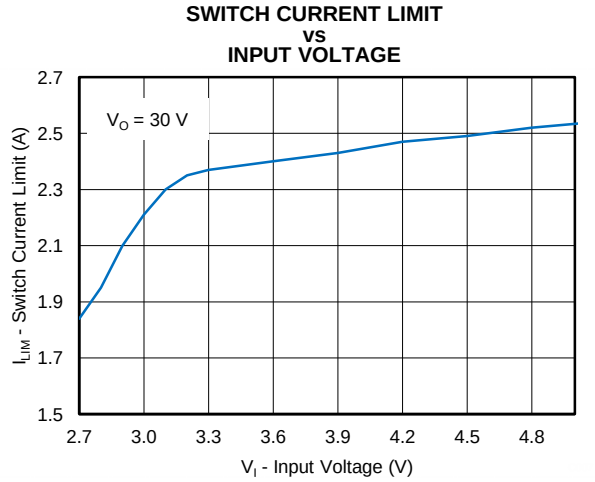



**Figure 7.**

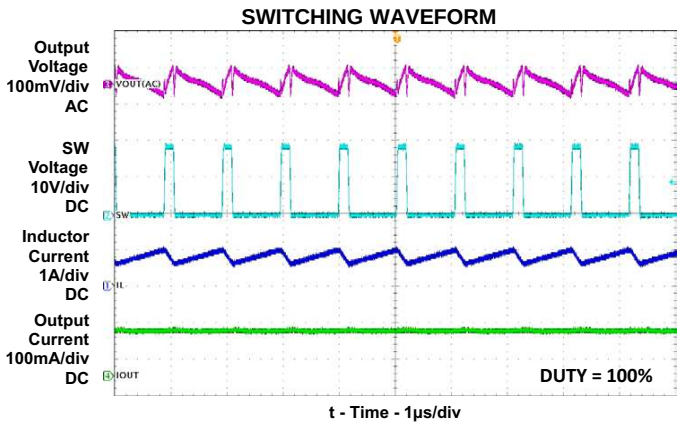



**Figure 8.**

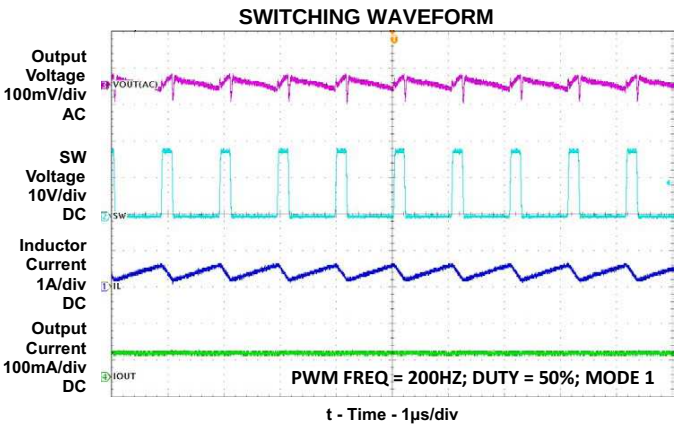



Figure 9.

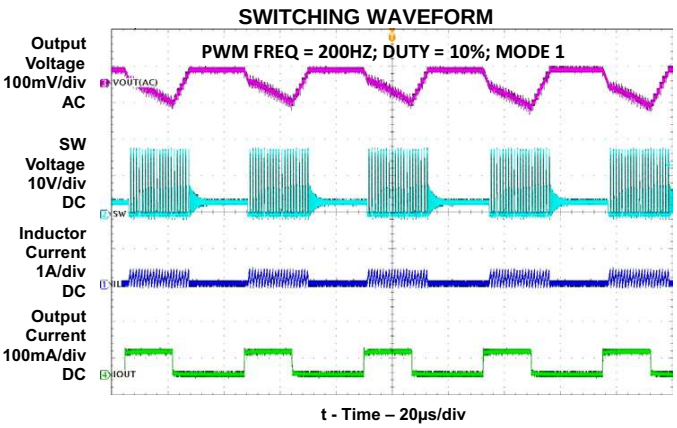
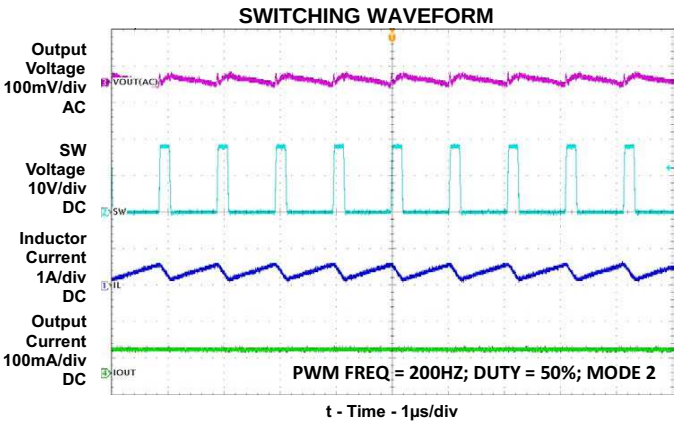



Figure 10.

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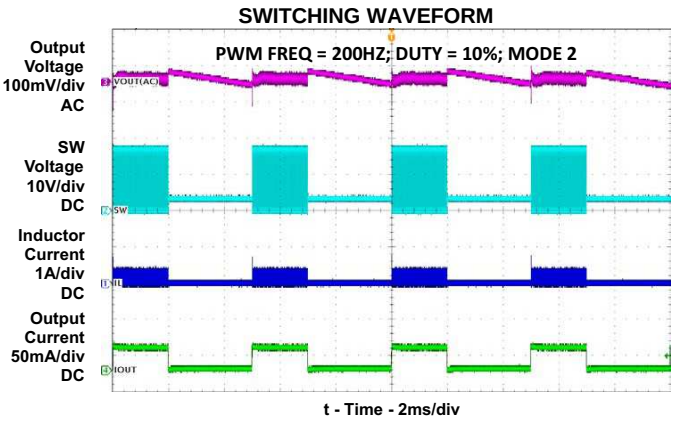


Figure 12.

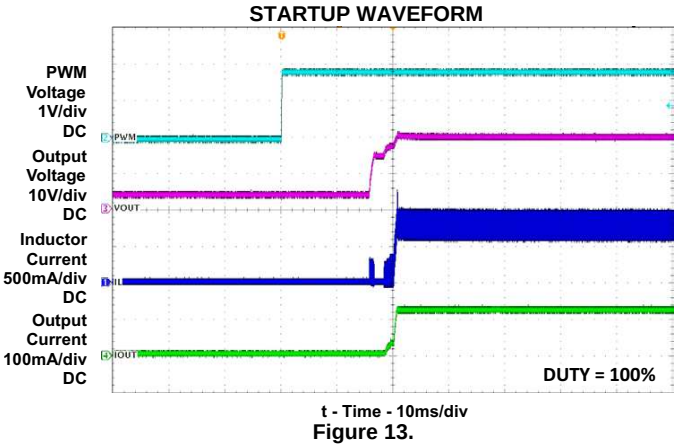


Figure 13.

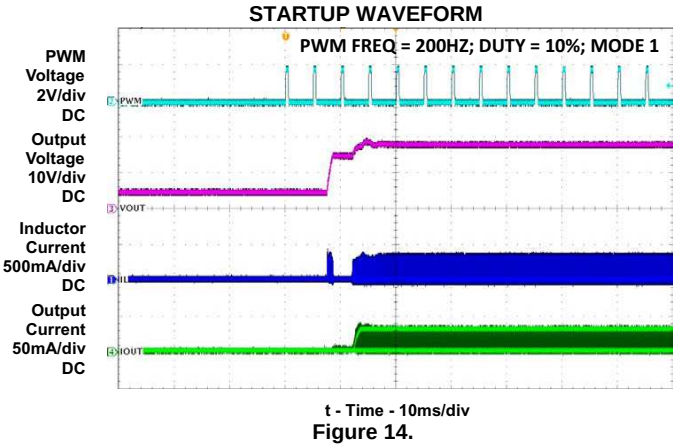


Figure 14.


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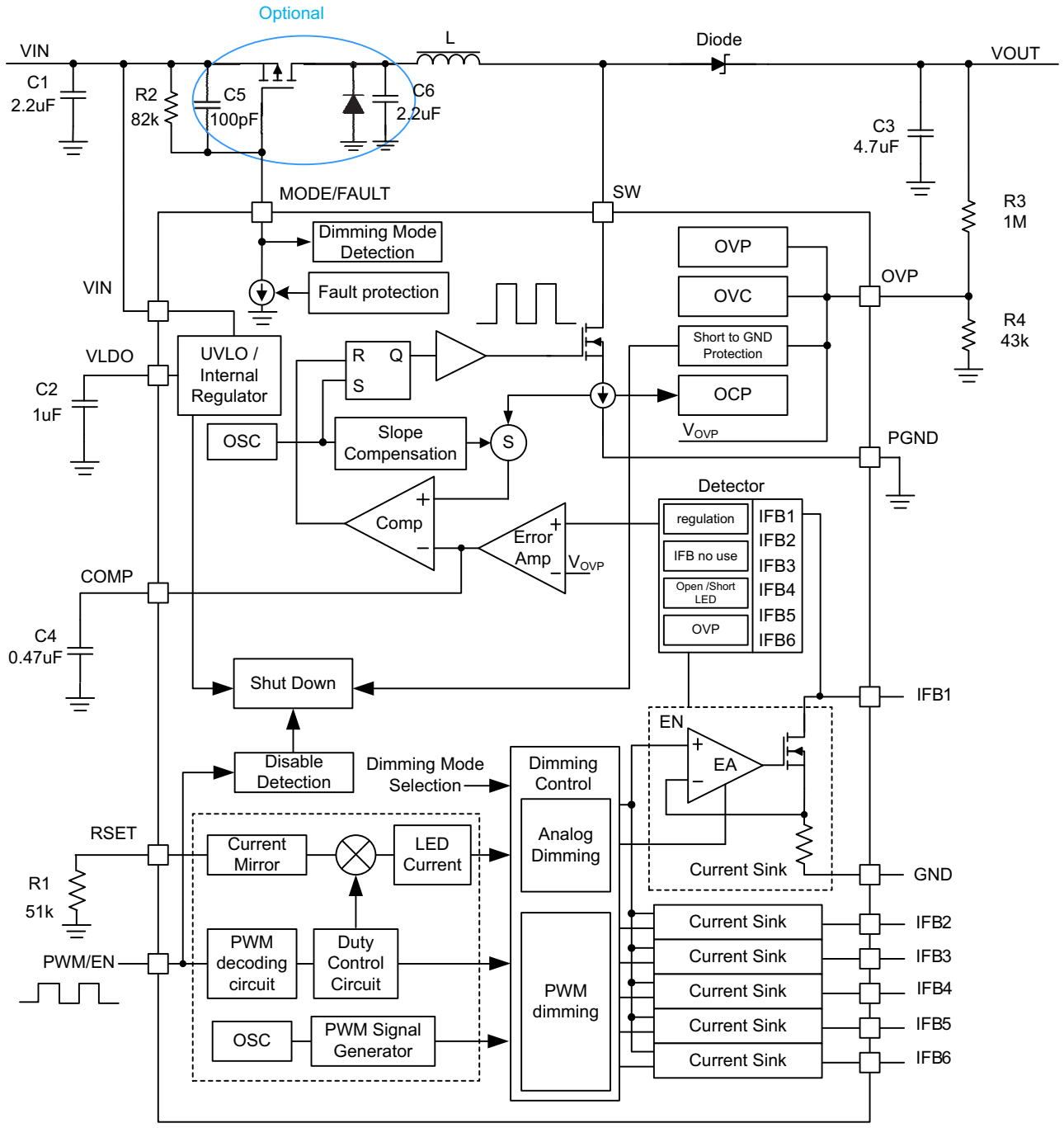
## FUNCTIONAL BLOCK DIAGRAM



## DETAILED DESCRIPTION

TPS61176 is a high-efficiency, multi-channel WLED driver for tablet and notebook backlighting applications. As more and more WLED diodes are required to provide high brightness backlighting for high resolution panels, the WLED diodes must be arranged in parallel strings. Having more WLED diodes in a string reduces the number of parallel strings and thus improves overall current matching; however, the efficiency of the boost regulator drops due to the high output voltage. Therefore, six current sink regulators of high current matching capability are integrated in TPS61176 to provide the WLED connection flexibility and to improve the overall power efficiency. The six channels can also be combined as 2 or 3 channels to drive high brightness WLED diodes.

TPS61176 has integrated all of the key function blocks to power and control up to 60 WLED diodes. The device consists of a boost converter with 2A/40V power MOSFET, six 35mA current sink regulators and protection circuit for over-current, over-voltage, open LED, short LED and output short circuit failures.

TPS61176 accepts PWM dimming signal and implements mixed dimming mode. When the dimming duty cycle is high, analog dimming mode works, under which the IC controls the DC current of the WLED diodes to realize brightness dimming; when the dimming duty cycle is low, the IC switches to PWM dimming mode automatically, so the current of WLED diodes is turned on and off in a high frequency to realize dimming. The automatic switch between analog and PWM dimming modes can leverage the advantages of the two modes: increasing the electrical-to-optical efficiency by analog dimming and avoiding potential color shit issue. The switch point can be programmed to either 25% or 12.5% by the external resistor connected at MODE/FAULT pin.

### SUPPLY VOLTAGE

TPS61176 can support single-cell Li-ion battery input directly. It has a built-in linear regulator to generate supply for internal analog and logic circuits. The VLDO pin, output of the regulator, should be connected to a 1 µF bypass capacitor for the regulator to be controlled in a stable loop. VLDO pin does not have current sourcing capability for external use.

If TPS61176 is used in a multi-cell battery system, the battery cannot be connected to VIN pin directly. In this case, connect a 3.3V or 5V power rail to bias the VIN pin and connect the battery voltage to the inductor. The VIN pin only consumes less than 3mA for normal operation. Please refer to APPLICATION INFORMATION section for more details.

### BOOST CONVERTER

The boost converter of TPS61176 has a fixed switching frequency of 1MHz and uses current-mode control. A 2A/40V power MOSFET is integrated so TPS61176 has a strong output driving capability. A 0.47µF~1µF capacitor should be connected at COMP pin to ensure stable output over the full input and output voltage ranges assuming the recommended inductance and output capacitance values shown in the Recommended Operating Conditions section are used. COMP pin is very sensitive, so careful layout is required to make sure no noise is coupled to it.

The output voltage of the boost is automatically set by the IC to minimize the voltage drop across the IFBx (IFB1 ~ IFB6) pins. Normally the voltage across each WLED string is not same, so the voltages at IFBx pins are different. The IC regulates the lowest IFBx voltage to 450mV, and consistently adjusts the boost output voltage to account for any change of WLED's forward voltage drop. If the input voltage is higher than the strings' forward voltage drop (e.g. at low duty cycles), the boost converter can't regulate the output due to its minimum duty cycle limitation. In this case, increasing the number of WLED diodes in series is helpful to provide enough headroom for the converter to boost the voltage.

### CURRENT SINKS

The six current sink regulators embedded in TPS61176 can output up to 35mA current each. By regulating the current sinks, TPS61176 controls the current of the WLED strings to realize brightness dimming. The full-scale current per channel is programmed by the resistor at ISET pin according to Equation 1.

$$I_{FBx_full} = \frac{V_{ISET_full}}{R_{ISET}} \times K_{ISET} \quad (1)$$

Where:

$I_{FBx_full}$, full-scale current per channel
$K_{ISET}$ = 1024 (Current multiple)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$V_{ISET_full}$ = 1.04V (ISET pin voltage under 100% dimming duty cycle)
$R_{ISET}$ = ISET pin resistor

## IFBx PIN UNUSED

If less than six channels are used, a user can easily disable the unused channel(s) by shorting the corresponding IFBx pin(s) to ground. TPS61176 detects IFBx pins' short status during startup process and will disable the unused channel(s) before the boost converter starts switching.

## ENABLE AND STARTUP

TPS61176 receives PWM signal at PWM/EN pin to implement the dimming as well as to enable and disable the IC. When PWM signal (high logic or PWM pulse) is input, the IC is enabled automatically; when the PWM signal is pulled low for more than 20ms, the IC is disabled and enters into shutdown mode. In shutdown mode, the boost converter stops switching, and the MODE/FAULT pin is internally pulled to VIN to turn off external isolation MOSFET for true shutdown. The input supply current at VIN pin is 4μA (max) in shutdown mode. In order to avoid fault triggered shut down during dimming, PWM dimming signal should have a higher frequency than 100Hz.

Once enabled by PWM input, TPS61176 enters startup process. The internal regulator is enabled first to supply current to internal circuits. Then TPS61176 detects the $R_{MODE}$ at MODE/FAULT pin to set the dimming mode. TPS61176 can detect if the mode resistor is connected between VIN pin and MODE/FAULT pin or connected between MODE/FAULT pin and GND pin. If the mode resistor is detected to be between VIN pin and MODE/FAULT pin, which indicates an external isolation P-channel MOSFET is connected, the MODE/FAULT pin will be pulled down by an internal current sink to turn on the isolation MOSFET after the detection process. The IC also checks the status of all IFBx pins (short to ground or not) to disable any unused channels. There is no special time sequence requirement of VIN and PWM signals for startup. If PWM signal is input first, TPS61176 starts up when VIN powers up.

The dimming mode and IFBx status detection process lasts about 4ms, during which the MODE/FAULT pin outputs a high voltage (VIN – 0.6V typical) to keep the isolation MOSFET off. When the 4ms detection window ends, an internal current sink pulls MODE/FAULT pin low to turn on the isolation MOSFET. Then another 4ms time window starts and at the end of the window the IC detects the OVP pin voltage. If the OVP voltage $V_{OVP}$ is still lower than $V_{OVP_SC}$ ramp up threshold (90mV typ.), which normally indicates output short to ground issue happens, the boost remains off and the MODE/FAULT pin is pulled up to VIN immediately by an internal resistor to turn off the isolation MOSFET. In this case, the IC restarts only after a power-on reset (POR) toggling or PWM toggling. POR toggling means the VIN pin voltage is pulled below UVLO falling threshold first and then pulled above UVLO rising threshold to restart the IC; PWM toggling means pulling PWM/EN low for more than 20ms to disable the IC and then apply PWM signal (high logic or PWM pulse) to restart the IC. If OVP voltage $V_{OVP}$ is higher than $V_{OVP_SC}$ ramp up threshold, indicating no short to ground issue is detected, boost starts switching to raise the output voltage. Soft start is implemented by gradually ramping up the reference voltage of the error amplifier to prevent voltage over-shoot and in-rush current. The capacitor at COMP pin can adjust the soft start speed. Larger capacitance leads to slower start up. 0.47μF~1μF COMP capacitor is recommended.

## BRIGHTNESS DIMMING CONTROL

TPS61176 receives the PWM dimming signal at PWM/EN pin. An internal PWM decoding circuit detects the on time and the period of the PWM signal and calculates the duty cycle information. Then the IC controls the current sink regulators' output current according to the duty cycle to realize the brightness dimming.

TPS61176 supports mixed dimming mode, which leverages the advantages of both analog dimming and PWM dimming modes. When the dimming duty cycle is high, analog dimming mode is auto-implemented, increasing the electrical-to-optical efficiency and reducing the power budget for the backlight; when the dimming duty cycle is low, PWM dimming mode is auto-implemented, eliminating potential color shift effect which normally happens when the DC current of WLED diode goes low. The switch point between analog dimming mode and PWM dimming mode can be programmed by the mode resistor connected at MODE/FAULT pin.

TPS61176 provides four dimming mode options as shown in Table 2. Besides two different switch point options: 25% or 12.5%, TPS61176 also offers two different PWM dimming mode options: direct PWM dimming or 22kHz fixed frequency PWM dimming. Please refer to DIMMING MODE for the details of different dimming modes.

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Different mode resistor values set the different dimming modes. 5% or higher precision resistor should be used for the mode resistor. When an isolation P-channel MOSFET is connected, the mode resistor must be connected between VIN pin and MODE/FAULT pin; when the isolation MOSFET is not connected, the mode resistor should be connected between MODE/FAULT pin and ground. If there is no resistor connected at MODE/FAULT pin, which is only allowed when the isolation MOSFET is not connected, default mode (Mode 1) will be selected. Please refer to APPLICATION INFORMATION section for more details.

**Table 2. Dimming Mode Setting**

| MODE | MODE RESISTOR | DIMMING MODE | SWITCH POINT BETWEEN ANALOG AND PWM DIMMING |
|---|---|---|---|
| Mode 1 (Default mode) | 1.3 MΩ (5%) | Analog dimming + 22 kHz fixed frequency PWM dimming | 25% |
| Mode 2 | 620 kΩ (5%) | Analog dimming + Direct PWM dimming | 25% |
| Mode 3 | 220 kΩ (5%) | Analog dimming + 22 kHz fixed frequency PWM dimming | 12.5% |
| Mode 4 | 82 kΩ (5%) | Analog dimming + Direct PWM dimming | 12.5% |

## DIMMING MODE

### ANALOG DIMMING MODE

In analog dimming mode, the brightness dimming is realized by controlling the DC current of WLED diodes. Since the forward voltage of a WLED diode drops when its DC current reduces, the required output voltage can become lower when dimming duty cycle goes low, reducing the power budget for the backlight and allowing more system power saving.

In analog dimming mode, the current of IFBx is regulated according to Equation 2:

$$I_{FBx} = \frac{V_{ISET}}{R_{ISET}} \times K_{ISET} = \frac{V_{ISET_full}}{R_{ISET}} \times K_{ISET} \times Duty \quad (2)$$

Where:

$I_{FBx}$, current per string
$V_{ISET}$, (ISET pin voltage during analog dimming)
$K_{ISET}$ = 1024 (Current multiple)
$V_{ISET_full}$ = 1.04V (ISET pin voltage with 100% dimming duty cycle)
$R_{ISET}$ = ISET pin resistor
Duty = duty cycle of the PWM signal

### PWM DIMMING

When the dimming duty cycle is below the switch point, PWM dimming mode is automatically implemented. In this mode, the current sink regulators are turned on and off according to the PWM duty cycle information, so the illumination of WLEDs is intermittent. At frequencies higher than human eyes' critical flicker frequency, the brightness is the same as the average brightness of the fluctuating light, thus controlling the duty cycle can realize the brightness dimming.

While a current sink regulator is turned on during PWM dimming, its output current is equal to the DC current at the switch point. For example, if the switch point is set to 25%, the regulator's output current during the "ON" phase is equal to $I_{FBx_full}$ x 25%, and the "ON" phase's duty cycle Duty' is equal to Duty / 25%, where Duty is the input PWM signal's duty cycle information. Then the average current during PWM dimming can be still equal to $I_{FBx_full}$ x Duty. This design is in order to keep the brightness consistency between analog dimming and PWM dimming and avoid any abrupt brightness change around the switch point. If the switch point is set to 12.5%, the regulator's output current during the "ON" phase is equal to $I_{FBx_full}$ x 12.5%, and the "ON" phase's duty cycle Duty' is equal to Duty / 12.5%. Refer to Figure 15 for a graphical explanation.


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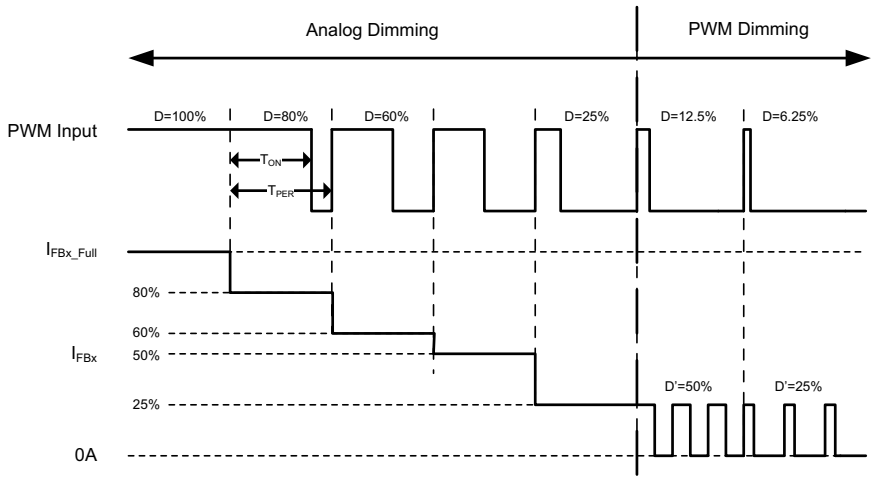
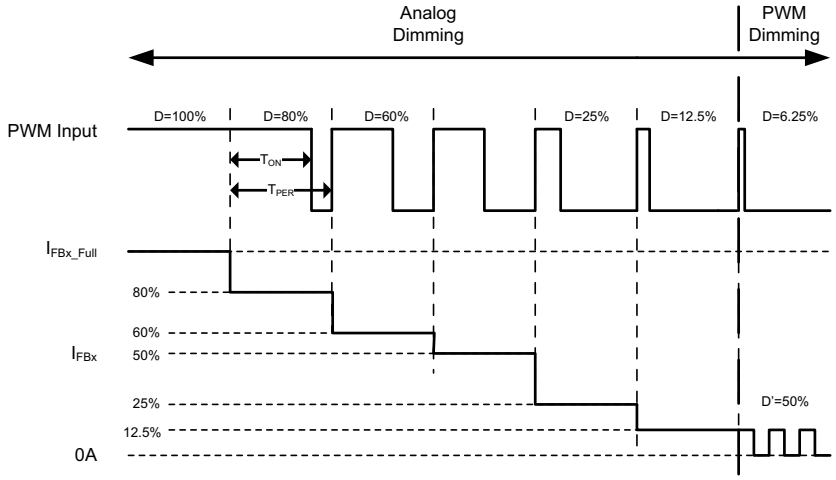



(a). Mixed Dimming Mode with switch point = 25%




(b). Mixed Dimming Mode with switch point = 12.5%

**Figure 15. Mixed Dimming Mode**

Generally, the average current of an LED string in PWM dimming mode is equal to

$$I_{FBx_PWM} = \frac{V_{ISET_full}}{R_{ISET}} \times K_{ISET} \times Duty \quad (3)$$

Where:

$I_{FBx_PWM}$, average current per string in PWM dimming mode
$V_{ISET_full}$ = 1.04V (ISET pin voltage with 100% dimming duty cycle)
$K_{ISET}$ = 1024 (Current multiple)
$R_{ISET}$ = ISET pin resistor
Duty = duty cycle of the PWM signal

The frequency of the current sink regulators' ON and OFF control depends on which PWM dimming mode is set. TPS61176 provides two different PWM dimming modes: direct PWM dimming mode and 22kHz fixed frequency PWM dimming mode.

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In direct PWM dimming mode, the current sinks are turned ON and OFF with the same frequency detected from the input PWM signal. The advantage of this mode is the dimming frequency can be adjusted freely. In addition, it is easy to achieve high dimming resolution in direct PWM dimming mode: with lower input PWM frequency, the higher dimming resolution can be detected and output. For example, when the input PWM frequency is 100Hz, 14-bit resolution can be achieved; when the input PWM frequency is 20kHz, 9-bit resolution achieved. So if high resolution is required, 100Hz or 200Hz dimming frequency is recommended. TPS61176 is designed to minimize the AC ripple on the output capacitor during PWM dimming. Careful passive component selection is also crucial to minimize AC ripple on the output capacitor. In order to further avoid the potential audible noise, input PWM frequency out of audible frequency range is recommended. See APPLICATION INFORMATION for more information.

In 22kHz fixed frequency PWM dimming mode, current sinks are turned on and off according to the duty cycle information detected from the input PWM signal but with an internally fixed frequency – 22kHz. This mode facilitates the application where the input PWM signal frequency can't be adjusted outside the audio frequency range. So in this mode the audible noise can be eliminated completely.

Human eyes are much more sensitive to the brightness change at low brightness compared to at high brightness, so in order to improve the visual experience and avoid any potential flickering perception, high resolution dimming is implemented in PWM dimming mode. TPS61176 can achieve up to 14-bit dimming resolution during the PWM dimming. Generally, higher resolution can be achieved with lower input PWM frequency. Please refer to Table 3 for detailed dimming resolution information.

**Table 3. Dimming Resolution Information in PWM Dimming Mode**

| DIMMING MODE | INPUT PWM FREQUENCY | DIMMING RESOLUTION IN PWM DIMMING MODE |
|---|---|---|
| Mode 1 | 100Hz ~ 4.5kHz | 12-bit |
| | 4.5kHz ~ 9kHz | 11-bit |
| | 9kHz ~ 18kHz | 10-bit |
| | 18kHz ~ 20kHz | 9-bit |
| Mode 2 | 100Hz ~ 1kHz | 14-bit |
| | 1kHz ~2kHz | 13-bit |
| | 2kHz ~ 4kHz | 12- bit |
| | 4kHz ~ 8kHz | 11-bit |
| | 8kHz ~ 16kHz | 10-bit |
| | 16kHz ~ 20kHz | 9 -bit |
| Mode 3 | 100Hz ~ 5kHz | 12-bit |
| | 5kHz ~ 10kHz | 11-bit |
| | 10kHz ~ 20kHz | 10-bit |
| Mode 4 | 100Hz ~ 1.2kHz | 14-bit |
| | 1.2kHz ~2.4kHz | 13-bit |
| | 2.4kHz ~ 4.8kHz | 12- bit |
| | 4.8kHz ~ 9.6kHz | 11-bit |
| | 9.6kHz ~ 20kHz | 10-bit |

## OVER VOLTAGE PROTECTION

The output voltage of the boost converter is detected by OVP pin. The Over-Voltage-Protection threshold can be programmed by an external resistor divider (R3 and R4 in Typical Application Circuits), allowing the usage of low voltage rating Schottky diode in low output voltage application. The correct divider ratio is important for optimum operation of TPS61176. Use the following guidelines to choose the divider value. It can be noise sensitive if $R_{upper}$ and $R_{down}$ have high impedance. Careful layout is required. Also, choose lower resistance values for $R_{upper}$ and $R_{down}$ when power dissipation allows.

Step1. Determine the maximum output voltage, $V_{OUT}$, for the system according to the number of series WLEDs.
Step2. Select $R_{upper}$ resistor value (1 MΩ for a typical application; a lower value such as 100 kΩ for a noisy environment).
Step3. Calculate $R_{down}$ by using Equation 4.


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$$V_{OUT} = \left( \frac{R_{upper}}{R_{down}} + 1 \right) \times V_{OVP_clamp} \quad (4)$$

Where: $V_{OVP_clamp}$ = 1.5 V

When the over-voltage threshold $V_{OVP_clamp}$ is reached, TPS61176 detects if there is any LED string open first by sensing whether there is current on IFBx pin. If any string is open, the corresponding current sink is disabled and removed from regulation. Subsequently, the output voltage drops down and will be regulated to a voltage for the connected WLED strings. The IFBx current of the connected WLED strings keeps in regulation during the whole transition. If an open string is reconnected again, a POR toggling or PWM toggling is required to reactivate a previously deactivated string. TPS61176 shuts down and keeps off when it detects that all of the WLED strings are open. In this case, a POR toggling or PWM toggling is required to restart the IC. If there isn't any string open, TPS61176 regulates the boost output at the over-voltage threshold.

If the output voltage can't be regulated at the value set by Equation 4 and keeps rising, once the OVP pin voltage exceeds $V_{OVP_sd}$ rising threshold (1.6V typical), the boost stops switching. When the OVP voltage falls below $V_{OVP_sd}$ falling threshold (1.55V typical), the boost recovers to switch. During the process, the IFBx current of the connected WLED strings keeps in regulation.

## CURRENT SINK OPEN PROTECTION

If any IFBx pin voltage is detected to exceed the 1st level IFB over-voltage threshold (8.5V typical) when its current sink is turned on, TPS61176 turns off this current sink and removes it from output regulation loop. The current regulation of the remaining IFBx pins is not affected. This situation often occurs when there are several shorted WLED diodes in one string. WLED mismatch typically does not create such large voltage difference among WLED strings. TPS61176 shuts down when it detects that all of the IFBx pin voltages exceed the threshold. In this case, a POR toggling or PWM toggling is required to restart the IC.

If any IFBx pin voltage is detected to exceed the 2nd level IFB over-voltage threshold (18V typical) no matter the current sink is turned on or off, TPS61176 shuts down immediately to avoid potential over stress damage at IFBx pin. A POR toggling or PWM toggling is required to restart the IC.

## OVER CURRENT AND SHORT CIRCUIT PROTECTION

TPS61176 has a pulse-by-pulse over-current limit of 2.0A (min). The boost power MOSFET is turned off when the inductor current reaches this current limit threshold and it remains off until the beginning of the next switching cycle. This protects TPS61176 and external component under overload conditions.

Under severe over-load or short circuit conditions, if the OVP pin voltage is detected below $V_{OVP_SC}$ ramp down threshold (70mV typical), TPS61176 shuts down and the MODE/FAULT pin is pulled to VIN by an internal switch immediately. As a result, the external isolation MOSFET can be turned off at once, cutting off the power path from input to output. The IC restarts after a POR toggling or PWM toggling.

## THERMAL PROTECTION

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

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# APPLICATION INFORMATION

## INDUCTOR SELECTION

Because the selection of the inductor affects power supply's steady state operation, transient behavior, loop stability and the boost converter efficiency, the inductor is the most important component in switching power regulator design. There are three specifications most important to the performance of the inductor: inductance value, DC resistance and saturation current. TPS61176 is designed to work with inductor values between 4.7µH and 10µH. A 4.7µH inductor is typically available in a smaller or lower profile package, while a 10µH inductor produces lower inductor ripple. If the boost output current is limited by the over-current protection of the IC, using a 10µH inductor can maximize the controller's output current capability.

In a boost regulator, the inductor DC current can be calculated as Equation 5.

$$I_{DC} = \frac{Vout \times Iout}{Vin \times \eta} \tag{5}$$

Where

Vout = boost output voltage
Iout = boost output current
Vin = boost input voltage
η = power conversion efficiency, use 85% for TPS61176 normal applications

The inductor current peak to peak ripple can be calculated as Equation 6.

$$I_{PP} = \frac{1}{L \times \left( \frac{1}{Vout - Vin} + \frac{1}{Vin} \right) \times F_S} \tag{6}$$

Where

$I_{PP}$ = inductor peak-to-peak ripple
L = inductor value
$F_S$ = Switching frequency
Vout = boost output voltage
Vin = boost input voltage

Therefore, the peak current seen by the inductor is calculated with Equation 7.

$$I_P = I_{DC} + \frac{I_{PP}}{2} \tag{7}$$

Select the inductor with saturation current over the calculated peak current. To calculate the worse case inductor peak current, use minimum input voltage, maximum output voltage and maximum load current.

Converter efficiency is dependent on the resistance of its high current path and switching losses associated with the internal switch and external power diode. Although TPS61176 has optimized the internal switch resistance, the overall efficiency is affected by the inductor's DC resistance (DCR). Lower DCR improves efficiency. However, there is a trade off between DCR and inductor footprint. Furthermore, shielded inductors typically have higher DCR than unshielded ones.

Note that inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. Table 4 lists the recommended inductors.

**Table 4. Recommended Inductor for TPS61176**

| Part Number | L (µH) | DCR (mΩ) | Isat (A) | Size (L x W x H mm) | Vendor |
|---|---|---|---|---|---|
| PCMB051H-4R7MS | 4.7 | 78 | 4.0 | 5.4 x 5.2 x 1.8 | Cyntec |
| PCMB051H-6R8MS | 6.8 | 107 | 3.4 | 5.4 x 5.2 x 1.8 | Cyntec |
| PCMB051H-100MS | 10 | 140 | 3 | 5.4 x 5.2 x 1.8 | Cyntec |
| LPS4018-472ML | 4.7 | 125 | 1.9 | 4.0 x 4.0 x 1.8 | Coilcraft |


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**Table 4. Recommended Inductor for TPS61176 (continued)**

| Part Number | L (µH) | DCR (mΩ) | Isat (A) | Size (L x W x H mm) | Vendor |
|---|---|---|---|---|---|
| LPS4018-103ML | 10 | 200 | 1.3 | 4.0 x 4.0 x 1.8 | Coilcraft |
| A915AY – 4R7M | 4.7 | 38 | 1.87 | 5.2 x 5.2 x 3 | TOKO |
| A915AY – 100M | 10 | 75 | 1.24 | 5.2 x 5.2 x 3 | TOKO |

## OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet the requirement for the loop stability and the output ripple. The loop is designed to be stable with an output capacitor within 2.2µF ~ 10µF range. This output ripple is related to the capacitor's capacitance and its equivalent series resistance (ESR). Due to its low ESR, the ripple caused by ESR could be neglected for ceramic capacitors. Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated with Equation 8.

$$Cout = \frac{(Vout - Vin) \times Iout}{Vout \times F_S \times Vripple} \quad (8)$$

Where: Vripple = peak-to-peak output ripple.

Note that capacitor degradation increases the ripple much. Select the capacitor which has less degradation at the output voltage. If the output ripple is too large, change a bigger capacitor could be helpful. Normally, X5R ±10% or better capacitors are recommended.

## SCHOTTKY DIODE SELECTION

TPS61176 demands a low forward voltage, high-speed rectification and low capacitance schottky diode for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. Vishay SS2P5, MSS1P4 and NXP PMEG4010EPK are recommended for TPS61176.

## ISOLATION FET SELECTION

TPS61176 provides a gate driver at MODE/FAULT pin to drive an external P-channel MOSFET which can act as an isolation MOSFET. When the IC is disabled or output short to ground issue happens, MODE/FAULT pin can turn off the isolation MOSFET to cut off the power path from the battery to the output. The source of the MOSFET should be connected to the battery input, and an external resistor must be connected between the source and gate of the MOSFET to keep the FET off when TPS61176 is disabled. This gate resistor also acts as a mode resistor to select the dimming mode. To turn on the isolation MOSFET, an internal current sink pulls MODE/FAULT pin low. When output short to ground fault happens, an internal switch pulls up the MODE/FAULT pin to VIN, turning off the isolation MOSFET immediately.

When the isolation FET is turned on during startup, an inrush current will flow through the MOSFET from battery to charge the output capacitor. If the peak current is too large, a capacitor can be connected between the source and the gate of the isolation MOSFET to control the turning on speed (C5 in Figure 16), thus controlling the inrush current. Normally, 100pF ~ 1nF capacitor is recommended.

During output short to ground protection process, the catch diode (D2 in Figure 16) may be forward biased to provide the continuous current of the inductor when the isolation FET is turned off. In this case, the drain of the isolation FET swings below ground. The voltage across the isolation FET can be momentarily greater than the input voltage. Therefore, select at least 10V maximum input MOSFET. Adding a capacitor parallel with D2 (refer to Figure 16) could also help reduce the voltage across MOSFET when this failure happens. The on resistance of the MOSFET has large impact on power conversion efficiency since the MOSFET carries the input current. Select a MOSFET with Rds(on) less than 100mΩ to limit the power losses. In order to detect larger than 1M $R_{Mode}$ correctly, the gate leakage of isolation MOSFET should be less than 0.1µA.

In multi-cell battery input applications, if the isolation MOSFET is connected, the voltage at MODE/FAULT pin may exceed its maximum rating voltage 7V when the IC is disabled or output short to ground issue happens. In order to prevent this over stress damange, isolation MOSFET can't be connected.

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## AUDIBLE NOISE REDUCTION

The controller's output voltage also ripples due to the load transient that occurs during PWM dimming. If the PWM dimming frequency is in the audible frequency range, the ripple can produce audible noises on the output ceramic capacitor. There are two ways of reducing or eliminating the audible noise. The first way is to reduce the amount of the output ripple, and therefore minimize the audible noise. TPS61176 adopts a patented technology to limit this type of output ripple even with the minimum recommended output capacitance. The second way is to select PWM dimming frequency outside the audible frequency range to eliminate the audible noise completely. However, in some applications, the input PWM signal's frequency range couldn't be adjusted outside the audible frequency range. To solve this problem, TPS61176 provides the 22kHz fixed frequency PWM dimming mode. In this dimming mode, no matter what the input PWM frequency is, the PWM dimming is implemented at 22kHz, which is outside the audible frequency range, saving the effort to adjust the input PWM frequency.

## LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in the typical application circuit Figure 16, needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the input ripple seen by the IC. It should also be placed close to the inductor. C3 is the filter and noise decoupling capacitor for the internal linear regulator powering the internal digital circuits. It should be placed as close as possible between the VLDO and GND pins to prevent any noise insertion to the digital circuits. The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the SW pin to the inductor and schottky diode should be kept as short and wide as possible. The trace between schottky diode and the output capacitor C2 should also be as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the PGND pin since there is a large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point, for example on the thermal pad. The thermal pad needs to be soldered on to the PCB and connected to the GND pin of the IC. An additional thermal via can significantly improve power dissipation of the IC.


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## TYPICAL APPLICATION CIRCUITS

### SINGLE-CELL BATTERY INPUT APPLICATION

TPS61176's VIN pin voltage range is from 2.7V to 6.5V, so it can support single-cell battery input directly. If isolation MOSFET is connected, the mode resistor must be connected between VIN pin and MODE/FAULT pin as shown in Figure 16; if isolation MOSFET is not connected, the mode resistor can be connected between VIN pin and GND as shown in Figure 17. If there is no resistor connected at MODE/FAULT pin, which is only allowed when the isolation MOSFET is not connected, default mode (Mode 1) will be selected.

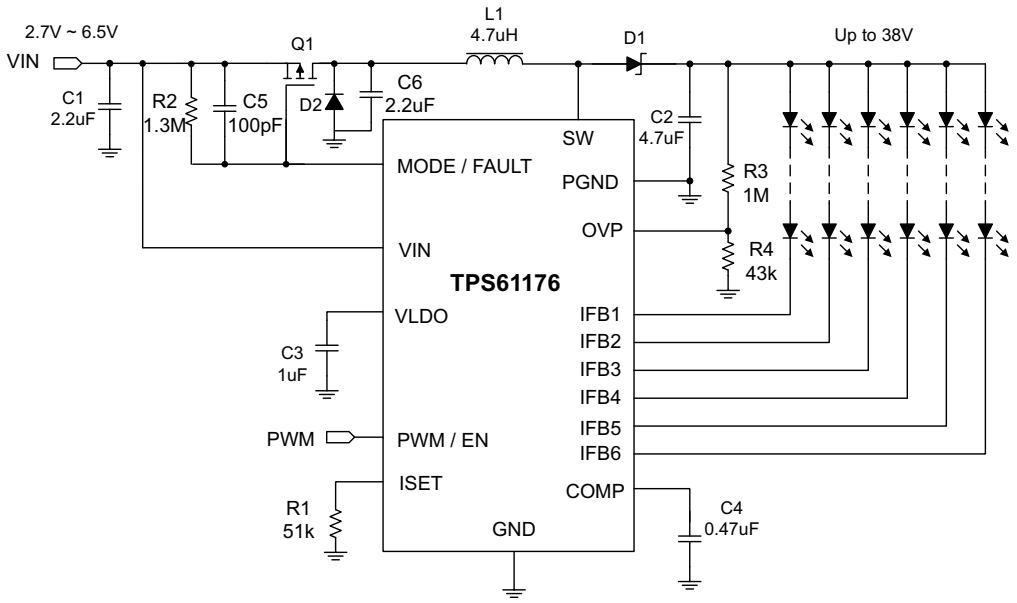


**Figure 16. Typical Applications (single-cell battery input application)**

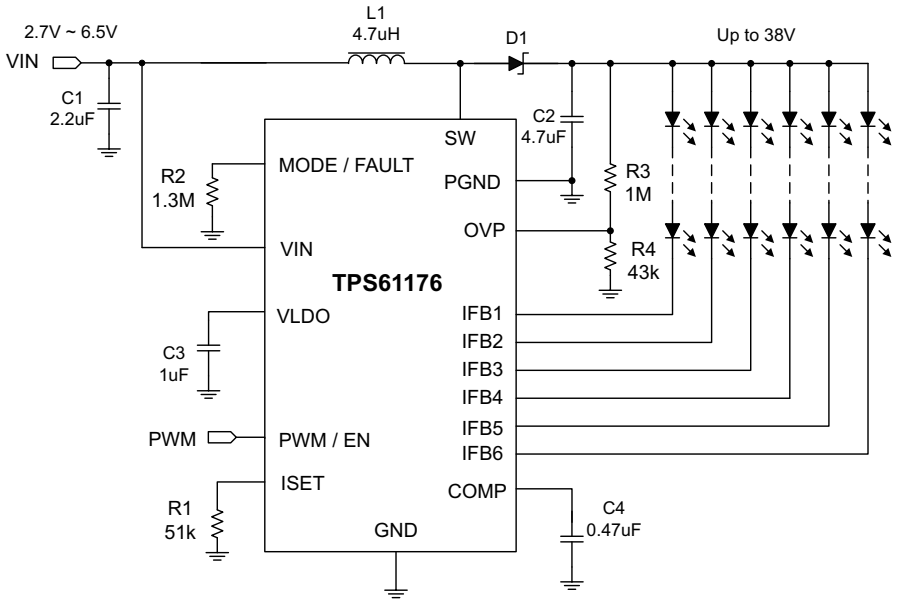


**Figure 17. Typical Applications (single-cell battery input without isolation MOSFET application)**

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## MULTI-CELL BATTERY INPUT APPLICATION

In multi-cell battery input applications, because normally the input voltage is higher than VIN pin and MODE/FAULT pin's maximum rating voltage 7V, the battery input can't be connected to VIN pin directly and the isolation MOSFET can't be connected either. A 3.3V or 5V bias is required to power VIN pin of the IC with up to 3mA current consumption, and the mode resistor should be connected between MODE/FAULT pin and ground. Please refer to Figure 18 as below.

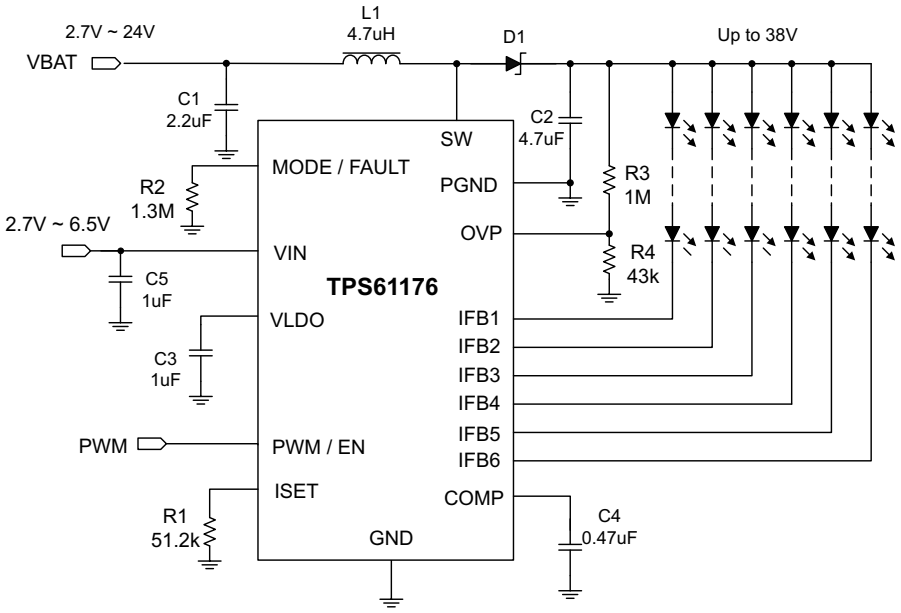


**Figure 18. Typical Applications (Multi-cell battery input application)**

## COMBINED STRING APPLICATION

TPS61176 provides six current sinks with up to 35mA current capability each. If high brightness WLED diodes are used, the current sinks can be combined as two or three channels to support higher current capability requirement. Please refer to Figure 19 as below.

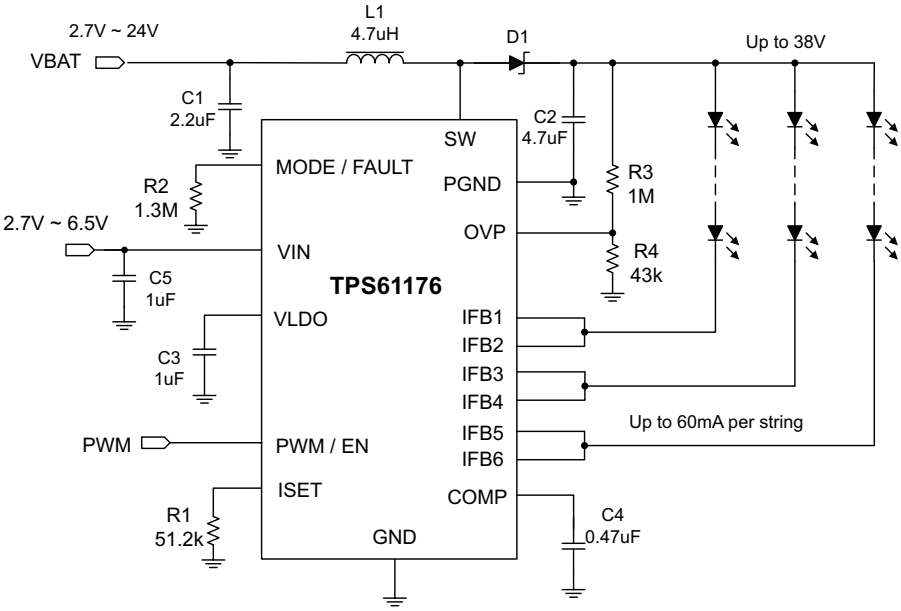


**Figure 19. Typical Applications (combined string to support high brightness WLED diodes)**


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## SEPARATE PWM AND EN SIGNALS APPLICATION

TPS61176 can be enabled or disabled automatically according to the PWM signal's status. However, if the user wants to use separate EN and PWM signals to control the driver, the application circuit in Figure 20 or Figure 21 are recommended.

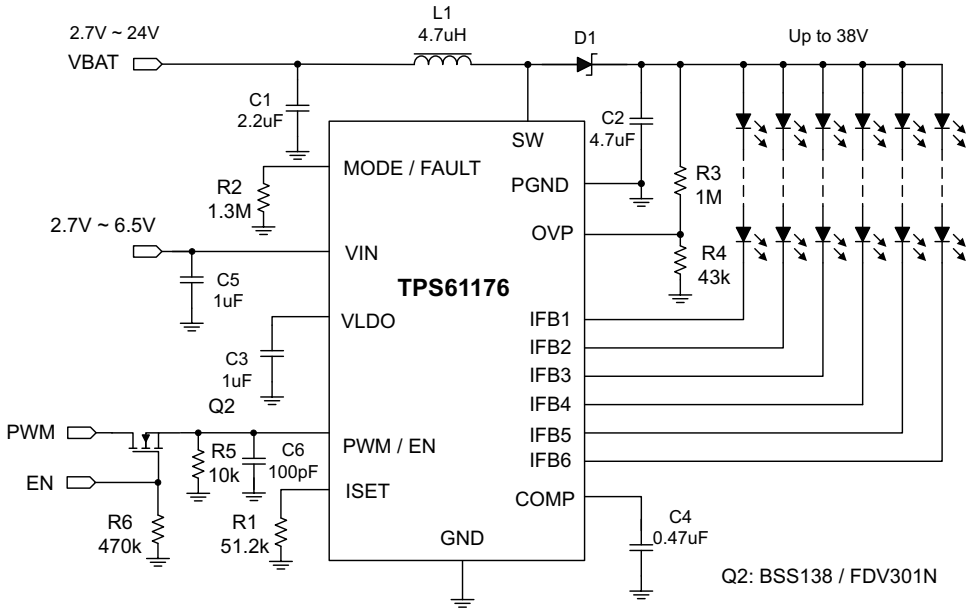


**Figure 20. Typical Applications (to support separate 3.3V logic PWM and EN signals)**

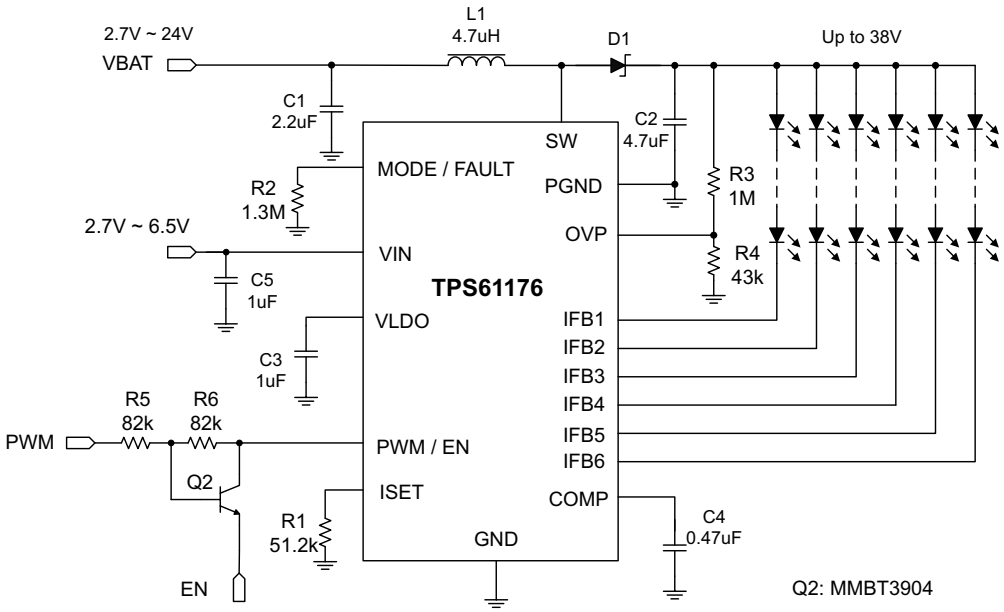


**Figure 21. Typical Applications (to support separate 1.8V logic PWM and EN signals)**

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## REVISION HISTORY

| Changes from Original (December 2012) to Revision A | Page |
|---|---|
| • 校正了整个数据表内的封装说明 | 1 |
| • Removed Ordering Information table. | 2 |


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## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TPS61176RTER | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PZJI |
| TPS61176RTER.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PZJI |
| TPS61176RTERG4 | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PZJI |
| TPS61176RTERG4.A | Active | Production | WQFN (RTE) \| 16 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | PZJI |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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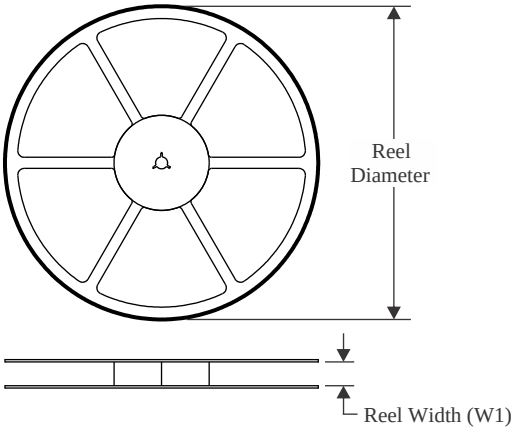
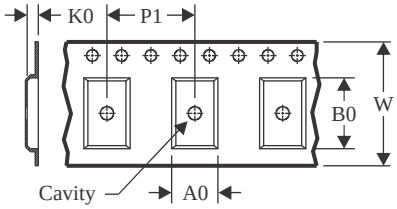
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

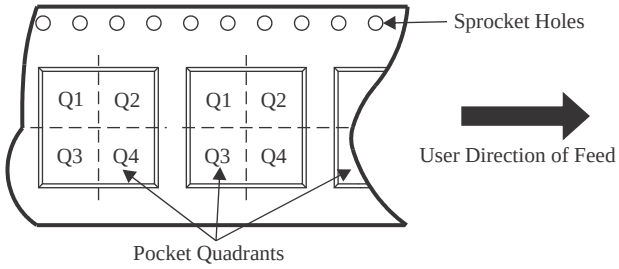



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

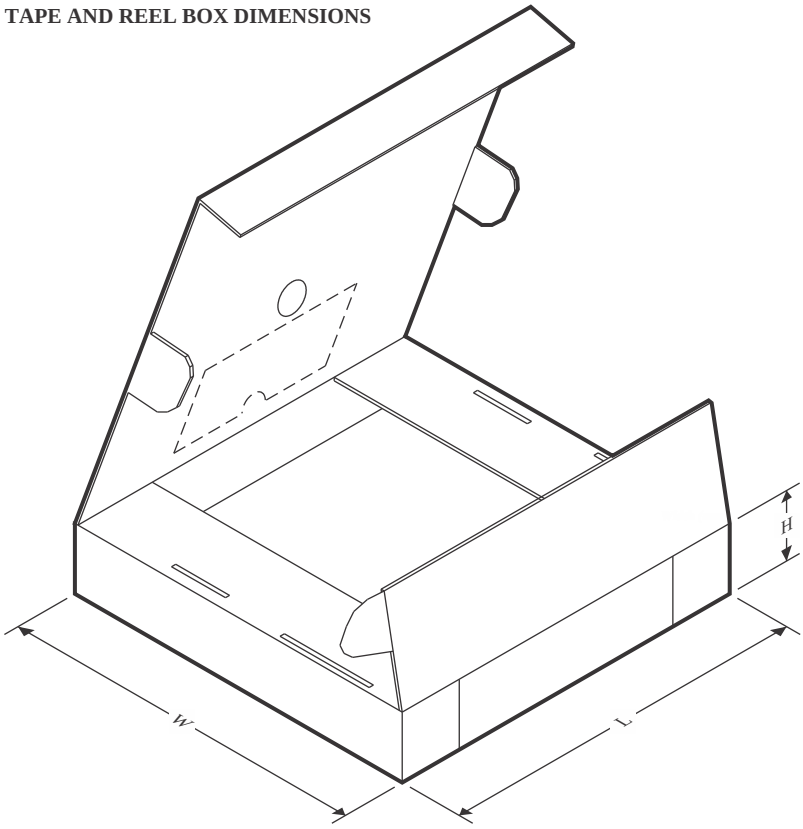
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS61176RTER | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TPS61176RTERG4 | WQFN | RTE | 16 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS61176RTER | WQFN | RTE | 16 | 3000 | 335.0 | 335.0 | 25.0 |
| TPS61176RTERG4 | WQFN | RTE | 16 | 3000 | 335.0 | 335.0 | 25.0 |

# GENERIC PACKAGE VIEW

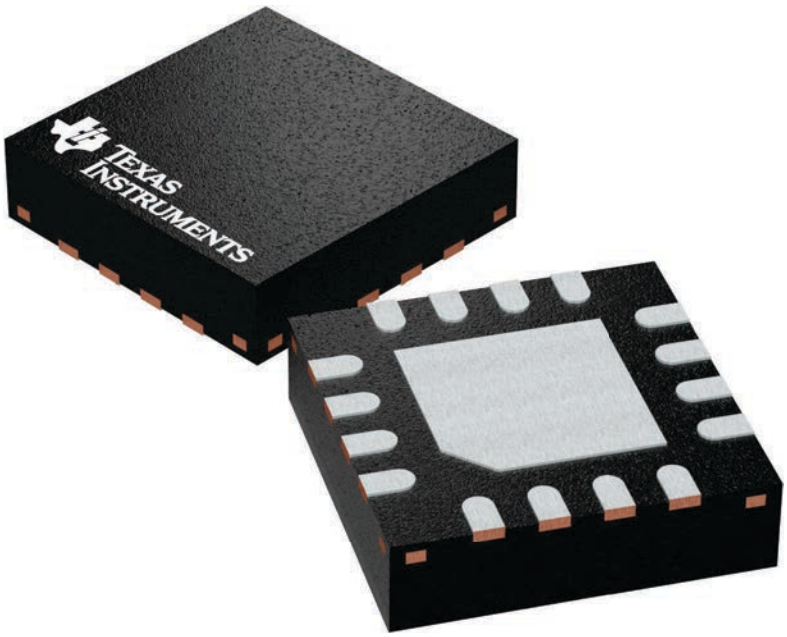
## RTE 16

## WQFN - 0.8 mm max height

**3 x 3, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



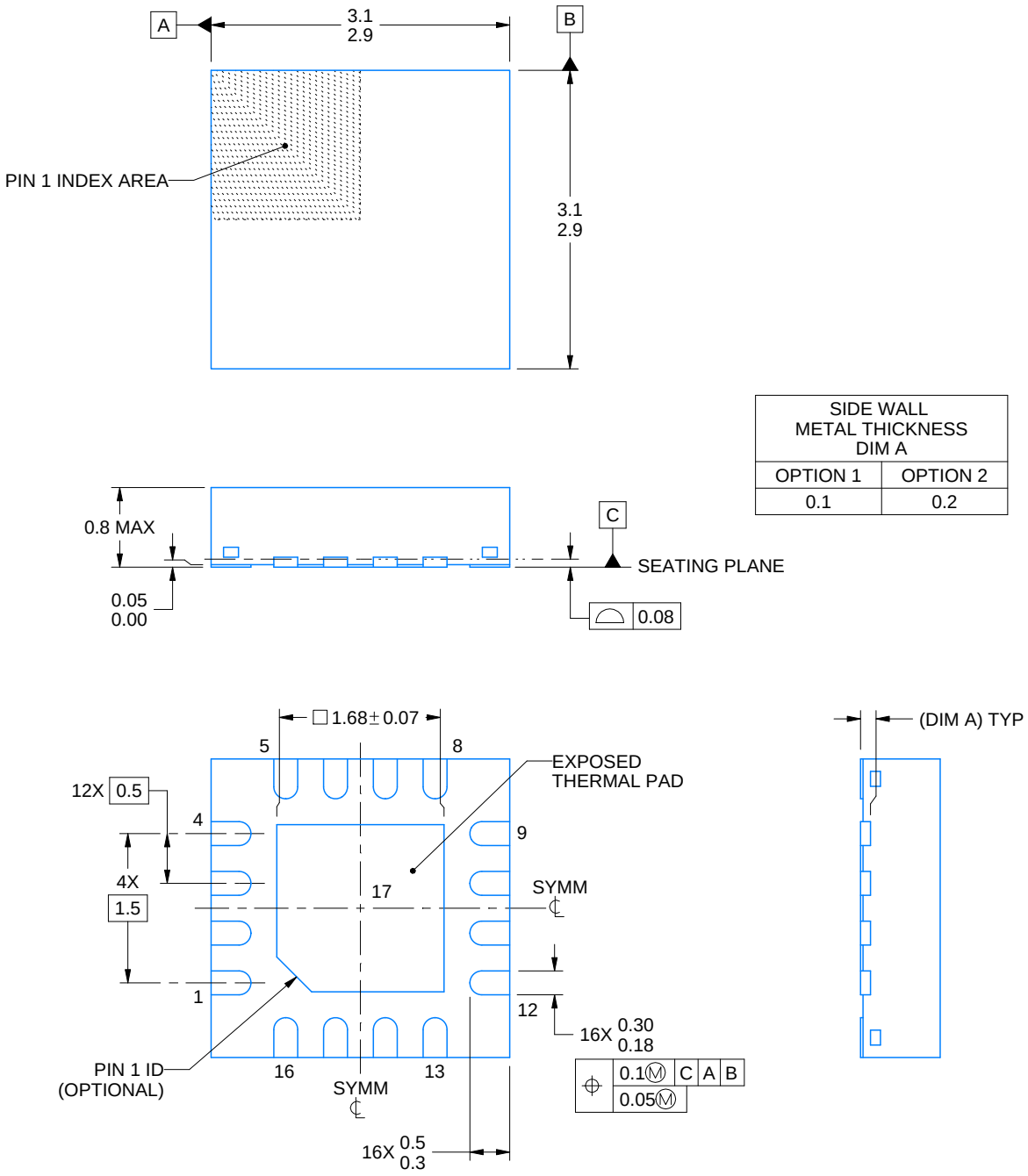

4225944/A

# RTE0016C

# PACKAGE OUTLINE

## WQFN - 0.8 mm max height

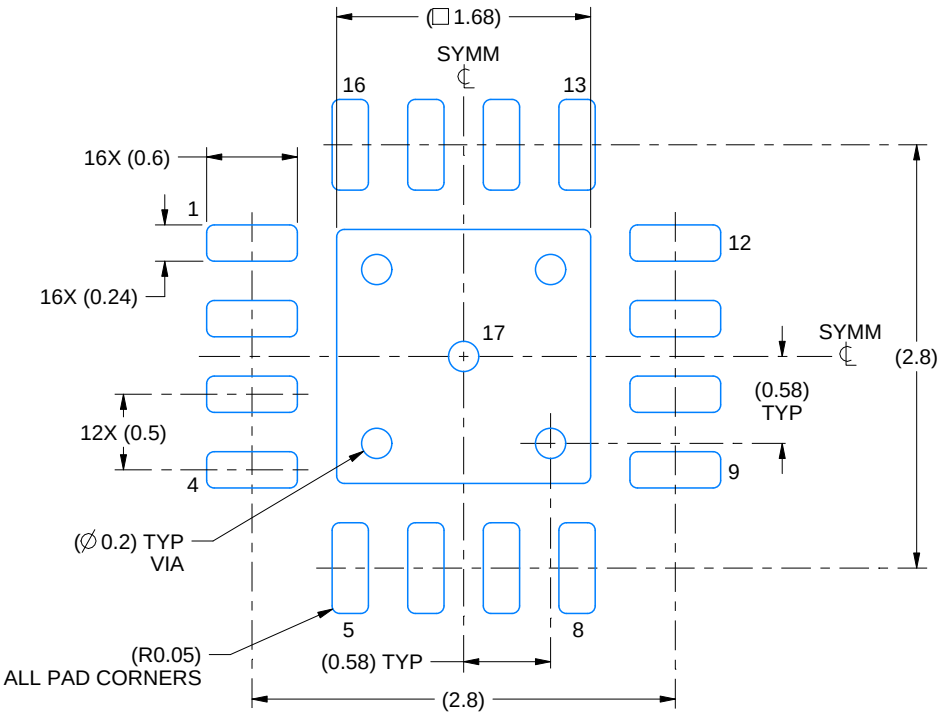
PLASTIC QUAD FLATPACK - NO LEAD



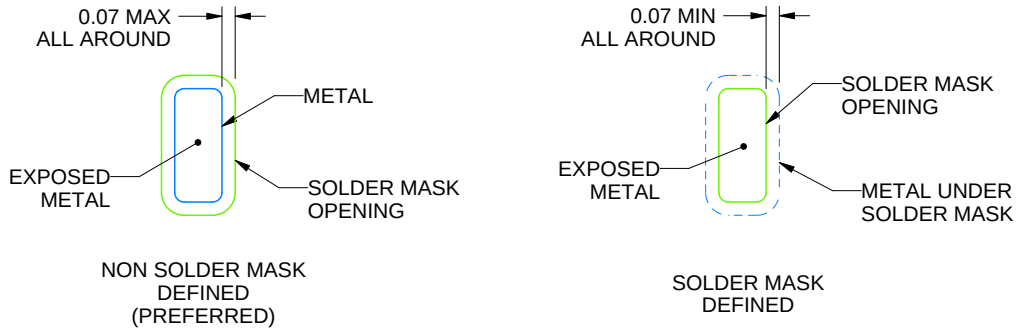

4219117/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X




SOLDER MASK DETAILS

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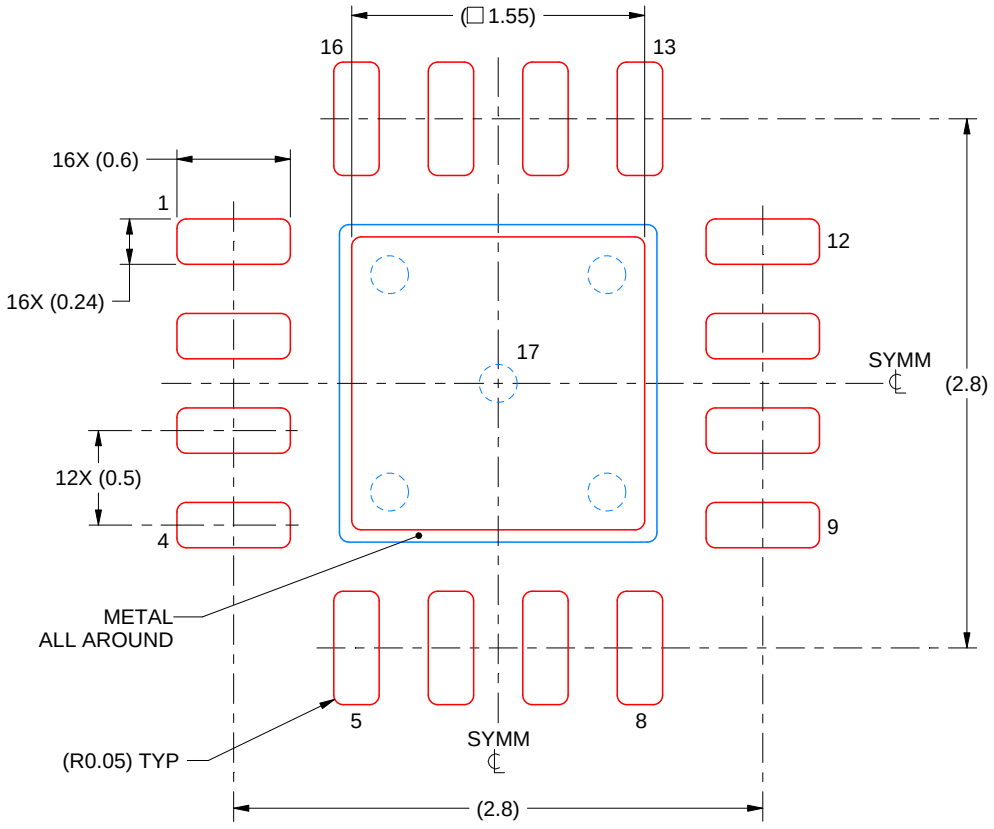
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月