带有集成功率二极管的白光发光二极管 (WLED) 驱动器

查询样品: TPS61158

特性

- **2.7V** 至 **5.5V** 输入电压范围
- **28V LED** 开路保护（多达 **8** 个 **LED**）
- 集成 **0.6A 30V** 内部开关场效应晶体管 **(FET)** 和功率二极管
- **750kHz** 开关频率
- 灵活的数字和脉宽调制 **(PWM)** 亮度控制
  - **1** 线制控制接口 **(EasyScale)**
  - **PWM** 亮度调节控制接口
- 高达 **100:1 PWM** 调光比
- 集成环路补偿
- 内置软起动
- 内置 **WLED** 开路保护
- 热关断
- 带有散热垫的 **2mm x 2mm x 0.8mm 6** 引脚四方扁平无引线 **(QFN)** 封装

应用范围

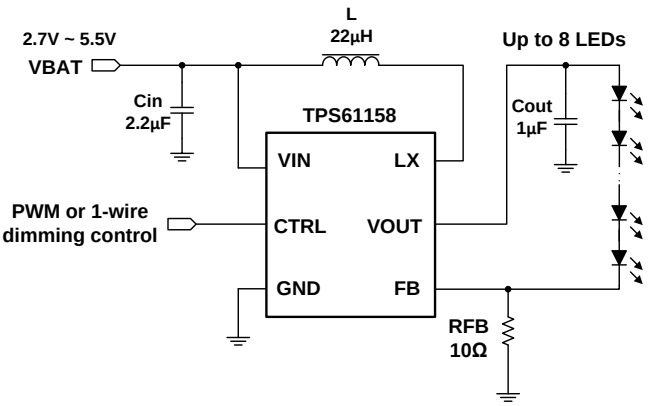
- 功能型手机
- 智能电话
- 便携式媒体播放器
- 超移动器件
- **GPS** 接收器
- 用于小型和媒体外形设计的 **LCD** 显示器的背光源

说明

借助额定电压为 30V 的集成开关 FET 和功率二极管，TPS61158 成为一个可驱动串联 LED 的升压转换器。 升压转换器以 750kHz 的固定开关频率运行，以降低输出波纹、提高转换效率并可用于小型外部组件。

如典型应用所示，缺省白光 LED 电流由外部传感器电阻器 RFB 设定，并且此反馈电压被调节至 200mV。运行期间，可由 CTRL 引脚上的 1 线制数字接口（Easyscale™ 协议）来控制 LED 电流。 或者，可将一个 PWM 信号施加到 CTRL 引脚上，占空比通过这个引脚确定反馈基准电压。 在数字或者 PWM 模式下，TPS61158 并不会突发 LED 电流；因此，它不会在输出电容器上生成可闻噪音。 为了大大增加保护能力，此器件特有集成的 LED 开路保护功能，此功能可在 LED 开路情况下关闭禁用 TPS61158，以防止输出电压超过集成电路 (IC) 的绝对最大电压额定值。TPS61158 采用节省空间的、带有散热垫的 2mm x 2mm QFN 封装。

典型应用



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

ORDERING	PACKAGE	PACKAGE MARKING
TPS61158DRV	QFN 2 x 2 6L - DRV	SIW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage range(2)	VIN	–0.3	6	V
	VOUT, LX	–0.3	30	V
	FB, CTRL	–0.3	7	V
ESD rating	HBM		2	kV
	CDM		500	V
Continuous power dissipation		See Thermal Information Table		
Operating junction temperature range		–40	150	°C
Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS61158	UNITS
		DRV (6 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance(2)	70.4	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	94.8	
θ_{JB}	Junction-to-board thermal resistance(4)	39.8	
ψ_{JT}	Junction-to-top characterization parameter(5)	2.5	
ψ_{JB}	Junction-to-board characterization parameter(6)	40.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	10.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.7		5.5	V
V_{OUT}	Output voltage range	Vin		29	V
I_{OUT}	Output load current			30	mA
L	Inductor	10		22	µH
C_I	Input capacitor	1.0		10	µF
C_O	Output capacitor	0.47		2.2	µF
F_{PWM}	Input PWM signal frequency range	20		100	kHz
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{IN}=3.6V, CTRL=High, IFB current=20mA, IFB voltage=200mV, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		5.5	V
V_{IN_UVLO}	V_{IN} under voltage lockout threshold	V_{IN} ramp down		2.2	2.35	V
		V_{IN} ramp up		2.5	2.65	
V_{IN_HYS}	V_{IN} under voltage lockout hysteresis			275		mV
I_Q	Operating quiescent current into VIN	Device enable, no switching and no load (V_{FB} = 0.4V)		0.3	0.5	mA
		Device enable, switching 750kHz and no load (V_{FB} = 0V)		0.5	1.65	
I_{SD}	Shutdown current	CTRL = GND		0.1	1	µA
CONTROL LOGIC AND TIMING						
V_H	CTRL logic high voltage		1.2			V
V_L	CTRL logic Low voltage				0.4	V
R_{PD}	CTRL pin internal pull-down resistor	V_{CTRL} = 1.8 V		300		kΩ
t_{SD}	CTRL pulse width to shutdown	CTRL from high to low	3.5			ms
VOLTAGE AND CURRENT REGULATION						
V_{REF}	Voltage feedback regulation voltage	Duty = 100%	194	200	206	mV
I_{FB}	FB pin bias current	V_{FB} = 200mV			2	µA
t_{REF}	V_{REF} filter time constant			230		µs
POWER SWITCH AND DIODE						
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = 3.6 V, T_A = 25°C, I_{OUT} = 100 mA		0.6	1	Ω
V_F	Power diode forward voltage	I_{DIODE} = 0.2A		0.75	1	V
I_{LEAK_LX}	LX pin leakage current	V_{LX} = 28V		0.1	2	µA
OSCILLATOR						
f_{SW}	Oscillator frequency		600	750	900	kHz
D_{max}	Maximum duty cycle of boost switching	V_{FB} = 0V, measured on the drive signal of the switch MOSFET	88%	94%		
PROTECTION AND SOFTSTART						
I_{LIM}	NMOS current limit	V_{IN} = 3.6V, D = D_{MAX}, T_A = 0°C to 85°C,	0.5	0.6	0.7	A
I_{LIM_Start}	Start up current limit			360		mA
t_{ILIM_Start}	Time step for start up current limit			8		ms
V_{OVP}	Open LED protection threshold	Tested at VOUT pin	27.5	28.2	29	V

ELECTRICAL CHARACTERISTICS (continued)

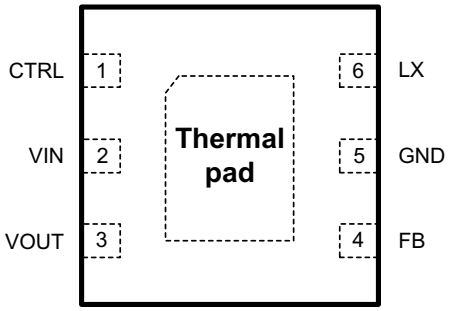
V_{IN}=3.6V, CTRL=High, IFB current=20mA, IFB voltage=200mV, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EasyScale TIMING						
t_{es_detect}	Easy Scale detection time(1)	CTRL low	450			µs
t_{es_delay}	Easy Scale detection delay		100			µs
t_{es_win}	Easy Scale detection window time	Measured from CTRL high	3.5			ms
t_{start}	Start time of program stream		3.5			µs
t_{EOS}	End time of program stream		3.5		600	µs
t_{H_LB}	High time of low bit	Logic 0	3.5		300	µs
t_{L_LB}	Low time of low bit	Logic 0	2 x t_{H_LB}		600	µs
t_{H_HB}	High time of high bit	Logic 1	2 x t_{L_HB}		600	µs
t_{L_HB}	Low time of high bit	Logic 1	3.5		300	µs
V_{ACKNL}	Acknowledge output voltage low	Open drain, R_{pullup} = 15kΩ to VIN			0.4	V
t_{valACK}	Acknowledge valid time	See(2)			3.5	µs
t_{ACKN}	Duration of acknowledge condition	See(2)			900	µs
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown hysteresis			15		°C

(1) To select EasyScale mode, the CTRL pin has to be low for more than t_{es_detect} during t_{es_win}
(2) Acknowledge condition active 0, this condition will only be applied in case the RFA bit is set. Open drain output, line needs to be pulled high by the host with resistor load.

DEVICE INFORMATION

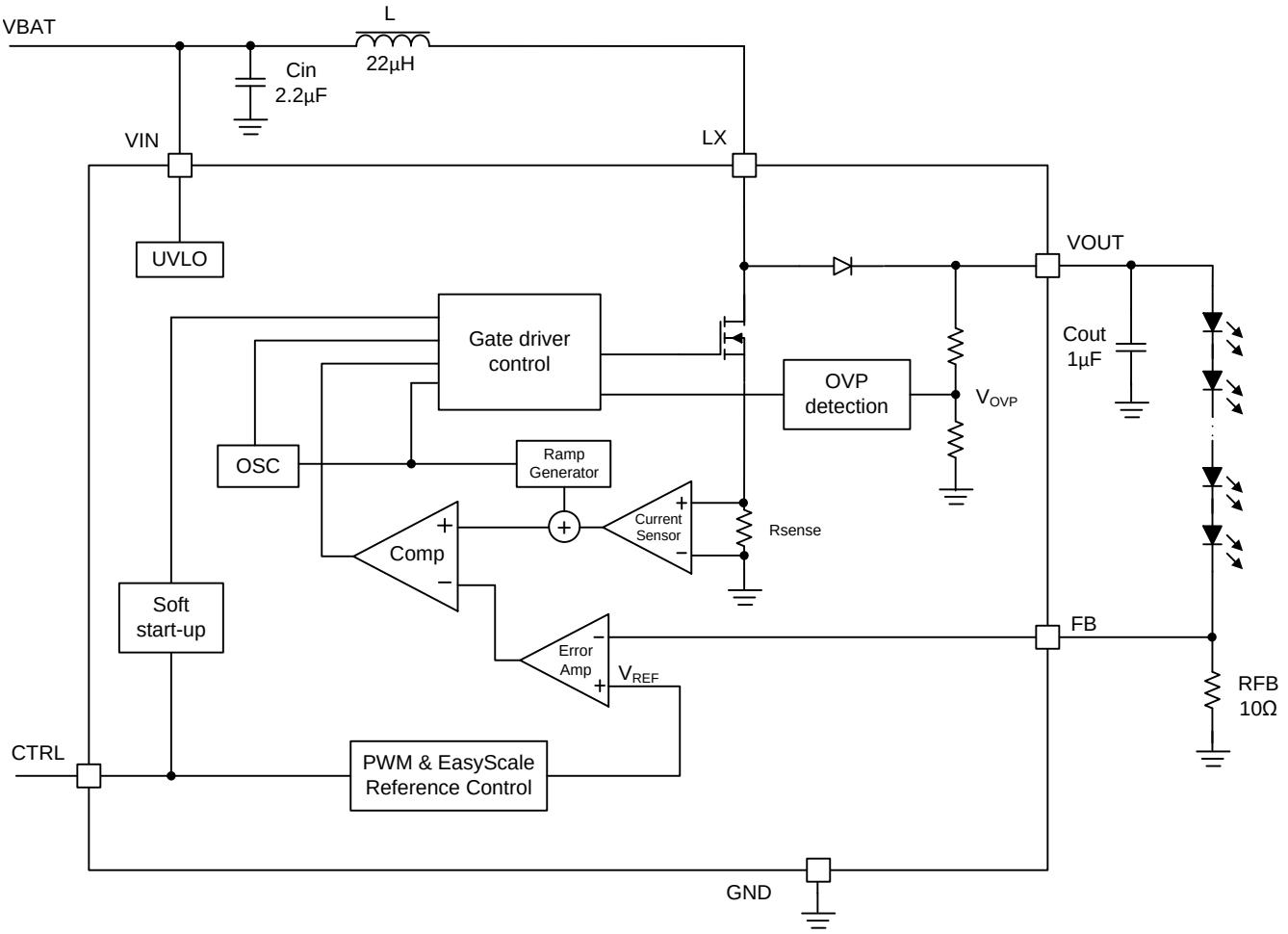
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CTRL	I	Control pin of the boost converter. It is a multi-functional pin which can be used for enable control, PWM and digital dimming.
2	VIN	I	The input supply pin for the IC. Connect VIN to a supply voltage between 2.7V and 5.5V.
3	VOUT	O	Output of the boost converter.
4	FB	I	Feedback pin for current. Connect the sense resistor from FB to GND.
5	GND	O	Ground
6	LX	I	This is the switching node of the IC. Connect the inductor between the VIN and LX pin.
7	Thermal Pad		The thermal pad should be soldered to the analog ground plane. If possible, use thermal via to connect to ground plane for ideal power dissipation.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

TITLE	DESCRIPTION	FIGURE
Dimming Efficiency	V_{IN} = 3.6V; 6 LEDs (V_{OUT} = 18.3V), 8 LEDs (V_{OUT} = 24.4V); R_{FB} = 10Ohm; PWM Freq = 40kHz; L = 22µH	Figure 1
Dimming Efficiency	V_{IN} = 3V, 3.6V, 4.2V, 5V; 6 LEDs (V_{OUT} = 18.3V); R_{FB} = 10Ohm; PWM Freq = 40kHz; L = 22µH	Figure 2
Dimming Efficiency	V_{IN} = 3V, 3.6V, 4.2V, 5V; 8 LEDs (V_{OUT} = 24.4V); R_{FB} = 10Ohm; PWM Freq = 40kHz; L = 22µH	Figure 3
Switch Current Limit vs Temperature	V_{IN} = 3.6V	Figure 4
Switch Current Limit vs VIN	T_A = 25°C	Figure 5
FB Voltage vs EasyScale Step	V_{IN} = 3.6V	Figure 6
FB voltage vs PWM duty cycle	V_{IN} = 3.6V; PWM Freq = 20kHz and 40kHz	Figure 7
Output Ripple at PWM Dimming	V_{IN} = 3.6V; 8 LEDs (V_{OUT} = 24.4V); R_{FB} = 10Ohm; PWM Freq = 20kHz; L = 22µH	Figure 8
Switching Waveform	V_{IN} = 3.6V; 8 LEDs (V_{OUT} = 24.4V); R_{FB} = 10Ohm; PWM Duty = 100%; L = 22µH	Figure 9
Switching Waveform	V_{IN} = 3.6V; 8 LEDs (V_{OUT} = 24.4V); R_{FB} = 10Ohm; PWM Freq = 20kHz; PWM Duty = 25%; L = 22µH	Figure 10
Startup Waveform	V_{IN} = 3.6V; 8 LEDs (V_{OUT} = 24.4V); R_{FB} = 10Ohm; PWM Duty = 100%; L = 22µH	Figure 11
Startup Waveform	V_{IN} = 3.6V; 8 LEDs (V_{OUT} = 24.4V); R_{FB} = 10Ohm; PWM Freq = 20kHz; PWM Duty = 25%; L = 22µH	Figure 12
Shutdown Waveform	V_{IN} = 3.6V; 8 LEDs (V_{OUT} = 24.4V); R_{FB} = 10Ohm; PWM Duty = 100%; L = 22µH	Figure 13
Shutdown Waveform	V_{IN} = 3.6V; 8 LEDs (V_{OUT} = 24.4V); R_{FB} = 10Ohm; PWM Freq = 20kHz; PWM Duty = 25%; L = 22µH	Figure 14
Open LED Protection	V_{IN} = 3.6V; 6 LEDs (V_{OUT} = 18.3V); R_{FB} = 10Ohm; PWM Duty = 100%; L = 22µH	Figure 15

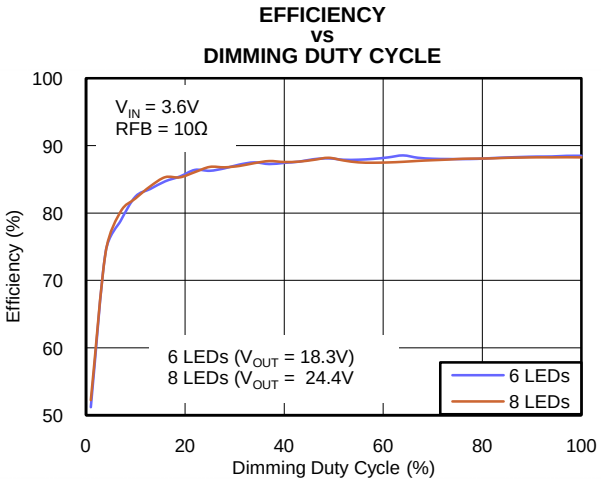


Figure 1.

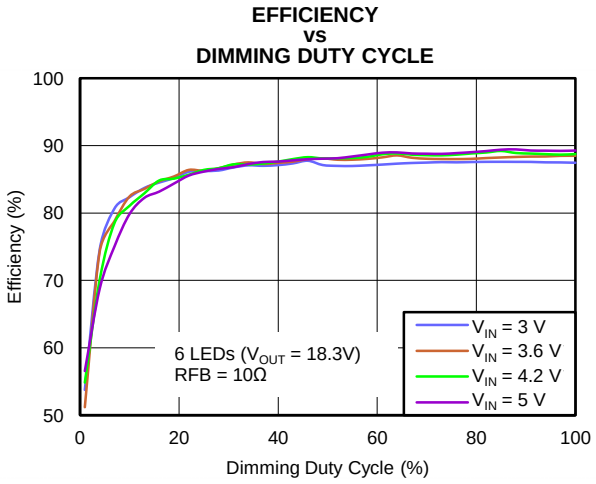


Figure 2.

EFFICIENCY vs DIMMING DUTY CYCLE

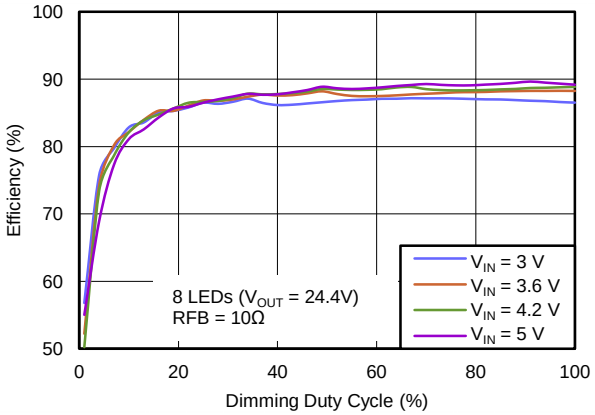


Figure 3.

SWITCH CURRENT LIMIT vs DUTY CYCLE

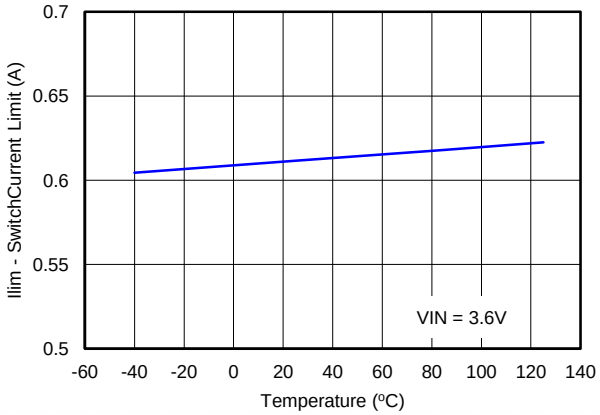


Figure 4.

SWITCH CURRENT LIMIT vs TEMPERATURE

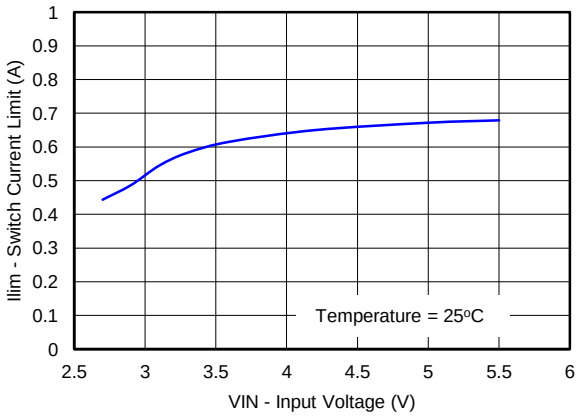


Figure 5.

FB VOLTAGE vs EASYSCALE STEP

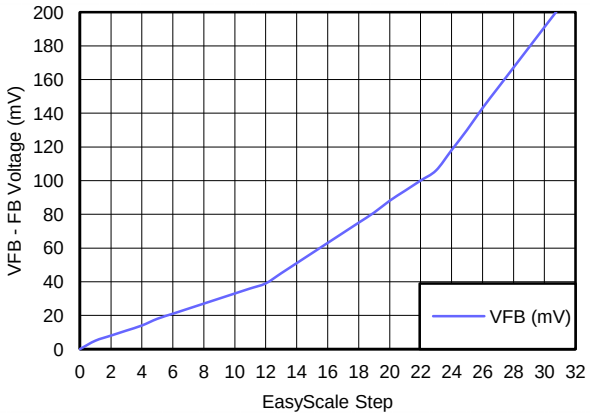


Figure 6.

FB VOLTAGE vs DIMMING DUTY CYCLE

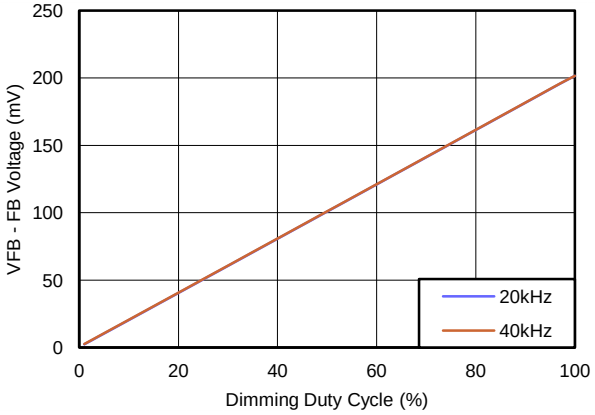


Figure 7.

OUTPUT RIPPLE at PWM DIMMING

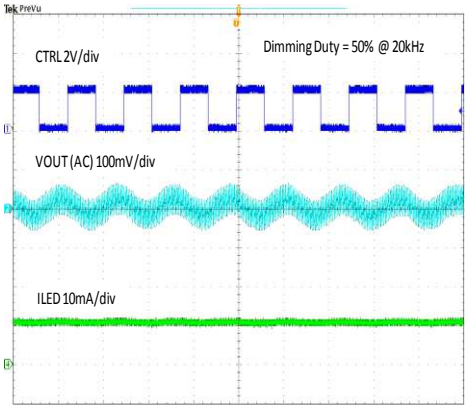


Figure 8.

SWITCHING WAVEFORM - DIMMING DUTY = 100%

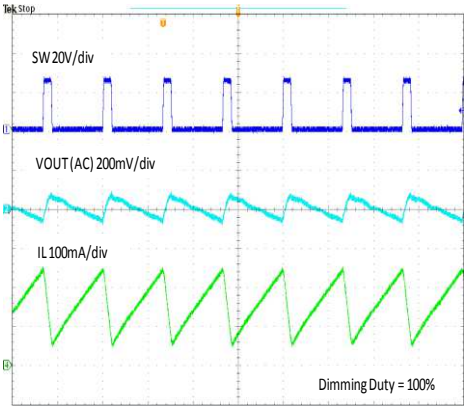


Figure 9.

SWITCHING WAVEFORM - DIMMING DUTY = 25%

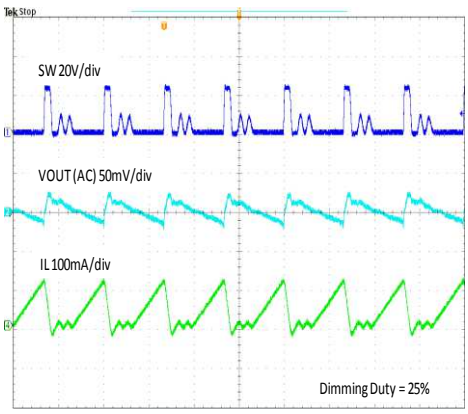


Figure 10.

START-UP DIMMING DUTY = 100%

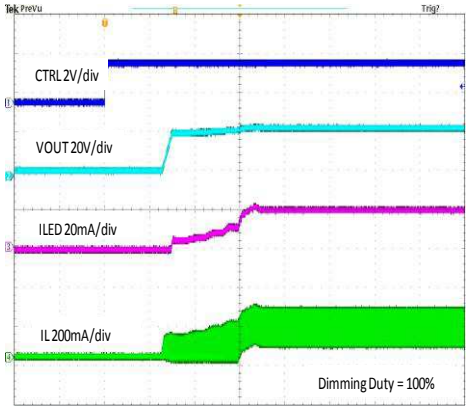


Figure 11.

START-UP DIMMING DUTY = 25%

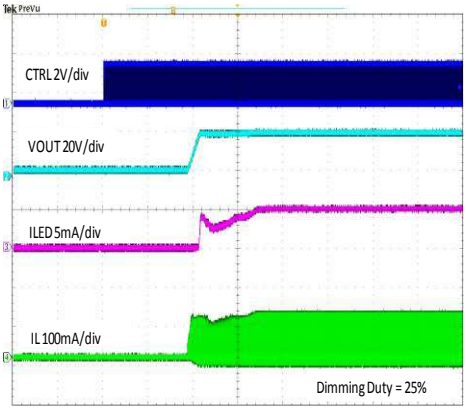


Figure 12.

SHUTDOWN DIMMING DUTY = 100%

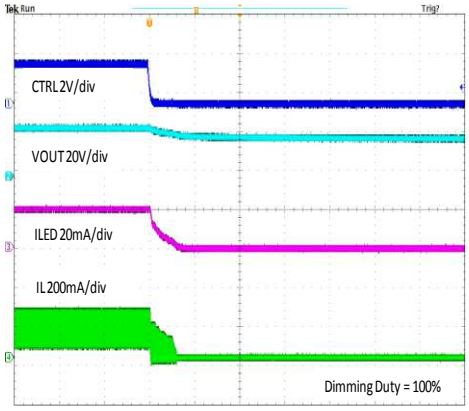


Figure 13.

SHUTDOWN DIMMING DUTY = 25%

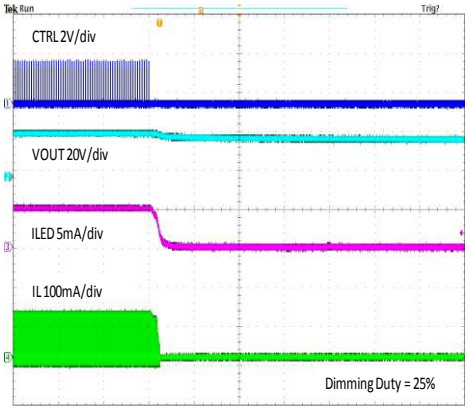


Figure 14.

OPEN LED PROTECTION

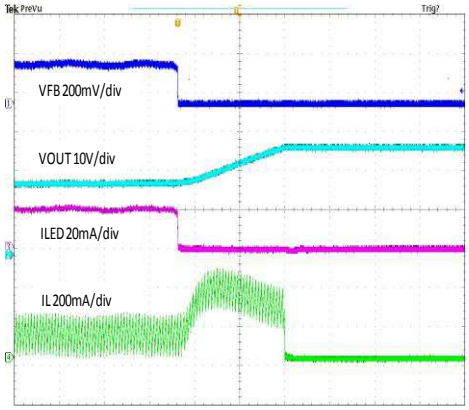


Figure 15.

DETAILED DESCRIPTION

OPERATION

The TPS61158 is a high efficiency boost converter with integrated power diode in a small package size. The device is ideal for driving white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates a 30V/0.6A low side switch MOSFET and a 30V power diode, and operates in pulse width modulation (PWM) with 750 kHz fixed switching frequency. For operation see the block diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control; therefore, slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%. The feedback loop regulates the FB pin to a low reference voltage (200mV typical), reducing the power dissipation in the current sense resistor.

SOFT START-UP

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps with each step taking 341µs. This ensures that the output voltage rises slowly to reduce the input current. Additionally, during the start up process, the current limit of the switch is set to half of the normal current limit spec. During this period, the input current is kept below 360mA (typical). See the start-up waveform of a typical example.

SHUTDOWN

The TPS61158 enters shutdown mode when the CTRL voltage is logic low for more than 3.5ms. During shutdown, the input supply current for the device is less than 1µA (max). Although the internal FET does not switch in shutdown mode, there is still a DC current path between the input and the LEDs through the inductor and the power diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. In the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the diode and keep leakage current low.

CURRENT PROGRAM

The FB voltage is regulated by a low 0.2V reference voltage. The LED current is programmed externally using a current-sense resistor RFB in series with the LED string. The value of the RFB is calculated using Equation 1:

$$R_{FB} = \frac{V_{FB}}{I_{LED}} \quad (1)$$

Where:

R_{FB} = current sense resistor at FB pin
V_{FB} = 200mV (regulated voltage of FB pin)
I_{LED} = full-scale output current of LEDs
The output current tolerance depends on the FB voltage accuracy and the current sensor resistor accuracy.

LED BRIGHTNESS DIMMING MODE SELECTION

The CTRL pin is used for the control input for both dimming modes, PWM dimming and 1 wire dimming. The dimming mode for the TPS61158 is selected each time the device is enabled. The default dimming mode is PWM dimming. To enter the 1 wire mode, the following digital pattern on the CTRL pin must be recognized by the IC every time the IC starts from the shutdown mode.

1. Pull CTRL pin high to enable the TPS61158, and to start the 1 wire detection window.
2. After the EasyScale detection delay (t_{es_delay}, 100µs) expires, drive CTRL low for more than the EasyScale detection time (t_{es_detect}, 450µs).
3. The CTRL pin has to be low for more than EasyScale detection time before the EasyScale detection window (t_{es_win}, 3.5ms) expires. EasyScale detection window starts from the first CTRL pin low to high transition.

The IC immediately enters the 1 wire mode once the above 3 conditions are met. The EasyScale communication can start before the detection window expires. Once the dimming mode is programmed, it can not be changed without another start up. This means the IC needs to be shutdown by pulling the CTRL low for 3.5ms and restarts. See the Dimming Mode Detection and Soft Start (Figure 16) for a graphical explanation.

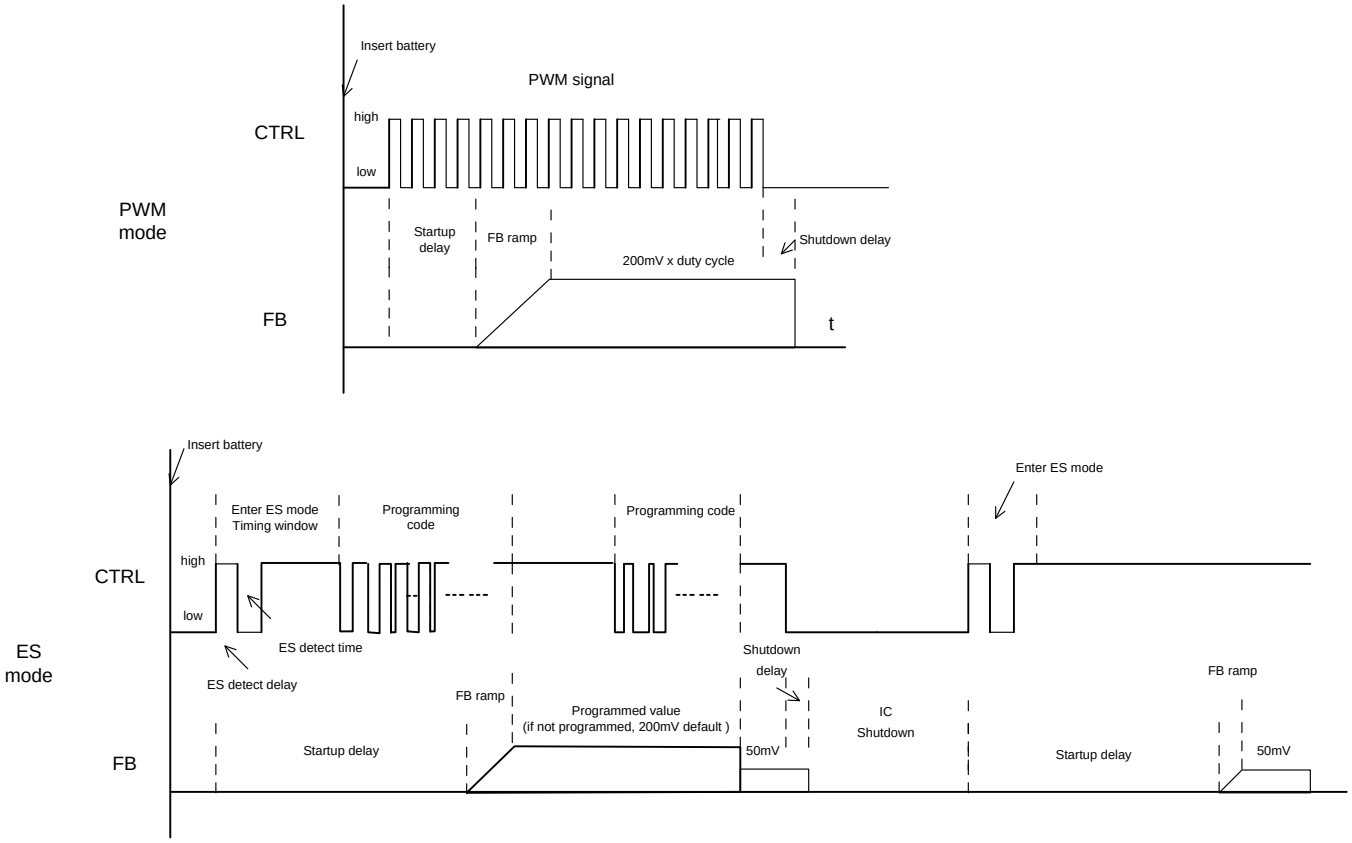


Figure 16. Dimming Mode Detection and Soft Start

PWM BRIGHTNESS DIMMING

When the CTRL pin is constantly high, the FB voltage is regulated to 200mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB voltage is given by Equation 2.

$$V_{FB} = \text{Duty} \times 200\ \text{mV} \quad (2)$$

Where:

Duty = duty cycle of the PWM signal
200 mV = internal reference voltage

As shown in Figure 17, the IC chops up the internal 200mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, TPS61158 regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 20kHz to 100kHz. Since the CTRL pin is logic only pin, adding an external RC filter applied to the pin does not work.

The minimum dimming duty cycle the IC can support is 1% within the PWM dimming frequency range 20kHz~100kHz.

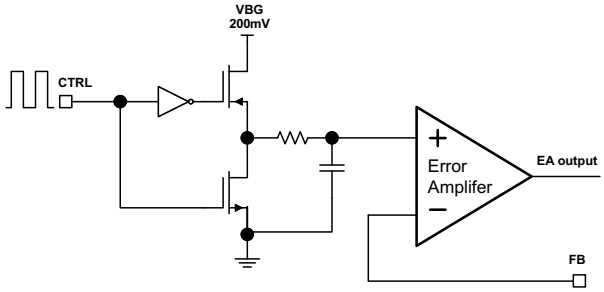


Figure 17. Block Diagram of Programmable FB Voltage Using PWM Signal

DIGITAL 1 WIRE BRIGHTNESS DIMMING

The CTRL pin features a simple digital interface to allow digital brightness control. The digital dimming can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The TPS61158 adopts the EasyScale™ protocol for the digital dimming, which can program the FB voltage to any of the 32 steps with single command. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See the Table 1 for the FB pin voltage steps. The default step is full scale when the device is first enabled (V_{FB} = 200mV). The programmed reference voltage is stored in an internal register. A power reset clears the register value and reset it to default.

EasyScale™: 1 WIRE DIGITAL DIMMING

EasyScale is a simple but flexible one pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. Figure 18 and Table 2 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 58 hex. The data byte consists of five bits for information, two address bits ("00"), and the RFA bit. The RFA bit set to high indicates the Request for Acknowledge condition. The Acknowledge condition is only applied if the protocol was received correctly. The advantage of EasyScale compared with other one pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.1kBit/sec and up to 100kBit/sec.

Table 1. Selectable FB Voltage

	FB VOLTAGE (mV)	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	5	0	0	0	0	1
2	8	0	0	0	1	0
3	11	0	0	0	1	1
4	14	0	0	1	0	0
5	17	0	0	1	0	1
6	20	0	0	1	1	0
7	23	0	0	1	1	1
8	26	0	1	0	0	0
9	29	0	1	0	0	1
10	32	0	1	0	1	0
11	35	0	1	0	1	1
12	38	0	1	1	0	0
13	44	0	1	1	0	1
14	50	0	1	1	1	0
15	56	0	1	1	1	1
16	62	1	0	0	0	0
17	68	1	0	0	0	1
18	74	1	0	0	1	0
19	80	1	0	0	1	1
20	86	1	0	1	0	0
21	92	1	0	1	0	1
22	98	1	0	1	1	0
23	104	1	0	1	1	1
24	116	1	1	0	0	0
25	128	1	1	0	0	1
26	140	1	1	0	1	0
27	152	1	1	0	1	1
28	164	1	1	1	0	0
29	176	1	1	1	0	1
30	188	1	1	1	1	0
31	200	1	1	1	1	1

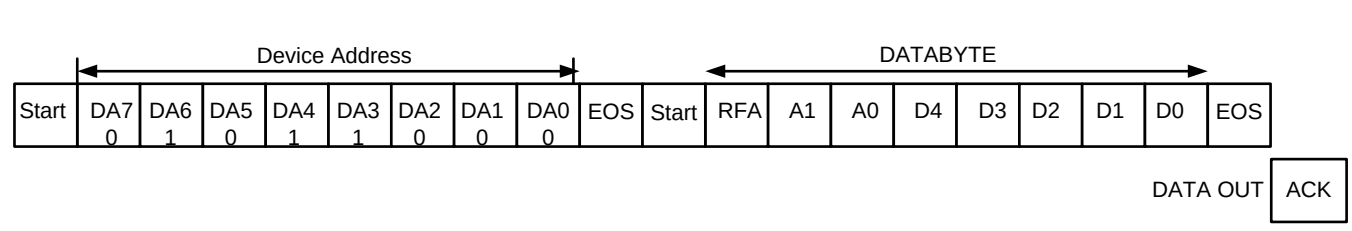


Figure 18. EasyScale™ Protocol Overview

Table 2. EasyScale™ Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte 72 hex	7	DA7	IN	0 (MSB device address)
	6	DA6		1
	5	DA5		0
	4	DA4		1
	3	DA3		1
	2	DA2		0
	1	DA1		0
	0	DA0		0 (LSB device address)
Data byte	7 (MSB)	RFA	IN	Request for acknowledge. If high, acknowledge is applied by device.
	6	A1		0 (Address bit A1)
	5	A0		0 (Address bit A0)
	4	D4		Data bit D4
	3	D3		Data bit D3
	2	D2		Data bit D2
	1	D1		Data bit D1
	0 (LSB)	D0		Data bit D0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied to case RFA bit is set. Open drain output, line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open drain output stage. In case of a push pull output stage Acknowledge condition may not be requested!

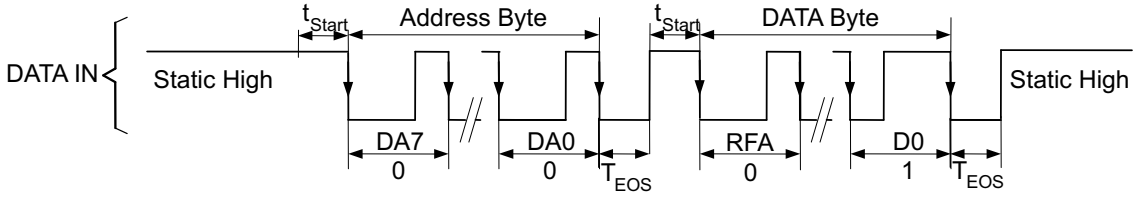


Figure 19. Easy Scale Timing, without acknowledge (RFA = 0)

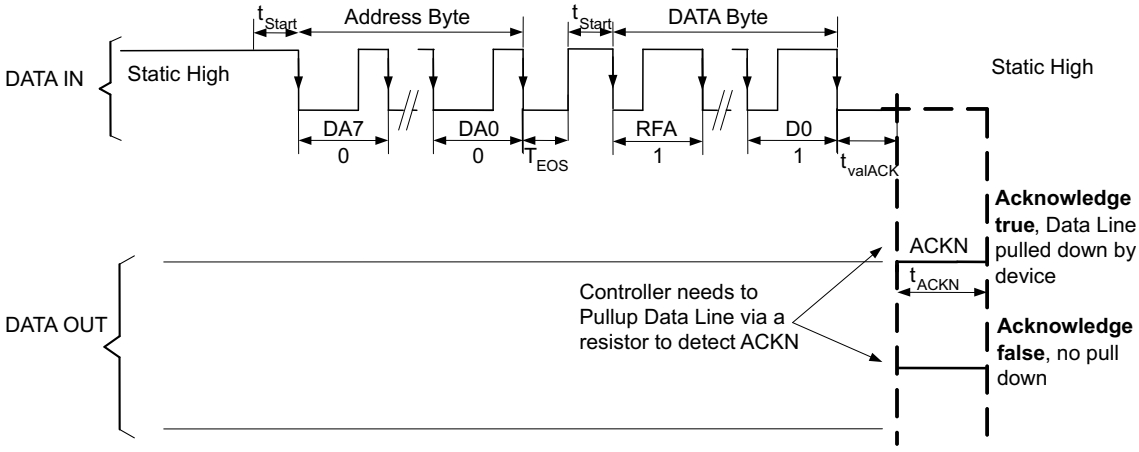


Figure 20. Easy Scale Timing, with acknowledge (RFA = 1)

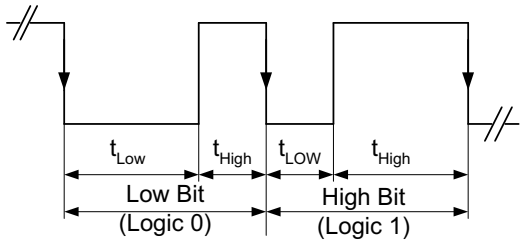


Figure 21. EasyScale™— Bit Coding

All bits are transmitted MSB first and LSB last. Figure 19 shows the protocol without acknowledge request (Bit RFA = 0), Figure 20 with acknowledge (Bit RFA = 1) request. Prior to both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least t_{start} (3.5µs) before the bit transmission starts with the falling edge. If the CTRL pin is already at high level, no start condition is needed prior to the device address byte. The transmission of each byte is closed with an End of Stream condition for at least t_{EOS} (3.5µs).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH} (refer to Figure 21). It can be simplified to:

- Low Bit (Logic 0): $t_{LOW} \geq 2 \times t_{HIGH}$
- High Bit (Logic 1): $t_{HIGH} \geq 2 \times t_{LOW}$

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by setting RFA bit to 1.
- The transmitted device address matches with the device address of the IC
- Device address byte and data byte are received correctly.

If above conditions are met, after t_{valACK} (3.5µs) delay from the moment when the last falling edge of the protocol is detected, an internal ACKN-MOSFET is turned on to pull the CTRL pin low for the time t_{ACKN} (900µs maximum), then the Acknowledge condition is valid. During the t_{valACK} delay, the master controller keeps the line low; after the delay, it should release the line by outputting high impedance and then detect the acknowledge condition. If it reads back a logic 0, it means the IC has received the command correctly. The CTRL pin can be used again by the master when the acknowledge condition ends after t_{ACKN} time.

Note that the acknowledge condition can only be requested in case the master device has an open drain output. For a push-pull output stage, the use a series resistor in the CTRL line to limit the current to 500µA is recommended to for such cases as:

- an accidentally requested acknowledge, or
- to protect the internal ACKN-MOSFET.

UNDERVOLTAGE LOCKOUT

An undervoltage lockout prevents operation of the device at input voltages below typical 2.2V. When the input voltage is below the undervoltage threshold, the device is shutdown and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

OPEN LED PROTECTION

Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The TPS61158 monitors the voltages at the VOUT pin and FB pin. The circuitry turns off the switch FET and shuts down the IC completely if both of the following two conditions are met: 1) the VOUT voltage reaches OVP threshold (28.2V typical), 2) FB voltage is lower than half of its regulation voltage. This means the LED string is open or the FB pin is short to ground. As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by pulling down the CTRL pin logic low for at least 3.5ms and then pulling it high.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

APPLICATION INFORMATION

MAXIMUM OUTPUT CURRENT

The overcurrent limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_P = \frac{1}{L \times F_S \times \left(\frac{1}{V_{OUT} + V_F - V_{IN}} + \frac{1}{V_{IN}}\right)} \quad (3)$$

Where

I_P = inductor peak to peak ripple
L = inductor value
F_S = switching frequency
V_{OUT} = output voltage of the boost converter. It is equal to the sum of V_{FB} and the voltage drop across LEDs.
V_F = forward voltage of internal power diode. 0.75V typical

$$I_{OUT\_max} = \frac{V_{IN} \times (I_{LIM} - I_P / 2) \times \eta}{V_{OUT}} \quad (4)$$

Where

I_{OUT_max} = maximum output current of the boost converter
I_{LIM} = over current limit
η = boost efficiency (85%, typical)

To calculate the maximum output current in the worst case, use the minimum input voltage, maximum output voltage and maximum forward voltage of internal power diode (1V). In order to leave enough design margin, the minimum current limit value 0.5A, the minimum switching frequency 600kHz, the inductor value with -30% tolerance, and a low power conversion efficiency, such as 80% or lower are recommended for the calculation. For instance, when minimum VIN is 3.0V, 8 LEDs output equivalent to VOUT is 26V, the inductor is 22uH, then the maximum output current is 33mA in the worst case.

INDUCTOR SELECTION

The selection of the inductor affects steady state operation as well as transient behavior, loop stability and the power conversion efficiency. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough. The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by Equation 3, plus the inductor DC current given by:

$$I_{in\_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (5)$$

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. When selecting an inductor, please make sure its rated current, especially the saturation current, is larger than its peak current during the operation. Using an inductor with a smaller inductance value causes larger current ripple. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a 10µH to 22µH inductor value range is recommended. A 22µH inductor optimizes the efficiency for most application while maintaining low inductor peak to peak ripple. Table 3 lists the recommended inductors for TPS61158. TPS61158 has built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is lower than 10µH, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers need to verify the inductor in their application if it is different from the recommended values.

Table 3. Recommended Inductors

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	Size (L x W x H mm)	VENDOR
LPS3015-103ML	10	440	0.73	3.0 x 3.0 x 1.5	Coilcraft
LPS3015-223ML	22	825	0.5	3.0 x 3.0 x 1.5	Coilcraft
1229AS-H-100M	10	288	0.75	3.5 x 3.7 x 1.2	TOKO
1229AS-H-220M	22	672	0.5	3.5 x 3.7 x 1.2	TOKO
VLS3012ET-100M	10	336	0.64	3.0 x 3.0 x 1.2	TDK
VLS3012ET-220M	22	756	0.44	3.0 x 3.0 x 1.2	TDK

INPUT AND OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by

$$C_{OUT} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times V_{ripple}} \quad (6)$$

Where: Vripple = peak-to-peak output ripple. The additional output ripple component caused by ESR is calculated using:

$$V_{ripple\_ESR} = I_{OUT} \times R_{ESR} \quad (7)$$

Due to its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under DC bias, aging and AC signal. The DC bias can significantly reduce capacitance. Ceramic capacitors can lose as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

The capacitor in the range of 1µF to 10µF is recommended for input side. The output requires a capacitor in the range of 0.47µF to 2.2µF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

LAYOUT CONSIDERATION

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. Therefore, use wide and short traces for high current paths. The input capacitor Cin needs to be close to the VIN pin and GND pin in order to reduce the input ripple seen by the IC. If possible, choose higher capacitance value for it. If the ripple seen at VIN pin is so large that it affects the boost loop stability or internal circuits operation, R1 and C1 is recommended to compose a filter to decouple the noise (refer to Figure 23). The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the SW pin to the inductor should be kept as short and wide as possible. The output capacitor Cout should be put close to VOUT pin. It is also beneficial to have the ground of Cout close to the GND pin since there is large ground return current flowing between them. FB resistor should be put close to FB pin. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point close to the GND pin.

ADDITIONAL APPLICATION CIRCUITS

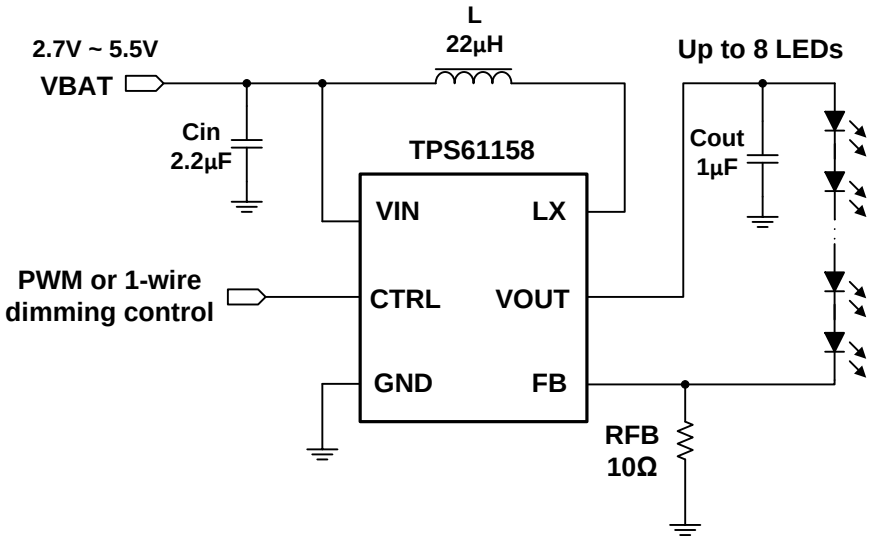


Figure 22. TPS61158 to Drive up to 8 LEDs

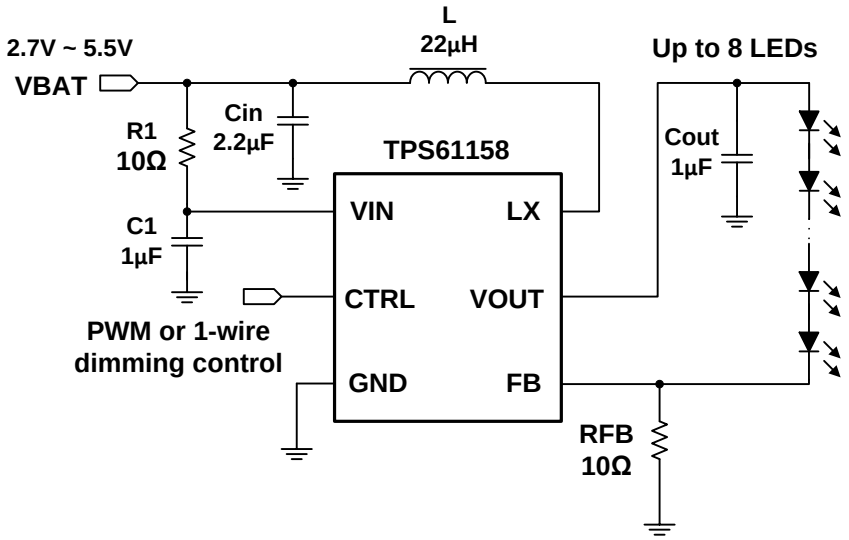


Figure 23. TPS61158 to Drive up to 8 LEDs with RC Filter at VIN Pin

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61158DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SIW
TPS61158DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SIW
TPS61158DRVRG4	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SIW
TPS61158DRVRG4.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SIW

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

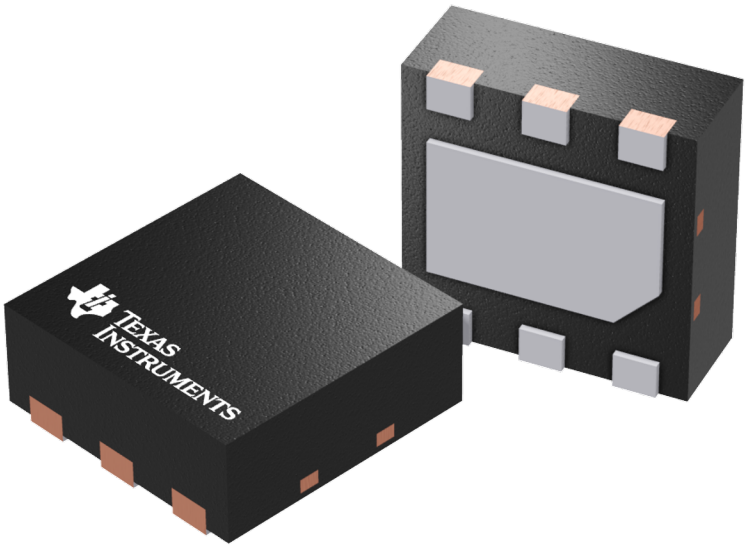
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

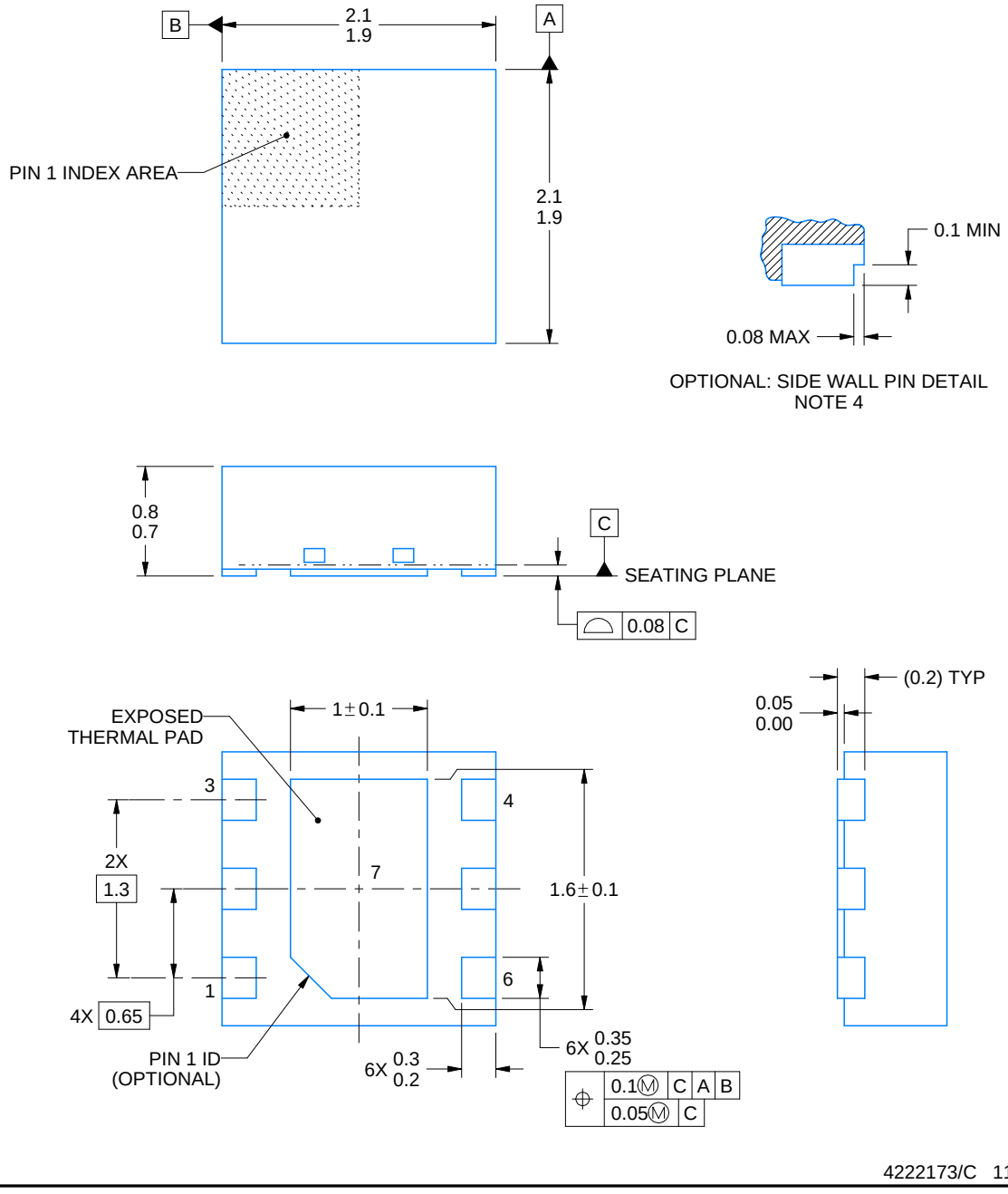
DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



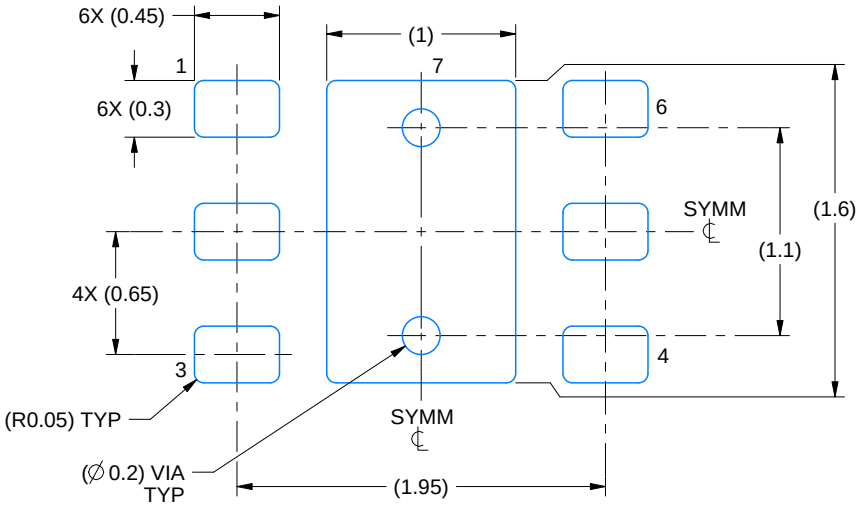
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PLASTIC SMALL OUTLINE - NO LEAD

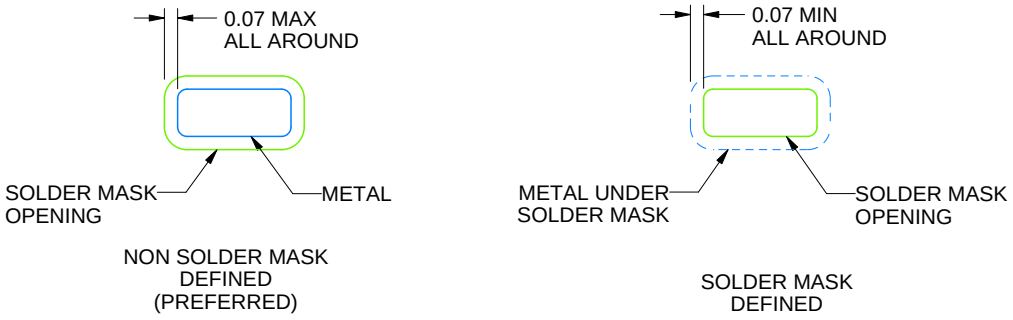


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS

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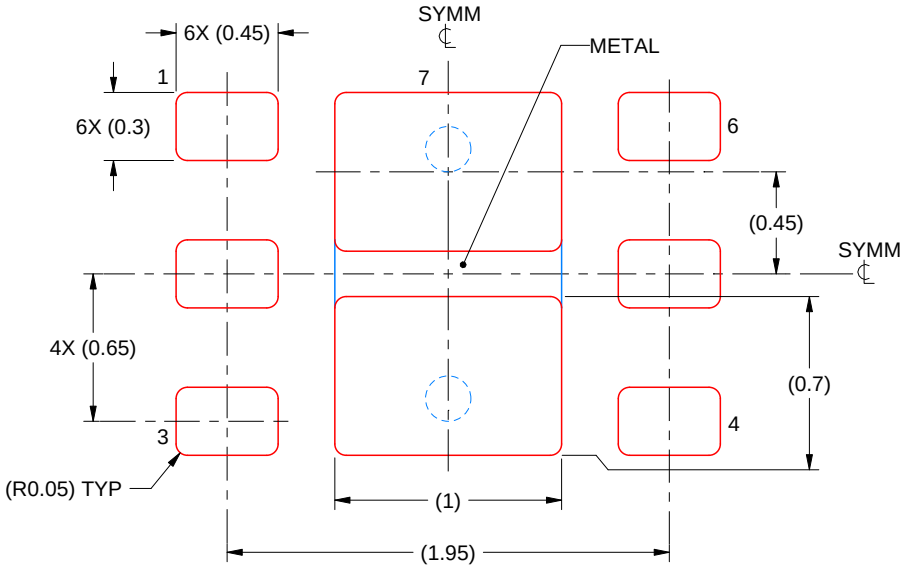
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/C 11/2025

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月