TPS6106x Constant Current LED Driver With Digital and PWM Brightness Control

1 Features

- LED Driver With Integrated Overvoltage and Short-Circuit Protection
- 2.7-V to 6-V Input Voltage Range
- 500-mV or 250-mV Feedback Voltage
- TPS61060 Powers up to 3 LEDs
- TPS61061 Powers up to 4 LEDs
- TPS61062 Powers up to 5 LEDs
- PWM Brightness Control on Enable
- Digital Brightness Control on ILED
- 1-MHz Fixed Switching Frequency
- 400-mA Internal Power MOSFET Switch
- LEDs Disconnected During Shutdown
- Operates With Small-Output Capacitors Down to 220 nF
- Up to 80% Efficiency
- 8-Pin NanoFree™ Package (Chipscale, CSP)
- 3-mm × 3-mm QFN Package

2 Applications

- White LED Drivers
- Cellular Phones
- PDAs, Pocket PCs, and Smart Phones
- Digital Still Cameras
- Handheld Devices

3 Description

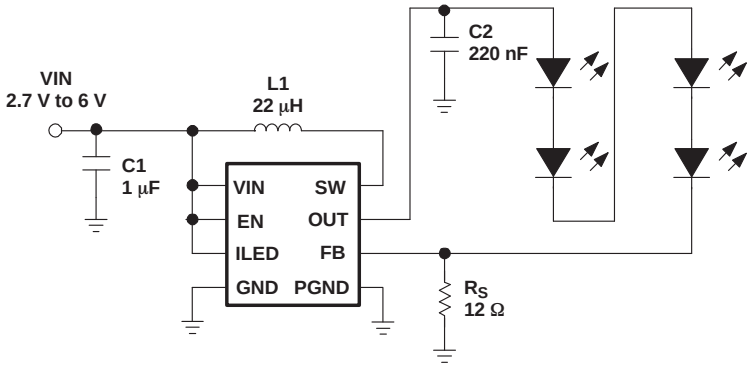
The TPS6106x is a high-frequency, synchronous boost converter with constant current output to drive up to five white LEDs. For maximum safety, the device features integrated overvoltage and an advanced short-circuit protection when the output is shorted to ground. The device operates with 1-MHz fixed switching frequency to allow for the use of small external components and to simplify possible EMI problems. The device comes with three different overvoltage protection thresholds (14 V, 18 V, and 23 V) to allow inexpensive and small-output capacitors with lower voltage ratings. The LED current is initially set with the external sense resistor R_S, and the feedback voltage is regulated to 500 mV or 250 mV, depending on the configuration of the ILED pin. Digital brightness control is implemented by applying a simple digital signal to the ILED pin. Alternatively, a PWM signal up to 1 kHz can be applied to the enable pin to control the brightness of the LED. During shutdown, the output is disconnected from the input to avoid leakage current through the LEDs.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61060, TPS61061, TPS61062	VSON (8)	3.00 mm × 3.00 mm
	DSBGA (8)	1.446 mm × 1.446 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application



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4 Revision History

Changes from Revision A (April 2005) to Revision B **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

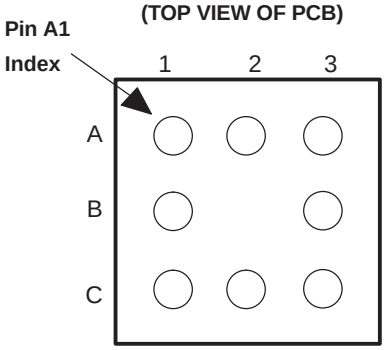
5 Device Comparison Table

T_A	OVERVOLTAGE PROTECTION (OVP)	PACKAGE		PACKAGE MARKING	
		NanoFree(1)	QFN(2)	NanoFree	QFN
–40 to 85°C	14 V (min)	TPS61060YZF	TPS61060DRB	AKX	AQP
	18 V (min)	TPS61061YZF	TPS61061DRB	AKY	AQQ
	22.2 V (min)	TPS61062YZF	TPS61062DRB	AKZ	AQR

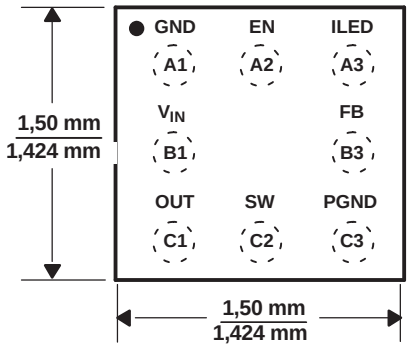
(1) The YZF package is available in tape and reel. Add R suffix (TPS61060YZFR) to order quantities of 3000 parts per reel or add T suffix (TPS61060YZFT) to order 250 parts per reel.
(2) The DRB package is available in tape and reel. Add R suffix (TPS61060DRBR) to order quantities of 3000 parts per reel.

6 Pin Configuration and Functions

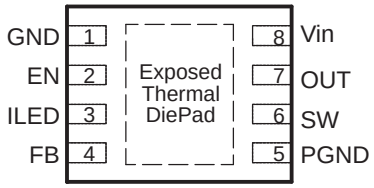
8-BALL NanoFree PACKAGE (TOP VIEW OF PCB)



8-BALL WAFER CHIP SCALE YZF PACKAGE TPS6106x DIMENSIONS (TOP VIEW OF PCB)



8-Pin 3x3-mm QFN Package Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	CSP	QFN		
VIN	B1	8	I	Input supply pin of the device
EN	A2	2	I	Enable pin. This pin needs to be pulled high to enable the device. To allow brightness control of the LEDs, a PWM signal up to 1 kHz can be applied. This pin has an internal pulldown resistor.
GND	A1	1		Analog ground
PGND	C3	5		Power ground
FB	B3	4	I	This is the feedback pin of the device. The feedback pin regulates the LED current through the sense resistor by regulating the voltage across Rs. The feedback voltage is set by the ILED pin. ILED=GND sets the feedback voltage to 500 mV. ILED=high sets the feedback voltage to 250 mV. Refer to digital brightness control section for more information.
OUT	C1	7	O	Output of the device

Pin Functions (continued)

PIN			I/O	DESCRIPTION
NAME	NO.			
	CSP	QFN		
SW	C2	6	I	Switch pin of the device
ILED	A3	3	I	Digital brightness control input. When this pin is grounded, the digital brightness control is disabled. When this pin is connected to high, then the feedback voltage is reduced to typically 250 mV and the digital brightness control is enabled. Refer to digital brightness control section for more information.
PowerPAD™	–	–		The PowerPAD™ (exposed thermal diepad) is only available on the QFN package. The PowerPAD™ needs to be connected and soldered to analog ground (GND).

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN(2)	Supply voltages on pin	–0.3	7	V
EN, ILED, FB(2)	Voltages on pins	–0.3	7	V
OUT(2)	Voltage on pin		33	V
SW(2)	Voltage on pin		33	V
	Operating junction temperature	–40	150	°C
	Lead temperature (soldering, 10 s)		260	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_I	Input voltage range	2.7		6.0	V
L	Inductor(1)		22		µH
C_I	Input capacitor(1)		1		µF
C_O	Output capacitor(1)	0.22	1		µF
T_A	Operating ambient temperature	-40		85	°C
T_J	Operating junction temperature	-40		125	°C

(1) Refer to application section for further information.

7.4 Thermal Information

THERMAL METRIC[1]		TPS6106x		UNIT
		DRB	YZF	
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.6	120.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.1	0.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	23.2	59.4	
ψ_{JT}	Junction-to-top characterization parameter	1.0	2.2	
ψ_{JB}	Junction-to-board characterization parameter	23.4	59.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.1	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{in} = 3.6 V, EN = V_{IN}, T_A= –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range		2.7		6	V
I_Q	Operating quiescent current into Vin	Device not switching			1	mA
I_{SD}	Shutdown current	EN = GND		1	10	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		1.65	1.8	V
V_{HYS}	Undervoltage lockout hysteresis			50		mV
ENABLE AND ILED						
V_{EN}	Enable high-level voltage	V_{IN} = 2.7 V to 6 V	1.2			V
V_{EN}	Enable low-level voltage	V_{IN} = 2.7 V to 6 V			0.4	V
R_{EN}	Enable pulldown resistor		200	300		kΩ
t_{shtdn}	Enable-to-shutdown delay (1)	EN = high to low			50	ms
t_{PWML}	PWM low-level signal time (1)	PWM signal applied to EN			25	ms
V_{ILED}	ILED high-level voltage	V_{IN} = 2.7 V to 6 V	1.2			V
V_{ILED}	ILED low-level voltage	V_{IN} = 2.7 V to 6 V			0.4	V
I_{ILED}	ILED input leakage current	ILED = GND or VIN		0.1	3	µA
	DAC resolution	5 Bit		15.6		mV
t_{up}	Increase feedback voltage one step	ILED = high to low	1		75	µs
t_{down}	Decrease feedback voltage one step	ILED = high to low	180		300	µs
t_{delay}	Delay time between up/down steps	ILED = low to high	1.5			µs
t_{off}	Digital programming off, VFB = 500 mV	ILED = high to low	720			µs
FEEDBACK FB						
I_{FB}	Feedback input bias current	V_{FB} = 500 mV		1	1.5	µA
V_{FB}	Feedback regulation voltage	ILED = GND, after start-up	485	500	515	mV
V_{FB}	Feedback regulation voltage	ILED = High, after start-up	240	250	260	mV
POWER SWITCH SYNCHRONOUS RECTIFIER AND CURRENT LIMIT (SW)						
$r_{DS(ON)}$	P-channel MOSFET on-resistance	V_O = 10 V, Isw = 10 mA		2.5	3.7	Ω
$R_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 3.6 V, Isw = 100 mA		0.6	0.9	Ω
	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 2.7 V, Isw = 100 mA		0.7	1.0	Ω
I_{swleak}	Switch leakage current (2)	V_{IN} = V_{SW}= 6 V, V_{OUT} = GND, EN = GND		0.1	2	µA
I_{SW}	N-Channel MOSFET current limit	V_O = 10 V	325	400	475	mA

(1) A PWM low signal applied to EN for a time (≥25 ms) could cause a device shutdown. After a period of ≥50 ms the device definitely enters shutdown mode.
(2) The switch leakage current includes the leakage current of both internal switches, which is the leakage current from SW to ground, and from SW to V_{OUT}, with V_{IN} = V_{SW}.

Electrical Characteristics (continued)

V_{in} = 3.6 V, EN = V_{IN}, T_A= –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR						
f_s	Switching frequency		0.8	1.0	1.2	MHz
OUTPUT						
Vovp	Output overvoltage protection	V_O rising; TPS61060	14	14.5	16	V
Vovp	Output overvoltage protection	V_O rising; TPS61061	18	18.5	19.8	V
Vovp	Output overvoltage protection	V_O rising; TPS61062	22.2	23.5	25	V
Vovp	Output overvoltage protection hysteresis	TPS61060/61/62, V_O falling		0.7		V
Vo	Output voltage threshold for short-circuit detection	V_O falling		V_{IN}–0.7		V
Vo	Output voltage threshold for short-circuit detection	V_O rising		V_{IN}–0.3		V
Ipre	Precharge current and short-circuit current	Start-up, EN = low to high, OUT = GND				mA
		V_{IN} = 6 V		180		
		V_{IN} = 3.6 V		95		
		V_{IN} = 2.7 V		65		
D	Maximum duty cycle			95%		

7.6 Typical Characteristics

Table 1. Table of Graphs

		FIGURE
Efficiency (η)	vs LED current; 2 LEDs, ILED = high	Figure 1
	vs LED current; 3 LEDs, ILED = low	Figure 2
	vs LED current; 3 LEDs, ILED = high	Figure 3
	vs LED current; 4 LEDs, ILED = low	Figure 4
	vs LED current; 4 LEDs, ILED = high	Figure 5
	vs LED current; 5 LEDs, ILED = high	Figure 6
Digital brightness control	Feedback voltage vs ILED programming step	Figure 7
LED current	vs PWM duty cycle	Figure 8

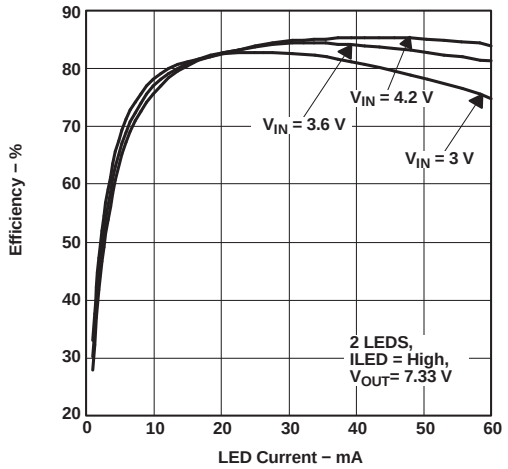


Figure 1. Efficiency vs LED Current

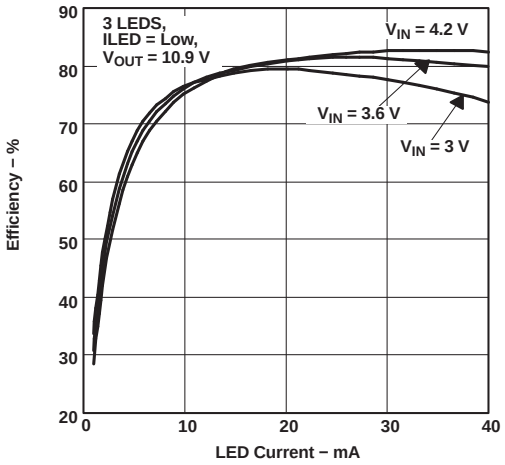


Figure 2. Efficiency vs LED Current

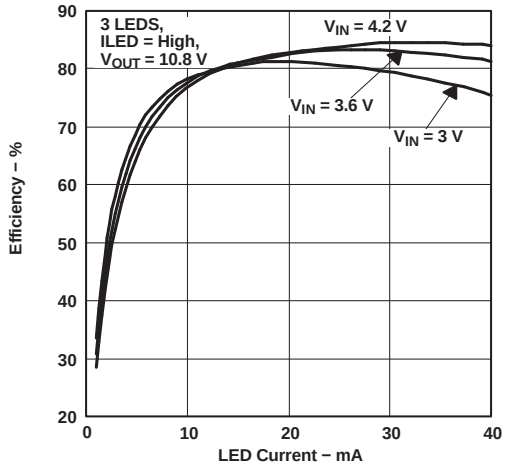


Figure 3. Efficiency vs LED Current

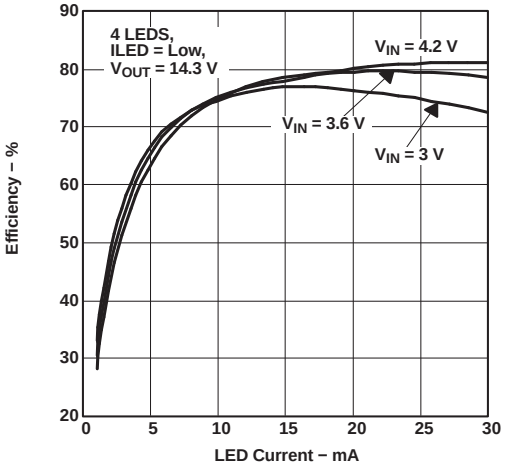


Figure 4. Efficiency vs LED Current

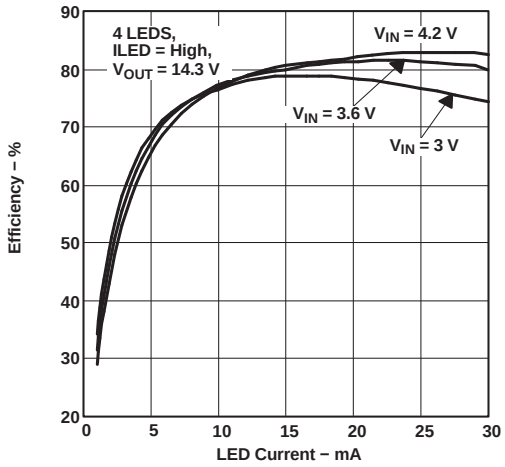


Figure 5. Efficiency vs LED Current

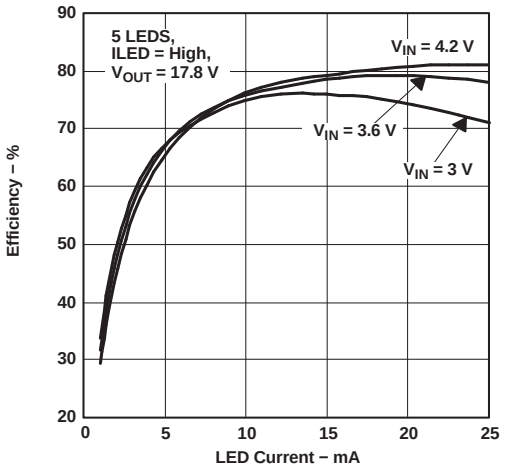


Figure 6. Efficiency vs LED Current

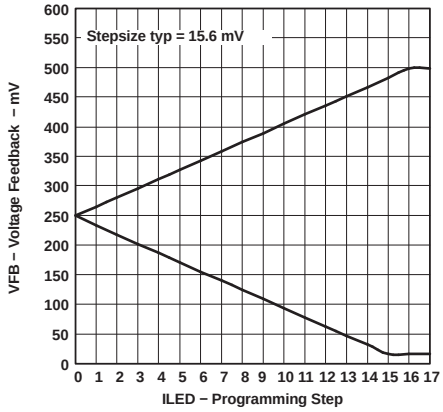


Figure 7. Digital Brightness Control Feedback Voltage vs ILED Programming Step

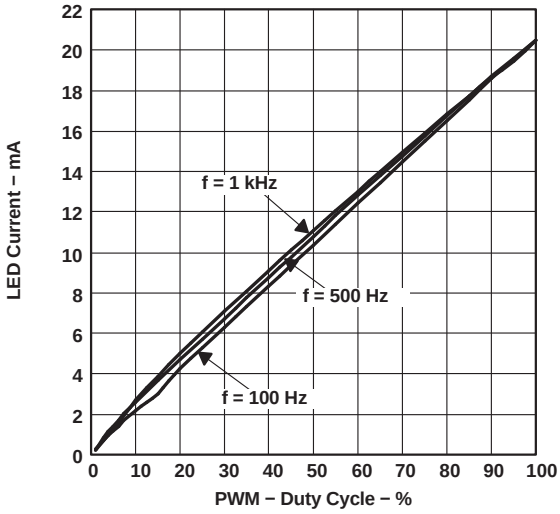


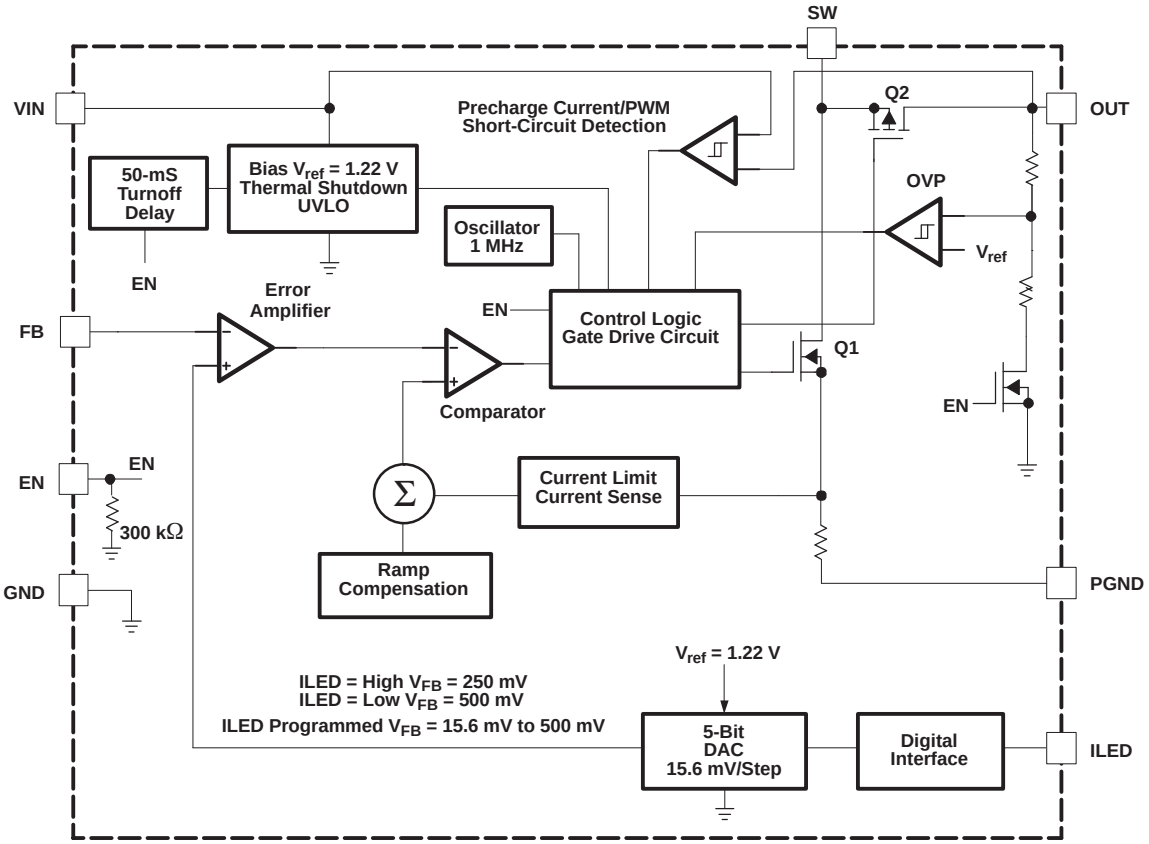
Figure 8. LED Current vs PWM Duty Cycle

8 Detailed Description

8.1 Overview

The TPS61060/61/62 family is a constant-frequency, PWM current-mode converter with an integrated N-channel MOSFET switch and synchronous P-channel MOSFET rectifier. The device operates in pulse width modulation (PWM) with a fixed switching frequency of 1 MHz. For an understanding of the device operation, refer the block diagram. The duty cycle of the converter is set by the error amplifier and the sawtooth ramp applied to the comparator. Because the control architecture is based on a current-mode control, a compensation ramp is added to allow stable operation for duty cycles larger than 50%. The converter is a fully integrated synchronous boost converter operating always in continuous conduction mode. This allows low noise operation and avoids ringing on the switch pin as it would be seen on a converter when entering discontinuous conduction mode.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Start-Up

To avoid high inrush current during start-up, special care is taken to control the inrush current. When the device is first enabled, the output capacitor is charged with a constant precharge current of typically 100 mA until the output voltage is typically 0.3 V below VIN. The device starts with a reduced analog controlled current limit for typically 40 µs. After this time, the device enters its normal regulation with full current limit. The fixed precharge current during start-up allows the device to start up without problems when driving LEDs because the LED only starts to conduct current when the forward voltage is reached. If, for any reason a resistive load is driven, the maximum start-up load current must be smaller, or equal to, the precharge current.

Feature Description (continued)

8.3.2 Short-Circuit Protection

The TPS6106x family has an advanced short-circuit protection in case the output of the device is shorted to ground. Because the device is configured as a current source even when the LEDs are shorted, the maximum current is controlled by the sense resistor Rs. As an additional safety feature, the TPS6106x series also protects the device and inductor when the output is shorted to ground. When the output is shorted to ground, the device enters precharge mode and limits the maximum current to typically 100 mA.

8.3.3 Overvoltage Protection (OVP)

As with any current source, the output voltage rises when the output gets high impedance or disconnected. To prevent the output voltage exceeding the maximum switch voltage rating (33 V) of the main switch, an overvoltage protection circuit is integrated. As soon as the output voltage exceeds the OVP threshold, the converter stops switching and the output voltage falls down. When the output voltage falls below the OVP threshold, the converter continues operation until the output voltage exceeds the OVP threshold again. To allow the use of inexpensive low-voltage output capacitors, the TPS6106x series has different OVP levels that must be selected according to the number of external LEDs and their maximum forward voltage.

8.3.4 Efficiency and Feedback Voltage

The feedback voltage has a direct effect on the converter efficiency. Because the voltage drop across the feedback resistor does not contribute to the output power (LED brightness), the lower the feedback voltage, the higher the efficiency. Especially when powering only three or less LEDs, the feedback voltage impacts the efficiency around 2% depending on the sum of the forward voltage of the LEDs. To take advantage of this, the ILED pin can be connected to VIN, setting the feedback voltage to 250 mV.

8.3.5 Undervoltage Lockout

An undervoltage lockout prevents mis-operation of the device at input voltages below typical 1.65 V. When the input voltage is below the undervoltage threshold, the device remains off and both internal MOSFETs are turned off providing isolation between input and output.

8.3.6 Thermal Shutdown

An internal thermal shutdown is implemented and turns off the internal MOSFETs when the typical junction temperature of 160°C is exceeded. The thermal shutdown has a hysteresis of typically 15°C.

8.4 Device Functional Modes

8.4.1 Enable PWM Dimming

The EN pin allows disabling and enabling of the device as well as brightness control of the LEDs by applying a PWM signal up to typically 1 kHz. When a PWM signal is applied, the LED current is turned on when the EN is high and off when EN is pulled low. Changing the PWM duty cycle therefore changes the LED brightness. To allow higher PWM frequencies on the enable pin, the device continues operation when a PWM signal is applied. As shown in the block diagram, the EN pin needs to be pulled low for at least 50 ms to fully turn the device off. The enable input pin has an internal 300-kΩ pulldown resistor to disable the device when this pin is floating.

8.4.2 Digital Brightness Control (ILED)

The ILED pin features a simple digital interface to allow digital brightness control. This can save processor power and battery life. Using the digital interface to control the LED brightness does not required a PWM signal all the time, and the processor can enter sleep mode if available. To save signal lines, the ILED pin can be connected to the enable pin to allow digital programming and enable/disable function at the same time with the same signal. Such a circuit is shown in Figure 9.

Device Functional Modes (continued)

The ILED pin basically sets the feedback regulation voltage (V_{FB}); thus, it sets the LED current. When the ILED pin is connected to GND, the digital brightness control is disabled and the feedback is regulated to V_{FB} = 500 mV. When the ILED pin is pulled high, the digital brightness control is enabled starting at its midpoint where the feedback is regulated to V_{FB} = 250 mV. The digital brightness control is implemented by adjusting the feedback voltage in digital steps with a typical maximum voltage of V_{FB} = 500 mV. For this purpose, a 5-bit DAC is used giving 32 steps equal to a 15.6-mV change in feedback voltage per step. To increase or decrease the internal reference voltage, the ILED pin needs to be pulled low over time as outlined in Table 2 and specified in the electrical table. When the internal DAC is programmed to its highest or lowest value, it stays at this value until it gets programmed in the opposite direction again.

Table 2. Increase/Decrease Internal Reference Voltage

FEEDBACK VOLTAGE	TIME	ILED LOGIC LEVEL
Increase	1 µs to 75 µs	Low
Decrease	180 µs to 300 µs	Low
Brightness control disabled	≥550 µs	Low
Delay between steps	1.5 µs	High

Between each cycle the ILED pin needs to be pulled high for 1.5 µs.

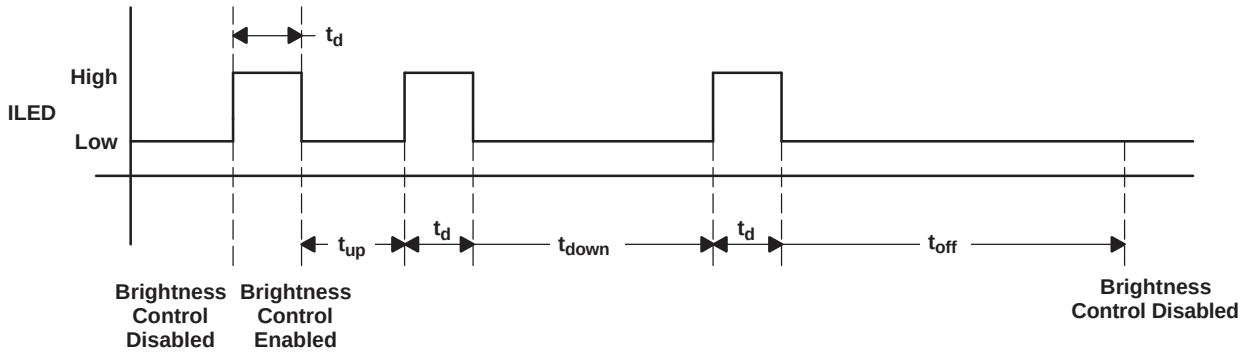


Figure 9. ILED Timing Diagram

Using the digital interface on the ILED pin allows simple implementation of a two-step brightness control by pulling the ILED either high or low. For full LED current with V_{FB} = 500 mV, the ILED must be pulled low; to program half the LED current with V_{FB} = 250 mV, the ILED pin must be pulled high.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6106x is designed to driver up to five LEDs in series with constant current output. The device, which operates in peak current mode PWM control, has a switch peak current limit of 325-mA minimum and internal loop compensation. The switching frequency is fixed at 1 MHz, and the input voltage range is 2.7 to 6.0 V. The following section provides a step-by-step design approach for configuring the TPS61060 to power two white LEDs in series.

9.2 Typical Application

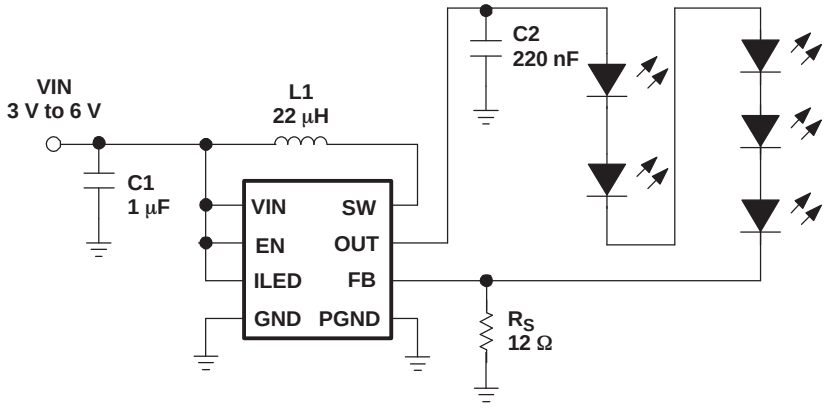


Figure 10. TPS61062 Powering Five White LEDs

9.2.1 Design Requirements

PARAMETER	VALUE
Input Voltage	3 V to 6 V
Output Current	20 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The device requires typically a 22-µH or 10-µH inductance. When selecting the inductor, the inductor saturation current should be rated as high as the peak inductor current at maximum load, and respectively, maximum LED current. Because of the special control loop design, the inductor saturation current does not need to be rated for the maximum switch current of the converter. The maximum converter switch current usually is not reached even when the LED current is pulsed by applying a PWM signal to the enable pin. The maximum inductor peak current, as well as LED current, is calculated as:

$$\text{Duty cycle}: D = 1 - \frac{Vin}{Vout} \quad (1)$$

$$\text{Maximum LED current}: I_{LED} = \left(Isw - \frac{Vin \times D}{2 \times fs \times L}\right) \times (1 - D) \times \eta \quad (2)$$

$$\text{Inductor peak current}: i_{Lpeak} = \frac{Vin \times D}{2 \times fs \times L} + \frac{I_{LED}}{(1 - D) \times \eta} \quad (3)$$

with:

fs = Switching frequency (1 MHz typical)
L = Inductor value
η = Estimated converter efficiency (0.75)
Isw = Minimum N-channel MOSFET current limit (325 mA)

(4)

Using the expected converter efficiency is a simple approach to calculate maximum possible LED current as well as peak inductor current. The efficiency can be estimated by taking the efficiency numbers out of the provided efficiency curves or to use a worst-case assumption for the expected efficiency, for example, 75%.

9.2.2.2 Efficiency

The overall efficiency of the application depends on the specific application conditions and mainly on the selection of the inductor. A physically smaller inductor usually shows lower efficiency due to higher switching losses of the inductor (core losses, proximity losses, skin effect losses). A trade-off between physical inductor size and overall efficiency has to be made. The efficiency can typically vary around ±5% depending on the selected inductor. Figure 2 to Figure 7 can be used as a guideline for the application efficiency. These curves show the typical efficiency with a 22-µH inductor (Murata Electronics LQH32CN220K23). Figure 11 shows a basic setup where the efficiency is taken/measured as:

$$\eta = \frac{V_{LED} \times I_{LED}}{V_{in} \times I_{in}} \quad (5)$$

Table 3. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER	DIMENSIONS
10 µH	TDK VLF3012AT-100MR49	2.6 mm × 2.8 mm × 1.2 mm
10 µH	Murata LQH32CN100K53	3.2 mm × 2.5 mm × 1.55 mm
10 µH	Murata LQH32CN100K23	3.2 mm × 2.5 mm × 2.0 mm
22 µH	TDK VLF3012AT-220MR33	2.6 mm × 2.8 mm × 1.2 mm
22 µH	Murata LQH32CN220K53	3.2 mm × 2.5 mm × 1.55 mm
22 µH	Murata LQH32CN220K23	3.2 mm × 2.5 mm × 2.0 mm

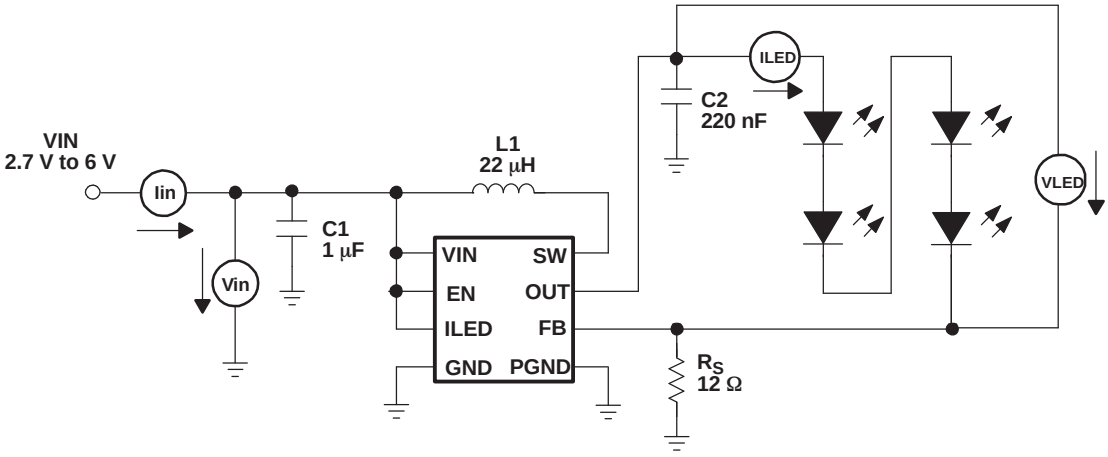


Figure 11. Efficiency Measurement Setup

9.2.2.3 Output Capacitor Selection

The device is designed to operate with a fairly wide selection of ceramic output capacitors. The selection of the output capacitor value is a trade-off between output voltage ripple and capacitor cost and form factor. In general, capacitor values of 220 nF up to 4.7 µF can be used. When using a 220-nF output capacitor, it is recommended to use X5R or X7R dielectric material to avoid the output capacitor value falling far below 220 nF over temperature and applied voltage. For systems with wireless or RF sections, EMI is always a concern. To minimize the voltage ripple in the LED string and board traces, the output capacitor needs to be connected directly from the OUT pin of the device to ground rather than across the LEDs. A larger output capacitor value reduces the output voltage ripple. Table 4 shows possible input and/or output capacitors.

9.2.2.4 Input Capacitor Selection

For good input voltage filtering, low ESR ceramic capacitors are recommended. A 1-µF ceramic input capacitor is sufficient for most of the applications. For better input voltage filtering and EMI reduction, this value can be increased. The input capacitor should be placed as close as possible to the input pin of the converter. Table 4 shows possible input and/or output capacitors.

Table 4. Capacitor Selection

CAPACITOR	VOLTAGE RATING	FORM FACTOR	COMPONENT SUPPLIER(1)	COMMENTS
INPUT CAPACITOR				
1 µF	10 V	0603	Tayo Yuden LMK107BJ105	
OUTPUT CAPACITOR				
220 nF	16 V	0603	Tayo Yuden EMK107BJ224	TPS61060
220 nF	50 V	0805	Tayo Yuden UMK212BJ224	TPS61060/61/62
470 nF	35 V	0805	Tayo Yuden GMK212BJ474	TPS61060/61/62
1 µF	16 V	0805	Tayo Yuden EMK212BJ105	TPS61060
1 µF	35 V	1206	Tayo Yuden GMK316BJ105	TPS61060/61/62
1 µF	25 V	1206	TDK C3216X7R1E105	TPS61060/61/62

(1) Similar capacitors are also available from TDK and other suppliers.

9.2.3 Application Curves

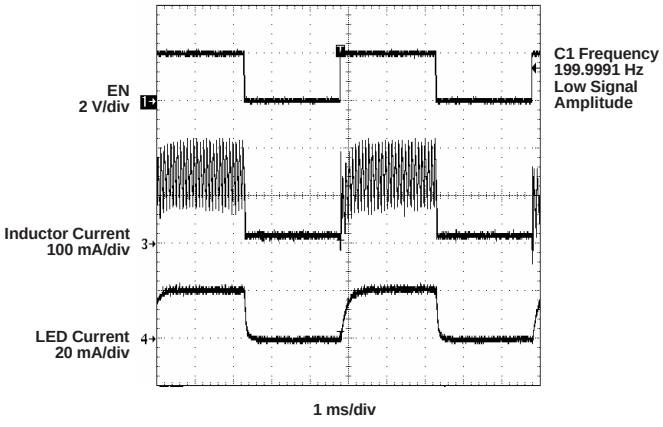


Figure 12. PWM Dimming

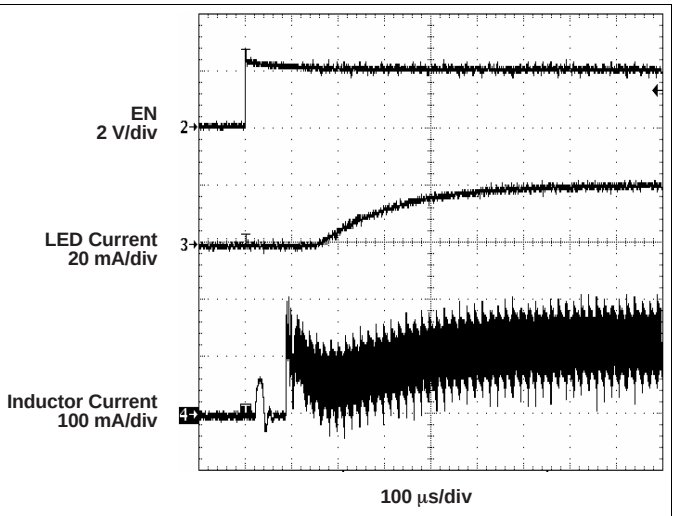


Figure 13. Soft-Start Operation

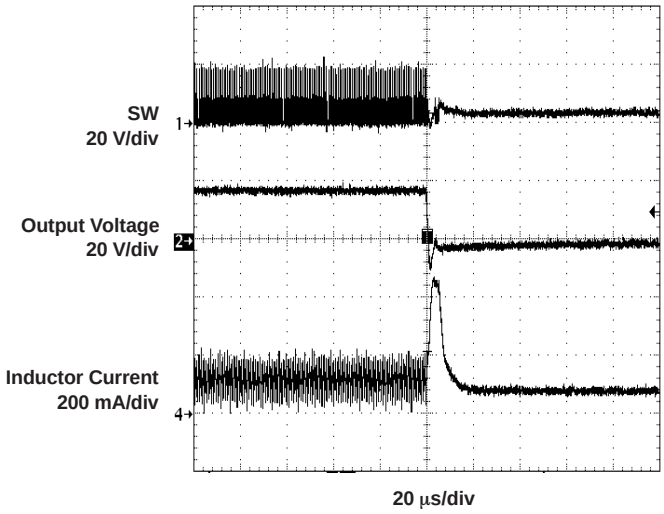


Figure 14. Short-Circuit Protection

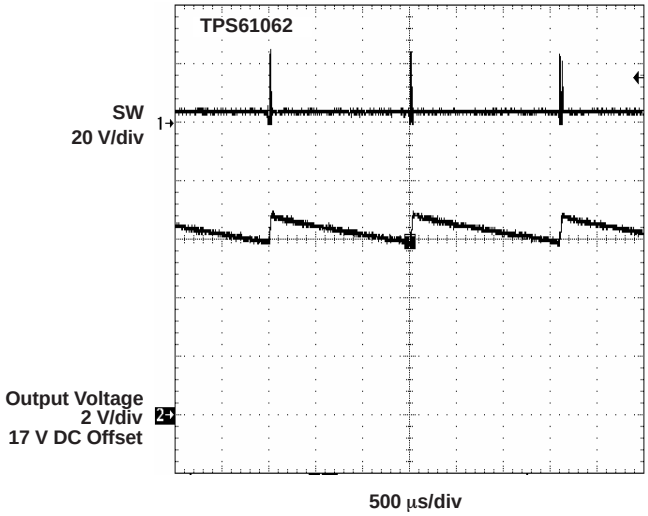


Figure 15. Overvoltage Protection

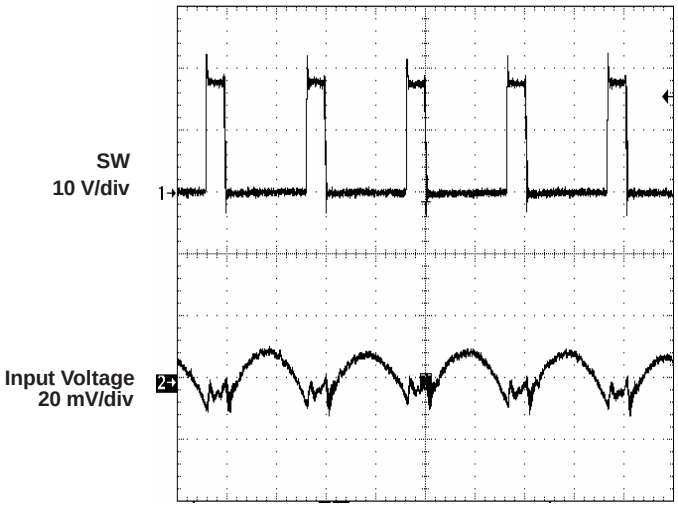


Figure 16. Input Voltage Ripple

9.3 System Examples

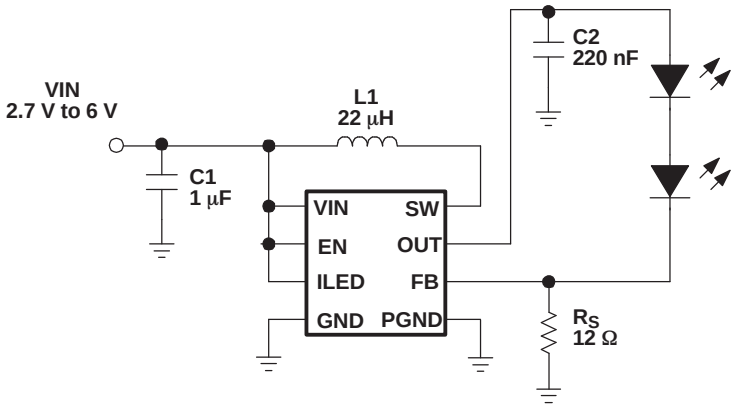


Figure 17. TPS61060 Powering Two White LEDs

System Examples (continued)

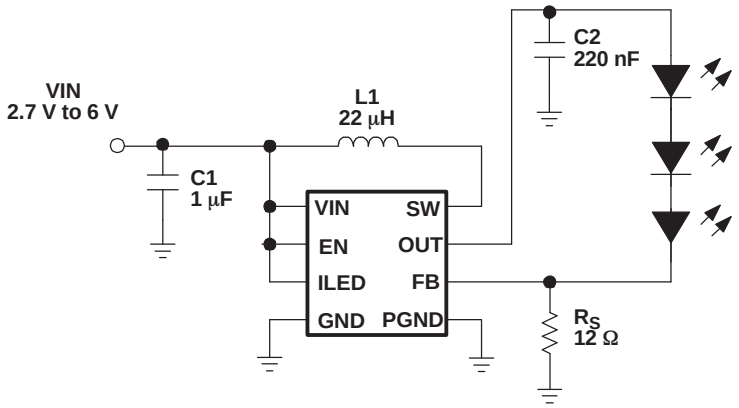


Figure 18. TPS61060 Powering Three White LEDs

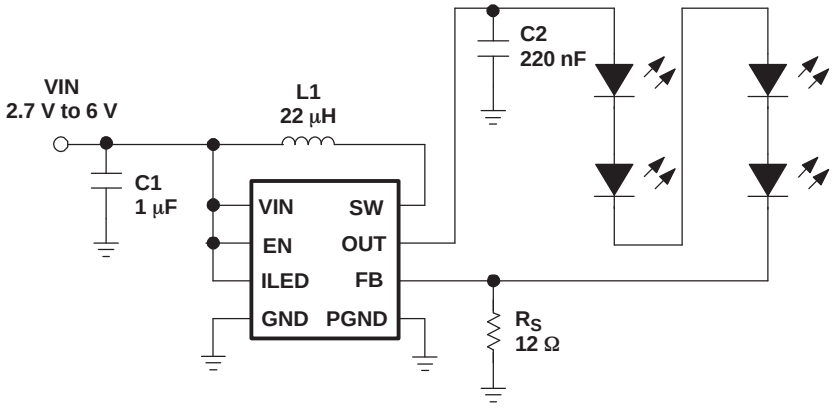


Figure 19. TPS61061 Powering Four White LEDs

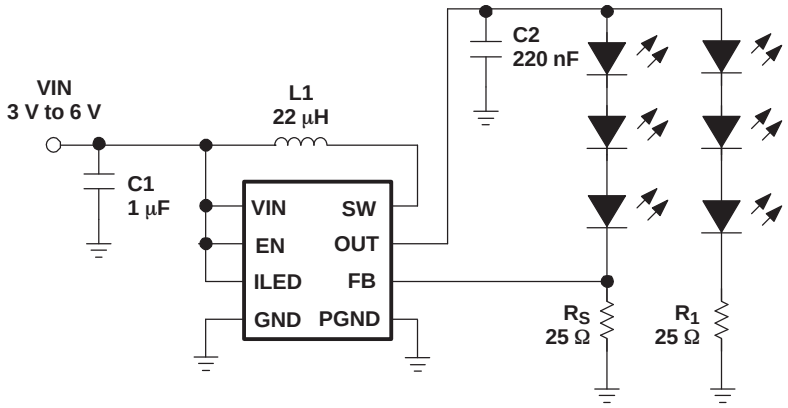
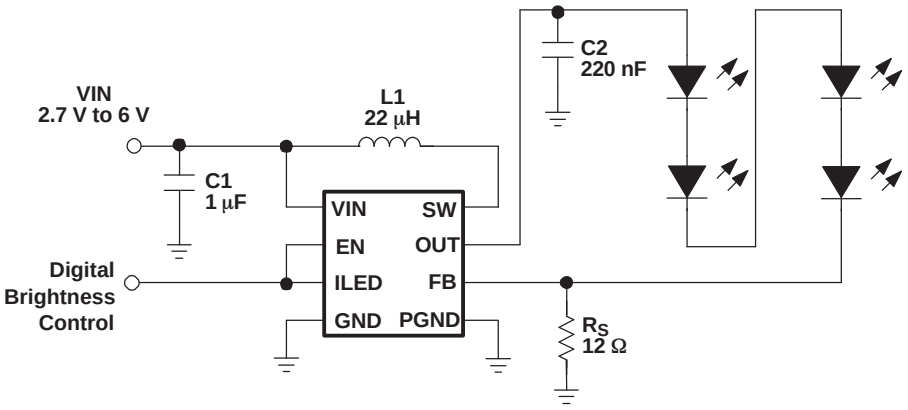


Figure 20. TPS61060 Powering Six White LEDs

System Examples (continued)



This circuit combines the enable with the digital brightness control pin, allowing the digital signal applied to ILED to also enable and disable the device.

Figure 21. TPS61061 Digital Brightness Control

10 Power Supply Recommendations

The TPS6106x is designed to operate from an input voltage supply range from 2.7-V to 6.0-V. The power supply to the TPS6106x must have a current rating according to the supply voltage, output voltage, and output current of the TPS6106x device.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter. The input capacitor should be placed as close as possible to the input pin for good input voltage filtering. The inductor should be placed as close as possible to the switch pin to minimize the noise coupling into other circuits. The output capacitor needs to be placed directly from the OUT pin to GND rather than across the LEDs. This reduces the ripple current in the trace to the LEDs. The GND pin must be connected directly to the PGND pin. When doing the PCB layout, the bold traces (Figure 22) should be routed first, as well as placement of the inductor, and input and output capacitors.

11.2 Layout Example

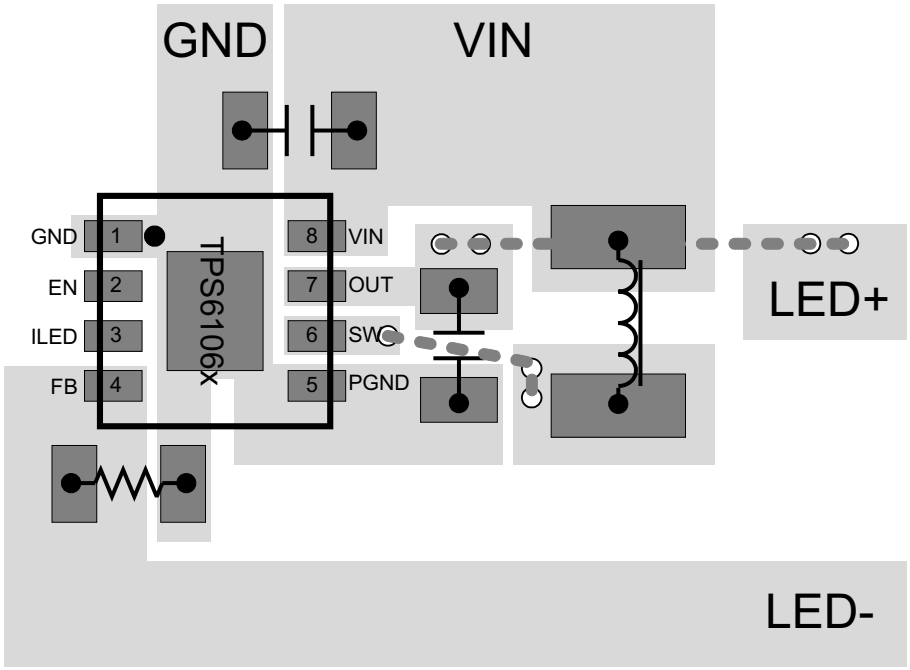


Figure 22. TPS6106x Layout Example

11.3 Thermal Considerations

The TPS6106x comes in a thermally enhanced QFN package. The package includes a thermal pad that improves the thermal capabilities of the package. Also see *QFN/SON PCB Attachment* application report (SLUA271). The thermal resistance junction-to-ambient $R_{\theta JA}$ of the QFN package greatly depends on the PCB layout. Using thermal vias and wide PCB traces improves the thermal resistance $R_{\theta JA}$. The thermal pad must be soldered to the analog ground on the PCB.

For the NanoFree package, similar guidelines apply for the QFN package. The thermal resistance $R_{\theta JA}$ depends mainly on the PCB layout.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS61060	Click here	Click here	Click here	Click here	Click here
TPS61061	Click here	Click here	Click here	Click here	Click here
TPS61062	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

NanoFree, PowerPAD are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Chipscale Package Dimensions

The TPS6106x is available in a Chipscale package and has the following mechanical dimensions: E=D=1,446 mm (typical), E=D=1,424 mm (minimum), E=D=1,5 mm (maximum). See the mechanical drawing of the package (YZF).

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS61060DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQP
TPS61060DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQP
TPS61060DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQP
TPS61060DRBRG4.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQP
TPS61060YZFR	Active	Production	DSBGA (YZF) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKX
TPS61060YZFR.B	Active	Production	DSBGA (YZF) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKX
TPS61060YZFT	Active	Production	DSBGA (YZF) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKX
TPS61060YZFT.B	Active	Production	DSBGA (YZF) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKX
TPS61061DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQQ
TPS61061DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQQ
TPS61061DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQQ
TPS61061DRBRG4.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQQ
TPS61061YZFT	Active	Production	DSBGA (YZF) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKY
TPS61061YZFT.B	Active	Production	DSBGA (YZF) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKY
TPS61062DRBR	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQR
TPS61062DRBR.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQR
TPS61062DRBRG4	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQR
TPS61062DRBRG4.B	Active	Production	SON (DRB) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AQR
TPS61062YZFR	Active	Production	DSBGA (YZF) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKZ
TPS61062YZFR.B	Active	Production	DSBGA (YZF) | 8	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKZ
TPS61062YZFT	Active	Production	DSBGA (YZF) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKZ
TPS61062YZFT.B	Active	Production	DSBGA (YZF) | 8	250 | SMALL T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	AKZ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

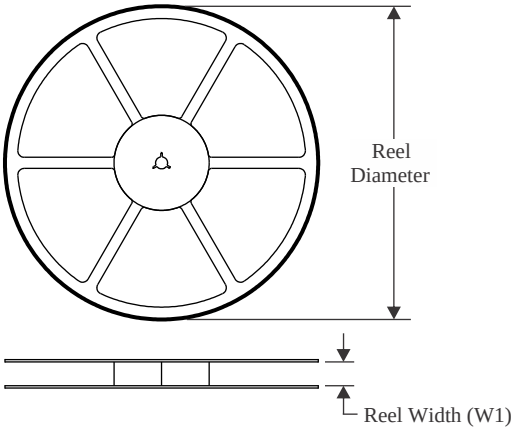
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

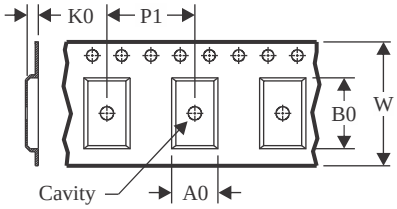
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

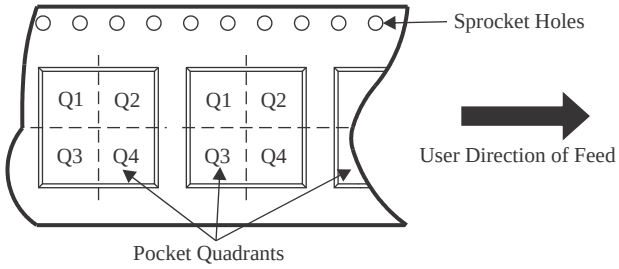


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

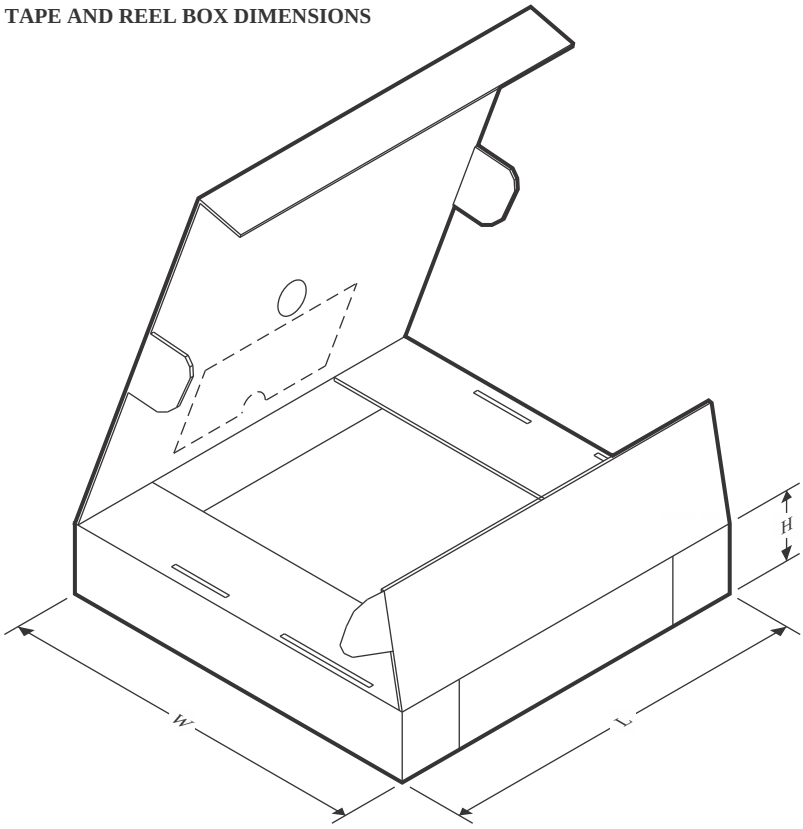
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61060DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61060DRBRG4	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61060YZFR	DSBGA	YZF	8	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPS61060YZFT	DSBGA	YZF	8	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPS61061DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61061DRBRG4	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61061YZFT	DSBGA	YZF	8	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPS61062DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61062DRBRG4	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS61062YZFR	DSBGA	YZF	8	3000	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1
TPS61062YZFT	DSBGA	YZF	8	250	180.0	8.4	1.65	1.65	0.81	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61060DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS61060DRBRG4	SON	DRB	8	3000	353.0	353.0	32.0
TPS61060YZFR	DSBGA	YZF	8	3000	182.0	182.0	20.0
TPS61060YZFT	DSBGA	YZF	8	250	182.0	182.0	20.0
TPS61061DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS61061DRBRG4	SON	DRB	8	3000	353.0	353.0	32.0
TPS61061YZFT	DSBGA	YZF	8	250	182.0	182.0	20.0
TPS61062DRBR	SON	DRB	8	3000	353.0	353.0	32.0
TPS61062DRBRG4	SON	DRB	8	3000	353.0	353.0	32.0
TPS61062YZFR	DSBGA	YZF	8	3000	182.0	182.0	20.0
TPS61062YZFT	DSBGA	YZF	8	250	182.0	182.0	20.0

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

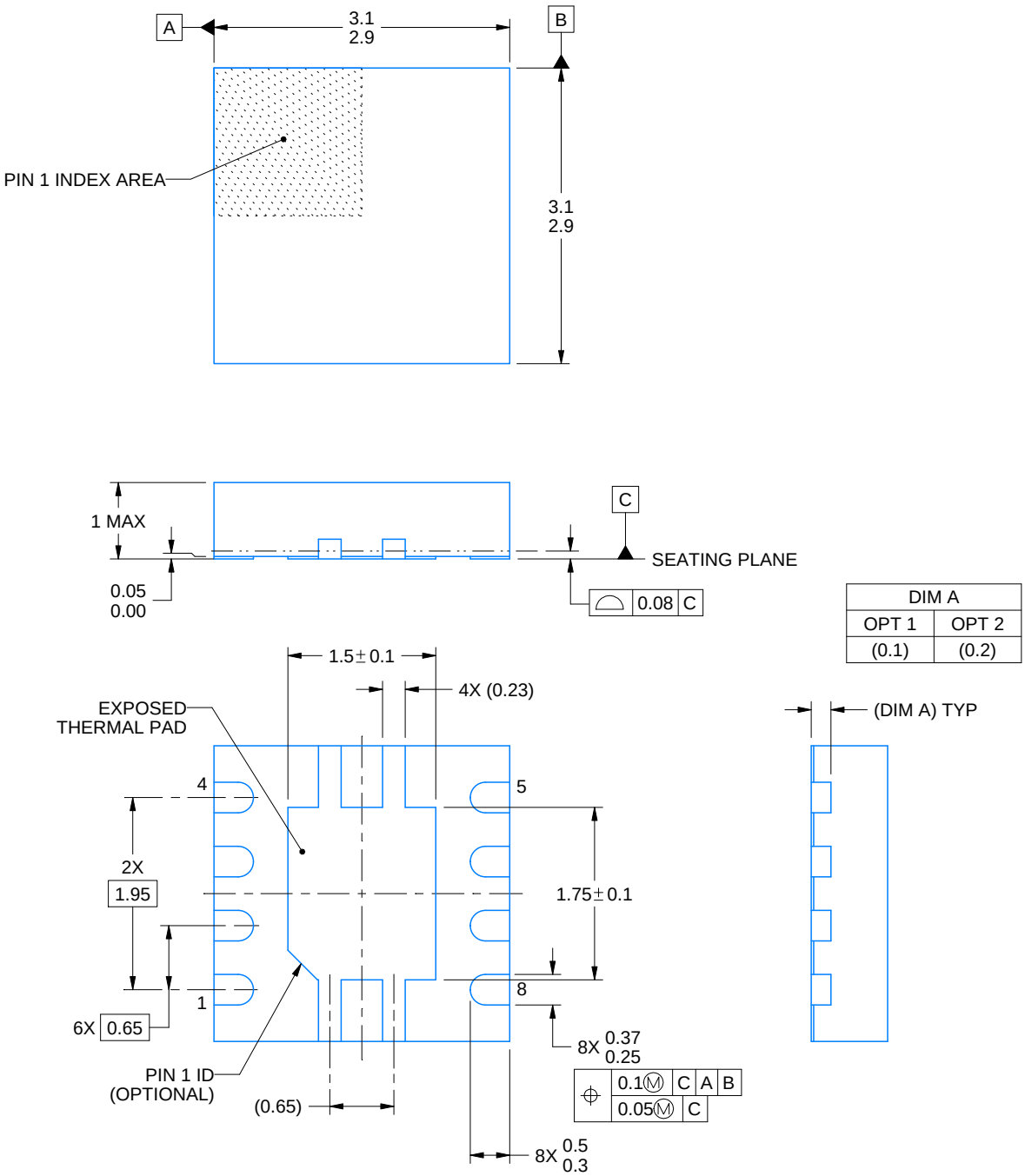
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

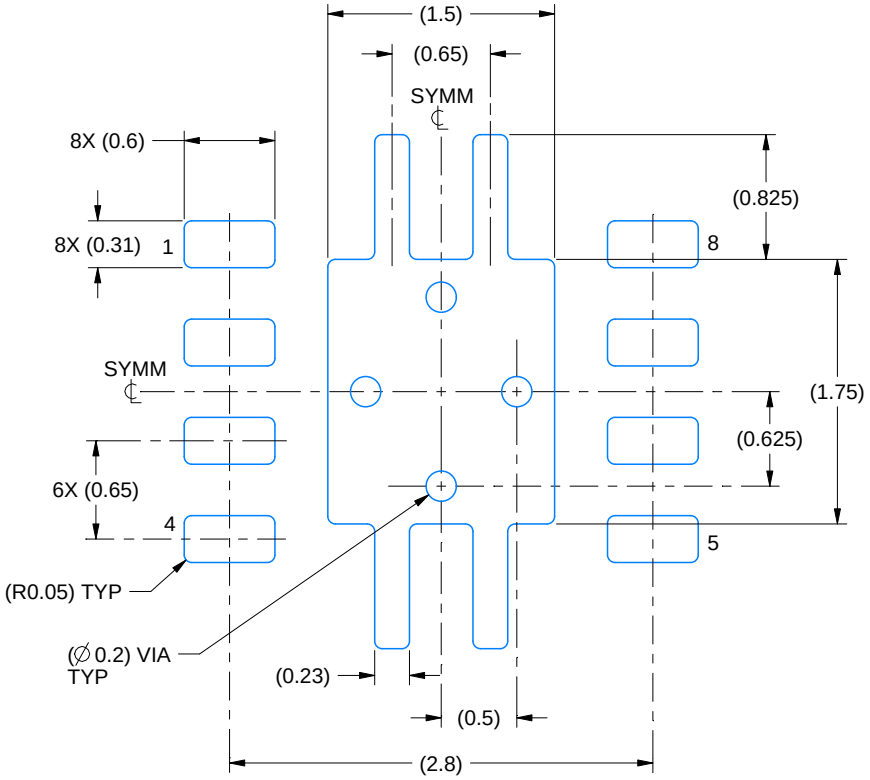
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

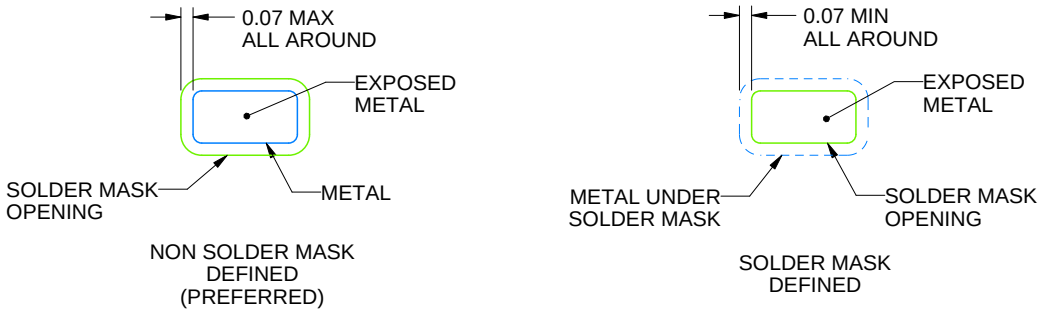
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

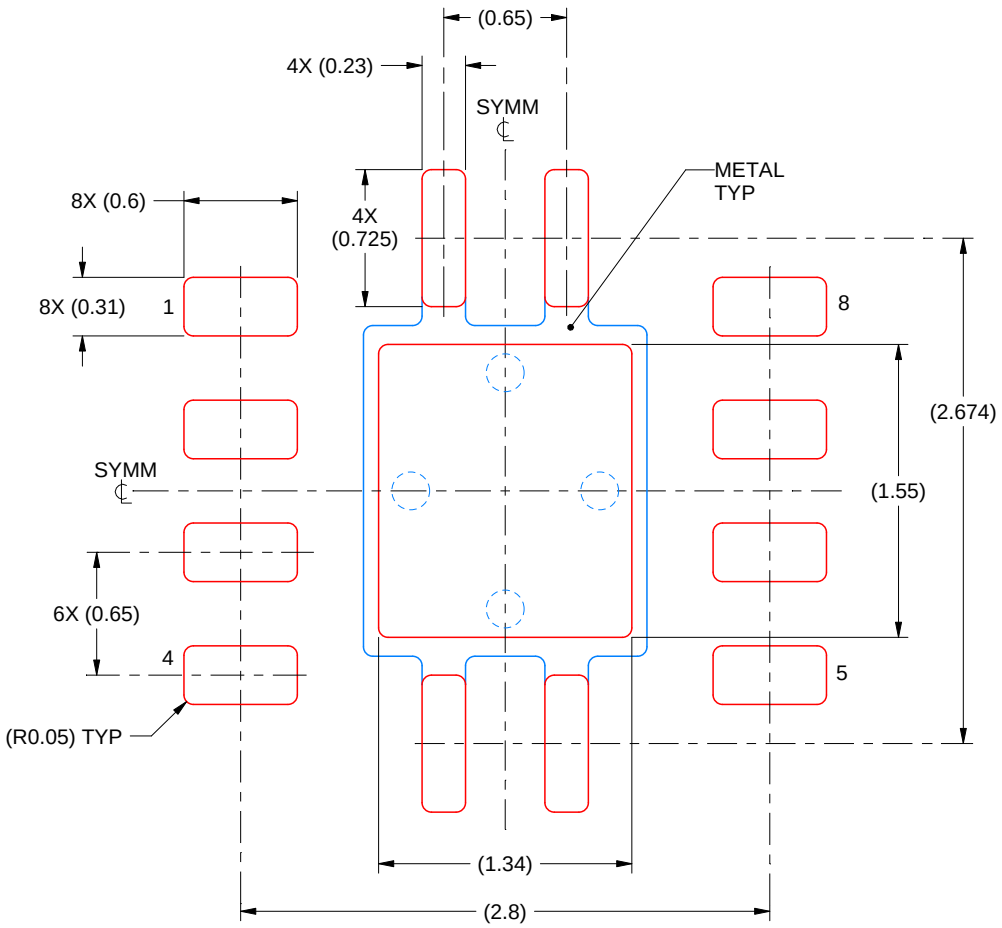


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

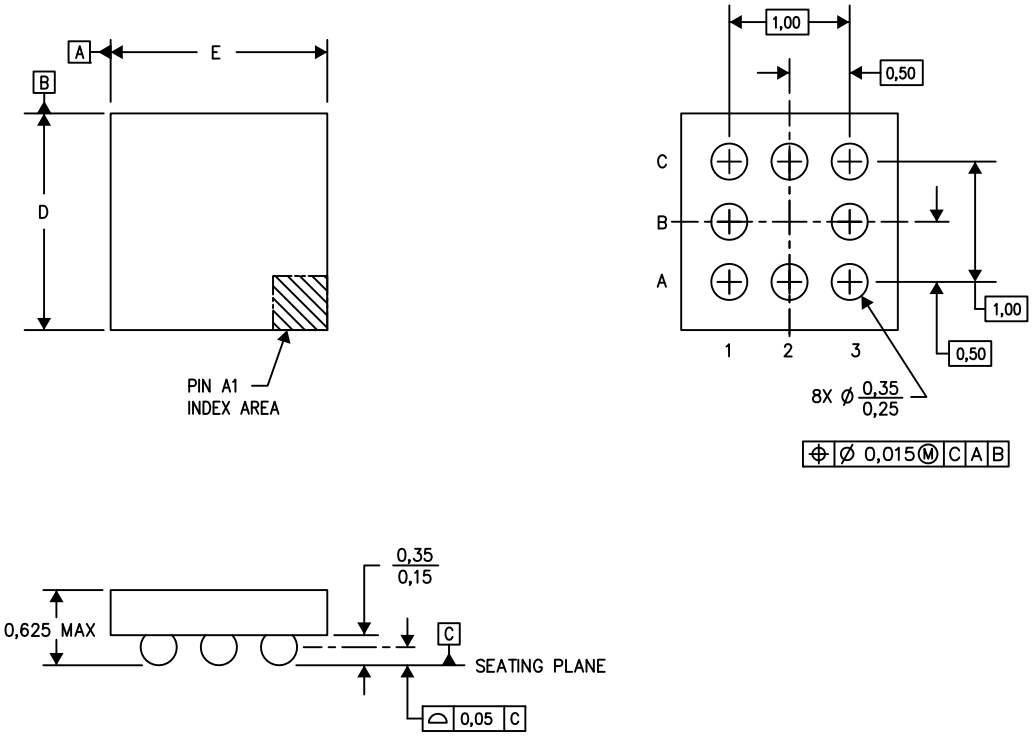
EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YZF (S–XBGA–N8) DIE–SIZE BALL GRID ARRAY



D: Max = 1.49 mm, Min = 1.43 mm

E: Max = 1.49 mm, Min = 1.43 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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