# TPS61033X 具有输出放电功能的 5.5V 5.5A 2.4MHz 全集成同步升压转换器

## 1 特性

- 输入电压范围：1.8V 至 5.5V
- 输出电压范围：2.2V 至 5.5V (TPS61033)
  - FB 连接到 VIN 时，输出电压为固定 5.0V (TPS61033X)
- 两个谷值开关电流限制选项
  - TPS61033：5.5A 典型值
  - TPS610333：1.85A 典型值
- 较高的效率和功率容量
  - 两个 25mΩ (LS)/46mΩ (HS) MOSFET
  - 支持高达 2.4MHz，L-C 较小
  - 效率高达 93.42%（$V_{IN}$ = 3.3V、$V_{OUT}$ = 5V 且 $I_{OUT}$ = 1A 时）
  - 效率高达 90.78%（$V_{IN}$ = 3.3V、$V_{OUT}$ = 5V 且 $I_{OUT}$ = 2A 时）
- 延长系统运行时间
  - 流入 $V_{IN}$ 引脚的静态电流典型值为 20μA
  - 流入 $V_{OUT}$ 引脚的静态电流典型值为 5.3μA
  - 关断电流典型值为 0.1μA
- 在 –40°C 至 +125°C 温度范围内，基准电压精度为 ±1.5%
- 具有窗口比较器的电源正常输出
- 可在轻负载下采用引脚可选的自动 PFM 模式或强制 PWM 模式
- $V_{IN}$ > $V_{OUT}$ 时切换为直通模式
- 安全、可靠运行的特性
  - 在关断期间真正断开输入域输出之间的连接
  - 输出过压和热关断保护
  - 输出短路保护
- 2.1mm × 1.6mm SOT583 8 引脚封装

## 2 应用

- 平板电脑（多媒体）
- 智能扬声器
- 移动 POS

## 3 说明

TPS61033X 是一款同步升压转换器。该器件可以为由多种电池和其他电源供电的便携式设备和智能设备提供电源解决方案。在整个温度范围内，TPS61033 具有 5.5A（典型值）谷值开关电流限制，TPS610333 具有 1.85A（典型值）谷值开关电流限制。

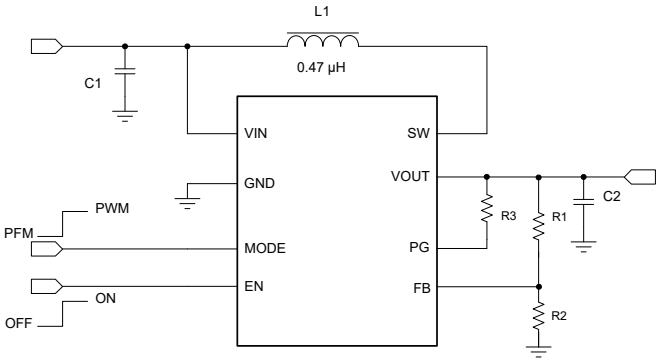
TPS61033X 使用自适应恒定导通时间谷值电流控制拓扑来调节输出电压，并在 2.4MHz 开关频率下运行。在轻负载条件下，通过配置 MODE 引脚可实现两种可选模式：自动 PFM 模式和强制 PWM 模式，以便在轻负载条件下实现效率和抗噪性平衡。在轻负载条件下，TPS61033X 通过 $V_{IN}$ 消耗 20μA 的静态电流。在关断期间，TPS61033X 与输入电源完全断开，仅消耗 0.1μA 的电流，以实现较长的电池寿命。TPS61033X 具有 5.75V 输出过压保护、输出短路保护和热关断保护。

TPS61033X 采用 2.1mm × 1.6mm SOT583 封装，最大限度地减少了外部元件的数量，因而拥有非常小巧的解决方案尺寸。

**器件信息**

| 器件型号 | 封装[1] | 封装尺寸（标称值） |
|---|---|---|
| TPS61033X | SOT583 (8) | 2.10mm × 1.20mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




**典型应用电路**

# 4 Device Comparison Table

表 4-1. Device comparison table

| PART NUMBER | Valley Switch Current Limit (typ) | Output Voltage (typ) | Spread Spectrum |
|---|---|---|---|
| TPS61033 | 5.5 A | 2.2 V ~5.5 V | NO |
| TPS610333 | 1.85 A | Fixed 5 V | NO |

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## 5 Revision History

注：以前版本的页码可能与当前版本的页码不同

**Changes from Revision C (August 2023) to Revision D (September 2023)** — **Page**

- Corrected TPS610333 Specification limits ..... 6

**Changes from Revision B (March 2023) to Revision C (August 2023)** — **Page**

- 添加了 TPS610333 器件 ..... 1

**Changes from Revision A (March 2023) to Revision B (June 2023)** — **Page**

- Changed unit in 图 7-7 to µA ..... 8
- Changed 80 mA to 800 mA in 图 9-6 ..... 19

**Changes from Revision * (October 2022) to Revision A (March 2023)** — **Page**

- 将器件状态从“预告信息”更改为“量产数据” ..... 1

# 6 Pin Configuration and Functions

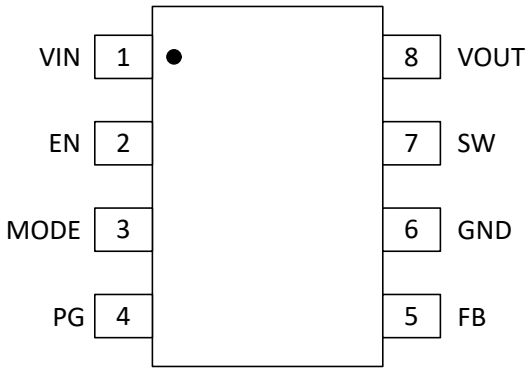



图 6-1. DRL Package 8-Pin SOT583 Top View

表 6-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | VIN | I | IC power supply input |
| 2 | EN | I | Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode. |
| 3 | MODE | I | Operation mode selection in the light load condition. When it is connected to logic high voltage, the device works in forced PWM mode. When it is connected to logic low voltage, the device works in auto PFM mode. |
| 4 | PG | O | Power good indicator and open drain output |
| 5 | FB | I | TPS61033: Voltage feedback of adjustable output voltage, when FB connect to VIN, output voltage is fixed 5.0V<br>TPS610333: Should be connected with VIN for fixed 5.0 V output voltage. |
| 6 | GND | PWR | Ground pin of the IC |
| 7 | SW | PWR | The switch pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET. |
| 8 | VOUT | PWR | Boost converter output |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Voltage range at terminals(2) | VIN, EN, FB, SW, VOUT | –0.3 | 7 | V |
| | SW spike at 10ns | –0.7 | 8 | V |
| | SW spike at 1ns | –0.7 | 9 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | | 1.8 | | 5.5 | V |
| $V_{OUT}$ | Output voltage setting range | | 2.2 | | 5.5 | V |
| L | Effective inductance range | | 0.33 | 0.47 | 1.3 | µH |
| $C_{IN}$ | Effective input capacitance range | | 1.0 | 4.7 | | µF |
| $C_{OUT}$ | Effective output capacitance range | $I_{OUT}$ <= 1A | 4 | 10 | 1000 | µF |
| | | $I_{OUT}$ > 1A | 10 | 20 | 1000 | µF |
| $T_J$ | Operating junction temperature | | –40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | TPS61033 DRL (SOT583)- 8 PINS Standard | TPS61033 DRL (SOT583)- 8 PINS EVM(2) | UNIT |
|---|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 117.5 | 65.8 | °C/W |
| $R_{\theta JC}$ | Junction-to-case thermal resistance | 40.0 | NA | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 23.0 | NA | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 2.8 | 1.0 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 22.9 | 28.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Measured on TPS61033EVM, 4-layer, 2oz copper NA PCB.

## 7.5 Electrical Characteristics

$T_J$ = –40°C to 125°C, $V_{IN}$ = 3.6 V and $V_{OUT}$ = 5.0 V. Typical values are at $T_J$ = 25°C (unless otherwise noted)

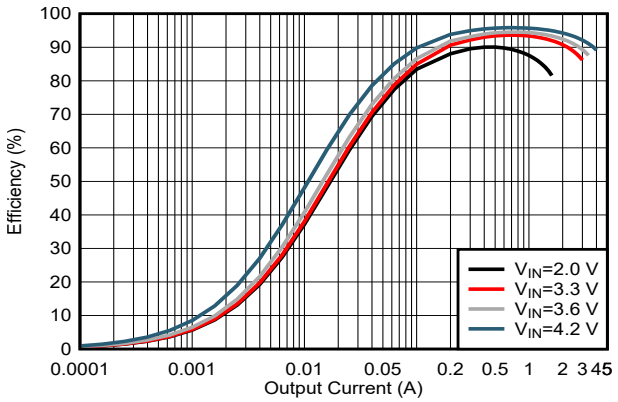
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| $V_{IN}$ | Input voltage range | | 1.8 | | 5.5 | V |
| $V_{IN\_UVLO}$ | Under-voltage lockout threshold | $V_{IN}$ rising | | 1.7 | 1.79 | V |
| | | $V_{IN}$ falling | | 1.6 | | V |
| VIN_HYS | VIN UVLO hysteresis | | | 65 | | mV |
| $I_Q$ | Quiescent current into VIN pin | IC enabled, No load, No switching $V_{IN}$ = 1.8 V to 5.5 V, $V_{FB}$ = $V_{REF}$ + 0.1 V, $T_J$ up to 125°C | 13 | 20 | 25 | µA |
| | Quiescent current into VOUT pin | IC enabled, No load, No switching $V_{OUT}$ = 2.2 V to 5.5 V, $V_{FB}$ = $V_{REF}$ + 0.1 V, $T_J$ up to 125°C | | 5.3 | 9 | µA |
| $I_{SD}$ | Shutdown current into VIN and SW pin | IC disabled, $V_{IN}$ = $V_{SW}$ = 3.6 V, $T_J$ = 25°C | | 0.1 | 0.2 | µA |
| **OUTPUT** | | | | | | |
| $V_{OUT}$ | Output voltage setting range | | 2.2 | | 5.5 | V |
| $V_{OUT}$ (fixed 5V) | Fixed output voltage | FB connected to VIN<br>VIN < VOUT, PWM mode | 4.93 | 5 | 5.07 | V |
| $V_{REF}$ | Reference voltage at the FB pin | PWM mode | 591 | 600 | 609 | mV |
| $V_{REF}$ | Reference voltage at the FB pin | PFM mode | | 606 | | mV |
| $V_{OVP}$ | Output over-voltage protection threshold | $V_{OUT}$ rising | 5.5 | 5.75 | 6.0 | V |
| $V_{OVP\_HYS}$ | Over-voltage protection hysteresis | | | 0.11 | | V |
| $I_{FB\_LKG}$ | Leakage current at FB pin | $T_J$ = 25°C | | 4 | 25 | nA |
| $I_{FB\_LKG}$ | Leakage current at FB pin | $T_J$ = 125°C | | 5 | 30 | nA |
| $I_{VOUT\_LKG}$ | Leakage current into VOUT pin | IC disabled, $V_{IN}$ = 0 V, $V_{SW}$ = 0 V, $V_{OUT}$ = 5.5 V, $T_J$ = 25°C | | 0.2 | 0.5 | µA |
| $t_{ss}$ | Soft startup time | Internal SS ramp time | | 0.86 | | ms |
| **POWER SWITCH** | | | | | | |
| $R_{DS(on)}$ | High-side MOSFET on resistance | $V_{OUT}$ = 5.0 V | | 46 | | mΩ |
| $R_{DS(on)}$ | Low-side MOSFET on resistance | $V_{OUT}$ = 5.0 V | | 25 | | mΩ |
| $f_{SW}$ | Switching frequency | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.0 V, PWM mode | 2.0 | 2.4 | 2.8 | MHz |
| $t_{ON\_min}$ | Minimum on time | | 20 | 48 | 65 | ns |
| $t_{OFF\_min}$ | Minimum off time | | | 35 | 70 | ns |
| $I_{LIM\_SW}$ | Valley current limit | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.0 V TPS61033 | 4.7 | 5.5 | 6.1 | A |
| $I_{LIM\_SW}$ | Valley current limit | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.0 V TPS610333 | 1.55 | 1.85 | 2.25 | A |
| $I_{REVERSE}$ | Reverse current limit (MODE=1) | $V_{IN}$ = 3.6 V, $V_{OUT}$ = 5.0 V; MODE = 1 | | -1.4 | | A |
| $I_{LIM\_CHG}$ | Pre-charge current | $V_{IN}$ = 1.8 - 5.5 V, $V_{OUT}$ < 0.4 V | | 330 | | mA |
| $I_{LIM\_CHG\_max}$ | Maximum pre-charge current | $V_{IN}$ = 2.4 V, $V_{OUT}$ > 0.4 V ; TPS610333 | | 800 | 1100 | mA |
| **LOGIC INTERFACE** | | | | | | |
| $V_{EN\_H}$ | EN logic high threshold | $V_{IN}$ > 1.8 V or $V_{OUT}$ > 2.2 V | | | 1.2 | V |
| $V_{EN\_L}$ | EN logic low threshold | $V_{IN}$ > 1.8 V or $V_{OUT}$ > 2.2 V | 0.4 | | | V |
| $V_{MODE\_H}$ | MODE Logic high threshold | $V_{IN}$ > 1.8 V or $V_{OUT}$ > 2.2 V | | | 1.2 | V |
| $V_{MODE\_L}$ | MODE Logic Low threshold | $V_{IN}$ > 1.8 V or $V_{OUT}$ > 2.2 V | 0.4 | | | V |
| $R_{DOWN}$ | EN pins internal pull-down resistor | | | 10 | | MΩ |
| $R_{DOWN}$ | MODE pins internal pull-down resistor | | | 1 | | MΩ |
| **POWER GOOD** | | | | | | |
| $PGD_{OV}$ | PGOOD upper threshold | % of VOUT setting | 105 | 107 | 110 | % |
| $PGD_{UV}$ | PGOOD lower threshold | % of VOUT setting | 91 | 93 | 95 | % |
| $PGD_{HYST}$ | PGOOD upper threshold (rising&falling) | % of VOUT setting | | 2.5 | | % |
| $t_{PGDFLT(rise)}$ | Delay time to PGOOD high signal | | | 1.3 | | ms |
| $t_{PGDFLT(fall)}$ | Glitch filter time of PGOOD | | | 33 | | µs |
| **PROTECTION** | | | | | | |

$T_J$ = –40°C to 125°C, $V_{IN}$ = 3.6 V and $V_{OUT}$ = 5.0 V. Typical values are at $T_J$ = 25°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{SD}$ | Thermal shutdown threshold | $T_J$ rising | | 170 | | °C |
| $T_{SD}$ | Thermal shutdown threshold | $T_J$ falling | | 155 | | °C |
| $T_{SD\_HYS}$ | Thermal shutdown hysteresis | $T_J$ falling below $T_{SD}$ | | 15 | | °C |

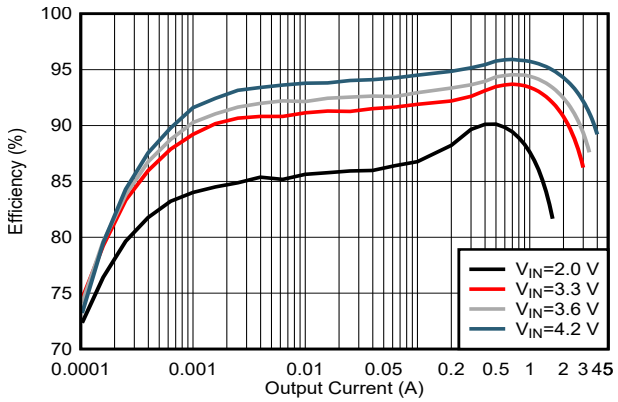
## 7.6 Typical Characteristics

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 5 V, $T_J$ = 25°C, unless otherwise noted



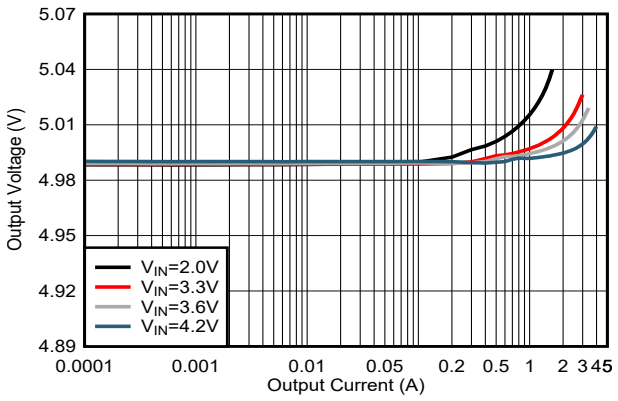

$V_{IN}$ = 2.0 V, 3.3 V, 3.6 V, 4.2 V; L = 0.47 µH, PWM Mode

**图 7-1. Efficiency vs Output Current $V_{OUT}$ = 5 V**



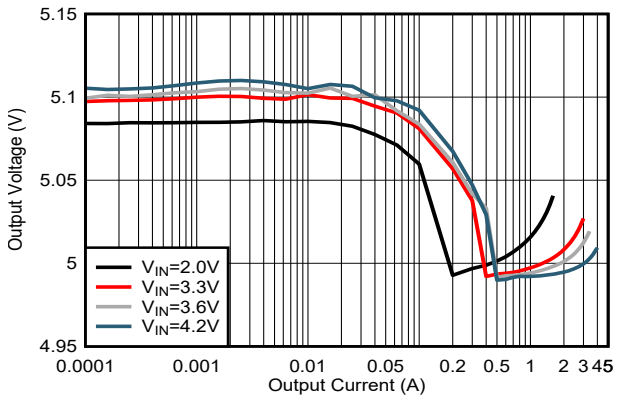

$V_{IN}$ = 2.0 V, 3.3 V, 3.6 V, 4.2 V; L = 0.47 µH, Auto PFM Mode

**图 7-2. Efficiency vs Output Current $V_{OUT}$ = 5 V**



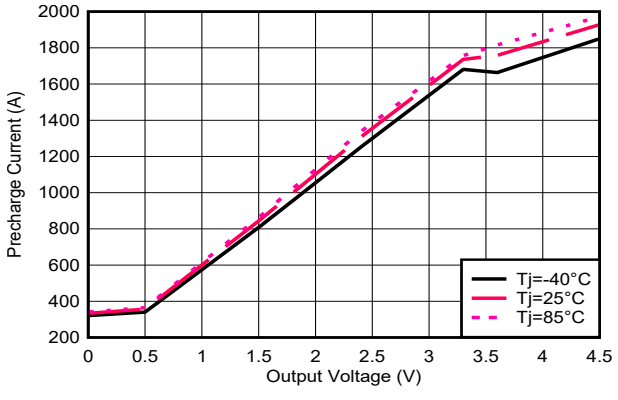

$V_{IN}$ = 2.0 V, 3.3 V, 3.6 V, 4.2 V; $V_{OUT}$ = 5 V

**图 7-3. Load Regulation in Auto PWM**



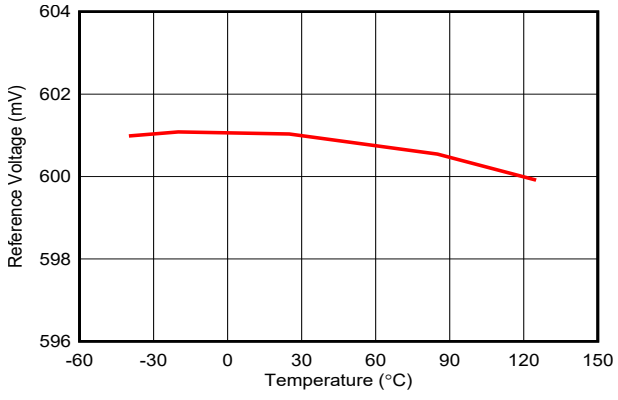

$V_{IN}$ = 2.0 V, 3.3 V, 3.6 V, 4.2 V; $V_{OUT}$ = 5 V

**图 7-4. Load Regulation in Forced PFM**



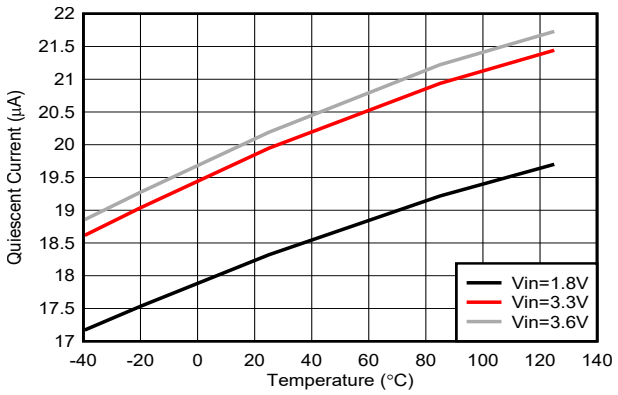

$V_{IN}$ = 3.3 V; $V_{OUT}$ = 0 V to 4.5 V

**图 7-5. Pre-charge Current vs Output Voltage**



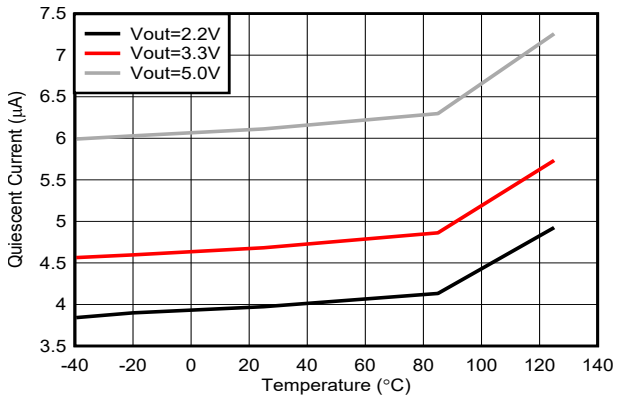

$V_{IN}$ = 3.3 V; $V_{OUT}$ = 5 V, $T_J$ = –40°C to +125°C

**图 7-6. Reference Voltage vs Temperature**



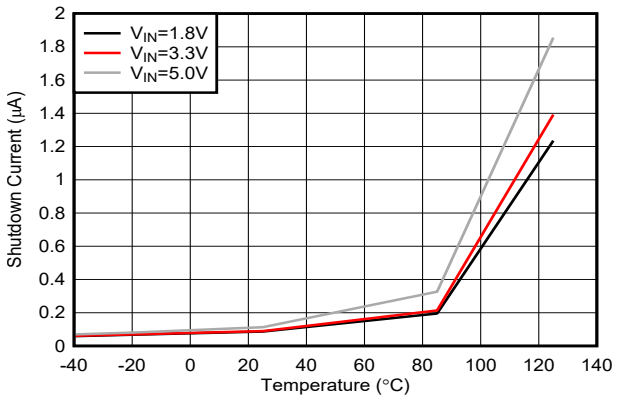

$V_{IN}$ = 1.8 V, 3.3 V 3.6 V; $V_{OUT}$ = 5 V, $T_J$ = –40°C to +125°C, No switching

**图 7-7. Quiescent Current into VIN vs Temperature**



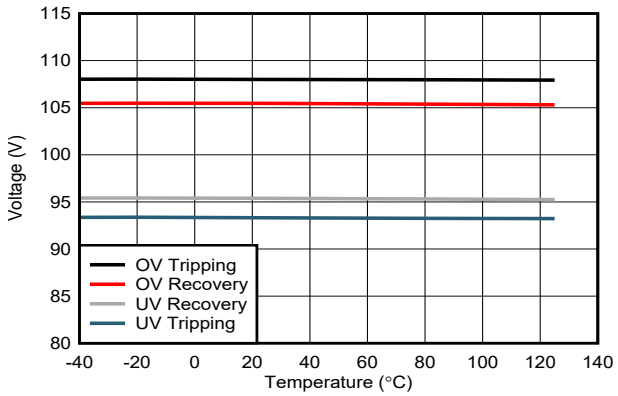

$V_{IN}$ = 1.8 V; $V_{OUT}$ = 2.2 V, 3.3 V, 5 V, $T_J$ = –40°C to +125°C, No switching

**图 7-8. Quiescent Current into VOUT vs Temperature**




$V_{IN}$ = $V_{SW}$ = 1.8 V, 3.3 V, 5 V; $V_{OUT}$ = 0 V; $T_J$ = –40°C to +125°C

**图 7-9. Shutdown Current vs Temperature**




$V_{IN}$ = 3.6 V; $V_{OUT}$ = 5 V; $T_J$ = –40°C to +125°C

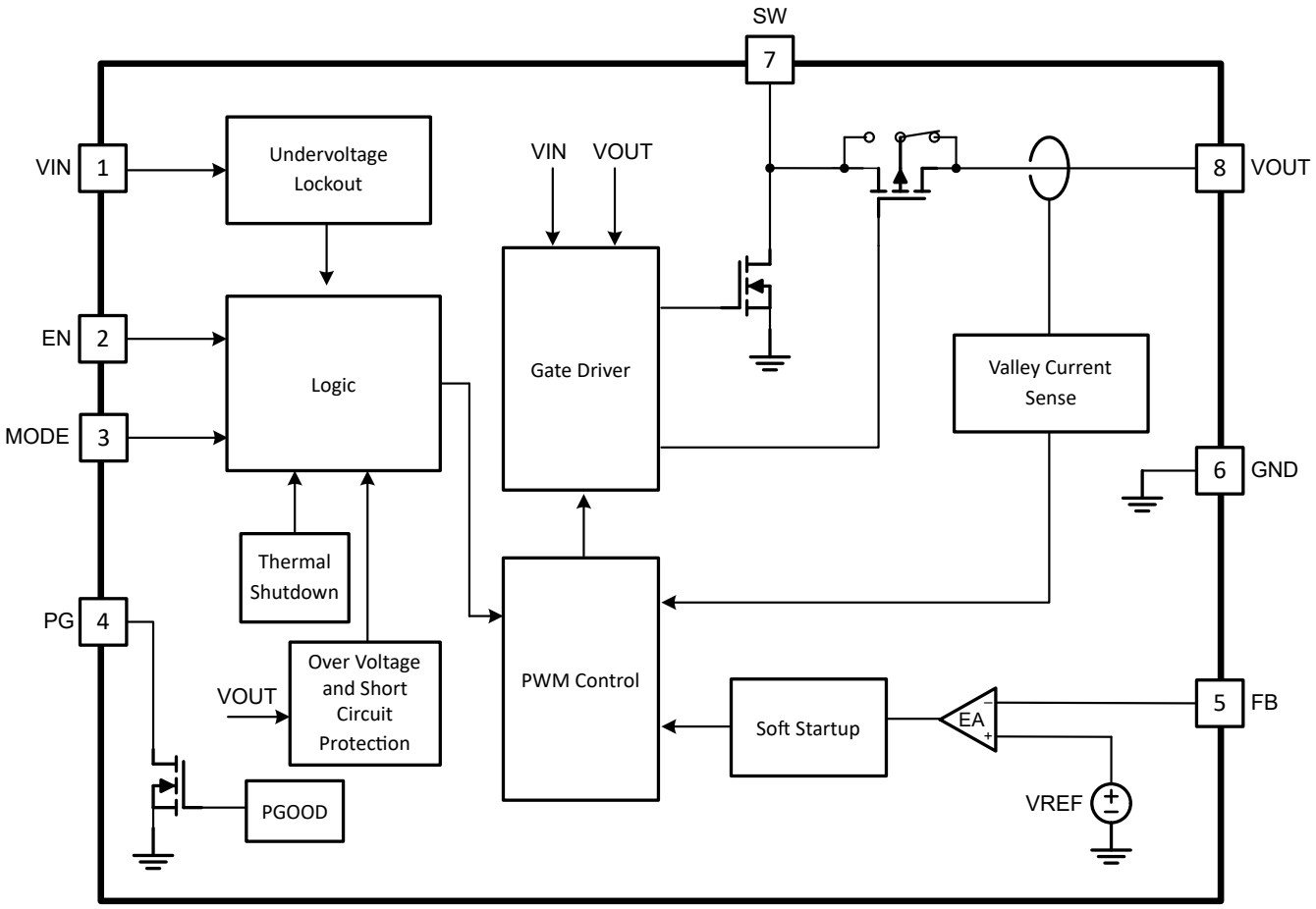
**图 7-10. PGOOD threshold vs Temperature**

# 8 Detailed Description

## 8.1 Overview

The TPS61033 is a fully-integrated synchronous boost converter and operates from an input voltage supply range from 1.8 V to 5.5 V with 5.5-A (typical) valley switch current limit. The TPS61033 operates at 2.4-MHz switching frequency. There are two optional modes at light load by configuring the MODE pin: auto PFM mode and forced PWM to balance the efficiency and noise immunity in light load. The TPS61033 consumes an 20- μA quiescent current from VIN at light load condition. During shutdown, the TPS61033 is completely disconnected from the input power and only consumes a 0.1- μA current to achieve long battery life. During PWM operation, the converter uses adaptive constant on-time valley current mode control scheme to achieve excellent line regulation and load regulation and allows the use of a small inductor and ceramic capacitors. Internal loop compensation simplifies the design process while minimizing the number of external components.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Undervoltage Lockout

The TPS61033 has a built-in undervoltage lockout (UVLO) circuit to ensure the device working properly. When the input voltage is above the UVLO rising threshold of 1.7 V (typical), the TPS61033 can be enabled to boost the output voltage. The device is disabled when the falling voltage at the VIN pin trips the UVLO falling threshold, which is 1.6 V (typical). A hysteresis of 100 mV (typical) is added so that the device cannot be enabled again until the input voltage exceeds 1.7 V (typical). This function is implemented to prevent the device from malfunctioning when the input voltage is between UVLO rising and falling threshold.

### 8.3.2 Enable and Soft Start

When the input voltage is above the UVLO rising threshold and the EN pin is pulled to a voltage above 1.2 V, the TPS61033 is enabled and starts up. To minimize the inrush current during start up, the TPS61033 has a soft start up function. At the beginning, the TPS61033 enters pre-charge phase and charges the output capacitors with a current of approximately 330 mA when the output voltage is below 0.4 V. When the output voltage is charged above 0.4 V, the output current is changed to having output current capability to drive the 2-Ω resistance load. To minimize the inrush current further, the TPS610333 has a maximum pre-charge current of 900 mA(typical). After the output voltage reaches the input voltage, the TPS61033 starts switching, and the reference voltage ramps up a 0.8 mV/μs. When the voltage at the EN pin is below 0.4 V, the internal enable comparator turns the device into shutdown mode. In the shutdown mode, the device is entirely turned off. The output is disconnected from input power supply.

### 8.3.3 Setting the Output Voltage

There are two ways to set the output voltage of the TPS61033: adjustable or fixed. If the FB is connected to VIN, the TPS61033 works as a fixed 5.0-V output voltage version, the TPS61033 uses the internal resistor divider.

The output voltage is also can be set by an external resistor divider (R1, R2 in 图 9-1). When the output voltage is regulated, the typical voltage at the FB pin is $V_{REF}$. Thus the resistor divider is determined by 方程式 5.

$$R1 = \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \tag{1}$$

where

- $V_{OUT}$ is the regulated output voltage
- $V_{REF}$ is the internal reference voltage at the FB pin

TPS610333 can only support fixed 5.0-V output voltage, so FB should be connected with VIN rather than external resistor divider.

### 8.3.4 Current Limit Operation

The TPS61033 uses a valley current limit sensing scheme. Current limit detection occurs during the off-time by sensing of the voltage drop across the synchronous rectifier.

When the load current is increased such that the inductor current is above the current limit within the whole switching cycle time, the off-time is increased to allow the inductor current to decrease to this threshold before the next on-time begins (so called frequency foldback mechanism). When the current limit is reached, the output voltage decreases during further load increase.

The maximum continuous output current ($I_{OUT(LC)}$), before entering current limit (CL) operation, can be defined by 方程式 2.

$$I_{OUT(CL)} = (1 - D) \times \left( I_{LIM} + \frac{1}{2} \Delta I_{L(P-P)} \right) \tag{2}$$

where

- D is the duty cycle
- $\Delta I_{L(P-P)}$ is the inductor ripple current

The duty cycle can be estimated by 方程式 3.

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \quad (3)$$

where

- $V_{OUT}$ is the output voltage of the boost converter
- $V_{IN}$ is the input voltage of the boost converter
- $\eta$ is the efficiency of the converter, use 90% for most applications

The peak-to-peak inductor ripple current is calculated by 方程式 4.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (4)$$

where

- L is the inductance value of the inductor
- $f_{SW}$ is the switching frequency
- D is the duty cycle
- $V_{IN}$ is the input voltage of the boost converter

### 8.3.5 Pass-Through Operation

When the input voltage is higher than the setting output voltage, the output voltage is higher than the target regulation voltage, the device works in pass-through mode. When the output voltage is 101% of the setting target voltage, the TPS61033 stops switching and fully turns on the high-side PMOS FET. The output voltage is the input voltage minus the voltage drop across the DCR of the inductor and the $R_{DS(on)}$ of the PMOS FET. When the output voltage drops below the 97% of the setting target voltage as the input voltage declines or the load current increases, the TPS61033 resumes switching again to regulate the output voltage.

### 8.3.6 Power Good Indicator

The TPS61033 integrates a power good indicator to simplify sequencing and supervision. The power-good output consists of an open-drain NMOS, requiring an external pullup resistor connect to a suitable voltage supply. The PG pin goes high with a typical 1.3 ms delay time after VOUT is between 93% (typical) and 107% (typical) of the target output voltage. When the output voltage is out of the target output voltage window, the PG pin immediately goes low with a 33 μs deglitch filter delay. This deglitch filter also prevents any false pulldown of the PGOOD due to transients. When EN is pulled low, the PG pin is also forced low with a 33 μs deglitch filter delay. If not used, the PG pin can be left floating or connected to GND.

### 8.3.7 Implement Output Discharge by PG function

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage and to let the output voltage close to 0 V quickly when the device is being disabled. TPS61033 can implement output discharge function by PG function that requires a $R_{Dummy}$ resistor connected between PG pin and Vout pin. PG is an open drain NMOS architecture with up to 50 mA current capability, the PG pin becomes logic high when the output voltage reaches the target value, so the dummy load resistor doesn't lead any power loss during normal operation. When the EN pin gets low, the TPS61033 is disabled and meanwhile the PG pin gets low with a typical 33 μs glitch time ($t_{glitch}$). With PG pin keeps low, the $R_{Dummy}$ works as a dummy load to discharge output voltage. Changing $R_{Dummy}$ can adjust the output discharge rate.

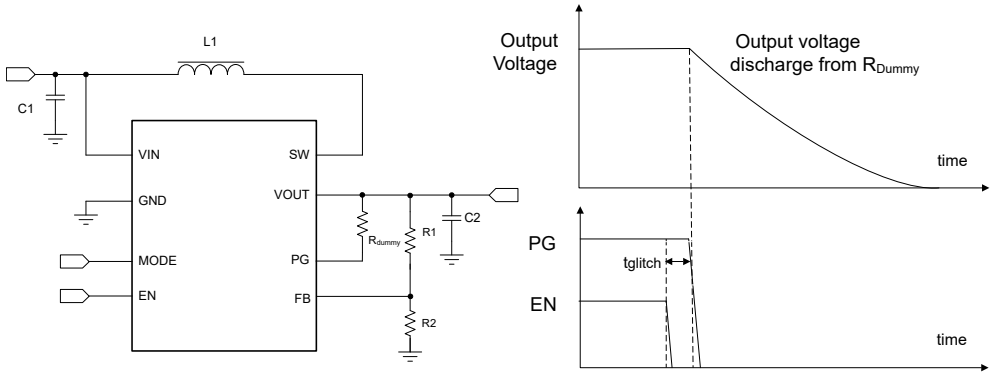



**图 8-1. Implement Output Discharge by PG function**

### 8.3.8 Overvoltage Protection

The TPS61033 has an output overvoltage protection (OVP) to protect the device if the external feedback resistor divider is wrongly populated. When the output voltage is above 5.75 V typically, the device stops switching. Once the output voltage falls 0.1 V below the OVP threshold, the device resumes operating again.

### 8.3.9 Output Short-to-Ground Protection

The TPS61033 starts to limit the output current when the output voltage is below 1.8 V. The lower the output voltage reaches, the smaller the output current is. When the VOUT pin is short to ground, and the output voltage becomes less than 0.4 V, the output current is limited to approximately 330 mA. Once the short circuit is released, the TPS61033 goes through the soft start-up again to the regulated output voltage.

### 8.3.10 Thermal Shutdown

The TPS61033 goes into thermal shutdown once the junction temperature exceeds 170°C. When the junction temperature drops below the thermal shutdown recovery temperature, typically 155°C, the device starts operating again.

## 8.4 Device Functional Modes

TPS61033 has two optional modes in light load by configuring the MODE pin: auto PFM mode and forced PWM to balance the efficiency and noise immunity in light load.

### 8.4.1 PWM Mode

The TPS61033 uses a quasi-constant 2.4-MHz frequency pulse width modulation (PWM) at moderate to heavy load current. Based on the input voltage to output voltage ratio, a circuit predicts the required on-time. At the beginning of the switching cycle, the NMOS switching FET. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the on-time expires, the main switch NMOS FET is turned off, and the rectifier PMOS FET is turned on. The inductor transfers its stored energy to replenish the output capacitor and supply the load. The inductor current declines because the output voltage is higher than the input voltage. When the inductor current hits the valley current threshold determined by the output of the error amplifier, the next switching cycle starts again.

The TPS61033 has a built-in compensation circuit that can accommodate a wide range of input voltage, output voltage, inductor value, and output capacitor value for stable operation.

### 8.4.2 Power-Save Mode

The TPS61033 integrates a power-save mode with PFM to improve efficiency at light load. When the load current decreases, the inductor valley current set by the output of the error amplifier no longer regulates the output voltage. When the inductor valley current hits the low limit, the output voltage exceeds the setting voltage as the load current decreases further. When the FB voltage hits the PFM reference voltage, the TPS61033 goes into the power-save mode. In the power-save mode, when the FB voltage rises and hits the PFM reference voltage, the device continues switching for several cycles because of the delay time of the internal comparator — then it stops switching. The load is supplied by the output capacitor, and the output voltage declines. When the FB voltage falls below the PFM reference voltage, after the delay time of the comparator, the device starts switching again to ramp up the output voltage.

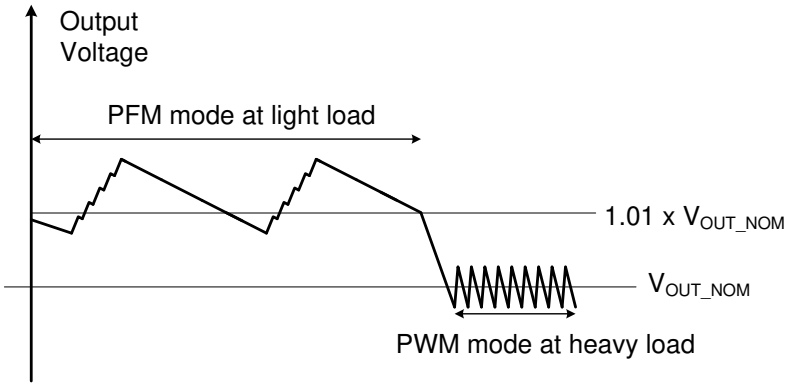



**图 8-2. Output Voltage in PWM Mode and PFM Mode**

# 9 Application and Implementation

**备注**

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

## 9.1 Application Information

The TPS61033 is a synchronous boost converter designed to operate from an input voltage supply range between 1.8 V and 5.5 V with a 5.5-A (typical) valley switch current limit. The TPS61033 typically operates at a quasi-constant 2.4-MHz frequency PWM at moderate-to-heavy load currents. At light load currents, the TPS61033 converter operates in power-save mode with PFM to achieve high efficiency over the entire load current range.

## 9.2 Typical Application

The TPS61033 provides a power supply solution for portable devices powered by batteries. With 5.5-A (typical) switch current capability, the TPS61033 can output 5 V and 2 A from a single-cell Li-ion battery.

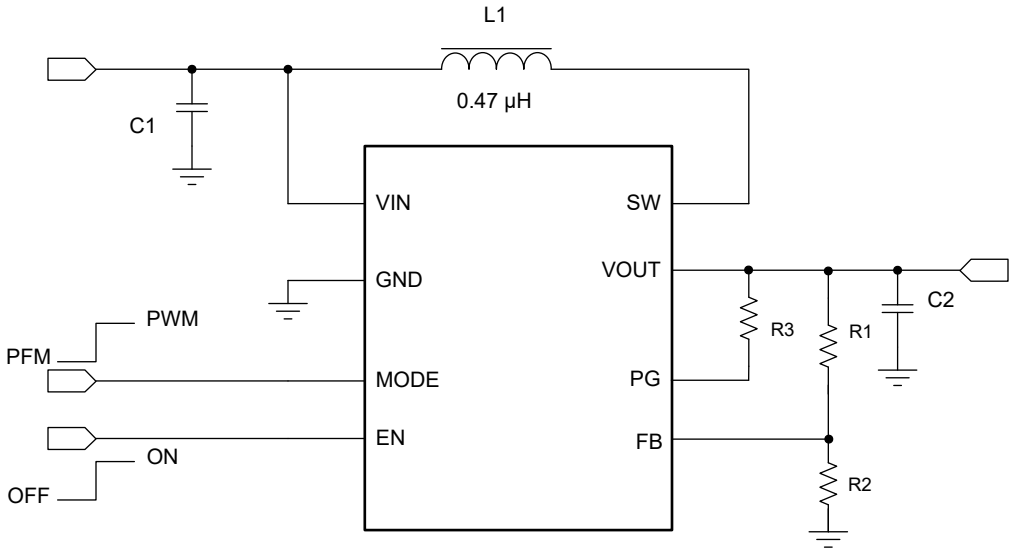



**图 9-1. Li-ion Battery to 5-V Boost Converter**

### 9.2.1 Design Requirements

The design parameters are listed in 表 9-1.

**表 9-1. Design Parameters**

| PARAMETERS | VALUES |
|---|---|
| Input voltage | 3.0 V to 4.35 V |
| Output voltage | 5 V |
| Output current | 2.0 A |

### 9.2.2 Detailed Design Procedure

#### *9.2.2.1 Setting the Output Voltage*

The output voltage is set by an external resistor divider (R1, R2 in 图 9-1). When the output voltage is regulated, the typical voltage at the FB pin is $V_{REF}$. Thus the resistor divider is determined by 方程式 5.

$$R1 = \left( \frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \quad (5)$$

where

- $V_{OUT}$ is the regulated output voltage
- $V_{REF}$ is the internal reference voltage at the FB pin

For the best accuracy, keep R2 smaller than 300 kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 towards a lower value increases the immunity against noise injection. Changing the R2 towards a higher value reduces the quiescent current for achieving highest efficiency at low load currents.

#### *9.2.2.2 Inductor Selection*

Because the selection of the inductor affects steady-state operation, transient behavior, and loop stability. The inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance (DCR).

The TPS61033 is designed to work with inductor values between 0.37 µH and 2.9 µH. Follow 方程式 6 to 方程式 8 to calculate the inductor peak current for the application. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margins, choose the inductor value with –30% tolerances, and low power-conversion efficiency for the calculation.

In a boost regulator, the inductor dc current can be calculated by 方程式 6.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (6)$$

where

- $V_{OUT}$ is the output voltage of the boost converter
- $I_{OUT}$ is the output current of the boost converter
- $V_{IN}$ is the input voltage of the boost converter
- $\eta$ is the power conversion efficiency, use 90% for most applications

The inductor ripple current is calculated by 方程式 7.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (7)$$

where

- D is the duty cycle, which can be calculated by 方程式 3
- L is the inductance value of the inductor
- $f_{SW}$ is the switching frequency
- $V_{IN}$ is the input voltage of the boost converter

Therefore, the inductor peak current is calculated by 方程式 8.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (8)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. The

saturation current of the inductor must be higher than the calculated peak inductor current. 表 9-2 lists the recommended inductors for the TPS61033.

**表 9-2. Recommended Inductors for the TPS61033**

| PART NUMBER(1) | L (µH) | DCR MAX (mΩ) | SATURATION CURRENT (A) | SIZE (LxWxH) | VENDOR |
|---|---|---|---|---|---|
| XGL4020-471MEC | 0.47 | 5.1 | 6.1 | 4 x 4 x 2.1 | Coilcraft |
| XGL4020-102MEC | 1 | 9.0 | 3.8 | 4 x 4 x 2.1 | Coilcraft |

(1) See *Third-party Products* disclaimer

#### 9.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. The ripple voltage is related to capacitor capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple voltage can be calculated by 方程式 9.

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \quad (9)$$

where

- $D_{MAX}$ is the maximum switching duty cycle
- $V_{RIPPLE}$ is the peak-to-peak output ripple voltage
- $I_{OUT}$ is the maximum output current
- $f_{SW}$ is the switching frequency

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used. The output peak-to-peak ripple voltage caused by the ESR of the output capacitors can be calculated by 方程式 10.

$$V_{RIPPLE(ESR)} = I_{L(P)} \times R_{ESR} \quad (10)$$

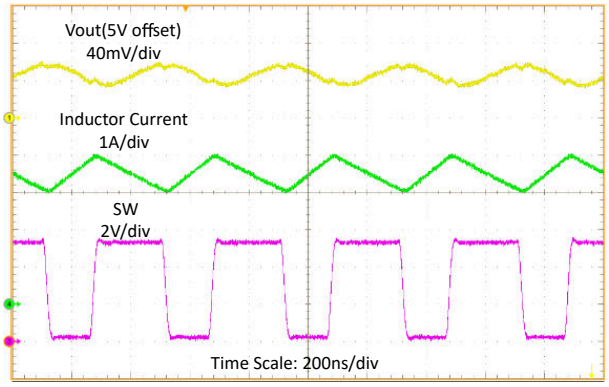
Take care when evaluating the derating of a ceramic capacitor under dc bias voltage, aging, and ac signal. For example, the dc bias voltage can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage. Increasing the output capacitor makes the output ripple voltage smaller in PWM mode.

TI recommends using the X5R or X7R ceramic output capacitor in the range of 4-µF to 1000-µF effective capacitance. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Increasing the output capacitor makes the output ripple voltage smaller in PWM mode.

#### 9.2.2.4 Input Capacitor Selection

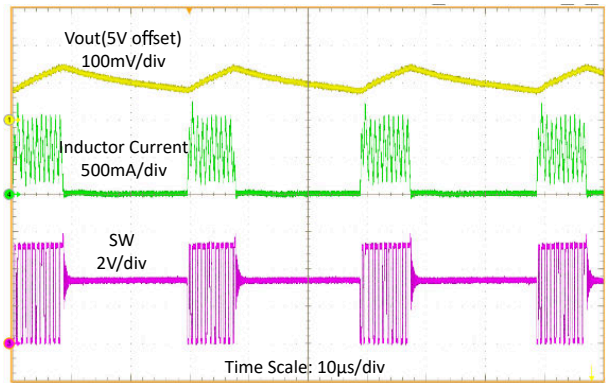
Multilayer X5R or X7R ceramic capacitors are excellent choices for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 10-µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or even damage the part. In this circumstance, place additional bulk capacitance (tantalum or aluminum electrolytic capacitor) between ceramic input capacitor and the power source to reduce ringing that can occur between the inductance of the power source leads and ceramic input capacitor.

### 9.2.3 Application Curves



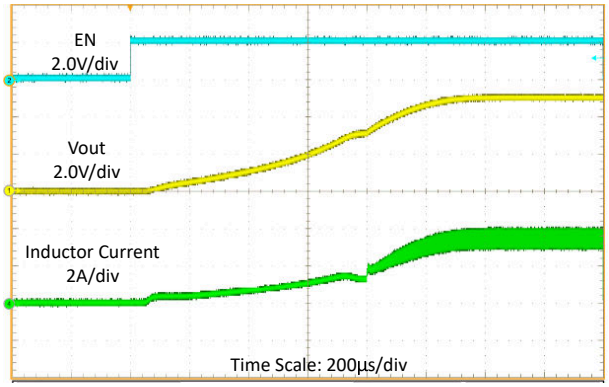

$V_{IN}$ = 3.3 V, $V_{OUT}$ = 5 V, $I_{OUT}$ = 2 A

**图 9-2. Switching Waveform at Heavy Load**



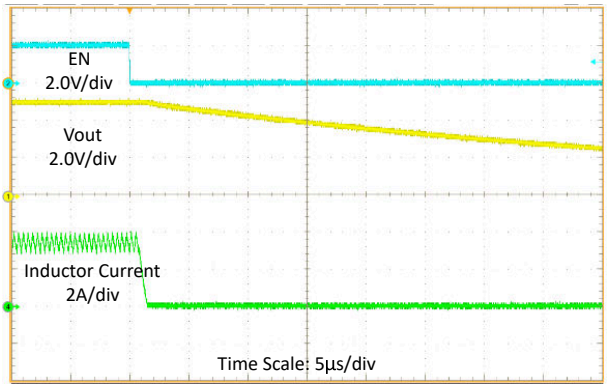

$V_{IN}$ = 3.3 V, $V_{OUT}$ = 5 V, $I_{OUT}$ = 100 mA

**图 9-3. Switching Waveform at Light Load**



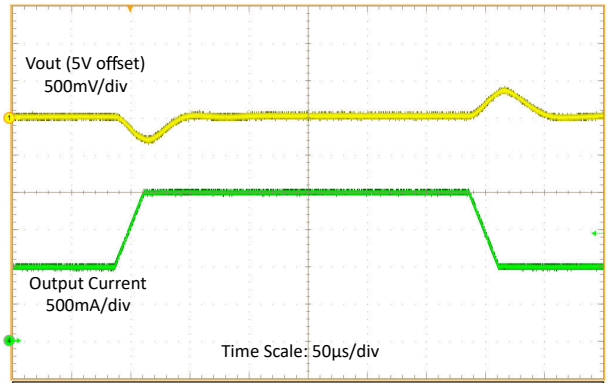

$V_{IN}$ = 3.3 V, $V_{OUT}$ = 5 V, 2.5-Ω resistance load

**图 9-4. Start-up Waveform**



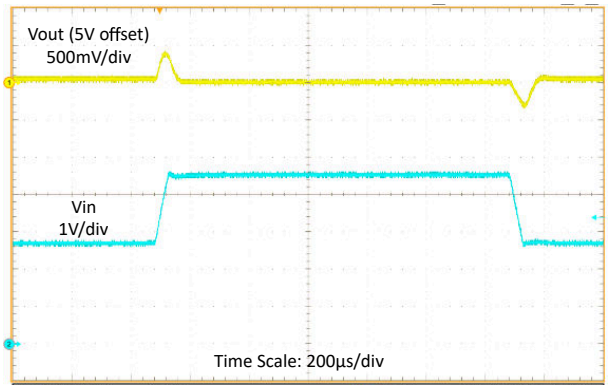

$V_{IN}$ = 3.3 V, $V_{OUT}$ = 5 V, 2.5-Ω resistance load

**图 9-5. Shutdown Waveform**



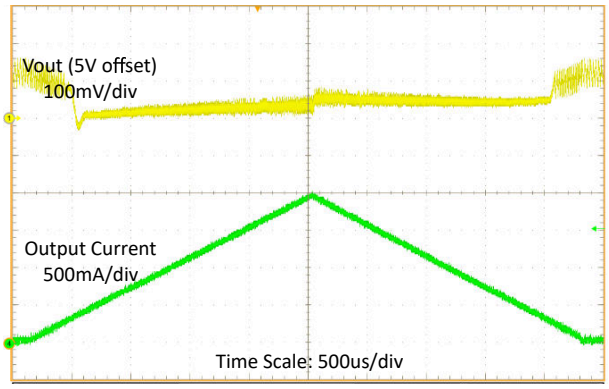

$V_{IN}$ = 3.3 V, $V_{OUT}$ = 5 V, $I_{OUT}$ = 1 A to 2 A with 20-µs slew rate

**图 9-6. Load Transient**



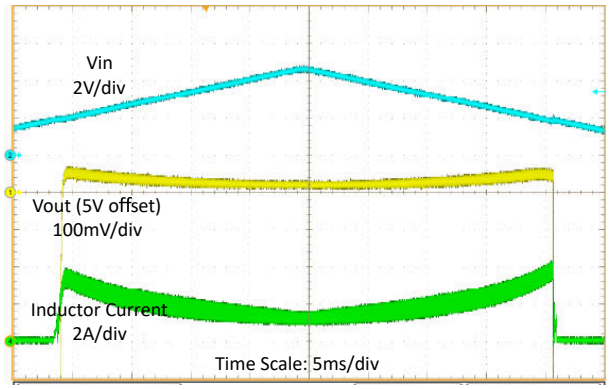

$V_{IN}$ = 2.7 V to 4.5 V with 20-µs slew rate, $V_{OUT}$ = 5 V, $I_{OUT}$ = 2 A

**图 9-7. Line Transient**



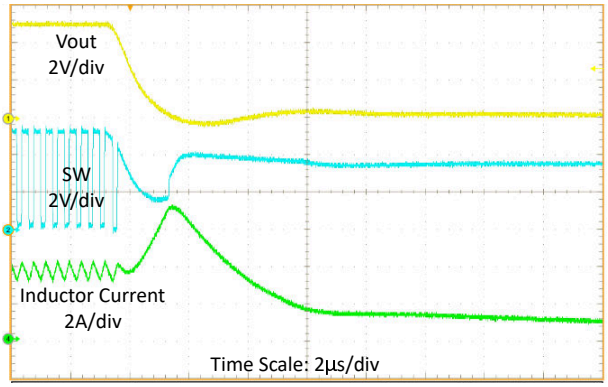

$V_{IN}$ = 3.3 V, $V_{OUT}$ = 5 V, $I_{OUT}$ = 50 mA to 2 A Sweep

**图 9-8. Load Sweep**



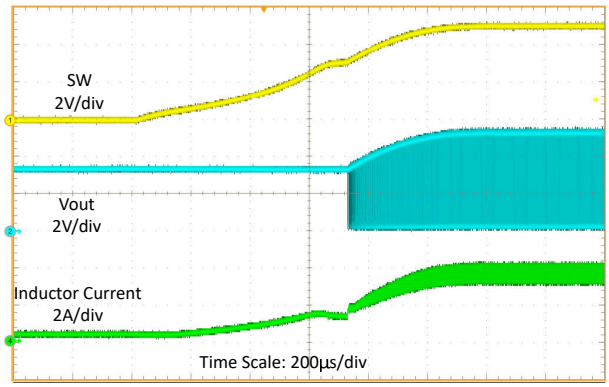

$V_{IN}$ = 1 V to 4.5 V Sweep, $V_{OUT}$ = 5 V, $I_{OUT}$ = 1 A

**图 9-9. Line Sweep**




$V_{IN}$ = 3.3 V, $V_{OUT}$ = 5 V, $I_{OUT}$ = 2 A

**图 9-10. Output Short Protection (Entry)**




$V_{IN}$ = 3.3 V, $V_{OUT}$ = 5 V, $I_{OUT}$ = 2 A

**图 9-11. Output Short Protection (Recover)**

## 9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.8 V to 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 100 µF. Output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TPS61033.

## 9.4 Layout

### 9.4.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If the layout is not carefully done, the regulator suffers from instability and noise problems. To maximize efficiency, switch rise and fall time are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize interplane coupling. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise and fall time and must be kept as short as possible. Therefore, the output capacitor not only must be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin.

For better thermal performance, TI suggest to make copper polygon connected with each pin bigger.

### 9.4.2 Layout Example

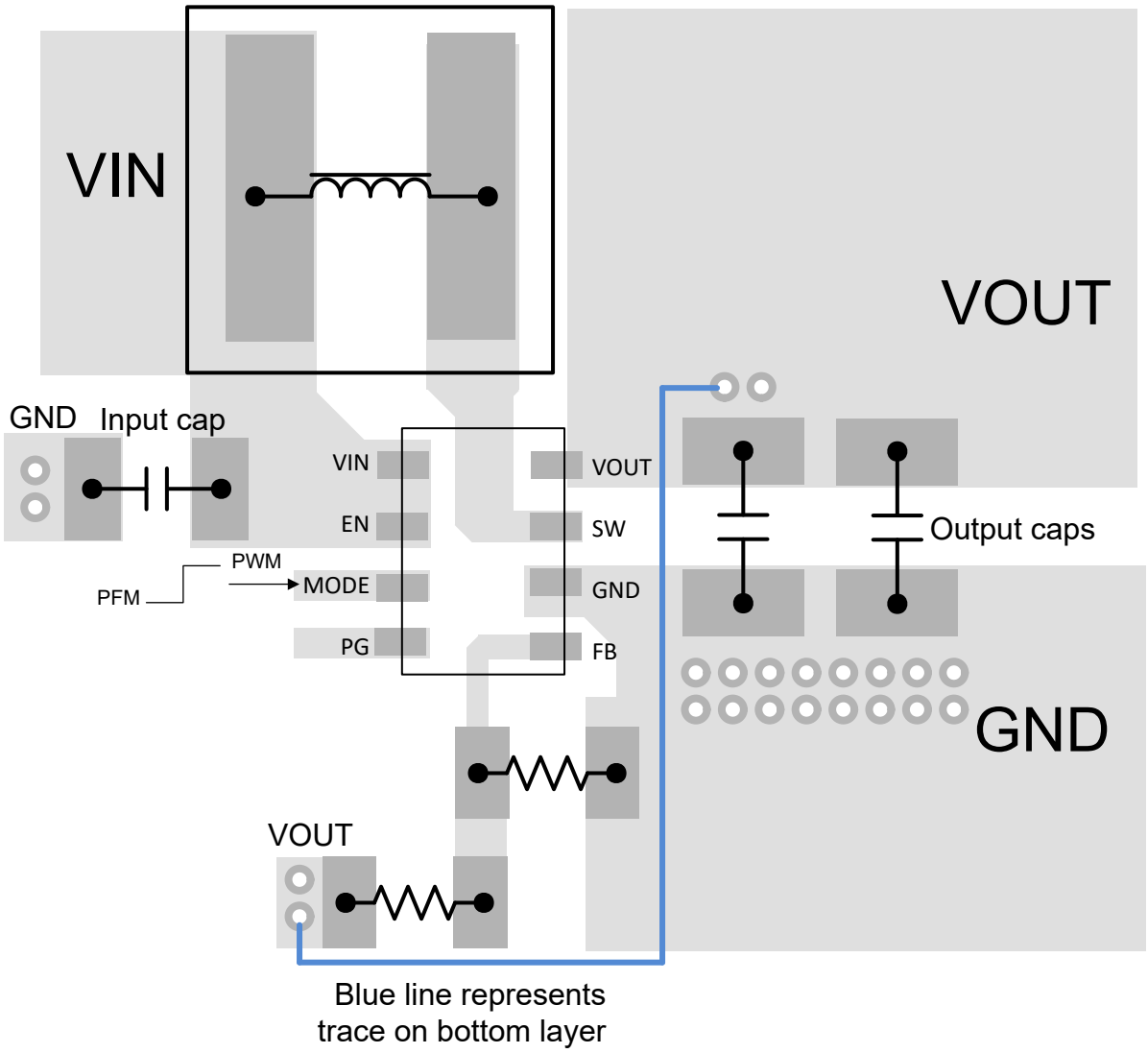



图 9-12. Layout Example

### 9.4.3 Thermal Considerations

Restrict the maximum IC junction temperature to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using 方程式 11.

$$P_{D(max)} = \frac{125 - T_A}{R_{\theta JA}} \tag{11}$$

where

- $T_A$ is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the junction-to-ambient thermal resistance given in *节 9.4.3*

The TPS61033 comes in a SOT583 package. The real junction-to-ambient thermal resistance of the package greatly depends on the PCB type, layout. Using larger and thicker PCB copper for the power pads (GND, SW, and VOUT) to enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also improves the thermal capability.

# 10 Device and Documentation Support

## 10.1 Device Support

### 10.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

## 10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 10.6 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS610333DRLR | ACTIVE | SOT-5X3 | DRL | 8 | 4000 | RoHS & Green | Call TI \| SN | Level-1-260C-UNLIM | -40 to 125 | 0333 | Samples |
| TPS61033DRLR | ACTIVE | SOT-5X3 | DRL | 8 | 4000 | RoHS & Green | Call TI \| SN | Level-1-260C-UNLIM | -40 to 125 | 033 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

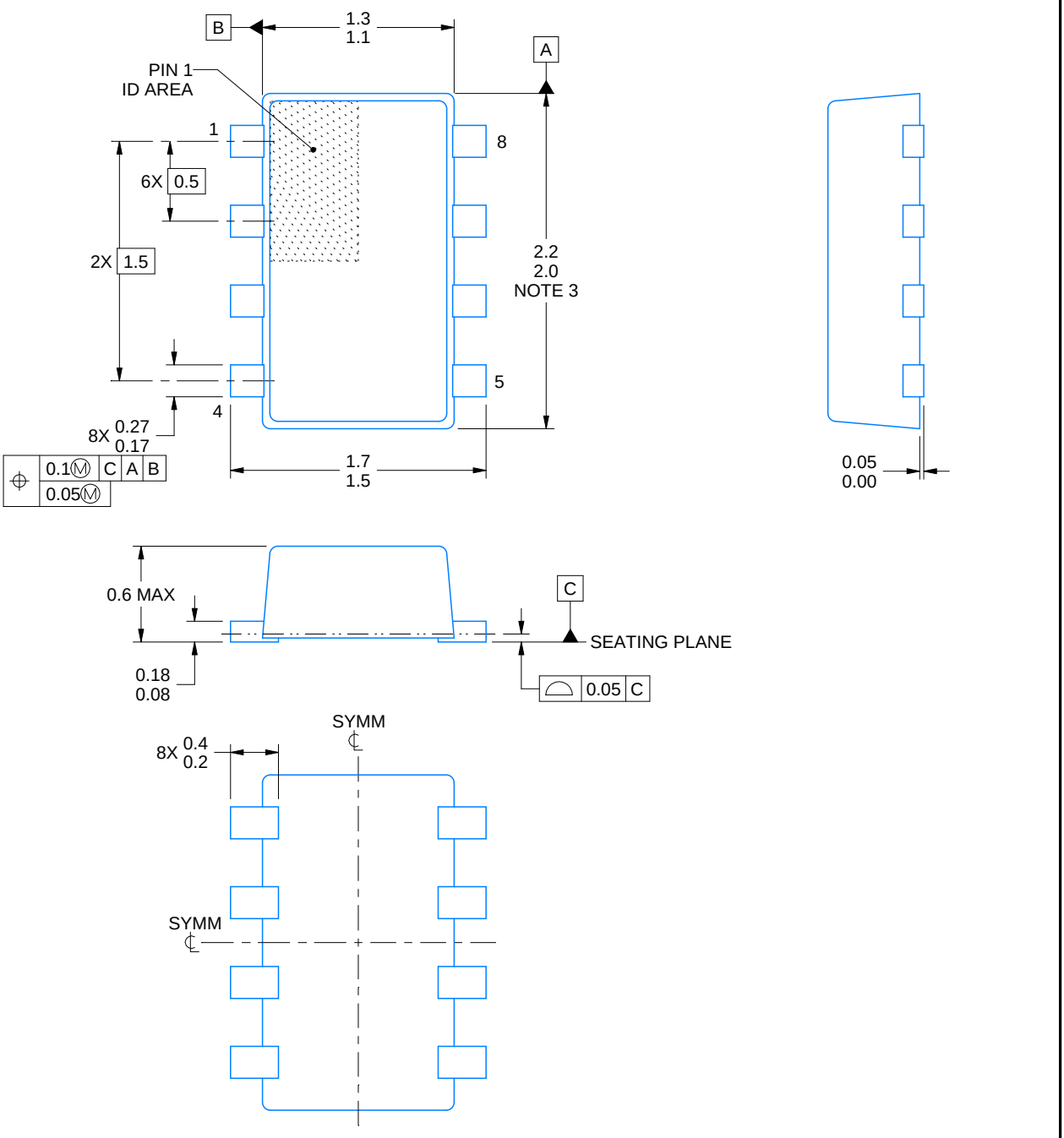
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE OUTLINE

## DRL0008A

## SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE

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NOTES:

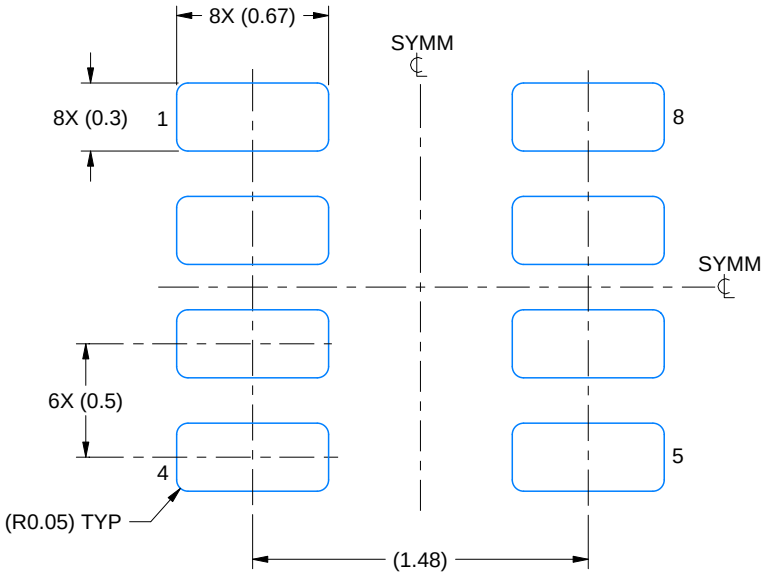
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

# EXAMPLE BOARD LAYOUT

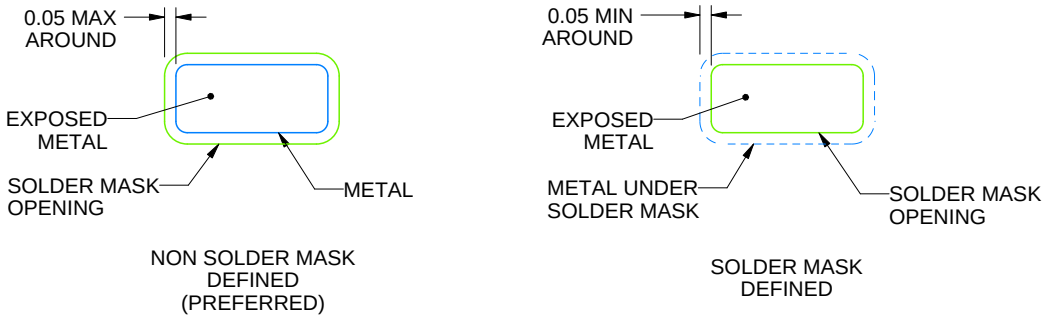
## DRL0008A

## SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X




SOLDERMASK DETAILS

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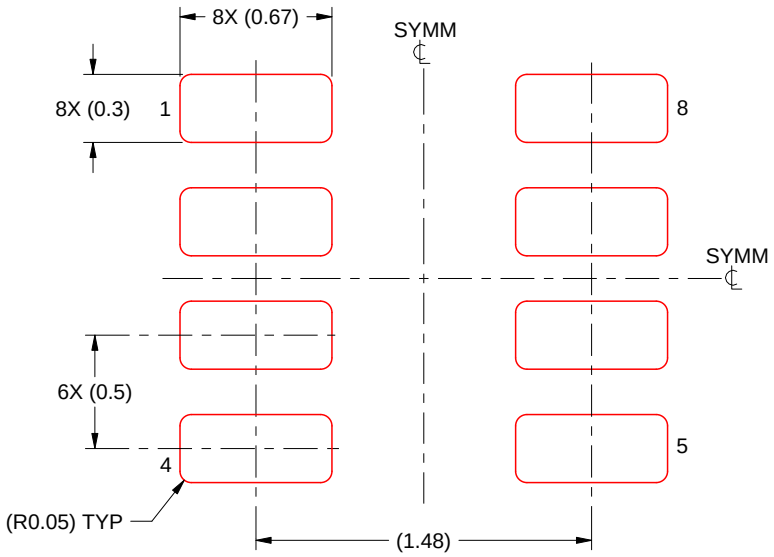
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.




SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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