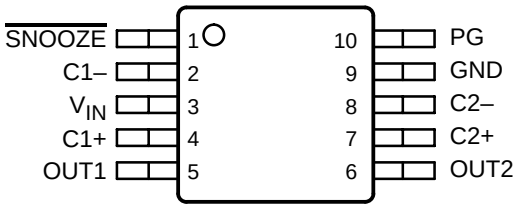
features

- Regulated 3-V or 3.3-V Output Voltage With up to 20-mA Output Current From a 0.9-V to 1.8-V Input Voltage Range
- High Power Conversion Efficiency (up to 90%) Over Wide Output Current Range, Optimized for 1.2-V Battery Voltage
- Snooze Mode for Improved Efficiency at Low-Output Current
- Additional Output With 2 Times V_I (OUT1)
- Device Quiescent Current Less Than 2 μA
- Supervisor Included; Open Drain or Push-Pull Power Good Output
- No Inductors Required/Low EMI
- Only Five Small, 1-μF Ceramic Capacitors Required
- Microsmall 10-Pin MSOP Package

applications

- Pagers
- Battery-Powered Toys
- Portable Measurement Instruments
- Home Automation Products
- Medical Instruments (Like Hearing Instruments)
- Metering Applications Using MSP430 Microcontroller
- Portable Smart Card Readers

DGS PACKAGES
(TOP VIEW)



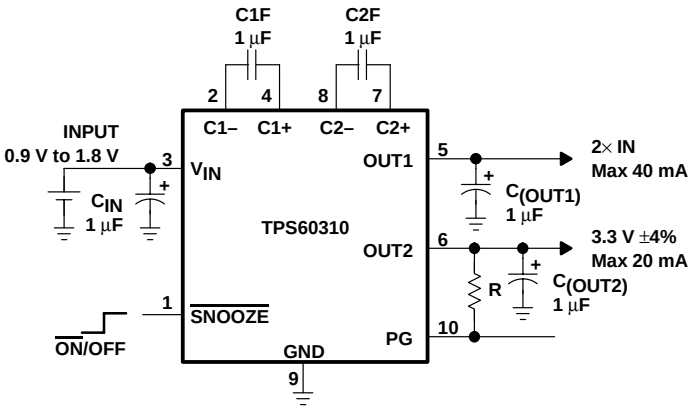
ACTUAL SIZE
3,05 mm x 4,98 mm

description

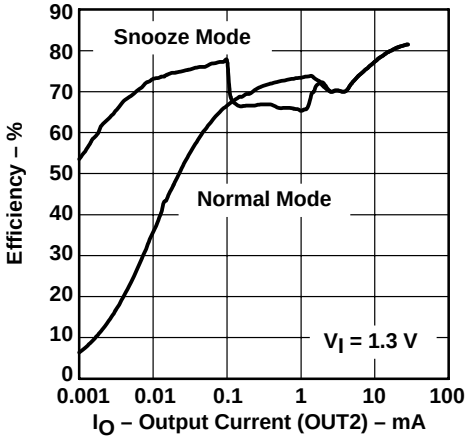
The TPS6031X step-up, regulated charge pumps generate a 3-V ±4% or 3.3-V ±4% output voltage from a 0.9-V to 1.8-V input voltage (one alkaline, NiCd, or NiMH battery).

Only five small 1-μF ceramic capacitors are required to build a complete high-efficiency dc/dc charge pump converter. To achieve the high efficiency over a wide input voltage range, the charge pump automatically selects between a 3x or 4x conversion mode.

typical application circuit



EFFICIENCY
vs
OUTPUT CURRENT (OUT2)



Snooze mode improves efficiency at an output current in the range of 1 μA to 100 μA.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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description (continued)

Output 1 (OUT1) can deliver a maximum of 40 mA, from a 1-V input, with output 2 (OUT2) not loaded. OUT2 can deliver a maximum of 20 mA, from a 1-V input, with OUT1 not loaded. Both outputs can be loaded at the same time, but the total output current of the first voltage doubler must not exceed 40 mA. For example, the load at OUT1 is 20 mA and the load at output 2 is 10 mA.

In snooze mode, the devices operate with a typical operating current of 2 μA, while the output voltage is maintained at 3.3 V ±10% or 3 V ±10%, respectively. This is lower than the self-discharge current of most batteries. Load current in snooze mode is limited to 2 mA. If the load current increases above 2 mA, the output voltage drops further and the devices automatically exits the snooze mode and operate in normal mode to regulate to the nominal output voltage with higher output currents. The device is set into the snooze mode by taking the $\overline{\text{SNOOZE}}$ pin low, and is set into normal operating mode by taking the $\overline{\text{SNOOZE}}$ pin high.

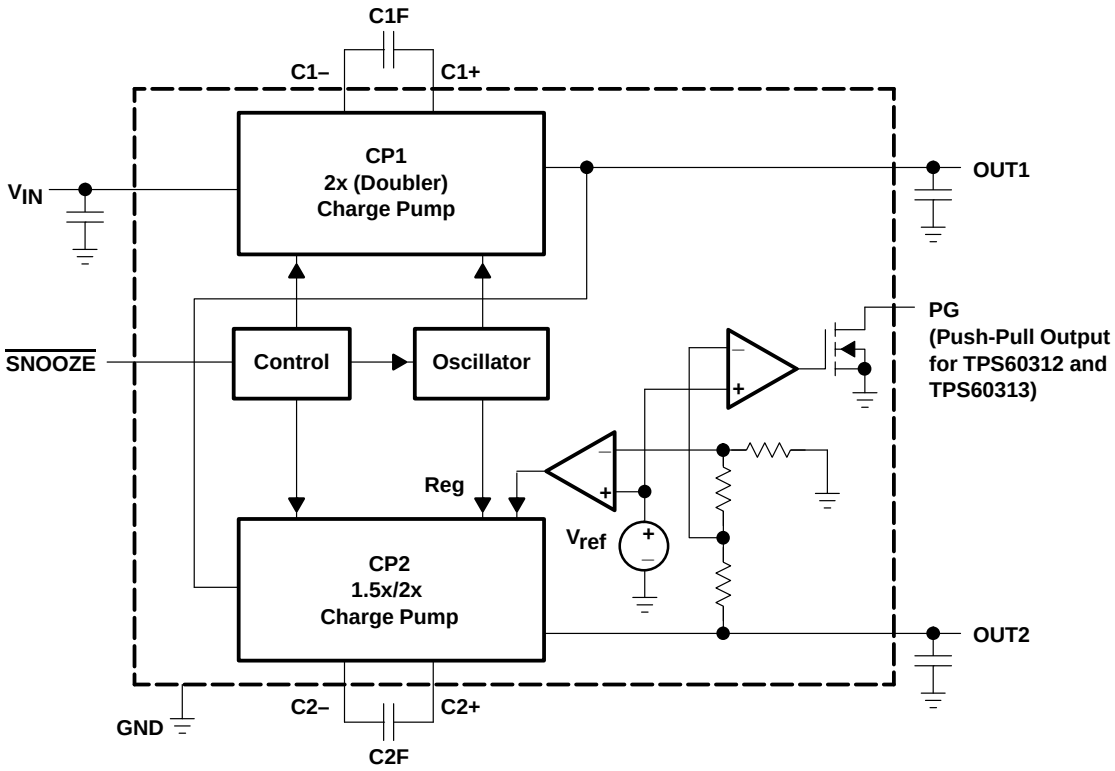
A power-good function supervises the output voltage of OUT2 and can be used for power up and power down sequencing. Power-good (PG) is offered as either open-drain or push-pull output.

AVAILABLE OPTIONS

PART NUMBER†	MARKING DGS PACKAGE	OUTPUT CURRENT 1 [mA]‡	OUTPUT CURRENT 2 [mA]§	OUTPUT VOLTAGE 1 [V]	OUTPUT VOLTAGE 2 [V]	FEATURE
TPS60310DGS	ATG	40	20	2 x V_{IN}	3.3	Open-drain power-good output
TPS60311DGS	ATI	40	20	2 x V_{IN}	3	Open-drain power-good output
TPS60312DGS	ATK	40	20	2 x V_{IN}	3.3	Push-pull power-good output
TPS60313DGS	ATL	40	20	2 x V_{IN}	3	Push-pull power-good output

† The DGS package is available taped and reeled. Add R suffix to device type (e.g. TPS60310DGSR) to order quantities of 2500 devices per reel.
‡ If OUT2 is not loaded.
§ If OUT1 is not loaded.

TPS60310 and TPS60311 functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
C1+	4		Positive terminal of the flying capacitor C1F
C1–	2		Negative terminal of the flying capacitor C1F
C2+	7		Positive terminal of the flying capacitor C2F
C2–	8		Negative terminal of the flying capacitor C2F
GND	9		GROUND
OUT1	5	O	$2 \times V_{IN}$ power output. Bypass OUT1 to GND with the output filter capacitor $C_{(OUT1)}$.
OUT2	6	O	Regulated 3.3-V power output (TPS60310, TPS60312) or 3-V power output (TPS60311, TPS60313), respectively Bypass OUT2 to GND with the output filter capacitor $C_{(OUT2)}$.
PG	10	O	Power good detector output. As soon as the voltage on OUT2 reaches about 98% of its nominal value this pin goes high. Open drain output on TPS60310 and TPS60311. A pullup resistor should be connected between PG and OUT1 or OUT2. Push-pull output stage on TPS60312 and TPS60313
$\overline{\text{SNOOZE}}$	1	I	Snooze mode enable input – $\overline{\text{SNOOZE}}$ = Low enables the snooze mode at low output current. – $\overline{\text{SNOOZE}}$ = High disables the snooze mode.
V_{IN}	3	I	Supply input. Bypass V_{IN} to GND with a ≥ 1-µF capacitor.

detailed description

operating principle

The TPS6031X charge pumps are voltage quadruplers that provide a regulated 3.3-V or 3-V output from a 0.9-V to 1.8-V input. They deliver a maximum load current of 20 mA. Designed specifically for space critical battery powered applications, the complete converter requires only five external capacitors and enables the design to use low-cost, small-sized, 1-µF ceramic capacitors. The TPS6031X circuits consist of an oscillator, a voltage reference, an internal resistive feedback circuit, two error amplifiers, two charge pump stages with MOSFET switches, a shutdown/start-up circuit, and a control circuit.

snooze mode

The devices contain a circuit which dramatically reduces the quiescent current at light loads. This so called snooze mode must be enabled by pulling the $\overline{\text{SNOOZE}}$ pin low. When the output current decreases below the snooze mode threshold, the device enters the snooze mode. In snooze mode, the main error amplifier with 4% error and 50-µA supply current is disabled and a 10%, 2-µA regulator controls the output voltage.

start-up procedure

The start-up performance of the device is independent of the level of the snooze input. When voltage is applied to the input, CP1 will first enter a dc start-up mode during which the capacitor on OUT1 is charged up to about V_{IN}. After that, it starts switching to boost the voltage further up to about two times V_{IN}. CP1 first enters a dc start-up mode during which the capacitor on OUT1 is charged up to about V_{IN}. CP2 then follows and charges up the capacitor on OUT2 to about the voltage on OUT1, after that, it also starts switching and boosts up the voltage to its nominal value. The voltage at the $\overline{\text{SNOOZE}}$ pin must not exceed the highest voltage applied to the device.

NOTE:

During start-up with V_{OUT} = 0 V, the highest voltage is the input voltage.

power-good detector

The power-good output is an open-drain output on the TPS60310 and TPS60311 or a push-pull output on the TPS60312 and TPS60313. The PG-output pulls low when the output of OUT2 is out of regulation. When the output rises to within 98% of regulation, the power-good output goes active high. In shutdown, power-good is pulled low. In normal operation, an external pullup resistor with the TPS60310 and TPS60311 is typically used to connect the PG pin to VOUT. The resistor should be in the 100-kΩ to 1-MΩ range. If the PG output is not used, it should remain unconnected. Output current at PG (TPS60312, TPS60313) reduces maximum output current at OUT2.

In snooze mode, the output voltage is sampled at a rate up to 2 ms and is applied to the power-good comparator. In normal mode, the output voltage is measured continuously.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Input voltage, V_I (IN to GND) (see Note 1) . . . . . –0.3 V to 2 V
Output voltage, V_O (OUT1, OUT2, EN, PG to GND) (see Note 1) . . . . . –0.3 V to 3.6 V
Voltage, (C1+ to GND) . . . . . –0.3 V to $V_{O(OUT1)}$ + 0.3 V
Voltage, (C1– to GND, C2– to GND) . . . . . –0.3 V to V_{IN} + 0.3 V
Voltage, (C2+ to GND) . . . . . –0.3 V to $V_{O(OUT2)}$ + 0.3 V
Continuous power dissipation . . . . . See Dissipation Rating Table
Output current, I_O (OUT1) . . . . . 80 mA
Output current, I_O (OUT2) . . . . . 40 mA
Storage temperature range, T_{stg} . . . . . –55°C to 150°C
Maximum junction temperature, T_J . . . . . 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The voltage at $\overline{\text{SNOOZE}}$ and PG can exceed IN up to the maximum rated voltage without increasing the leakage current drawn by these pins.

DISSIPATION RATING TABLE

PACKAGE	T_A <25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DGS	424 mW	3.4 mW/°C	271 mW	220 mW

NOTE: The thermal resistance junction to ambient of the DGS package is $R_{TH–JA}$ = 294°C/W.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Input voltage, V_I	0.9		1.8	V
Output current (OUT2), $I_{O(OUT2)}$			20	mA
Output current (OUT1), $I_{O(OUT1)}$			40	mA
Input capacitor, C_I	1			µF
Flying capacitors, C1F, C2F		1		µF
Output capacitors, $C_{O(1)}$, $C_{O(2)}$	1			µF
Operating junction temperature, T_J	–40		125	°C

electrical characteristics at C_{IN} = C1F = C2F = $C_{(OUT1)}$ = $C_{(OUT2)}$ = 1 μF, T_C = –40°C to 85°C, V_{IN} = 1 V, $V_{(SNOOZE)}$ = V_{IN} (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Supply voltage range				0.9		1.8	V
$I_{O(OUT1)}$	Maximum output current for TPS60310, TPS60312		V_{IN} ≥ 1.1 V, $I_{O(OUT2)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA		40			mA
			V_{IN} = 0.9 V, $I_{O(OUT2)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA		20			
$I_{O(OUT2)}$			V_{IN} ≥ 1.1 V, $I_{O(OUT1)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA		20			
			V_{IN} = 0.9 V, $I_{O(OUT1)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA		10			
$I_{O(OUT1)}$	Maximum output current for TPS60311, TPS60313		V_{IN} ≥ 1.1 V, $I_{O(OUT2)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA		40			mA
			V_{IN} = 0.9 V, $I_{O(OUT2)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA		20			
$I_{O(OUT2)}$			V_{IN} ≥ 1 V, $I_{O(OUT1)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA		20			
			V_{IN} = 0.9 V, $I_{O(OUT1)}$ = 0 mA, $I_{(PG,1)}$ = 0 mA		12			
$V_{O(OUT2)}$	Output voltage for TPS60310, TPS60312		1.1 V < V_{IN} < 1.8 V, $I_{O(OUT1)}$ = 0 mA, 0 < $I_{O(OUT2)}$ < 20 mA		3.17	3.3	3.43	V
			0.9 V < V_{IN} < 1.1 V, $I_{O(OUT1)}$ = 0 mA, $I_{O(OUT2)}$ < 10 mA		3.17	3.3	3.43	
			0.9 V < V_{IN} < 1.8 V, $V_{(SNOOZE)}$ = 0 V, 0 < $I_{O(OUT2)}$ < 1 mA or 0 < $I_{O(OUT1)}$ < 2 mA		2.85	3.3	3.6	V
$V_{O(OUT2)}$	Output voltage for TPS60311, TPS60313		1 V < V_{IN} < 1.8 V, $I_{O(OUT1)}$ = 0 mA, 0 < $I_{O(OUT2)}$ < 20 mA		2.88	3	3.12	V
			V_{IN} > 1.65 V, $I_{O(OUT1)}$ = 0 mA, 25 μA < $I_{O(OUT2)}$ < 20 mA		2.88	3	3.15	
			0.9 V < V_{IN} < 1.8 V, $V_{(SNOOZE)}$ = 0 V, 0 < $I_{O(OUT2)}$ < 1 mA or 0 < $I_{O(OUT1)}$ < 2 mA		2.6	3.3	3.27	V
$V_{P–P}$	Output voltage ripple	OUT2	$I_{O(OUT2)}$ = 20 mA, $I_{O(OUT1)}$ = 0 mA			30		$mV_{P–P}$
		OUT1	$I_{O(OUT1)}$ = 40 mA, $I_{O(OUT2)}$ = 0 mA			60		
I_Q	Quiescent current (no-load input current)		I_O = 0 mA, V_{IN} = 1.8 V			35	70	μA
$I_{(SQ)}$	Quiescent supply current in snooze mode		V_{IN} = 1.65 V, $V_{(SNOOZE)}$ = 0 V, T_C = 60°C			2	10	μA
			V_{IN} = 1.65 V, $V_{(SNOOZE)}$ = 0 V, T_C ≤ 25°C			1.5	4	
f_{OSC}	Internal switching frequency				470	700	900	kHz
$V_{IL(EN)}$	EN input low voltage		V_{IN} = 0.9 V to 1.8 V				0.3×V_{IN}	V
$V_{IH(EN)}$	EN input high voltage		V_{IN} = 0.9 V to 1.8 V		0.7×V_{IN}			V
I_{lkg}	EN input leakage current		$V_{(EN)}$ = 0 V or V_{IN} or $V_{O(OUT2)}$ or $V_{O(OUT1)}$			0.01	0.1	μA
	LinSkip switching threshold		V_{IN} = 1.25 V			7.5		mA
	Snooze mode threshold		V_{IN} = 1.25 V	$I_{O(OUT1)}$	2		8	mA
				$I_{O(OUT2)}$	1		4	mA

electrical characteristics at C_{IN} = C1F = C2F = $C_{(OUT1)}$ = $C_{(OUT2)}$ = 1 μF, T_C = –40°C to 85°C, V_{IN} = 1 V, $V_{(SNOOZE)}$ = V_{IN} (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Short circuit current	V_{IN} = 1.8 V	$V_{O(OUT2)}$ = 0 V	5	20	50	mA
		$V_{O(OUT1)}$ = 0 V	2	80	150	
Output load regulation	V_{IN} = 1.25 V, T_C = 25°C 2 mA < $I_{O(OUT2)}$ < 20 mA			0.1		%/mA
Output line regulation	1 V < V_{IN} < 1.65 V, T_C = 25°C, $I_{O(OUT)}$ = 10 mA			0.75		%/V
	1 V < V_{IN} < 1.65 V, T_C = 25°C, $I_{O(OUT2)}$ = 1 mA, $V_{(SNOOZE)}$ = 0 V			1		%/V
No load start-up time				400		μs
Impedance of first charge pump stage				4.0		Ω
Start-up performance at OUT2 (minimum start-up load resistance)	V_{IN} ≥ 1.1 V		165			Ω
	V_{IN} ≥ 1 V		330			
	V_{IN} = 0.9 V		1000			
Startup performance at OUT1 (minimum start-up load resistance)	V_{IN} = 1 V		500			Ω

electrical characteristics for power good comparator of devices TPS6031X at T_C = –40°C to 85°C, V_{IN} = 1 V and $V_{(SNOOZE)}$ = V_{IN} (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(PG)}$	Power-good trip voltage		V_O ramping positive		V_O – 1%	V_O	V
V_{hys}	Power-good trip voltage hysteresis		V_O ramping negative		10%		
V_{OL}	Power-good output voltage low		V_O = 0 V, $I_{(PG)}$ = 1.6 mA			0.3	V
I_{lkg}	Power-good leakage current	TPS60310	V_O = 3.3 V, $V_{(PG)}$ = 3.3 V		0.01	0.1	μA
		TPS60311	V_O = 3 V, $V_{(PG)}$ = 3 V		0.01	0.1	
V_{OH}	Power-good output voltage high	TPS60312	$I_{O(PG)}$ = –5 mA	3			V
		TPS60313		2.7			
$I_{O(PG,1)}$	Output current at power good (source)	TPS60312, TPS60313		–5			mA
$I_{O(PG,0)}$	Output current at power good (sink)	All devices	$V_{(PG)}$ = 0 V	1.6			mA
$R_{(PG,1)}$	Output resistance at power good	TPS60312, TPS60313	$V_{(PG)}$ = $V_{O(OUT2)}$		15		Ω
$R_{(PG,0)}$		All devices	$V_{(PG)}$ = 0 V		100		Ω

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
η	Efficiency	vs Output current (TPS60310 and TPS60311)	1, 2
I_S	Supply current	vs Output current	3
I_Q	Quiescent current	vs Input voltage	4
$V_{O(OUT2)}$	Output voltage at OUT2	vs Output current (TPS60310 and TPS60311)	5, 6
$V_{O(OUT1)}$	Output voltage at OUT1	vs Output current at 25°C, V_I = 0.9 V, 1.1 V, 1.25 V, 1.4 V, 1.6 V, 1.8 V	7
$V_{O(OUT2)}$	Output voltage at OUT2	vs Input voltage (TPS60310 and TPS60311)	8, 9
$V_{O(OUT1)}$	Output voltage at OUT1	vs Input voltage (TPS60310 and TPS60311)	10
$V_{O(OUT2)}$	Output voltage at OUT2	vs Free-air temperature (TPS60310, TPS60312, TPS60311, and TPS60313)	11, 12
$V_{O(OUT2)}$	Output voltage ripple at OUT2		13
	Minimum input voltage	vs Output current for TPS60310, TPS60312, TPS60311, and TPS60313	14, 15
	Start-up timing enable		16
	Switching frequency	vs Input voltage	17
	Load transient response		18
	Line transient response		19
V_O	Output voltage	vs Time	20
	Output voltage ripple in Snooze mode		21

TYPICAL CHARACTERISTICS

TPS60310, TPS60312
EFFICIENCY
vs
OUTPUT CURRENT

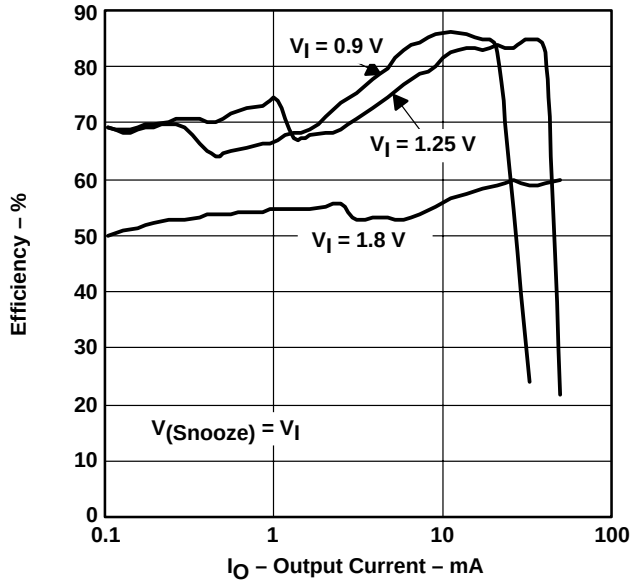


Figure 1

TPS60311, TPS60313
EFFICIENCY
vs
OUTPUT CURRENT

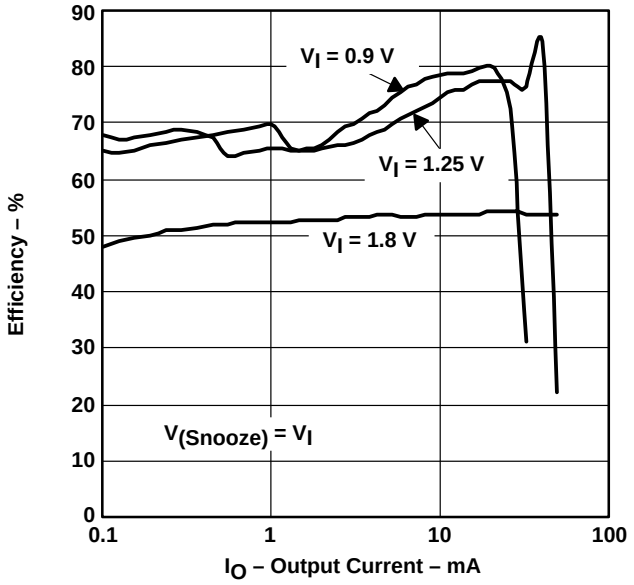


Figure 2

TYPICAL CHARACTERISTICS

TPS60310
SUPPLY CURRENT
vs
OUTPUT CURRENT

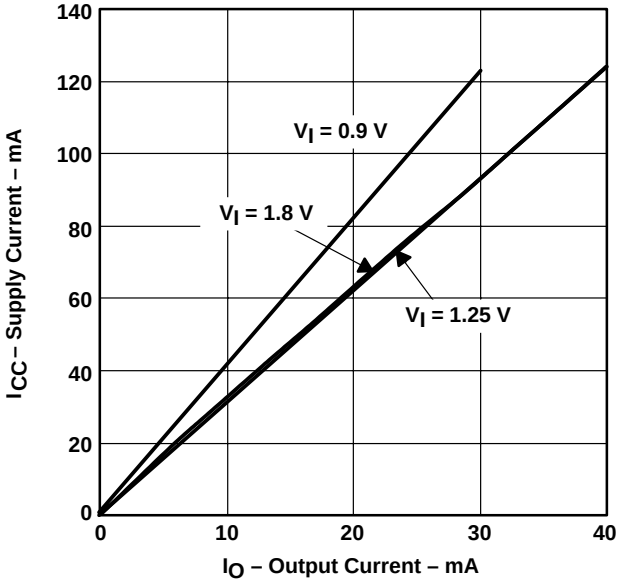


Figure 3

TPS6031X
QUIESCENT CURRENT
vs
INPUT VOLTAGE

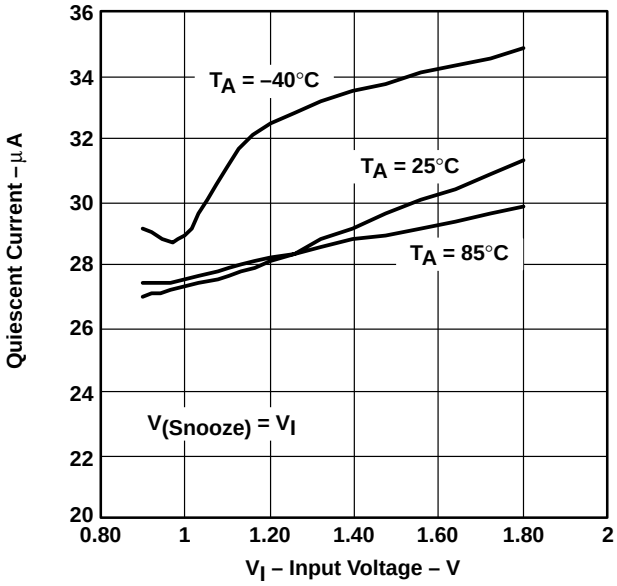


Figure 4

TPS60310, TPS60312
OUTPUT VOLTAGE (OUT2)
vs
OUTPUT CURRENT (OUT2)

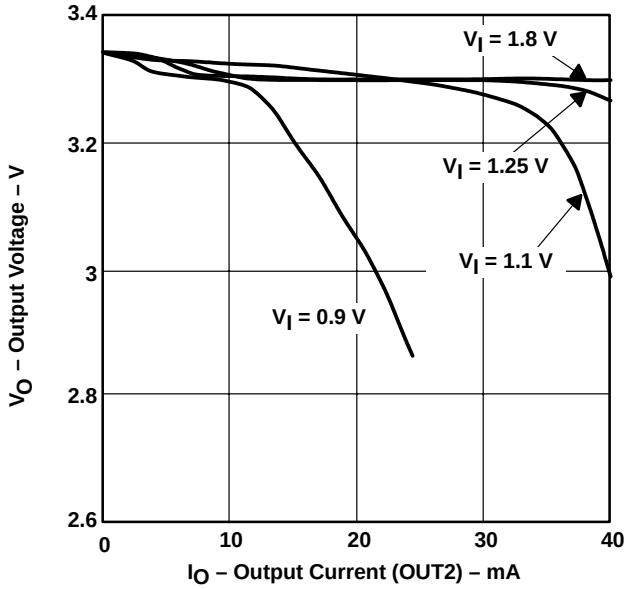


Figure 5

TPS60311, TPS60313
OUTPUT VOLTAGE (OUT2)
vs
OUTPUT CURRENT (OUT2)

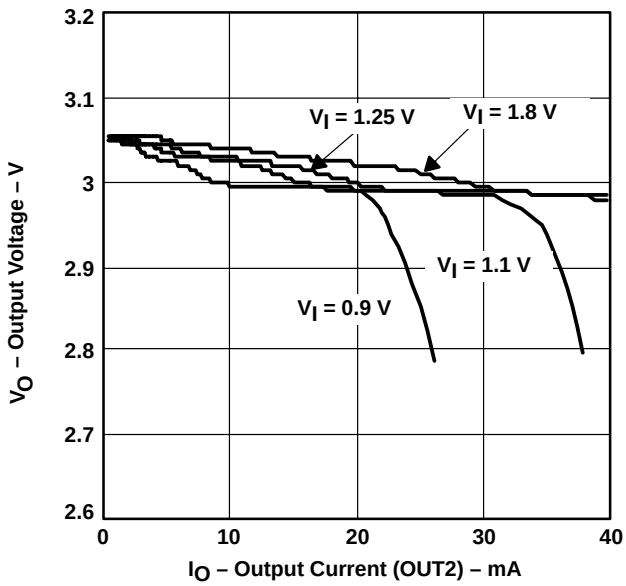


Figure 6

TYPICAL CHARACTERISTICS

TPS60310, TPS60312
OUTPUT VOLTAGE (OUT1)
vs
OUTPUT CURRENT (OUT1)

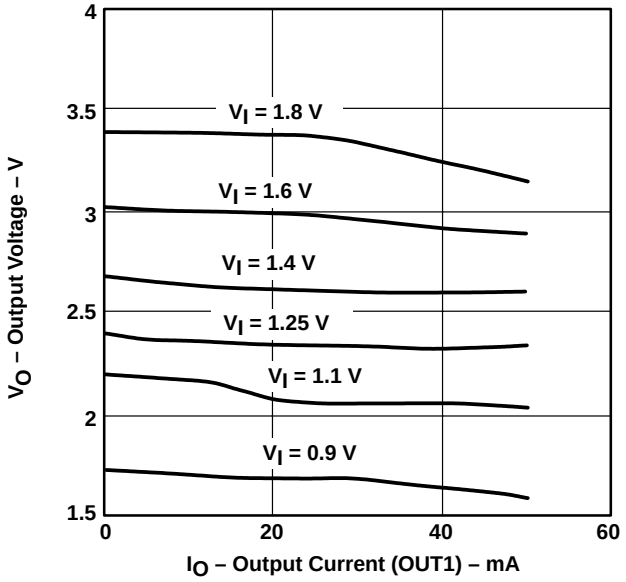


Figure 7

TPS60310, TPS60312
OUTPUT VOLTAGE (OUT2)
vs
INPUT VOLTAGE

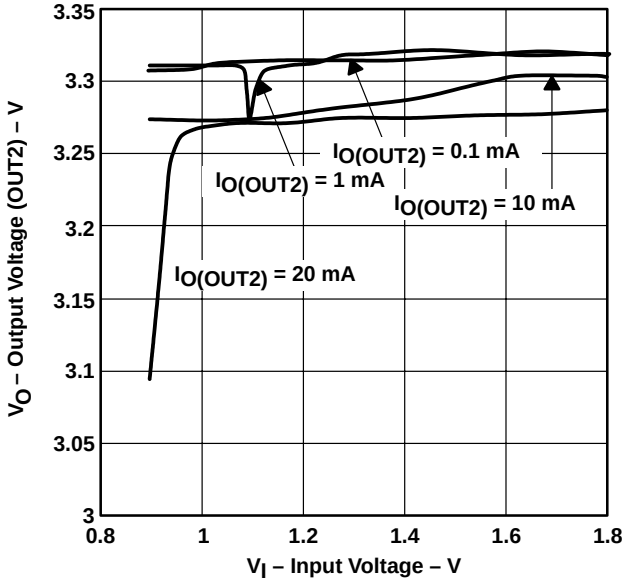


Figure 8

TPS60310, TPS60312
OUTPUT VOLTAGE (OUT2)
vs
INPUT VOLTAGE

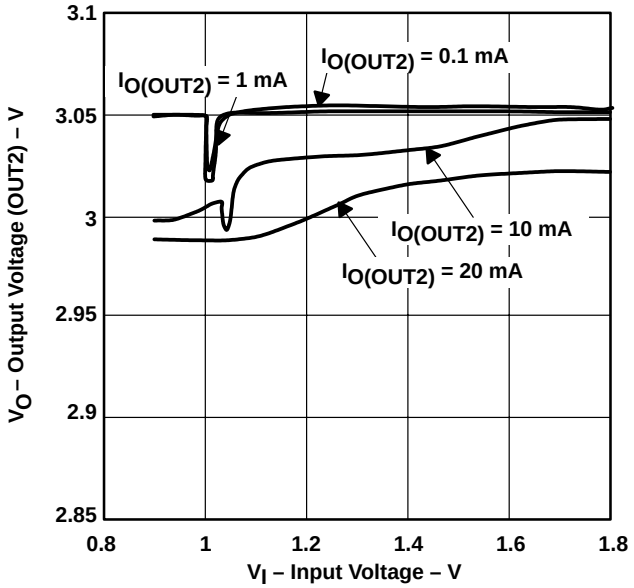


Figure 9

TPS6031x
OUTPUT VOLTAGE (OUT1)
vs
INPUT VOLTAGE

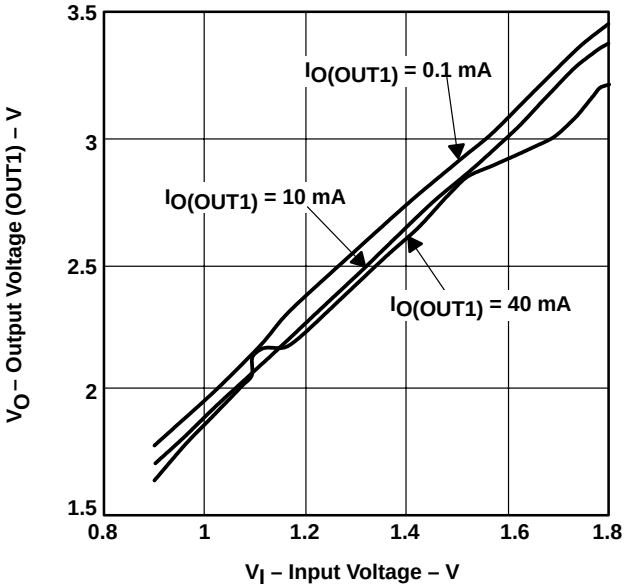


Figure 10

TYPICAL CHARACTERISTICS

TPS60310, TPS60312
OUTPUT VOLTAGE (OUT2)
vs
FREE-AIR TEMPERATURE

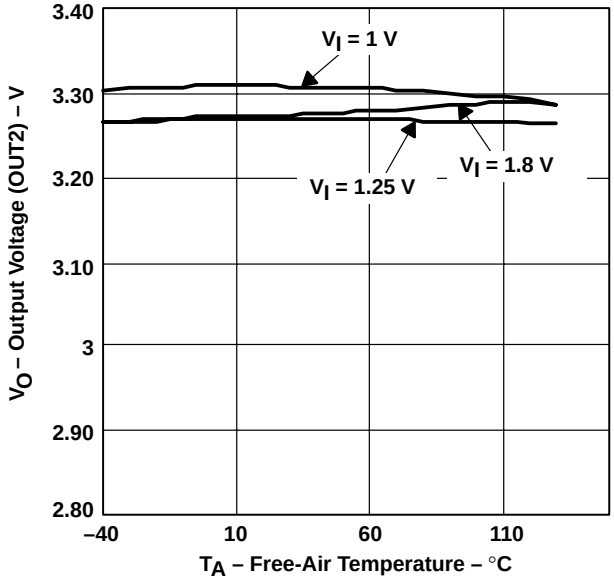


Figure 11

TPS60311, TPS60313
OUTPUT VOLTAGE (OUT2)
vs
FREE-AIR TEMPERATURE

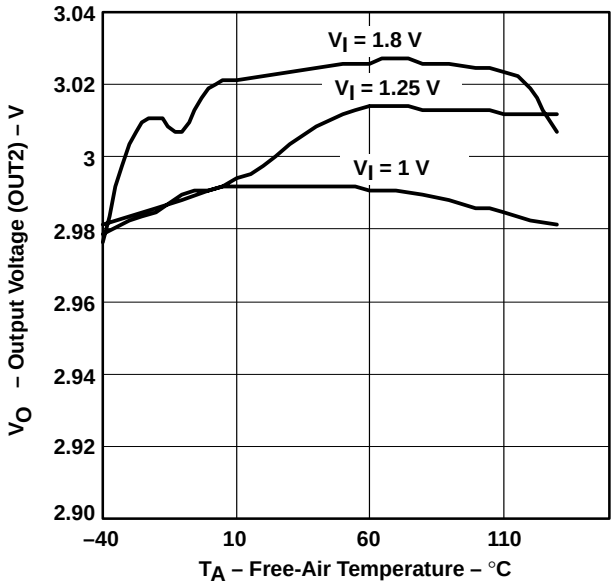


Figure 12

TPS6031x
OUTPUT VOLTAGE RIPPLE (OUT2)

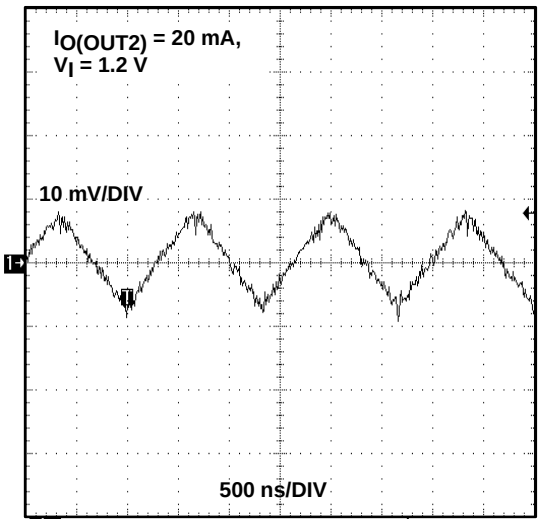


Figure 13

TPS60310, TPS60312
MINIMUM INPUT VOLTAGE
vs
OUTPUT CURRENT

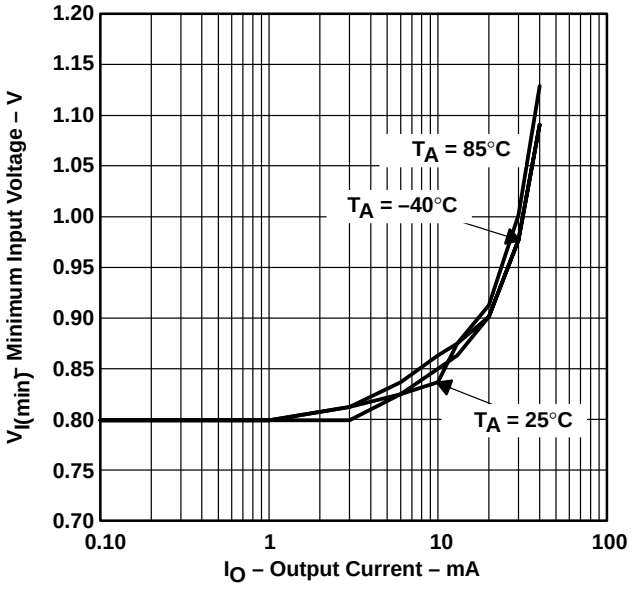


Figure 14

TYPICAL CHARACTERISTICS

TPS60311, TPS60313
MINIMUM INPUT VOLTAGE
vs
OUTPUT CURRENT

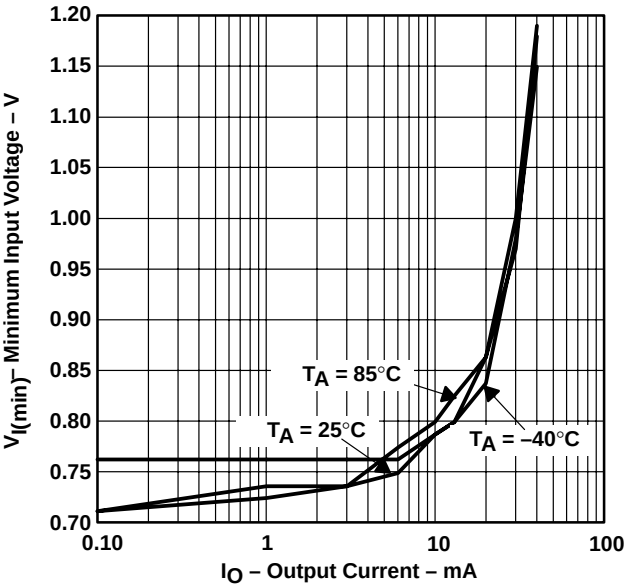


Figure 15

START-UP TIMING ENABLE

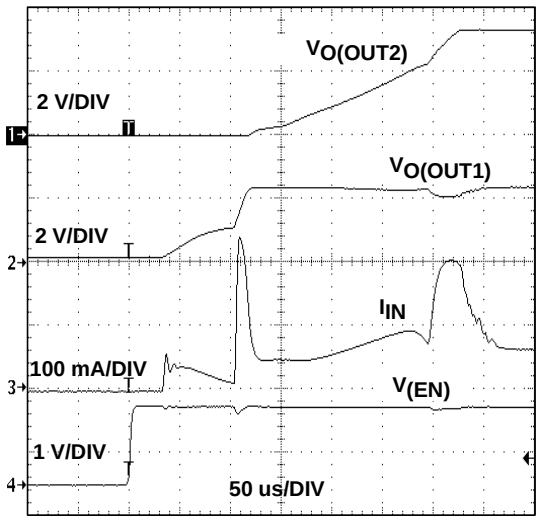


Figure 16

SWITCHING FREQUENCY
vs
INPUT VOLTAGE

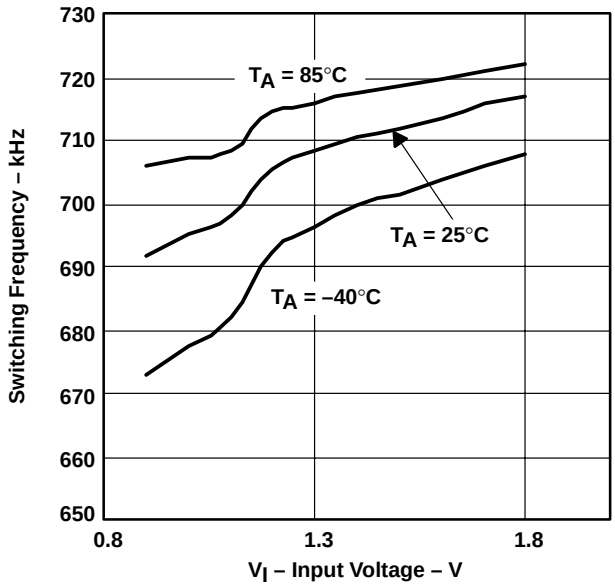


Figure 17

LOAD TRANSIENT RESPONSE

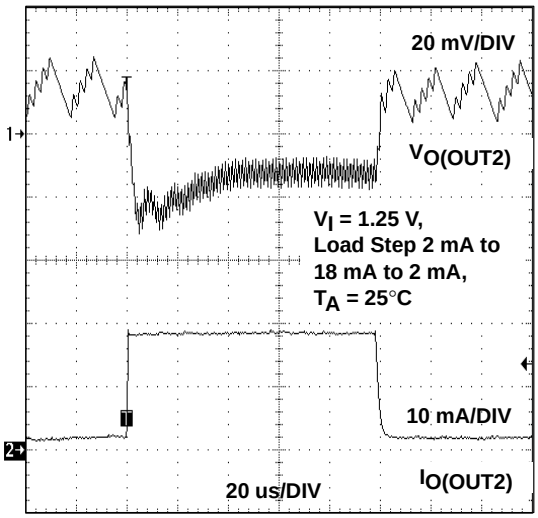


Figure 18

TYPICAL CHARACTERISTICS

LINE TRANSIENT RESPONSE

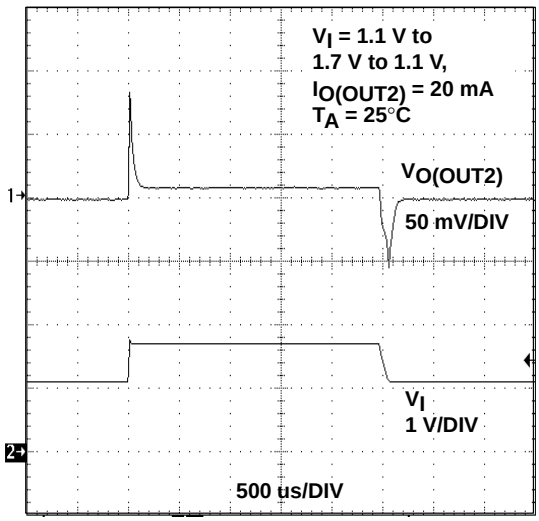


Figure 19

OUTPUT VOLTAGE
vs
TIME

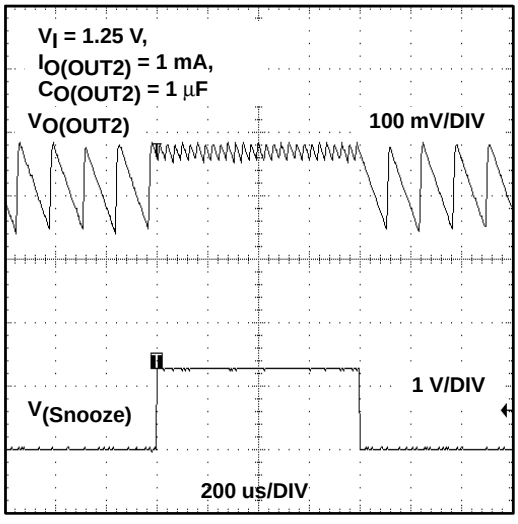


Figure 20

OUTPUT VOLTAGE RIPPLE IN SNOOZE MODE

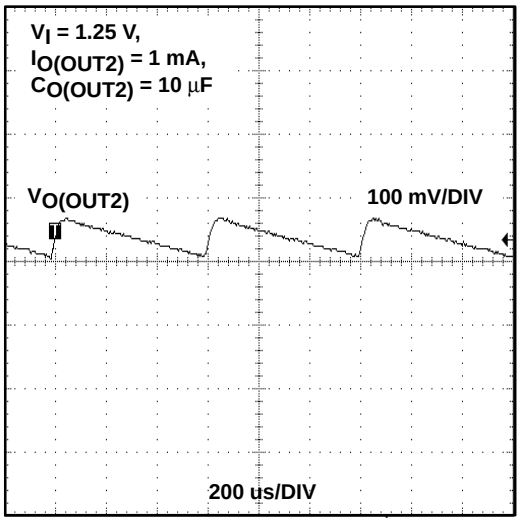


Figure 21

APPLICATION INFORMATION

design procedure

capacitor selection

The TPS6031X devices require only five external capacitors. Their values are closely linked to the required output current and the output noise and ripple requirements. It is possible to only use 1-µF capacitors of the same type.

The input capacitor improves system efficiency by reducing the input impedance and stabilizing the input current.

The minimum required capacitance of the output capacitor (C_O) that can be selected is 1 µF. Depending on the maximum allowed output ripple voltage, larger values can be chosen. Table 1 shows capacitor values recommended for low output voltage ripple operation. A recommendation is given for the smallest size.

Table 1. Recommended Capacitor Values for Low-Output Voltage Ripple Operation

V_{IN} [V]	$I_{O(OUT2)}$ [mA]	C_{IN} [µF]	C_{XF} [µF]	C_{OUT} [µF]	V_{P-P} [mV] AT 20 mA/ V_{IN} = 1.1 V
		CERAMIC	CERAMIC	CERAMIC	
0.9...1.8	0…20	1	1	1	16
0.9…1.8	0…20	1	1	2.2	10
0.9…1.8	0…20	1	1	10 // 0.1	6

Table 2. Recommended Capacitors

MANUFACTURER	PART NUMBER	SIZE	CAPACITANCE	TYPE
Taiyo Yuden	UMK212BJ104MG	0805	0.1 µF	Ceramic
	LMK212BJ105KG	0805	1 µF	Ceramic
	LMK212BJ225MG	0805	2.2 µF	Ceramic
	JMK316BJ475KL	1206	4.7 µF	Ceramic
AVX	0805ZC105KAT2A	0805	1 µF	Ceramic
	1206ZC225KAT2A	1206	2.2 µF	Ceramic

Table 3 lists the manufacturers of recommended capacitors. However, ceramic capacitors will provide the lowest output voltage ripple due to their typically lower ESR.

Table 3. Recommended Capacitor Manufacturers

MANUFACTURER	CAPACITOR TYPE	INTERNET
Taiyo Yuden	X7R/X5R ceramic	www.t-yuden.com
AVX	X7R/X5R ceramic	www.avxcorp.com
Vishay	X7R/X5R ceramic	www.vishay.com
Kemet	X7R/X5R ceramic	www.kemet.com
TDK	X7R/X5R ceramic	www.component.tdk.com

APPLICATION INFORMATION

capacitor selection (continued)

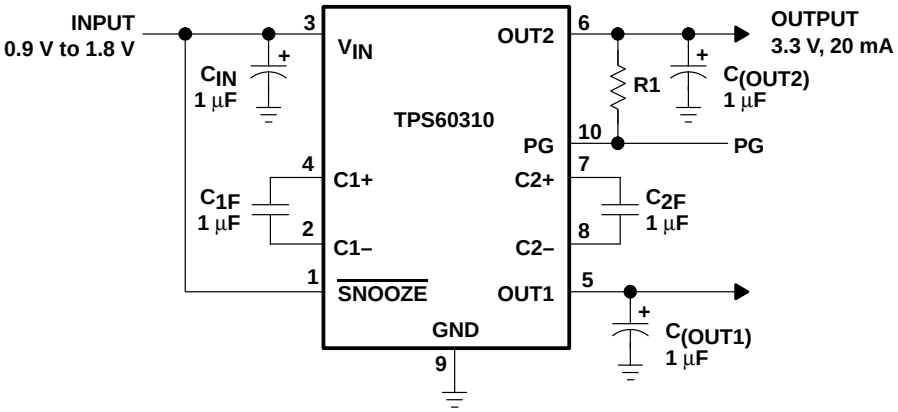


Figure 22. Typical Operating Circuit

For the maximum output current and best performance, five ceramic capacitors of 1 µF are recommended. For lower currents or higher allowed output voltage ripple, other capacitors can be used. It is recommended that the input and output capacitors have a minimum value of 1 µF. This value is necessary to assure a stable operation of the system due to the linear mode. With flying capacitors lower than 1 µF, the maximum output power decreases. This means that the device works in the linear mode with lower output currents.

output filter design

The power-good output is capable of driving light loads up to 5 mA (see Figure 23). Therefore, the output resistance of the power-good pin with the output capacitor, can be used as an RC-filter.

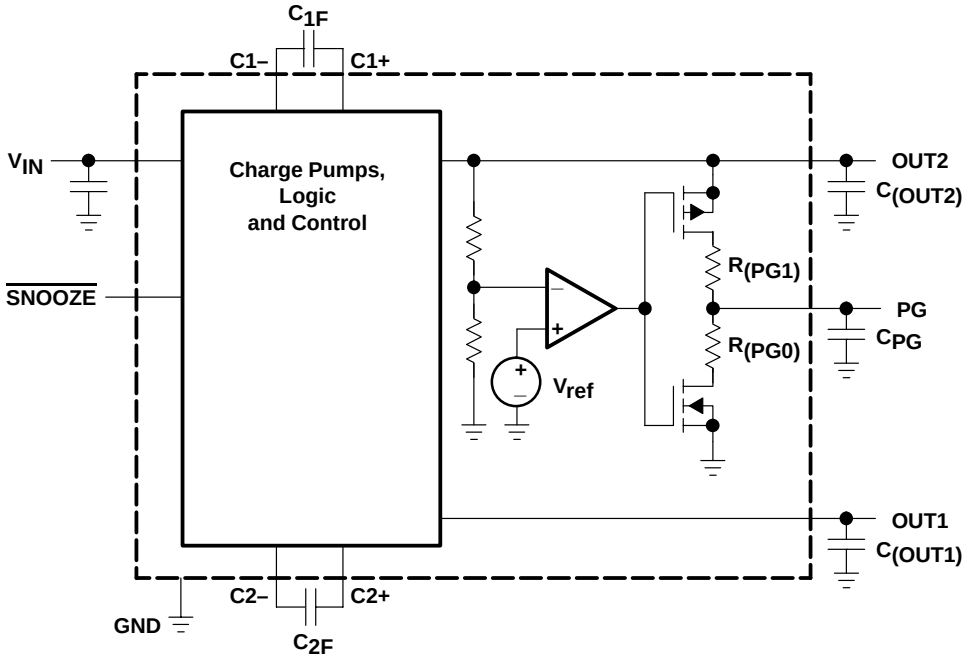


Figure 23. TPS60312, TPS60313 Push-Pull Power-Good Output-Stage as Filtered Supply

APPLICATION INFORMATION

output filter design (continued)

Due to $R_{(PG,1)}$, an output filter can easily be formed with an output capacitor (C_{PG}). Cutoff frequency is given by:

$$f_c = \frac{1}{2\pi R_{(PG,1)} C_{PG}} \quad (1)$$

and ratio V_O/V_I for the ac ripple is:

$$\left|\frac{V_{(PG,1)}}{V_{O(OUT2)}}\right| = \frac{1}{\sqrt{1 + \left(2\pi f R_{(PG,1)} C_{PG}\right)^2}} \quad (2)$$

with $R_{(PG,1)}$ = 15 Ω, C_{PG} = 0.1 µF, and f = 600 kHz (at nominal switching frequency)

$$\left|\frac{V_{(PG,1)}}{V_{O(OUT2)}}\right| = 0.175 \quad (3)$$

Load current sourced by power-good output reduces maximum output current at OUT2. During start-up (power-good going high) current charging C_{PG} discharges $C_{(OUT2)}$. Therefore, C_{PG} must not be larger than $C_{PG} \leq 0.1\ C_{(OUT2)}$ or the device does not start. By charging C_{PG} through $C_{(OUT2)}$, the output voltage at OUT2 decreases. If the capacitance of C_{PG} is to large, the circuit detects power bad. The power-good output goes low and discharges C_{PG}. Then the cycle starts again. Figure 24 shows a configuration with an LC-post filter to further reduce output ripple and noise.

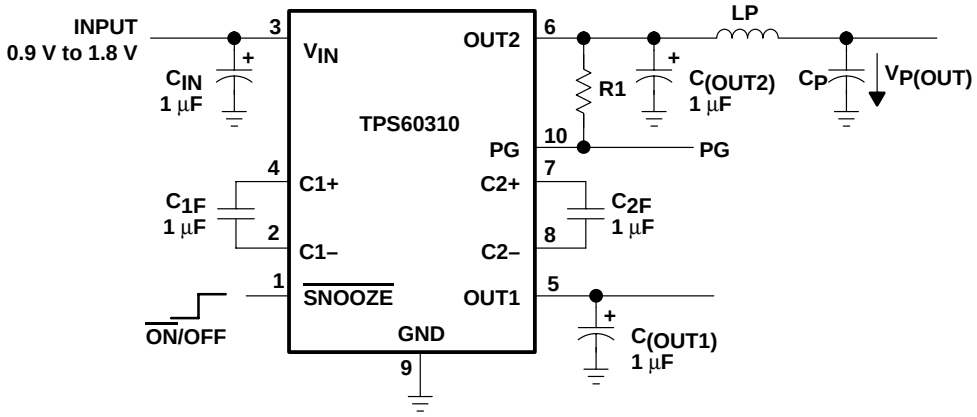


Figure 24. LC-Post Filter

Table 4. Recommended Values for Lowest Output Voltage Ripple

V_{IN} [V]	$I_{O(OUT2)}$ [mA]	C_{IN}[µF] CERAMIC	C_{XF}[µF] CERAMIC	C_{OUT}[µF] CERAMIC	L_P[µH]	C_P[µF] CERAMIC	$V_{P(OUT)}$ V_{P-P}[mV]
0.9…1.8	20	1	1	1	0.1	0.1 (X7R)	16
0.9…1.8	20	1	1	1	0.1	1 // 0.1 (X7R)	12
0.9…1.8	20	1	1	1	1	0.1 (X7R)	14
0.9…1.8	20	1	1	1	1	1 // 0.1 (X7R)	3

APPLICATION INFORMATION

output filter design (continued)

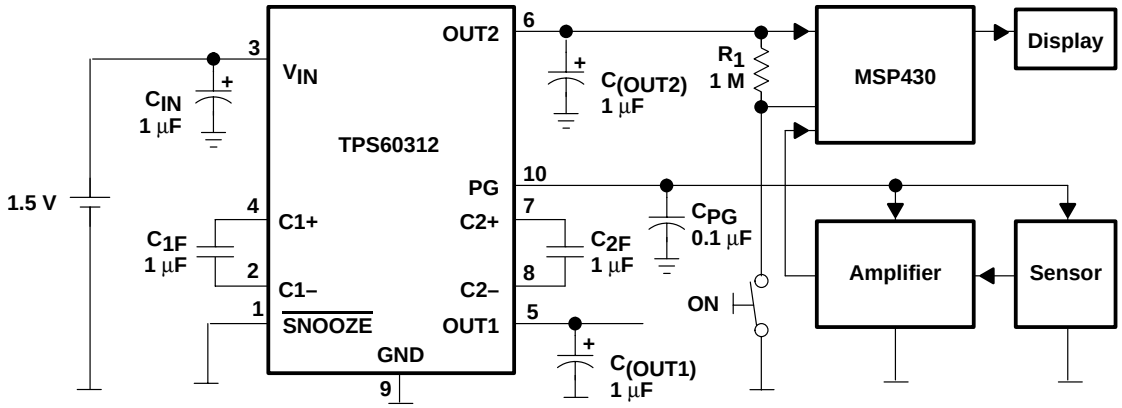


Figure 25. Application With MSP430; PG as Supply for Analog Circuits

power dissipation

As given in the data sheet, the thermal resistance of the unsoldered package is $R_{\theta JA}$ = 294°C/W. Soldered on the EVM, a typical thermal resistance of $R_{\theta JA(EVM)}$ = 200°C/W was measured.

The thermal resistance can be calculated using equation 4.

$$R_{\theta JA} = \frac{T_J - T_A}{P_D} \quad (4)$$

Where:

T_J is the junction temperature.
T_A is the ambient temperature.
P_D is the power that needs to be dissipated by the device.

The maximum power dissipation can be calculated using equation 5.

$$P_D = V_{IN} \times I_{IN} - V_O \times I_O = V_{IN(max)} \times (3 \times I_O + I_{(SUPPLY)}) - V_O \times I_O \quad (5)$$

The maximum power dissipation happens with maximum input voltage and maximum output current:

At maximum load the supply current is approximately 2 mA.

$$P_D = 1.8\ V \times (3 \times 20\ mA + 2\ mA) - 3.3\ V \times 20\ mA = 46\ mW \quad (6)$$

With this maximum rating and the thermal resistance of the device on the EVM, the maximum temperature rise above ambient temperature can be calculated using equation 7.

$$\Delta T_J = R_{\theta JA} \times P_D = 200°C/W \times 46\ mW = 10°C \quad (7)$$

This means that internal dissipation increases T_J by 10°C.

The junction temperature of the device must not exceed 125°C.

This means the IC can easily be used at ambient temperatures up to:

$$T_A = T_{J(max)} - \Delta T_J = 125°C - 10°C = 115°C \quad (8)$$

layout and board space

All capacitors should be soldered as close as possible to the IC. A PCB layout proposal for a two-layer board is shown in Figure 26. Care has been taken to connect all capacitors as close as possible to the circuit to achieve optimized output voltage ripple performance. The bottom layer is not shown in Figure 26. It only consists of a ground-plane with a single track between the two vias that can be seen in the left part of the top layer.

APPLICATION INFORMATION

layout and board space (continued)

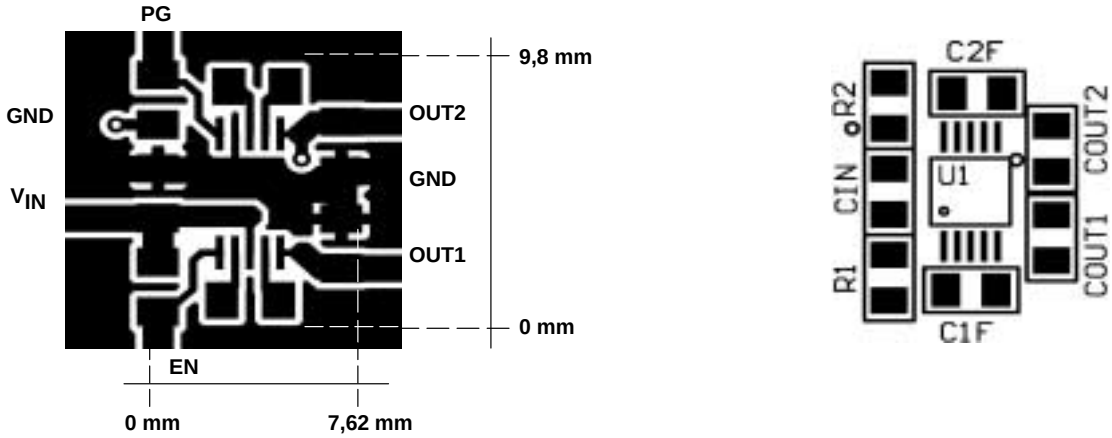


Figure 26. Recommended PCB Layout for TPS6031X (top layer)

device family products

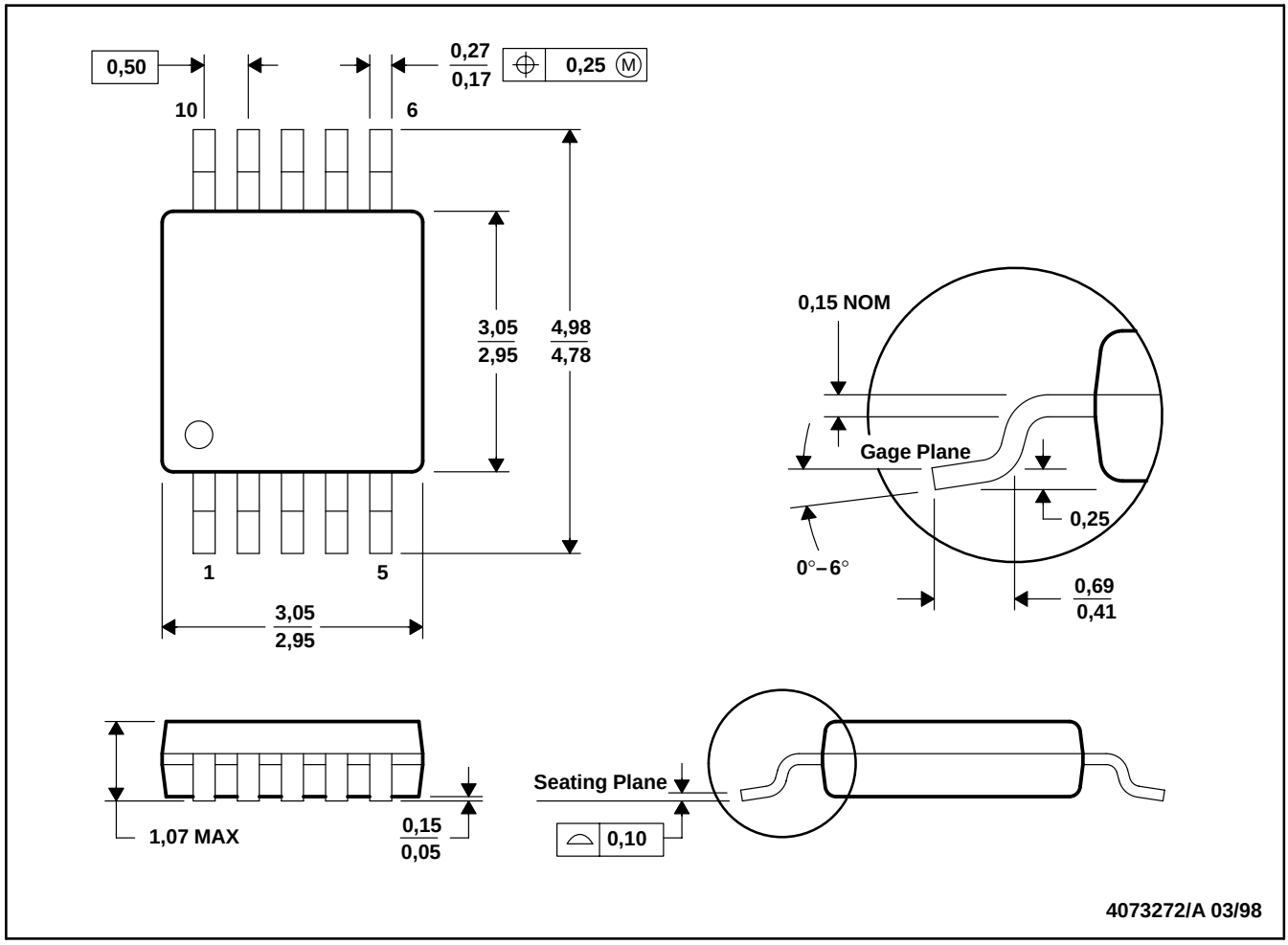
Other charge pump dc-dc converters in this family are:

Table 5. Product Identification

PART NUMBER	DESCRIPTION
TPS60100	2-cell to regulated 3.3-V, 200-mA low-noise charge pump
TPS60101	2-cell to regulated 3.3-V, 100-mA low-noise charge pump
TPS60110	3-cell to regulated 5-V, 300-mA low-noise charge pump
TPS60111	3-cell to regulated 5-V, 150-mA low-noise charge pump
TPS60120	2-cell to regulated 3.3-V, 200-mA high-efficiency charge pump with low-battery comparator
TPS60121	2-cell to regulated 3.3-V, 200-mA high-efficiency charge pump with power-good comparator
TPS60122	2-cell to regulated 3.3-V, 100-mA high-efficiency charge pump with low-battery comparator
TPS60123	2-cell to regulated 3.3-V, 100-mA high-efficiency charge pump with power-good comparator
TPS60124	2-cell to regulated 3-V, 200-mA high-efficiency charge pump with low-battery comparator
TPS60125	2-cell to regulated 3-V, 200-mA high-efficiency charge pump with power-good comparator
TPS60130	3-cell to regulated 5-V, 300-mA high-efficiency charge pump with low-battery comparator
TPS60131	3-cell to regulated 5-V, 300-mA high-efficiency charge pump with power-good comparator
TPS60132	3-cell to regulated 5-V, 150-mA high-efficiency charge pump with low-battery comparator
TPS60133	3-cell to regulated 5-V, 150-mA high-efficiency charge pump with power-good comparator
TPS60140	2-cell to regulated 5-V, 100-mA charge pump voltage tripler with low-battery comparator
TPS60141	2-cell to regulated 5-V, 100-mA charge pump voltage tripler with power-good comparator
TPS60200	2-cell to regulated 3.3-V, 100-mA low-ripple charge pump with low-battery comparator in MSOP10
TPS60201	2-cell to regulated 3.3-V, 100-mA low-ripple charge pump with power-good comparator in MSOP10
TPS60202	2-cell to regulated 3.3-V, 50-mA low-ripple charge pump with low-battery comparator in MSOP10
TPS60203	2-cell to regulated 3.3-V, 50-mA low-ripple charge pump with power-good comparator in MSOP10
TPS60210	2-cell to regulated 3.3-V, 100-mA low-ripple charge pump with ultralow operating current and low-battery comparator in MSOP10
TPS60211	2-cell to regulated 3.3-V, 100-mA low-ripple charge pump with ultralow operating current and power-good comparator in MSOP10
TPS60212	2-cell to regulated 3.3-V, 100-mA low-ripple charge pump with ultralow operating current and low-battery comparator in MSOP10
TPS60213	2-cell to regulated 3.3-V, 50-mA low-ripple charge pump with ultralow operating current and power-good comparator in MSOP10

MECHANICAL DATA

DGS (S-DPS-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS60310DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATG
TPS60310DGS.B	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATG
TPS60310DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATG
TPS60310DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATG
TPS60311DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATI
TPS60311DGS.B	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATI
TPS60311DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATI
TPS60311DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATI
TPS60312DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATK
TPS60312DGS.B	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATK
TPS60312DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATK
TPS60312DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATK
TPS60313DGS	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATL
TPS60313DGS.B	Active	Production	VSSOP (DGS) | 10	80 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATL
TPS60313DGSR	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATL
TPS60313DGSR.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATL
TPS60313DGSRG4	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATL
TPS60313DGSRG4.B	Active	Production	VSSOP (DGS) | 10	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ATL

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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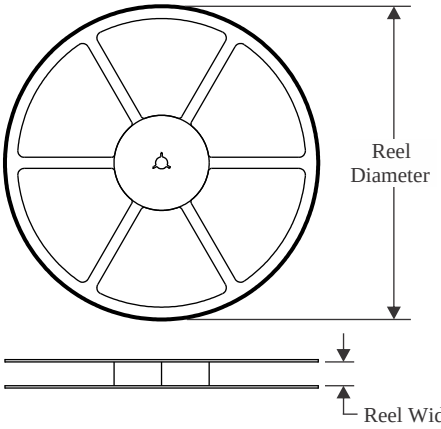
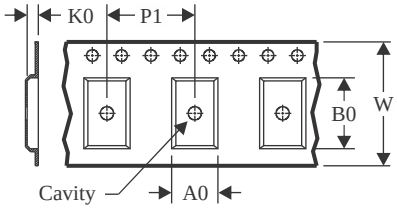
TAPE AND REEL INFORMATION

REEL DIMENSIONS

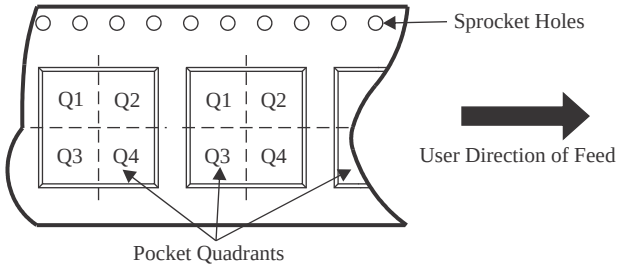


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

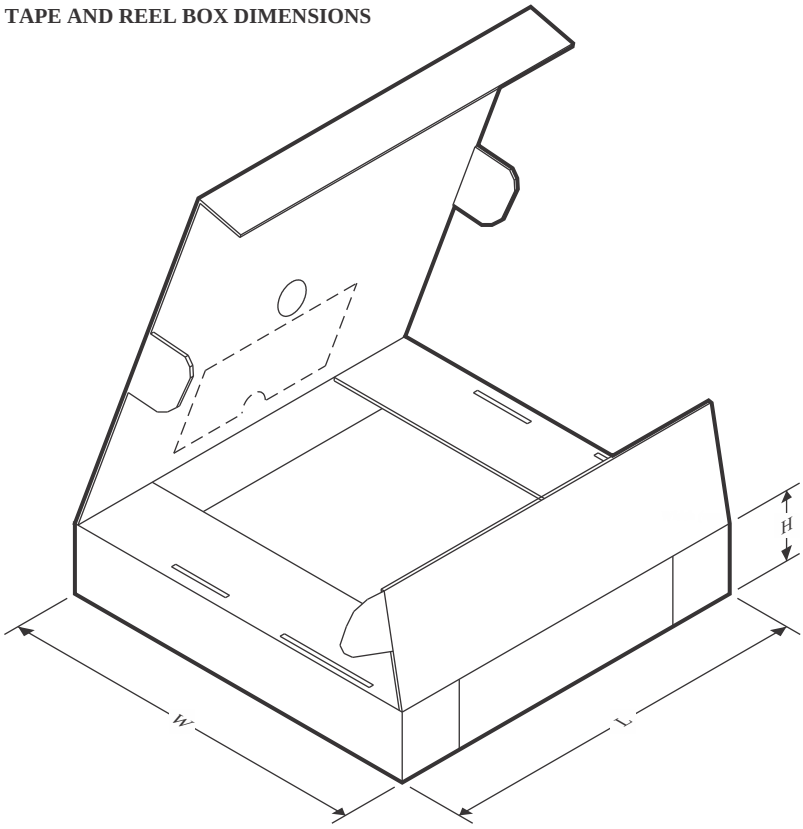
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS60310DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60311DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60312DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60313DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS60313DGSRG4	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

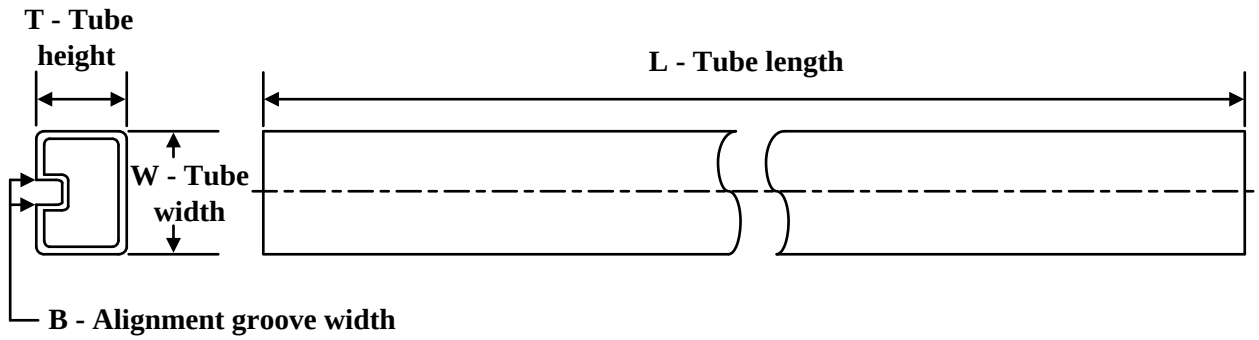
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS60310DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60311DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60312DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60313DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS60313DGSRG4	VSSOP	DGS	10	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

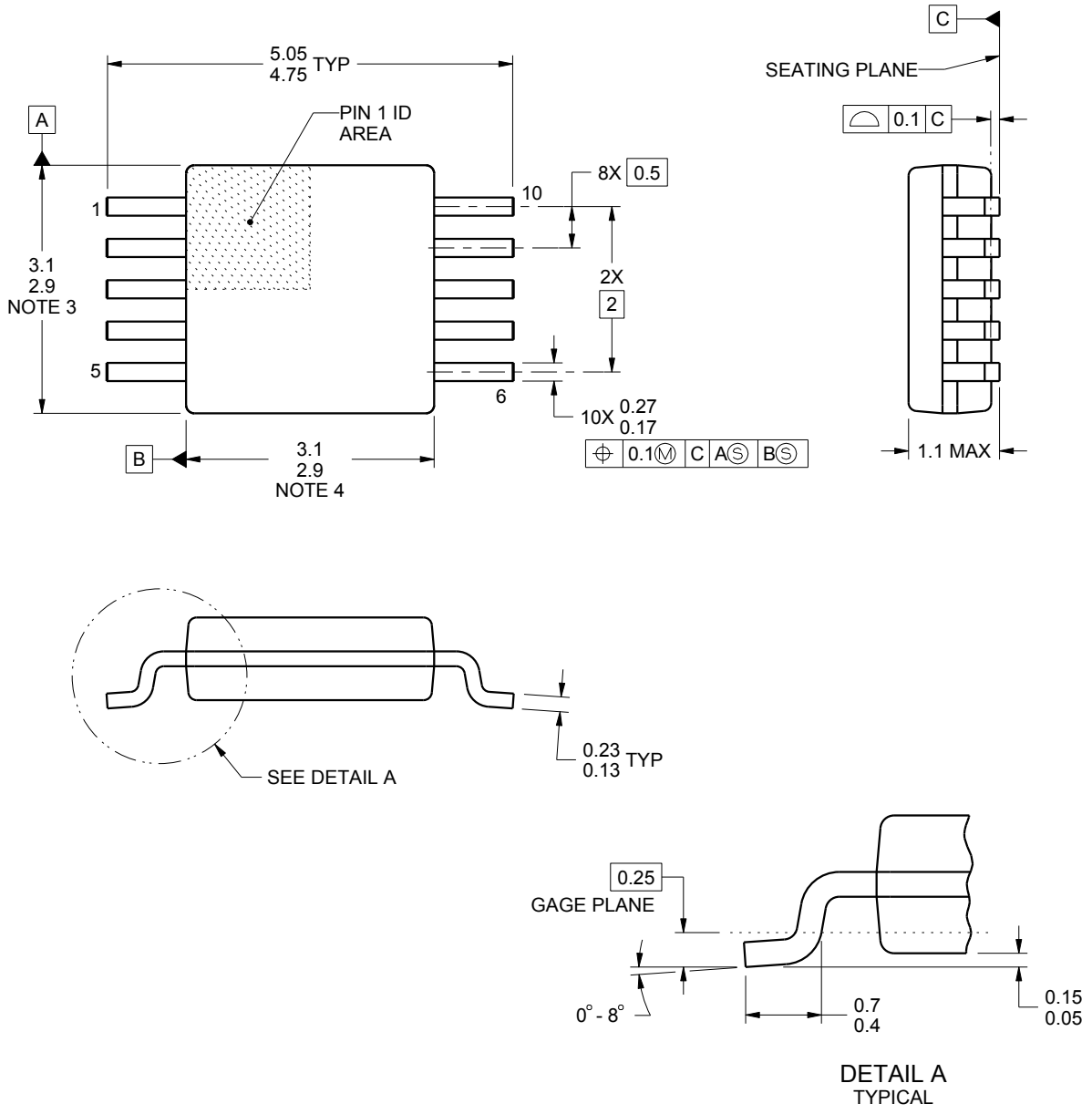
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS60310DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60310DGS.B	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60311DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60311DGS.B	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60312DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60312DGS.B	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60313DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS60313DGS.B	DGS	VSSOP	10	80	331.47	6.55	3000	2.88

PACKAGE OUTLINE

DGS0010A

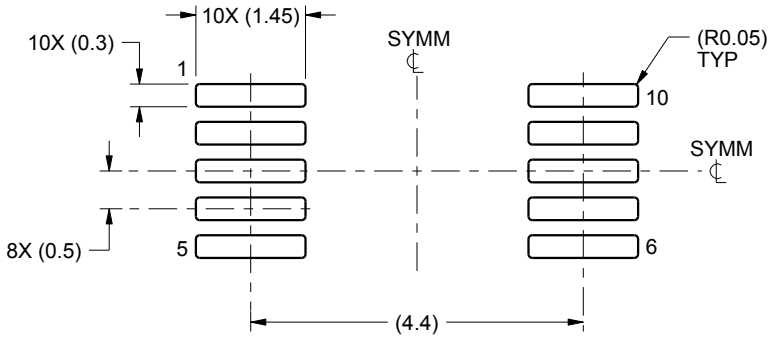
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

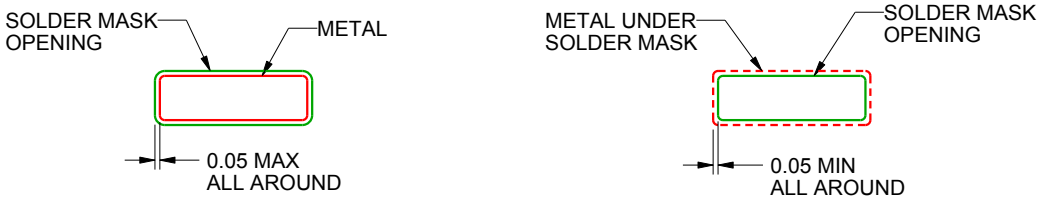


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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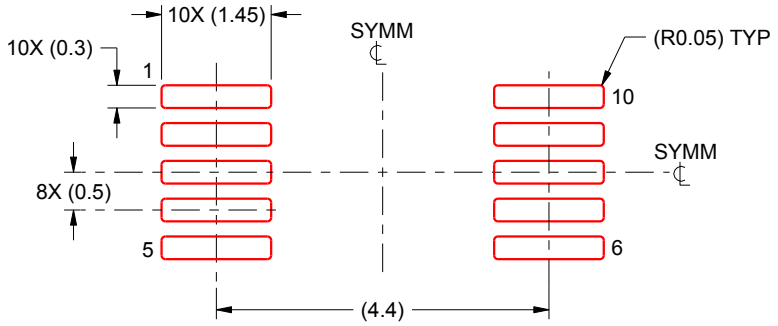
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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