采用 6 引脚 SOT-23 封装的 TPS56x209 4.5V 至 17V 输入、2A、3A 同步降压稳压器

1 特性

- TPS562209 - 集成有 122mΩ 和 72mΩ FET 的 2A 转换器
- TPS563209 - 带有集成 68mΩ 和 39mΩ FET 的 3A 转换器
- D-CAP2™针对快速瞬态响应的模式控制
- 输入电压范围：4.5V 至 17V
- 输出电压范围：0.76V 至 7V
- 650kHz 开关频率
- 低于 10μA 的低关断电流
- 1% 反馈电压精度 (25°C)
- 从预偏置输出电压中启动
- 逐周期过流限制
- 断续模式欠压保护
- 非锁存过压保护 (OVP)，欠压闭锁 (UVLO) 和热关断 (TSD) 保护
- 固定软启动时间：1.0ms

2 应用

- 数字电视电源
- 高清 Blu-ray Disc™播放器
- 网络家庭终端设备
- 数字机顶盒 (STB)

3 说明

TPS562209 和 TPS563209 是采用 6 引脚 SOT-23 封装的简单易用型 2A/3A 同步降压转换器。

此器件被优化为使用尽可能少的外部组件即可运行，并且可以实现低待机电流。

这些开关模式电源 (SMPS) 器件采用 D-CAP2™ 模式控制，从而提供快速瞬态响应，并且在无需外部补偿组件的情况下支持诸如高分子聚合物等低等效串联电阻 (ESR) 输出电容器以及超低 ESR 陶瓷电容器。

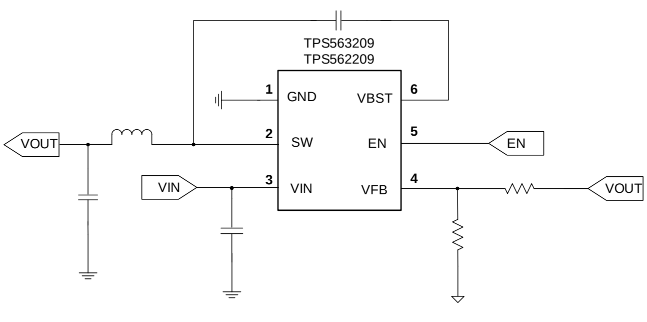
TPS562209 和 TPS563209 始终在连续传导模式下运行，与非连续传导模式相比，该模式可降低轻负载条件下的输出纹波电压。TPS56x209 采用 6 引脚 1.6mm × 2.9mm SOT (DDC) 封装，结温范围为 –40°C 至 150° C。

器件信息(1)

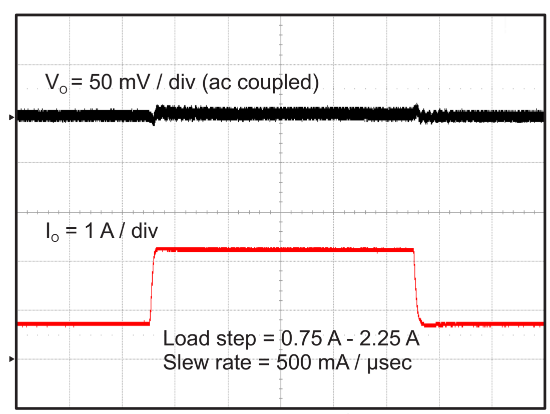
器件型号	封装	封装尺寸（标称值）
TPS563209，TPS562209	SOT (6)	1.60mm x 2.90mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



瞬态响应



English Data Sheet: SLVSCM5

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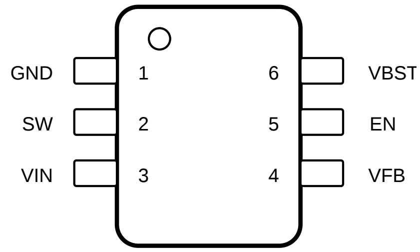
4 修订历史记录

Changes from Original (September 2014) to Revision A	Page
• Updated the Pinout image in Pin Configuration and Functions	3
• Changed the "Handling Ratings" table to the ESD Ratings table	4
• Changed $R_{\theta JB}$ for TPS562209 From: 57.3 To: 13.4 in Thermal Information	4
• The Adaptive On-Time Control and PWM Operation, changed text From: "proportional to the converter input voltage, V_{IN}, and inversely proportional to the output voltage, V_O" To: "inversely proportional to the converter input voltage, V_{IN}, and proportional to the output voltage, V_O"	11

5 Pin Configuration and Functions

DDC Package
6 Pin (SOT)
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins.

6 Specifications

6.1 Absolute Maximum Ratings

T_J = –40°C to 150°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage range	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10 ns transient)	–0.3	27.5	V
	VBST (vs SW)	–0.3	6.5	V
	VFB,	–0.3	6.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_J = -40°C to 150°C (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	17	V
V_I	Input voltage range	VBST	–0.1	23	V
		VBST (10 ns transient)	–0.1	26	
		VBST(vs SW)	–0.1	6.0	
		EN	–0.1	17	
		VFB	–0.1	5.5	
		SW	–1.8	17	
		SW (10 ns transient)	–3.5	20	
T_A	Operating free-air temperature		–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS562209	TPS563209	UNIT
		DDC (6 PINS)		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	109.2	87.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.5	42.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	13.4	13.6	
ψ_{JT}	Junction-to-top characterization parameter	2.3	1.9	
ψ_{JB}	Junction-to-board characterization parameter	60.4	13.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_J = -40°C to 150°C, VIN = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5V, VFB = 0.8 V		650	900	µA
						µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V		3.0	10	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN	1.6			V
V_{ENL}	EN low-level input voltage	EN			0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, continuous mode operation	758	765	772	mV
I_{VFB}	V_{FB} input current	V_{FB} = 0.8V, T_A = 25°C		0	±0.1	mA
MOSFET						
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V (TPS562209)		122		mΩ
		T_A = 25°C, V_{BST} – SW = 5.5 V (TPS563209)		68		
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C (TPS562209)		72		mΩ
		T_A = 25°C (TPS563209)		39		
CURRENT LIMIT						
I_{ocl}	Current limit (1)	DC current, VOUT = 1.05V , L1 = 2.2 µH	2.5	3.2	4.3	A
		DC current, VOUT = 1.05V , L1 = 1.5 µH	3.5	4.2	5.3	
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Shutdown temperature		155		°C
		Hysteresis		35		
ON-TIME TIMER CONTROL						
t_{ON}	On time	VIN = 12 V, VO = 1.05 V		150		ns
$t_{OFF(MIN)}$	Minimum off time	T_A = 25°C, V_{FB} = 0.5 V		260	310	ns
SOFT START						
T_{ss}	Soft –start time	Internal soft-start time, T_A = 25°C	0.7	1.0	1.3	ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP Detect		125%x Vfbth		
V_{UVP}	Output UVP threshold	Hiccup detect		65%xVf bth		
$T_{HiccupOn}$	Hiccup Power On Time	Relative to soft start time		1		ms
$T_{HiccupOff}$	Hiccup Power Off Time	Relative to soft start time		7		ms
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage	3.45	3.75	4.05	V
		Hysteresis VIN voltage	0.13	0.32	0.55	

(1) Not production tested.

6.6 Typical Characteristics TPS562209

V_{IN} = 12V (unless otherwise noted)

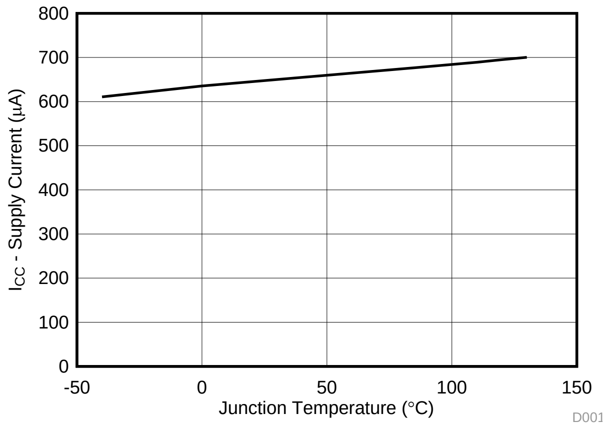


Figure 1. Supply Current vs Junction Temperature

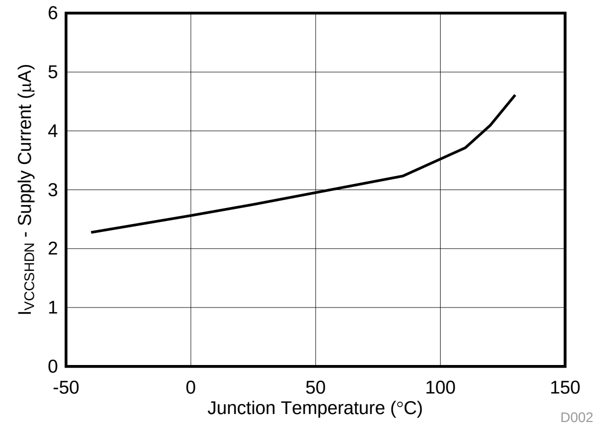


Figure 2. VIN Shutdown Current vs Junction Temperature

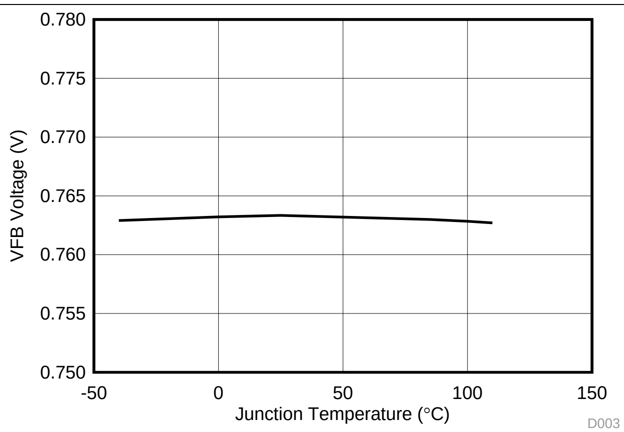


Figure 3. VFB Voltage vs Junction Temperature

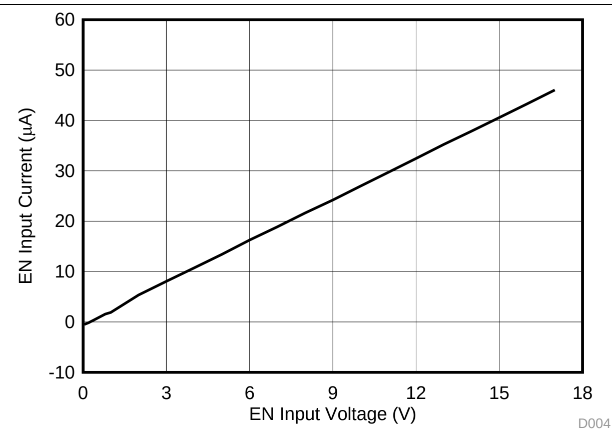


Figure 4. EN Current vs EN Voltage

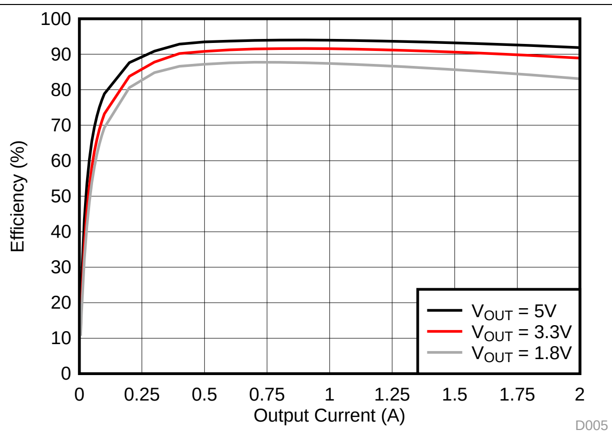


Figure 5. Efficiency vs Output Current

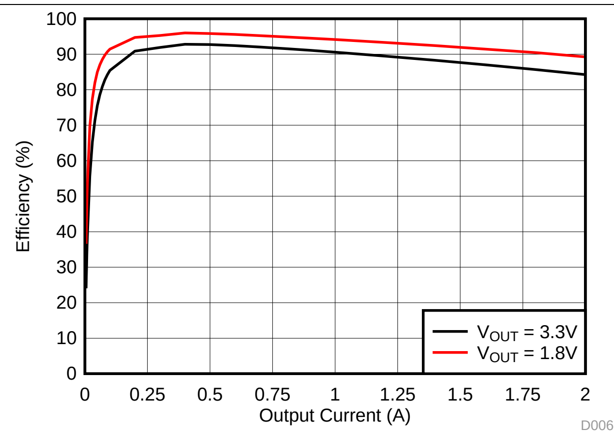


Figure 6. Efficiency vs Output current (V_I = 5 V)

Typical Characteristics TPS562209 (continued)

V_{IN} = 12V (unless otherwise noted)

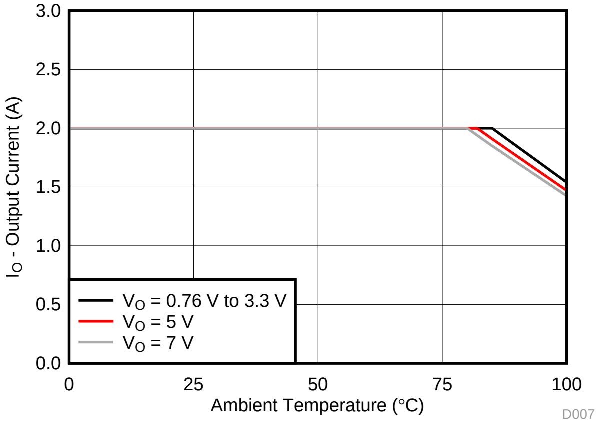


Figure 7. Output Current vs Ambient Temperature

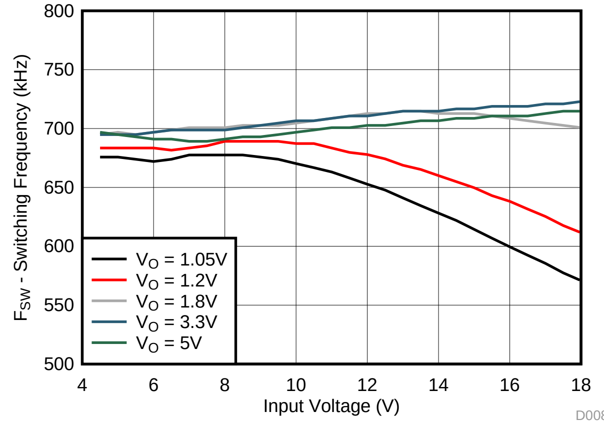


Figure 8. Switching Frequency vs Input Voltage

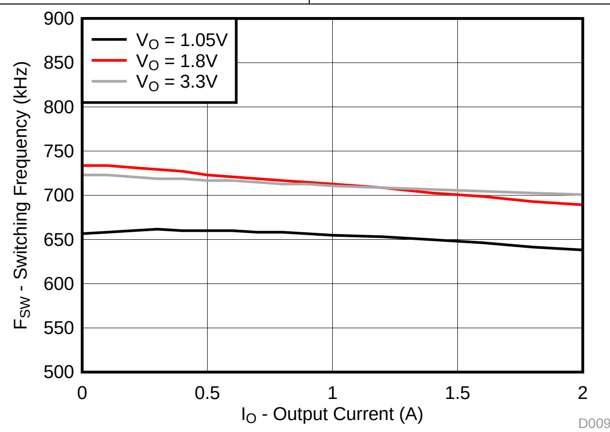


Figure 9. Switching Frequency vs Output Current

6.7 Typical Characteristics TPS563209

V_{IN} = 12V (unless otherwise noted)

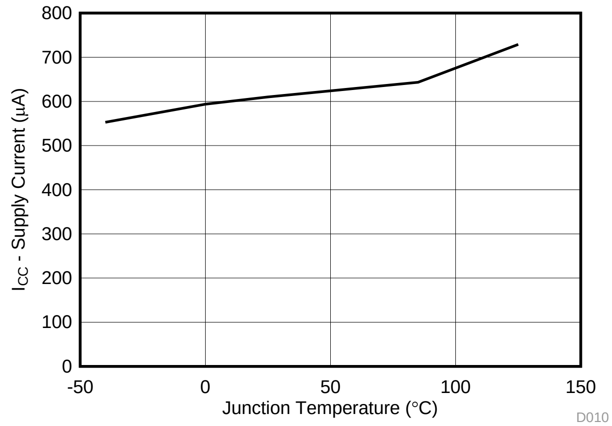


Figure 10. Supply Current vs Junction Temperature

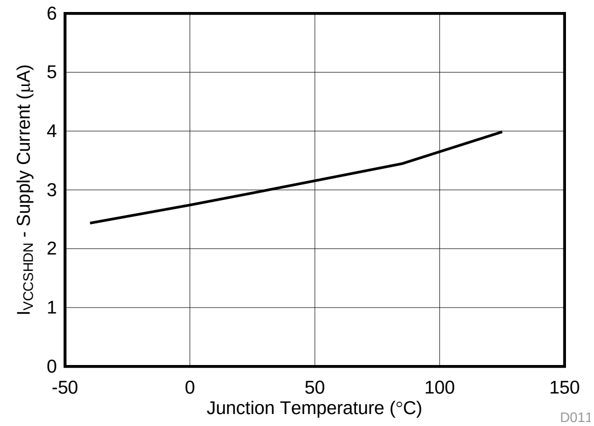


Figure 11. VIN Shutdown Current vs Junction Temperature

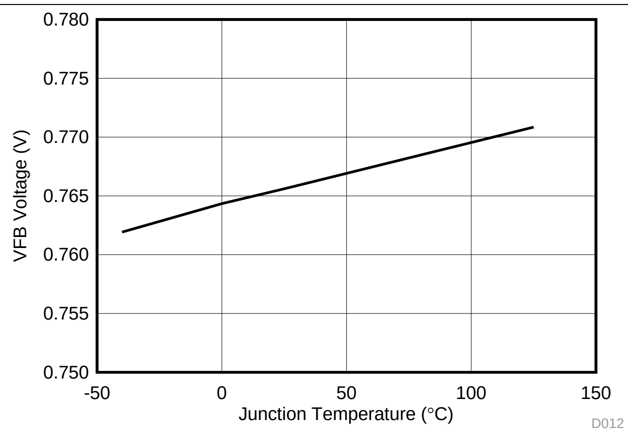


Figure 12. VFB Voltage vs Junction Temperature

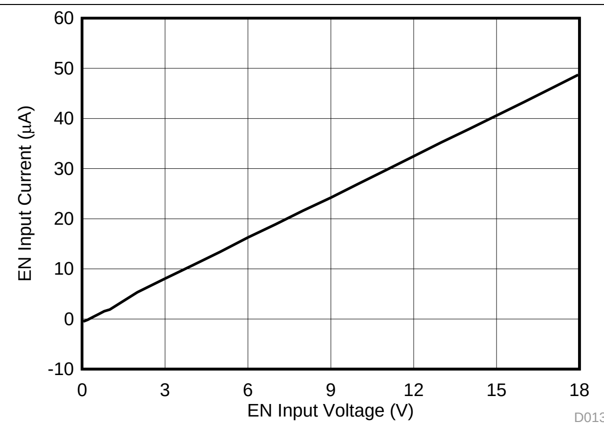


Figure 13. EN Current vs EN Voltage

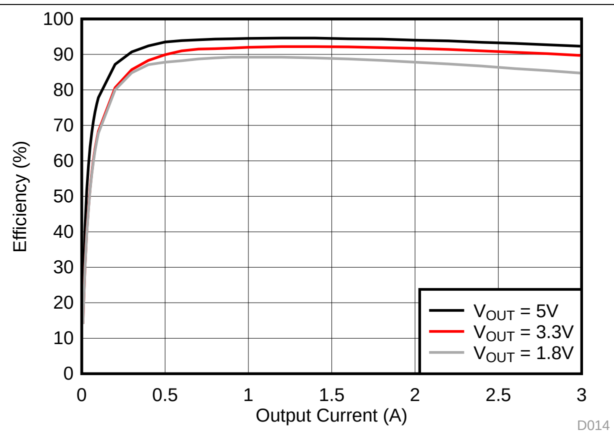


Figure 14. Efficiency vs Output Current

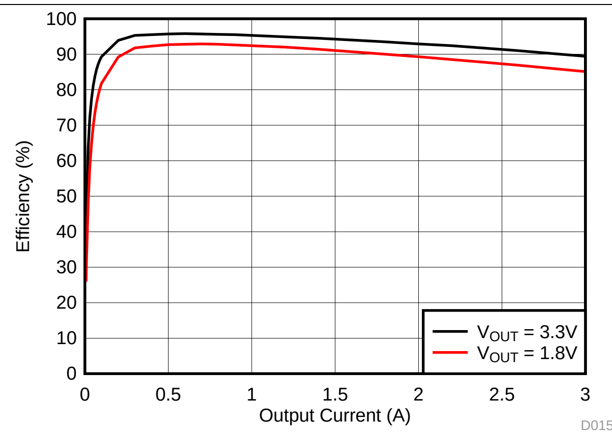


Figure 15. Efficiency vs Output current (V_I = 5 V)

Typical Characteristics TPS563209 (continued)

V_{IN} = 12V (unless otherwise noted)

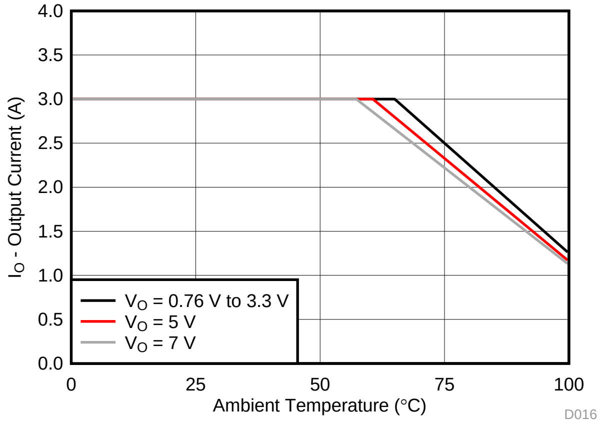


Figure 16. Output Current vs Ambient Temperature

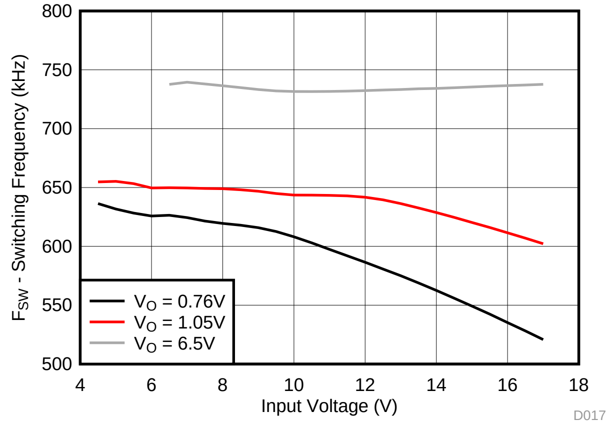


Figure 17. Switching Frequency vs Input Voltage

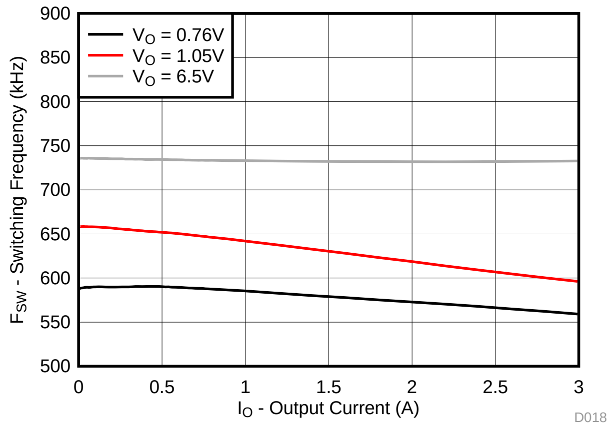


Figure 18. Switching Frequency vs Output Current

7 Detailed Description

7.1 Overview

The TPS562209 and TPS563209 are 2-A and 3-A synchronous step-down converters, respectively. The proprietary D-CAP2™ mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2™ mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram

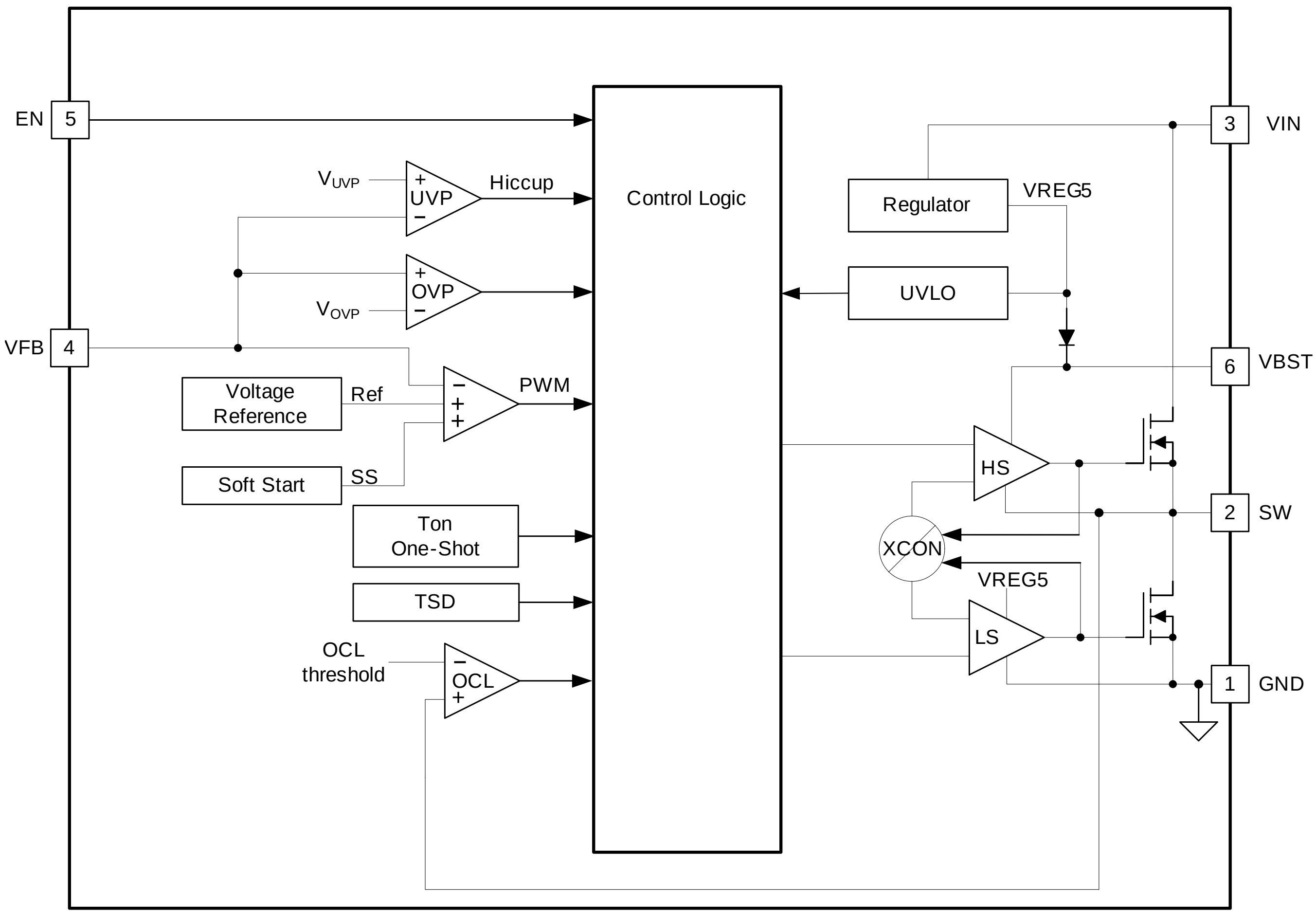


Figure 19. TPS56x209

7.3 Feature Description

7.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPS56x209 are adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. The D-CAP2™ mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set inversely proportional to the converter input voltage, V_{IN}, and proportional to the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

7.3.2 Soft Start and Pre-Biased Soft Start

The TPS562209 and TPS563209 have an internal 1.0ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.3 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value.

During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current Iout. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL threshold is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 14µs) and re-start after the hiccup time (typically 12ms).

When the over current condition is removed, the output voltage returns to the regulated value.

7.3.4 Over Voltage Protection

TPS562209 and TPS563209 detect over voltage condition by monitoring the feedback voltage (VFB). When the feedback voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high and both the high-side MOSFET and the low-side MOSFET turn off. This function is non-latch operation.

7.3.5 UVLO Protection

Under voltage lock out protection (UVLO) monitors the device input voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

Feature Description (continued)

7.3.6 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 155°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS562209 and TPS563209 can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS562209 and TPS563209 operate at a quasi-fixed frequency of 650 kHz.

7.4.2 Forced CCM Operation

When the TPS562209 and TPS563209 are in the normal CCM operating mode and the switch current falls below 0 A, the TPS562209 and TPS563209 begin operating in forced CCM.

7.4.3 Standby Operation

When the TPS562209 and TPS563209 are operating in either normal CCM or forced CCM, they may be placed in standby by asserting the EN pin low.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS562209 and TPS563209 are typically used as step down converters, which convert a voltage from 4.5V - 17V to a lower voltage. Webench software is available to aid in the design and analysis of circuits

8.2 Typical Applications

8.2.1 TPS562209 4.5-V to 17-V Input, 1.05-V Output Converter

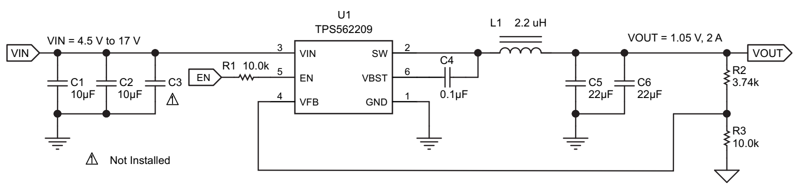


Figure 20. TPS562209 1.05V/2A Reference Design

8.2.1.1 Design Requirements

To begin the design process, you must know a few application parameters:

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	2 A
Output voltage ripple	20 mVpp

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 1 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R2}{R3}\right) \tag{1}$$

8.2.1.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{2}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 2 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 2.

Table 2. Recommended Component Values

OUTPUT VOLTAGE (V)	R2 (kΩ)	R3 (kΩ)	L1 (µH)			C5 + C6 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1.5	2.2	4.7	20 - 68
1.05	3.74	10.0	1.5	2.2	4.7	20 - 68
1.2	5.76	10.0	1.5	2.2	4.7	20 - 68
1.5	9.53	10.0	1.5	2.2	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	2.2	3.3	4.7	20 - 68
3.3	33.2	10.0	2.2	3.3	4.7	20 - 68
5	54.9	10.0	3.3	4.7	4.7	20 - 68
6.5	75	10.0	3.3	4.7	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 3, Equation 4 and Equation 5. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 4 and the RMS current of Equation 5.

$$Il_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{3}$$

$$Il_{PEAK} = I_O + \frac{Il_{P-P}}{2} \tag{4}$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} Il_{P-P}^2} \tag{5}$$

For this design example, the calculated peak current is 2.34 A and the calculated RMS current is 2.01 A. The inductor used is a TDK CLF7045T-2R2N with a peak current rating of 5.5-A and an RMS current rating of 4.3-A

The capacitor value and ESR determines the amount of output voltage ripple. The TPS562209 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20µF to 68µF. Use Equation 6 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{6}$$

For this design two TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.199A and each output capacitor is rated for 4A.

8.2.1.2.3 Input Capacitor Selection

The TPS562209 and TPS563209 require an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.1.2.4 Bootstrap Capacitor Selection

A 0.1µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

8.2.1.3 Application Curves

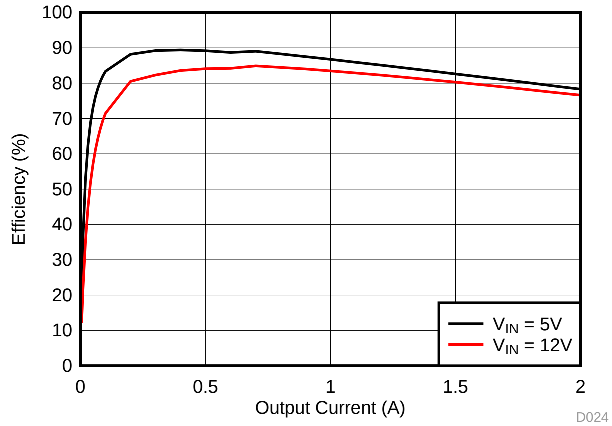


Figure 21. TPS562209 Efficiency

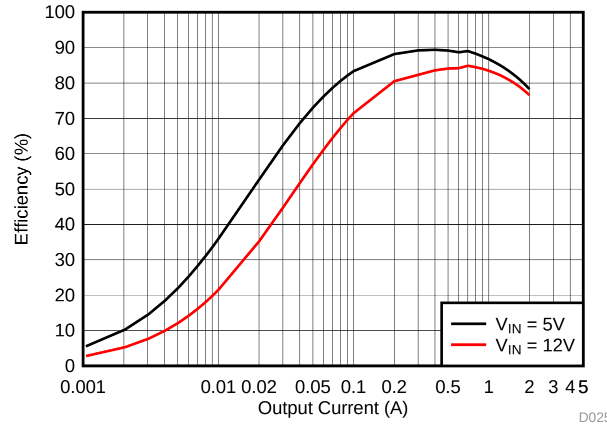


Figure 22. TPS562209 Light Load Efficiency

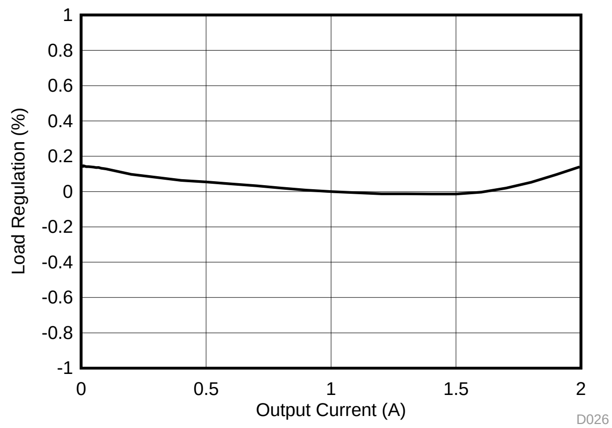


Figure 23. TPS562209 Load Regulation, V_I = 5 V

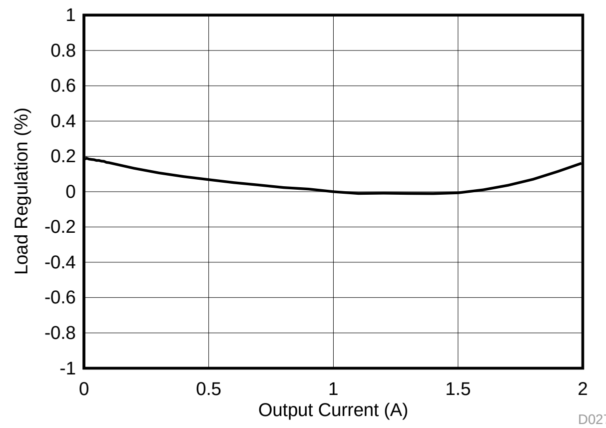


Figure 24. TPS562209 Load Regulation, V_I = 12 V

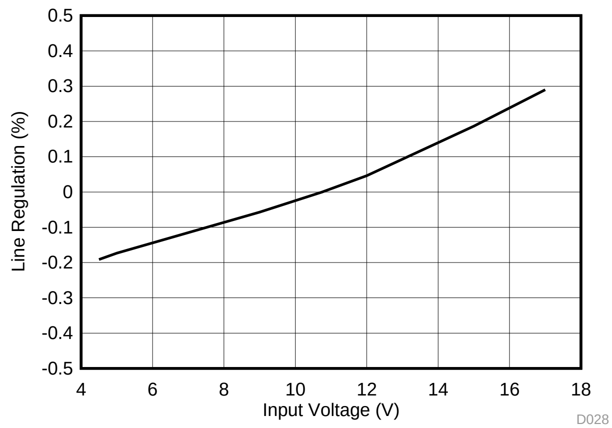


Figure 25. TPS562209 Line Regulation

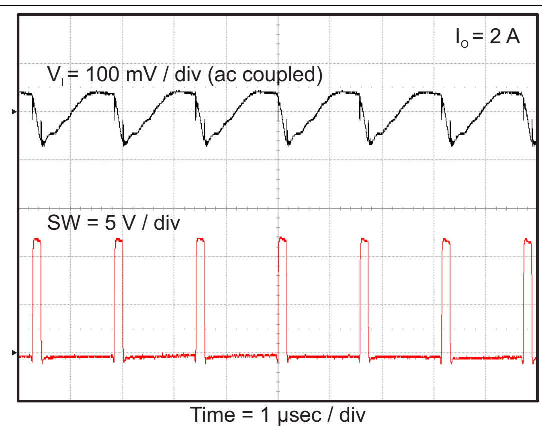


Figure 26. TPS562209 Input Voltage Ripple

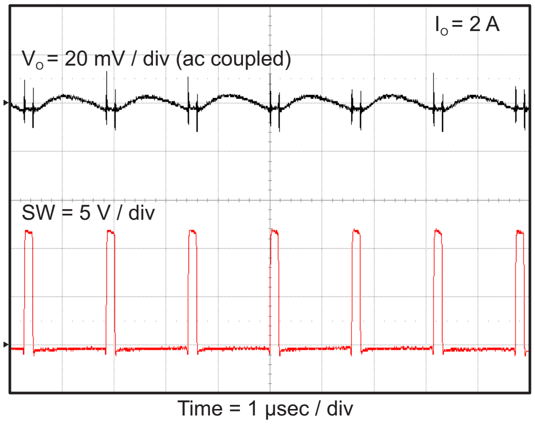


Figure 27. TPS562209 Output Voltage Ripple

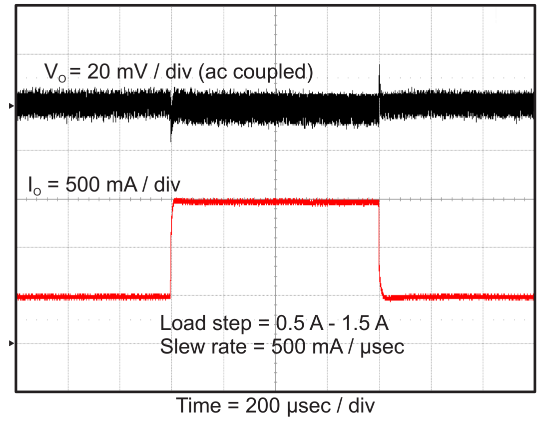


Figure 28. TPS562209 Transient Response

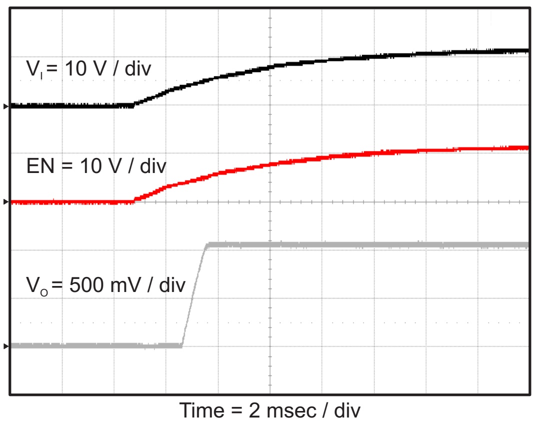


Figure 29. TPS562209 Start Up Relative to V_I

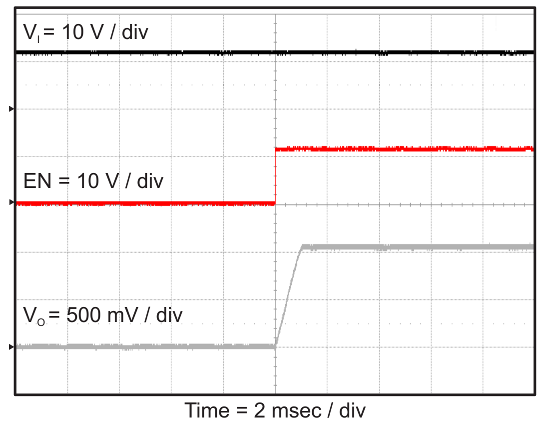


Figure 30. TPS562209 Start Up Relative to EN

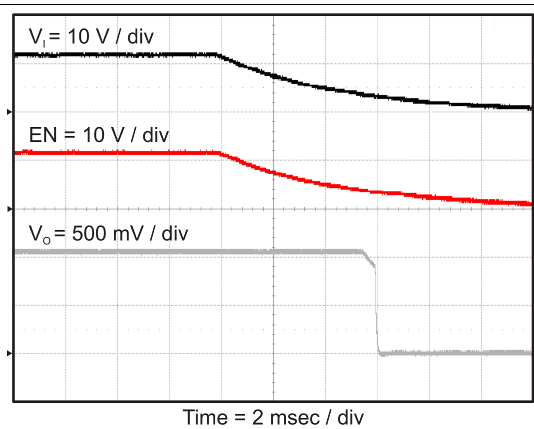


Figure 31. TPS562209 Shut Down Relative to V_I

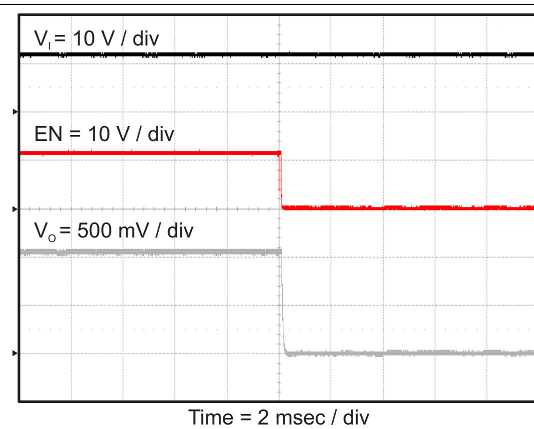


Figure 32. TPS562209 Shut Down Relative to EN

8.2.2 TPS563209 4.5-V to 17-V Input, 1.05-V Output Converter

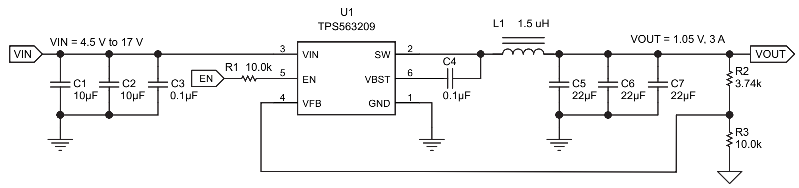


Figure 33. TPS563209 1.05V/3A Reference Design

8.2.2.1 Design Requirements

To begin the design process, the user must know a few application parameters:

Table 3. Design Parameters

PARAMETER	VALUE
Input voltage range	4.5 V to 17 V
Output voltage	1.05 V
Output current	3 A
Output voltage ripple	20 mVpp

8.2.2.2 Detailed Design Procedures

The detailed design procedure for TPS563209 is the same as for TPS562209 except for inductor selection.

8.2.2.2.1 Output Filter Selection

Table 4. Recommended Component Values

OUTPUT VOLTAGE (V)	R2 (kΩ)	R3 (kΩ)	L1 (µH)			C5 +C6 + C7 (µF)
			MIN	TYP	MAX	
1	3.09	10.0	1.0	1.5	4.7	20 - 68
1.05	3.74	10.0	1.0	1.5	4.7	20 - 68
1.2	5.76	10.0	1.0	1.5	4.7	20 - 68
1.5	9.53	10.0	1.0	1.5	4.7	20 - 68
1.8	13.7	10.0	1.5	2.2	4.7	20 - 68
2.5	22.6	10.0	1.5	2.2	4.7	20 - 68
3.3	33.2	10.0	1.5	2.2	4.7	20 - 68
5	54.9	10.0	2.2	3.3	4.7	20 - 68
6.5	75	10.0	2.2	3.3	4.7	20 - 68

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 7, Equation 8 and Equation 9. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{SW}.

Use 650 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 8 and the RMS current of Equation 9.

$$Il_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (7)$$

$$Il_{PEAK} = I_O + \frac{Il_{P-P}}{2} \quad (8)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I I_{P-P}^2} \tag{9}$$

For this design example, the calculated peak current is 3.505 A and the calculated RMS current is 3.014 A. The inductor used is a TDK CLF7045T-1R5N with a peak current rating of 7.3-A and an RMS current rating of 4.9-A

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563209 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20µF to 68µF. Use Equation 6 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \tag{10}$$

For this design three TDK C3216X5R0J226M 22µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.292A and each output capacitor is rated for 4A.

8.2.2.3 Application Curves

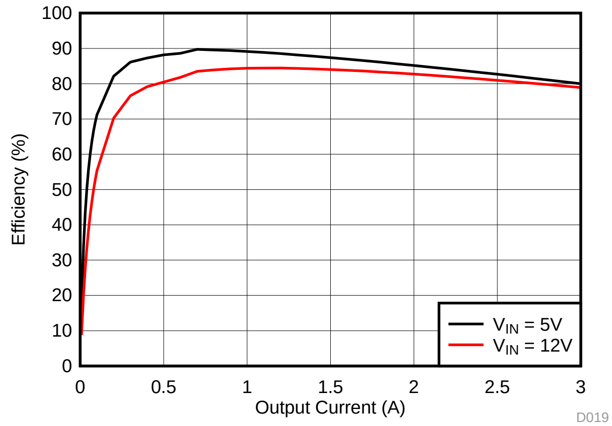


Figure 34. TPS563209 Efficiency

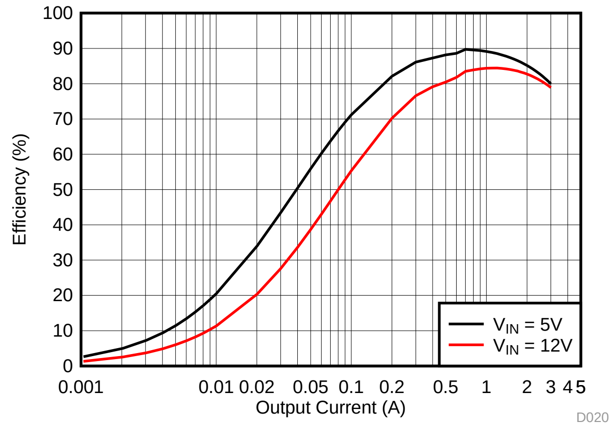


Figure 35. TPS563209 Light Load Efficiency

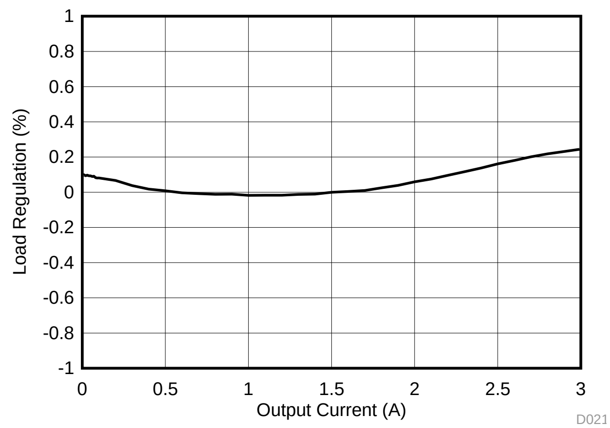


Figure 36. TPS563209 Load Regulation, V_I = 5 V

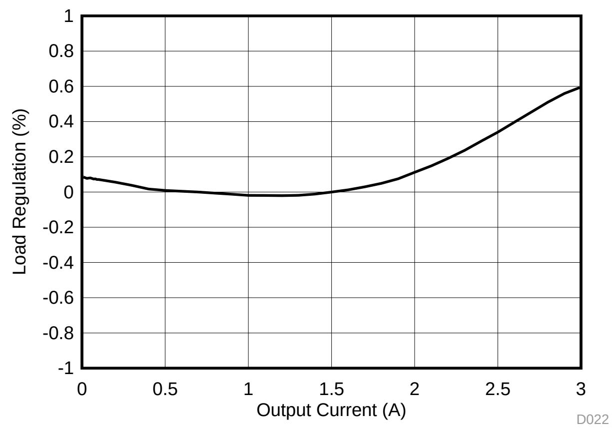


Figure 37. TPS563209 Load Regulation, V_I = 12 V

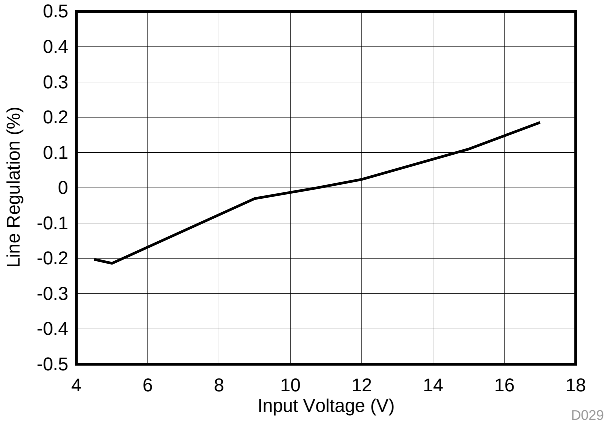


Figure 38. TPS563209 Line Regulation

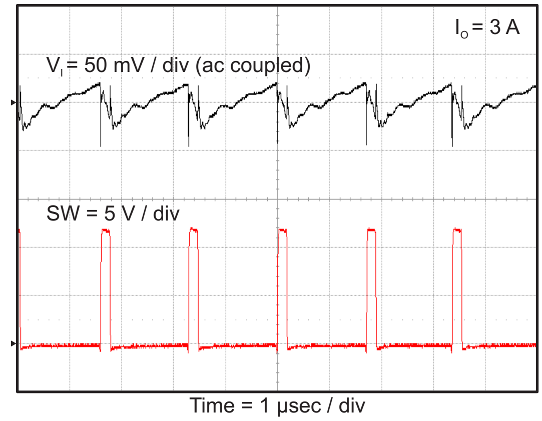


Figure 39. TPS563209 Input Voltage Ripple

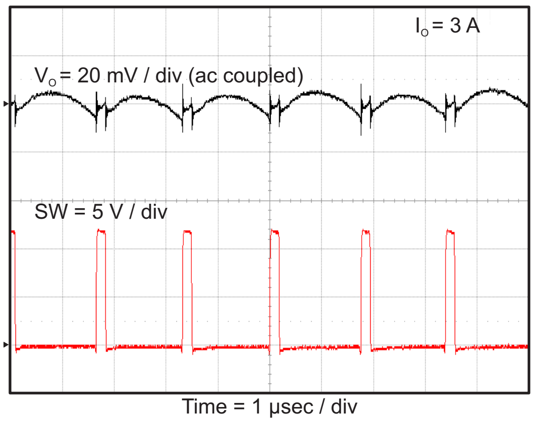


Figure 40. TPS563209 Output Voltage Ripple

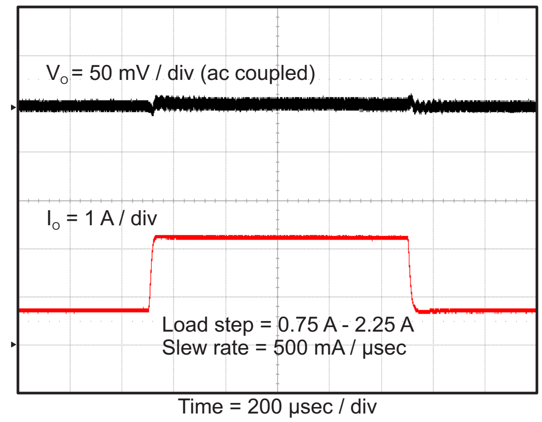


Figure 41. TPS563209 Transient Response

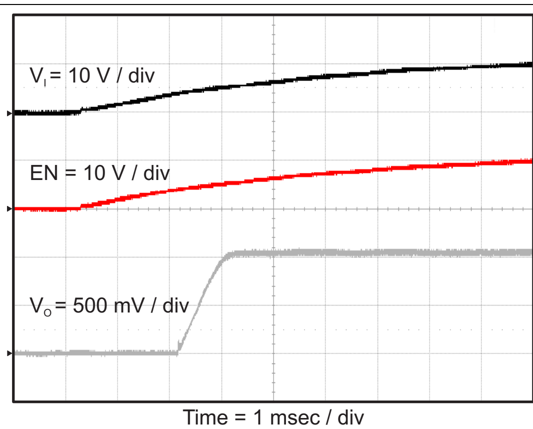


Figure 42. TPS563209 Start Up Relative to V_I

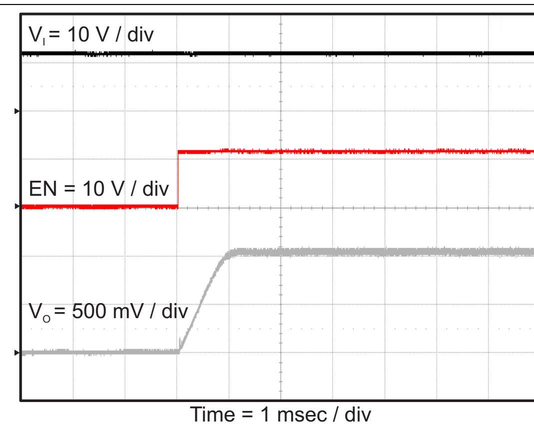


Figure 43. TPS563209 Start Up Relative to EN

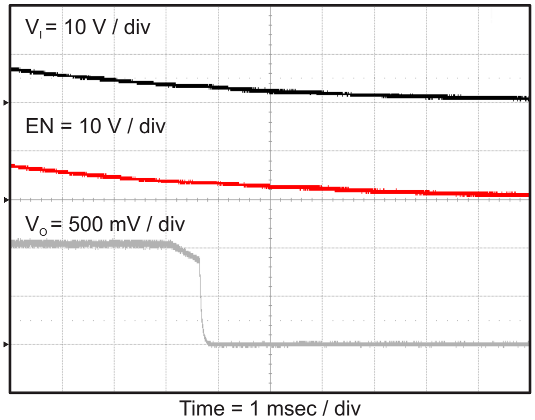


Figure 44. TPS563209 Shut Down Relative to V_I

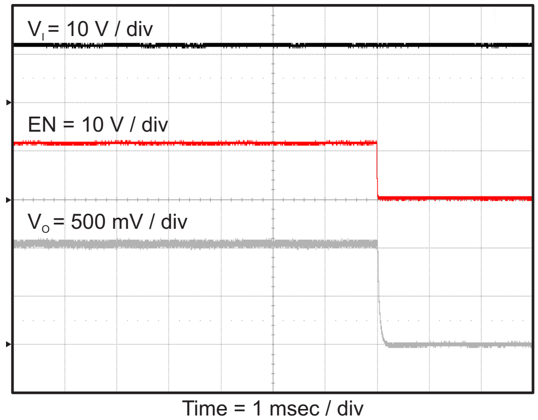


Figure 45. TPS563209 Shut Down Relative to EN

9 Power Supply Recommendations

The TPS562209 and TPS563209 are designed to operate from input supply voltage in the range of 4.5V to 17V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 65%. Using that criteria, the minimum recommended input voltage is V_O / 0.65.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

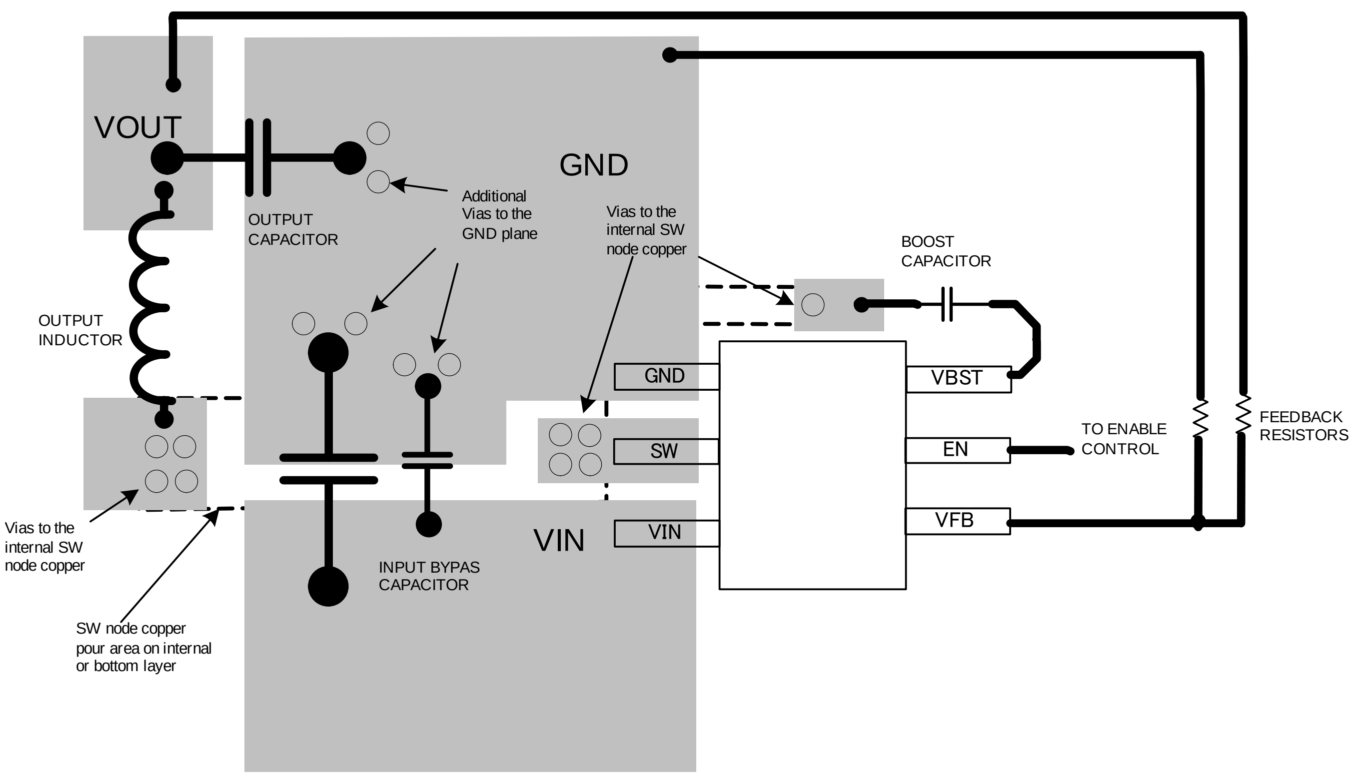


Figure 46. TPS562209 and TPS563209 Layout

11 器件和文档支持

11.1 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 **5.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS563209	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS562209	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

D-CAP2, E2E are trademarks of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc Association.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS562209DDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	209
TPS562209DDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	209
TPS562209DDCR.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	209
TPS562209DDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	Call TI | Sn	Level-1-260C-UNLIM	-40 to 125	209
TPS562209DDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	209
TPS562209DDCT.B	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	209
TPS563209DDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	309
TPS563209DDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	309
TPS563209DDCR.B	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	309
TPS563209DDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	309
TPS563209DDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	309
TPS563209DDCT.B	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	309

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

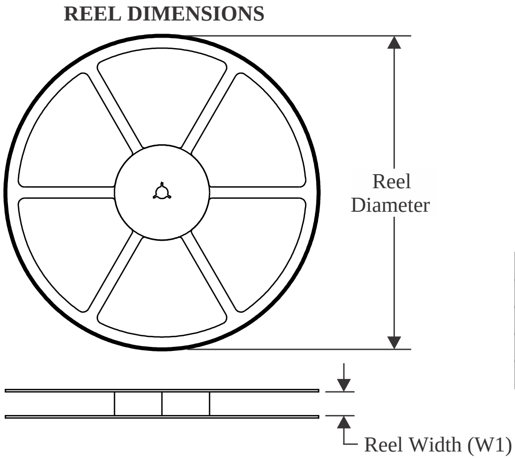
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

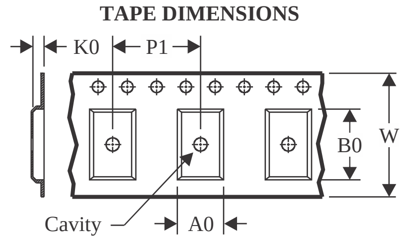
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

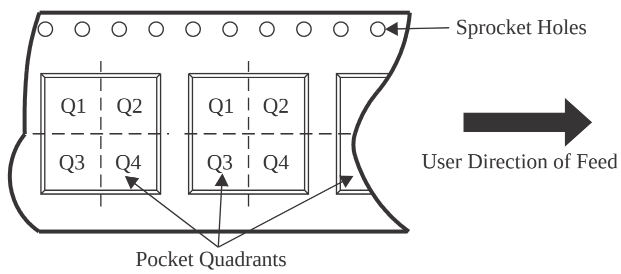
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

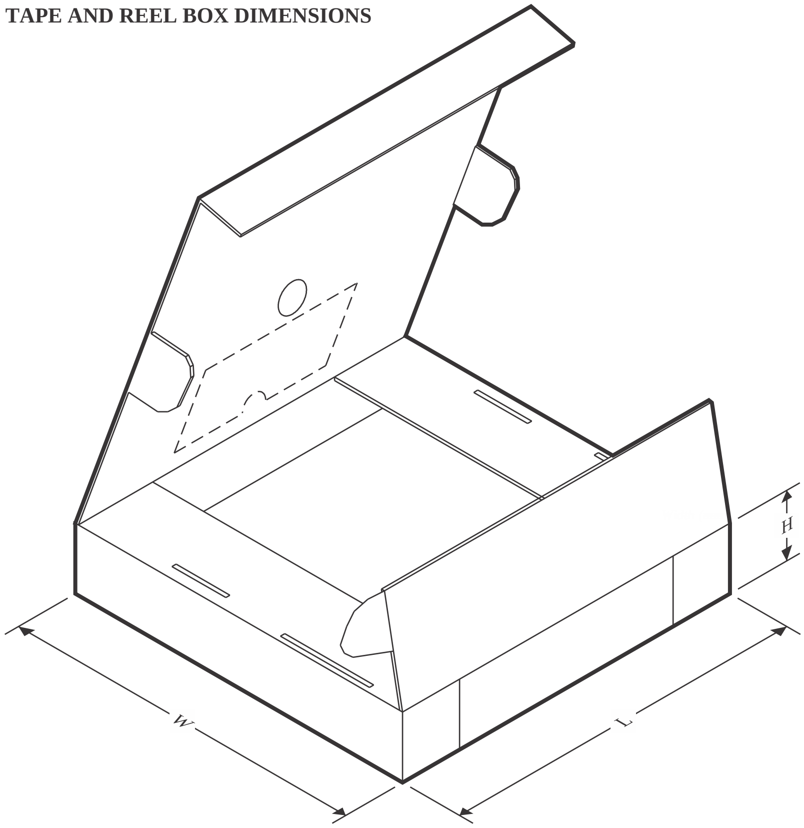
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

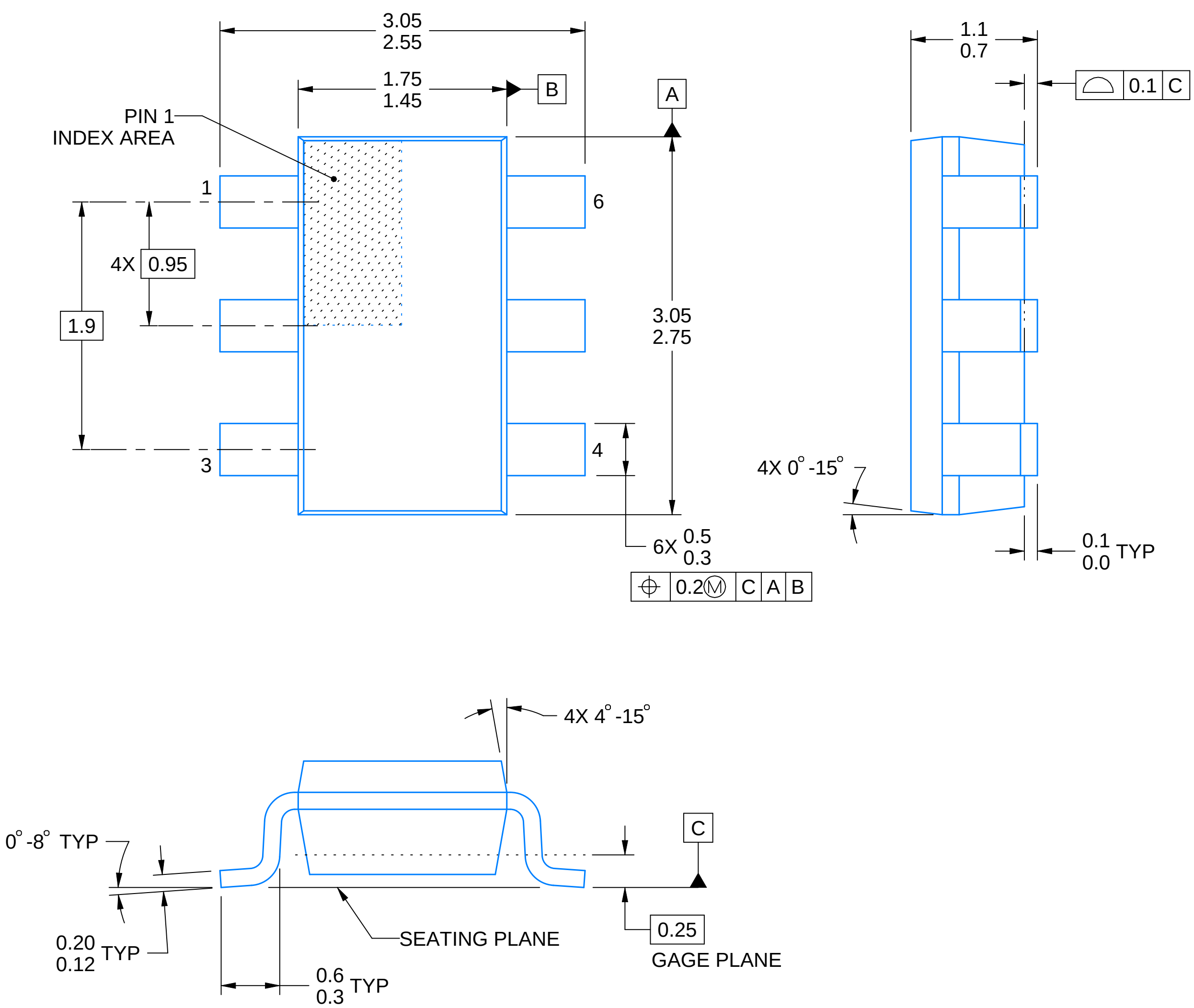
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS562209DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS562209DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563209DDCR	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS563209DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS562209DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS562209DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0
TPS563209DDCR	SOT-23-THIN	DDC	6	3000	210.0	185.0	35.0
TPS563209DDCT	SOT-23-THIN	DDC	6	250	210.0	185.0	35.0



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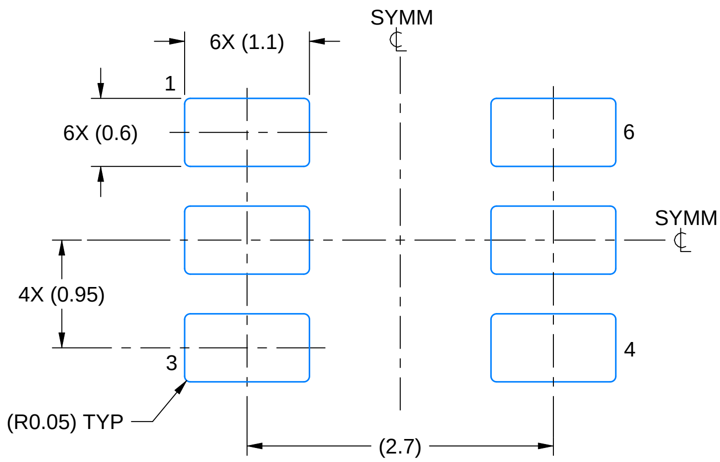
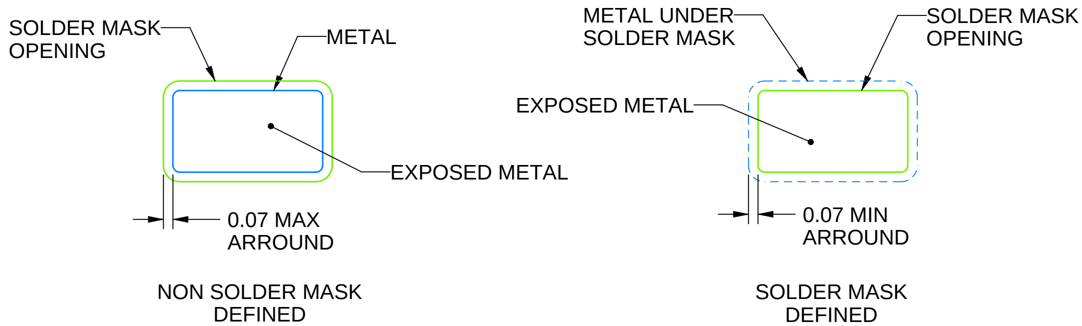
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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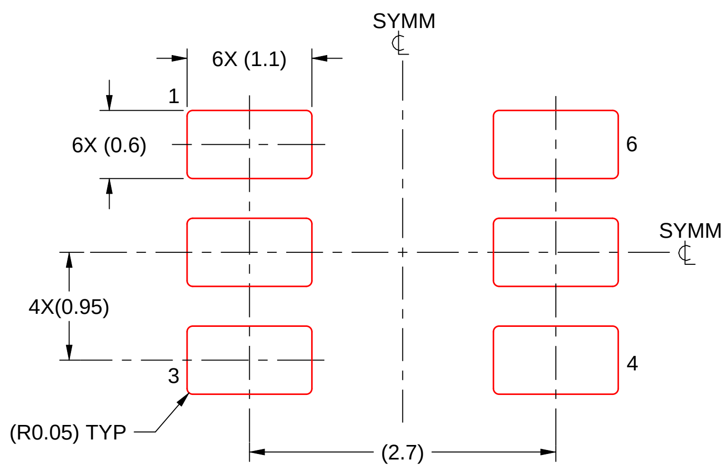
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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