

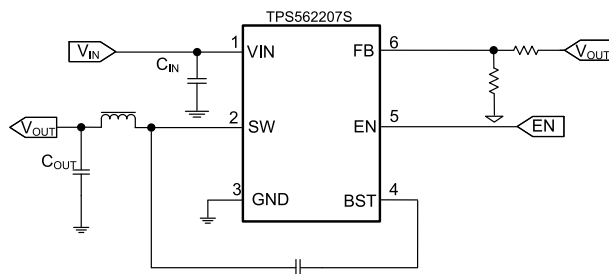
采用 SOT563 封装的 TPS562207S 4.3V 至 17V 输入、2A FCCM 模式 同步降压转换器

1 特性

- 带集成 140mΩ 和 84mΩ FET 的 2A 转换器
- 具有快速瞬态响应的 D-CAP2™ 模式控制
- 输入电压范围：4.3V 至 17V
- 输出电压范围：0.804V 至 7V
- 强制连续导通模式
- 580kHz 开关频率
- 小于 3μA 的低关断电流
- 1.5% 反馈电压精度 (25°C)
- 支持预偏置启动
- 逐周期过流限制
- 断续模式过流保护
- 非锁存欠压保护 (UVP) 和热关断 (TSD) 保护
- 固定软启动：1.2ms

2 应用

- 电视 SMPS 电源
- 智能扬声器
- 有线网络
- 数字机顶盒 (STB)
- 监控



简化版原理图

3 说明

TPS562207S 是一款采用 SOT563 封装的简单易用型 2A 同步降压转换器。

该器件经过优化，更大幅度地减少了运行所需的外部器件并可实现低待机电流。

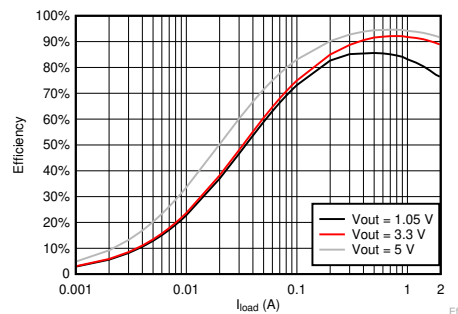
该开关模式电源 (SMPS) 器件采用 D-CAP2 模式控制，能够提供快速瞬态响应，并且在无需外部补偿器件的情况下支持专用聚合物等低等效串联电阻 (ESR) 输出电容以及超低 ESR 陶瓷电容器。

TPS562207S 采用强制连续导通模式 (FCCM) 运行，从而保持固定的开关频率并实现很小的输出电压纹波。TPS562207S 采用 6 引脚 1.6mm × 1.6mm SOT563 (DRL) 封装，额定结温范围为 -40°C 至 125°C。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TPS562207S	DRL (6)	1.60mm x 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



TPS562207S 效率



Table of Contents

1 特性	1	8.4 Device Functional Modes.....	11
2 应用	1	9 Application and Implementation	12
3 说明	1	9.1 Application Information.....	12
4 Revision History	2	9.2 Typical Application.....	12
5 Device Comparison Table	2	10 Power Supply Recommendations	16
6 Pin Configuration and Functions	3	11 Layout	17
7 Specifications	4	11.1 Layout Guidelines.....	17
7.1 Absolute Maximum Ratings.....	4	11.2 Layout Example.....	17
7.2 ESD Ratings.....	4	12 Device and Documentation Support	18
7.3 Recommended Operating Conditions.....	4	12.1 Receiving Notification of Documentation Updates..	18
7.4 Thermal Information.....	4	12.2 Support Resources.....	18
7.5 Electrical Characteristics.....	5	12.3 Trademarks.....	18
7.6 Typical Characteristics.....	7	12.4 Electrostatic Discharge Caution.....	18
8 Detailed Description	10	12.5 Glossary.....	18
8.1 Overview.....	10	13 Mechanical, Packaging, and Orderable Information	18
8.2 Functional Block Diagram.....	10		
8.3 Feature Description.....	10		

4 Revision History

DATE	REVISION	NOTES
October 2020	*	Initial release

5 Device Comparison Table

PART NUMBER	WORK MODE AT LIGHT LOADING
TPS562202S	ECO
TPS562207S	FCCM

6 Pin Configuration and Functions

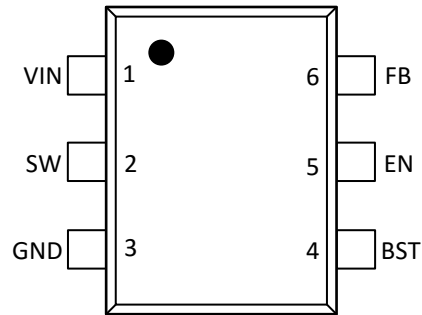


图 6-1. 6-Pin SOT563 DRL Package (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	Input voltage supply pin
SW	2	O	Switch node connection between high-side NFET and low-side NFET
GND	3	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive FB to this GND at a single point.
BST	4	O	Supply input for the high-side NFET gate drive circuit. Connect a 0.1- μ F capacitor between the BST and SW pin.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
FB	6	I	Converter feedback input. Connect to output voltage with feedback resistor divider.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	VIN, EN	- 0.3	19	V
	BST	- 0.3	25	V
	BST (10 ns transient)	- 0.3	27	V
	BST (vs SW)	- 0.3	6.5	V
	FB	- 0.3	6.5	V
	SW	- 2	19	V
	SW (10 ns transient)	- 3.5	21	V
Operating junction temperature, T _J		- 40	150	°C
Storage temperature, T _{stg}		- 55	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Supply input voltage range	4.3		17	V
V _I	Input voltage range	BST		23	V
		BST (10 ns transient)	- 0.1	26	
		BST (vs SW)	- 0.1	6	
		EN	- 0.1	17	
		FB	- 0.1	5.5	
		SW	- 1.8	17	
		SW (10 ns transient)	- 3.5	20	
T _J	Operating junction temperature	- 40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS562207S	UNIT
		DRL	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	141.0	°C/W
R _{θJA_effective}	Junction-to-ambient thermal resistance with TI EVM board ⁽²⁾	75	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	42.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	25.5	°C/W

THERMAL METRIC ⁽¹⁾		TPS562207S	
		DRL	
		6 PINS	
			UNIT
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) This $R_{\theta JA_effective}$ is tested on TI EVM board(2 layer, copper thickness is 2 OZ) at $V_{IN} = 12V$, $V_{OUT} = 5V$, $I_{OUT} = 2A$, $T_A = 25^{\circ}C$.

7.5 Electrical Characteristics

$T_J = -40^{\circ}C$ to $125^{\circ}C$, $V_{IN} = 12 V$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating - non-switching supply current	V_{IN} current, $EN = 5 V$, $V_{FB} = 1 V$		590	750	μA
I_{VINSN}	Shutdown supply current	V_{IN} current, $EN = 0 V$		1	3	μA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN		1.35	1.6	V
V_{ENL}	EN low-level input voltage	EN	0.8	1.05		V
R_{EN}	EN pin resistance to GND	$V_{EN} = 12 V$	225	400	900	$k\Omega$
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE						
V_{FBTH}	V_{FB} threshold voltage	$T_A = 25^{\circ}C$	792	804	816	mV
I_{FB}	V_{FB} input current	$V_{FB} = 1 V$		0	± 0.1	μA
MOSFET						
$R_{DS(on)h}$	High-side switch resistance	$T_A = 25^{\circ}C$, $V_{BST} - SW = 5.5 V$		140		$m\Omega$
$R_{DS(on)l}$	Low-side switch resistance	$T_A = 25^{\circ}C$		84		$m\Omega$
CURRENT LIMIT						
$I_{ocL_l_source}$	Low side FET source current limit		2.24	3.1	4	A
$I_{NoCL_l_sink}$	Low side FET sink current limit			1.1		A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold ⁽¹⁾	Shutdown temperature		160		°C
		Hysteresis		25		
ON-TIME TIMER CONTROL						
$t_{OFF(MIN)}$	Minimum off time	$V_{FB} = 0.5 V$		220	310	ns
SOFT START						
T_{SS}	Soft-start time	Internal soft-start time, Test Vout from 10% to 90%		1.2		ms
FREQUENCY						
F_{sw}	Switching frequency	$V_O = 1.05 V$		580		kHz
OUTPUT UNDERVOLTAGE						
V_{UVP}	Output UVP threshold	Hiccup detect ($H > L$)		65%		
T_{HICCUP_WAIT}	Hiccup on time			2.2		ms
T_{HICCUP_RE}	Hiccup time before restart			18		ms
UVLO						

T_J = -40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UVLO	UVLO threshold	Wake up VIN voltage		4.0	4.3	V
		Shutdown VIN voltage	3.3	3.6		
		Hysteresis VIN voltage		0.4		

(1) Not production tested.

7.6 Typical Characteristics

$V_{IN} = 12\text{ V}$ (unless otherwise noted)

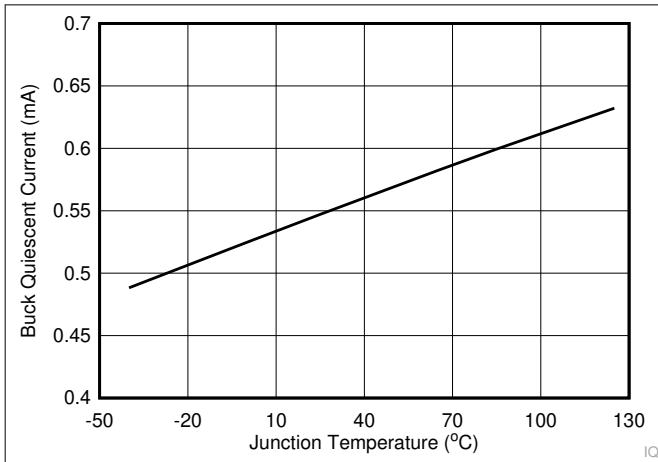


图 7-1. Supply Current vs Junction Temperature

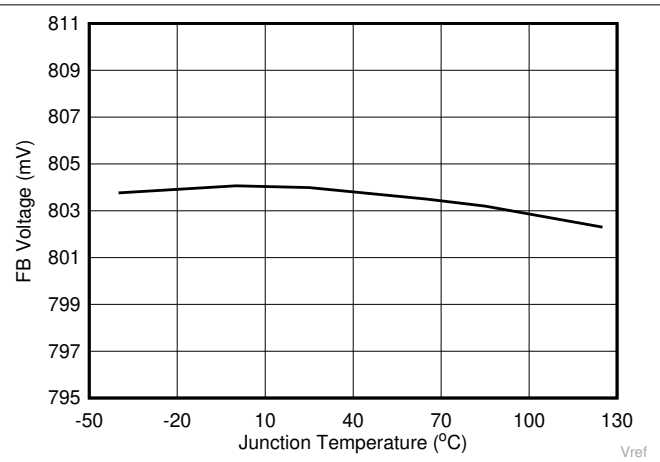


图 7-2. FB Voltage vs Junction Temperature

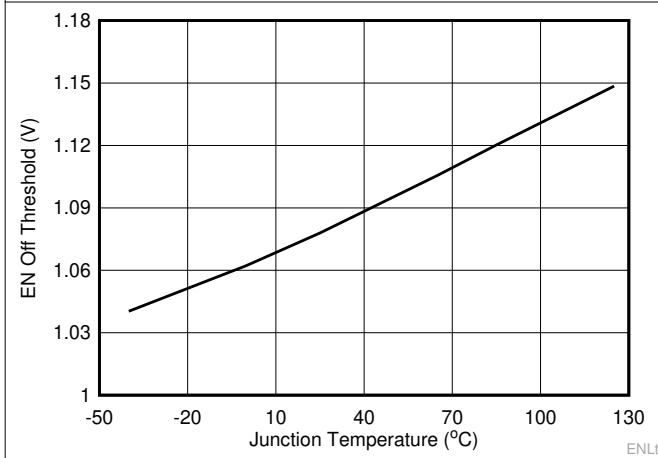


图 7-3. EN Off-threshold Voltage vs Junction Temperature

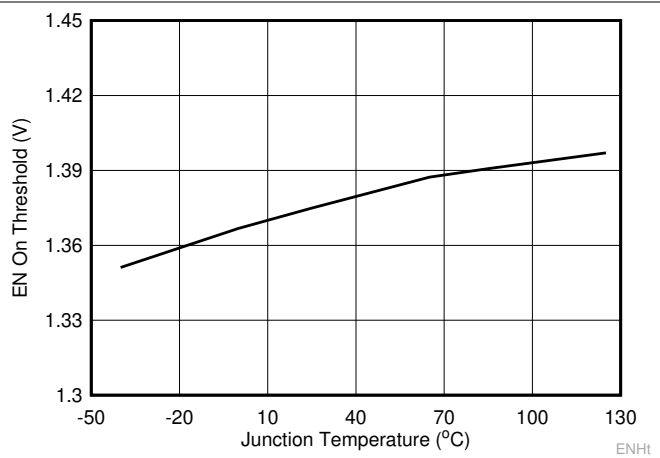


图 7-4. EN On-threshold Voltage vs Junction Temperature

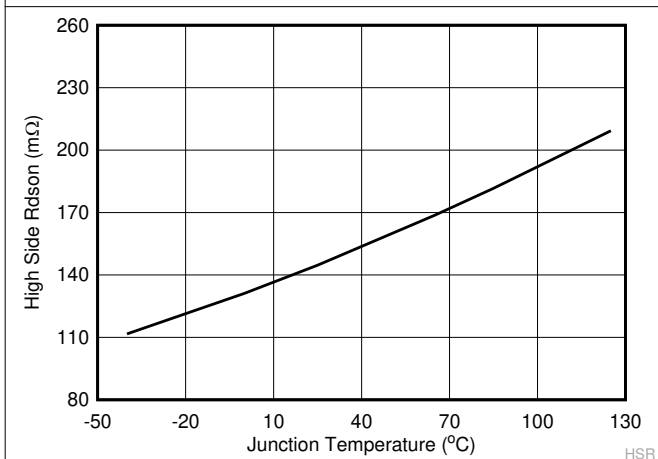


图 7-5. High-Side R_{ds-On} vs Junction Temperature

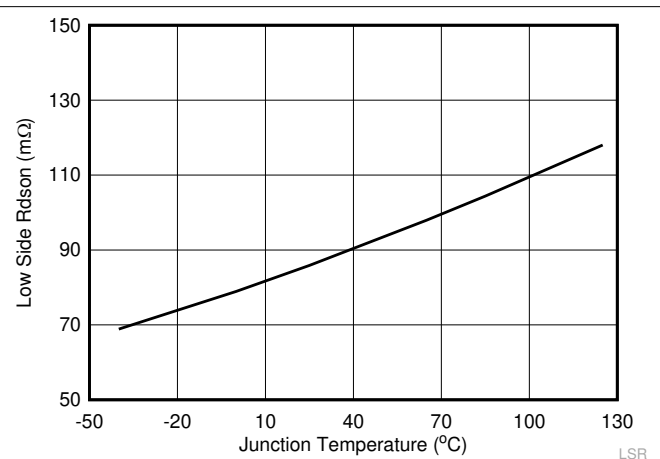


图 7-6. Low-Side R_{ds-On} vs Junction Temperature

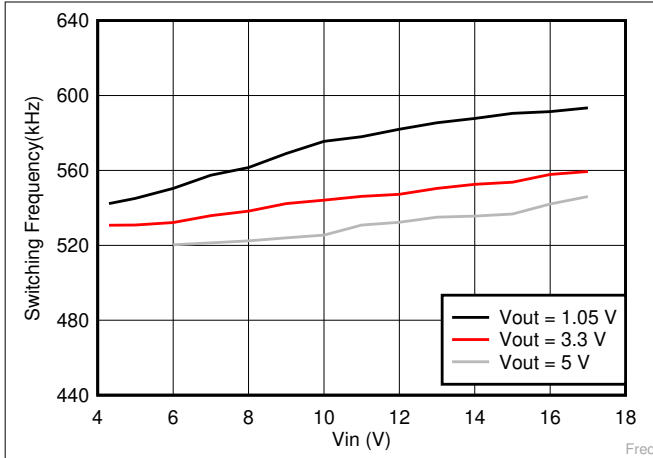


图 7-7. Switching Frequency vs Input Voltage

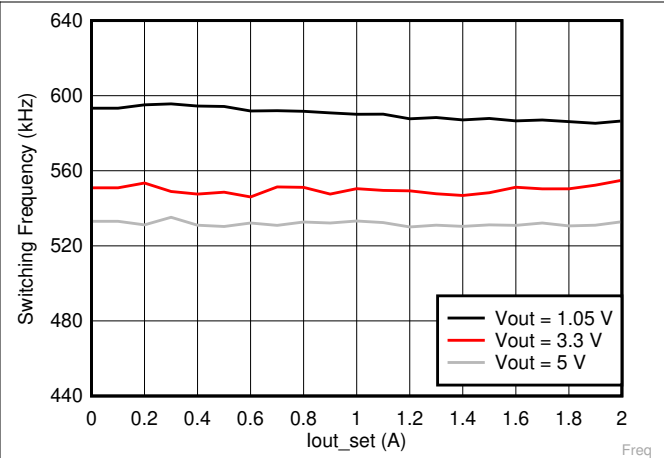


图 7-8. Switching Frequency vs Output Current

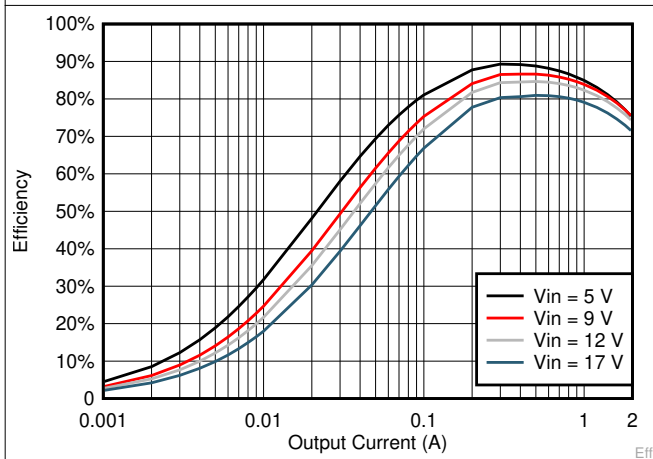


图 7-9. $V_{OUT} = 0.95\text{ V}$ Efficiency, $L = 2.2\ \mu\text{H}$

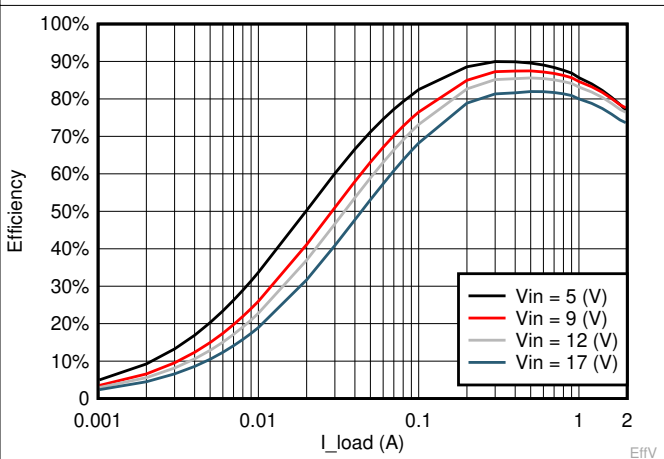


图 7-10. $V_{OUT} = 1.05\text{ V}$ Efficiency, $L = 2.2\ \mu\text{H}$

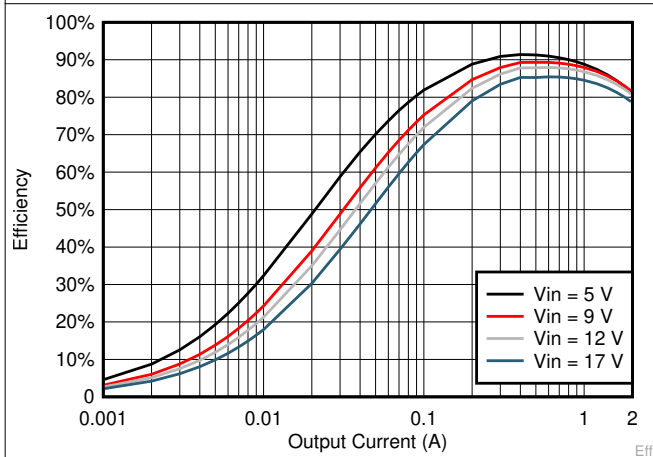


图 7-11. $V_{OUT} = 1.5\text{ V}$ Efficiency, $L = 2.2\ \mu\text{H}$

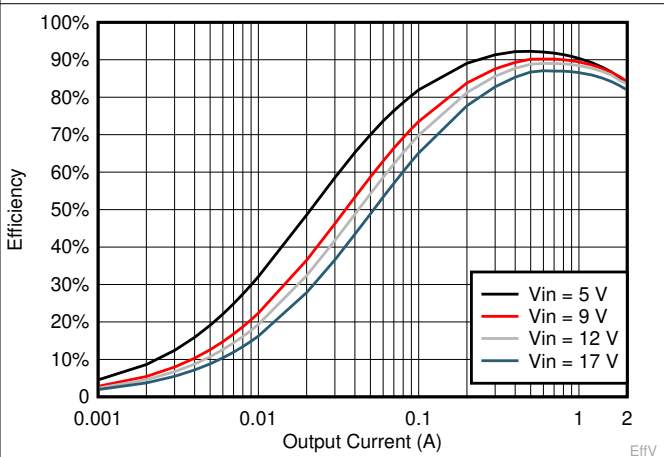
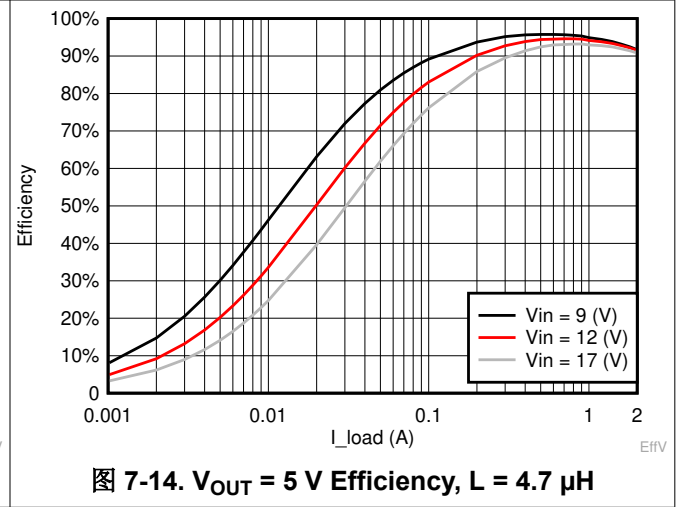
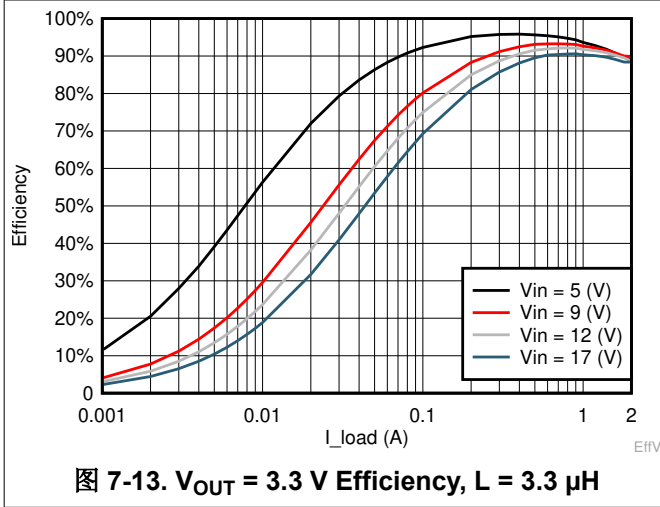


图 7-12. $V_{OUT} = 1.8\text{ V}$ Efficiency, $L = 2.2\ \mu\text{H}$

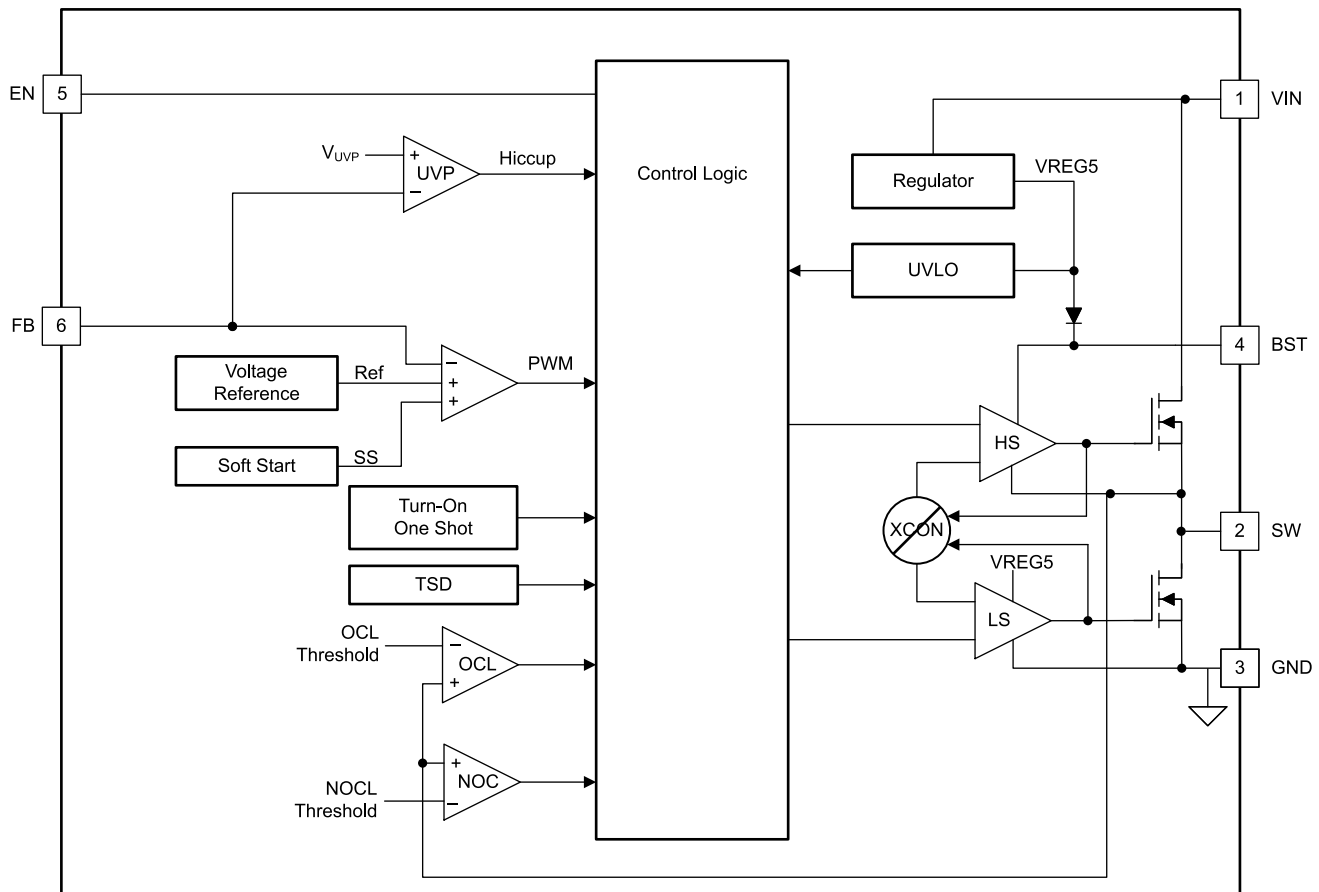


8 Detailed Description

8.1 Overview

The TPS562207S is a 2-A synchronous buck converter. The proprietary D-CAP2 mode control supports low-ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2 mode control can reduce the output capacitance required to meet a specific level of performance.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS562207S is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. The D-CAP2 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after an internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, V_{IN} , and inversely proportional to the output voltage, V_O , to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

8.3.2 Soft Start and Pre-Biased Soft Start

The TPS562207S have an internal 1.2-ms soft start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at start-up, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage, V_{FB} . This scheme ensures that the converters ramp up smoothly into regulation point.

8.3.3 Current Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain-to-source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN} , V_{out} , the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{out} . If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter. This can cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device shuts down after the UVP delay time (typically 24 μ s) and re-starts after the hiccup time (typically 18 ms).

When the overcurrent condition is removed, the output voltage returns to the regulated value.

The TPS562207S works in Forced Continuous Conduction Mode (FCCM). To support light load operation, the current flowing through low-side FET is allowed to be negative, which means the current flow from drain-to-source of low-side FET. This negative current is compared with low-side FET sink current limit to prevent device from being over-current damaged. Once the sink current crosses the limit, the low-side FET turns off and the high-side FET turns on to limit the negative current from overcurrent.

8.3.4 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

8.3.5 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 160°C), the device is shut off. This is a non-latch protection. The device will resume normal working once the temperature return below the recovery threshold value (typically 135°C).

8.4 Device Functional Modes

8.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS562207S can operate in their normal switching modes. In continuous conduction mode (CCM), the TPS562207S operates at a quasi-fixed frequency of 580 kHz.

8.4.2 Standby Operation

The TPS562207S can be placed in standby mode by asserting the EN pin low.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The devices are typical buck DC-DC converters. It typically uses to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 2 A. The following design procedure can be used to select component values for the TPS562207S. This section presents a simplified discussion of the design process.

9.2 Typical Application

The application schematic in [图 9-1](#) was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

[图 9-1](#) shows the TPS562207S 4.3-V to 17-V input, 1.05-V output converter schematics.

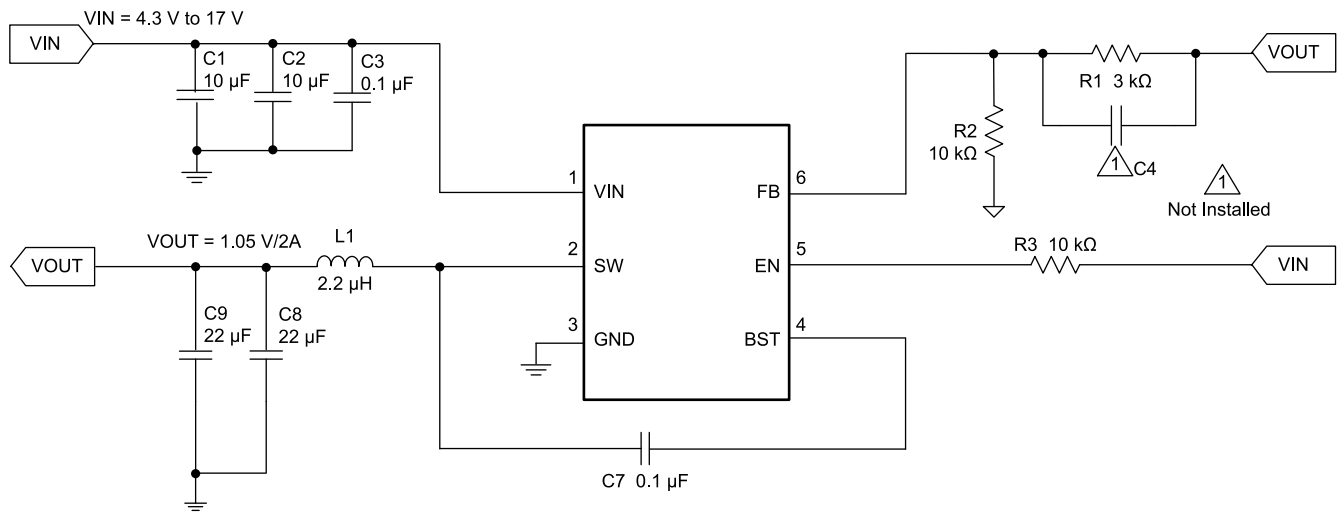


图 9-1. 1.05-V/2-A Reference Design

9.2.1 Design Requirements

表 9-1 shows the design parameters for this application.

表 9-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.3 to 17 V
Output voltage	1.05 V
Transient response, load step: 10% ~ 90% of full loading	$\Delta V_{out} = \pm 5\%$
Input ripple voltage	200 mV
Output ripple voltage	20 mV
Output current rating	2 A
Operating frequency	580 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 方程式 1 to calculate V_{OUT} .

To improve efficiency at very light loads, consider using larger value resistors. Too high of resistance will be more susceptible to noise and voltage errors from the FB input current will be more noticeable.

$$V_{out} = 0.804 \times (1 + R_{FBT}/R_{FBB}) \quad (1)$$

9.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_p = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (2)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 方程式 2 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 9-2.

表 9-2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (k Ω)	R2 (k Ω)	TYP L1 (μ H)	C8 + C9 (μ F)			CFF (pF)
				MIN	TYP	MAX	
0.85	0.55	10.0	2.2	20	44	110	-
0.9	1.2	10.0	2.2	20	44	110	-
1	2.4	10.0	2.2	20	44	110	-
1.05	3.0	10.0	2.2	20	44	110	-
1.2	4.9	10.0	2.2	20	44	110	-
1.5	8.6	10.0	2.2	20	44	110	-
1.8	12.3	10.0	2.2	20	44	110	-
2.5	21.0	10.0	3.3	20	44	110	-
3.3	31.0	10.0	3.3	20	44	110	10-220
5	52.0	10.0	4.7	20	44	110	10-220

表 9-2. Recommended Component Values (continued)

OUTPUT VOLTAGE (V)	R1 (k Ω)	R2 (k Ω)	TYP L1 (μ H)	C8 + C9 (μ F)			CFF (pF)
				MIN	TYP	MAX	
6.5	70.5	10.0	4.7	20	44	110	10-220

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using 方程式 3, 方程式 4, and 方程式 5. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (3)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (4)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (5)$$

For this design example, the calculated peak current is 2.35 A and the calculated RMS current is 2.01 A. The inductor used is a WE 74437349022.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS562207S is intended for use with ceramic or other low-ESR capacitors. Recommended values range from 20 μ F to 110 μ F. Use 方程式 6 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (6)$$

For this design two MuRata GRM21BR61A226ME44L 22- μ F output capacitors are used. The typical ESR is 2 m Ω each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

9.2.2.3 Input Capacitor Selection

The TPS562207S requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 μ F for the decoupling capacitor. An additional 0.1- μ F capacitor (C3) from pin 1 to ground is necessary to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

9.2.2.4 Bootstrap Capacitor Selection

A typical 0.1- μ F ceramic capacitor must be connected between the BST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

9.2.3 Application Curves

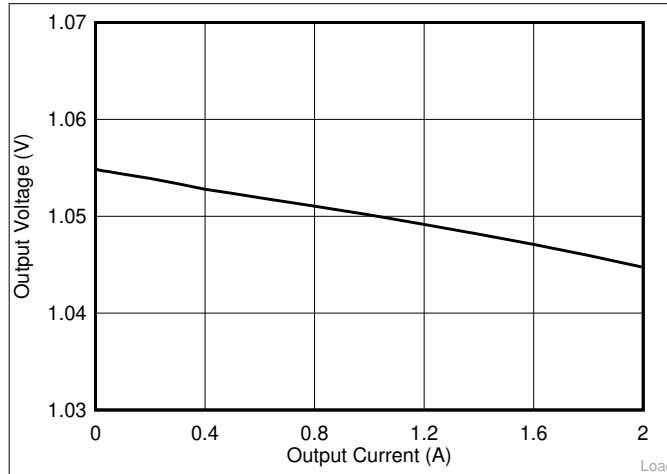


图 9-2. Load Regulation with Different Loading

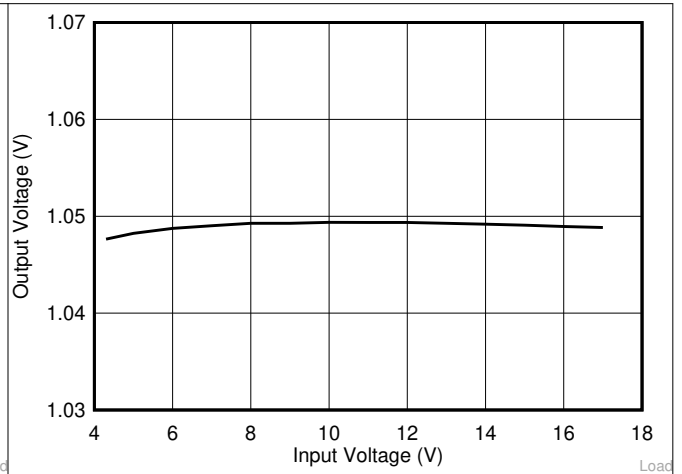


图 9-3. Load Regulation with Different Input Voltage

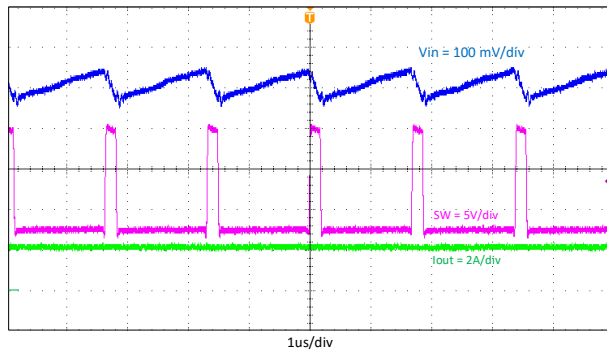


图 9-4. Input Voltage Ripple

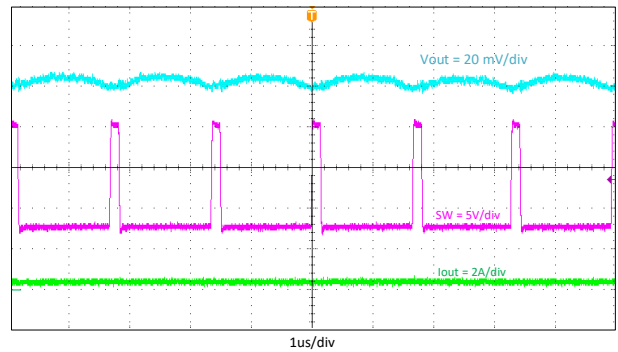


图 9-5. Output Voltage Ripple, $I_{out} = 0.2 A$

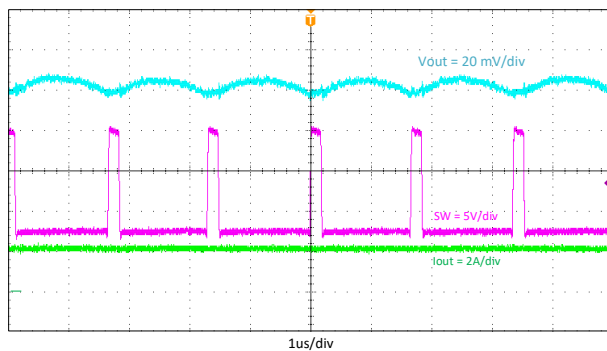


图 9-6. Output Voltage Ripple, $I_{out} = 2 A$

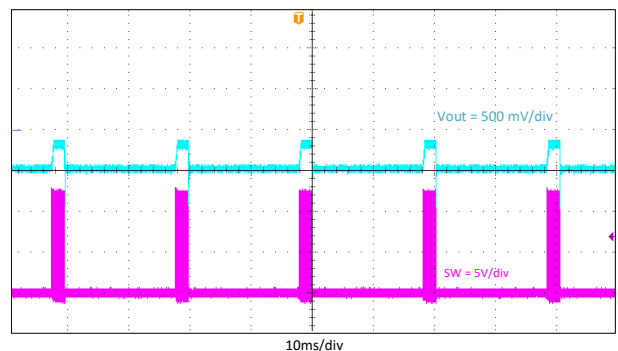


图 9-7. Hiccup, $I_{out} = 5 A$

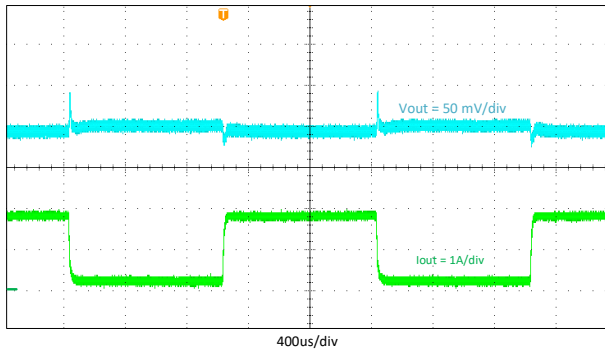


图 9-8. Transient Response, 0.2 to 1.8 A

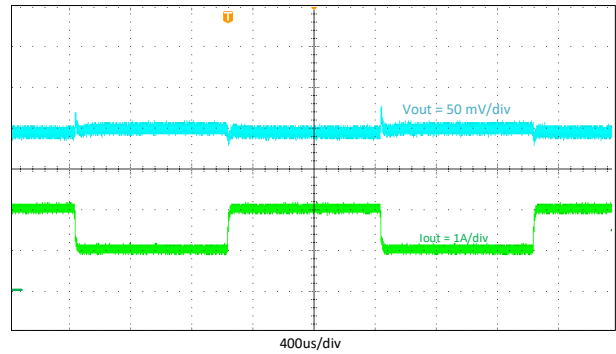


图 9-9. Transient Response, 1 to 2 A

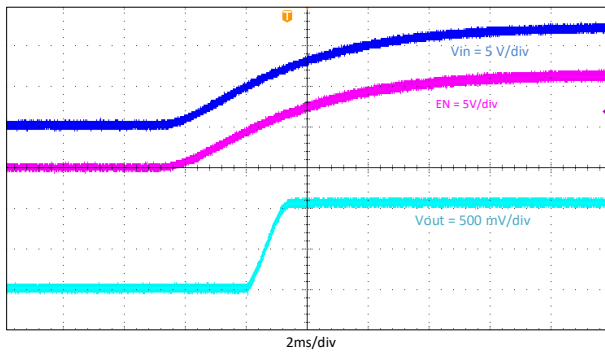


图 9-10. Start-Up Relative to VIN

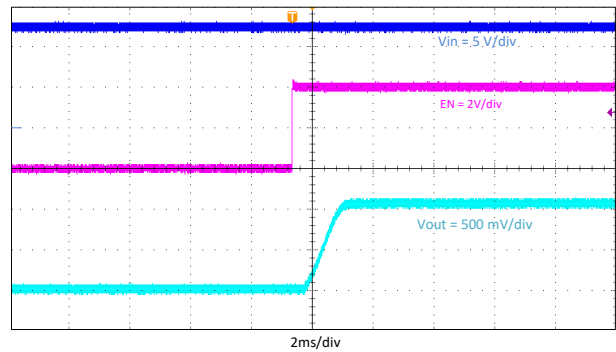


图 9-11. Start-Up Relative to EN

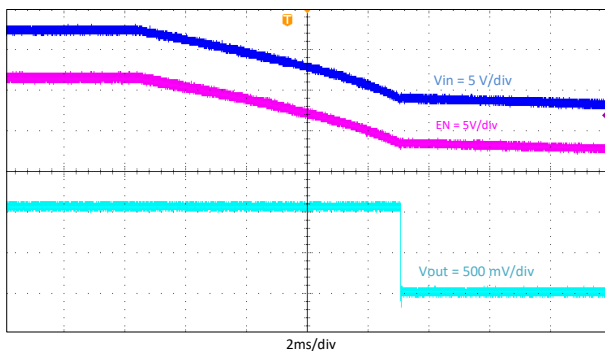


图 9-12. Shutdown Relative to VIN

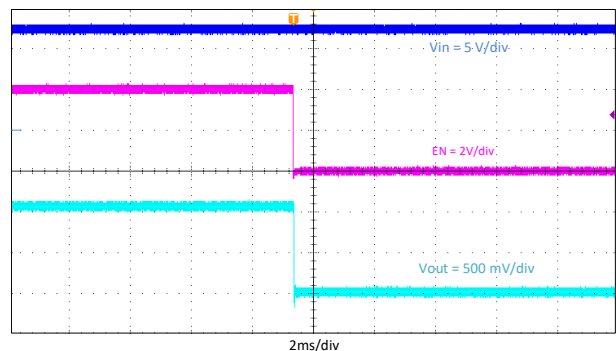


图 9-13. Shutdown Relative to EN

10 Power Supply Recommendations

The TPS562207S is designed to operate from input supply voltage in the range of 4.3 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is $V_O / 0.75$.

11 Layout

11.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the FB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

11.2 Layout Example

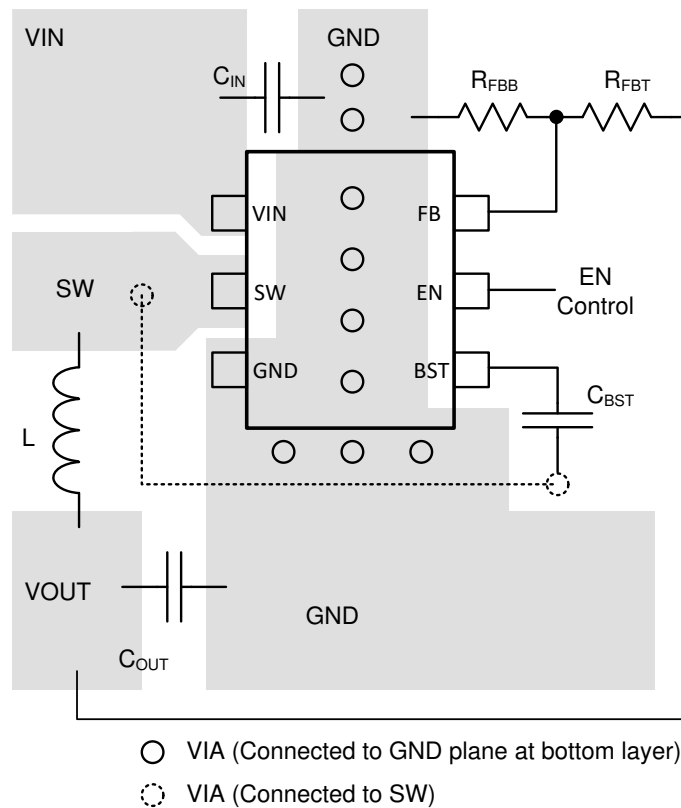


图 11-1. TPS562207S Layout

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.3 Trademarks

D-CAP2™ and TI E2E™ are trademarks of Texas Instruments.

所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS562207SDRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI SN	Level-1-260C-UNLIM	-40 to 125	S207	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

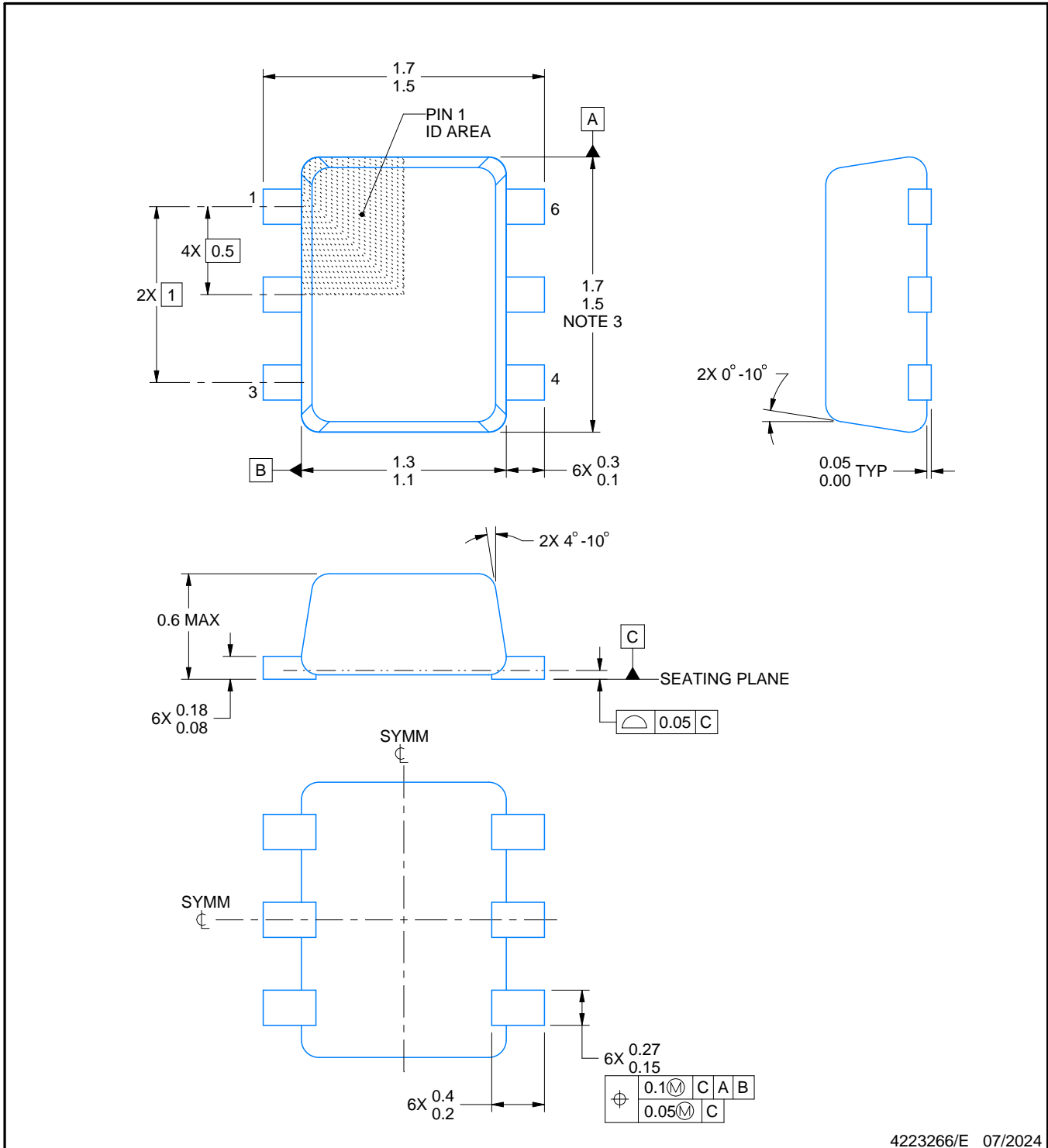
DRL0006A



PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/E 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



4223266/E 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/E 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024，德州仪器 (TI) 公司