

TPS536C9 具有 PMBus 和 VR14 SVID 接口的双 channel($N + M \leq 12$ 相)D-CAP+™、降压多相控制器

1 特性

- 输入电压范围：4.5V 至 17V
- 输出电压范围：0.25V 至 5.5V
- 支持 N+M 相位配置 ($N+M \leq 12$, $M \leq 6$) 的双路输出
- 符合 Intel® VR14 SVID 标准且支持 PSYS
- 向后兼容 VR13.HC/VR13.0 SVID
- 自动 NVM 故障状态记录
- 动态电流限制，可提高快速电压模式性能
- 与 TI NexFET™ 功率级完全兼容，可实现高密度解决方案
- 增强型 D-CAP+ 控制可提供卓越的瞬态性能和出色的动态电流共享
- 可通过可编程阈值实现动态切相，从而提高轻负载和重负载下的效率
- 可通过非易失性存储器 (NVM) 进行配置，从而减少外部组件数量
- 支持精确可调自适应电压定位 (AVP、负载线)
- 单独的每相位 IMON 校准，具有多斜率增益校准以提高系统精度。
- 快速增相可实现瞬态下冲衰减
- 具有可编程超时的二极管制动，可减少瞬态过冲
- 获得专利的 AutoBalance™ 电流共享
- 可编程的每相位谷值电流限制 (OCL)
- PMBus™ v1.3.1 系统接口，用于遥测电压、电流、功率、温度和故障条件
- 可通过 PMBus 对环路补偿进行编程
- 无驱动器配置，有助于实现高效的高频开关
- 6 mm × 6 mm 48 引脚 QFN 封装

2 应用

- [数据中心和企业计算机机架式服务器](#)
- [硬件加速器](#)
- [网络接口卡 \(NIC\)](#)
- ASIC 和 [高性能客户端](#)

3 说明

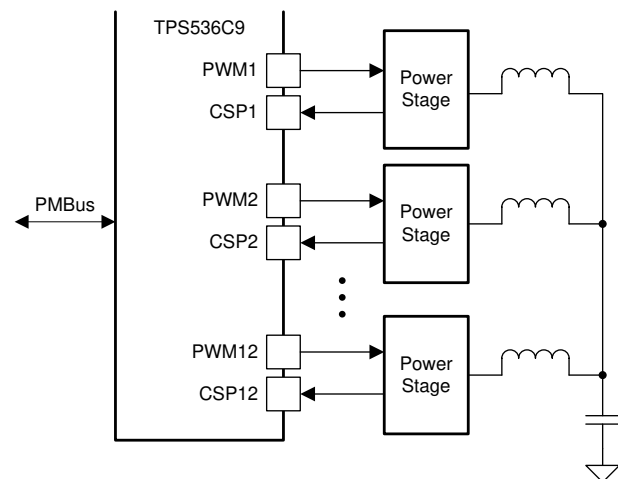
TPS536C9 是一款符合 VR14 SVID 标准的降压控制器，具有双通道、内置非易失性存储器 (NVM) 和 PMBus™ 接口，而且与 TI NexFET™ 功率级完全兼容。D-CAP+ 架构等高级控制特性以及下冲衰减 (USR) 和过冲衰减 (OSR) 可提供快速瞬态响应、最低输出波纹和出色的动态电流共享。该器件还提供全新的相位交错策略和动态切相功能，可有效提升轻负载条件下的效率。还本地支持输出电压转换率和自适应电压定位的可调控制。此外，该器件还支持 PMBus 通信接口，可向主机系统报告遥测的电压、电流、功率、温度和故障状况。所有可编程参数均可通过 PMBus 接口进行配置，而且可作为新的默认值存储在 NVM 中，以尽可能减少外部组件数量。

TPS536C9 器件采用散热增强型 48 引脚 QFN 封装，额定工作温度为 -40°C 至 125°C 。

器件信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
TPS536C9	QFN (48)	6.00 × 6.00 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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简化版应用



4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (June 2021) to Revision A (December 2021)	Page
• 将文档状态从 预告信息 更改为 量产数据	1

5 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

5.1 Getting Started and Next Steps

5.2 Device Support

5.2.1 第三方产品免责声明

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5.3 Device Nomenclature

5.4 Tools and Software

5.5 Documentation Support

5.5.1 Related Documentation

5.6 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

5.7 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

5.10 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS536C9RSLR	Active	Production	VQFN (RSL) 48	3000 LARGE T&R	Yes	Call TI Nipdauag	Level-3-260C-168 HR	-40 to 125	TPS 536C9
TPS536C9RSLR.A	Active	Production	VQFN (RSL) 48	3000 LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	TPS 536C9

- (1) **Status:** For more details on status, see our [product life cycle](#).
- (2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
- (3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.
- (4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
- (5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
- (6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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GENERIC PACKAGE VIEW

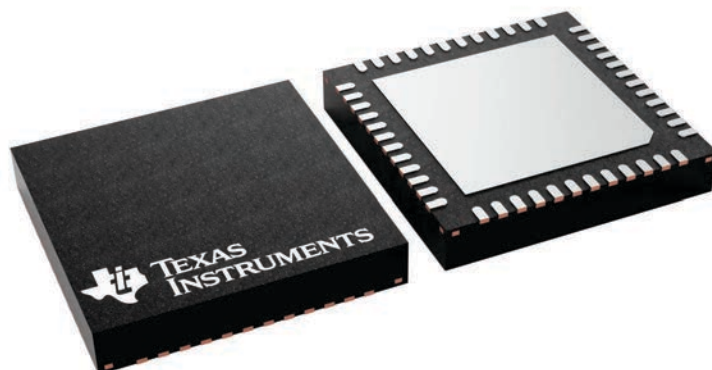
RSL 48

VQFN - 1 mm max height

6 x 6, 0.4 mm pitch

QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



VQFN - 1 mm max height

Top View Dimensions:

- Overall Width: 6.1 mm (5.9 mm typical)
- Overall Height: 6.1 mm (5.9 mm typical)
- Pin Pitch: 0.4 mm
- Pin 1 ID (45° X 0.3)
- Exposed Thermal Pad: 4.2 ± 0.1 mm

Side View Dimensions:

- Maximum Height: 1.0 mm (0.8 mm typical)
- Seating Plane

Table of Tolerances:

0.1 (M)	C	A	B
0.05 (M)	C		

Notes:

- SYMM: Symmetrical
- 48X 0.5 0.3: 48 pins, 0.5 mm width, 0.3 mm height
- 48X 0.25 0.15: 48 pins, 0.25 mm width, 0.15 mm height
- (0.2) TYP: Typical value of 0.2 mm

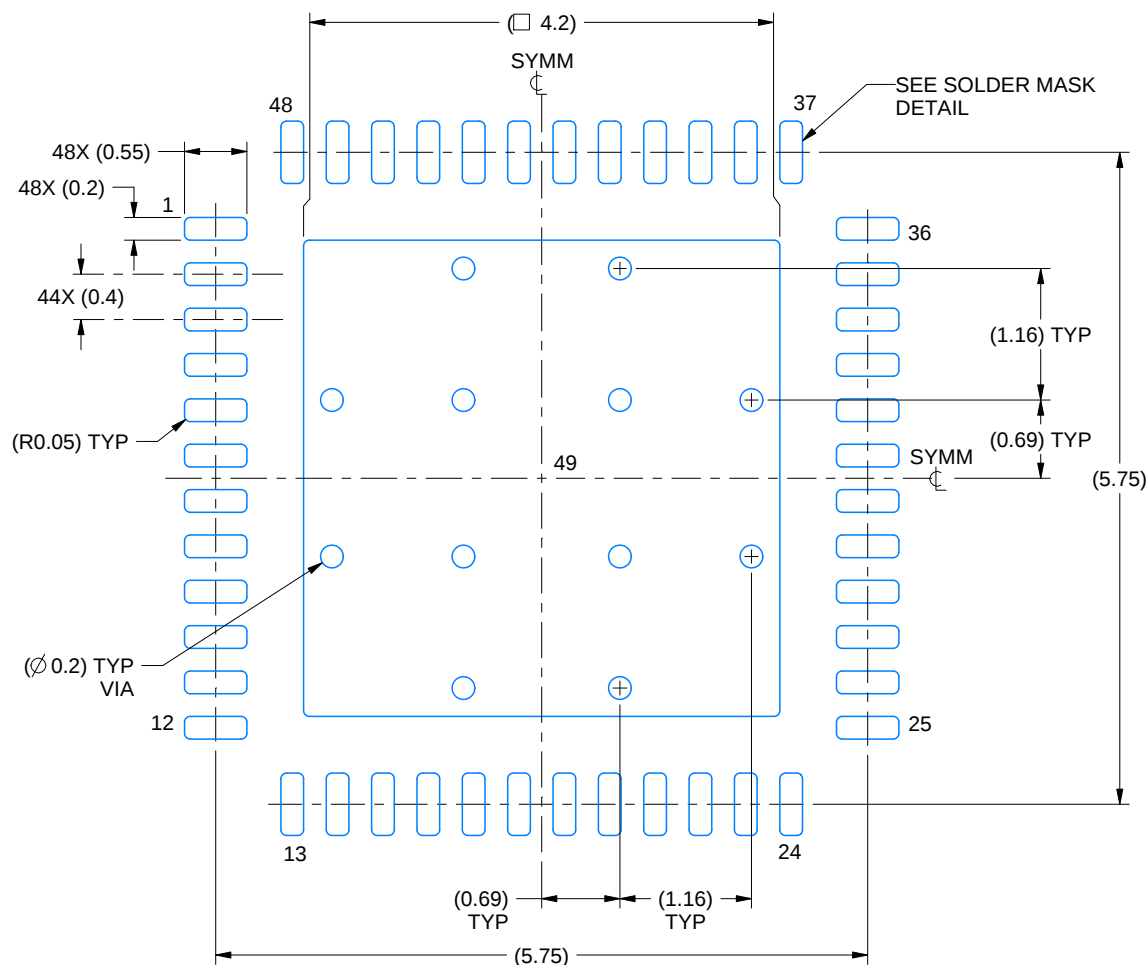
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

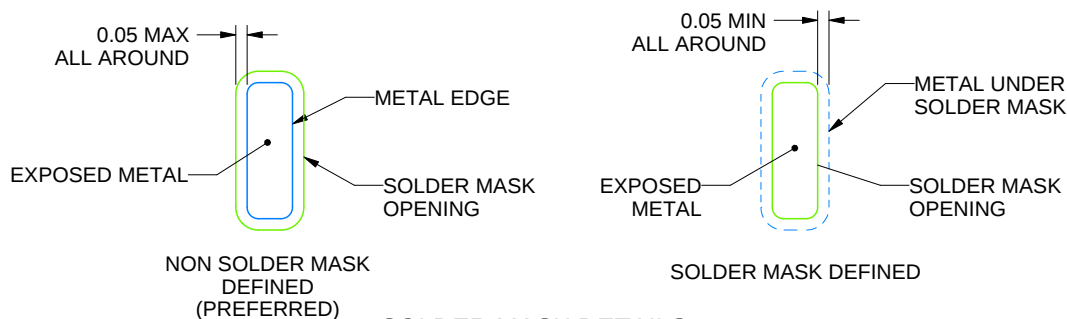
RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4231403/A 12/2024

NOTES: (continued)

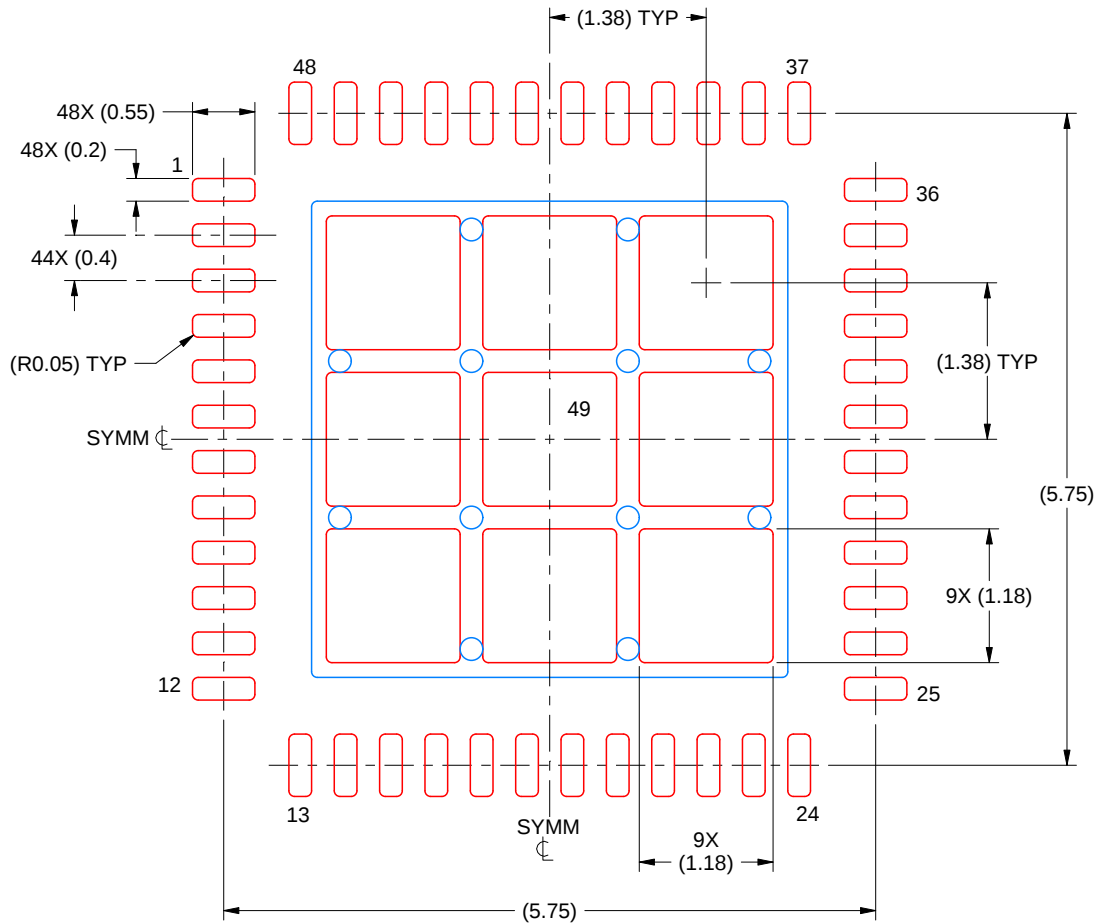
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSL0048G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 49
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4231403/A 12/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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