具有超低静态 (ULQ™) 的22V 输入，10A 集成场效应晶体管(FET) 转换器

查询样品: TPS51362

特性

- 输入电压范围：**3V** 至 **22V**
- 输出电压范围：**0.6V** 至 **2V**
- **10A** 集成 **FET** 转换器
- 最少的外部组件数量
- **ULQ™-100** 模式运行以实现系统待机期间的长电池使用寿命
- 软启动时间可由外部电容器设定
- 开关频率：**800kHz**
- **D-CAP2™** 架构以实现高分子有机半导体固体电容器 **(POSCAP)** 和所有多层陶瓷电容 **(MLCC)** 输出电容器的使用
- 用于精确过流限制 **(OCL)** 保护的集成且支持温度补偿的低侧导通电阻感测
- 电源良好输出
  OCL，过压保护 **(OVP)**，欠压保护 **(UVP)** 和欠压闭锁 **(UVLO)** 保护
- 热关断（非锁存）
- 输出放电功能
- 集成升压金属氧化物半导体场效应晶体管 **(MOSFET)** 开关
- 焊球间距 **0.4mm**，高度 **1mm** 的 **28** 引脚，**3.5mm x 4.5mm**，**RVE**，四方扁平无引线 **(QFN)** 封装

应用范围

- 笔记本电脑 **(VCCIO)**
- 内存轨道 **(DDR VDDQ)**

说明

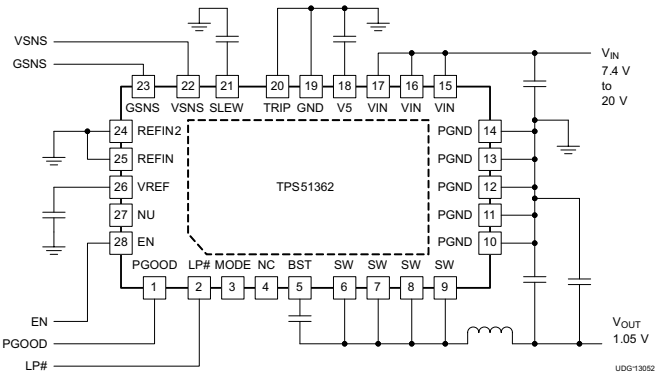
TPS51362 是一款高压输入、同步转换器，此转换器带有集成的 FET，它基于 DCAP-2™ 控制拓扑结构，从而实现快速瞬态响应并支持 POSCAP 和所有 MLCC 输出电容器。 与 TI 领先的封装技术组合在一起，TI 专有的 FET 技术为诸如 VCCIO 和 VDDQ 等用于 DDR 笔记本内存的单输出电源轨或者广泛应用中的任何负载点 (POL) 提供最高密度的解决方案。

TPS51362 的主要特性是其 ULQ™-100 模式以实现低偏置电流（低功率模式下为 100μA，由 LP# 启用）。 这个特性对于延长系统待机模式中的电池使用寿命非常有帮助。

此特性集包括 800kHz 的开关频率。 可由一个外部电容器设定的软启动时间。自动跳跃、预偏置启动、集成引导加载开关、电源良好、使能和一整套的故障保护机制，其中包括 OCL，UVP，OVP 5V UVLO 和热关断。

它采用 3.5mm x 4.5mm，焊球间距 0.4mm，28 引脚 QFN (RVE) 封装，额定运行温度范围为 -10°C 至 85°C。

简化的应用



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ULQ, DCAP-2 are trademarks of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1) (2)

T_A	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	TRANSPORT MEDIA	MINIMUM ORDER QUANTITY
–10°C to 85°C	Plastic Quad Flat Pack (QFN)	TPS51362RVET	28	Small tape-and-reel	250
		TPS51362RVER		Large tape-and-reel	3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
Input voltage range(2)	VIN		–0.3	30	V
	BST			36	
		transient <10 ns		38	
		w/r/t SW		6	
	SW			30	
	EN, TRIP, NU, MODE, V5, LP#		-0.3	6	
	SLEW, VSNS, REFIN, REFIN2		–0.3	3.6	
	GSNS		–0.35	0.35	
	PGND		-0.3	0.3	
Output voltage range(2)	PGOOD		–0.3	6	V
	VREF		–0.3	3.6	
	NC		–5	36	
Electrostatic discharge	Human body model (HBM) QSS 009-105 (JESD22-A114A)			2000	V
	Charged device model (CDM) QSS 009-147 (JESD22-C101B.01)			500	
Junction temperature range, T_J			–10	150	°C
Storage temperature range, T_{stg}			–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal unless otherwise noted.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS51362 QFN (RVE) (28 PINS)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	40.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	22.8	
θ_{JB}	Junction-to-board thermal resistance	20.1	
ψ_{JT}	Junction-to-top characterization parameter	1.6	
ψ_{JB}	Junction-to-board characterization parameter	19.4	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supplu voltage range	VIN	3	22	V
	V5	4.6	5.5	
Input voltage range	BST	–0.1	33.5	
	SW	–3	27	
	EN, TRIP, NU, MODE, LP#	–0.1	5.5	
	SLEW, VSNS, REFIN, REFIN2	–0.1	3.5	
	GSNS	–0.1	0.3	
	PGND	–0.1	0.1	
Output voltage range	PGOOD	–0.1	5.5	
	VREF, SLEW	–0.1	3.5	
Operating free-air temperature, T_A		–10	85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{IN} = 12 V, V_{V5} = 5 V, MODE = GND, V_{EN} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{V5}	V5 supply current	T_A=25°C, No load, V_{EN} = 5 V, LP # = 0 V		100		µA
		T_A=25°C, No load, V_{EN} = 5 V		560		
I_{V5SDN}	V5 shutdown current	T_A=25°C, No load, V_{EN} = 0 V		1		µA
VREF OUTPUT						
V_{VREF}	Reference voltage	I_{VREF} = 30 µA, w.r.t. GSNS		2		V
		0 µA ≤ I_{VREF} ≤ 300 µA, -10°C ≤ T_A ≤ 85°C	-1%		1%	
$I_{VREF(OCL)}$	Current limit	(V_{VREF}–V_{GSNS}) = 1.7 V	0.4	1		mA
VOLTAGE AMPLIFIER						
I_{VSNS}	VSNS input current	V_{VSNS} = 1 V	-1		1	µA
$I_{VSNS(DIS)}$	VSNS discharge current	V_{EN} = 0 V, V_{VSNS} = 0.5 V		12		mA
SMPS FREQUENCY						
$t_{OFF(min)}$	Minimum off-time			320		ns
t_{DEAD1}	Deadtime1 (1)	SW rising to falling		10		ns
t_{DEAD2}	Deadtime2 (1)	SW falling to rising		10		ns
INTERNAL BOOT STRAP SW						
V_{FBST}	Forward foltage	V_{V5} - B_{ST}, T_A = 25°C, I_F = 10 mA		0.1	0.2	V
I_{BST}	BST leakage current	T_A = 25°C, V_{BST} = 14 V, V_{SW} = 7 V		0.01	1.5	µA
MOSFET ON-RESISTANCE						
$R_{DS(on)H}$	High-side on-resistance	T_A = 25°C, V_{V5} = 5 V			17.5	mΩ
$R_{DS(on)L}$	Low-side on-resistance	T_A = 25°C, V_{V5} = 5 V			8.75	mΩ
LOGIC THRESHOLD						
$V_{MODE(TH)}$	MODE threshold voltage	MODE = Float		2.5		V
V_{LL}	EN low-level voltage				0.35	V
V_{LH}	EN high-level voltage		0.9			V
$V_{L(HYST)}$	EN hysteresis voltage			0.25		V
$V_{L(LK)}$	EN input leakage current		-1	0	1	µA
V_{LL}	LP# low-level voltage				0.35	V
V_{LH}	LP# high-level voltage		0.85			V
$V_{L(HYST)}$	LP# hysteresis voltage			0.4		V
$V_{L(LK)}$	LP# input leakage current		-1	0	1	µA
SOFT-START						
I_{SS}	Soft-Start current	Soft-start current source		10		µA
PGOOD COMPARATOR						
V_{PGTH}	PGOOD threshold	PGOOD in from lower (startup)		92%		
I_{PG}	PGOOD sink current	V_{PGOOD} = 0.5V		6		mA
$t_{PG(CMPSS)}$	PGOOD start-up delay	PGOOD comparator startup delay		1.5		ms
$I_{PG(LK)}$	PGOOD leakage current		-1	0	1	µA

(1) Ensured by design.

ELECTRICAL CHARACTERISTICS (continued)

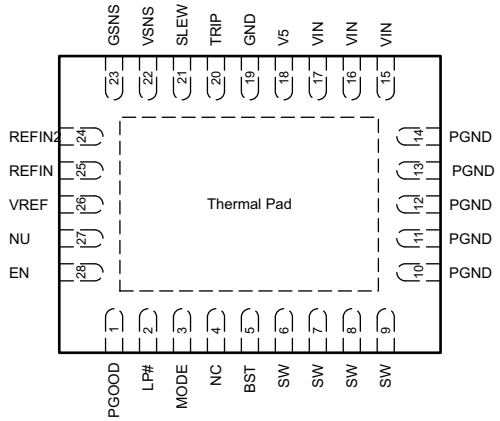
over operating free-air temperature range, V_{IN} = 12 V, V_{V5} = 5 V, MODE = GND, V_{EN} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OVERCURRENT LIMIT LEVEL						
I_{OCL}	Current limit threshold	V_{TRIP} = 0 V, valley current set point, T_A=25°C	7	8	9	A
		V_{TRIP} = 5 V, valley current set point, T_A=25°C	10.5	12	13.5	
V_{ZC} (2)	Zero cross detection offset			0		mV
PROTECTIONS						
V_{POR}	V5 POR threshold voltage (2)	Reset OVP fault		1.7		V
V_{PORHYS}	V5 POR threshold voltage hysteresis (2)	Reset OVP fault hysteresis		85		mV
V_{UVLO}	V5 UVLO threshold voltage	Wake-up	4.3	4.4	4.6	V
		Shutdown	3.8	4	4.2	
V_{OVP}	OVP threshold voltage	OVP detect voltage	118%	120%	123%	
t_{OVPDLY}	OVP propagation delay	With 100 mV overdrive		430		ns
V_{OOB}	OOB threshold voltage		105.5%		109.5%	
V_{UVP}	UVP threshold voltage	UVP detect voltage	63%	66%	69%	
t_{UVPDLY}	UVP delay			1		ms
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (2)	Shutdown temperature		140		°C
		Hysteresis		10		

(2) Ensured by design.

DEVICE INFORMATION

RVE PACKAGE
28 PINS
(TOP VIEW)

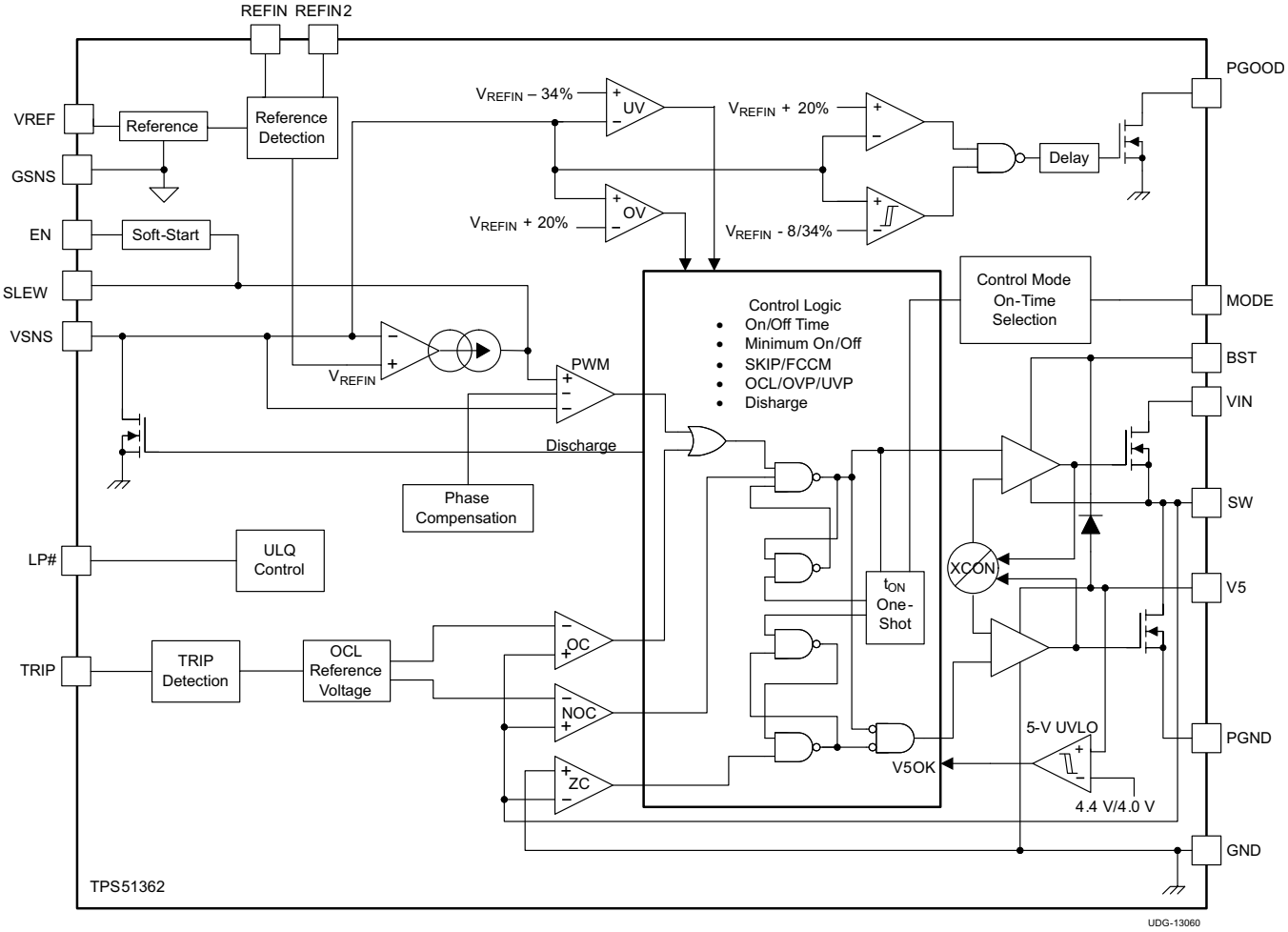


PIN FUNCTIONS

NAME	NO.	I/O/P (1)	DESCRIPTION
BST	5	I	Power supply for internal high side MOSFET. Connect a 0.1-µF bootstrap capacitor between this pin and SW pin.
EN	28	I	Enable signal, 1.05-V logic compatible.
GND	19	—	General device ground.
GSNS	23	O	GND sense input. Connect GSNS to general/system ground or GND sensing point at the output return.
LP#	2	I	Low power signal (active low) to indicate the converter entering ULQ™ mode. 1.05-V logic compatible.
MODE	3	I	Frequency (800 kHz) programmable input (see Table 2).
NC	4	—	Not connected.
NU	27	—	Not used for external applications.
PGND	10	—	Power ground. Connect to the system ground.
	11		
	12		
	13		
	14		
PGOOD	1	O	PGOOD output. Connect a pull-up resistor with a value of 100 kΩ to this pin.
Power PAD	29	—	Connect to system ground by multiple vias.
REFIN	25	I	Target output voltage input pin. 0.6 V to 2 V, 1.05 V/1.2 V built-in (GND and Open) (see Table 1).
REFIN2	24	I	Tie to GND or float. This input is used to determine the fixed voltage setpoint (see Table 1).
SLEW	21	O	Connect a capacitor between this pin and GND for soft start and integrator functions.
SW	6	O	Switching node output. Connect external inductor.
	7		
	8		
	9		
TRIP	20	I	OCL programmable input (see Table 3).
V5	18	I	5-V power supply for analog circuits and gate driver.
VIN	15	I	Power supply input pin. Apply 3-V to 22-V of supply voltage.
	16	I	
	17	I	
VREF	26	O	2-V reference output. Connect a 0.1-µF ceramic capacitor between this pin and the GNDS pin.
VSNS	22	I	Output voltage sense input.

(1) I = Input, O = Output, P = Power, G = Ground

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

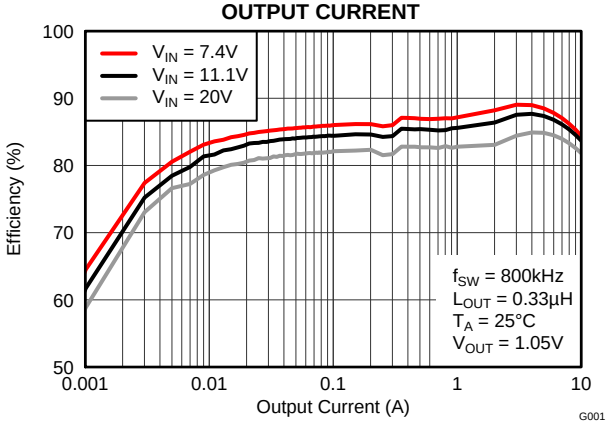


Figure 1.

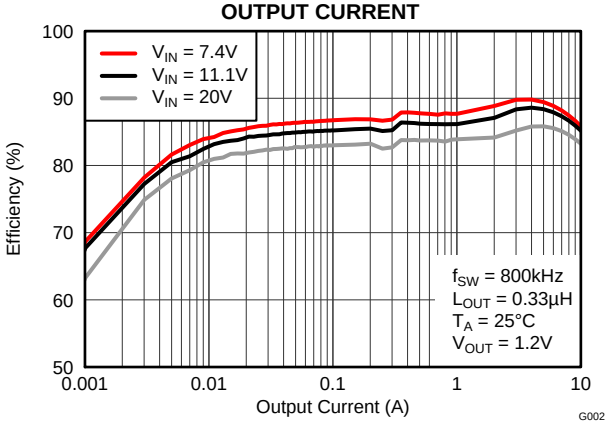


Figure 2.

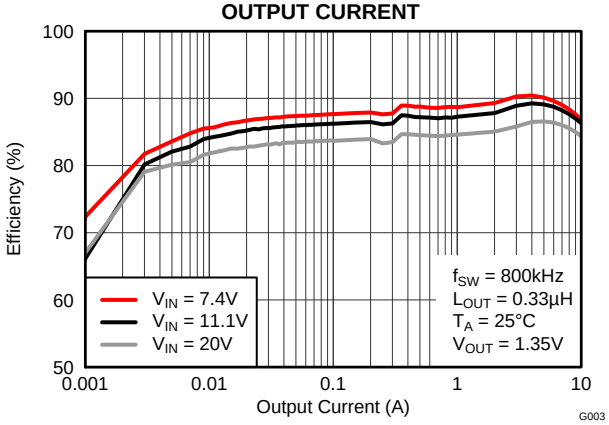


Figure 3.

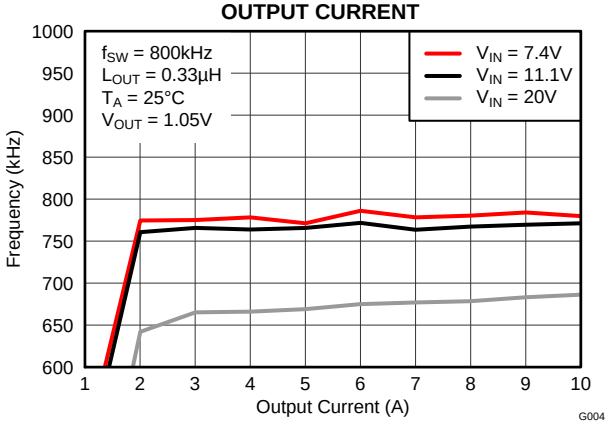


Figure 4.

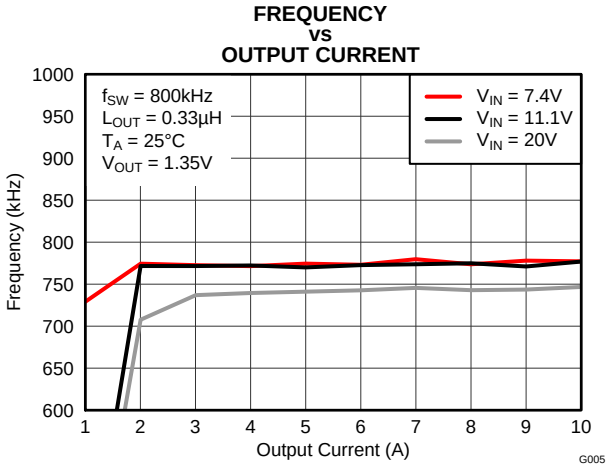


Figure 5.

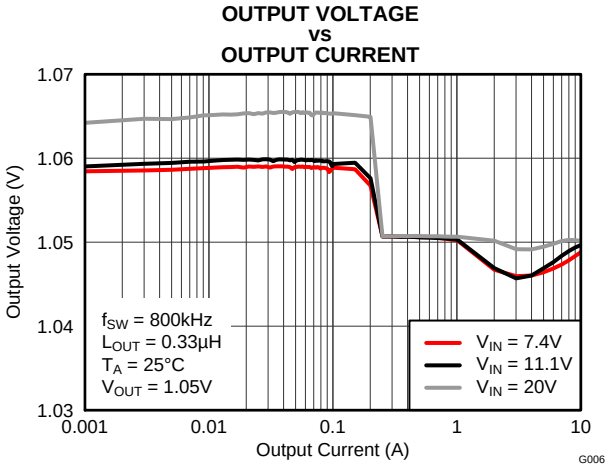


Figure 6.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE vs OUTPUT CURRENT

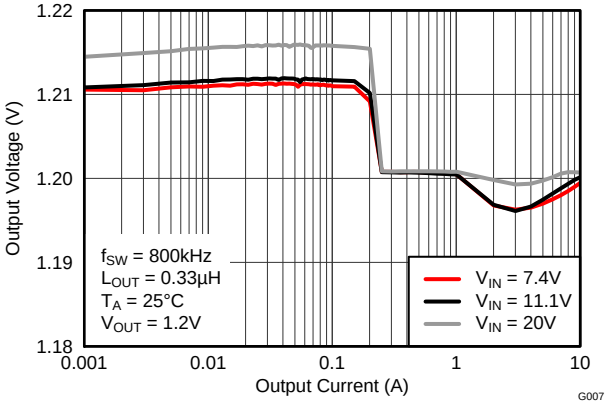


Figure 7.

GAIN and PHASE vs FREQUENCY

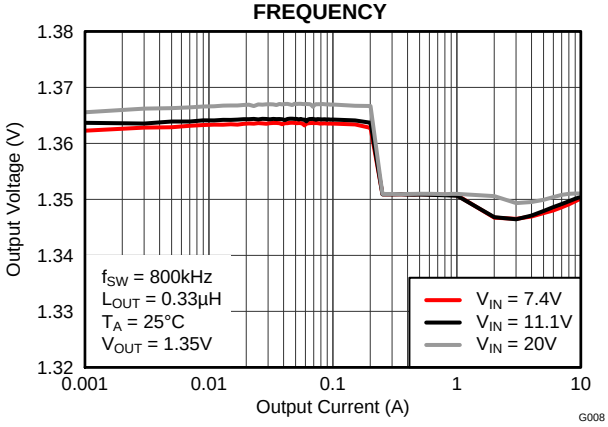


Figure 8.

GAIN and PHASE vs FREQUENCY

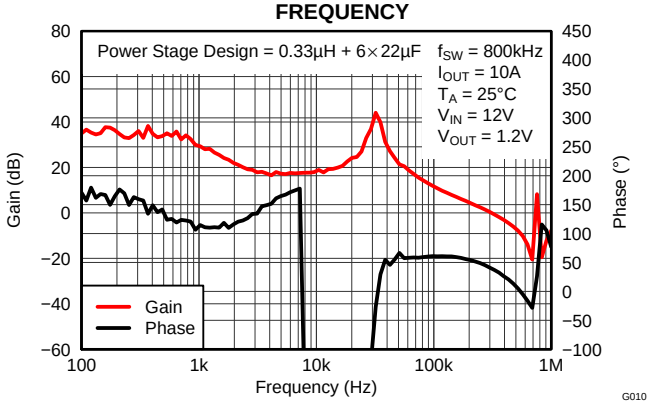


Figure 9.

GAIN and PHASE vs FREQUENCY

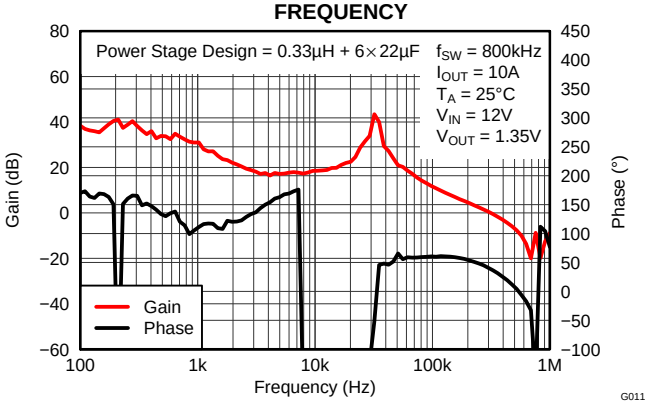


Figure 10.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT (I_{OUT} = 0.1A)

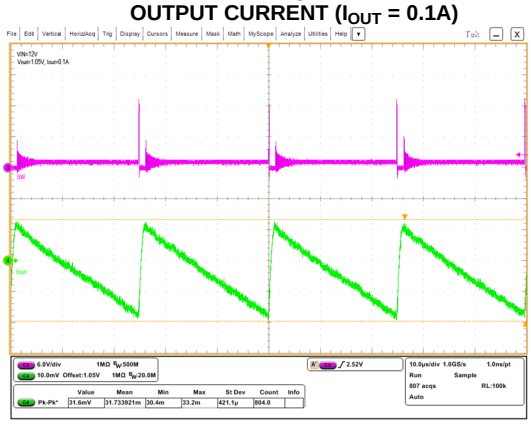


Figure 11.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT (I_{OUT} = 1A)

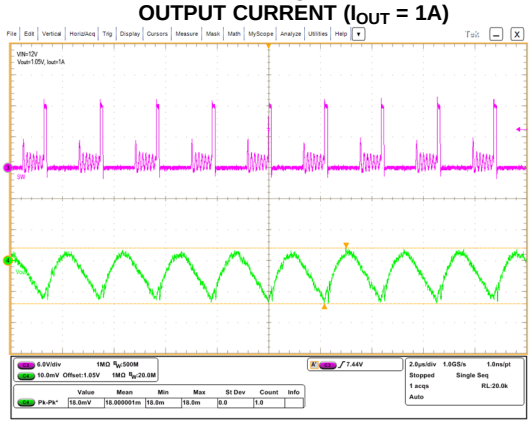


Figure 12.

TYPICAL CHARACTERISTICS (continued)

OUTPUT VOLTAGE RIPPLE VS OUTPUT CURRENT (I_{OUT} = 10A)

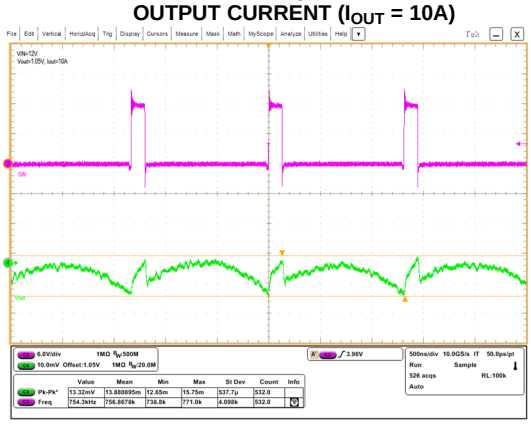


Figure 13.

LOAD TRANSIENT RESPONSE

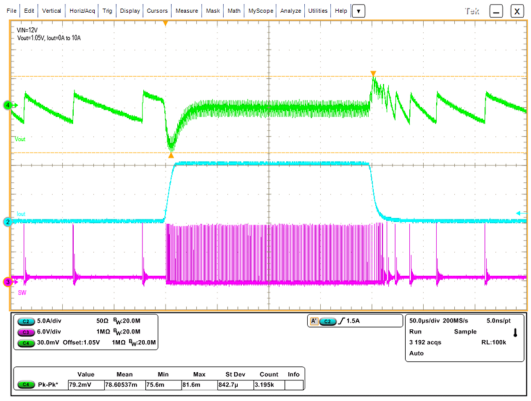


Figure 14.

START-UP

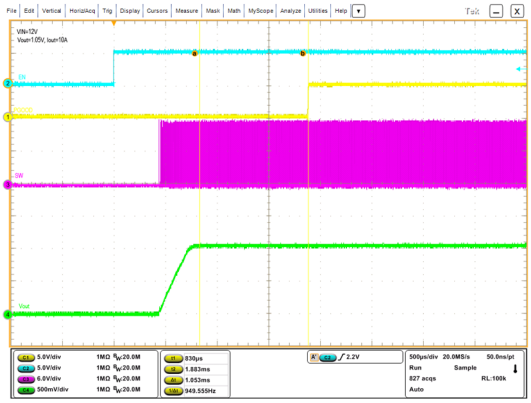


Figure 15.

SHUTDOWN

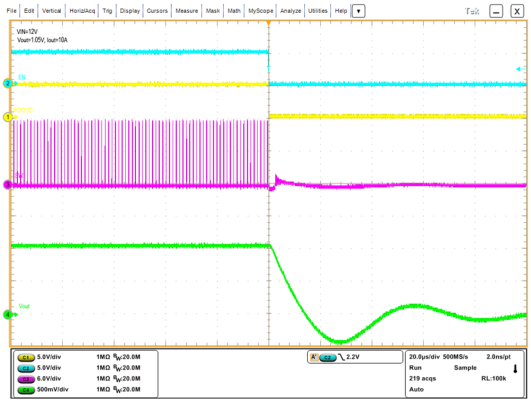


Figure 16.

LP TOGGLE

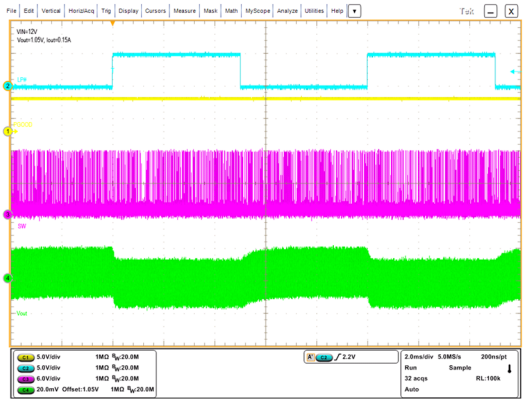


Figure 17.

AMBIENT TEMPERATURE VS OUTPUT CURRENT

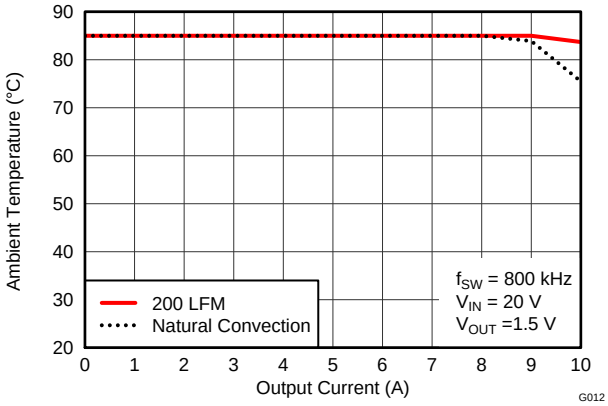


Figure 18.

APPLICATION INFORMATION

Functional Overview

The TPS51362 is a 10-A, integrated FET synchronous step-down converter with differential voltage feedback support.

It uses adaptive on-time D-CAP2 for compensation-less stable loop operation in POSCAP, POSCAP/MLCCs and all MLCCs output capacitor configurations.

TPS51362 automatically operates in discontinuous mode to optimize light-load efficiency. An 800-kHz switching frequency enables optimization of the power train for cost, size and efficiency performance of the design. The key feature of the TPS51362 is its ULQ™ mode to enable low-bias current (100 µA in low power mode, enabled by LP#). This feature is extremely beneficial for long battery life in system standby mode.

VREF, REFIN, REFIN2 and Output Voltage

This device provides a 2.0-V, accurate voltage reference from the VREF pin. This output has a 300-uA sourcing current capability to drive voltage setpoint reference through a voltage divider circuit as shown in Figure 19. To ensure higher overall system voltage accuracy, the sum of the total resistance from VREF to GND should be designed to be more than 67kohm. A MLCC capacitor with a value of 0.1uF or larger should be attached close to the VREF pin. The voltage setpoint range supported by this device is between 0.6 V and 2.0 V.

This device also supports resistor-less fixed voltage operation by the use of both REFIN and REFIN2 pins. Table 1 lists all the possible fixed voltage configurations by the REFIN and REFIN2 pin. The TPS51362 detects the state of both REFIN and REFIN2 during the initial startup and decides the output voltage setpoint for the operation.

Table 1. REFIN and REFIN2 Pin Settings

VOLTAGE (V)		V_{OUT} OUTPUT VOLTAGE (V)
REFIN PIN (V_{REFIN})	REFIN2 PIN (V_{REFIN2})	
GND	GND	1.05
Float	GND	1.2
GND	Float	1.5
Float	Float	1.35
Resistor dividers	Either GND or Float	Adjustable from 0.6 to 2.0

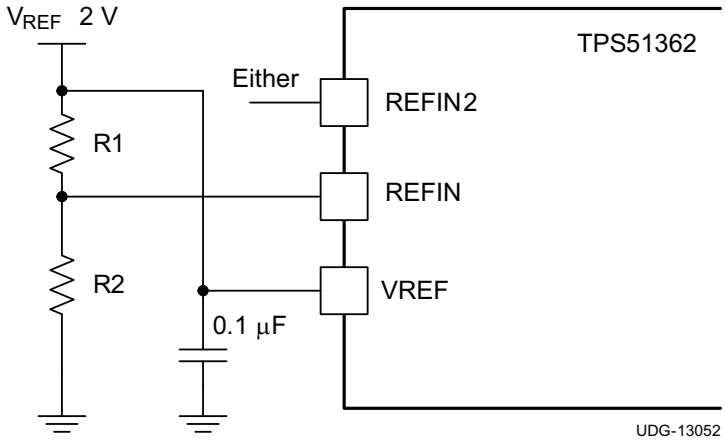


Figure 19. Setting the Output Voltage

PWM Operation

TPS51362 employs DCAP2 mode operation. It uses an internal phase compensation network (R_{C1}, R_{C2}, C_{C1}, C_{C2} and gain) to work with very low ESR output capacitors such as multi-layer ceramic capacitor (MLCC). The role of such network is to sense and scale the current ripple component of the output inductor current information and then use it in conjunction with the voltage feedback signal to achieve loop stability of the converter.

The transconductance (g_M) amplifier and SLEW capacitor (C1) forms an integrator. The output ripple voltage generated is inversed and averaged by this integrator. The AC information is superimposed onto otherwise DC information and forms a reference voltage at the input of the PWM comparator. As long as the integrator time constant is much larger than the inverse of the loop crossover frequency, the AC component is negligible.

$$\frac{gM}{(2\pi \times C1)} \leq \frac{f_0}{10} \quad (1)$$

where

- g_M is 60 µS
- f_0 is 1/3 or 1/4 of the switching frequency (f_{SW})

The voltage difference ($V_{SLEW} - V_{VSNS}$) is then compared to the G×(CSP-CSN) (see Figure 21) voltage at the PWM comparator inputs. The PWM comparator creates a SET signal to turn on the high-side MOSFET during each cycle when the current level falls below the loop demand (see Figure 20).

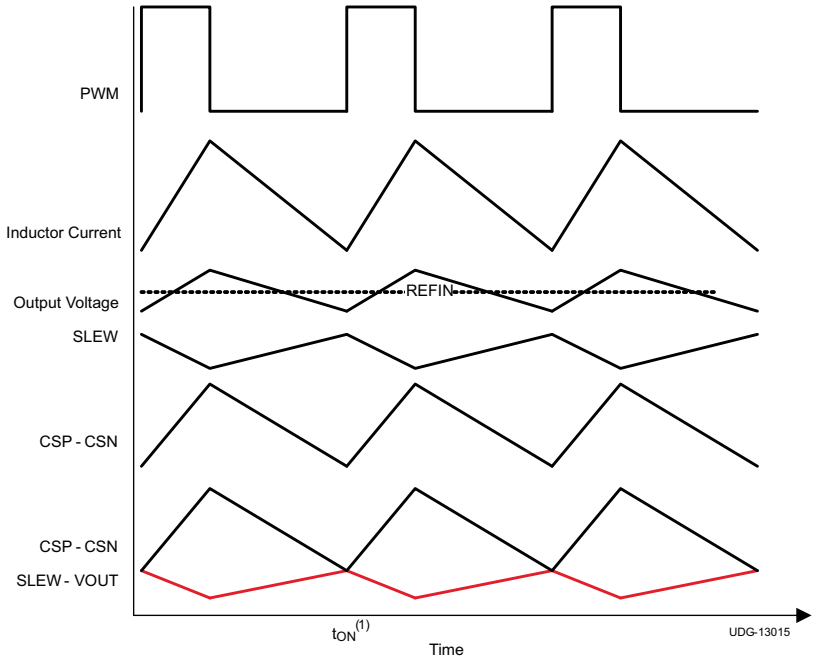


Figure 20. On-Time Waveforms (1)

(1) ON time is initiated by (VOUT-SLEW) and (CSP-CSN) crossover

The device operates at one distinct switching frequencies, 800 kHz. The switching frequency is configured by MODE pin for this converter operation (see Table 2). For stable operation of the buck converter, it is generally recommended to have a unity gain crossover (f_0) of 1/4 or 1/3 or the switching frequency. (see Table 2).

Table 2. Mode and Recommended Frequency Settings

MODE	FREQUENCY (kHz)		
	CROSSOVER (f_0)		SWITCHING (f_{SW})
	MIN	MAX	
FLOAT	200	267	800

Given the range of the recommended unity gain frequency, the power stage design is flexible, as long as the following equation is satisfied.

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}} \leq \frac{1}{10} \times f_0 \quad (2)$$

Operating in D-CAP2 mode, the overall loop response is dominated by the internal phase compensation network. The compensation network is designed to have two identical zeros at 8 kHz (800-kHz operation) in the frequency domain, which serves the purpose of splitting the LC double pole into one low frequency pole (same as the L-C double pole) and one high-frequency pole (greater than the unity gain crossover frequency).

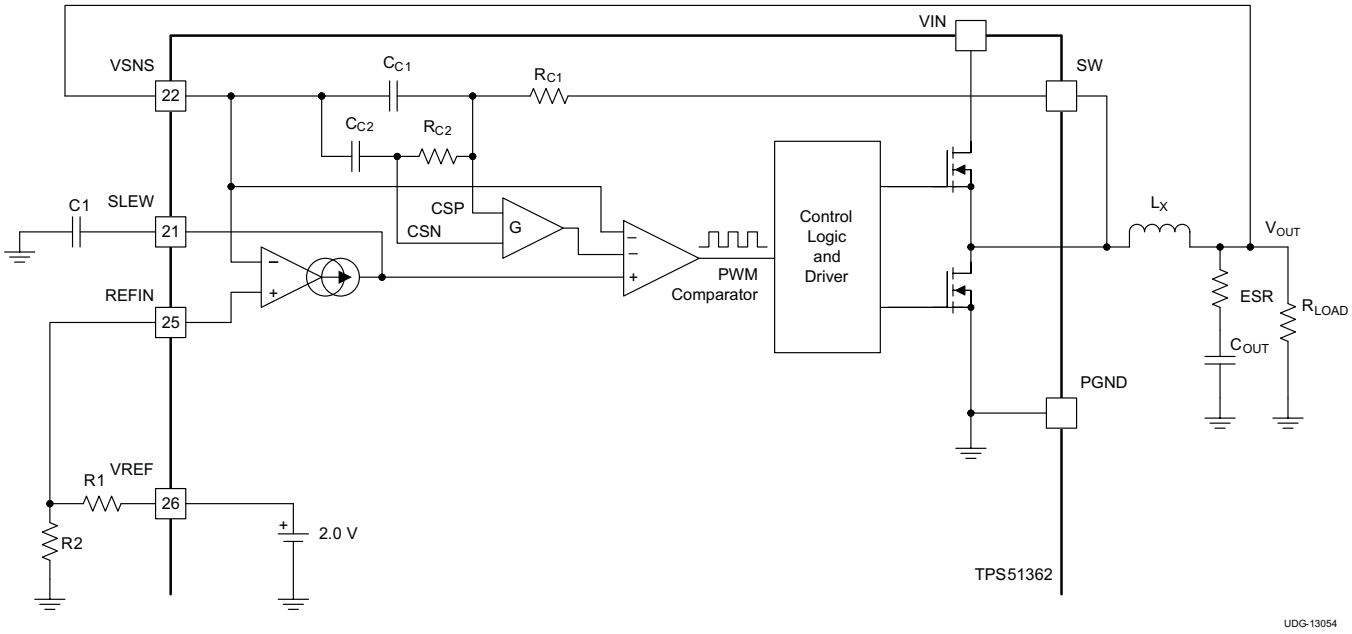


Figure 21. Simplified Architecture Illustrating DCAP2 Mode

Light-Load Operation

The mandatory light load operation for TPS51362 is referred to as auto skip. In auto-skip mode, the control logic automatically reduces its switching frequency to improve light load efficiency. To achieve this intelligence, a zero crossing detection comparator is used to prevent negative inductor current by turning off the low side FET when the SW crossing zero is detected. The equation below shows the boundary load condition of this skip mode and continuous conduction operation.

$$I_{LOAD(LL)} = \frac{(V_{IN} - V_{OUT})}{2 \times L_X} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}} \quad (3)$$

Power Sequences: Soft-Start and Power Good

Prior to asserting EN high, the power stage conversion voltage and V5IN voltage should be up and running. When EN is asserted high, TPS51362 provides soft start operation to suppress in-rush current during startup. The soft start action is achieved by an internal SLEW current of 10 µA (typ) sourcing into a small external MLCC capacitor connected from SLEW pin to GND.

Use Equation 4 to determine the soft-start timing.

$$t_{SS} = C_{SLEW} \times \frac{V_{OUT}}{I_{SLEW}} \quad (4)$$

where

- C_{SLEW} is the soft-start capacitance
- V_{OUT} is the output voltage
- I_{SLEW} is the internal, 10-µA current source

The TPS51362 includes a PGOOD open drain output. During the startup, once the output voltage is slewing up within –8% of the final setpoint target, the PGOOD becomes asserted after 1.5 ms of delay from the end of the soft-start period. During the operation, if the output voltage rises beyond 120% (typ) of the setpoint, the PGOOD pin becomes immediately de-asserted without hysteresis. Re-asserting the PGOOD pin requires either resetting either the V5IN pin or the EN pin. If the output voltage falls below 68% (typ) of the setpoint, the PGOOD pin becomes immediately de-asserted without hysteresis. Re-asserting the PGOOD pin requires resetting either the V5IN pin or the EN pin.

Fault Protection

Overcurrent Limit

TPS51362 integrates both high side and low side FETs to support a maximum DC current of 10-A operation. The current sensing method employed for over current limit is to monitor the SW node during the “ON” state of the low side FET for each switching cycle. TRIP pin is used to program one of the two current limits for TPS51362 operation (see Table 3). When the overcurrent limit is detected, the converter does not allow the next “ON” cycle for the high side FET until the overcurrent limit is no longer reached. This ensures the safe operation of the converter. And when the overcurrent limit condition persists, the current to the load exceeds the current to the output capacitors, the output voltage tends to fall. When the output voltage falls below the undervoltage protection threshold, the converter latch shut down.

Table 3. TRIP Pin Settings

TRIP	TYPICAL OCL LIMIT I_{OCL} (A)
GND	8
5V	12

Negative Overcurrent Limit

TPS51362 is also protected by the negative over current limit. Both positive and negative current limit is programmed by the TRIP pin. Negative current limit level is the same as that of positive current limit level (see Table 3). During the normal converter operation, negative current is not allowed due to the mandatory light load operation for this device (Auto Skip). It is during the OOB or OVP operation, negative overcurrent might be engaged.

Out-of-Bounds Operation (OOB)

When the output voltage rises to 8% above the target value, the out-of-bound operation starts. During the OOB operation, the controller operates in forced PWM-only mode by turning on low side FET. Turning on the low side FET beyond the zero inductor current can quickly discharge the output capacitor thus causing V_{OUT} to fall quickly towards setpoint. During the operation, the cycle by cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

Overvoltage Profection (OVP) and Undervoltage Protection (UVP)

When the output voltage rises to a level 20% (typ) higher than the setpoint voltage, an overvoltage condition is present. When a 0-V event is detected, the converter turns off the high side FET and turns on the low side FET. The operation continues until the cycle by cycle negative current limit is reached and low side FET is turned off and high side FET is turned on, for a minimum on-time. After the minimum on-time expires, the high side FET is driven off and low side FET is driven on again until negative current limit is reached or V_{OUT} is discharged to 0 V. When the V_{OUT} is discharged to 0 V, both high-side and low-side FETs are latched off. An OVP fault requires the V5IN voltage to fall below POR threshold or EN reset to clear.

Undervoltage Protection (UVP)

The undervoltage protection (UVP) is set when the V_{OUT} voltage falls below 68% (typ) of the setpoint voltage for 1msec or longer. In this fault condition, the converter turns off both high-side and low-side FETs. The UVP function is enabled after 1.4 ms of soft start completion. An UVP fault requires 5-V UVLO or EN reset.

V5IN Undervoltage Lockout (UVLO) Protection

TPS51362 has a 5-V supply undervoltage lockout protection (UVLO) threshold. When the V5IN voltage is lower than UVLO threshold voltage, Vout is shut off. This is a non-latch protection.

Power-On-Reset (POR)

To prevent single rail supply voltage brown-out due to output OV condition, when the output voltage is shut down due to OVP fault, Power-on-Reset (POR) on V5IN is implemented. To reset OVP fault, V5IN voltage must fall below POR threshold voltage of 1.7 V (typ) or EN reset to clear.

Thermal Shutdown

TPS51362 includes an internal temperature monitor. If the die temperature exceeds the threshold (published in the EC table of this datasheet), the converter will be shutdown. This is a non-latch protection and the operation is restarted with soft-start sequence when the device temperature is reduced by the hysteresis.

DESIGN PROCEDURE

Introduction

The simplified design procedure is done for a VCCIO rail for Intel platform application using TPS51362.

Step One: Determine the system specifications.

The VCCIO rail requirements provide the following key parameters:

- V_{OUT} = 1.05 V
- $I_{CC(max)}$ = 6 A
- $I_{DYN(max)}$ = 4 A

Step Two: Determine the power supply design specifications.

The input voltage range and operating frequency are of primary interest. For this example:

- 7.4 V ≤ V_{IN} ≤ 19.5 V
- f_{SW} = 800 kHz

Step Three: Set the output voltage.

TPS51362 supports resistor-less fixed voltage operation by the use of both REFIN and REFIN2 pins (see Table 1). Grounding both REFIN and REFIN2 pins provides a 1.05-V fixed output setpoint.

Step Four: Determine inductance value and choose inductor.

Smaller values of inductor have better transient performance and smaller physical size but higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 25% to 50% of the maximum current. For this example,use 30% as a starting point. $I_{L(P-P)}$= 6 A × 0.30 = 1.8 A. For a switching frequency of 800 kHz, maximum 19.5-V input and 1.05-V output.

$$L = \frac{V \times dT}{I_{P-P}} = \frac{(V_{IN} - V_{OUT}) \times \left(\frac{V_{OUT}}{f_{SW} \times V_{IN}} \right)}{I_{P-P}} = \frac{(19.5\,V - 1.05\,V) \times \left(\frac{1.05V}{800\,kHz \times 19.5\,V} \right)}{1.8\,A} = 0.68\,\mu H \quad (5)$$

For this application, a 0.68-µH, 6.8 mm × 7.3 mm × 3.0 mm inductor with typical DCR of 4.8 mΩ and heating current of 16 A is chosen. The Cyntec part number of the inductor is PIMB063T.

Step Five: Calculate SLEW capacitance.

The SLEW pin is used to program the soft-start time. During soft-start operation, the current source used to program the SLEW rate is 10 µA (typ). In this design example, the soft-start timing should be target to be in the range of 500 µs to 2 ms. The proper slew rate design minimizes large inductor current perturbation during the startup, thus reducing the possibility of acoustic noise in the system.

$$C_{SLEW} = I_{SLEW} \times \frac{dt}{\Delta V_{OUT}} = 10\,nF \quad (6)$$

- I_{SLEW} = 10 µA,
- dt = t_{SS} = 1 ms
- ΔV_{OUT} = 1.05 V

Step Six: Select the proper OCL.

There are two options for the over current limit (see Table 3). For this application example, because $I_{CC(max)}$ = 6 A, the proper OCL level should be set at least 30% over the $I_{CC(max)}$ level, which makes the 8-A OCL appropriate for this design. Grounding the TRIP pin achieves this effect.

Step Seven: Determine the output capacitance.

The amount of the output capacitance needed for this design is both a function of loop stability and of transient requirement.

Stability Considerations

The switching frequency of the design example is 800 kHz (which is set by the MODE pin, see Table 3). For D-CAP2 mode operation, it is generally recommended to have a unity gain crossover (f0) of less than 1/4 or 1/3 of the switching frequency, which is approximately between 200 kHz and 266 kHz. In this design example, use 1/4.

$$f_0 = \frac{f_{SW}}{4} = 200\,kHz \tag{7}$$

Given the range of the recommended unity gain crossover frequency, the power stage design is flexible, as long as the L-C double pole frequency is less than 10% of f_0.

When the above criteria is met, the internal compensation network provides sufficient phase boost at the unity gain crossover frequency such that the converter is stable with sufficient phase margin (greater than 60 deg.).

When the ESR frequency of the output bulk capacitor is in the vicinity of the unity gain crossover frequency of the loop, additional phase boost can be achieved. This applies to higher ESR output bulk capacitor, POSCAP and SPCAP.

When the ESR frequency of the output capacitor is beyond the unity gain crossover frequency of the control loop, no additional phase boost is achieved. This applies to low or ultra low ESR output capacitor, such as MLCCs.

For this application example,consider only all MLCCs for output capacitors. Based on Equation 3 and Equation 7, the minimum capacitance for stable operation is calculated to be 110 µF.

Transient considerations

- $I_{DYN(max)}$ = 4 A
- di/dt = 2.5 A/µs
- V_{OUT} deviation = ±3% for the given transient

Use Equation 8 and Equation 9 to estimate the amount of capacitance needed for a given dynamic load/release.

$$C_{OUT(min\_under)} = \frac{L \times \left(\Delta I_{LOAD(max)}\right)^2 \times \left(\frac{V_{OUT} \times t_{SW}}{V_{IN(min)}} + t_{MIN(off)}\right)}{2 \times \Delta V_{LOAD(insert)} \times \left(\left(\frac{V_{IN(min)} - V_{OUT}}{V_{IN(min)}}\right) \times t_{SW} - t_{MIN(off)}\right) \times V_{OUT}} \tag{8}$$

$$C_{OUT(min\_over)} = \frac{L_{OUT} \times \left(\Delta I_{LOAD(max)}\right)^2}{2 \times \Delta V_{LOAD(release)} \times V_{OUT}} \tag{9}$$

Based on these calculation, to meet the transient requirement, the minimum amount of capacitance in this design is 164 µF.

Considering both stability and transient, the minimum capacitance is 164 µF. The design example uses 8, 22-µF capacitors with minor consideration of the MLCC derating for both DC and AC effect.

Step Eight: Select decoupling and peripheral components.

For the TPS51362, peripheral capacitors use the following minimum values of ceramic capacitance. X5R or better temperature coefficient is recommended. Tighter tolerance and higher voltage rating are always appropriate.

- V5IN decoupling ≥ 2.2 µF, ≥ 10 V
- VREF decoupling 0.1 µF to 1 µF, ≥ 4 V
- Bootstrap capacitor ≥ 0.1 µF, ≥ 10 V
- Pull-up resistors on PGOOD, 100 kΩ

Step Nine: Layout guidelines.

Figure 22 applies to the layer where device is situated. Additional reinforcement of VIN, PGND, and VOUT through vias are always recommended.

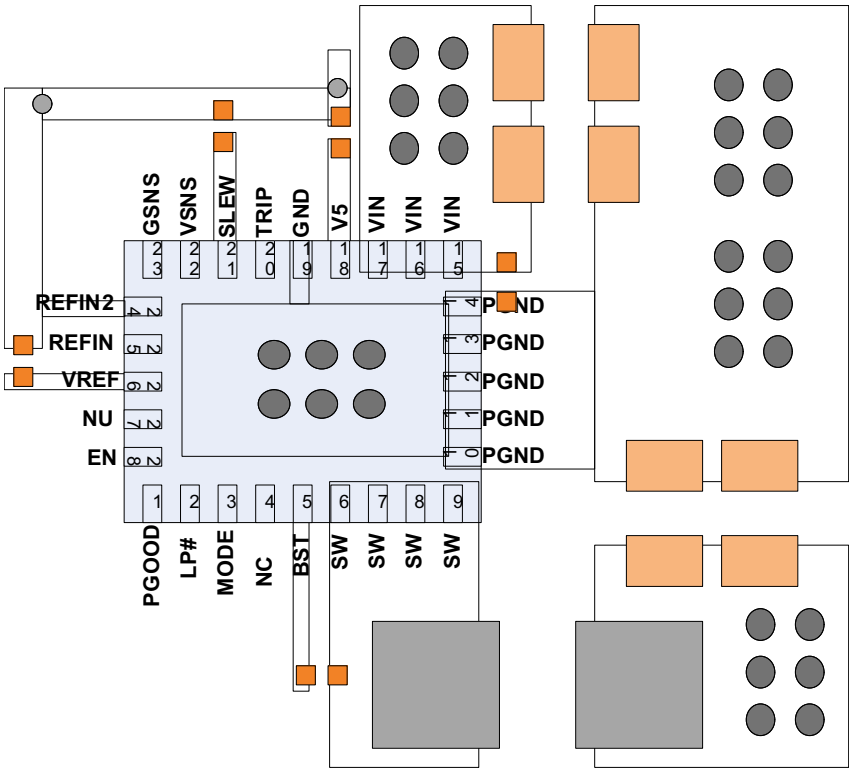


Figure 22. TPS51362 Design Layout

Input capacitors, output capacitors, and the output inductor are the power components and should be placed on one side of the PCB. Small signal components can be placed on the same side of the PCB with proper ground isolation or the opposite side with at least one inner ground plane in between, depending on the system/motherboard design requirement.

All sensitive analog traces and components such as VSNS, GSNS, SLEW, VREF, REFIN and REFIN2 should be placed away from the high voltage switching node, such as SW and BST to avoid switching noise coupling. Use internal layer(s) as ground plane(s) and shield feedback traces from power traces.

VSNS can be connected directly to the output voltage sense point at the load device or the bulk capacitor at the converter side. Connect GSNS to ground return at the general ground plane/layer. VSNS and GSNS can be used for the purpose of remote sensing across the load device, however, ensure to minimize the routing trace length to prevent excess noise injection into the sense lines.

In order to effectively remove heat from the package, prepare the thermal land and solder to the package thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps to dissipate the heat. Numerous vias (at least 6) with a 0.3-mm diameter connected from the thermal land to the internal/solder side ground plane(s) should be used to help dissipation.

REFERENCE DESIGNS

This section describes one typical application circuit using the TPS51362.

Design 1

This design is a VCCIO application with an output voltage of 1.05 V, maximum processor current ($I_{CC(max)}$) of 6 A, an OCL of 8 A and a switching frequency of 800 kHz.

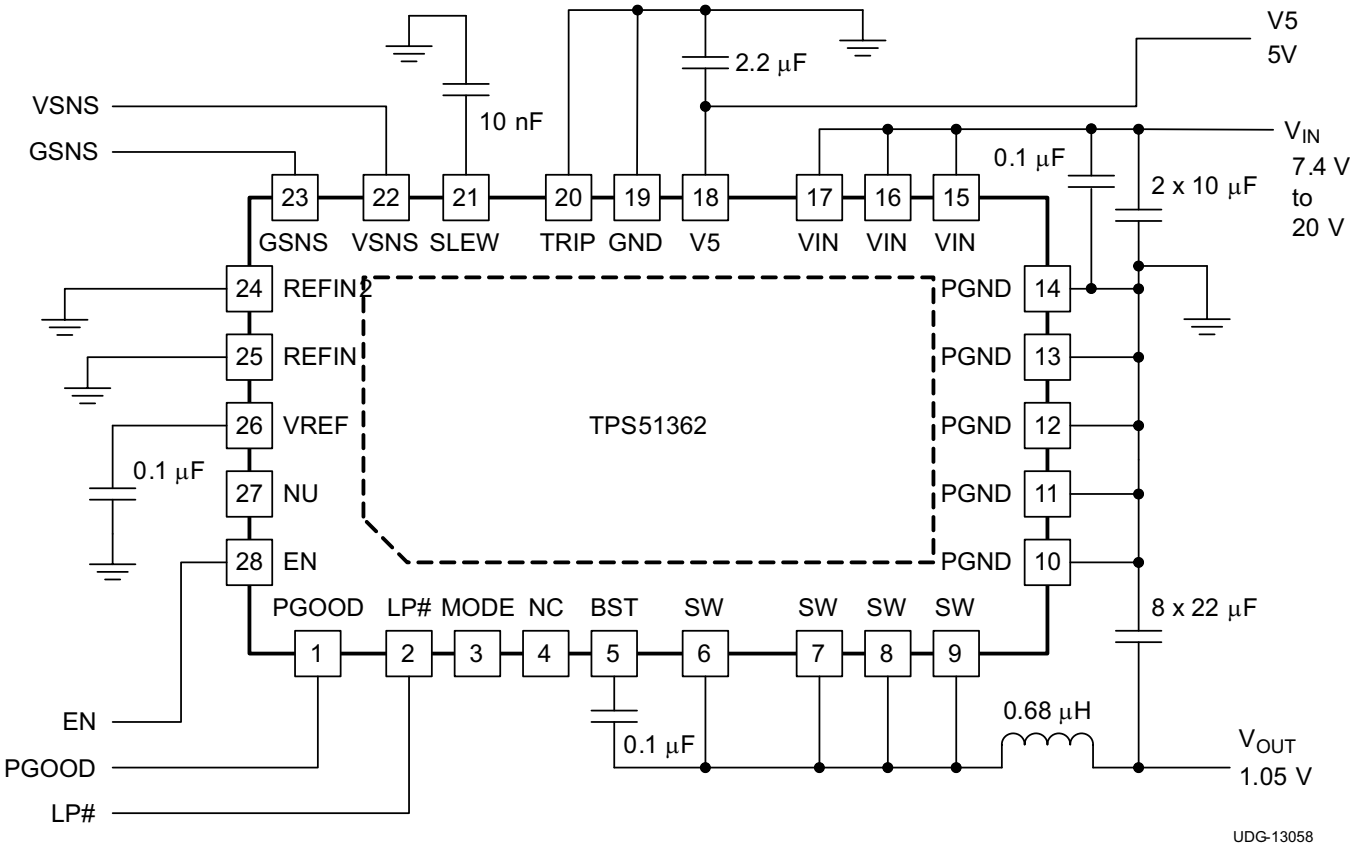


Figure 23. Design 1: Application Schematic

Table 4. Design 1: List of Materials

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	2	10 µF, 25 V	Taiyo Yuden	TMK325BJ106MM
C_{OUT}	8	22 µF, 6.3 V	Murata	GRM21BB30J226ME38
L_{OUT}	1	0.68 µH, 4.8 mΩ	Cyntec	PIMB063T-R68MS-63

REVISION HISTORY

NOTE: Page numbers of current version may differ from previous versions.

Changes from Original (February 2013) to Revision A **Page**

- Added MIN and MAX values to I_{OCL} spec in the Elec Characteristics table 5
- Changed the Functional Block Diagram V_{REFIN} signal line identifier on the UV-detect device from "$V_{REFIN\ -\ 32\%}$" to "$V_{REFIN\ -\ 34\%}$". Changed signal line identifier on the high-side comparator from "V_{REFIN}+ 8/20%" to "V_{REFIN}+ 20%". Changed the high-side device symbol from hysteresis to a comparator. Changed signal line identifier on the low-side device from "V_{REFIN}– 8/32%" to "V_{REFIN}– 8/34%. 8
- Added Land pads for a 0.1-µF capacitor between VIN and PGND of the TPS51362 Design Layout figure. 19
- Added a 0.1-µF capacitor symbol between VIN and PGND of the Design 1: Application Schematic. 20
- Changed L_{OUT} inductor part number from PIMB063T to PIMB063T-R68MS-63 in Design 1: List of Materials table. 20

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
FX026	Active	Production	VQFN-CLIP (RVE) | 28	3000 | LARGE T&R	ROHS Exempt	NIPDAU	Level-2-260C-1 YEAR	-10 to 85	TPS51362
TPS51362RVER	Active	Production	VQFN-CLIP (RVE) | 28	3000 | LARGE T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-10 to 85	TPS51362
TPS51362RVET	Active	Production	VQFN-CLIP (RVE) | 28	250 | SMALL T&R	ROHS Exempt	NIPDAU | SN	Level-2-260C-1 YEAR	-10 to 85	TPS51362

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

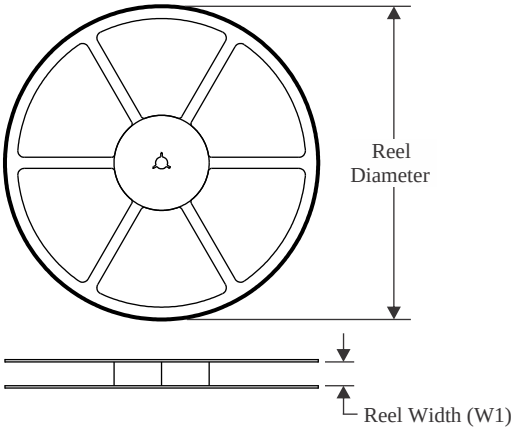
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

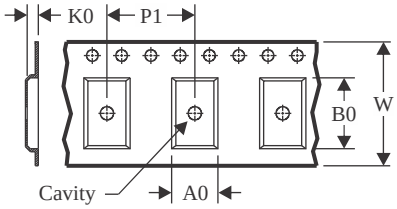
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

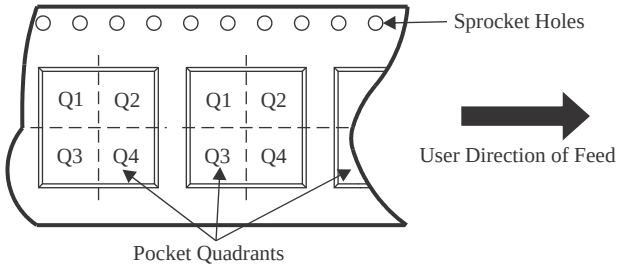


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

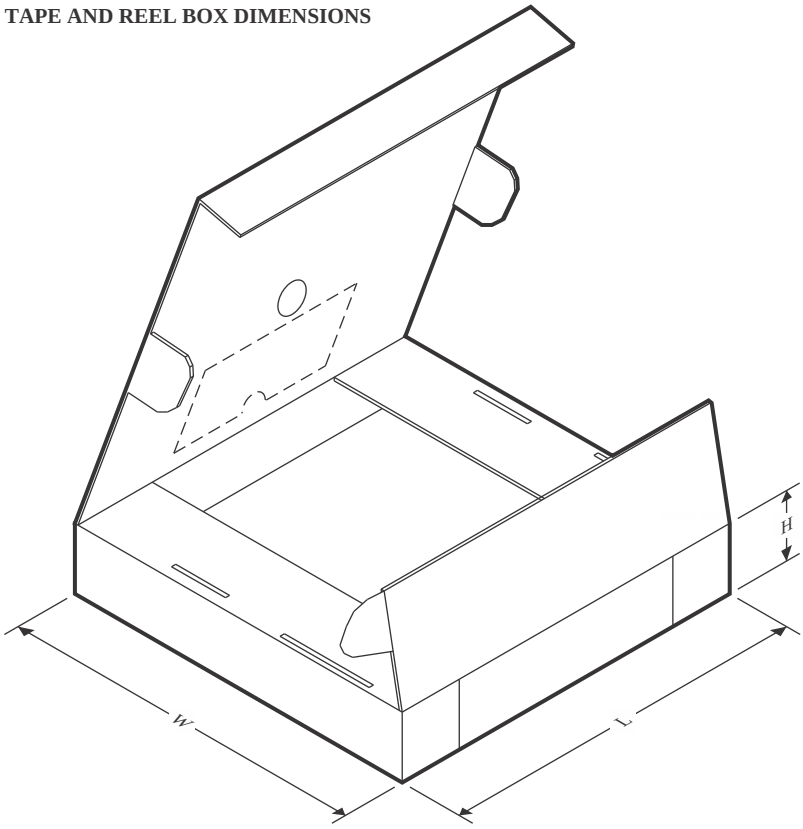
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51362RVER	VQFN-CLIP	RVE	28	3000	330.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1
TPS51362RVET	VQFN-CLIP	RVE	28	250	180.0	12.4	3.71	4.71	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

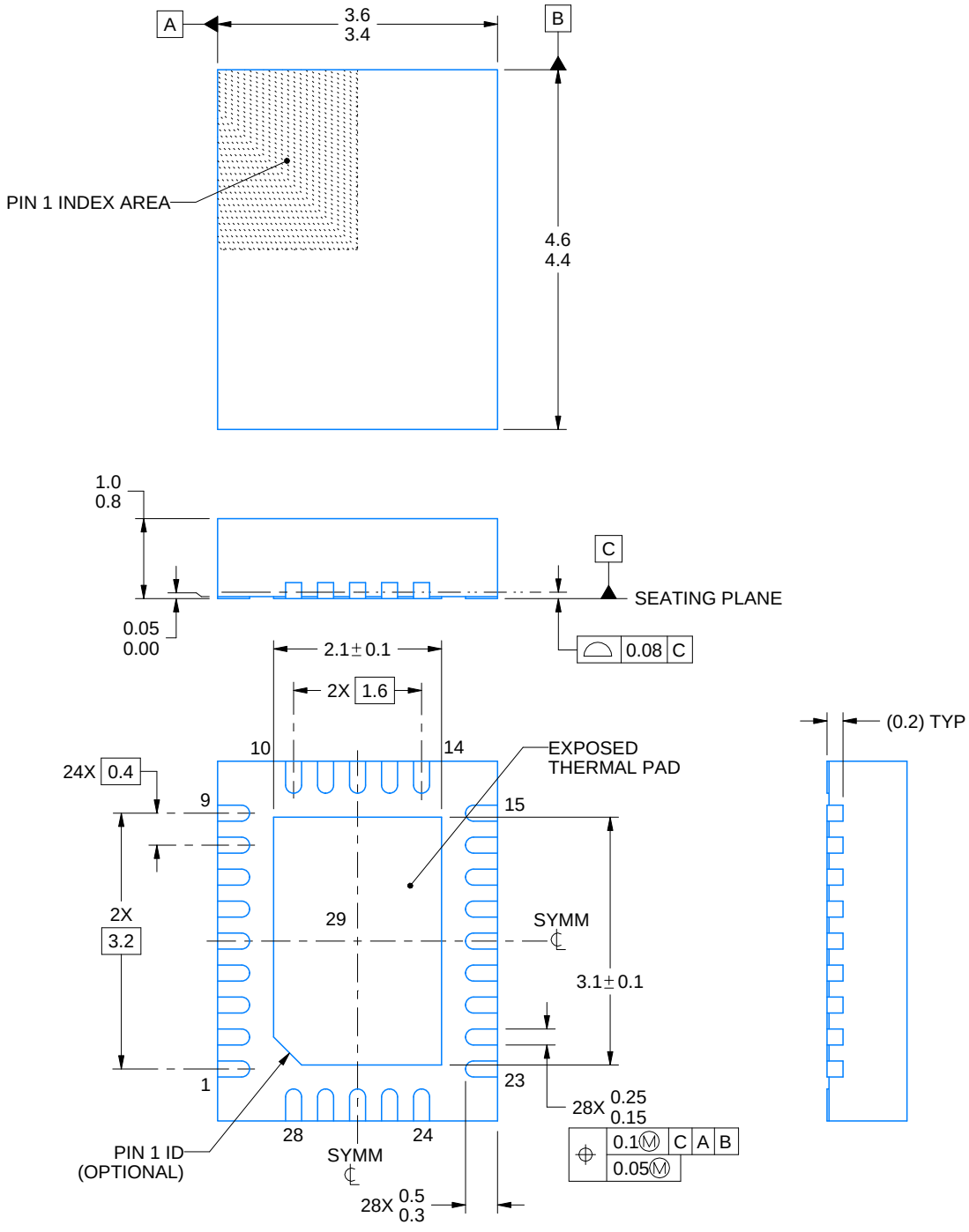
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51362RVER	VQFN-CLIP	RVE	28	3000	346.0	346.0	33.0
TPS51362RVET	VQFN-CLIP	RVE	28	250	210.0	185.0	35.0

PACKAGE OUTLINE

RVE0028A

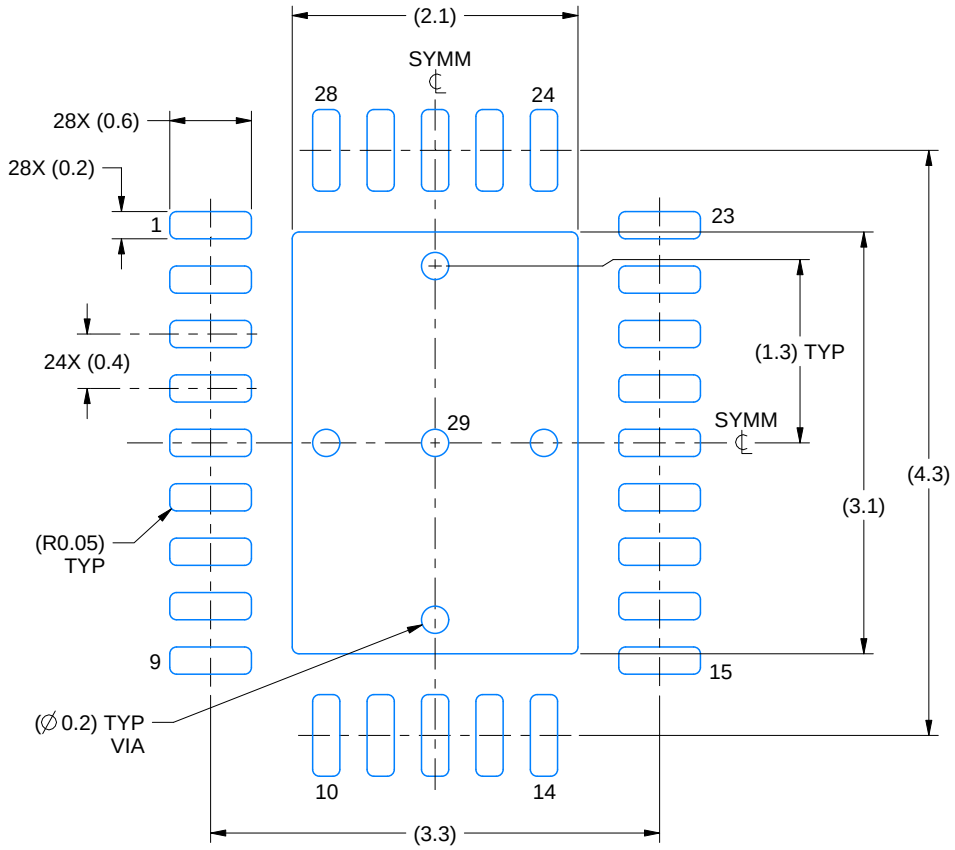
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

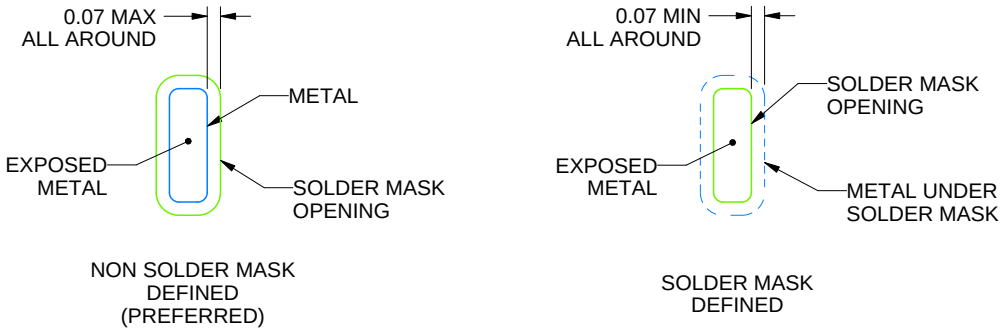


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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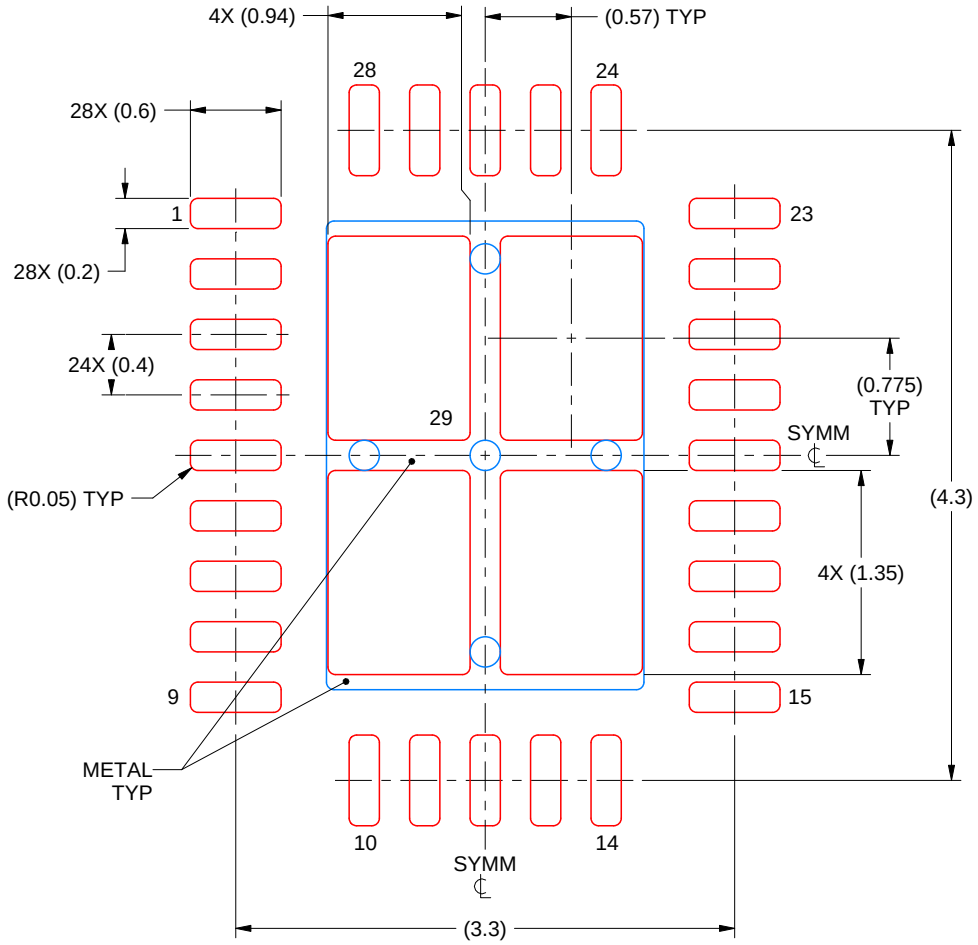
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 29
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219151/A 07/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

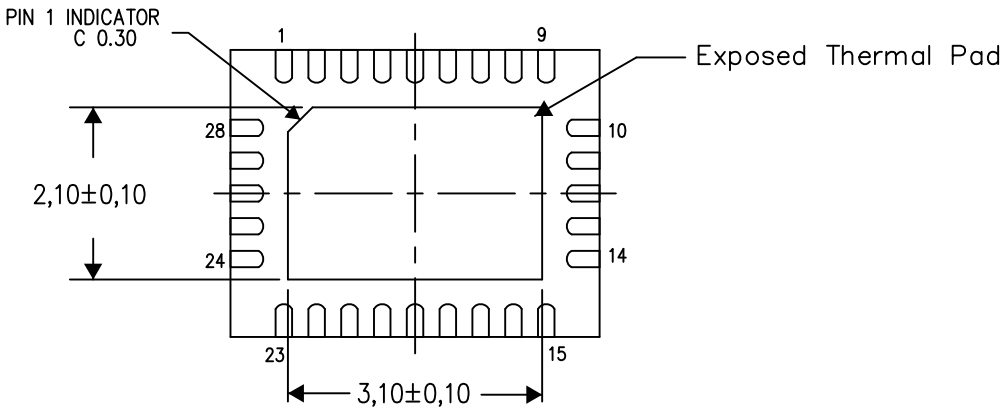
RVE (R–PVQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



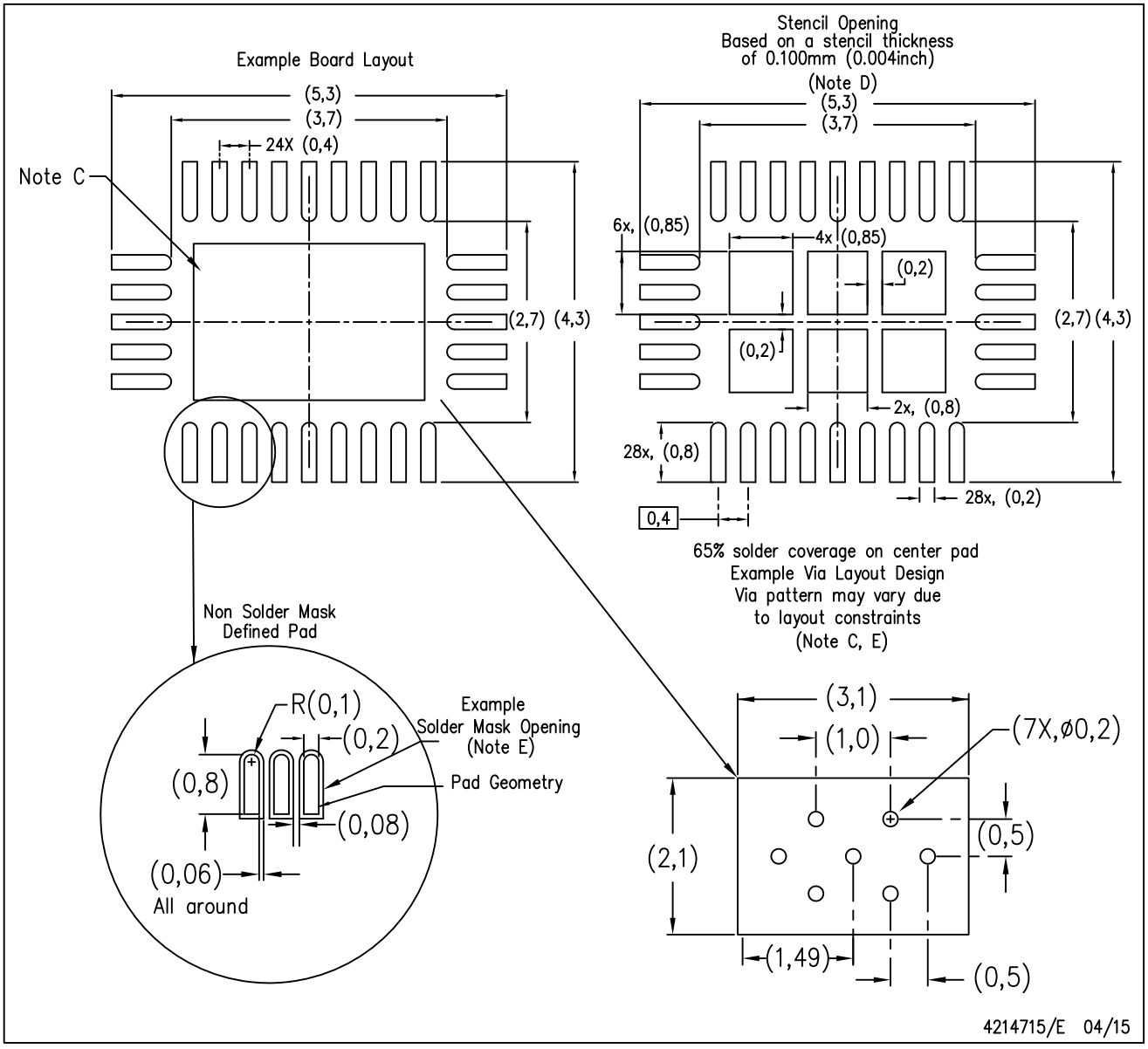
Bottom View

Exposed Thermal Pad Dimensions

4211776/E 04/15

NOTE: All linear dimensions are in millimeters

RVE (R–PWQFN–N28) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Electroformed stencils offer adequate release at thicker values/lower Area Ratios. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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