

## 5V 输入或 3.3V 输入，3A 完全集成转换器

查询样品: [TPS51313](#)

### 特性

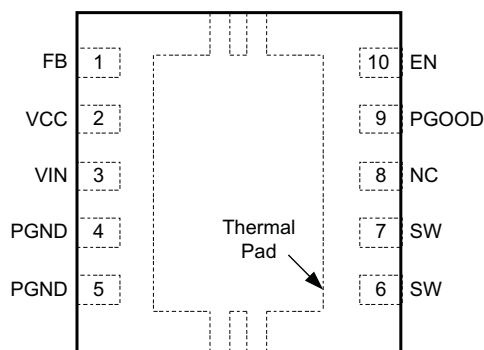
- 输入电压 **VIN** 范围: **3.1V 至 5.5V**
- 偏置电压 **VCC** 范围: **3.1V 至 5.5V**
- 输出电压范围: **0.6V 至 3.3V**
- **0.6V, 1%** 电压基准精度
- 开关频率: **1MHz**
- 无需外部补偿
- 固定电压伺服器软启动功能
- 过热保护

### 应用范围

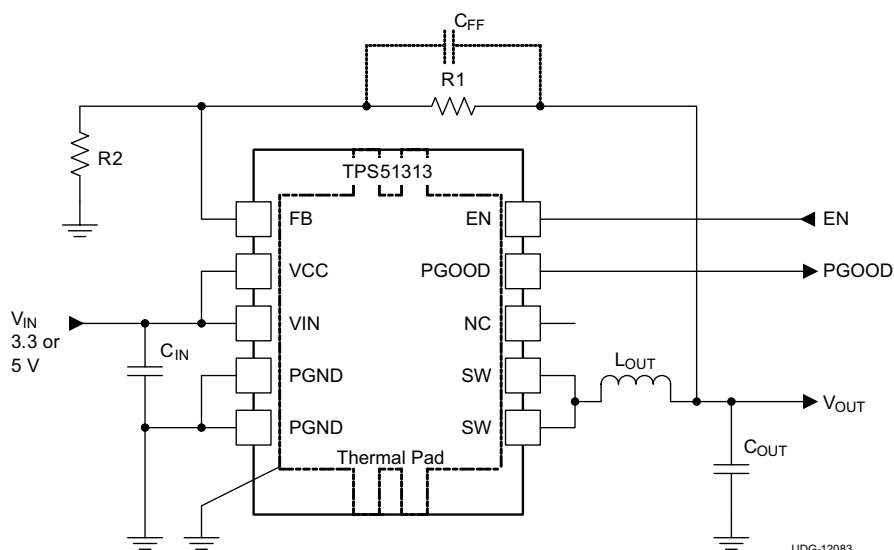
- 离散图形 **PCIe® PEX** 轨
- 低压负载点 (**POL**) 电源轨

### 说明

TPS51313 是一款针对低压负载点应用的易于使用的、完全集成、同步降压转换器。它被设计成符合 NVIDIA™ OpenVreg 类型 0 技术规范，其中包括对封装和封装尺寸的要求。它在输出电压介于 0.6V 至 3.3V 之间时支持 3A（最大值）直流输出电流。D-CAP2™ 模式适应、恒定接通时间控制（开关频率 1MHz）可在使用全陶瓷输出电容器设计时实现小封装尺寸并提供一个低外部组件数量。此器件还在轻负载条件下特有自动跳跃功能、预偏置启动和内部固定软启动时间。当器件被禁用时，输出电容器通过内部电阻器放电。TPS51313 采用 3mm × 3mm, 10 引脚 DRC 封装（符合 RoHs 环保标准且无铅），额定温度范围为 -10°C 至 85°C。



### 简化的应用



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English Data Sheet: [SLUSB31](#)

# TPS51313

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE	ORDERABLE DEVICE NUMBER	PINS	OUTPUT SUPPLY	MINIMUM QUANTITY	ECO PLAN
-10°C to 85°C	Plastic SON (DRC)	TPS51313DRCR	10	Tape and reel	3000	Green (RoHS and no Pb/Br)
		TPS51313DRCT		Mini reel	250	

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

		VALUE		UNIT
		MIN	MAX	
Input voltage range <sup>(2)</sup>	VIN, VCC	-0.3	6.0	V
	SW	-2.0	6.0	
	SW (transient 20nsec)	-3.0	8.5	
	EN	-0.3	6.0	
	FB	-1	3.6	
Output voltage range <sup>(2)</sup>	PGOOD	-0.3	6.0	V
Junction temperature, T <sub>J</sub>			125	°C
Storage temperature, T <sub>stg</sub>		-55	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the network ground terminal unless otherwise noted.

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		TPS51313 DRC (10-PIN)	UNITS
θ <sub>JA</sub>	Junction-to-ambient thermal resistance	42.4	°C/W
θ <sub>JCTop</sub>	Junction-to-case (top) thermal resistance	53.9	
θ <sub>JB</sub>	Junction-to-board thermal resistance	18.1	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.1	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	18.3	
θ <sub>JCbot</sub>	Junction-to-case (bottom) thermal resistance	6.3	

- (1) 有关传统和新的热 度量的更多信息，请参阅IC 封装热度量应用报告， [SPRA953](#)。

## RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Input voltage range	VIN, VCC	-0.1	5.5	V
	SW	-0.1	5.5	
	EN	-0.1	5.5	
	FB	-0.1	3.5	
Output voltage range	PGOOD	-0.1	5.5	V
Operating free-air temperature, T <sub>A</sub>		-10	85	°C

## ELECTRICAL CHARACTERISTICS

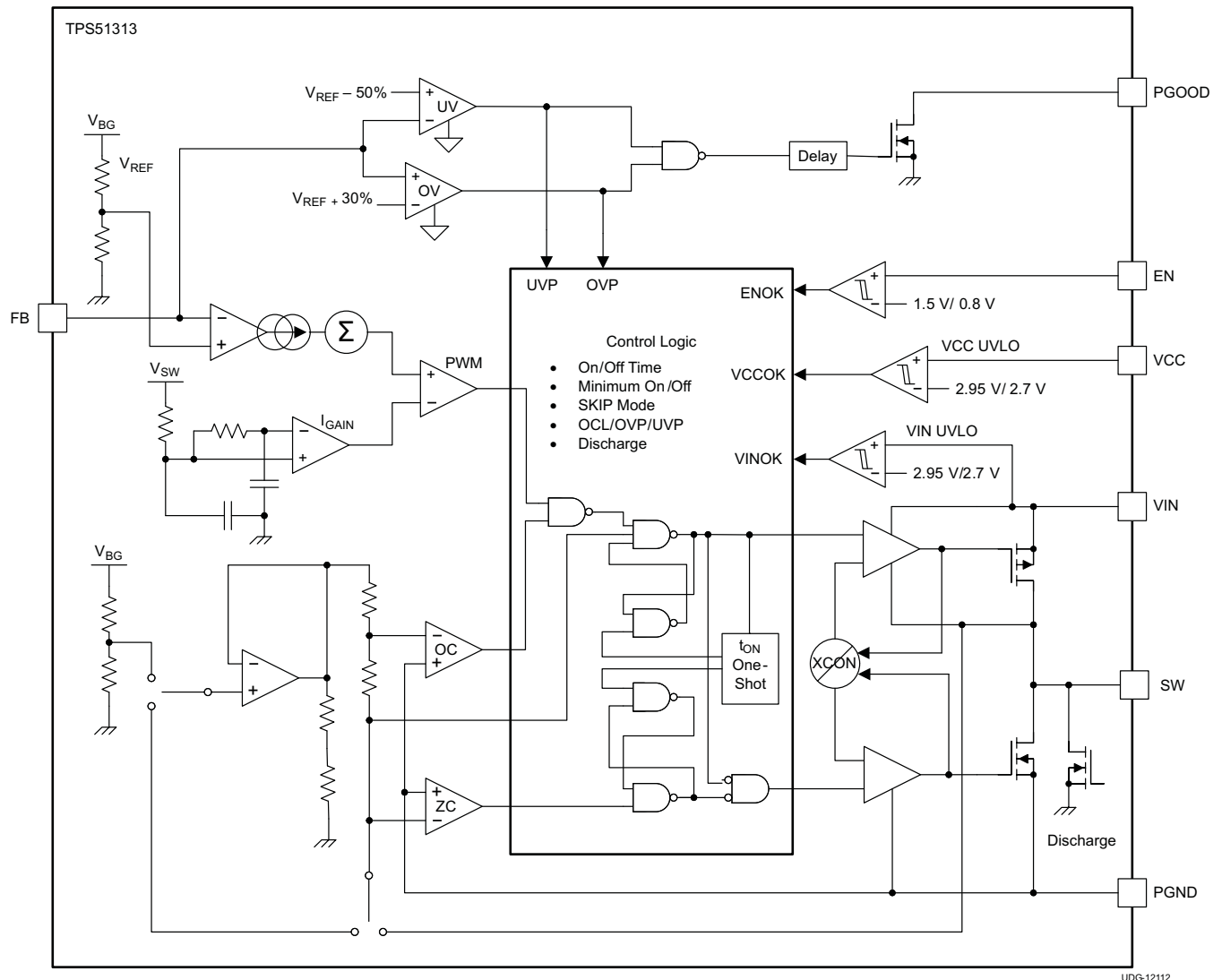
Over operating free-air temperature range,  $V_{IN} = 5\text{ V}$ ,  $V_{CC} = 5\text{ V}$ ,  $V_{EN} = 3.3\text{ V}$  (unless otherwise noted).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
V <sub>IN</sub>	Supply voltage		3.1		5.5	V
V <sub>CC</sub>	Supply voltage		3.1		5.5	V
SUPPLY CURRENT						
I <sub>IN</sub>	Input voltage supply current	EN = High			100	μA
I <sub>SD</sub>	Input voltage shutdown current	EN = Low			12	μA
I <sub>VCC(in)</sub>	VCC supply current	EN = High		700		μA
I <sub>VCC(sd)</sub>	VCC shutdown current	EN = Low, T <sub>A</sub> = 25°C			20	μA
VFB REFERENCE VOLTAGE						
V <sub>FREF</sub>	Reference voltage			0.6		V
V <sub>FREFTOL</sub>	Reference voltage tolerance	T <sub>A</sub> = 25°C	−1%		1%	
I <sub>FB</sub>	Feedback pin leakage current		−100		100	nA
SMPS FREQUENCY						
f <sub>SW</sub>	Switching frequency	EVM close loop measurement. V <sub>IN</sub> = 5 V, V <sub>OUT</sub> = 1.05 V, I <sub>OUT</sub> = 3 A		1		MHz
t <sub>OFF(min)</sub>	Minimum off-time		110	190	270	ns
t <sub>DEAD</sub>	Deadtime <sup>(1)</sup>	SW node high, V <sub>IN</sub> = 5 V		9		ns
		SW node low, V <sub>IN</sub> = 5 V		10		
LOGIC THRESHOLD						
V <sub>LL</sub>	EN low-level voltage				0.8	V
V <sub>LH</sub>	EN high-level voltage		1.5			V
I <sub>LLK</sub>	EN input leakage current	V <sub>IN</sub> = V <sub>CC</sub> = 3.3 V	−3	1	3	μA
SOFT START						
t <sub>SS</sub>	Soft-start time <sup>(1)</sup>	V <sub>FB</sub> rising from 0 V to 0.6 V		300		μs
PGOOD COMPARATOR						
V <sub>PGTH</sub>	PGOOD threshold	PGOOD out to higher w/r/t V <sub>FB</sub>		130%		
		PGOOD out to lower w/r/t V <sub>FB</sub>		50%		
t <sub>PGDLY</sub>	PGOOD high delay time	Delay for PGOOD in, after EN = Hi		1.3		ms
I <sub>PGLK</sub>	PGOOD leakage current		−1	0	1	μA
CURRENT DETECTION						
I <sub>OCL</sub>	Current limit threshold	Valley current limit, V <sub>IN</sub> = V <sub>CC</sub> = 3.3 V, T <sub>A</sub> = 25°C	4.8			A
PROTECTIONS						
V <sub>IN_UVLO</sub>	VIN UVLO threshold voltage	Wake-up	2.85	2.95	3.05	V
		Shutdown	2.6	2.7	2.8	
V <sub>CC_UVLO</sub>	VCC UVLO threshold voltage	Wake-up	2.85	2.95	3.05	
		Shutdown	2.6	2.7	2.8	
V <sub>OVP</sub>	OVP threshold voltage	OVP detect voltage, overdrive = 100 mV		130%		
t <sub>OVP</sub>	OVP delay time	Overdrive = 100 mV		1.9		μs
V <sub>UVP</sub>	UVP threshold voltage	UVP detect voltage, overdrive = 100 mV		50%		
t <sub>UVPDLY</sub>	UVP delay time	Overdrive = 100 mV		2.4		μs
SW PULL DOWN						
R <sub>SWPD</sub>	Switch node pull down resistance	EN = Lo		260		Ω
THERMAL SHUTDOWN						
T <sub>SDN</sub>	Thermal shutdown threshold <sup>(1)</sup>	Shutdown temperature		145		°C
		Hysteresis		20		

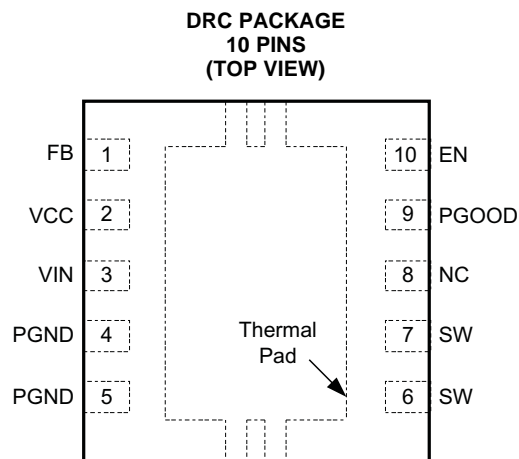
(1) Specified by design. Not production tested.

## DEVICE INFORMATION

### Functional Block Diagram



UDG-12112



### PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	10	I	Enable function for the switched-mode power supply (SMPS) (3.3-V logic compatible)
FB	1	I	Voltage feedback. Also used for OVP, UVP and PGOOD determination.
NC	8	I	No connect. Make no external connection to this pin.
PGND	4	I	Device ground
	5		
PGOOD	9	O	Power good indicator. Requires external pull-up resistor.
SW	6	I	Switching node output. Connect to external inductor. Also serve as current sensing negative input for over current protection purpose
	7		
VCC	2	I	Power supply for analog circuit.
VIN	3		Main power conversion input and gate-drive voltage supply for output FETs.
Thermal Pad			Connect to PGND.

## TYPICAL CHARACTERISTICS

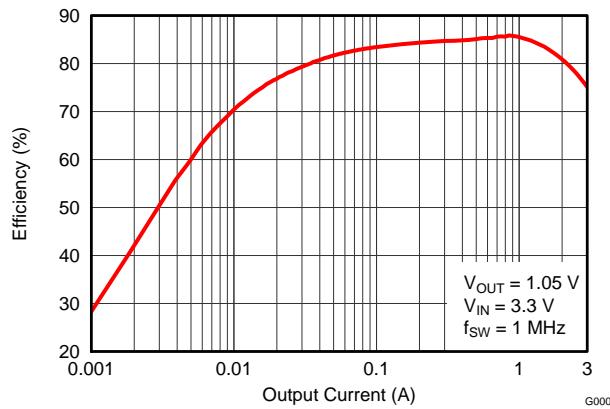


Figure 1. Efficiency vs. Output Current

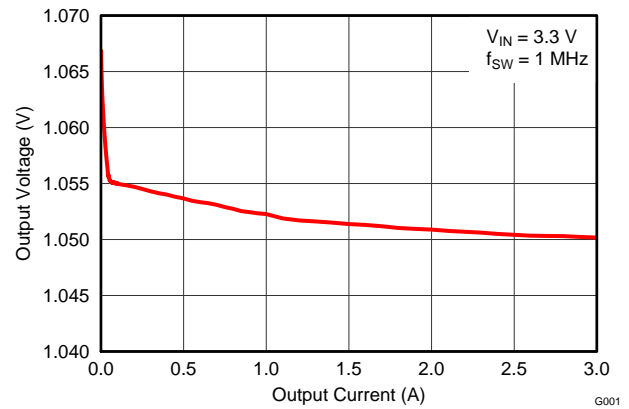


Figure 2. DC Load Regulation

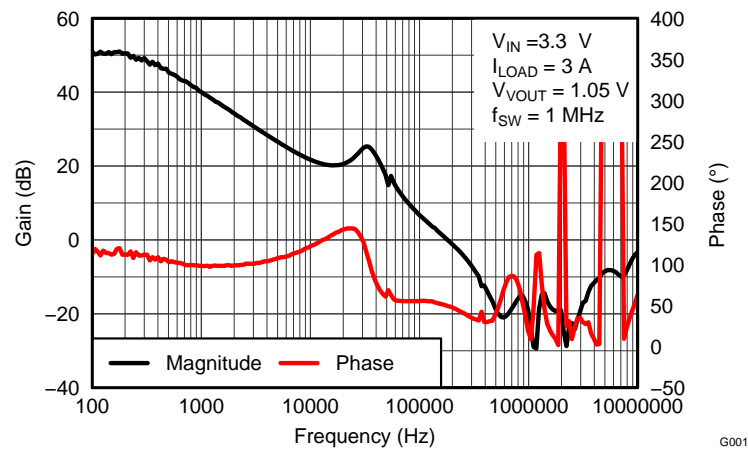


Figure 3. Bode Plot

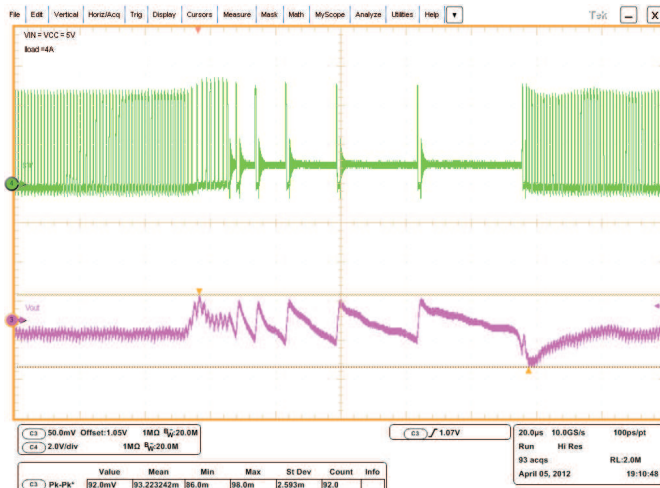


Figure 4. Fast 0-A to 3-A Transient Response

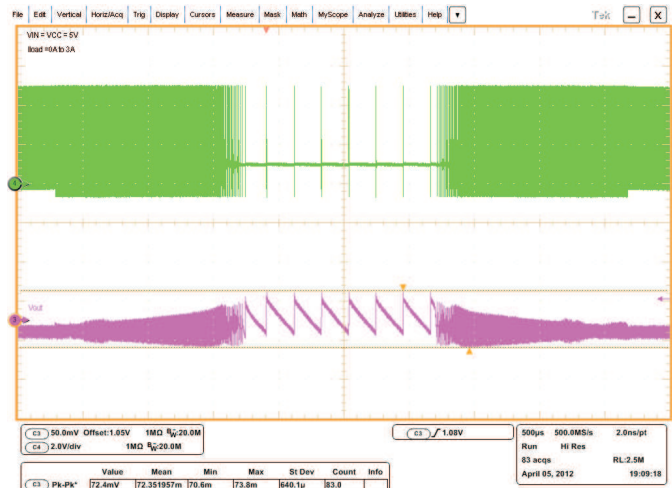


Figure 5. Slow 0-A to 3-A Transient Response

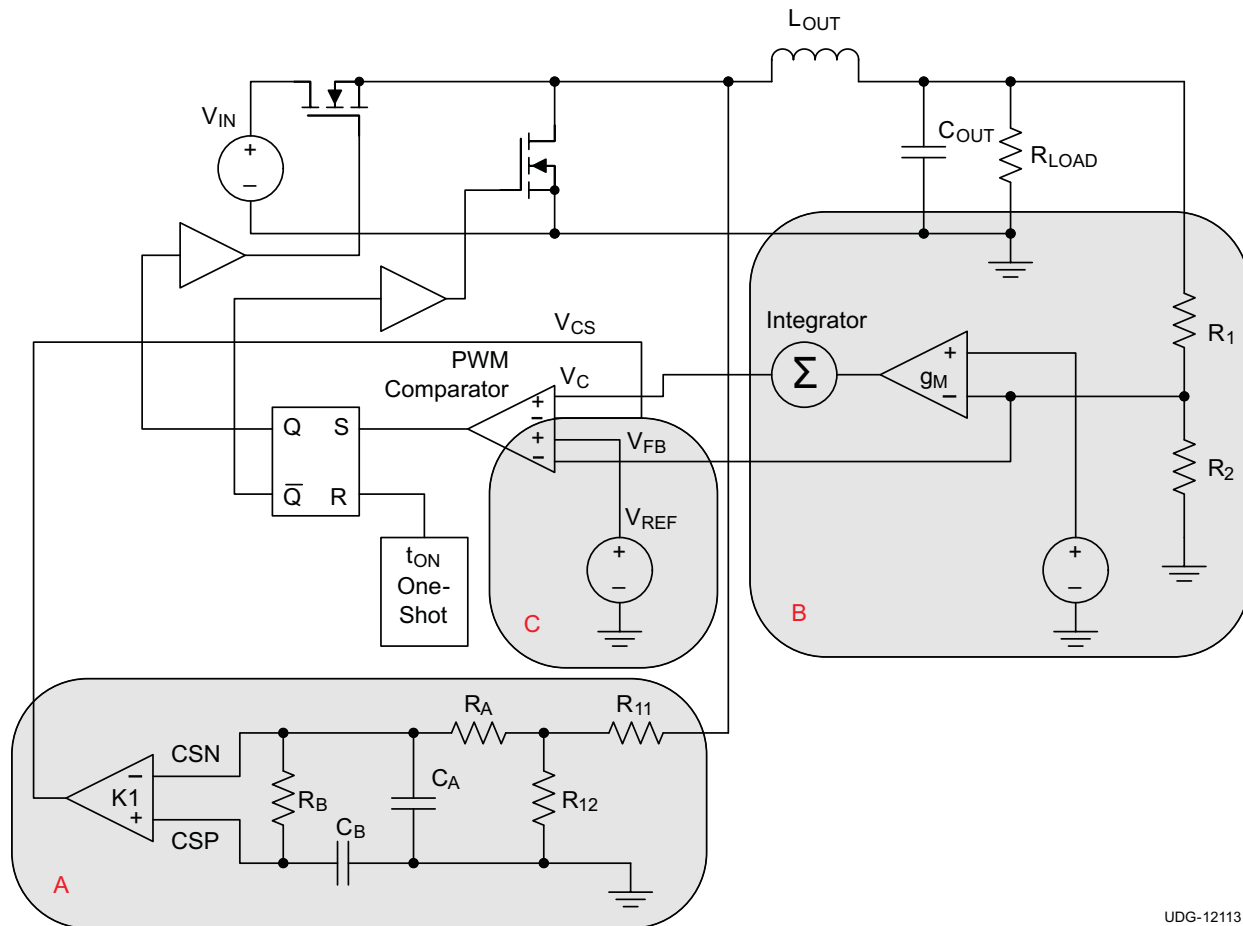
## APPLICATION INFORMATION

### Functional Overview

TPS51313 is a D-CAP2 mode adaptive on time converter with internal integrator. Monolithically integrate high side and low side FET supports output current to a maximum of 3-ADC. The converter automatically runs in discontinuous conduction mode to optimize light load efficiency. A switching frequency of 1-MHz enables optimization of the power train for the cost, size and efficiency performance of the design.

### PWM Operation

The PWM operation is comprised of three separate loops, A, B and C as shown in [Figure 6](#).



UDG-12113

**Figure 6. PWM Operation**

#### Internal Current Loop (A)

Loop A is the internal current loop. The current information is sampled, divided and averaged at the SW node. The RC time constant and the gain of the current sense amplifier is chosen to cover the wide range of power stage design intended for this application.

#### Internal Voltage Loop (B)

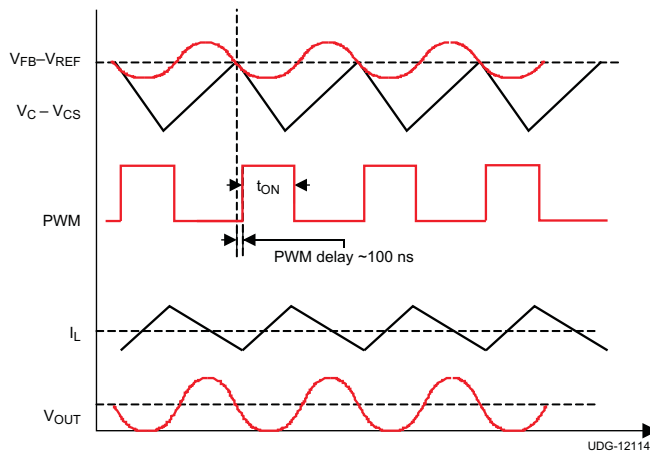
Loop B is the internal voltage loop. The feedback voltage information is compared to the voltage reference at the input of the  $g_M$  amplifier, the internal integrator is designed to provide a zero at the double pole location to boost phase margin at the desired crossover frequency.

## Fast Feedforward Loop (C)

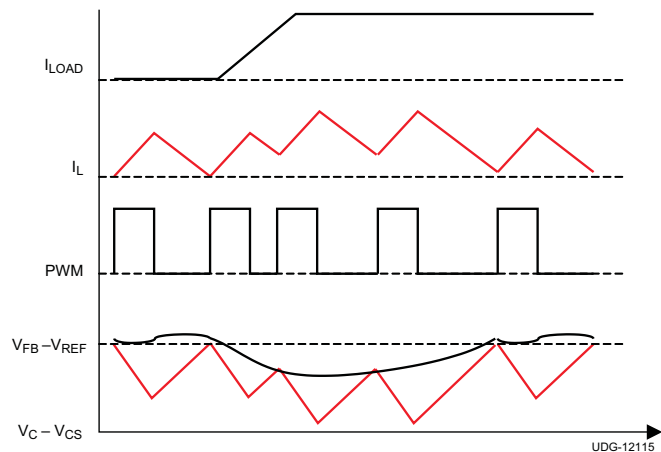
Loop C is the additional loop that acts a direct fast feedforward loop to enhance the transient response.

In steady state operation as shown in Figure 7, the on time is initiated by the interaction of the three loops mentioned above. When the  $(V_C - V_{CS})$  is rising above threshold defined by  $(V_{FB} - V_{REF})$ , the PWM comparator issues the on time pulse after the propagation delay. The demand of on time occurs when the artificial current has reached the valley point. The load regulation is maintained by the integrator provided by the  $g_M$  amplifier and internal integrator.

In transient operation as shown in Figure 8, the benefit of this topology is becoming evident. In an all MLCC output configuration, especially when the output capacitance is low, when the load step is applied, the output voltage is immediately discharged to try to keep the load demand. The immediate reflection of the load demand is instantly reflected in the FB voltage. The  $(V_{FB} - V_{REF})$  is thus served as a termination voltage level for the  $(V_C - V_{CS})$ , thus modulating the initiation of the on time. The transient response can be improved further by amplifying the difference between  $V_{FB}$  and the  $V_{REF}$  reference.



**Figure 7. Steady-State Operation**



**Figure 8. Transient Operation**

## PWM Frequency

The TPS51313 operates at a switching frequency of 1 MHz.

## Light Load Power Saving Features

The TPS51313 offers an automatic pulse-skipping feature to provide excellent efficiency over the entire load range. The converter senses the current when the low-side FET is on and prevents negative current flow by turning off the low side FET. This saves power by eliminating re-circulation of the inductor current. When the bottom FET is turned off, the converter enters discontinuous mode, and the switching frequency decreases, reducing switching loss.

## Power Sequences

TPS51313 initiates the soft-start process when the EN, VIN and VCC pins are ready. The soft-start time 300  $\mu$ s when the reference voltage is between 0 V and 0.6 VREF. The actual output ramp-up time is the same as that of the VREF start-up time, which is 300  $\mu$ s.

## Power Good Signal

The TPS51313 has one open-drain power good (PGOOD) pin. During initial startup, there is a 1.3-ms power good high propagation delay after EN goes high. The PGOOD de-asserts when the EN is pulled low or an undervoltage condition on VCC or VIN or any other faults (such as V\_OUT, UVP, OCP, OVP) that require latch off action is detected.

## Protection Features

The TPS51313 offers many features to protect the converter power chain as well as the system electronics.



### Input Undervoltage Protection on $V_{CC}$ and $V_{IN}$ (UVLO)

The TPS51313 continuously monitor the voltage on the  $V_{CC}$  and  $V_{IN}$  to ensure the voltage level is high enough to bias the converter properly and to provide sufficient gate drive potential to maintain high efficiency for the converter. The converter starts with  $V_{CC}$  and  $V_{IN}$  approximately 2.95 V and has a nominal of 250 mV of hysteresis, assuming EN is above the logic threshold level. If the UVLO level is reached for either  $V_{CC}$  or  $V_{IN}$ , the converter transitions the SW node into a tri-state and remains off until the device is reset by both  $V_{CC}$  and  $V_{IN}$  reaches 2.95 V (nominal). The PGOOD is deasserted when UVLO is detected and remains low until the device is reset. The device resumes operation when VIN recovers to 2.95 V (nominal).

### Output Overvoltage Protection (OVP)

The TPS51313 has OVP protection circuit. An OVP event is detected when the FB voltage is approximately  $130\% \times 0.6V_{REF}$ . In this case, the converter de-asserts the PGOOD signal and performs the overvoltage protection function. The converter latches off both high-side and low-side FET (after a typical delay of 1.9  $\mu$ s) and remains in this state until the device is reset by EN, or  $V_{CC}$  or  $V_{IN}$ .

### Output Undervoltage Protection (UVP)

Output undervoltage protection works in conjunction with the current protection described in the [Overcurrent and Current Limit Protection](#) section. If the FB voltage drops below  $50\% \times 0.6 V_{REF}$ , after a delay of 2.4  $\mu$ s, the converter latches off. Undervoltage protection can be reset by EN,  $V_{CC}$  or  $V_{IN}$ .

### Overcurrent and Current Limit Protection

The TPS51313 provides an overcurrent protection function. The minimum OCP level is 4.8-A DC. When the current limit is exceeded for consecutive 9 cycles, the converter latches off and remains latched off until it is reset by EN,  $V_{CC}$  or  $V_{IN}$ .

The TPS51313 also provides current limit protection function. If the sense current is above the OCL setting, the converter delays the next on pulse until the current level drops below the OCL limit. Current limiting occurs on a pulse-by-pulse basis. During a fast or very fast overcurrent event, the output voltage tends to droop until the UVP limit is reached. Then the converter de-asserts the PGOOD signal, and latches off after a delay between 1  $\mu$ s and 2  $\mu$ s. The converter remains in this state until the device is reset by EN,  $V_{CC}$  or  $V_{IN}$ .

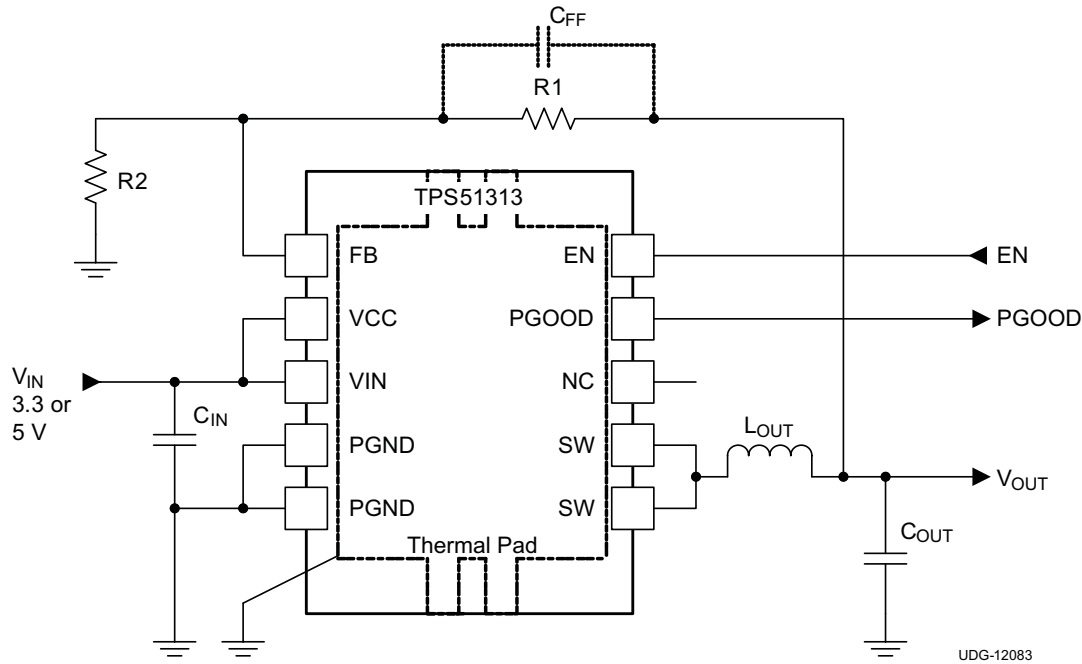
### Thermal Protection

The TPS51313 has an internal temperature sensor. When the die temperature reaches a nominal of 145°C, the device shuts down until the temperature cools by approximately 20°C. Then the converter restarts. The thermal shutdown is a non-latched behavior.

## REFERENCE DESIGN

### Application Schematic

This section describes a simplified design procedure for a discrete graphics processor PEX rail application using the TPS51313 converter. Figure 9 shows the application schematic..



**Figure 9. Reference Design Schematic**

**Table 1. Reference Design List of Materials**

FUNCTION	MANUFACTURER	PART NUMBER
Output Inductor	Vishay	IHLP-1212AB-11
Ceramic Output Capacitors	Panasonic	ECJ2FB0J226M
	Murata	GRM21BR60J226ME39L

### Design Procedure

#### Step One. Determine the specifications.

. The PEX rail requirement provides the following key paramaters.

- $V_{OUT} = 1.05\text{ V}$
- $I_{CC(max)} = 3\text{ A}$
- $\Delta I = 2\text{ A}$  (transient load step and release)
- $di/dt = 2.5\text{ A}/\mu\text{s}$

#### Step Two. Determine the system parameters.

The input voltage range and operating frequency are of primary interest. For example,

- $V_{IN} = V_{CC} = 3.3\text{ V}$
- $f_{SW} = 1\text{ MHz}$ .
- Maximum height of power chain components = 1.2 mm

### Step Three. Set the output voltage.

Use Equation 1 to determine the output voltage.

$$V_{OUT} = V_{REF} \times \frac{(R1 + R2)}{R2} \quad (1)$$

The output voltage is determined by 0.6-V voltage reference and the resistor dividers (R1 and R2). The output voltage is regulated to the FB pin. For this  $V_{OUT} = 1.05$  V, reference design, select  $R1 = 30$  k $\Omega$  and  $R2 = 40$  k $\Omega$ . (see Figure 9) To improve signal-to-noise performance of the converter, add a small feedforward capacitor (typically approximately 27 pF or less) in parallel with the upper resistor (R1).

### Step Four. Determine inductor value and choose inductor.

Smaller inductance yields better transient performance but the consequence is higher ripple and lower efficiency. Higher values have the opposite characteristics. It is common practice to limit the ripple current to 25% to 50% of the maximum current. In this case, use 40%:

$$I_{P-P} = 3 \text{ A} \times 0.4 = 1.2 \text{ A}$$

where

- $f_{SW} = 1$  MHz
- $V_{IN} = 3.3$  V
- $V_{OUT} = 1.05$  V

$$L = \frac{V \times dT}{I_{P-P}} = \left( \frac{(V_{IN} - V_{OUT})}{I_{P-P}} \right) \times \left( \frac{V_{OUT}}{(f_{SW} \times V_{IN})} \right) = 0.596 \mu\text{H} \quad (2)$$

For this application, a 0.56- $\mu\text{H}$ , 18.7-m $\Omega$  inductor from Vishay with part number IHLP-1212AB-11 is chosen. Maximum height for this inductor is 1.2 mm.

### Step Five. Determine the output capacitance.

To determine  $C_{OUT}$  based on transient and stability requirement, first calculate the minimum output capacitance for a given transient.

Equation 4 and Equation 5 calculate the minimum output capacitance for meeting the transient requirement, which is 33.8- $\mu\text{F}$  assuming a  $\pm 3\%$  voltage allowance for load step and release.

$$C_{OUT(\min\_under)} = \frac{L \times \Delta I_{LOAD(\max)}^2 \times \left( \frac{V_{VOUT} \times t_{SW}}{V_{IN(\min)}} + t_{MIN(off)} \right)}{2 \times \Delta V_{LOAD(insert)} \times \left( \left( \frac{V_{IN(\min)} - V_{VOUT}}{V_{IN(\min)}} \right) \times t_{SW} - t_{MIN(off)} \right) \times V_{VOUT}} \quad (4)$$

$$C_{OUT(\min\_over)} = \frac{L_{OUT} \times (\Delta I_{LOAD(\max)})^2}{2 \times \Delta V_{LOAD(release)} \times V_{VOUT}} \quad (5)$$

This design uses 3 22- $\mu\text{F}$  capacitors with consideration of the MLCC derating effect (60% derating for both AC and DC effect).

### Step Six. Establishing the internal compensation loop.

The TPS51313 is designed with an internal compensation loop. The internal integrator zero location is approximately 60 kHz. When the power stage double pole frequency contributed by the  $L_{OUT}$  and  $C_{OUT}$  is less than or equal to that of the zero frequency location, the converter is stable with sufficient margin.

### Step Seven. Select decoupling and peripheral components.

For TPS51313 peripheral capacitors use the following minimum value of ceramic capacitance, X5R or better temperature coefficient is recommended. Tighter tolerances and higher voltage ratings are always appropriate.

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$V_{CC}$  and  $V_{IN}$  decoupling  $\geq 2 \times 10 \mu\text{F}$ , 6.3 V

Pull up resistor on PGOOD = 100 k $\Omega$

### Step Eight. (Optional) Snubber design for optimizing maximum switch node ringing.

For TPS51313 layout design, if the maximum switch node voltage is above 8.5 V for 20 ns, snubber circuit is recommended to limit the maximum voltage to be within the absolute maximum voltage rating (see Absolute maximum rating table on page 2). A series combination of R and C (where the value of R is approximately 2.2  $\Omega$ , and the value of C is approximately 470 pF) from SW node to PGND can be added to achieve effective snubbing for SW node.

### Layout Considerations

Good layout is essential for stable power supply operation. Follow these guidelines for an efficient PCB layout.

- Widen the PGND connection area as much as possible.
- Place  $V_{IN}$ ,  $V_{CC}$  decoupling capacitors as close to the device as possible.
- Use wide traces for the VIN, SW and PGND pins. These nodes carry high current and also serve as heat sinks.
- Place FB and voltage setting dividers as close to the device as possible.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS51313DRCR</a>	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-10 to 85	S51313
TPS51313DRCR.A	Active	Production	VSON (DRC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-10 to 85	S51313
<a href="#">TPS51313DRCT</a>	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-10 to 85	S51313
TPS51313DRCT.A	Active	Production	VSON (DRC)   10	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-10 to 85	S51313

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## GENERIC PACKAGE VIEW

**DRC 10**

**VSON - 1 mm max height**

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



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## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

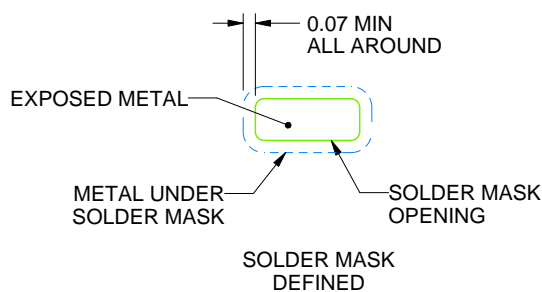
DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

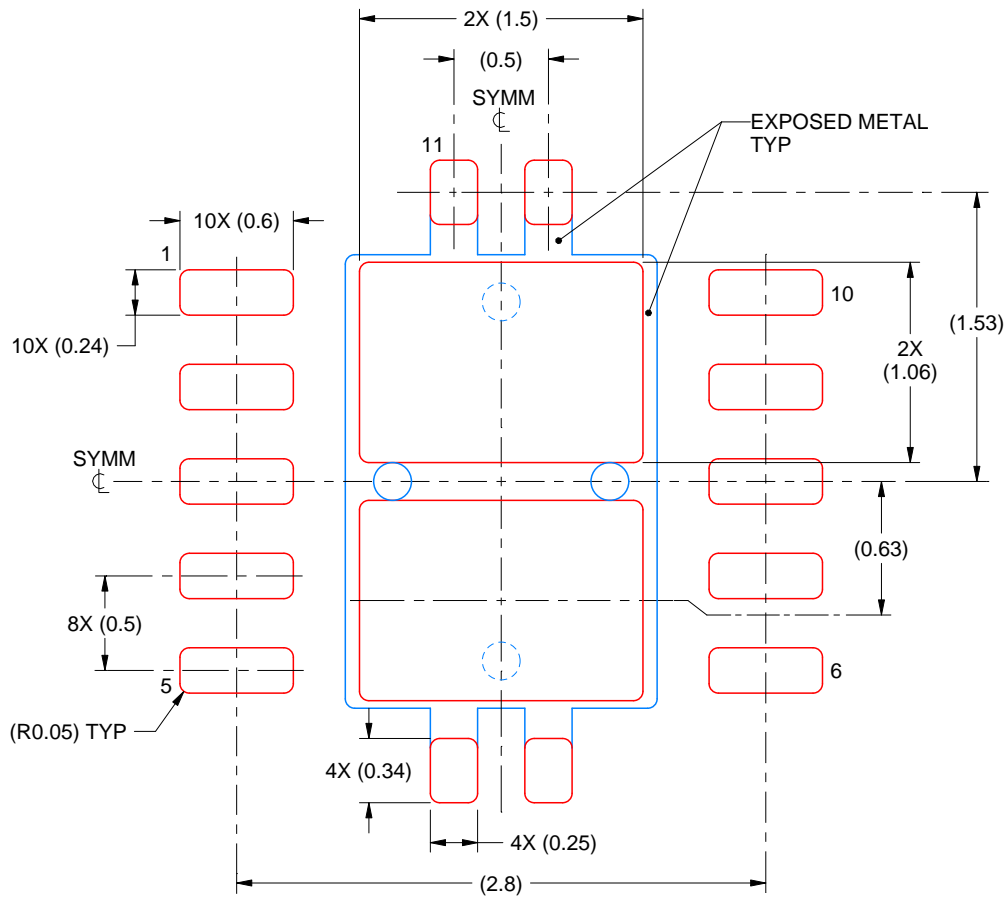


# EXAMPLE STENCIL DESIGN

DRC0010J

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:  
80% PRINTED SOLDER COVERAGE BY AREA  
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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