

TPS51116 全套 DDR、DDR2、DDR3、DDR3L、LPDDR3 和 DDR4 电源解决方案

同步降压控制器、3A LDO、缓冲基准

1 特性

- 同步降压控制器 (VDDQ)
 - 宽输入电压范围: 3.0V 至 28V
 - 负载阶跃响应为 100ns 的 D-CAP™ 模式
 - 电流模式选项支持陶瓷输出电容器
 - 支持 S4/S5 状态内的软关闭
 - 利用 $R_{DS(on)}$ 或电阻器进行电流检测
 - 2.5V (DDR)、1.8V (DDR2), 可调节至 1.5V (DDR3)、1.35V (DDR3L)、1.2V (LPDDR3 和 DDR4) 或输出范围 0.75V 至 3.0V
 - 配备有电源正常、过压保护和欠压保护
- 3A LDO (VTT), 经缓冲基准 (VREF)
 - 拉电流和灌电流的能力达到 3A
 - 提供 LDO 输入以优化功率损耗
 - 只需 20 μ F 陶瓷输出电容器
 - 经缓冲的低噪声 10mA VREF 输出
 - 针对 VREF 和 VTT 的 ± 20 mV 精度
 - 在 S3 中支持高阻抗 (high-Z), 在 S4/S5 中支持软关闭
 - 热关断

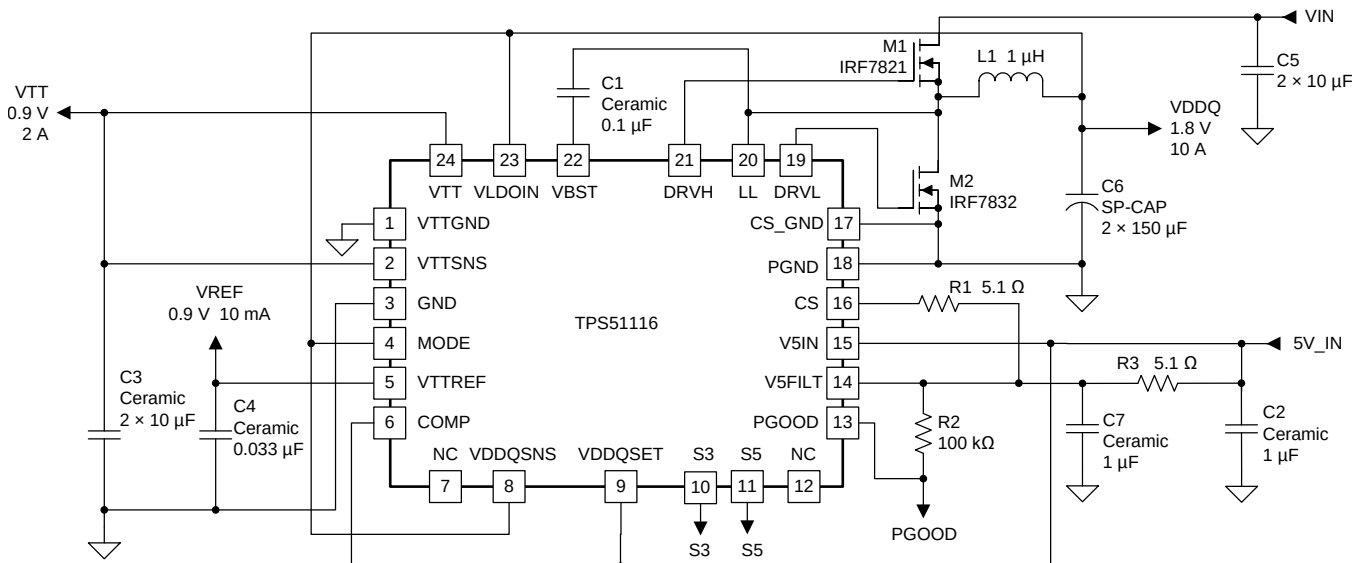
2 应用

- DDR/DDR2/DDR3/DDR3L/LPDDR3/DDR4 存储器电源
- SSTL-2、SSTL-18、SSTL-15 和 HSTL 终端

3 说明

TPS51116 提供一个用于 DDR/SSTL-2、DDR2/SSTL-18、DDR3/SSTL-15、DDR3L、LPDDR3 和 DDR4 内存系统的完整电源。它集成了一个具有 3A 拉电流/灌电流跟踪线性稳压器和经缓冲的低噪声基准的同步降压控制器。该器件在空间受限的系统中提供最低的总解决方案成本。同步控制器运行具有自适应接通时间控制的定频 400kHz、伪恒定频率脉宽调制 (PWM), 此控制可在 D-CAP 中配置™易于使用和最快瞬态响应或者电流模式以支持陶瓷输出电容器。3A 拉电流/灌电流 LDO 只需 20 μ F ($2 \times 10\mu$ F) 陶瓷输出电容器即可保持快速瞬态响应。此外, LDO 电源输入是外部可用的, 这样可大大减少总体功耗。该器件支持所有睡眠状态控制, 此类控制在 S3 (挂起到 RAM) 中将 VTT 置于 high-Z 状态并且在 S4/S5 (挂起到硬盘) 中将 VDDQ、VTT 和 VTTREF (软关闭) 放电。该器件还具有全部保护特性, 包括热关断保护, 并且提供 20 引脚 HTSSOP PowerPAD™封装和 24 引脚 4×4 QFN 封装。

4 典型应用



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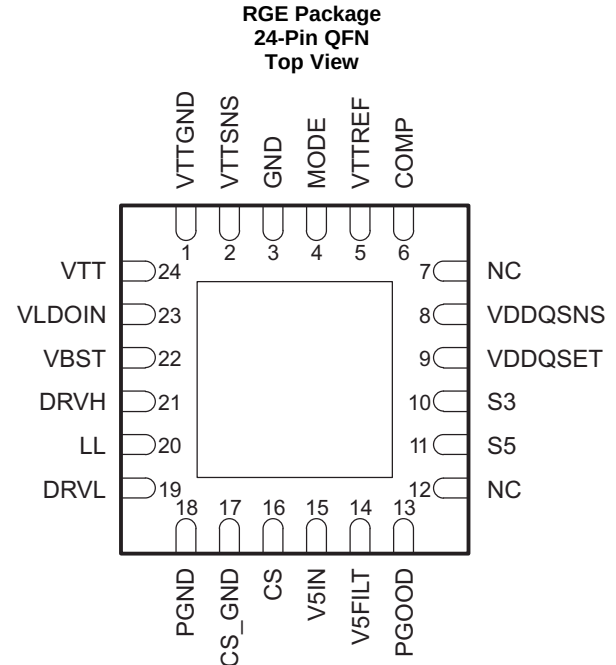
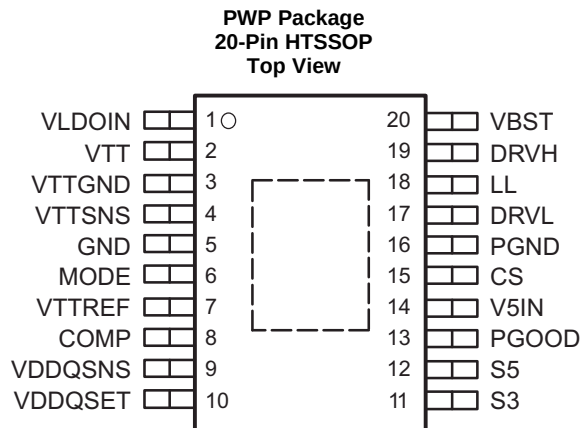
5 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision I (March 2012) to Revision J	Page
• 已添加 引脚配置和功能部分、ESD 额定值表、特性 说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	1
• 已添加 整个数据表的 DDR4 工作模式说明和规格	1
• Clarified graphs in Typical Characteristics section	9

Changes from Revision H (July 2009) to Revision I	Page
• 已添加 向 特性 部分添加了澄清说明	1
• 已添加 将"SSTL-15"添加到了 应用 部分	1
• 已添加 "LPDDR3"添加到标题和说明部分	1
• Added references to "LPDDR3 " to the Detailed Description section	19
• Added clarity to Figure 34	21

6 Pin Configuration and Functions



Pin Functions

NAME	NO.		I/O	DESCRIPTION
	PWP	RGE		
COMP	8	6	I/O	Output of the transconductance amplifier for phase compensation. Connect to V5IN pin to disable g_m amplifier and use D-CAP mode.
CS	15	16	I/O	Current sense comparator input (-) for resistor current sense scheme. Or overcurrent trip voltage setting input for $R_{DS(on)}$ current sense scheme if connected to V5IN (PWP), V5FILT (RGE) through the voltage setting resistor.
DRVH	19	21	O	Switching (high-side) MOSFET gate-drive output.
DRVH	19	21	O	Rectifying (low-side) MOSFET gate-drive output.
LL	18	20	I/O	Switching (high-side) MOSFET gate driver return. Current sense comparator input (-) for $R_{DS(on)}$ current sense.
MODE	6	4	I	Discharge mode setting pin. See <i>VDDQ and VTT Discharge Control</i> section.
NC	–	7	–	No connect.
	–	12	–	
PGND	16	18	–	Ground for rectifying (low-side) MOSFET gate driver (PWP, RGE). Also current sense comparator input(+) and ground for powergood circuit (PWP).
PGOOD	13	13	O	Powergood signal open drain output, In HIGH state when VDDQ output voltage is within the target range.
S3	11	10	I	S3 signal input.
S5	12	11	I	S5 signal input.
V5IN	14	15	I	5-V power supply input for internal circuits (PWP) and MOSFET gate drivers (PWP, RGE).
V5FILT	–	14	I	Filtered 5-V power supply input for internal circuits. Connect R-C network from V5IN to V5FILT.
VBST	20	22	I/O	Switching (high-side) MOSFET driver bootstrap voltage input.
VDDQSET	10	9	I	VDDQ output voltage setting pin. See <i>VDDQ Output Voltage Selection</i> section.
VDDQSNS	9	8	I/O	VDDQ reference input for VTT and VTTREF. Power supply for the VTTREF. Discharge current sinking terminal for VDDQ Non-tracking discharge. Output voltage feedback input for VDDQ output if VDDQSET pin is connected to V5IN or GND.
VLDOIN	1	23	I	Power supply for the VTT LDO.

Pin Functions (continued)

NAME	NO.		I/O	DESCRIPTION
	PWP	RGE		
VTT	2	24	O	Power output for the VTT LDO.
VTTGND	3	1	-	Power ground output for the VTT LDO.
VTTREF	7	5	O	VTTREF buffered reference output.
VTTSENS	4	2	I	Voltage sense input for the VTT LDO. Connect to plus terminal of the VTT LDO output capacitor.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Input voltage range	VBST	–0.3	36
		VBST wrt LL	–0.3	6
		CS, MODE, S3, S5, VTTSENS, VDDQSNS, V5IN, VLDOIN, VDDQSET, V5FILT	–0.3	6
		PGND, VTTGND, CS_GND	–0.3	0.3
V _{OUT}	Output voltage range	DRVH	–1.0	36
		LL	–1.0	30
		COMP, DRVL, PGOOD, VTT, VTTREF	–0.3	6
T _A	Operating ambient temperature range	–40	85	°C
T _{stg}	Storage temperature	–55	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V5IN, V5FILT		4.75	5.25	V
Voltage range	VBST, DRVH	–0.1	34	V
	LL	–0.6	28	
	VLDOIN, VTT, VTTSENS, VDDQSNS	–0.1	3.6	
	VTTREF	–0.1	1.8	
	PGND, VTTGND, CS_GND	–0.1	0.1	
	S3, S5, MODE, VDDQSET, CS, COMP, PGOOD, DRVL	–0.1	5.25	
Operating free-air temperature, T _A		–40	85	°C

7.4 Dissipation Ratings

PACKAGE	T _A < 25°C POWER RATING (W)	DERATING FACTOR ABOVE T _A = 25°C (mW/°C)	T _A = 85°C POWER RATING (W)
20-pin PWP	2.53	25.3	1.01
24-pin RGE	2.20	22.0	0.88

7.5 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS51116		UNIT
		PWP HTSSOP	RGE QFN	
		20	24	
R _{θJA}	Junction-to-ambient thermal resistance	41.2	35.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	27.4	41.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	23.9	12.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	1.1	07	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	23.7	12.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	3.6	3.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Electrical Characteristics

over operating free-air temperature range V_{V5IN} = 5 V, VLDOIN is connected to VDDQ output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{V5IN1}	Supply current 1, V5IN ⁽¹⁾	T _A = 25°C, No load, V _{S3} = V _{S5} = 5 V, COMP connected to capacitor		0.8	2	mA
I _{V5IN2}	Supply current 2, V5IN ⁽¹⁾	T _A = 25°C, No load, V _{S3} = 0 V, V _{S5} = 5 V, COMP connected to capacitor		300	600	μA
I _{V5IN3}	Supply current 3, V5IN ⁽¹⁾	T _A = 25°C, No load, V _{S3} = 0 V, V _{S5} = 5 V, V _{COMP} = 5 V		240	500	
I _{V5INSDN}	Shutdown current, V5IN ⁽¹⁾	T _A = 25°C, No load, V _{S3} = V _{S5} = 0 V		0.1	1.0	
I _{VLDOIN1}	Supply current 1, VLDOIN	T _A = 25°C, No load, V _{S3} = V _{S5} = 5 V		1	10	
I _{VLDOIN2}	Supply current 2, VLDOIN	T _A = 25°C, No load, V _{S3} = 5 V, V _{S5} = 0 V,		0.1	10	
I _{VLDOINSDN}	Standby current, VLDOIN	T _A = 25°C, No load, V _{S3} = V _{S5} = 0 V		0.1	1.0	
VTTREF OUTPUT						
V _{VTTREF}	Output voltage, VTTREF		V _{VDDQSNS} /2			V
V _{VTTREFTOL}	Output voltage tolerance	–10 mA < I _{VTTREF} < 10 mA, V _{VDDQSNS} = 2.5 V, Tolerance to V _{VDDQSNS} /2	–20		20	mV
		–10 mA < I _{VTTREF} < 10 mA, V _{VDDQSNS} = 1.8 V, Tolerance to V _{VDDQSNS} /2	–18		18	
		–10 mA < I _{VTTREF} < 10 mA, V _{VDDQSNS} = 1.5 V, Tolerance to V _{VDDQSNS} /2	–15		15	
		–10 mA < I _{VTTREF} < 10 mA, V _{VDDQSNS} = 1.2 V, Tolerance to V _{VDDQSNS} /2	–12		12	
V _{VTTREFSRC}	Source current	V _{VDDQSNS} = 2.5 V, V _{VTTREF} = 0 V	–20	–40	–80	mA
V _{VTTREFSNK}	Sink current	V _{VDDQSNS} = 2.5 V, V _{VTTREF} = 2.5 V	20	40	80	

(1) V5IN references to PWP packaged devices should be interpreted as V5FILT references to RGE packaged devices.

Electrical Characteristics (continued)

 over operating free-air temperature range $V_{VIN} = 5\text{ V}$, VLDOIN is connected to VDDQ output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDQ OUTPUT						
V_{VDDQ}	Output voltage, VDDQ	$T_A = 25^\circ\text{C}$, $V_{VDDQSET} = 0\text{ V}$, No load	2.465	2.500	2.535	V
		$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $V_{VDDQSET} = 0\text{ V}$, No load ⁽²⁾	2.457	2.500	2.543	
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $V_{VDDQSET} = 0\text{ V}$, No load ⁽²⁾	2.440	2.500	2.550	
		$T_A = 25^\circ\text{C}$, $V_{VDDQSET} = 5\text{ V}$, No load ⁽²⁾	1.776	1.800	1.824	
		$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $V_{VDDQSET} = 5\text{ V}$, No load ⁽²⁾	1.769	1.800	1.831	
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, $V_{VDDQSET} = 5\text{ V}$, No load ⁽²⁾	1.764	1.800	1.836	
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, Adjustable mode, No load ⁽²⁾	0.75		3.0	
$V_{VDDQSET}$	VDDQSET regulation voltage	$T_A = 25^\circ\text{C}$, Adjustable mode	742.5	750.0	757.5	mV
		$0^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, Adjustable mode	740.2	750.0	759.8	
		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$, Adjustable mode	738.0	750.0	762.0	
$R_{VDDQSNS}$	Input impedance, VDDQSNS	$V_{VDDQSET} = 0\text{ V}$		215		k Ω
		$V_{VDDQSET} = 5\text{ V}$		180		
		Adjustable mode		460		
$I_{VDDQSET}$	Input current, VDDQSET	$V_{VDDQSET} = 0.78\text{ V}$, COMP = Open		–0.04		μA
		$V_{VDDQSET} = 0.78\text{ V}$, COMP = 5 V		–0.06		
$I_{VDDQDisch}$	Discharge current, VDDQ	$V_{S3} = V_{S5} = 0\text{ V}$, $V_{VDDQSNS} = 0.5\text{ V}$, $V_{MODE} = 0\text{ V}$	10	40		mA
$I_{VLDOINDisch}$	Discharge current, VLDOIN	$V_{S3} = V_{S5} = 0\text{ V}$, $V_{VDDQSNS} = 0.5\text{ V}$, $V_{MODE} = 0.5\text{ V}$		700		mA
VTT OUTPUT						
V_{VTTNS}	Output voltage, VTT	$V_{S3} = V_{S5} = 5\text{ V}$, $V_{VLDOIN} = V_{VDDQSNS} = 2.5\text{ V}$		1.25		V
		$V_{S3} = V_{S5} = 5\text{ V}$, $V_{VLDOIN} = V_{VDDQSNS} = 1.8\text{ V}$		0.9		
		$V_{S3} = V_{S5} = 5\text{ V}$, $V_{VLDOIN} = V_{VDDQSNS} = 1.5\text{ V}$		0.75		
$V_{VTTOL25}$	VTT output voltage tolerance to VTTREF	$V_{VDDQSNS} = V_{VLDOIN} = 2.5\text{ V}$, $V_{S3} = V_{S5} = 5\text{ V}$, $I_{VTT} = 0\text{ A}$	–20		20	mV
		$V_{VDDQSNS} = V_{VLDOIN} = 2.5\text{ V}$, $V_{S3} = V_{S5} = 5\text{ V}$, $ I_{VTT} < 1.5\text{ A}$	–30		30	
		$V_{VDDQSNS} = V_{VLDOIN} = 2.5\text{ V}$, $V_{S3} = V_{S5} = 5\text{ V}$, $ I_{VTT} < 3\text{ A}$	–40		40	
$V_{VTTOL18}$	VTT output voltage tolerance to VTTREF	$V_{VDDQSNS} = V_{VLDOIN} = 1.8\text{ V}$, $V_{S3} = V_{S5} = 5\text{ V}$, $I_{VTT} = 0\text{ A}$	–20		20	mV
		$V_{VDDQSNS} = V_{VLDOIN} = 1.8\text{ V}$, $V_{S3} = V_{S5} = 5\text{ V}$, $ I_{VTT} < 1\text{ A}$	–30		30	
		$V_{VDDQSNS} = V_{VLDOIN} = 1.8\text{ V}$, $V_{S3} = V_{S5} = 5\text{ V}$, $ I_{VTT} < 2\text{ A}$	–40		40	
$V_{VTTOL15}$	VTT output voltage tolerance to VTTREF	$V_{VDDQSNS} = V_{VLDOIN} = 1.5\text{ V}$, $V_{S3} = V_{S5} = 5\text{ V}$, $I_{VTT} = 0\text{ A}$	–20		20	mV
		$V_{VDDQSNS} = V_{VLDOIN} = 1.5\text{ V}$, $V_{S3} = V_{S5} = 5\text{ V}$, $ I_{VTT} < 1\text{ A}$	–30		30	
		$V_{VDDQSNS} = V_{VLDOIN} = 1.5\text{ V}$, $V_{S3} = V_{S5} = 5\text{ V}$, $ I_{VTT} < 2\text{ A}$	–40		40	

(2) Specified by design. Not production tested.

Electrical Characteristics (continued)

over operating free-air temperature range $V_{VIN} = 5\text{ V}$, VLDOIN is connected to VDDQ output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{VTTTOL12}	VTT output voltage tolerance to VTTREF	V _{VDDQSNS} = V _{VLDOIN} = 1.2 V, V _{S3} = V _{S5} = 5 V, I _{VTT} = 0 A	−20		20	mV
		V _{VDDQSNS} = V _{VLDOIN} = 1.2 V, V _{S3} = V _{S5} = 5 V, I _{VTT} < 1 A	−30		30	
		V _{VDDQSNS} = V _{VLDOIN} = 1.2 V, V _{S3} = V _{S5} = 5 V, I _{VTT} < 1.5 A	−40		40	
I _{VTTOCLSRC}	Source current limit, VTT	V _{VLDOIN} = V _{VDDQSNS} = 2.5 V, V _{VTT} = V _{VTTSNS} = 1.19 V, PGOOD = HI	3.0	3.8	6.0	A
		V _{VLDOIN} = V _{VDDQSNS} = 2.5 V, V _{VTT} = 0 V	1.5	2.2	3.0	
I _{VTTOCLSNK}	Sink current limit, VTT	V _{VLDOIN} = V _{VDDQSNS} = 2.5 V, V _{VTT} = V _{VTTSNS} = 1.31 V, PGOOD = HI	3.0	3.6	6.0	
		V _{VLDOIN} = V _{VDDQSNS} = 2.5 V, V _{VTT} = V _{VDDQ}	1.5	2.2	3.0	
I _{VTTLK}	Leakage current, VTT	V _{S3} = 0 V, V _{S5} = 5 V, V _{VTT} = V _{VDDQSNS} /2	−10		10	μA
I _{VTTBIAS}	Input bias current, VTTSNS	V _{S3} = 5 V, V _{VTTSNS} = V _{VDDQSNS} /2	−1	−0.1	1	
I _{VTTNSLK}	Leakage current, VTTSNS	V _{S3} = 0 V, V _{S5} = 5 V, V _{VTT} = V _{VDDQSNS} /2	−1		1	
I _{VTTDisch}	Discharge current, VTT	T _A = 25°C, V _{S3} = V _{S5} = V _{VDDQSNS} = 0 V, V _{VTT} = 0.5 V	10	17		mA
TRANSCONDUCTANCE AMPLIFIER						
gm	Gain	T _A = 25°C	240	300	360	μS
I _{COMPSNK}	COMP maximum sink current	V _{S3} = 0 V, V _{S5} = 5 V, V _{VDDQSET} = 0 V, V _{VDDQSNS} = 2.7 V, V _{COMP} = 1.28 V		13		μA
I _{COMPSRC}	COMP maximum source current	V _{S3} = 0 V, V _{S5} = 5 V, V _{VDDQSET} = 0 V, V _{VDDQSNS} = 2.3 V, V _{COMP} = 1.28 V		−13		
V _{COMPHI}	COMP high clamp voltage	V _{S3} = 0 V, V _{S5} = 5 V, V _{VDDQSET} = 0 V, V _{VDDQSNS} = 2.3 V, V _{CS} = 0 V	1.31	1.34	1.37	V
V _{COMPLO}	COMP low clamp voltage	V _{S3} = 0 V, V _{S5} = 5 V, V _{VDDQSET} = 0 V, V _{VDDQSNS} = 2.7 V, V _{CS} = 0 V	1.18	1.21	1.24	
DUTY CONTROL						
t _{ON}	Operating on-time	V _{IN} = 12 V, V _{VDDQSET} = 0 V		520		ns
t _{ON0}	Startup on-time	V _{IN} = 12 V, V _{VDDQSNS} = 0 V		125		
t _{ON(min)}	Minimum on-time	T _A = 25°C ⁽²⁾		100		
t _{OFF(min)}	Minimum off-time	T _A = 25°C ⁽²⁾		350		
ZERO CURRENT COMPARATOR						
V _{ZC}	Zero current comparator offset		−6	0	6	mV
OUTPUT DRIVERS						
R _{DRVH}	DRVH resistance	Source, I _{DRVH} = −100 mA		3	6	Ω
		Sink, I _{DRVH} = 100 mA		0.9	3	
R _{DRVL}	DRVL resistance	Source, I _{DRVL} = −100 mA		3	6	
		Sink, I _{DRVL} = 100 mA		0.9	3	
t _D	Dead time	LL-low to DRVL-on ⁽²⁾		10		ns
		DRVL-off to DRVH-on ⁽²⁾		20		
INTERNAL BST DIODE						
V _{FBST}	Forward voltage	V _{V5IN-VBST} , I _F = 10 mA, T _A = 25°C	0.7	0.8	0.9	V
I _{VBSTLK}	VBST leakage current	V _{VBST} = 34 V, V _{LL} = 28 V, V _{VDDQ} = 2.6 V, T _A = 25°C		0.1	1.0	μA

Electrical Characteristics (continued)

over operating free-air temperature range $V_{VIN} = 5\text{ V}$, VLDOIN is connected to VDDQ output (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTIONS						
V _{OCL}	Current limit threshold	V _{PGND-CS} , PGOOD = HI, V _{CS} < 0.5 V	50	60	70	mV
		V _{PGND-CS} , PGOOD = LO, V _{CS} < 0.5 V	20	30	40	
I _{TRIP}	Current sense sink current	T _A = 25°C, V _{CS} > 4.5 V, PGOOD = HI	9	10	11	μA
		T _A = 25°C, V _{CS} > 4.5 V, PGOOD = LO	4	5	6	
TC _{ITRIP}	TRIP current temperature coefficient	R _{DS(on)} sense scheme, On the basis of T _A = 25°C ⁽²⁾	4500			ppm/°C
V _{OCL(off)}	Overcurrent protection COMP offset	(V _{V5IN-CS} - V _{PGND-LL}), V _{V5IN-CS} = 60 mV, V _{CS} > 4.5 V ⁽²⁾	–5	0	5	mV
V _{R(trip)}	Current limit threshold setting range	V _{V5IN-CS} ⁽²⁾ (1)	30	150		
POWERGOOD COMPARATOR						
V _{TVDDQPG}	VDDQ powergood threshold	PG in from lower	92.5%	95.0%	97.5%	
		PG in from higher	102.5%	105.0%	107.5%	
		PG hysteresis	5%			
I _{PG(max)}	PGOOD sink current	V _{VTT} = 0 V, V _{PGOOD} = 0.5 V	2.5	7.5	mA	
t _{PG(del)}	PGOOD delay time	Delay for PG in	80	130	200	μs
UNDERVOLTAGE LOCKOUT/LOGIC THRESHOLD						
V _{UVV5IN}	V5IN UVLO threshold voltage	Wake up	3.7	4.0	4.3	V
		Hysteresis	0.2	0.3	0.4	
V _{THMODE}	MODE threshold	No discharge	4.7			
		Non-tracking discharge	0.1			
V _{THVDDQSET}	VDDQSET threshold voltage	2.5 V output	0.08	0.15	0.25	
		1.8 V output	3.5	4.0	4.5	
V _{IH}	High-level input voltage	S3, S5	2.2			
V _{IL}	Low-level input voltage	S3, S5			0.3	
V _{IHYST}	Hysteresis voltage	S3, S5	0.2			
V _{INLEAK}	Logic input leakage current	S3, S5, MODE	–1	1		
V _{INVDDQSET}	Input leakage/ bias current	VDDQSET	–1	1		
UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V _{OVP}	VDDQ OVP trip threshold voltage	OVP detect	110%	115%	120%	
		Hysteresis	5%			
t _{OVPDEL}	VDDQ OVP propagation delay ⁽²⁾		1.5			μs
V _{UVP}	Output UVP trip threshold	UVP detect	70%			
		Hysteresis	10%			
t _{UVPDEL}	Output UVP propagation delay ⁽²⁾		32			cycle
t _{UVPEN}	Output UVP enable delay ⁽²⁾		1007			
THERMAL SHUTDOWN						
T _{SDN}	Thermal SDN threshold ⁽²⁾	Shutdown temperature	160			°C
		Hysteresis	10			

7.7 Typical Characteristics

All data in the following graphs are measured from the PWP packaged device.

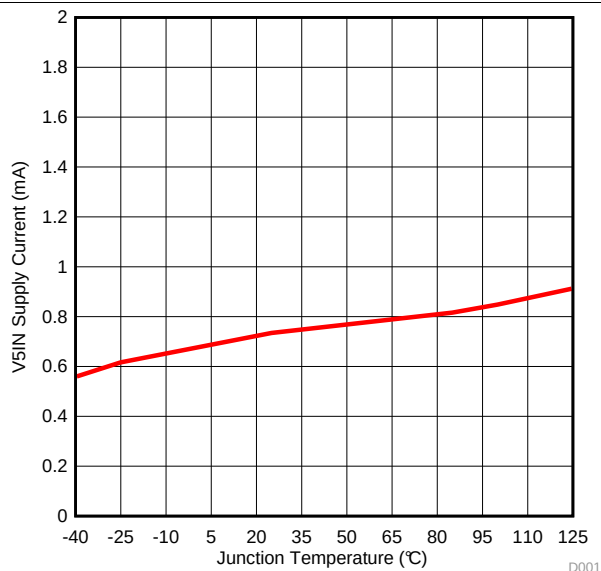


Figure 1. V5IN Supply Current vs Junction Temperature

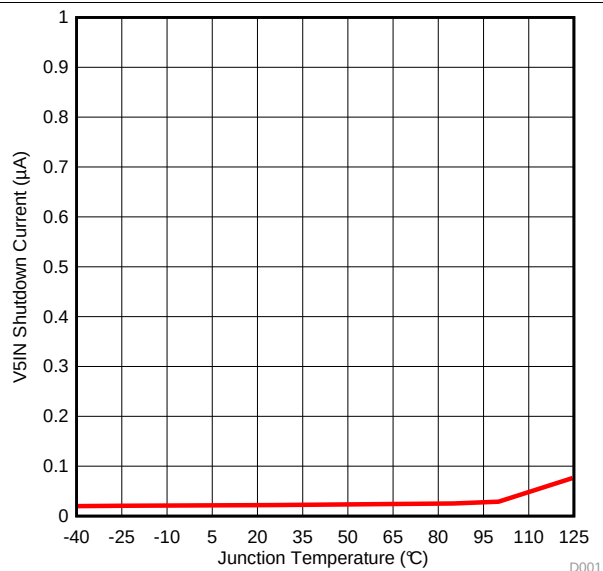
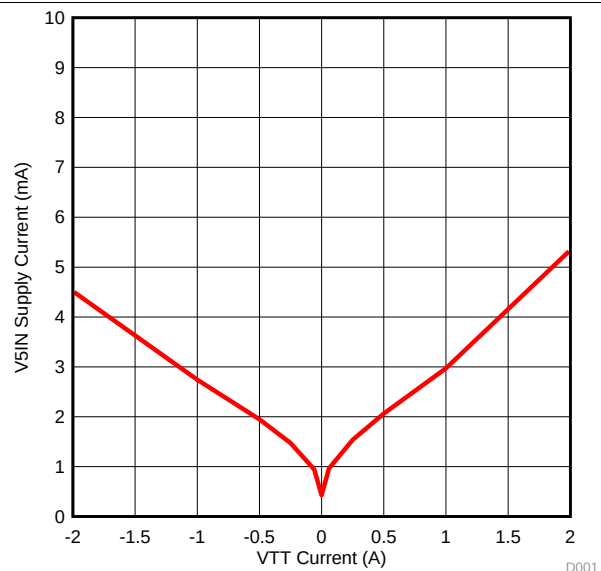


Figure 2. V5IN Shutdown Current vs Junction Temperature



DDR2

$V_{VTT} = 0.3 \text{ V}$

Figure 3. V5IN Supply Current vs VTT Current

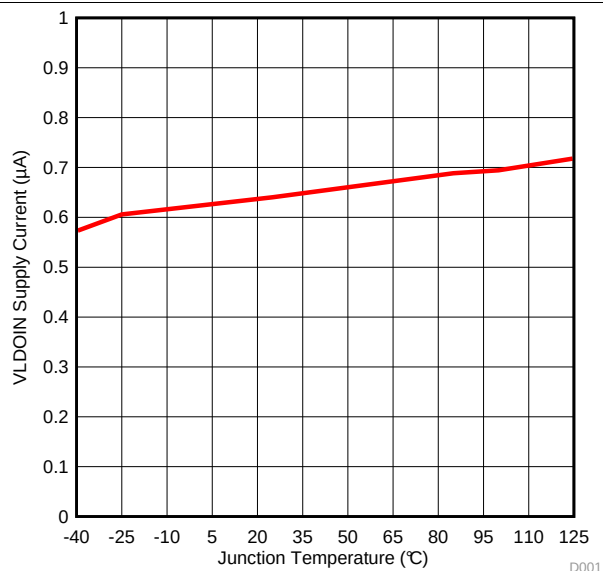


Figure 4. VLDOIN Supply Current vs Junction Temperature

Typical Characteristics (continued)

All data in the following graphs are measured from the PWP packaged device.

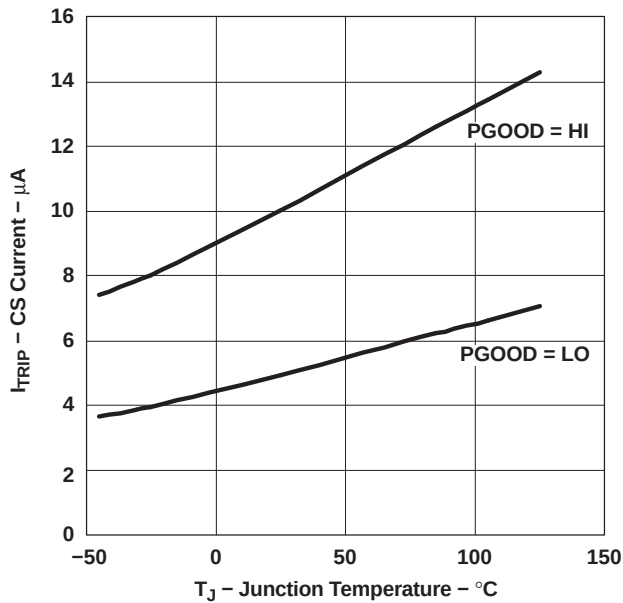


Figure 5. CS Current vs Junction Temperature

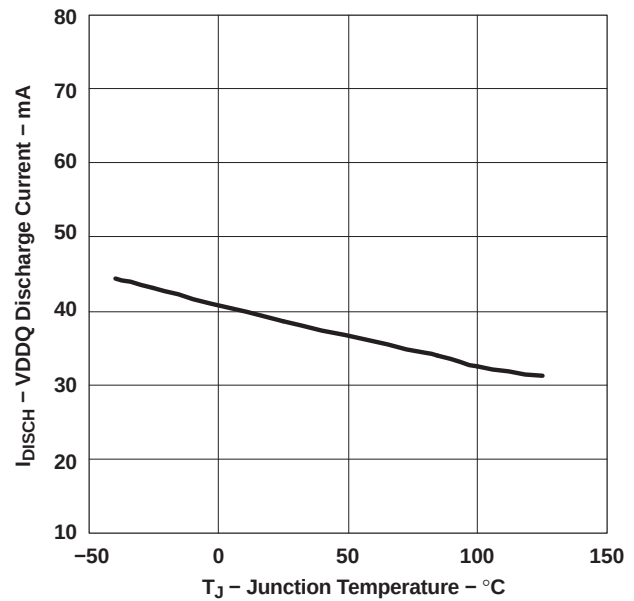


Figure 6. VDDQ Discharge Current vs Junction Temperature

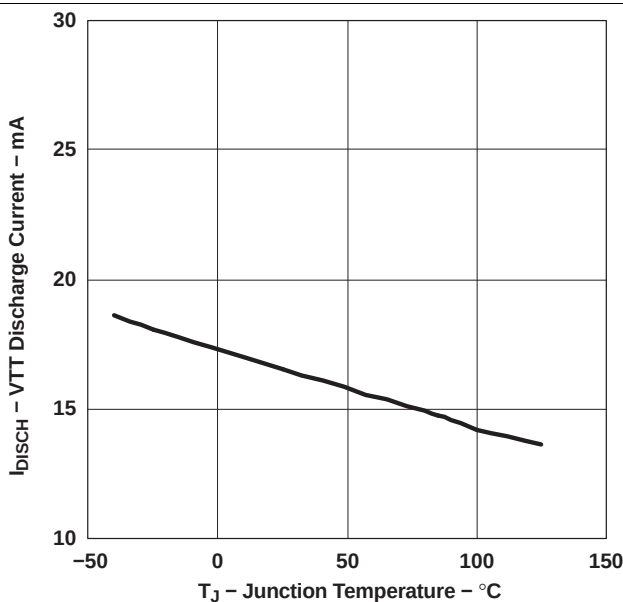


Figure 7. VTT Discharge Current vs Junction Temperature

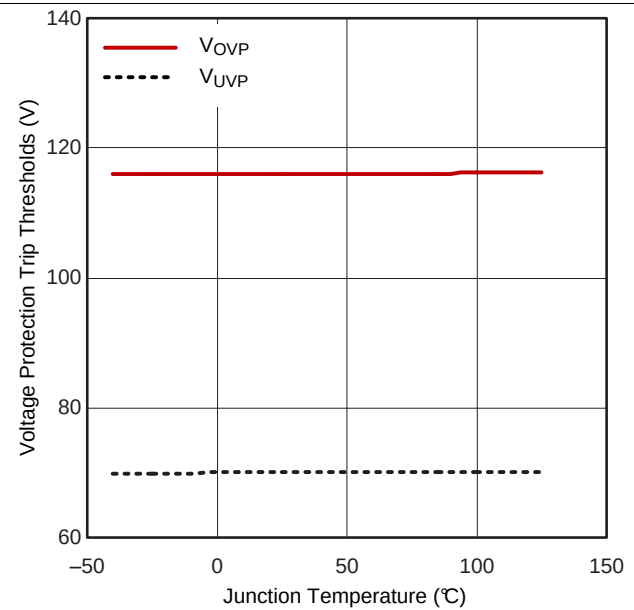


Figure 8. Overvoltage and Undervoltage Threshold vs Junction Temperature

Typical Characteristics (continued)

All data in the following graphs are measured from the PWP packaged device.

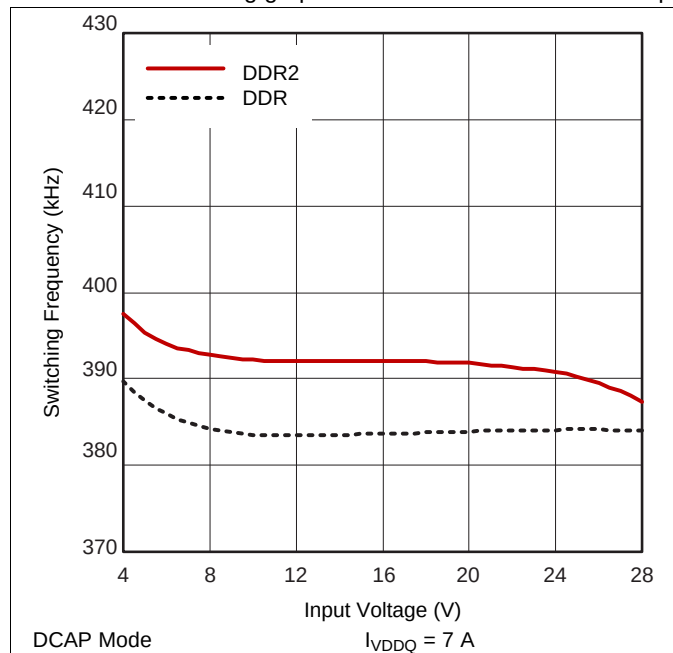


Figure 9. Switching Frequency vs Input Voltage

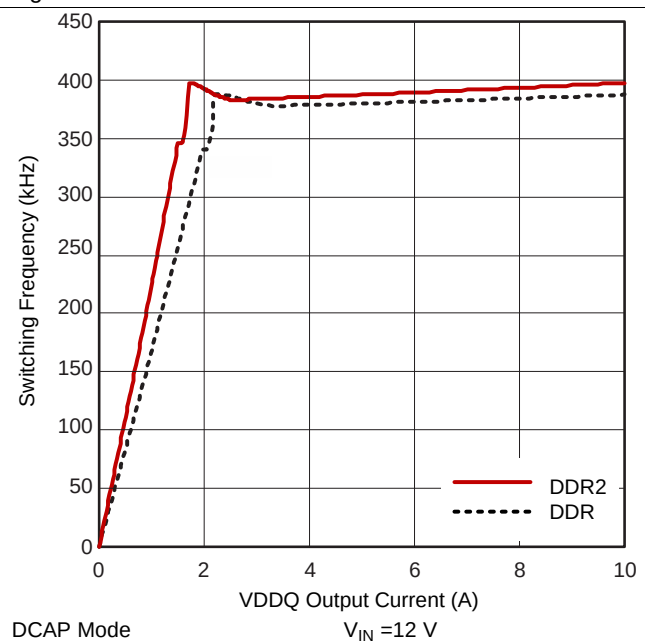


Figure 10. Switching Frequency vs I_{VDDQ} Output Current

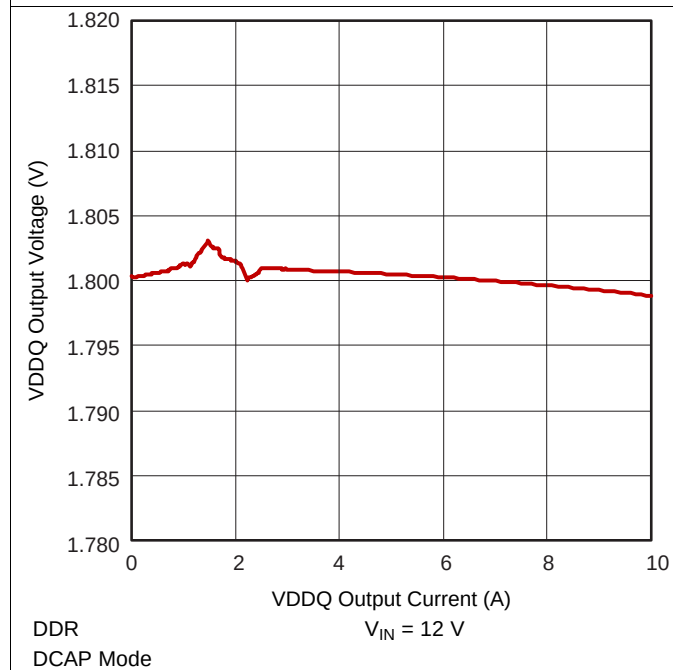


Figure 11. VDDQ Load Regulation

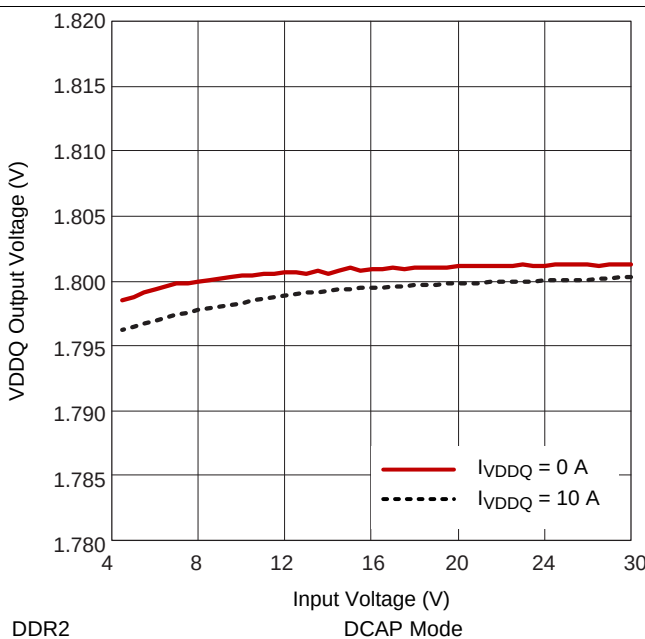


Figure 12. VDDQ Line Regulation

Typical Characteristics (continued)

All data in the following graphs are measured from the PWP packaged device.

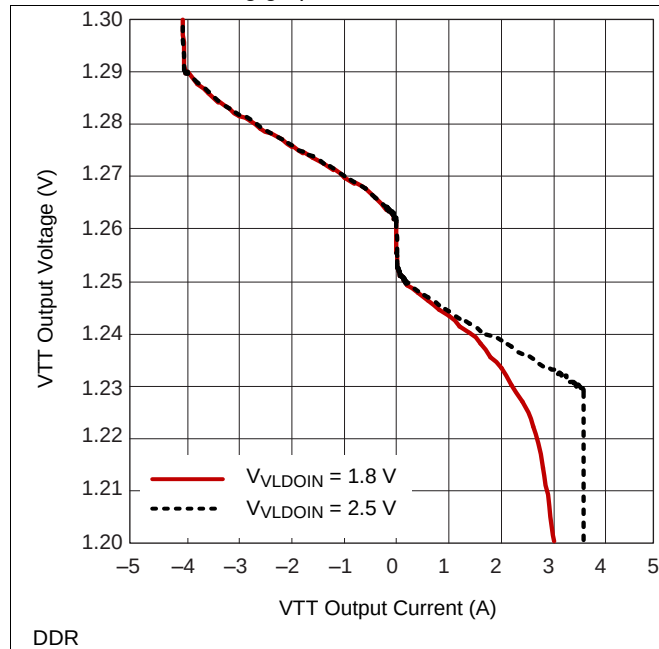


Figure 13. VTT Load Regulation

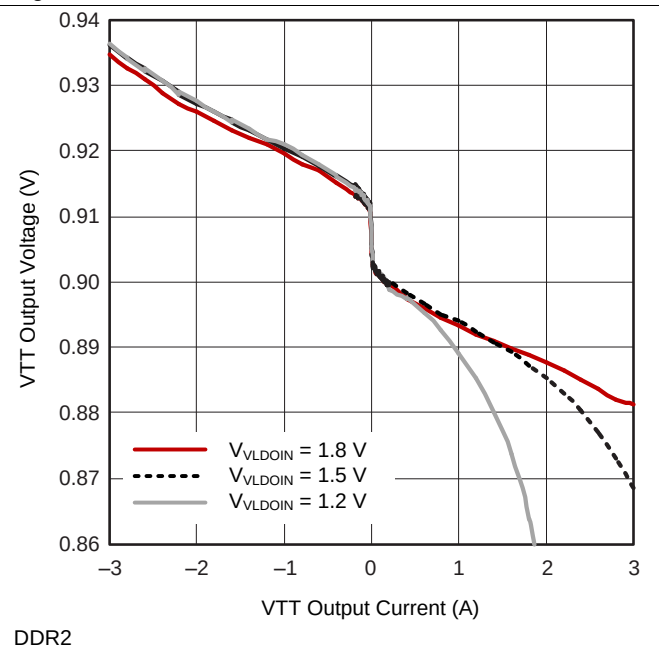


Figure 14. VTT Load Regulation

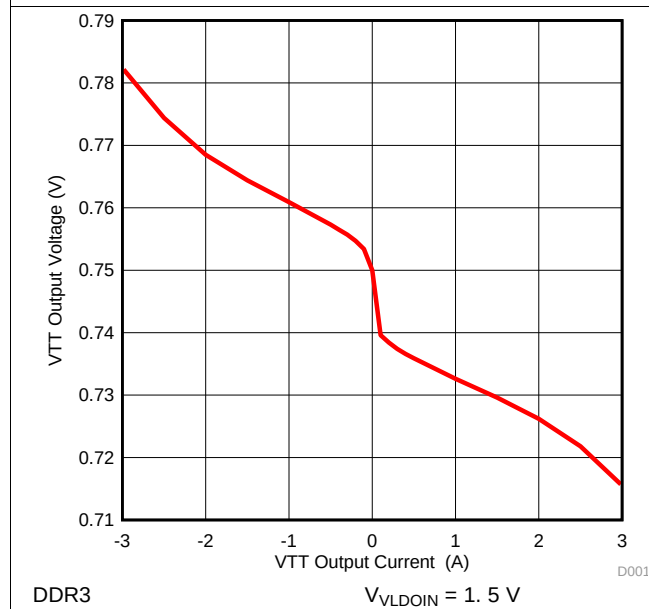


Figure 15. VTT Load Regulation

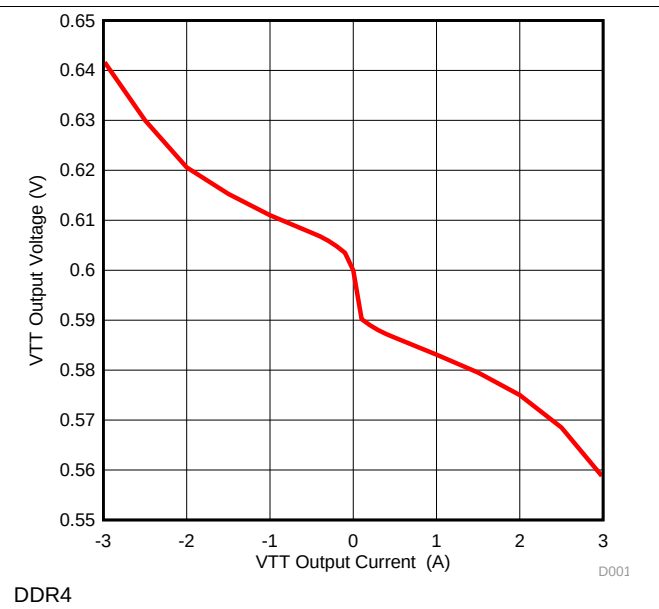


Figure 16. VTTREF Output Voltage vs Output Current

Typical Characteristics (continued)

All data in the following graphs are measured from the PWP packaged device.

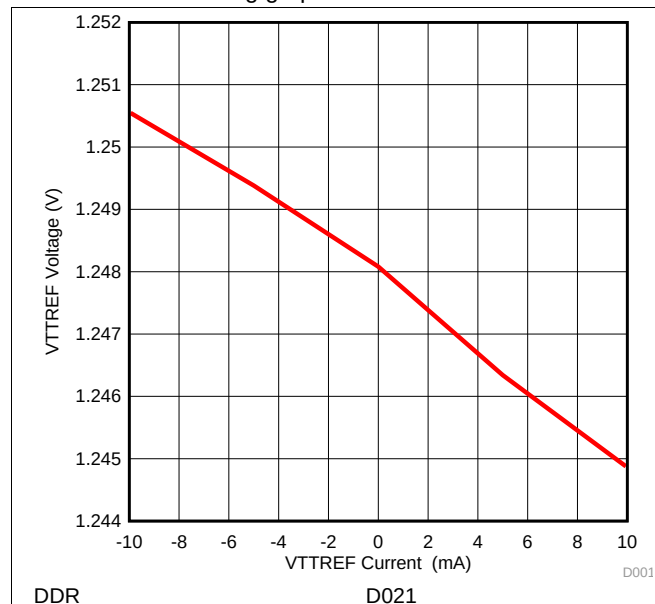


Figure 17. VTTREF Load Regulation

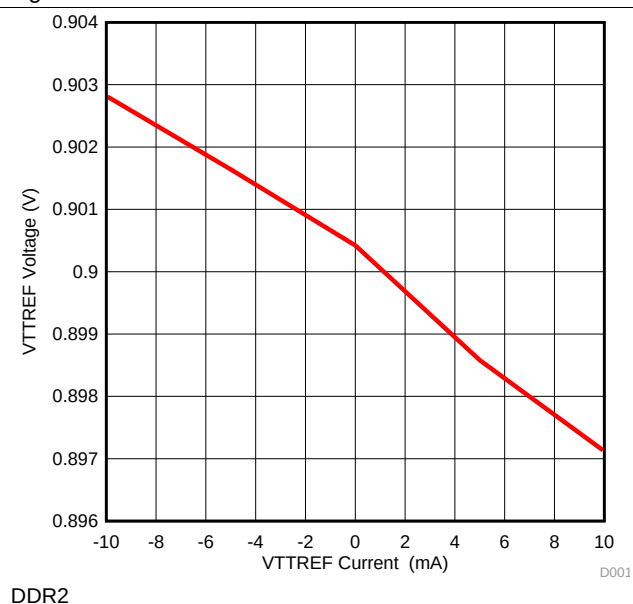


Figure 18. VTTREF Load Regulation

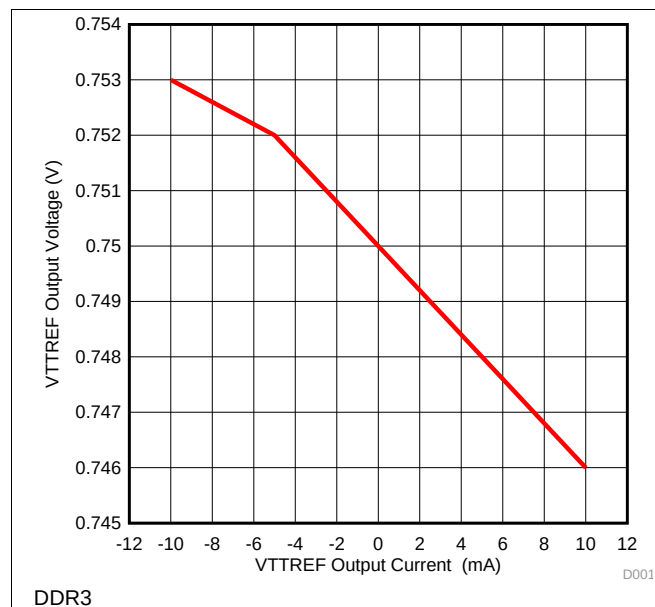


Figure 19. VTTREF Load Regulation

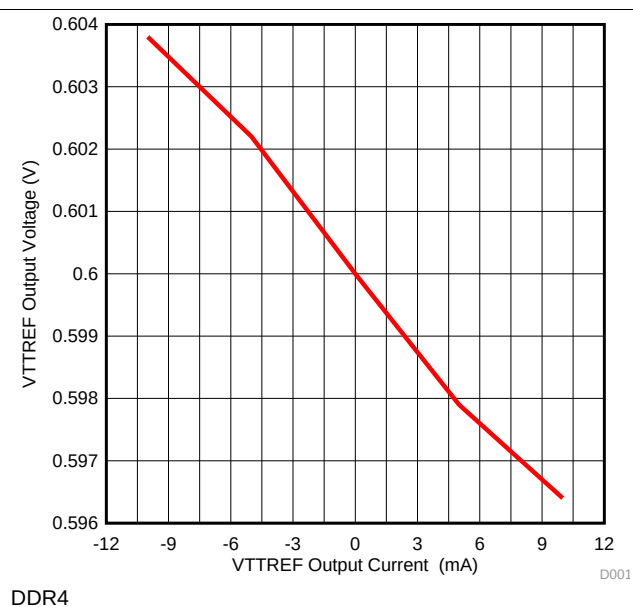


Figure 20. VTTREF Load Regulation

Typical Characteristics (continued)

All data in the following graphs are measured from the PWP packaged device.

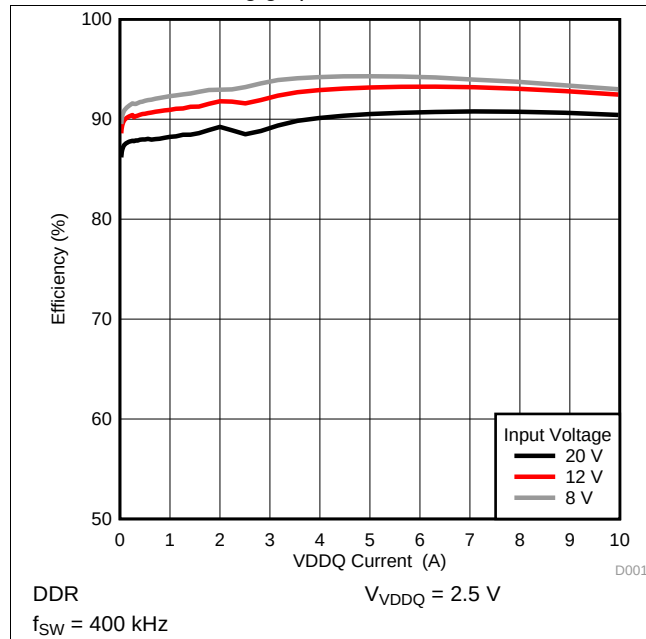


Figure 21. VDDQ Efficiency vs VDDQ Current

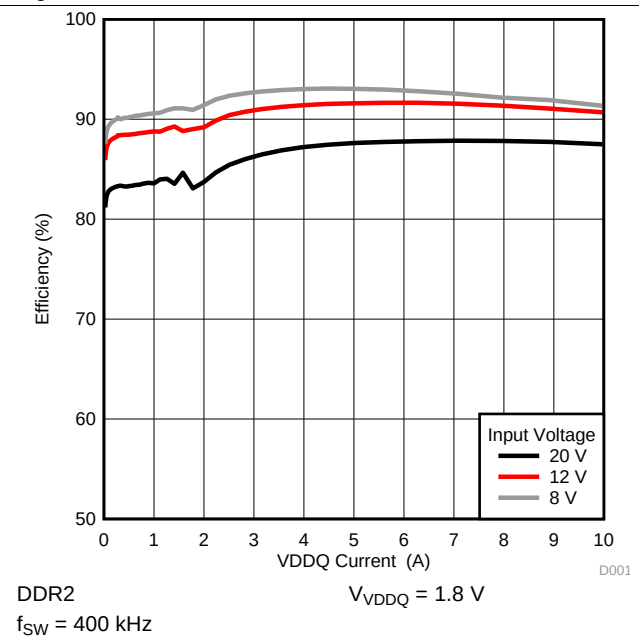


Figure 22. VDDQ Efficiency vs VDDQ Current

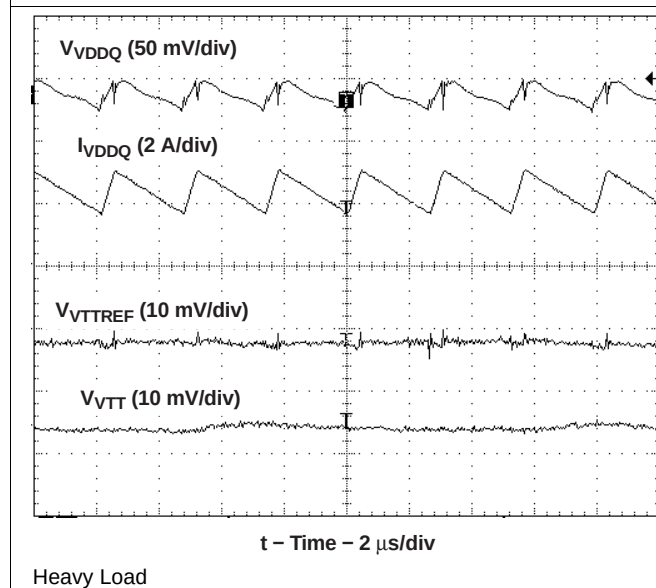


Figure 23. Ripple Waveforms

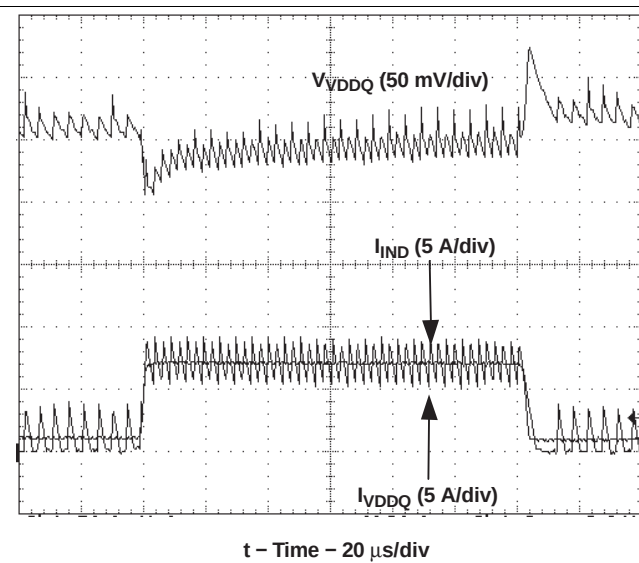
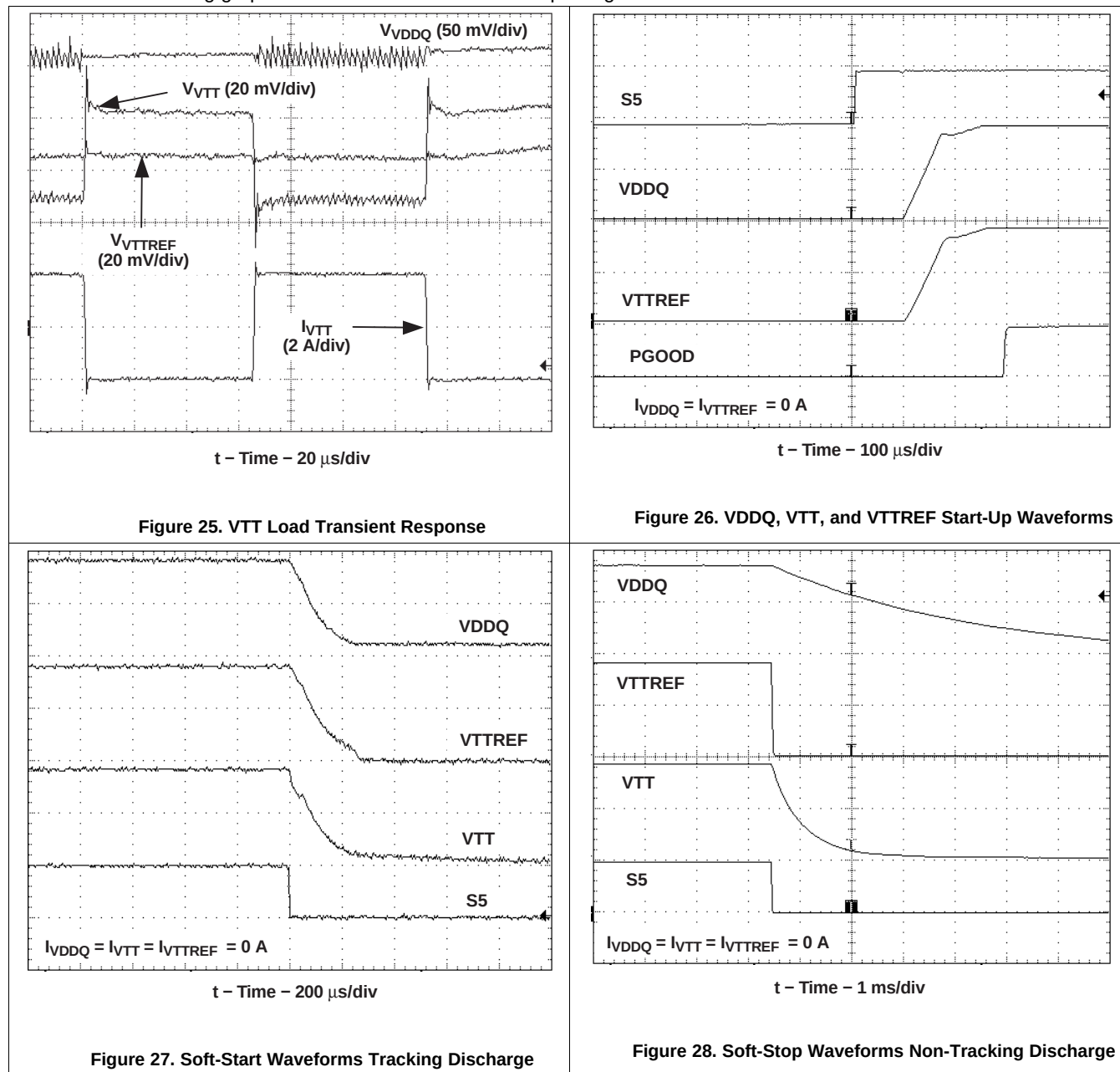


Figure 24. VDDQ Load Transient Response

Typical Characteristics (continued)

All data in the following graphs are measured from the PWP packaged device.



Typical Characteristics (continued)

All data in the following graphs are measured from the PWP packaged device.

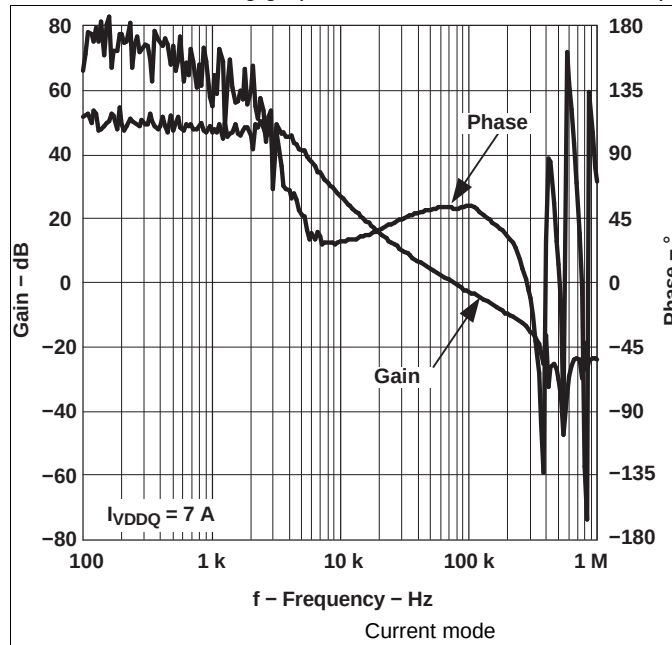


Figure 29. VDDQ Bode Plot

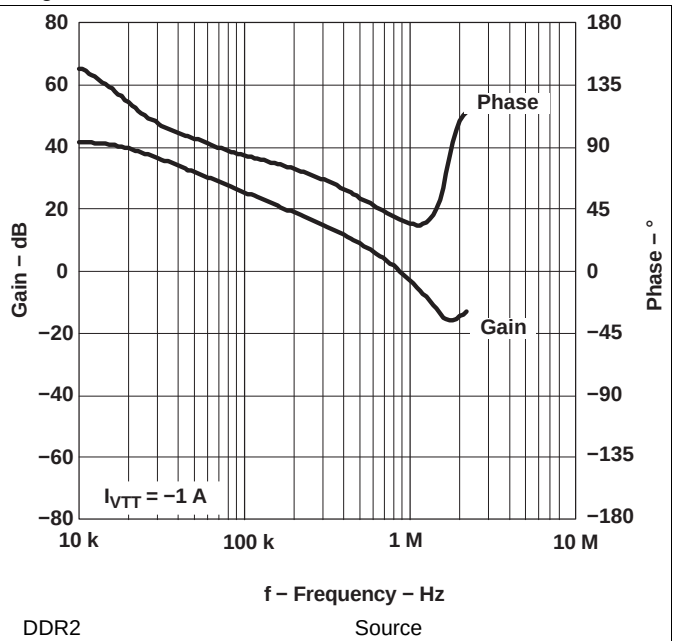


Figure 30. VTT Bode Plot

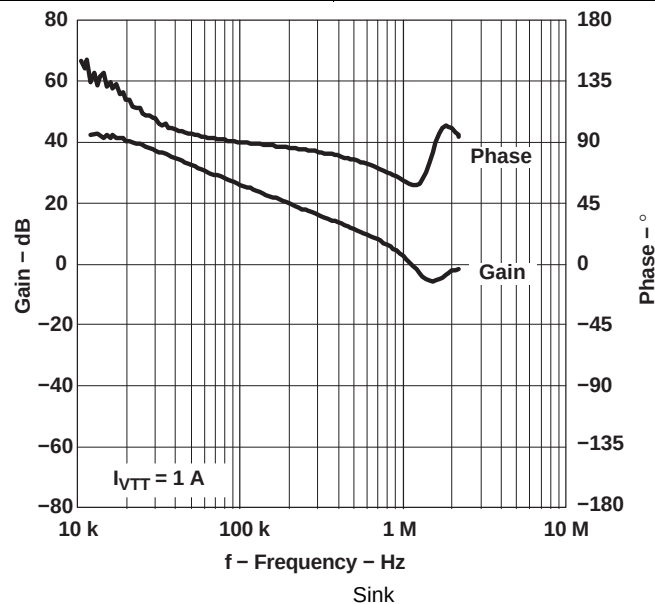


Figure 31. VTT Bode Plot

8 Detailed Description

8.1 Overview

8.2 Functional Block Diagram

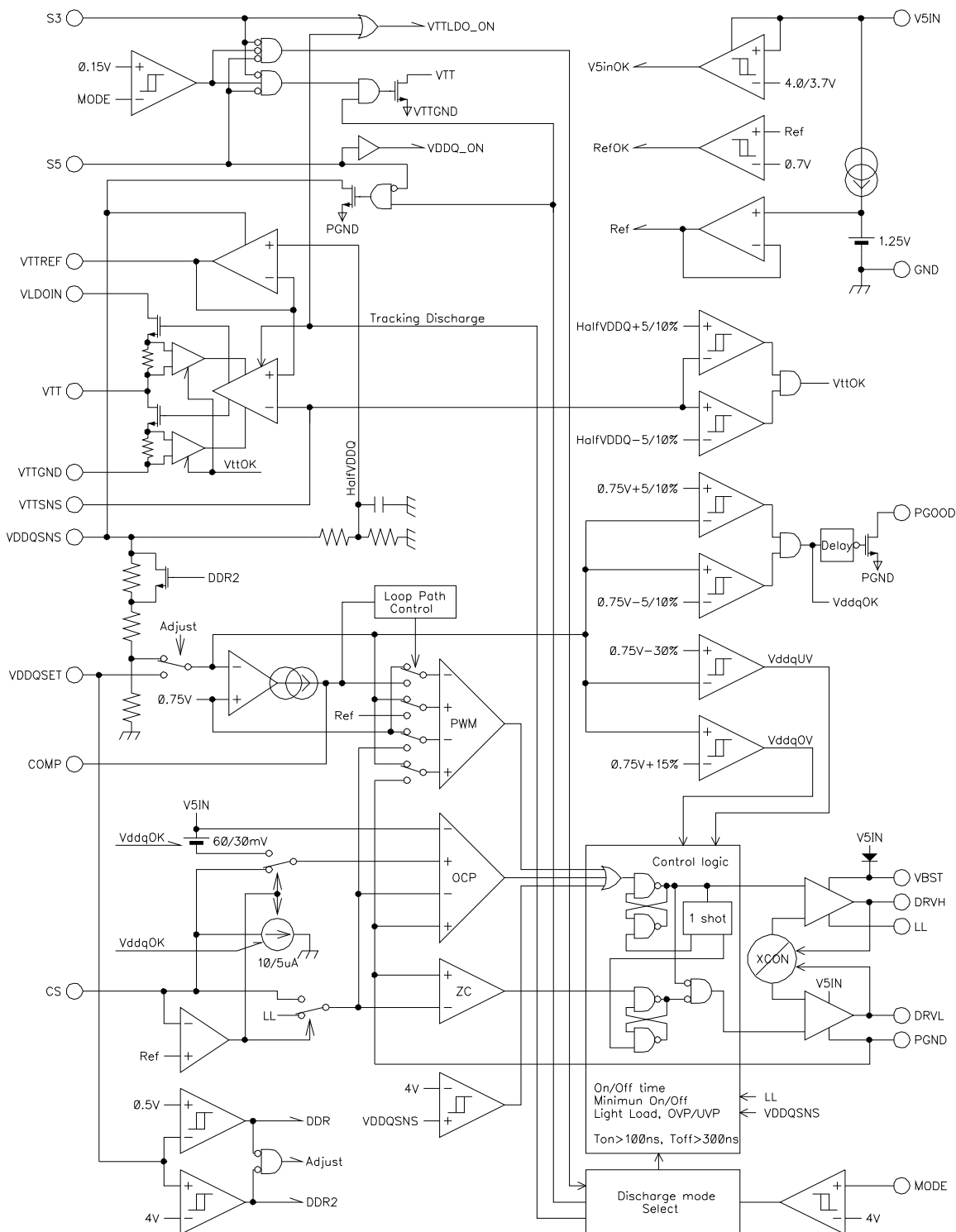
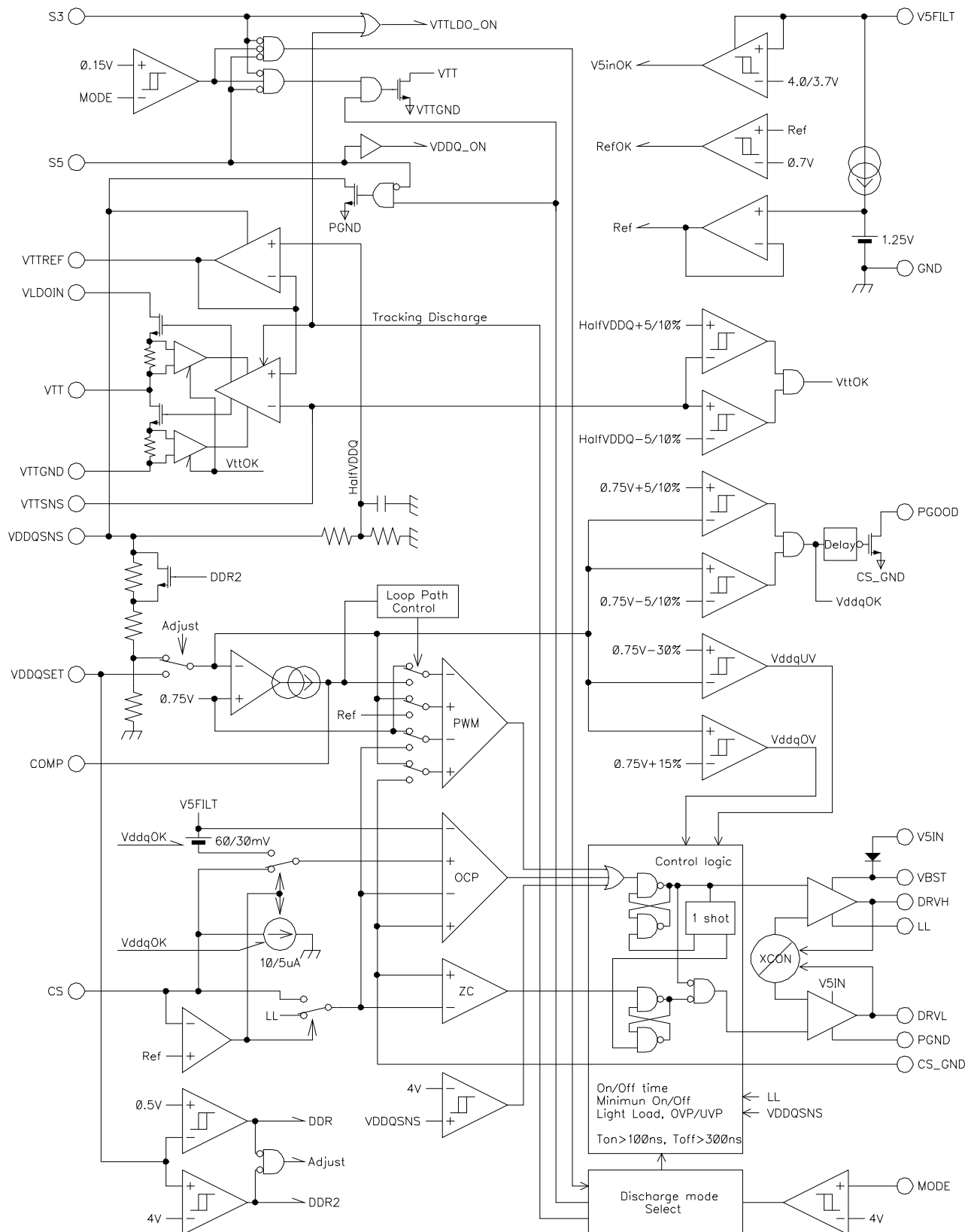


Figure 32. PWP Package

Functional Block Diagram (continued)

Figure 33. RGE Package

8.3 Feature Description

The TPS51116 is an integrated power management solution which combines a synchronous buck controller, a 10-mA buffered reference and a high-current sink/source low-dropout linear regulator (LDO) in a small 20-pin HTSSOP package or a 24-pin QFN package. Each of these rails generates VDDQ, VTTREF and VTT that required with DDR/DDR2/DDR3/DDR3L/LPDDR3/DDR4 memory systems. The switch mode power supply (SMPS) portion employs external N-channel MOSFETs to support high current for DDR/DDR2/DDR3/LPDDR3/DDR4 memory VDD/VDDQ. The preset output voltage is selectable from 2.5 V or 1.8 V. User-defined output voltage is also possible and can be adjustable from 0.75 V to 3 V. Input voltage range of the SMPS is 3 V to 28 V. The SMPS runs an adaptive on-time PWM operation at high-load condition and automatically reduces frequency to keep excellent efficiency down to several mA. Current sensing scheme uses either $R_{DS(on)}$ of the external rectifying MOSFET for a low-cost, loss-less solution, or an optional sense resistor placed in series to the rectifying MOSFET for more accurate current limit. The output of the switcher is sensed by VDDQSNS pin to generate one-half VDDQ for the 10-mA buffered reference (VTTREF) and the VTT active termination supply. The VTT LDO can source and sink up to 3-A peak current with only 20- μ F (two 10- μ F in parallel) ceramic output capacitors. VTTREF tracks VDDQ/2 within $\pm 1\%$ of VDDQ. VTT output tracks VTTREF within ± 20 mV at no load condition while ± 40 mV at full load. The LDO input can be separated from VDDQ and optionally connected to a lower voltage by using VLDOIN pin. This helps reducing power dissipation in sourcing phase. The TPS51116 is fully compatible to JEDEC DDR/DDR2 specifications at S3/S5 sleep state (see Table 2). The device offers two output discharge function alternatives when both VTT and VDDQ are disabled. The tracking discharge mode discharges VDDQ and VTT outputs through the internal LDO transistors and then VTT output tracks half of VDDQ voltage during discharge. The non-tracking discharge mode discharges outputs using internal discharge MOSFETs which are connected to VDDQSNS and VTT. The current capability of these discharge FETs are limited and discharge occurs more slowly than the tracking discharge. These discharge functions can be disabled by selecting non-discharge mode.

8.3.1 VDDQ SMPS, Light Load Condition

TPS51116 automatically reduces switching frequency at light load condition to maintain high efficiency. This reduction of frequency is achieved smoothly and without increase of V_{OUT} ripple or load regulation. Detail operation is described as follows. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to the point that its valley touches zero current, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when this zero inductor current is detected. As the load current further decreased, the converter runs in discontinuous conduction mode and it takes longer and longer to discharge the output capacitor to the level that requires next ON cycle. The ON-time is kept the same as that in the heavy load condition. In reverse, when the output current increase from light load to heavy load, switching frequency increases to the constant 400 kHz as the inductor current reaches to the continuous conduction. The transition load point to the light load operation $I_{OUT(LL)}$ (i.e. the threshold between continuous and discontinuous conduction mode) can be calculated in Equation 1:

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}}$$

where

- f is the PWM switching frequency (400 kHz) (1)

Switching frequency versus output current in the light load condition is a function of L , f , V_{IN} and V_{OUT} , but it decreases almost proportional to the output current from the $I_{OUT(LL)}$ given above. For example, it is 40 kHz at $I_{OUT(LL)}/10$ and 4 kHz at $I_{OUT(LL)}/100$.

8.3.2 Low-Side Driver

The low-side driver is designed to drive high-current, low- $R_{DS(on)}$, N-channel MOSFET(s). The drive capability is represented by the internal resistance, which is 3 Ω for V5IN to DRV1 and 0.9 Ω for DRV1 to PGND. A dead-time to prevent shoot through is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. 5-V bias voltage is delivered from V5IN supply. The instantaneous drive current is supplied by an input capacitor connected between V5IN and GND. The average drive current is equal to the gate charge at $V_{GS} = 5$ V times switching frequency. This gate drive current as well as the high-side gate drive current times 5 V makes the driving power which needs to be dissipated from the device package.

Feature Description (continued)

8.3.3 High-Side Driver

The high-side driver is designed to drive high-current, low on-resistance, N-channel MOSFET(s). When configured as a floating driver, 5-V bias voltage is delivered from V5IN supply. The average drive current is also calculated by the gate charge at $V_{GS} = 5V$ times switching frequency. The instantaneous drive current is supplied by the flying capacitor between VBST and LL pins. The drive capability is represented by the internal resistance, which is $3\ \Omega$ for VBST to DRVH and $0.9\ \Omega$ for DRVH to LL.

8.3.4 Current Sensing Scheme

In order to provide both good accuracy and cost effective solution, TPS51116 supports both of external resistor sensing and MOSFET $R_{DS(on)}$ sensing. For resistor sensing scheme, an appropriate current sensing resistor should be connected between the source terminal of the low-side MOSFET and PGND. CS pin is connected to the MOSFET source terminal node. The inductor current is monitored by the voltage between PGND pin and CS pin. For $R_{DS(on)}$ sensing scheme, CS pin should be connected to V5IN (PWP), or V5FILT (RGE) through the trip voltage setting resistor, R_{TRIP} . In this scheme, CS terminal sinks $10\text{-}\mu A$ I_{TRIP} current and the trip level is set to the voltage across the R_{TRIP} . The inductor current is monitored by the voltage between PGND pin and LL pin so that LL pin should be connected to the drain terminal of the low-side MOSFET. I_{TRIP} has $4500\text{ppm}/^{\circ}C$ temperature slope to compensate the temperature dependency of the $R_{DS(on)}$. In either scheme, PGND is used as the positive current sensing node so that PGND should be connected to the proper current sensing device, i.e. the sense resistor or the source terminal of the low-side MOSFET.

8.3.5 PWM Frequency and Adaptive On-Time Control

TPS51116 includes an adaptive on-time control scheme and does not have a dedicated oscillator on board. However, the device runs with fixed 400-kHz pseudo-constant frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The on-time is controlled inverse proportional to the input voltage and proportional to the output voltage so that the duty ratio is kept as V_{OUT}/V_{IN} technically with the same cycle time. Although the TPS51116 does not have a pin connected to VIN, the input voltage is monitored at LL pin during the ON state. This helps pin count reduction to make the part compact without sacrificing its performance. In order to secure minimum ON-time during startup, feed-forward from the output voltage is enabled after the output becomes 750 mV or larger.

8.3.6 VDDQ Output Voltage Selection

TPS51116 can be used for both of DDR ($V_{VDDQ} = 2.5\text{ V}$) and DDR2 ($V_{VDDQ} = 1.8\text{ V}$) power supply and adjustable output voltage ($0.75\text{ V} < V_{VDDQ} < 3\text{ V}$) by connecting VDDQSET pin as shown in Table 1. Use the adjustable output voltage scheme for a DDR3 ($V_{VDDQ} = 1.5\text{ V}$) or LPDDR3/DDR4 ($V_{VDDQ} = 1.2\text{ V}$) application.

Table 1. VDDQSET and Output Voltages

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	$V_{VDDQSNS}/2$	DDR
V5IN	1.8	$V_{VDDQSNS}/2$	DDR2
FB Resistors	Adjustable	$V_{VDDQSNS}/2$	$0.75\text{ V} < V_{VDDQ} < 3\text{ V}^{(1)(2)}$

(1) $V_{VDDQ} \geq 1.2\text{ V}$ when used as VLDOIN

(2) Including DDR3, LPDDR3 and DDR4

8.3.7 VTT Linear Regulator and VTTREF

The TPS51116 device integrates high performance low-dropout linear regulator that is capable of sourcing and sinking current up to 3 A. This VTT linear regulator employs ultimate fast response feedback loop so that small ceramic capacitors are enough to keep tracking the VTTREF within $\pm 40\text{ mV}$ at all conditions including fast load transient. To achieve tight regulation with minimum effect of wiring resistance, a remote sensing terminal, VTTSENS, should be connected to the positive node of VTT output capacitor(s) as a separate trace from VTT pin. For stable operation, total capacitance of the VTT output terminal can be equal to or greater than $20\ \mu F$. It is recommended to attach two $10\text{-}\mu F$ ceramic capacitors in parallel to minimize the effect of ESR and ESL. If ESR

of the output capacitor is greater than 2 mΩ, insert an RC filter between the output and the VTTSENS input to achieve loop stability. The RC filter time constant should be almost the same or slightly lower than the time constant made by the output capacitor and its ESR. VTTREF block consists of on-chip 1/2 divider, LPF and buffer. This regulator also has sink and source capability up to 10 mA. Bypass VTTREF to GND by a 0.033-μF ceramic capacitor for stable operation.

When VTT is not required in the design, following treatment is strongly recommended.

- Connect VLDOIN to VDDQSNS.
- Tie VTTSENS to VTT, and remove capacitors from VTT to float.
- Connect VTTGND and MODE to GND (Non-tracking discharge mode as shown in Table 3)
- Maintain a 0.033-μF capacitor connected at VTTREF.
- Pull down S3 to GND with 1 kΩ of resistance.

A typical circuit for this application is shown in Figure 34

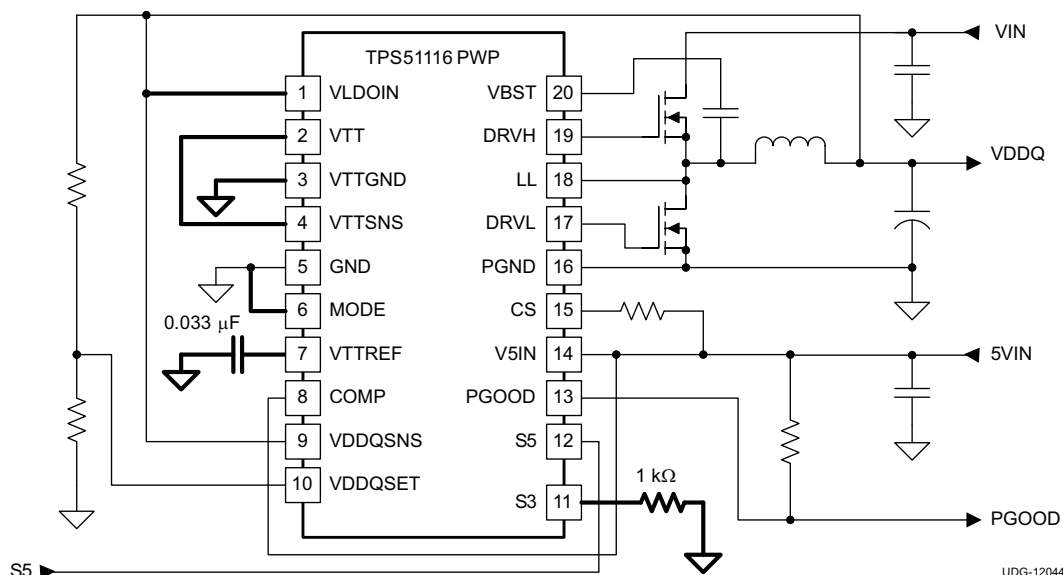


Figure 34. Application Circuit When VTT Is Not Required

8.3.8 Controlling Outputs Using the S3 and S5 Pins

In the DDR, DDR2, DDR3, LPDDR3 or DDR4 memory applications, it is important to maintain the VDDQ voltage level higher than VTT (or VTTREF) voltage including both start-up and shutdown. The TPS51116 device provides this management by simply connecting both the S3 and S5 pins to the sleep-mode signals such as SLP_S3 and SLP_S5 in the notebook PC system. All of VDDQ, VTTREF and VTT are turned on at S0 state (S3 = S5 = high). In S3 state (S3 = low, S5 = high), VDDQ and VTTREF voltages are kept on while VTT is turned off and left at high impedance (high-Z) state. The VTT output is floated and does not sink or source current in this state. In S4/S5 states (S3 = S5 = low), all of the three outputs are disabled. Outputs are discharged to ground according to the discharge mode selected by MODE pin (see *VDDQ and VTT Discharge Control* section). Each state code represents as follow; S0 = full ON, S3 = suspend to RAM (STR), S4 = suspend to disk (STD), S5 = soft OFF. (See Table 2)

Table 2. Sleep Mode Control Using the S3 and S5 Pins

STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF (High-Z)
S4/S5	LO	LO	OFF (Discharge)	Off (Discharge)	OFF (Discharge)

8.3.9 Soft-Start Function and Powergood Status

The soft-start function of the SMPS is achieved by ramping up reference voltage and two-stage current clamp. At the starting point, the reference voltage is set to 650 mV (87% of its target value) and the overcurrent threshold is set half of the nominal value. When UVP comparator detects VDDQ become greater than 80% of the target, the reference voltage is raised toward 750 mV using internal 4-bit DAC. This takes approximately 85 μ s. The overcurrent threshold is released to nominal value at the end of this period. The powergood signal waits another 45 μ s after the reference voltage reaches 750 mV and the VDDQ voltage becomes good (above 95% of the target voltage), then turns off powergood open-drain MOSFET.

The soft-start function of the VTT LDO is achieved by current clamp. The current limit threshold is also changed in two stages using an internal powergood signal dedicated for LDO. During VTT is below the powergood threshold, the current limit level is cut into 60% (2.2 A). This allows the output capacitors to be charged with low and constant current that gives linear ramp up of the output. When the output comes up to the good state, the overcurrent limit level is released to normal value (3.8 A). The device has an independent counter for each output, but the PGOOD signal indicates the status of VDDQ only and does not indicate VTT powergood status externally. See [Figure 35](#).

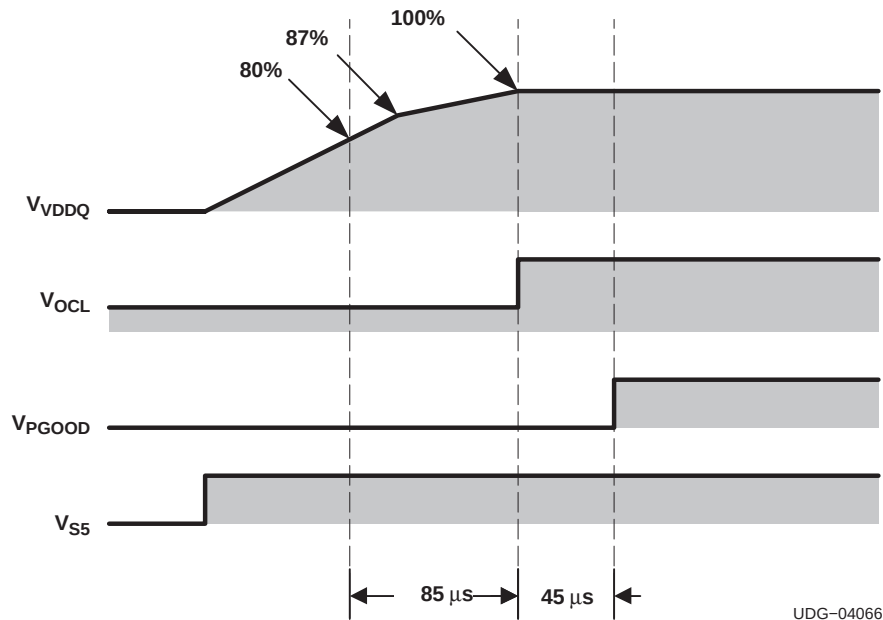


Figure 35. VDDQ Soft-Start and Powergood Timing

Soft-start duration, t_{VDDQSS} , t_{VTTSS} are functions of output capacitances.

$$t_{VDDQSS} = \frac{2 \times C_{VDDQ} \times V_{VDDQ} \times 0.8}{I_{VDDQOCP}} + 85 \mu s$$

where

- $I_{VDDQOCP}$ is the current limit value for VDDQ switcher calculated by [Equation 5](#) (2)

$$t_{VTTSS} = \frac{C_{VTT} \times V_{VTT}}{I_{VTT OCL}}$$

where

- $I_{VTT OCL} = 2.2 \text{ A (typ)}$ (3)

In both [Equation 2](#) and [Equation 3](#), no load current during start-up are assumed. Note that both switchers and the LDO do not start up with full load condition.

8.3.10 VDDQ and VTT Discharge Control

The TPS51116 device discharges VDDQ, VTTREF and VTT outputs when S3 and S5 are both low. There are two different discharge modes. The discharge mode can be set by connecting MODE pin as shown in [Table 3](#).

Table 3. Discharge Selection

MODE	DISCHARGE MODE
V5IN	No discharge
VDDQ	Tracking discharge
GND	Non-tracking discharge

When in tracking-discharge mode, the device discharges outputs through the internal VTT regulator transistors and VTT output tracks half of VDDQ voltage during this discharge. Note that VDDQ discharge current flows via VLDOIN to LDOGND thus VLDOIN must be connected to VDDQ output in this mode. The internal LDO can handle up to 3 A and discharge quickly. After VDDQ is discharged down to 0.2 V, the internal LDO is turned off and the operation mode is changed to the non-tracking-discharge mode.

When in non-tracking-discharge mode, the device discharges outputs using internal MOSFETs which are connected to VDDQSNS and VTT. The current capability of these MOSFETs are limited to discharge slowly. Note that VDDQ discharge current flows from VDDQSNS to PGND in this mode. In no discharge mode, the device does not discharge any output charge.

8.3.11 Current Protection for VDDQ

The SMPS has cycle-by-cycle overcurrent limiting control. The inductor current is monitored during the *OFF* state and the controller keeps the *OFF* state during the inductor current is larger than the overcurrent trip level. The trip level and current sense scheme are determined by CS pin connection (see *Current Sensing Scheme* section). For resistor sensing scheme, the trip level, V_{TRIP} , is fixed value of 60 mV.

For $R_{DS(on)}$ sensing scheme, CS terminal sinks 10 μ A and the trip level is set to the voltage across this R_{TRIP} resistor.

$$V_{TRIP} \text{ (mV)} = R_{TRIP} \text{ (k}\Omega\text{)} \times 10 \text{ (}\mu\text{A)} \quad (4)$$

As the comparison is done during the *OFF* state, V_{TRIP} sets valley level of the inductor current. Thus, the load current at overcurrent threshold, I_{OCP} , can be calculated as shown in [Equation 5](#).

$$I_{OCP} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{I_{RIPPLE}}{2} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (5)$$

In an overcurrent condition, the current to the load exceeds the current to the output capacitor thus the output voltage tends to fall down. If the output voltage becomes less than Powergood level, the V_{TRIP} is cut into half and the output voltage tends to be even lower. Eventually, it crosses the undervoltage protection threshold and shutdown.

8.3.12 Current Protection for VTT

The LDO has an internally fixed constant overcurrent limiting of 3.8 A while operating at normal condition. This trip point is reduced to 2.2 A before the output voltage comes within $\pm 5\%$ of the target voltage or goes outside of $\pm 10\%$ of the target voltage.

8.3.13 Overvoltage and Undervoltage Protection for VDDQ

TPS51116 monitors a resistor divided feedback voltage to detect overvoltage and undervoltage. If VDDQSET is connected to V5IN or GND, the feedback voltage is made by an internal resistor divider inside VDDQSNS pin. If an external resistor divider is connected to VDDQSET pin, the feedback voltage is VDDQSET voltage itself. When the feedback voltage becomes higher than 115% of the target voltage, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

The device monitors the VDDQSNS pin voltage directly and if it becomes greater than 4 V, it turns off the high-side MOSFET driver. When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 32 cycles, TPS51116 latches OFF both top and low-side MOSFETs. This function is enabled after 1007 cycles of SMPS operation to ensure startup.

8.3.14 Undervoltage Lockout (UVLO) Protection, V5IN (PWP), V5FILT (RGE)

The device has 5-V supply undervoltage lockout protection (UVLO). When the V5IN (PWP) voltage or V5FILT (RGE) voltage is lower than UVLO threshold voltage, SMPS, VTTLDO and VTTREF are shut off. This is a non-latch protection.

8.3.15 Input Capacitor, V5IN (PWP), V5FILT (RGE)

Add a ceramic capacitor with a value between 1.0 μF and 4.7 μF placed close to the V5IN (PWP) pin or V5FILT (RGE) pin to stabilize 5 V from any parasitic impedance from the supply.

8.3.16 Thermal Shutdown

TPS51116 monitors the temperature of itself. If the temperature exceeds the threshold value, 160°C (typ), SMPS, VTTLDO and VTTREF are shut off. This is a non-latch protection and the operation is resumed when the device is cooled down by about 10°C.

8.4 Device Functional Modes

8.4.1 VDDQ SMPS, Dual PWM Operation Modes

The main control loop of the SMPS is designed as an adaptive on-time pulse width modulation (PWM) controller. It supports two control schemes which are a current mode and a proprietary D-CAP™ mode. D-CAP™ mode uses internal compensation circuit and is suitable for low external component count configuration with an appropriate amount of ESR at the output capacitor(s). Current mode control has more flexibility, using external compensation network, and can be used to achieve stable operation with very low ESR capacitor(s) such as ceramic or specialty polymer capacitors.

These control modes are selected by the COMP terminal connection. If the COMP pin is connected to V5IN, TPS51116 works in the D-CAP™ mode, otherwise it works in the current mode. VDDQ output voltage is monitored at a feedback point voltage. If VDDQSET is connected to V5IN or GND, this feedback point is the output of the internal resistor divider inside VDDQSNS pin. If an external resistor divider is connected to VDDQSET pin, VDDQSET pin itself becomes the feedback point (see *VDDQ Output Voltage Selection* section).

At the beginning of each cycle, the synchronous high-side MOSFET is turned on, or becomes ON state. This MOSFET is turned off, or becomes OFF state, after internal one shot timer expires. This one shot is determined by V_{IN} and V_{OUT} to keep frequency fairly constant over input voltage range, hence it is called adaptive on-time control (see *PWM Frequency and Adaptive On-Time Control* section). The MOSFET is turned on again when feedback information indicates insufficient output voltage and inductor current information indicates below the overcurrent limit. Repeating operation in this manner, the controller regulates the output voltage. The synchronous low-side or the *rectifying* MOSFET is turned on each OFF state to keep the conduction loss minimum. The rectifying MOSFET is turned off when inductor current information detects zero level. This enables seamless transition to the reduced frequency operation at light load condition so that high efficiency is kept over broad range of load current.

Device Functional Modes (continued)

In the current mode control scheme, the transconductance amplifier generates a target current level corresponding to the voltage difference between the feedback point and the internal 750 mV reference. During the *OFF* state, the PWM comparator monitors the inductor current signal as well as this target current level, and when the inductor current signal comes lower than the target current level, the comparator provides *SET* signal to initiate the next *ON* state. The voltage feedback gain is adjustable outside the controller device to support various types of output MOSFETs and capacitors. In D-CAP mode, the transconductance amplifier is disabled and the PWM comparator compares the feedback point voltage and the internal 750-mV reference during the *OFF* state. When the feedback point comes lower than the reference voltage, the comparator provides *SET* signal to initiate the next *ON* state.

8.4.2 Current Mode Operation

A buck converter using current mode operation can be partitioned into three portions, a voltage divider, an error amplifier and a switching modulator. By linearizing the switching modulator, we can derive the transfer function of the whole system. Because current mode scheme directly controls the inductor current, the modulator can be linearized as shown in Figure 36.

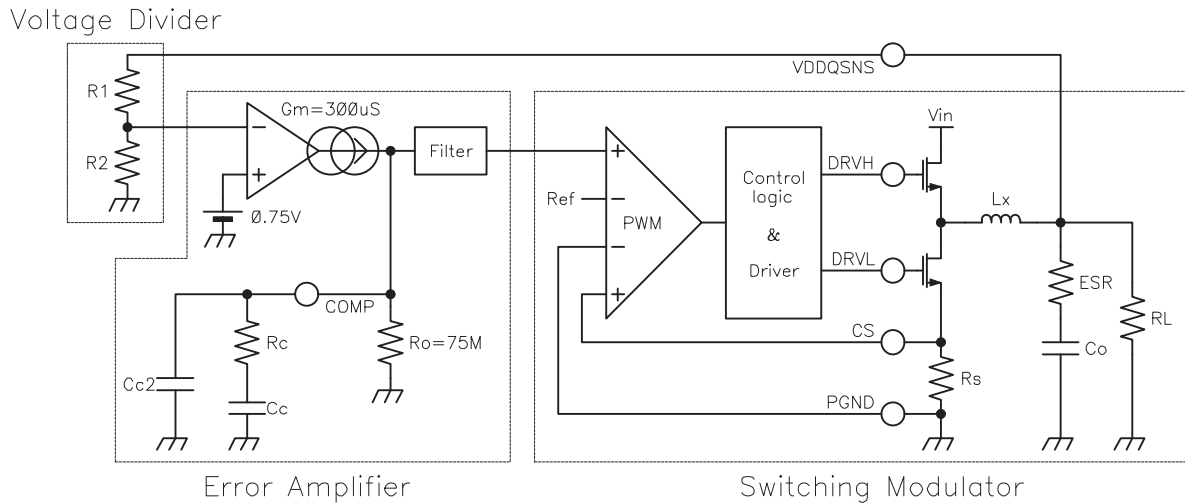


Figure 36. Linearizing the Modulator

In this example, the inductor is located inside the local feedback loop and its inductance does not appear in the small signal model. As a result, a modulated current source including the power inductor can be modeled as a current source with its transconductance of $1/R_S$ and the output capacitor represent the modulator portion. This simplified model is applicable in the frequency space up to approximately a half of the switching frequency. One note is, although the inductance has no influence to small signal model, it has influence to the large signal model as it limits slew rate of the current source. This means the buck converter's load transient response, one of the large signal behaviors, can be improved by using smaller inductance without affecting the loop stability.

Equation 6 describes the total open loop transfer function of the entire system.

$$H(s) = H_1(s) \times H_2(s) \times H_3(s) \quad (6)$$

Assuming $R_L \gg ESR$, $R_O \gg R_C$ and $C_C \gg C_{C2}$, each transfer function of the three blocks is shown starting with Equation 7.

$$H_1(s) = \frac{R_2}{(R_2 + R_1)} \quad (7)$$

$$H_2(s) = -gm \times \frac{R_O (1 + s \times C_C \times R_C)}{(1 + s \times C_C \times R_O) (1 + s \times C_{C2} \times R_C)} \quad (8)$$

Device Functional Modes (continued)

$$H_3(s) = \frac{(1 + s \times C_O \times \text{ESR})}{(1 + s \times C_O \times R_L)} \times \frac{R_L}{R_S} \quad (9)$$

There are three poles and two zeros in $H(s)$. Each pole and zero is given by the following five equations.

$$\omega_{P1} = \frac{1}{(C_C \times R_O)} \quad (10)$$

$$\omega_{P2} = \frac{1}{(C_O \times R_L)} \quad (11)$$

$$\omega_{P3} = \frac{1}{(C_{C2} \times R_C)} \quad (12)$$

$$\omega_{Z1} = \frac{1}{(C_C \times R_C)} \quad (13)$$

$$\omega_{Z2} = \frac{1}{(C_O \times \text{ESR})} \quad (14)$$

Usually, each frequency of those poles and zeros is lower than the 0 dB frequency, f_0 . However, the f_0 should be kept under 1/3 of the switching frequency to avoid effect of switching circuit delay. Equation 15 calculates the 0 dB frequency, f_0 .

$$f_0 = \frac{1}{2\pi} \times \frac{R_1}{R_1 + R_2} \times \frac{g_m}{C_O} \times \frac{R_C}{R_S} = \frac{1}{2\pi} \times \frac{0.75}{V_{OUT}} \times \frac{g_m}{C_O} \times \frac{R_C}{R_S} \quad (15)$$

8.4.3 D-CAP™ Mode Operation

Figure 37 shows a simplified schematic of a buck converter application operating in D-CAP™ mode.

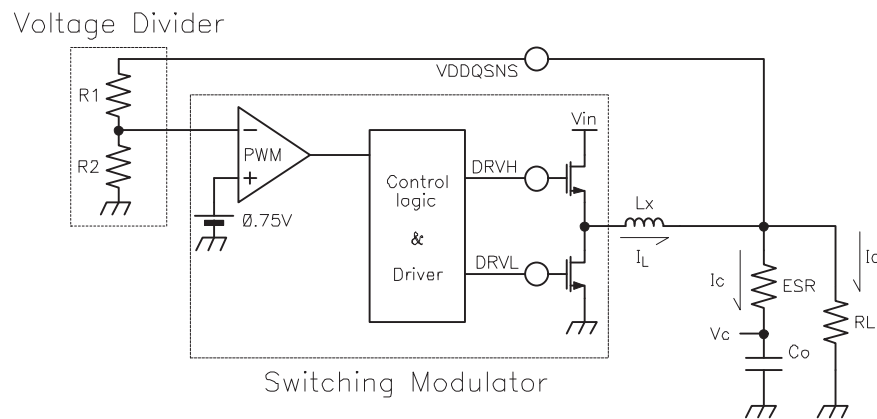


Figure 37. Linearizing the Modulator

The PWM comparator compares the VDDQSNS voltage divided by R1 and R2 with internal reference voltage, and determines the timing to turn on the high-side MOSFET. The gain and speed of the comparator is high enough to maintain the voltage at the beginning of each on cycle (or the end of off cycle) substantially constant. The DC output voltage may have line regulation due to ripple amplitude that slightly increases as the input voltage increase.

f_0 , must be lower than 1/3 of the switching frequency. Equation 16 defines the 0-dB frequency calculation.

$$f_0 = \frac{1}{2\pi \times \text{ESR} \times C_O} \leq \frac{f_{SW}}{3} \quad (16)$$

Device Functional Modes (continued)

Because the 0-dB frequency, f_0 is determined solely by the output capacitor characteristics, loop stability of D-CAP™ mode is determined by the capacitor's chemistry. For example, specialty polymer capacitors (SP-CAP) have C_O in the order of several 100 μ F and ESR in range of 10 m Ω . These makes f_0 on the order of 100 kHz or less and the loop is then stable. However, ceramic capacitors have f_0 at more than 700 kHz, which is not suitable for this operational mode.

Although D-CAP™ mode design provides many advantages such as ease-of-use, minimum external components configuration and extremely short response time, due to not employing an error amplifier in the loop, sufficient amount of feedback signal needs to be provided by external circuit to reduce jitter level.

The required signal level is approximately 15 mV at comparing point. This gives $V_{\text{RIPPLE}} = (V_{\text{OUT}}/0.75) \times 15$ (mV) at the output node. The output capacitor's ESR should meet this requirement.

The external components selection is simple for applications that operate in D-CAP™ mode.

1. **Choose inductor.** Inductor selection for DCAP mode operation is the same as for current mode operation. Please refer to the instructions in the [Current Mode Operation](#) section.
2. **Choose output capacitor(s).** Organic semiconductor capacitor(s) or specialty polymer capacitor(s) are recommended. Determine ESR to meet required ripple voltage above. [Equation 17](#) shows an approximation calculation.

$$\text{ESR} = \frac{V_{\text{OUT}} \times 0.015}{I_{\text{RIPPLE}} \times 0.75} \approx \frac{V_{\text{OUT}}}{I_{\text{OUT(max)}}} \times 60 \text{ [m}\Omega\text{]} \quad (17)$$

9.2.2 Detailed Design Procedure

9.2.2.1 Pin Connections

In current mode configuration, the COMP pin is connect to ground via compensation network. The VDDQSET pin is connect to a resistor divider to set VDDQ voltage at 1.5 V. In this design, the $R_{DS(on)}$ of low side switch is used for current sense, therefore the CS pin connected to V5IN via a resistor. The MODE pin is connected to VDDQ to select tracking discharge mode.

9.2.2.2 Choose the inductor

The inductance value should be determined to give the ripple current of approximately 1/4 to 1/2 of maximum output current.

$$L = \frac{1}{I_{IND(ripple)} \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}} = \frac{2}{I_{OUT(max)} \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}} \quad (18)$$

The inductor also needs to have low DCR to achieve good efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated as shown in [Equation 19](#).

$$I_{IND(peak)} = \frac{V_{TRIP}}{R_{DS(on)}} + \frac{1}{L \times f} \times \frac{(V_{IN(max)} - V_{OUT}) \times V_{OUT}}{V_{IN(max)}} \quad (19)$$

9.2.2.3 Choose rectifying (low-side) MOSFET

When $R_{DS(on)}$ sensing scheme is selected, the rectifying MOSFET's on-resistance is used as this R_S so that lower $R_{DS(on)}$ does not always promise better performance. In order to clearly detect inductor current, minimum R_S recommended is to give 15 mV or larger ripple voltage with the inductor ripple current. This promises smooth transition from CCM to DCM or vice versa. Upper side of the $R_{DS(on)}$ is of course restricted by the efficiency requirement, and usually this resistance affects efficiency more at high-load conditions. When using external resistor current sensing, there is no restriction for low $R_{DS(on)}$. However, the current sensing resistance R_S itself affects the efficiency

9.2.2.4 Choose output capacitance

When organic semiconductor capacitors (OS-CON) or specialty polymer capacitors (SP-CAP) are used, ESR to achieve required ripple value at stable state or transient load conditions determines the amount of capacitor(s) need, and capacitance is then enough to satisfy stable operation. The peak-to-peak ripple value can be estimated by ESR times the inductor ripple current for stable state, or ESR times the load current step for a fast transient load response. When ceramic capacitor(s) are used, the ESR is usually small enough to meet ripple requirement. In contrast, transient undershoot and overshoot driven by output capacitance becomes the key factor in determining the capacitor(s) required.

9.2.2.5 Determine f_0 and calculate R_C

Use [Equation 20](#) to and calculate R_C . A higher R_C value shows faster transient response in cost of unstableness. If the transient response is not enough even with high R_C value, try increasing the out put capacitance. The recommended f_0 value is $f_{OSC}/4$.

$$R_C \leq 2\pi \times f_0 \times \frac{V_{OUT}}{0.75} \times \frac{C_O}{gm} \times R_S \quad (20)$$

$$R_C = 2.8 \times V_{OUT} \times C_O [\mu F] \times R_S [m\Omega] \quad (21)$$

9.2.2.6 Calculate C_{C2}

This capacitance acts to cancel zero caused by ESR of the output capacitor. When ceramic capacitors are used, there is no need for capacitor C_{C2} .

$$\omega_{z2} = \frac{1}{(C_O \times ESR)} = \omega_{p3} = \frac{1}{(C_{C2} \times R_C)} \quad (22)$$

$$C_{C2} = \frac{C_O \times ESR}{R_C} \quad (23)$$

9.2.2.7 Calculate C_C .

The purpose of C_C is to cut DC component to obtain high DC feedback gain. However, as it causes phase delay, another zero to cancel this effect at f_0 frequency is need. This zero, ω_{z1} , is determined by C_C and R_C . Recommended ω_{z1} is 10 times lower to the f_0 frequency.

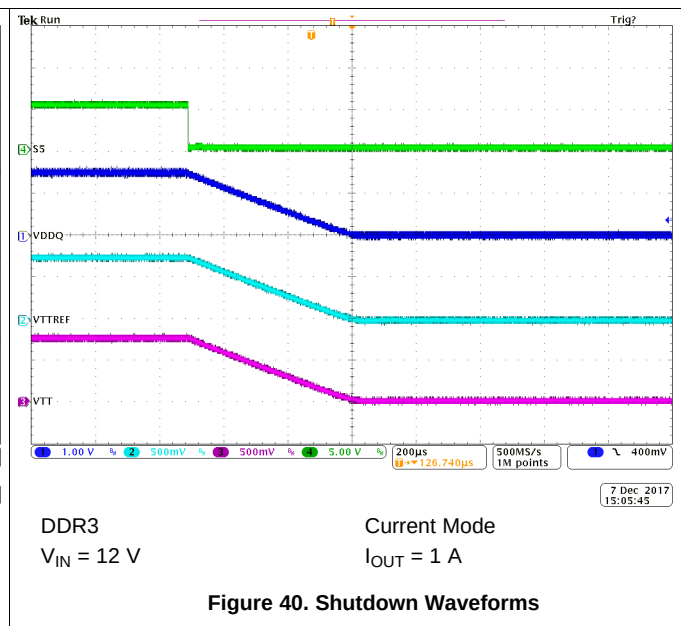
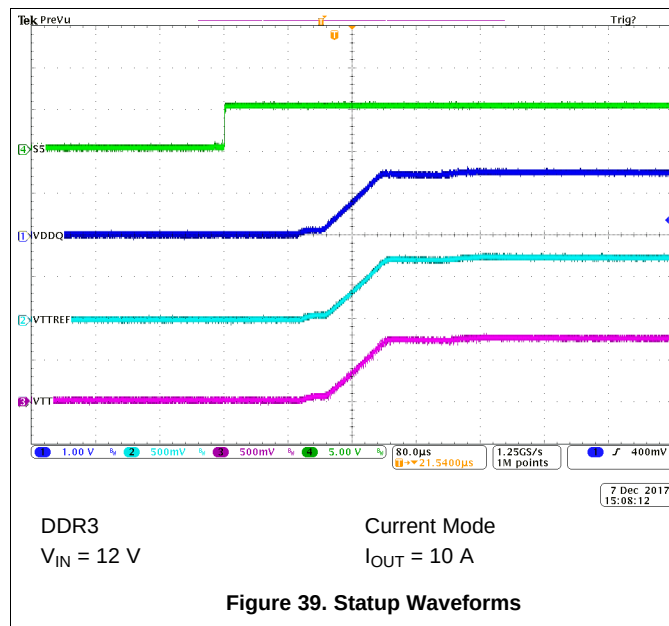
$$f_{z1} = \frac{1}{2\pi \times C_C \times R_C} = \frac{f_0}{10} \quad (24)$$

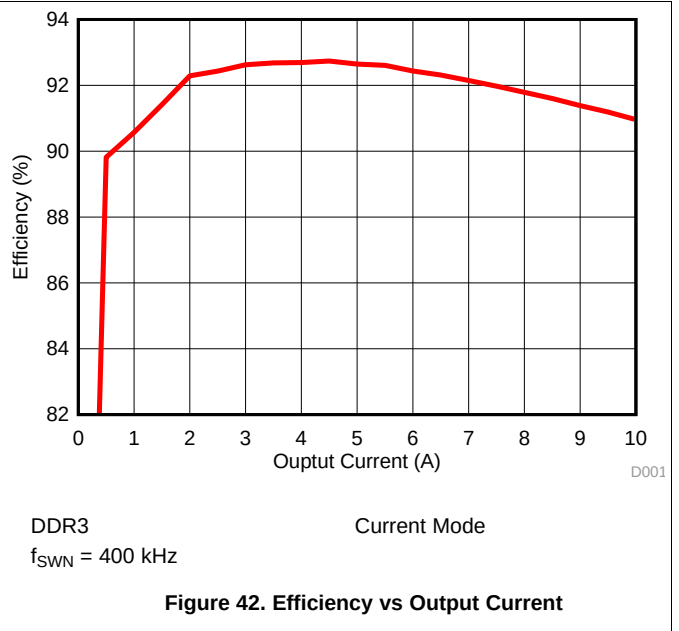
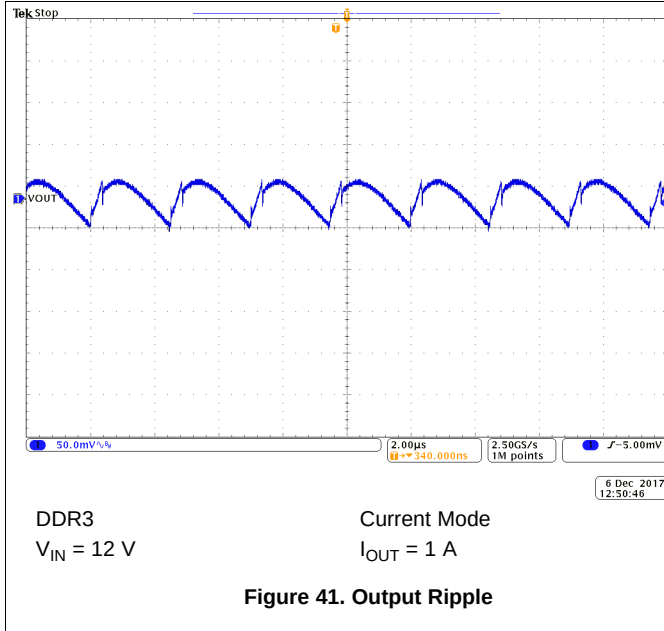
9.2.2.8 Determine the value of $R1$ and $R2$.

These two resistor values are required when using adjustable mode,

$$R1 = \frac{V_{OUT} - 0.75}{0.75} \times R2 \quad (25)$$

9.2.3 Application Curves





9.3 DDR3 Application With D-CAP™ Mode

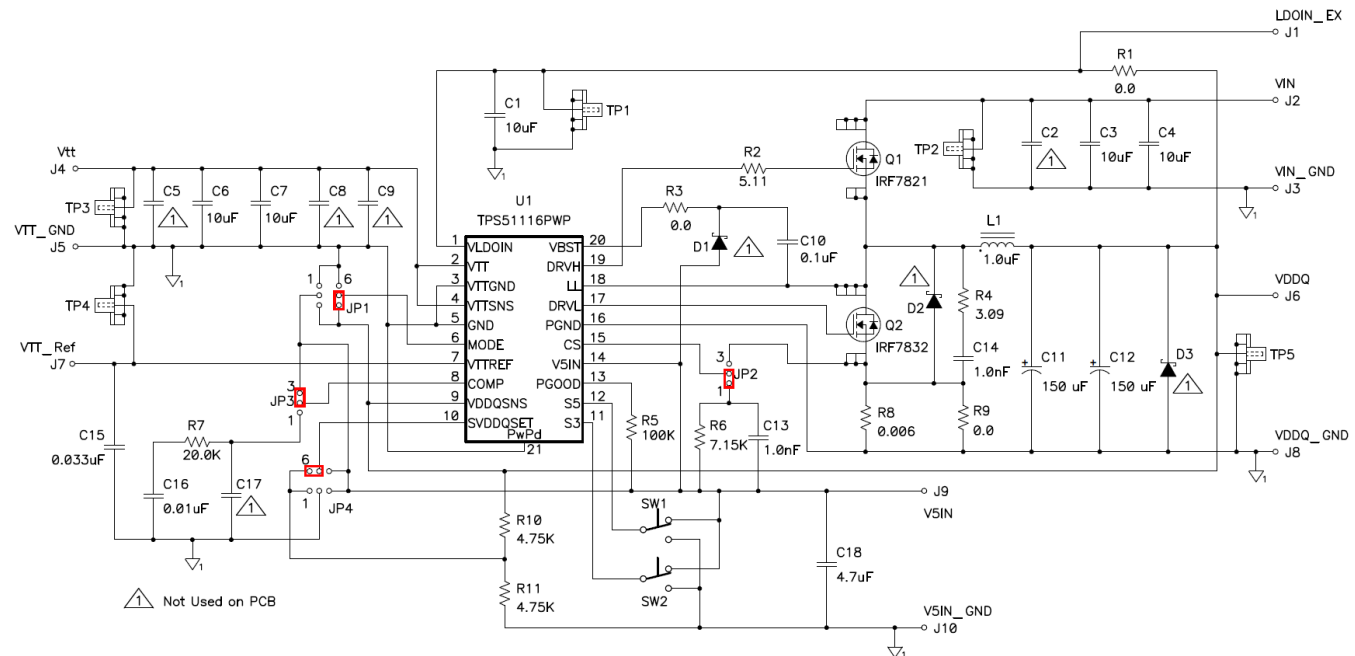


Figure 43. DDR3 DCAP Mode Application Schematic

9.3.1 Design Requirements

Table 5. Design Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		4.5	12	28	V
V_{V5IN}	V5IN voltage			5		V
V_{VDDQ}	VDDQ output voltage	DDR3		1.5		V
I_{VDDQ}	VDDQ output current		0		10	A
V_{VTT}	VTT output voltage			0.75		V
I_{VTT}	VTT output current	DDR3, $V_{VTT} = 0.75$ V	-3		3	A

9.3.2 Detailed Design Procedure

The general design procedure is the same as that for the current mode design example described in [Detailed Design Procedure](#).

9.3.2.1 Pin Connections

In D-CAP™ mode configuration, the COMP pin is connect to V5IN. The VDDQSET pin is connect to a resistor divider to set VDDQ voltage at 1.5 V. In this design, the $R_{DS(on)}$ of low side switch is used for current sense, therefore the CS pin connected to V5IN via a resistor. The MODE pin is connected to VDDQ to select tracking discharge mode.

9.3.2.2 Choose the Components

Refer to the instructions in the current mode design example to choose inductor, MOSFETs. Organic semiconductor capacitor or polymer capacitor are recommended for D-CAP™ mode design. The output ripple should be larger than $(V_{OUT}/0.75) \times 15$ (mV). In this design, two pieces of 150 µF PSCAP capacitors with 45 mΩ ESR are selected.

9.3.3 Application Curves

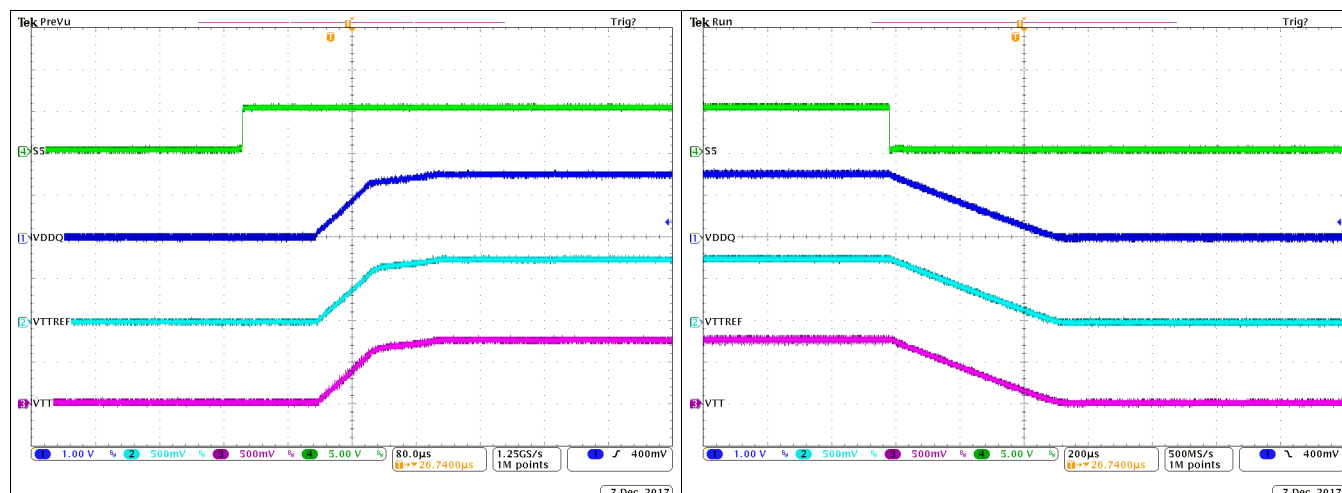


Figure 44. Startup Waveforms

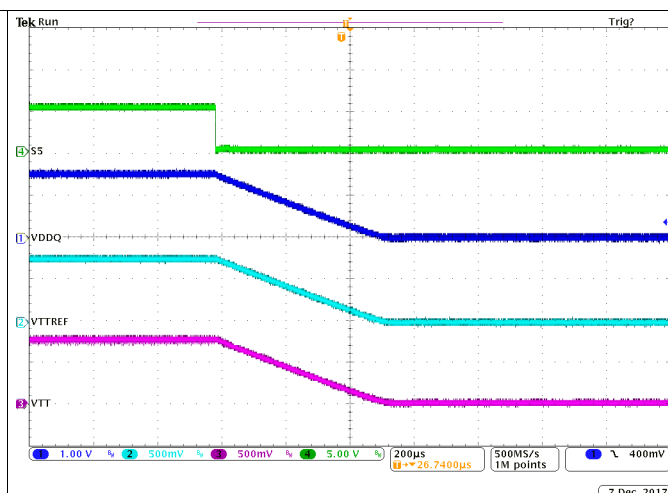


Figure 45. Shutdown Waveforms

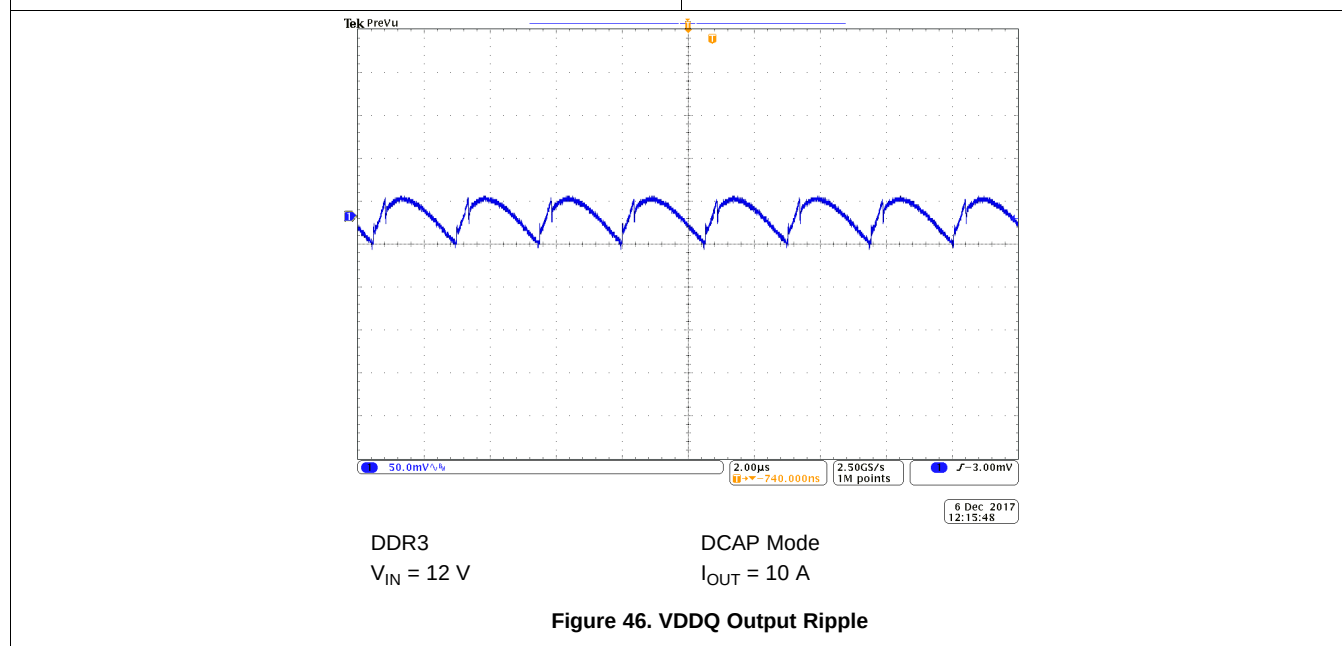


Figure 46. VDDQ Output Ripple

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply between 3 V and 28 V. There are input voltage and switch node voltage limitations from the MOSFET. A separate 5-V power supply is required for the internal circuits and MOSFET gate drivers of the device.

11 Layout

11.1 Layout Guidelines

Consider these guidelines before designing a layout using the TPS51116 device.

- PCB trace defined as LL node, which connects to source of switching MOSFET, drain of rectifying MOSFET and high-voltage side of the inductor, should be as short and wide as possible.
- Consider adding a small snubber circuit, consisting of a 3-Ω resistor and a 1-nF capacitor, between LL and PGND in case a high-frequency surge is observed on the LL voltage waveform.
- All sensitive analog traces such as VDDQSNS, VTTSNS and CS should be placed away from high-voltage switching nodes such as LL, DRVH or DRVH nodes to avoid coupling.
- VLDOIN should be connected to VDDQ output with short and wide trace. If different power source is used for VLDOIN, an input bypass capacitor should be placed to the pin as close as possible with short and wide connection.
- The output capacitor for VTT should be placed close to the pin with short and wide connection in order to avoid additional ESR and/or ESL of the trace.
- VTTSNS should be connected to the positive node of VTT output capacitor(s) as a separate trace from the high current power line and is strongly recommended to avoid additional ESR and/or ESL. If it is needed to sense the voltage of the point of the load, it is recommended to attach the output capacitor(s) at that point. Also, it is recommended to minimize any additional ESR and/or ESL of ground trace between GND pin and the output capacitor(s).
- Consider adding LPF at VTTSNS when the ESR of the VTT output capacitor(s) is larger than 2 mΩ.
- VDDQSNS can be connected separately from VLDOIN. Remember that this sensing potential is the reference voltage of VTTREF. Avoid any noise generative lines.
- Negative node of VTT output capacitor(s) and VTTREF capacitor should be tied together by avoiding common impedance to the high current path of the VTT source/sink current.
- GND (Signal GND) pin node represents the reference potential for VTTREF and VTT outputs. Connect GND to negative nodes of VTT capacitor(s), VTTREF capacitor and VDDQ capacitor(s) with care to avoid additional ESR and/or ESL. GND and PGND (power ground) should be connected together at a single point.
- Connect CS_GND (RGE) to source of rectifying MOSFET using Kevin connection. Avoid common trace for high-current paths such as the MOSFET to the output capacitors or the PGND to the MOSFET trace. When using an external current sense resistor, apply the same care and connect it to the positive side (ground side) of the resistor.
- PGND is the return path for rectifying MOSFET gate drive. Use 0.65 mm (25 mil) or wider trace. Connect to source of rectifying MOSFET with shortest possible path.
- Place a V5FILT filter capacitor (RGE) close to the device, within 12 mm (0.5 inches) if possible.
- The trace from the CS pin should avoid high-voltage switching nodes such as those for LL, VBST, DRVH, DRVH or PGOOD.
- In order to effectively remove heat from the package, prepare thermal land and solder to the package's thermal pad. Wide trace of the component-side copper, connected to this thermal land, helps heat spreading. Include numerous vias with a 0.33-mm diameter connected from the thermal land to the internal and solder-side ground plane(s) to enhance heat dissipation.

11.2 Layout Example

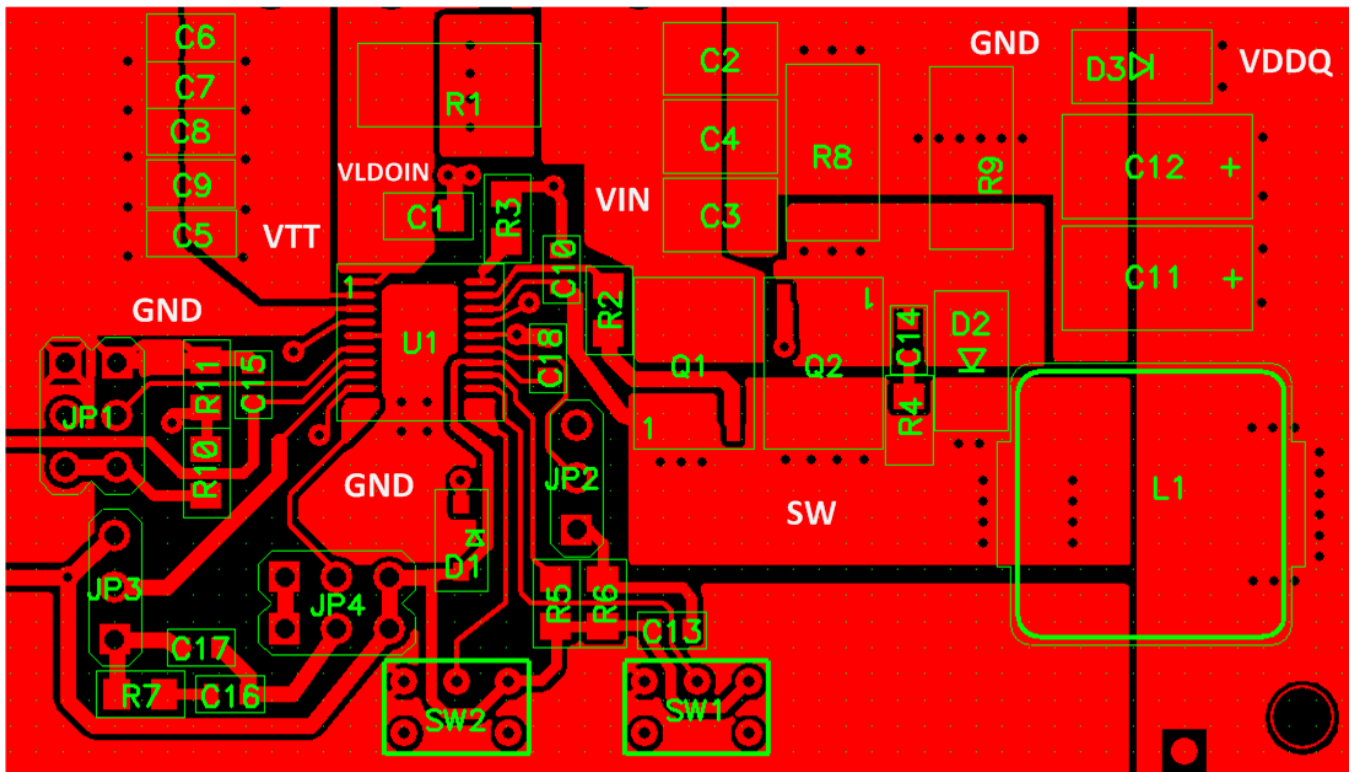


Figure 47. Layout

12 器件和文档支持

12.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

TI E2E™ 在线社区 [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.3 商标

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12.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS51116PWP	Active	Production	HTSSOP (PWP) 20	70 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS51116
TPS51116PWP.A	Active	Production	HTSSOP (PWP) 20	70 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS51116
TPS51116PWP.B	Active	Production	HTSSOP (PWP) 20	70 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS51116
TPS51116PWPG4	Active	Production	HTSSOP (PWP) 20	70 TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS51116
TPS51116PWPR	Active	Production	HTSSOP (PWP) 20	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS51116
TPS51116PWPR.A	Active	Production	HTSSOP (PWP) 20	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS51116
TPS51116PWPR.B	Active	Production	HTSSOP (PWP) 20	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS51116
TPS51116PWPRG4	Active	Production	HTSSOP (PWP) 20	2000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS51116
TPS51116RGER	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51116
TPS51116RGER.A	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51116
TPS51116RGER.B	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51116
TPS51116RGERG4	Active	Production	VQFN (RGE) 24	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51116
TPS51116RGET	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51116
TPS51116RGET.A	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51116
TPS51116RGET.B	Active	Production	VQFN (RGE) 24	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 51116

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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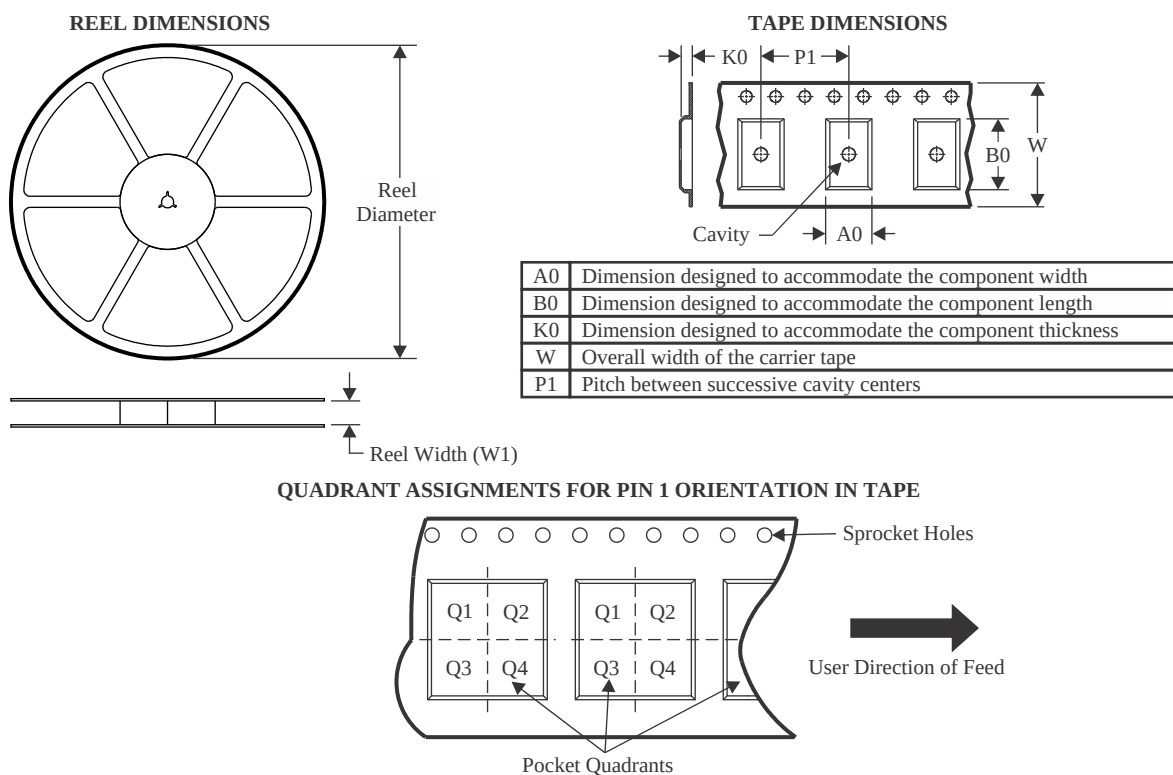
OTHER QUALIFIED VERSIONS OF TPS51116 :

- Enhanced Product : [TPS51116-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

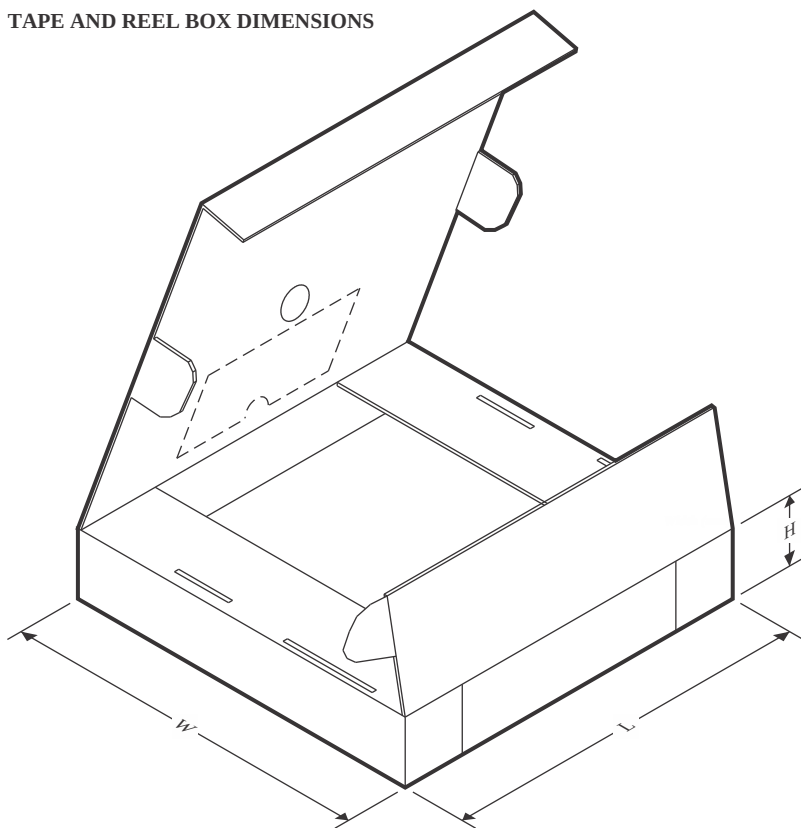
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS51116PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS51116RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS51116RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS51116PWPR	HTSSOP	PWP	20	2000	350.0	350.0	43.0
TPS51116RGER	VQFN	RGE	24	3000	346.0	346.0	33.0
TPS51116RGET	VQFN	RGE	24	250	210.0	185.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
TPS51116PWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS51116PWP.A	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS51116PWP.B	PWP	HTSSOP	20	70	530	10.2	3600	3.5
TPS51116PWPG4	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

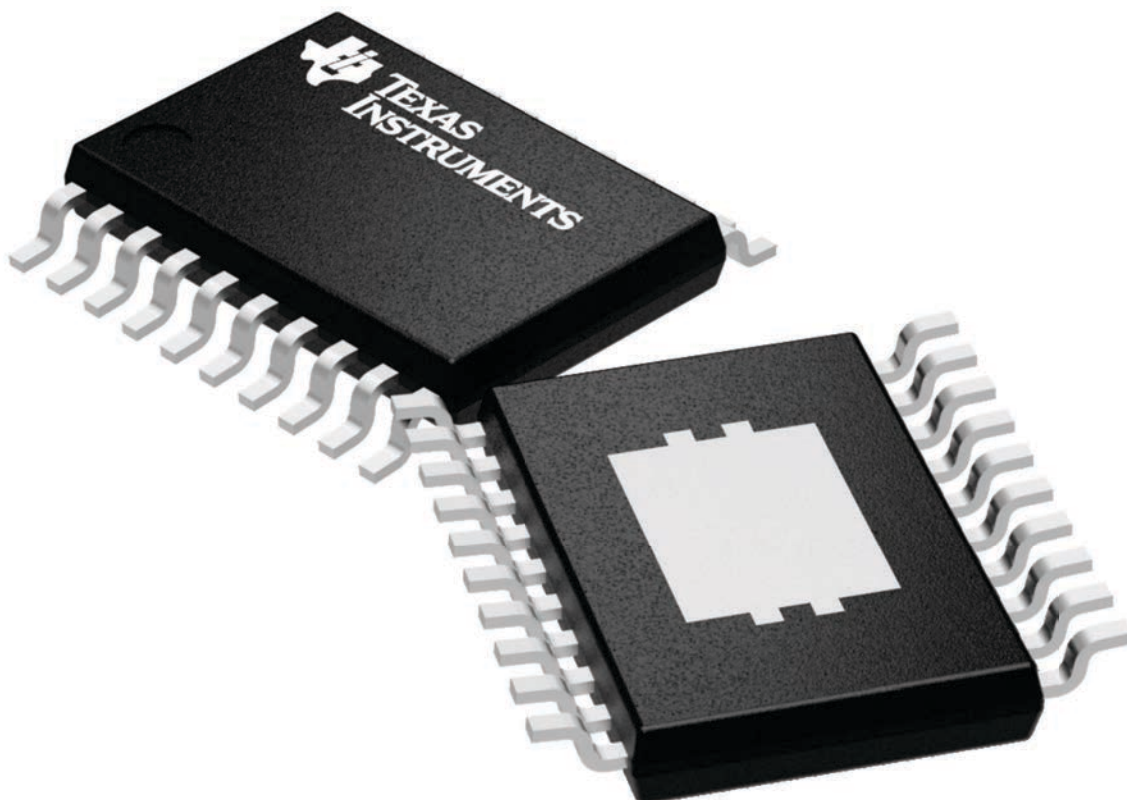
PWP 20

HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

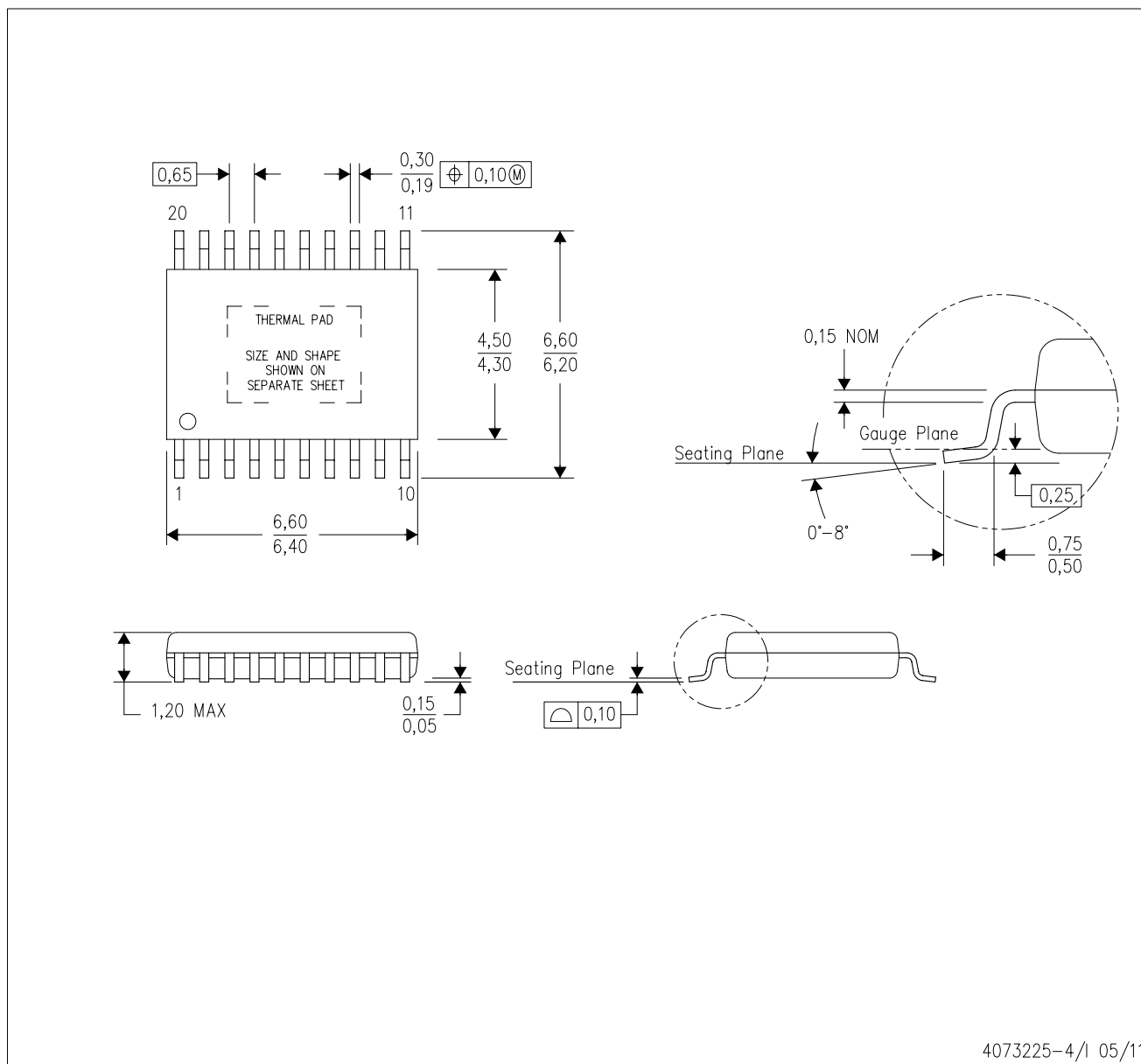
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224669/A

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

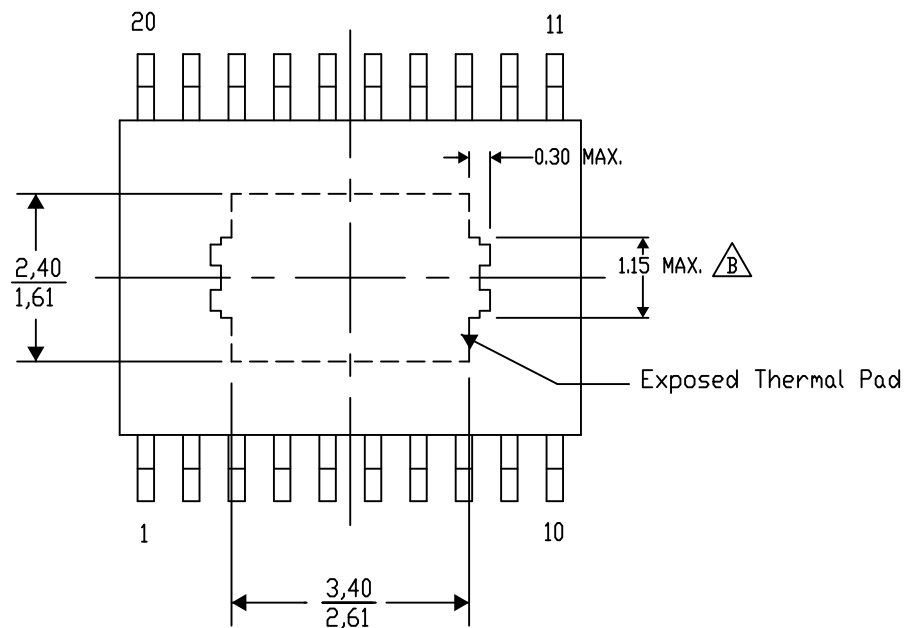
PWP (R-PDSO-G20) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



4206332-15/AO 01/16

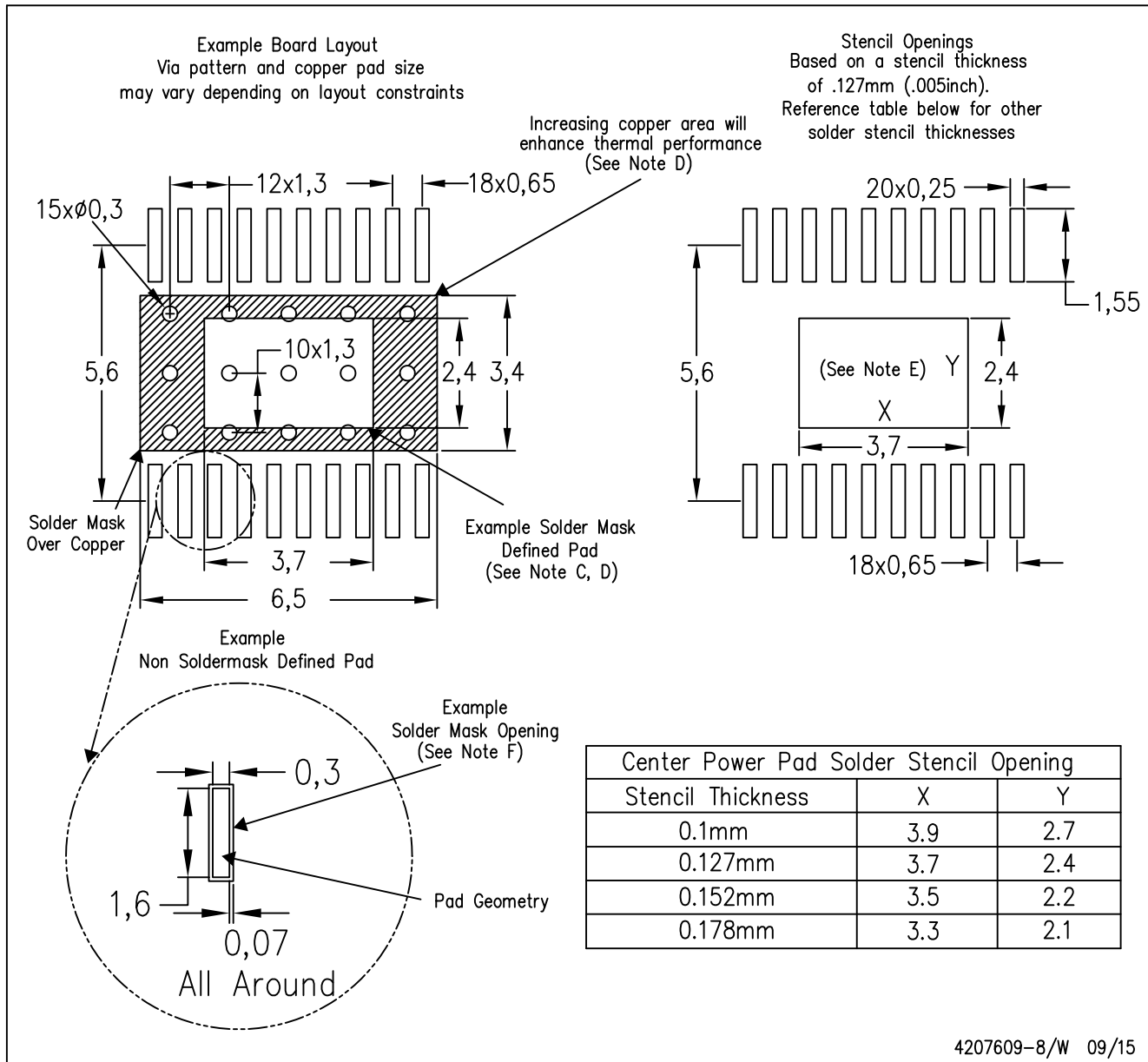
NOTE: A. All linear dimensions are in millimeters

 Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G20)

PowerPAD™ PLASTIC SMALL OUTLINE



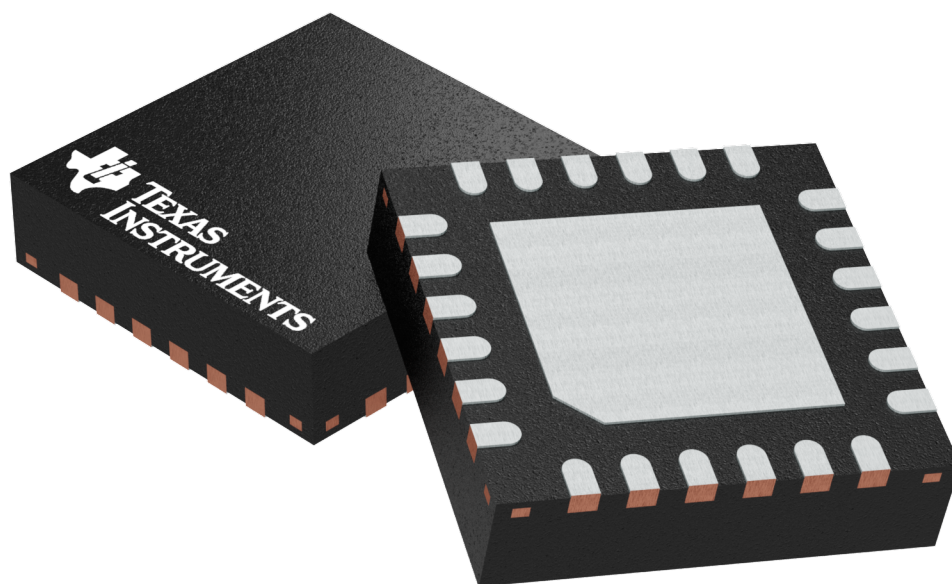
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGE 24

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H



VQFN - 1 mm max height

The drawing shows a 24-pin connector with the following features and dimensions:

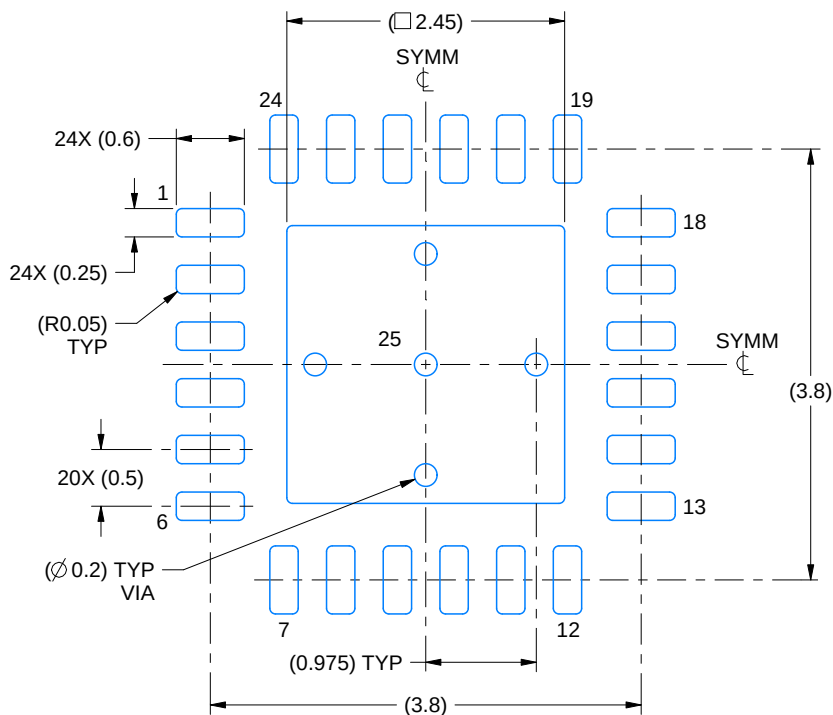
- Overall Dimensions:** Width is 4.1 with a tolerance of 3.9. Height is 4.1 with a tolerance of 3.9.
- PIN 1 INDEX AREA:** A shaded rectangular area in the top-left corner.
- DETAIL OPTIONAL TERMINAL TYPICAL:** A cross-sectional view of a terminal with dimensions 0.5, 0.3, 0.3, and 0.2.
- SEATING PLANE:** Indicated by a horizontal line and a triangle symbol.
- Terminal Dimensions:**
 - Top terminals: 1 MAX height, 0.05 to 0.00 thickness.
 - Bottom terminals: 0.08 C width.
- Internal Features:**
 - 2X 2.5 dimensions for internal structures.
 - 2.45 ± 0.1 dimension for a central feature.
 - 7, 12, 13, 19, 24, 25 dimensions for various internal features.
 - EXPOSED THERMAL PAD: A central square feature.
 - SYMM: Symmetry lines.
 - 20X 0.5 dimension for a series of small features.
 - 24X 0.5 to 0.3 dimension for a series of small features.
 - 24X 0.3 to 0.2 dimension for a series of small features.
 - 0.1 (M) and 0.05 (M) dimensions for small features.
 - 0.1 (M) dimension for a small feature.
 - 0.08 C dimension for a small feature.
 - 0.1 (M) dimension for a small feature.
 - 0.05 (M) dimension for a small feature.
- Other Callouts:**
 - SEE TERMINAL DETAIL: Points to a specific terminal.
 - PIN 1 ID (OPTIONAL): Points to a specific pin.
 - (0.2) TYP: Typical dimension for a small feature.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

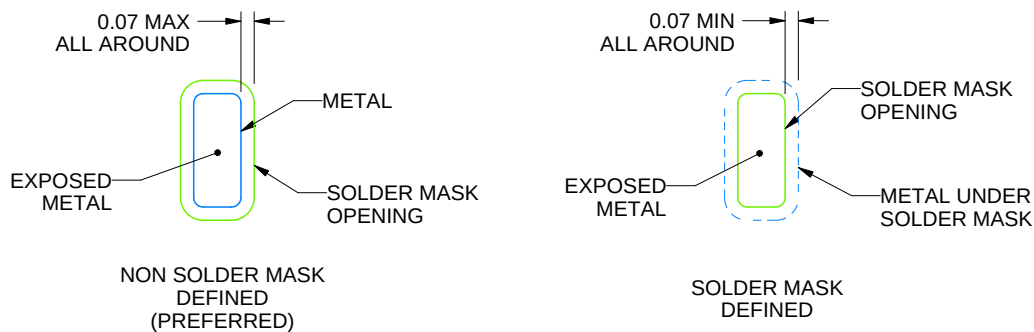
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

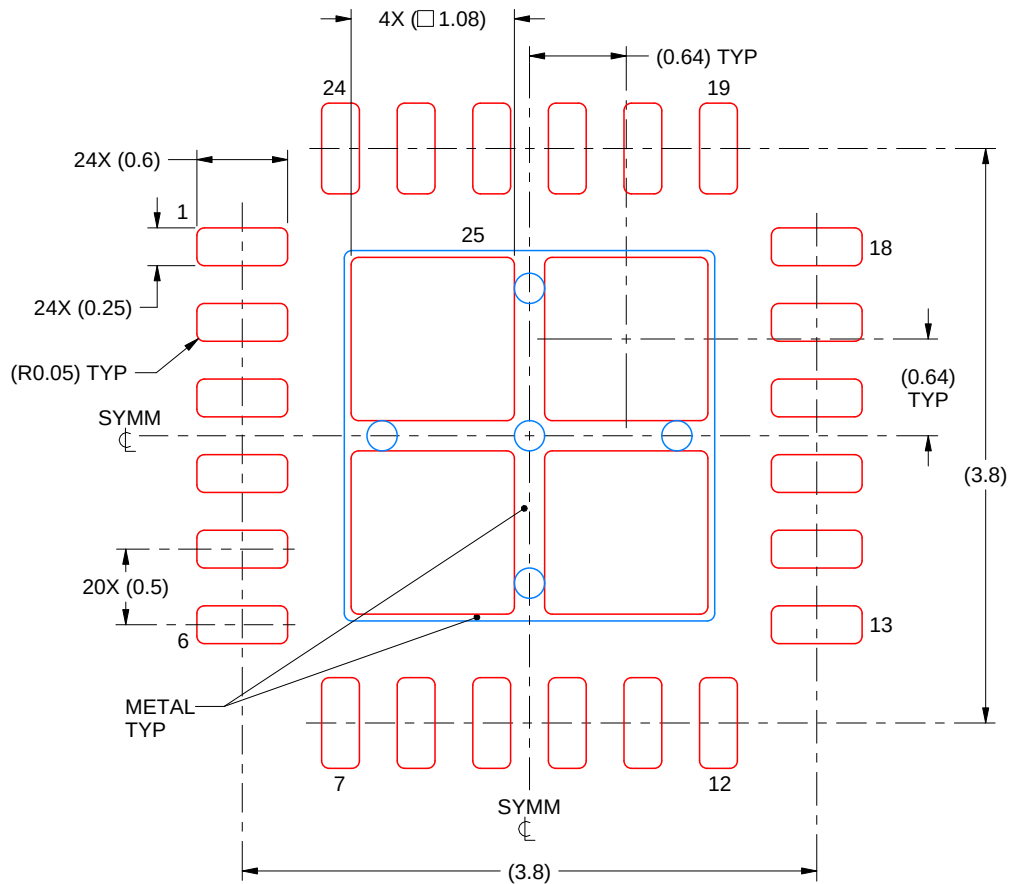
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



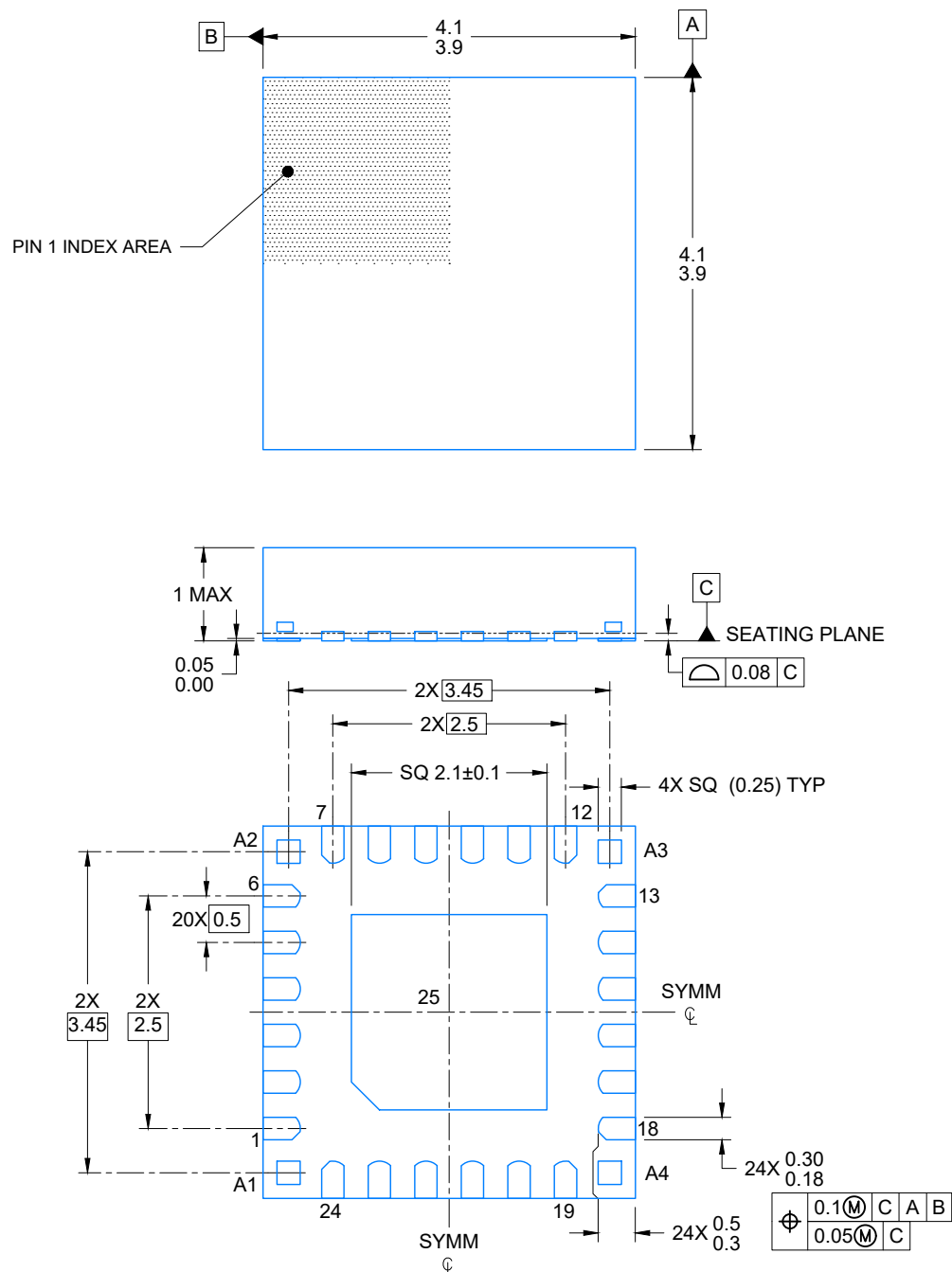
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4225246/A 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

SOLDER MASK DETAILS

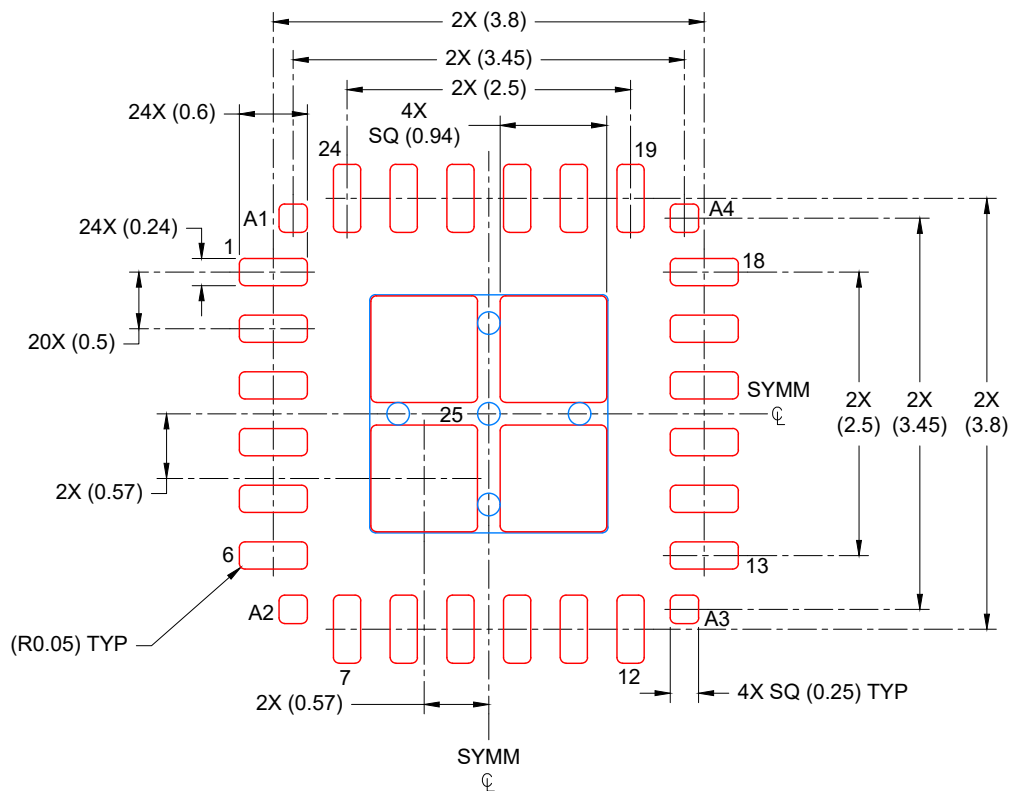
The diagram illustrates two cross-sectional views of a microvia, comparing non-solder mask defined and solder mask defined structures.

NON SOLDER MASK DEFINED (PREFERRED): This view shows a microvia with a green solder mask opening and a blue metal layer. The dimensions are labeled as 0.07 MAX ALL AROUND. The labels include METAL, EXPOSED METAL, and SOLDER MASK OPENING.

SOLDER MASK DEFINED: This view shows a microvia with a blue solder mask opening and a green metal layer. The dimensions are labeled as 0.07 MIN ALL AROUND. The labels include METAL UNDER SOLDER MASK, EXPOSED METAL, and SOLDER MASK OPENING.



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SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
 80% PRINTED COVERAGE BY AREA
 SCALE: 15X

4225246/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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