

# 具有可编程延迟的 TPS3890-Q1 低静态电流、1% 精度监控器

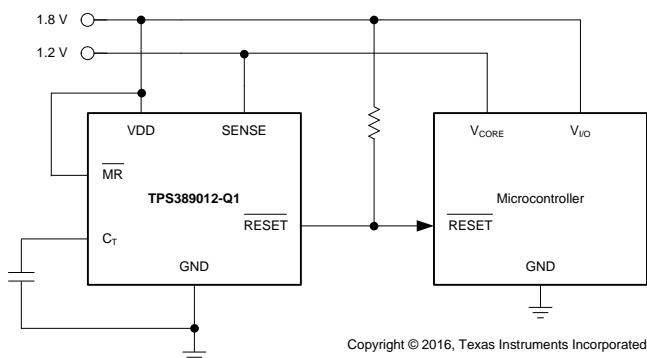
## 1 特性

- 符合汽车应用 标准
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1: -40°C 至 125°C 的环境运行温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 上电复位 (POR) 发生器具有可调延迟时间: 25 $\mu$ s 到 30s
- 极低电源电流: 2.1 $\mu$ A (典型值)
- 高阈值精度: 1% (最大值)
- 高精度迟滞
- 固定和可调节阈值电压:
  - 标准电压轨的固定阈值为: 1.2V 到 5V
  - 可调节阈值电压低至 1.15V
- 手动复位 ( $\overline{\text{MR}}$ ) 输入
- 开漏  $\overline{\text{RESET}}$  输出
- 温度范围: -40°C 至 +125°C
- 封装: 1.5mm x 1.5mm 晶圆级小外形无引线 (WSON) 封装

## 2 应用

- 信息娱乐系统音响主机
- 混合/数字仪表盘组
- 外部放大器
- ADAS 摄像头
- 汽车网关

典型应用电路



## 3 说明

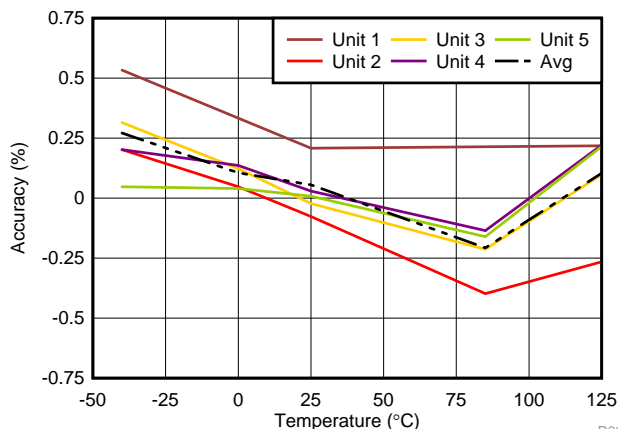
TPS3890-Q1 是一款具有较低静态电流的高精度电压监控器，可监视低至 1.15V 的系统电压，在 SENSE 电压降至低于预设阈值或手动复位 ( $\overline{\text{MR}}$ ) 引脚降为逻辑低电平时发出开漏  $\overline{\text{RESET}}$  信号。在 SENSE 电压和手动复位 ( $\overline{\text{MR}}$ ) 返回至相应阈值以上之后， $\overline{\text{RESET}}$  输出会在用户可调节延迟时间内保持低电平。TPS3890-Q1 系列采用高精度电压基准，可实现 1% 的阈值精度。通过将 CT 引脚与外部电容器相连，用户可在 25 $\mu$ s 到 30s 范围内调节复位延迟时间。TPS3890-Q1 具有 2.1 $\mu$ A 的极低静态电流，采用 1.5mm x 1.5mm 小型封装，非常适用于电池供电和空间受限应用供电的绝佳器件。该器件的额定工作温度范围为 -40°C 至 +125°C ( $T_J$ )。

器件信息<sup>(1)</sup>

| 器件型号       | 封装       | 封装尺寸 (标称值)      |
|------------|----------|-----------------|
| TPS3890-Q1 | WSON (6) | 1.50mm x 1.50mm |

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

$V_{ITN}$  精度与温度间的关系



D001



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## 4 修订历史记录

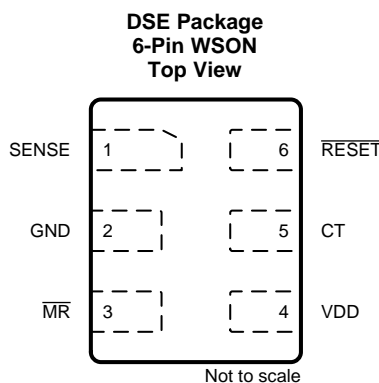
| <b>Changes from Revision A (October 2017) to Revision B</b> | <b>Page</b> |
|---|-------------|
| • 已添加 汽车 特性 .....   | <b>1</b>    |
| • Added new voltage options to Device Comparison Table..... | <b>3</b>    |

| <b>Changes from Original (March 2017) to Revision A</b> | <b>Page</b> |
|---|-------------|
| • Added TPS389050L-Q1 to Device Comparison Table .....  | <b>3</b>    |

## 5 Device Comparison Table

| PART NUMBER   | NOMINAL SUPPLY VOLTAGE | NEGATIVE THRESHOLD ( $V_{ITN}$ ) | POSITIVE THRESHOLD ( $V_{ITP}$ ) |
|---------------|------------------------|----------------------------------|----------------------------------|
| TPS389001-Q1  | Adjustable             | 1.15 V                           | 1.157 V                          |
| TPS389012-Q1  | 1.2 V                  | 1.15 V                           | 1.157 V                          |
| TPS389015-Q1  | 1.5 V                  | 1.44 V                           | 1.449 V                          |
| TPS389018-Q1  | 1.8 V                  | 1.73 V                           | 1.740 V                          |
| TPS389025-Q1  | 2.5 V                  | 2.40 V                           | 2.414 V                          |
| TPS389030-Q1  | 3.0 V                  | 2.89 V                           | 2.907 V                          |
| TPS389033-Q1  | 3.3 V                  | 3.17 V                           | 3.189 V                          |
| TPS389033G-Q1 | 3.3 V                  | 3.06 V                           | 3.084 V                          |
| TPS389033K-Q1 | 3.3 V                  | 2.93 V                           | 2.947 V                          |
| TPS389050-Q1  | 5.0 V                  | 4.80 V                           | 4.828 V                          |
| TPS389050G-Q1 | 5.0 V                  | 4.65 V                           | 4.677 V                          |
| TPS389050L-Q1 | 5.0 V                  | 4.40 V                           | 4.425 V                          |

## 6 Pin Configuration and Functions



### Pin Functions

| PIN |                           | I/O | DESCRIPTION   |
|-----|---------------------------|-----|---|
| NO. | NAME                      |     |   |
| 1   | SENSE                     | I   | This pin is connected to the voltage to be monitored. When the voltage on SENSE falls below the negative threshold voltage $V_{ITN}$ , $\overline{\text{RESET}}$ goes low (asserts). When the voltage on SENSE rises above the positive threshold voltage $V_{ITP}$ , $\overline{\text{RESET}}$ goes high (deasserts).  |
| 2   | GND                       | —   | Ground  |
| 3   | $\overline{\text{MR}}$    | I   | Driving the manual reset pin ( $\overline{\text{MR}}$ ) low causes $\overline{\text{RESET}}$ to go low (assert).  |
| 4   | VDD                       | I   | Supply voltage pin. Good analog design practice is to place a 0.1- $\mu\text{F}$ ceramic capacitor close to this pin.   |
| 5   | CT                        | —   | The CT pin offers a user-adjustable delay time. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$ delay time to deassert. $t_{PD(f)}$ (sec) = $C_{CT}$ ( $\mu\text{F}$ ) $\times$ 1.07 + 25 $\mu\text{s}$ (nom).  |
| 6   | $\overline{\text{RESET}}$ | O   | $\overline{\text{RESET}}$ is an open-drain output that is driven to a low-impedance state when either the $\overline{\text{MR}}$ pin is driven to a logic low or the monitored voltage on the SENSE pin is lower than the negative threshold voltage ( $V_{ITN}$ ). $\overline{\text{RESET}}$ remains low (asserted) for the delay time period after both $\overline{\text{MR}}$ is set to a logic high and the SENSE input is above $V_{ITP}$ . A pullup resistor from 10 k $\Omega$ to 1 M $\Omega$ should be used on this pin. |

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)<sup>(1)</sup>

|             |                                    | MIN  | MAX | UNIT |
|-------------|------------------------------------|------|-----|------|
| Voltage     | V <sub>DD</sub>                    | -0.3 | 7   | V    |
|             | SENSE                              | -0.3 | 7   |      |
|             | RESET                              | -0.3 | 7   |      |
|             | MR                                 | -0.3 | 7   |      |
|             | V <sub>CT</sub>                    | -0.3 | 7   |      |
| Current     | RESET                              | -20  | 20  | mA   |
| Temperature | Operating junction, T <sub>J</sub> | -40  | 125 | °C   |
|             | Operating ambient, T <sub>A</sub>  | -40  | 125 |      |
|             | Storage, T <sub>stg</sub>          | -65  | 150 |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

|  |   | VALUE | UNIT |
|--|---|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±2000 | V    |
|  | Charged-device model (CDM), per AEC Q100-011            | ±750  |      |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                    |   | MIN | NOM | MAX  | UNIT |
|--------------------|---|-----|-----|------|------|
| V <sub>DD</sub>    | Power-supply voltage                        | 1.5 |     | 5.5  | V    |
| V <sub>SENSE</sub> | SENSE voltage                               | 0   |     | 5.5  | V    |
| V <sub>RESET</sub> | RESET pin voltage                           | 0   |     | 5.5  | V    |
| I <sub>RESET</sub> | RESET pin current                           | -5  |     | 5    | mA   |
| C <sub>IN</sub>    | Input capacitor, V <sub>DD</sub> pin        | 0   | 0.1 |      | μF   |
| C <sub>CT</sub>    | Reset timeout capacitor, CT pin             | 0   |     | 26   | μF   |
| R <sub>PU</sub>    | Pullup resistor, RESET pin                  | 1   |     | 1000 | kΩ   |
| T <sub>J</sub>     | Junction temperature (free-air temperature) | -40 | 25  | 125  | °C   |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TPS3890-Q1 | UNIT |
|-------------------------------|--|------------|------|
|                               |  | DSE (WSO)  |      |
|                               |  | 6 PINS     |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 321.3      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 207.9      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 281.5      | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 42.4       | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 284.8      | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 142.3      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ( $T_A = T_J$ ),  $1.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{DD}$  (unless otherwise noted); typical values are at  $V_{DD} = 5.5\text{ V}$  and  $T_J = 25^{\circ}\text{C}$

| PARAMETER             |   | TEST CONDITIONS  | MIN                 | TYP                  | MAX    | UNIT          |
|-----------------------|---|--|---------------------|----------------------|--------|---------------|
| $V_{DD}$              | Input supply voltage                                  |  | 1.5                 |                      | 5.5    | V             |
| $V_{POR}$             | Power-on-reset voltage                                | $V_{OL(max)} = 0.2\text{ V}$ , $I_{RESET} = 15\text{ }\mu\text{A}$   |                     |                      | 0.8    | V             |
| $I_{DD}$              | Supply current (into VDD pin)                         | $V_{DD} = 3.3\text{ V}$ , $I_{RESET} = 0\text{ mA}$ ,<br>$-40^{\circ}\text{C} < T_J < 85^{\circ}\text{C}$  |                     | 2.09                 | 3.72   | $\mu\text{A}$ |
|                       |   | $V_{DD} = 3.3\text{ V}$ , $I_{RESET} = 0\text{ mA}$ ,<br>$-40^{\circ}\text{C} < T_J < 105^{\circ}\text{C}$ |                     |                      | 4.5    |               |
|                       |   | $V_{DD} = 3.3\text{ V}$ , $I_{RESET} = 0\text{ mA}$  |                     |                      | 5.8    |               |
|                       |   | $V_{DD} = 5.5\text{ V}$ , $I_{RESET} = 0\text{ mA}$ ,<br>$-40^{\circ}\text{C} < T_J < 85^{\circ}\text{C}$  |                     | 2.29                 | 4      |               |
|                       |   | $V_{DD} = 5.5\text{ V}$ , $I_{RESET} = 0\text{ mA}$ ,<br>$-40^{\circ}\text{C} < T_J < 105^{\circ}\text{C}$ |                     |                      | 5.2    |               |
|                       |   | $V_{DD} = 5.5\text{ V}$ , $I_{RESET} = 0\text{ mA}$  |                     |                      | 6.5    |               |
| $V_{ITN}$ , $V_{ITP}$ | SENSE input threshold voltage accuracy                |  | -1%                 | $\pm 0.5\%$          | 1%     |               |
| $V_{HYST}$            | Hysteresis <sup>(1)</sup>                             |  | 0.325%              | 0.575%               | 0.825% |               |
| $I_{SENSE}$           | Input current   | $V_{SENSE} = 5\text{ V}$   |                     |                      | 8      | $\mu\text{A}$ |
|                       |   | $V_{SENSE} = 5\text{ V}$ , TPS389001-Q1,<br>TPS389012-Q1   |                     | 10                   | 100    | nA            |
| $I_{CT}$              | CT pin charge current                                 |  | 0.90                | 1.15                 | 1.35   | $\mu\text{A}$ |
| $V_{CT}$              | CT pin comparator threshold voltage                   |  | 1.17                | 1.23                 | 1.29   | V             |
| $R_{CT}$              | CT pin pulldown resistance                            | When $\overline{\text{RESET}}$ is deasserted   |                     | 200                  |        | $\Omega$      |
| $V_{IL}$              | Low-level input voltage ( $\overline{\text{MR}}$ pin) |  |                     | $0.25 \times V_{DD}$ |        | V             |
| $V_{IH}$              | High-level output voltage                             |  | $0.7 \times V_{DD}$ |                      |        | V             |
| $V_{OL}$              | Low-level output voltage                              | $V_{DD} \geq 1.5\text{ V}$ , $I_{RESET} = 0.4\text{ mA}$   |                     |                      | 0.25   | V             |
|                       |   | $V_{DD} \geq 2.7\text{ V}$ , $I_{RESET} = 2\text{ mA}$   |                     |                      | 0.25   |               |
|                       |   | $V_{DD} \geq 4.5\text{ V}$ , $I_{RESET} = 3\text{ mA}$   |                     |                      | 0.3    |               |
| $I_{LKG(OD)}$         | Open-drain output leakage                             | High impedance,<br>$V_{SENSE} = V_{RESET} = 5.5\text{ V}$  |                     |                      | 250    | nA            |

(1)  $V_{HYST} = [(V_{ITP} - V_{ITN}) / V_{ITN}] \times 100\%$ .

## 7.6 Timing Requirements

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ( $T_A = T_J$ ),  $1.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $\overline{\text{MR}} = V_{DD}$ , and 5% input overdrive<sup>(1)</sup> (unless otherwise noted); typical values are at  $V_{DD} = 5.5\text{ V}$  and  $T_J = 25^{\circ}\text{C}$

|                 |   | MIN   | NOM | MAX | UNIT          |
|-----------------|---|---|-----|-----|---------------|
| $t_{PD(f)}$     | SENSE (falling) to $\overline{\text{RESET}}$ propagation delay                | $C_T = \text{open}$ , $V_{DD} = 3.3\text{ V}$ | 18  |     | $\mu\text{s}$ |
|                 |   | $C_T = \text{open}$ , $V_{DD} = 5.5\text{ V}$ | 8   |     |               |
| $t_{PD(r)}$     | SENSE (rising) to $\overline{\text{RESET}}$ propagation delay                 | $C_T = \text{open}$ , $V_{DD} = 3.3\text{ V}$ | 25  |     | $\mu\text{s}$ |
| $t_{GI(SENSE)}$ | SENSE pin glitch immunity   | $V_{DD} = 5.5\text{ V}$                       | 9   |     | $\mu\text{s}$ |
| $t_{GI(MR)}$    | $\overline{\text{MR}}$ pin glitch immunity                                    | $V_{DD} = 5.5\text{ V}$                       | 100 |     | ns            |
| $t_{MRW}$       | $\overline{\text{MR}}$ pin pulse duration to assert $\overline{\text{RESET}}$ | 1   |     |     | $\mu\text{s}$ |
| $t_{d(MR)}$     | $\overline{\text{MR}}$ pin low to out delay                                   |   | 250 |     | ns            |
| $t_{STRT}$      | Startup delay   |   | 325 |     | $\mu\text{s}$ |

(1) Overdrive =  $| (V_{IN} / V_{THRESH} - 1) \times 100\% |$ .

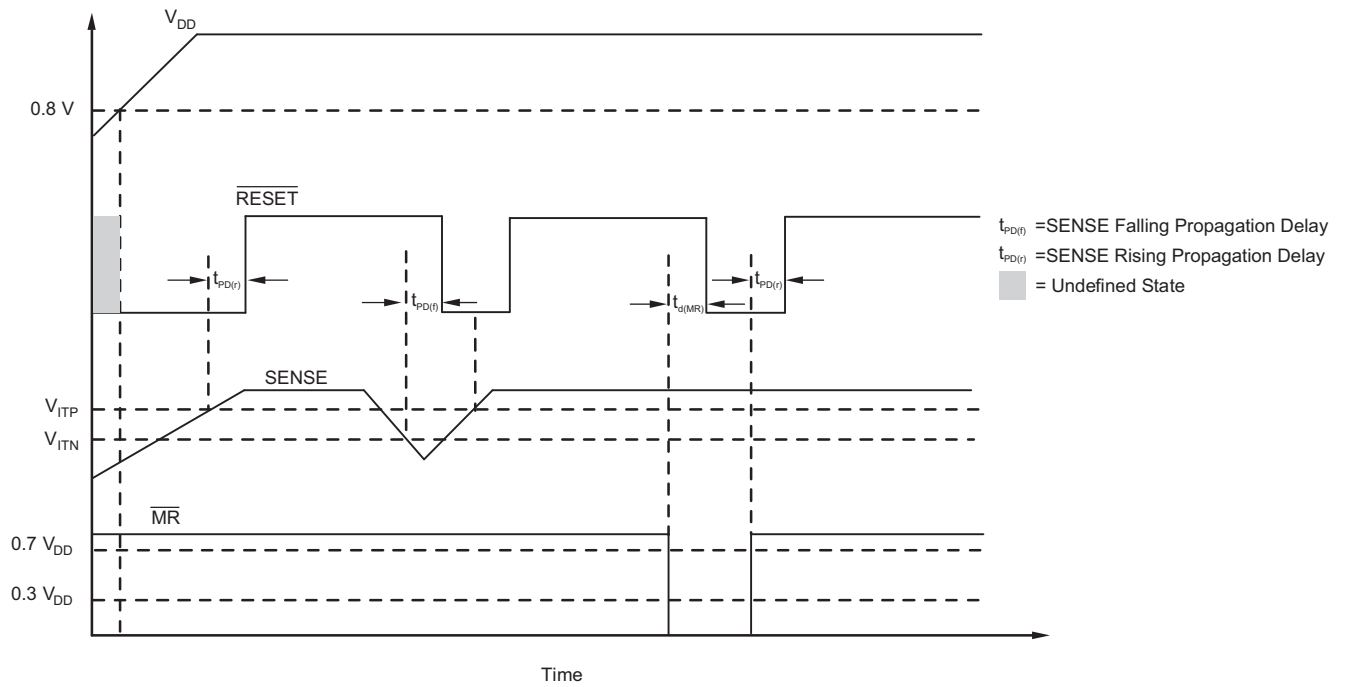


图 1. Timing Diagram

### 7.7 Typical Characteristics

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{\text{DD}}$  (unless otherwise noted)

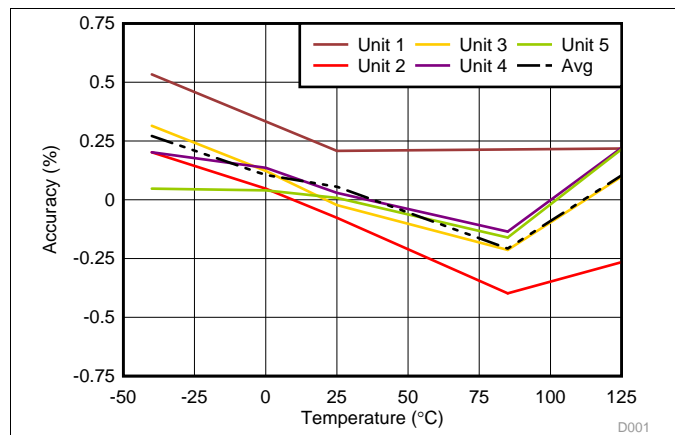


图 2.  $V_{\text{ITN}}$  Accuracy vs Temperature

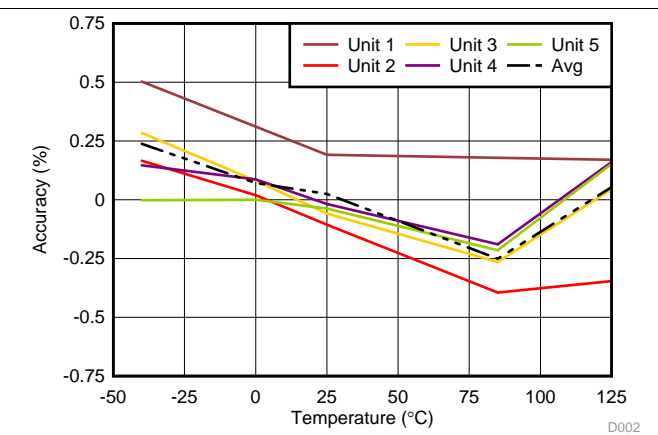


图 3.  $V_{\text{ITP}}$  Accuracy vs Temperature

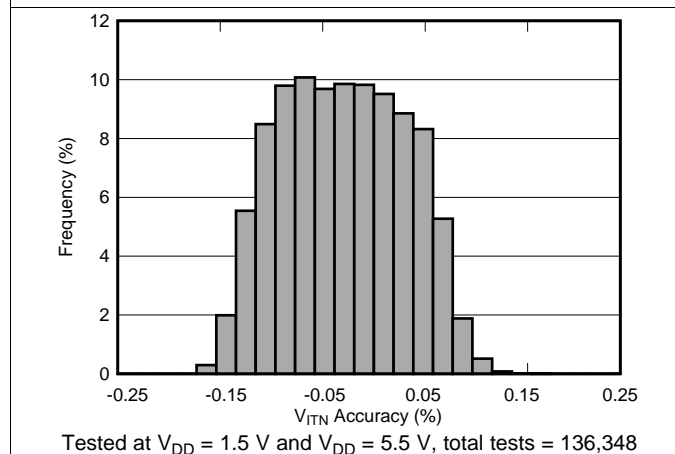


图 4.  $V_{\text{ITN}}$  Accuracy Histogram

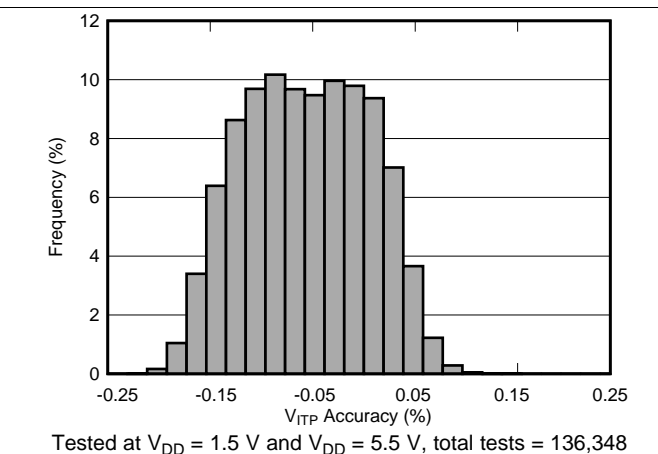


图 5.  $V_{\text{ITP}}$  Accuracy Histogram

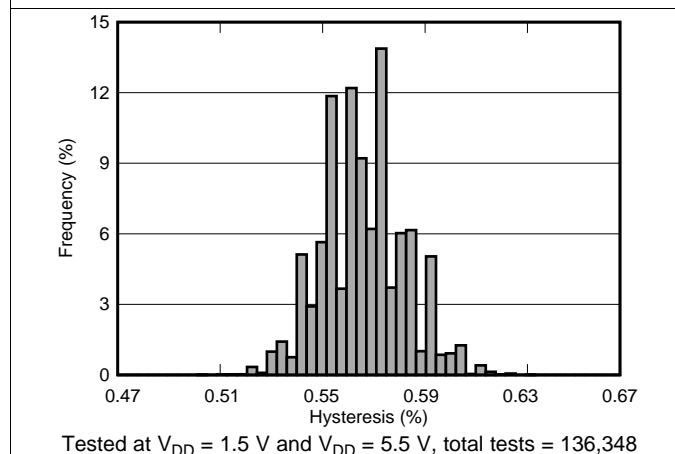


图 6. Hysteresis Histogram

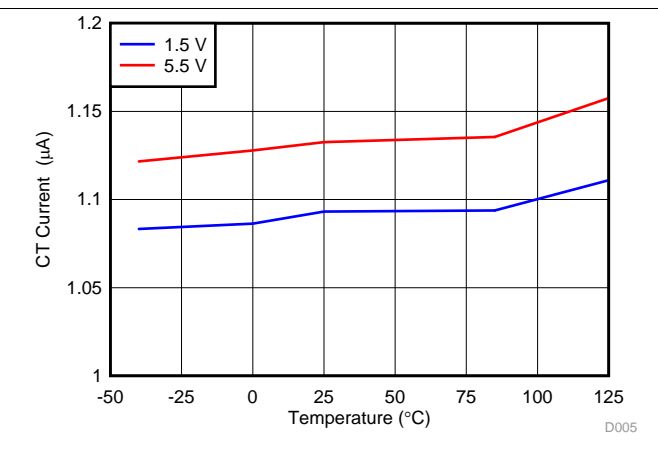


图 7. CT Current vs Temperature

Typical Characteristics (接下页)

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{\text{DD}}$  (unless otherwise noted)

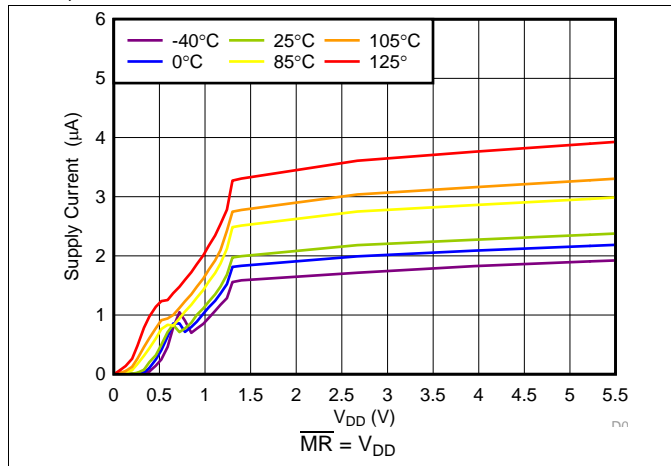


图 8. Supply Current vs Power-Supply Voltage

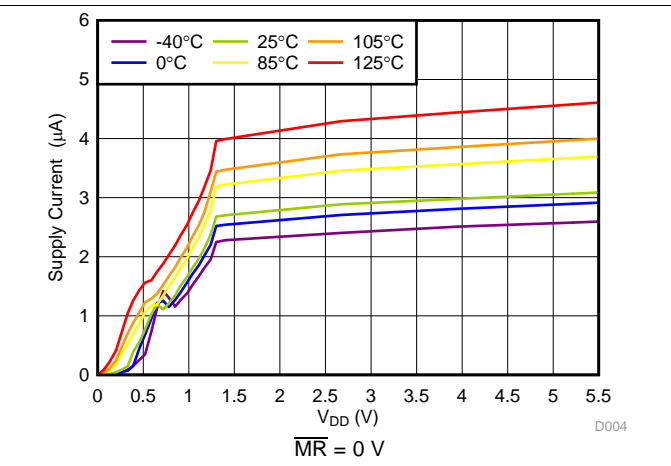


图 9. Supply Current vs Power-Supply Voltage

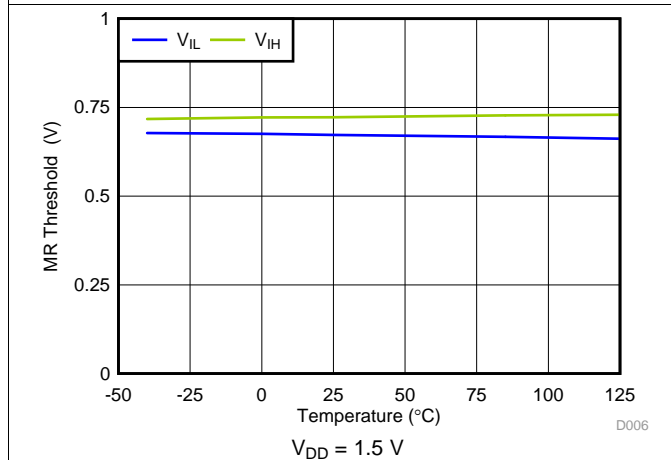


图 10.  $\overline{\text{MR}}$  Threshold vs Temperature

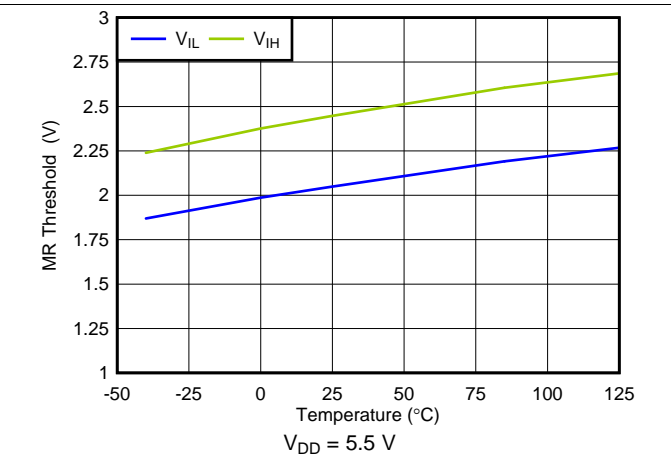


图 11.  $\overline{\text{MR}}$  Threshold vs Temperature

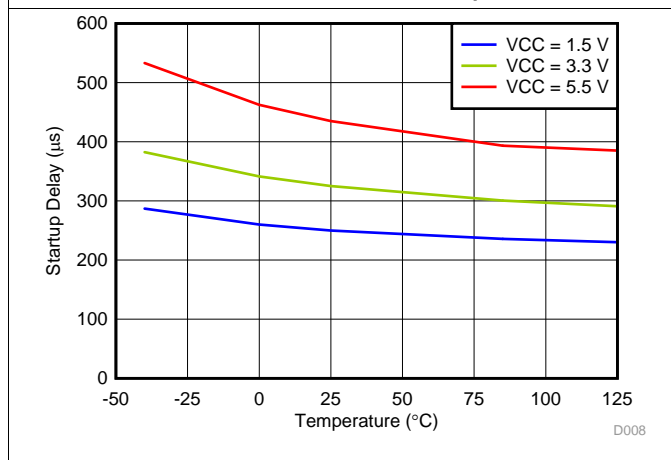


图 12. Startup Delay vs Temperature

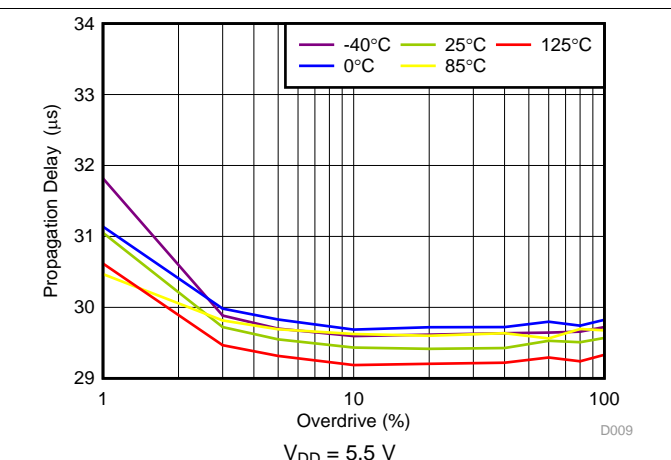


图 13. Propagation Delay ( $t_{\text{PD}(r)}$ ) vs Overdrive



Typical Characteristics (接下页)

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{\text{DD}}$  (unless otherwise noted)

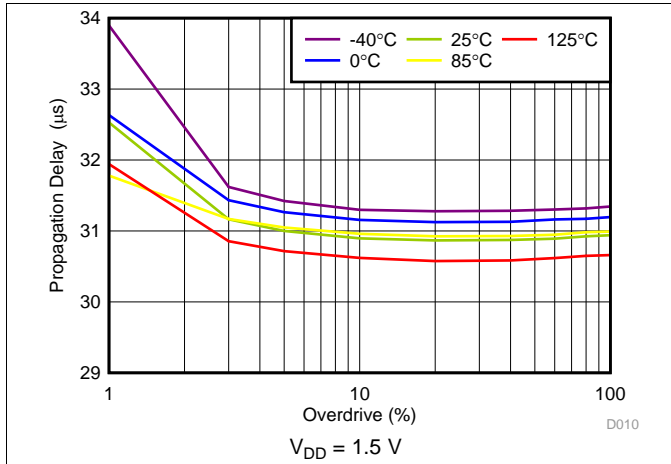


图 14. Propagation Delay ( $t_{\text{PD}(f)}$ ) vs Overdrive

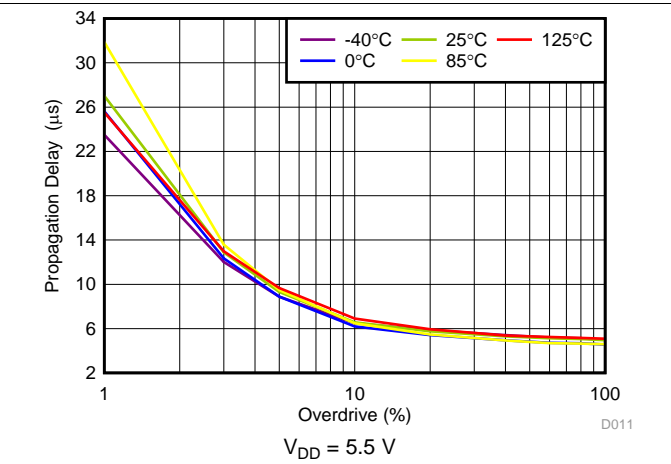


图 15. Propagation Delay ( $t_{\text{PD}(f)}$ ) vs Overdrive

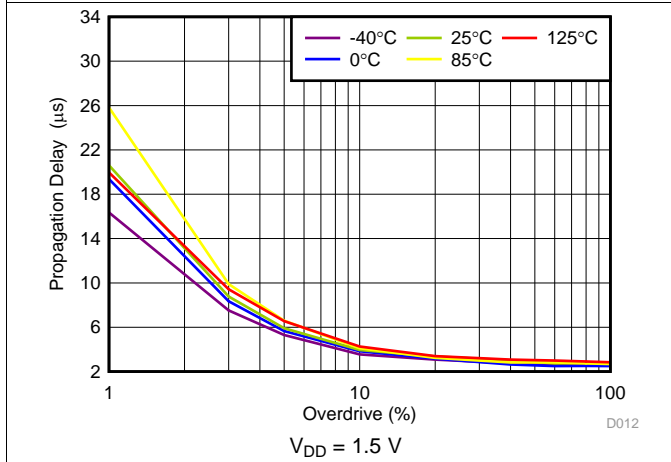


图 16. Propagation Delay ( $t_{\text{PD}(f)}$ ) vs Overdrive

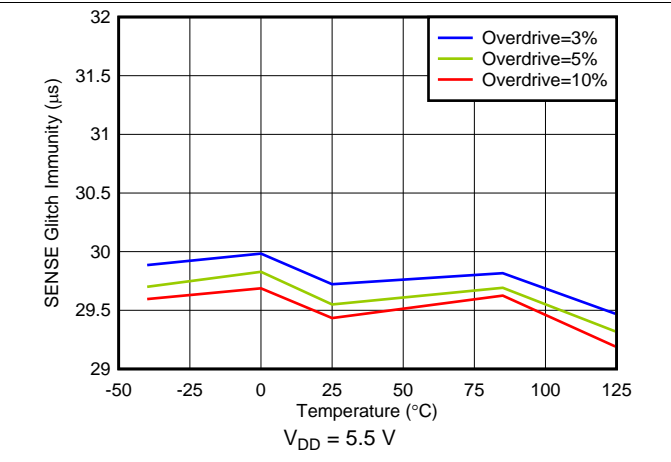


图 17. Low-to-High Glitch Immunity vs Temperature

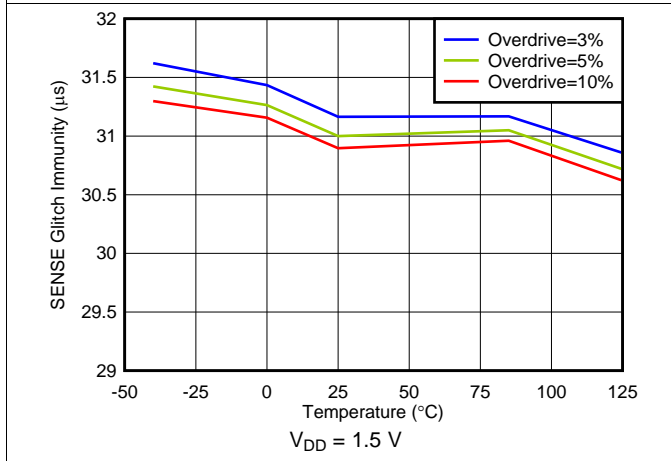


图 18. Low-to-High Glitch Immunity vs Temperature

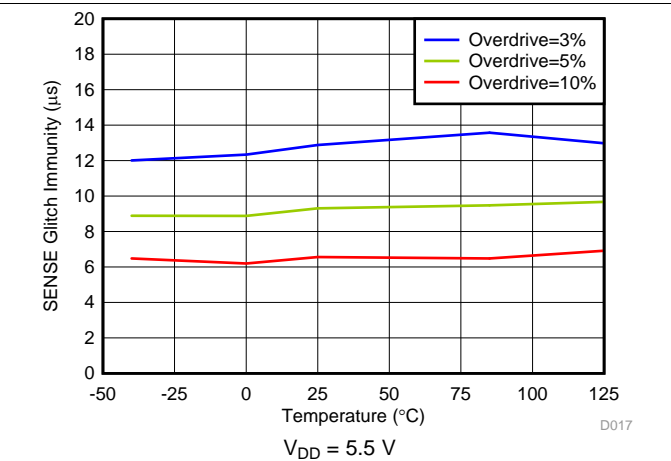


图 19. High-to-Low Glitch Immunity vs Temperature

Typical Characteristics (接下页)

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{\text{DD}}$  (unless otherwise noted)

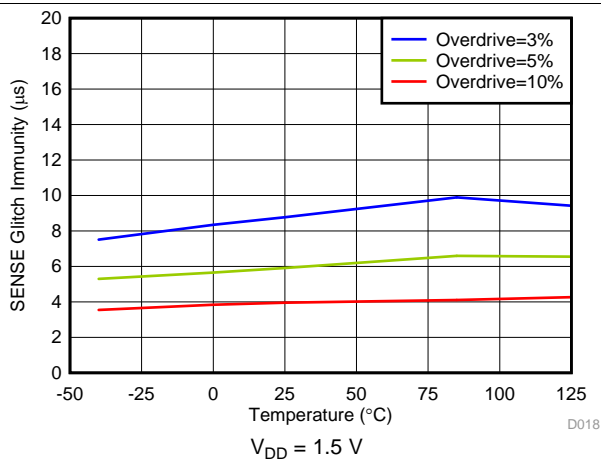


图 20. High-to-Low Glitch Immunity vs Temperature

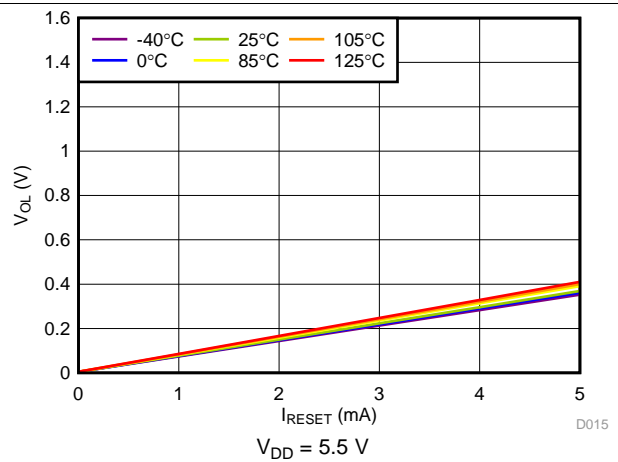


图 21. Low-Level Output Voltage vs RESET Current

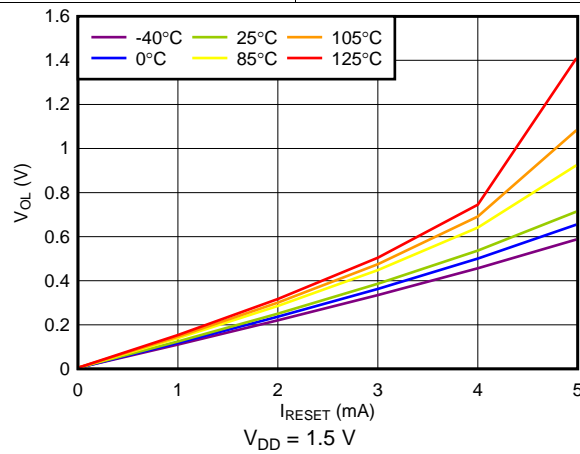


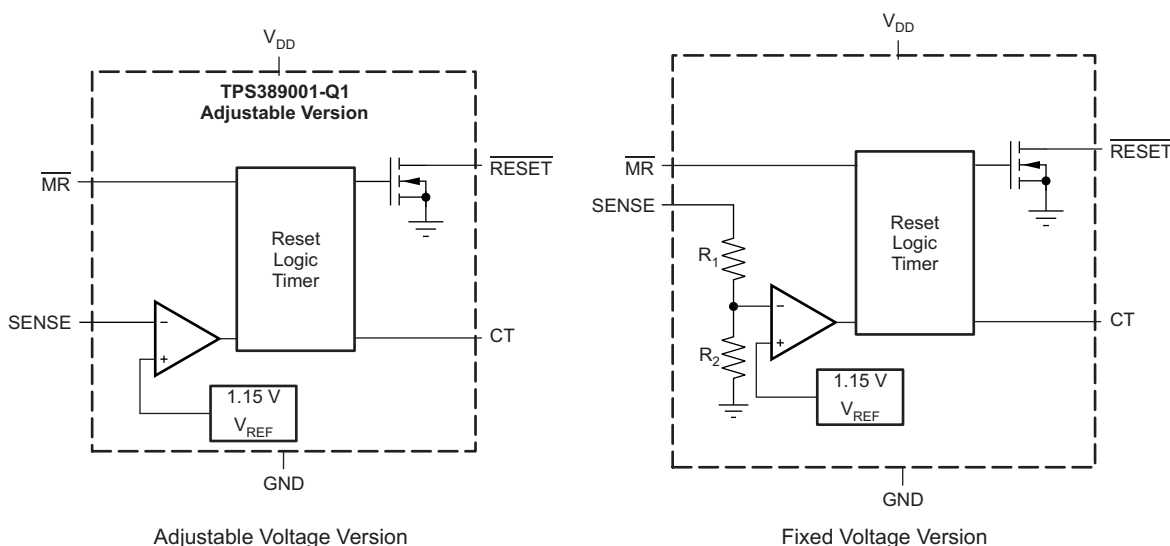
图 22. Low-Level Output Voltage vs RESET Current

## 8 Detailed Description

### 8.1 Overview

The TPS3890-Q1 supervisory product family is designed to assert a  $\overline{\text{RESET}}$  signal when either the SENSE pin voltage drops below  $V_{\text{ITN}}$  or the manual reset ( $\overline{\text{MR}}$ ) is driven low. The  $\overline{\text{RESET}}$  output remains asserted for a user-adjustable time after both the manual reset ( $\overline{\text{MR}}$ ) and SENSE voltages return above their respective thresholds.

### 8.2 Functional Block Diagram



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### 8.3 Feature Description

The combination of user-adjustable reset delay time with a broad range of threshold voltages allow these devices to be used in a wide array of applications. Fixed negative threshold voltages ( $V_{\text{ITN}}$ ) can be factory set from 1.15 V to 3.17 V (see the [Device Comparison Table](#) for available options), and the adjustable device can be used to customize the threshold voltage for other application needs by using an external resistor divider. The CT pin allows the reset delay to be set between 25  $\mu\text{s}$  and 30 s with the use of an external capacitor.

#### 8.3.1 User-Configurable $\overline{\text{RESET}}$ Delay Time

The rising  $\overline{\text{RESET}}$  delay time ( $t_{\text{PD}(r)}$ ) can be configured by installing a capacitor connected to the CT pin. The TPS3890-Q1 uses a CT pin charging current ( $I_{\text{CT}}$ ) of 1.15  $\mu\text{A}$  to help counter the effect of capacitor and board-level leakage currents that can be substantial in certain applications. The rising  $\overline{\text{RESET}}$  delay time can be set to any value between 25  $\mu\text{s}$  (no  $C_{\text{CT}}$  installed) and 30 s ( $C_{\text{CT}} = 26 \mu\text{F}$ ).

The capacitor value needed for a given delay time can be calculated using [公式 1](#):

$$t_{\text{PD}(r)} (\text{SEC}) = C_{\text{CT}} \times V_{\text{CT}} \div I_{\text{CT}} + t_{\text{PD}(r)(\text{nom})} \quad (1)$$

The slope of [公式 1](#) is determined by the time that the CT charging current ( $I_{\text{CT}}$ ) takes to charge the external capacitor up to the CT comparator threshold voltage ( $V_{\text{CT}}$ ). When  $\overline{\text{RESET}}$  is asserted, the capacitor is discharged through the internal CT pulldown resistor ( $R_{\text{CT}}$ ). When the  $\overline{\text{RESET}}$  conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor and when the voltage on this capacitor reaches 1.22 V,  $\overline{\text{RESET}}$  is deasserted. Note that in order to minimize the difference between the calculated  $\overline{\text{RESET}}$  delay time and the actual  $\overline{\text{RESET}}$  delay time, use a low-leakage type capacitor (such as a ceramic capacitor) and minimize parasitic board capacitance around this pin.

## Feature Description (接下页)

### 8.3.2 Manual Reset ( $\overline{\text{MR}}$ ) Input

The manual reset ( $\overline{\text{MR}}$ ) input allows a processor or other logic circuits to initiate a reset. A logic low on  $\overline{\text{MR}}$  causes  $\overline{\text{RESET}}$  to assert. After  $\overline{\text{MR}}$  returns to a logic high and  $\text{SENSE}$  is above  $V_{\text{ITP}}$ ,  $\overline{\text{RESET}}$  is deasserted after the user-defined reset delay. If  $\overline{\text{MR}}$  is not controlled externally, then  $\overline{\text{MR}}$  must be connected to  $V_{\text{DD}}$ . Note that if the logic signal driving  $\overline{\text{MR}}$  is not greater than or equal to  $V_{\text{DD}}$ , then some additional current flows into  $V_{\text{DD}}$  and out of  $\overline{\text{MR}}$  and the difference is apparent when comparing 图 8 and 图 9.

图 23 shows how  $\overline{\text{MR}}$  can be used to monitor multiple system voltages when only a single CT capacitor is needed to set the  $\overline{\text{RESET}}$  delay time.

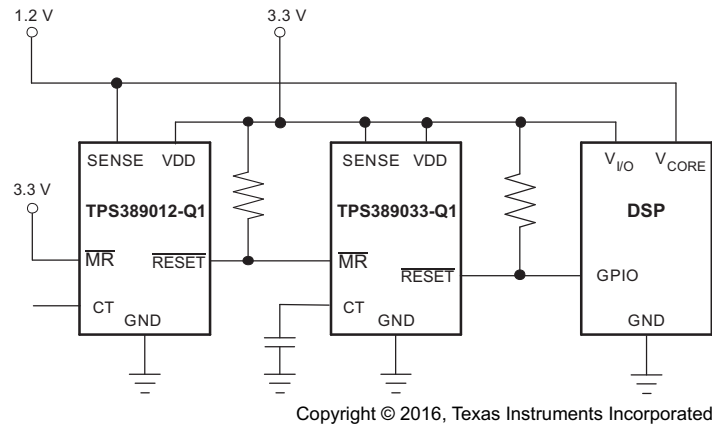


图 23. Using  $\overline{\text{MR}}$  to Monitor Multiple System Voltages

### 8.3.3 $\overline{\text{RESET}}$ Output

$\overline{\text{RESET}}$  remains high (deasserted) as long as  $\text{SENSE}$  is above the positive threshold ( $V_{\text{ITP}}$ ) and the manual reset signal ( $\overline{\text{MR}}$ ) is logic high. If  $\text{SENSE}$  falls below the negative threshold ( $V_{\text{ITN}}$ ) or if  $\overline{\text{MR}}$  is driven low, then  $\overline{\text{RESET}}$  is asserted, driving the  $\overline{\text{RESET}}$  pin to a low impedance.

When  $\overline{\text{MR}}$  is again logic high and  $\text{SENSE}$  is above  $V_{\text{ITP}}$ , a delay circuit is enabled that holds  $\overline{\text{RESET}}$  low for a specified reset delay period ( $t_{\text{PD}(r)}$ ). When the reset delay has elapsed, the  $\overline{\text{RESET}}$  pin goes to a high-impedance state and uses a pullup resistor to hold  $\overline{\text{RESET}}$  high. Connect the pullup resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level.  $\overline{\text{RESET}}$  can be pulled up to any voltage up to 5.5 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by  $V_{\text{OL}}$ , the output capacitive loading, and the output leakage current ( $I_{\text{LKG(OD)}}$ ).

### 8.3.4 SENSE Input

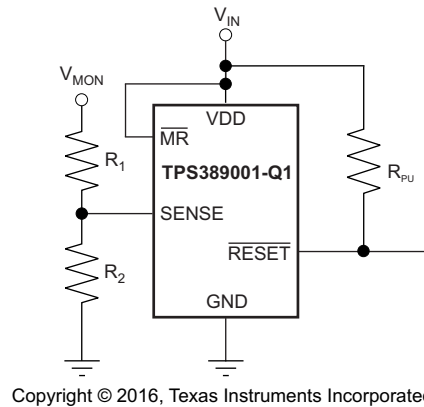
The  $\text{SENSE}$  input can vary from ground to 5.5 V (7.0 V, absolute maximum), regardless of the device supply voltage used. The  $\text{SENSE}$  pin is used to monitor the critical voltage rail. If the voltage on this pin drops below  $V_{\text{ITN}}$ , then  $\overline{\text{RESET}}$  is asserted. When the voltage on the  $\text{SENSE}$  pin exceeds the positive threshold voltage,  $\overline{\text{RESET}}$  deasserts after the user-defined  $\overline{\text{RESET}}$  delay time.

The internal comparator has built-in hysteresis to ensure well-defined  $\overline{\text{RESET}}$  assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3890-Q1 device is relatively immune to short transients on the  $\text{SENSE}$  pin. Glitch immunity is dependent on threshold overdrive, as illustrated in 图 19 for  $V_{\text{ITN}}$  and 图 18 for  $V_{\text{ITP}}$ . Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the  $\text{SENSE}$  input to reduce sensitivity to transient voltages on the monitored signal.

## Feature Description (接下页)

The adjustable version (TPS389001-Q1) can be used to monitor any voltage rail down to 1.15 V using the circuit shown in 图 24.



**图 24. Using the TPS389001-Q1 to Monitor a User-Defined Threshold Voltage**

The target threshold voltage for the monitored supply ( $V_{ITx(MON)}$ ) and the resistor divider values can be calculated by using 公式 2 and 公式 3, respectively:

$$V_{ITx(MON)} = V_{ITx} \times (1 + R_1 \div R_2) \quad (2)$$

公式 3 can be used to calculate either the negative threshold or the positive threshold by replacing  $V_{ITx}$  with either  $V_{ITN}$  or  $V_{ITP}$ , respectively.

$$R_{TOTAL} = R_1 + R_2 \quad (3)$$

Resistors with high values minimize current consumption; however, the input bias current of the device degrades accuracy if the current through the resistors is too low. Therefore, choosing an  $R_{TOTAL}$  value so that the current through the resistor divider is at least 100 times larger than the SENSE input current is simplest. See the [Optimizing Resistor Dividers at a Comparator Input](#) application report for more details on sizing input resistors.

### 8.3.4.1 Immunity to SENSE Pin Voltage Transients

The TPS3890-Q1 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient. Overdrive is defined by how much  $V_{SENSE}$  exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs (that is, undervoltage and overvoltage). Threshold overdrive is calculated as a percent of the threshold in question, as shown in 公式 4.

$$\text{Overdrive} = | (V_{SENSE} / V_{ITx} - 1) \times 100\% | \quad (4)$$

图 17 to 图 20 illustrate the glitch immunity that the TPS3890-Q1 has versus temperature with three different overdrive voltages. The propagation delay versus overdrive curves (图 13 to 图 16) can be used to determine how sensitive the TPS3890-Q1 family of devices are across an even wider range of overdrive voltages.

## 8.4 Device Functional Modes

表 1 summarizes the various functional modes of the device.

表 1. Truth Table

| $V_{DD}$                               | $\overline{MR}$ | SENSE                 | $\overline{RESET}$ |
|--|-----------------|-----------------------|--------------------|
| $V_{DD} < V_{POR}$                     | —               | —                     | Undefined          |
| $V_{POR} < V_{DD} < V_{DD(MIN)}^{(1)}$ | —               | —                     | L                  |
| $V_{DD} \geq V_{DD(MIN)}$              | L               | —                     | L                  |
| $V_{DD} \geq V_{DD(MIN)}$              | H               | $V_{SENSE} < V_{ITN}$ | L                  |
| $V_{DD} \geq V_{DD(MIN)}$              | H               | $V_{SENSE} > V_{ITP}$ | H                  |

(1) When  $V_{DD}$  falls below  $V_{DD(MIN)}$ , undervoltage-lockout (UVLO) takes effect and  $\overline{RESET}$  is held low until  $V_{DD}$  falls below  $V_{POR}$ .

### 8.4.1 Normal Operation ( $V_{DD} > V_{DD(min)}$ )

When  $V_{DD}$  is greater than  $V_{DD(min)}$ , the  $\overline{RESET}$  signal is determined by the voltage on the SENSE pin and the logic state of  $\overline{MR}$ .

- $\overline{MR}$  high: when the voltage on  $V_{DD}$  is greater than 1.5 V, the  $\overline{RESET}$  signal corresponds to the voltage on the SENSE pin relative to the threshold voltage.
- $\overline{MR}$  low: in this mode,  $\overline{RESET}$  is held low regardless of the voltage on the SENSE pin.

### 8.4.2 Above Power-On-Reset But Less Than $V_{DD(min)}$ ( $V_{POR} < V_{DD} < V_{DD(min)}$ )

When the voltage on  $V_{DD}$  is less than the  $V_{DD(min)}$  voltage, and greater than the power-on-reset voltage ( $V_{POR}$ ), the  $\overline{RESET}$  signal is asserted regardless of the voltage on the SENSE pin.

### 8.4.3 Below Power-On-Reset ( $V_{DD} < V_{POR}$ )

When the voltage on  $V_{DD}$  is lower than  $V_{POR}$ , the device does not have enough voltage to internally pull the asserted output low and  $\overline{RESET}$  is undefined and must not be relied upon for proper device function.

## 9 Application and Implementation

### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

### 9.2 Typical Application

A typical application for the TPS389018-Q1 is shown in 图 25. The TPS389018-Q1 can be used to monitor the 1.8-V VDD rail required by the TI Delfino™ microprocessor family. The open-drain RESET output of the TPS389018-Q1 is connected to the XRS input of the microprocessor. A reset event is initiated when the VDD voltage is less than  $V_{ITN}$  or when MR is driven low by an external source.

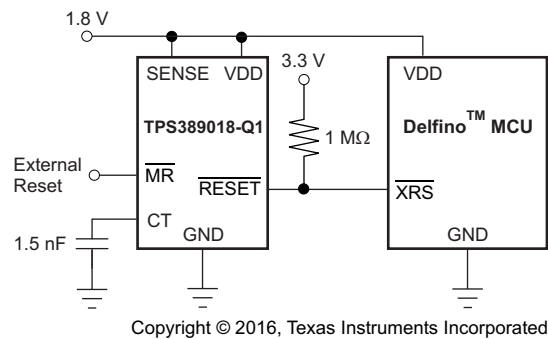


图 25. TPS3890-Q1 Monitoring the Supply Voltage for a Delfino Microprocessor

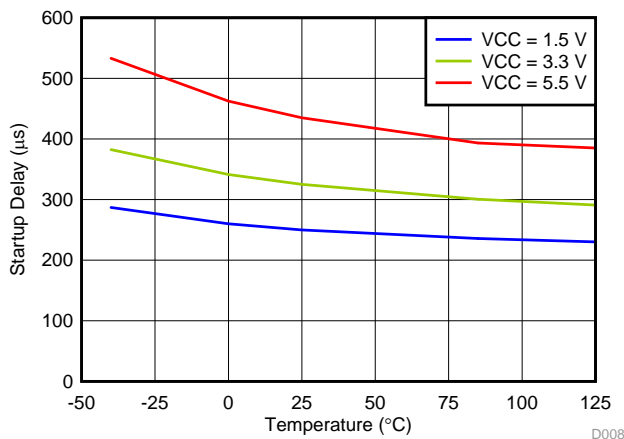
#### 9.2.1 Design Requirements

The TPS3890-Q1 RESET output can be used to drive the reset (XRS) input of a microprocessor. The RESET pin of the TPS3890-Q1 is pulled high with a 1-MΩ resistor; the reset delay time is controlled by the CT capacitor and is set depending on the reset requirement times of the microprocessor. During power-up, XRS must remain low for at least 1 ms after VDD reaches 1.5 V for the C2000™ Delfino family of microprocessors. For 100-MHz operation, the Delfino TMS320F2833x microcontroller uses a supply voltage of 1.8 V that must be monitored by the TPS3890-Q1.

#### 9.2.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS389018-Q1 has a negative threshold of 1.73 V and a positive threshold of 1.74 V, making the device suitable for monitoring a 1.8-V rail. The secondary constraint for this application is the reset delay time that must be at least 1 ms to allow the Delfino microprocessor enough time to startup up correctly. Because a minimum time is required, the worst-case scenario is a supervisor with a high CT charging current ( $I_{CT}$ ) and a low CT comparator threshold ( $V_{CT}$ ). For applications with ambient temperatures ranging from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $C_{CT}$  can be calculated using  $I_{CT(\text{Max})}$ ,  $V_{CT(\text{MIN})}$ , and solving for  $C_{CT}$  in 公式 1 such that the minimum capacitance required at the CT pin is 1.149 nF. If standard capacitors with  $\pm 20\%$  tolerances are used, then the CT capacitor must be 1.5 nF or larger to ensure that the 1-ms delay time is met.

A 0.1-μF decoupling capacitor is connected to the VDD pin as a good analog design practice and a 1-MΩ resistor is used as the RESET pullup resistor to minimize the current consumption when RESET is asserted. The MR pin can be connected to an external signal if desired or connected to VDD if not used.

**Typical Application (接下页)**
**9.2.3 Application Curve**

**图 26. Startup Delay vs Temperature**
**10 Power Supply Recommendations**

These devices are designed to operate from an input supply with a voltage range between 1.5 V and 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1- $\mu$ F capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.



## 11 Layout

### 11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1- $\mu$ F ceramic capacitor near the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the  $\overline{\text{RESET}}$  delay time is not adversely affected.

### 11.2 Layout Example

The layout example in shows how the TPS3890-Q1 is laid out on a printed circuit board (PCB) with a user-defined delay.

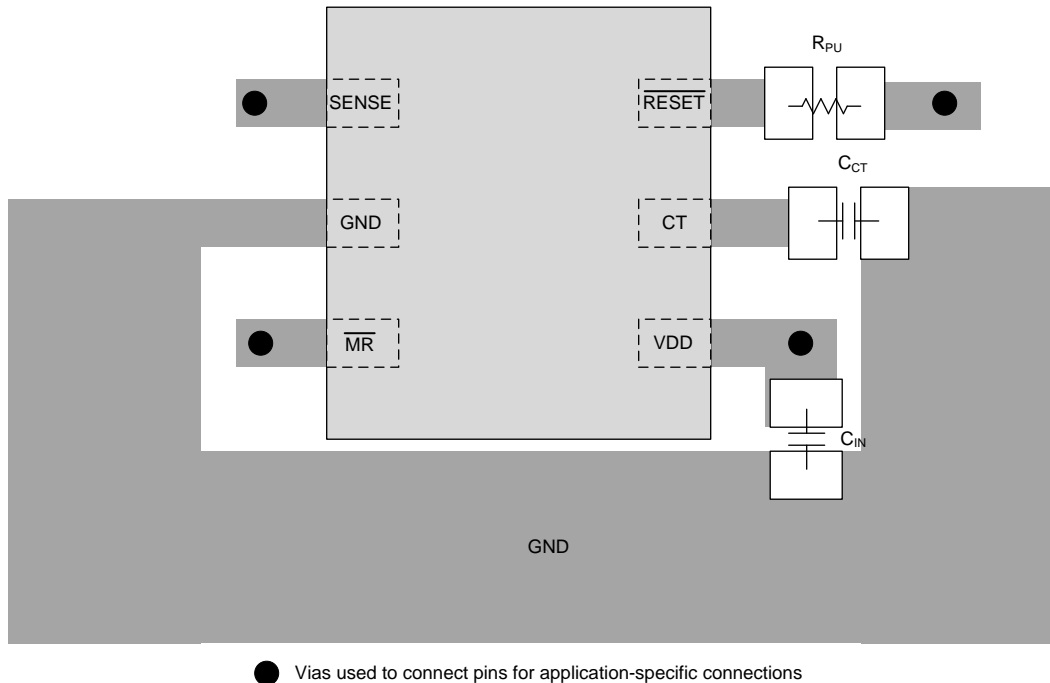


图 27. Recommended Layout

## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 器件命名规则

表 2 以 TPS389033G-Q1 为例，介绍了如何根据器件编号来解译器件的功能。

表 2. 器件命名约定

| 说明                            | 命名规则 | 值    |
|-------------------------------|------|------|
| TPS3890<br>(高精度监控器系列)         | —    | —    |
| 33<br>(拟监控的标称轨电压)             | 10   | 1.0V |
|                               | 12   | 1.2V |
|                               | 18   | 1.8V |
|                               | 33   | 3.3V |
|                               | 50   | 5.0V |
| G<br>( $V_{ITN}$ 低于标称轨电压的百分比) | —    | 4%   |
|                               | G    | 7%   |
|                               | K    | 11%  |
|                               | L    | 12%  |
| Q1<br>(汽车版本)                  | —    | —    |

### 12.2 文档支持

#### 12.2.1 相关文档

如需相关文档，请参阅：

- [《优化比较器输入上的电阻分压器》](#)
- [《电源设计灵敏度分析》](#)
- [《TMS320C28x 数字信号控制器入门》](#)
- [《TPS3890EVM-775 评估模块用户指南》](#)
- [C2000 Delfino 系列微处理器](#)
- [《TMS320F2833x 数字信号控制器 \(DSC\)》](#)

#### 12.3 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。请单击右上角的提醒我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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## 12.5 商标

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## 12.6 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，也不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

**PACKAGING INFORMATION**

| Orderable part number             | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-----------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS389001QDSERQ1</a>  | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2N                  |
| TPS389001QDSERQ1.B                | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2N                  |
| <a href="#">TPS389012QDSERQ1</a>  | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2O                  |
| TPS389012QDSERQ1.B                | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2O                  |
| <a href="#">TPS389015QDSERQ1</a>  | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2P                  |
| TPS389015QDSERQ1.B                | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2P                  |
| <a href="#">TPS389018QDSERQ1</a>  | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2Q                  |
| TPS389018QDSERQ1.B                | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2Q                  |
| <a href="#">TPS389025QDSERQ1</a>  | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2R                  |
| TPS389025QDSERQ1.B                | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2R                  |
| <a href="#">TPS389030QDSERQ1</a>  | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2S                  |
| TPS389030QDSERQ1.B                | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2S                  |
| <a href="#">TPS389033GQDSERQ1</a> | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7V                  |
| TPS389033GQDSERQ1.B               | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7V                  |
| <a href="#">TPS389033KQDSERQ1</a> | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7W                  |
| TPS389033KQDSERQ1.B               | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7W                  |
| <a href="#">TPS389033QDSERQ1</a>  | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2T                  |
| TPS389033QDSERQ1.B                | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 2T                  |
| <a href="#">TPS389050GQDSERQ1</a> | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7T                  |
| TPS389050GQDSERQ1.B               | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7T                  |
| <a href="#">TPS389050LQDSERQ1</a> | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7U                  |
| TPS389050LQDSERQ1.B               | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7U                  |
| <a href="#">TPS389050QDSERQ1</a>  | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7S                  |
| TPS389050QDSERQ1.B                | Active        | Production           | WSON (DSE)   6 | 3000   LARGE T&R      | Yes         | NIPDAUAG                             | Level-1-260C-UNLIM                | -40 to 125   | 7S                  |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TPS3890-Q1 :**

- Catalog : [TPS3890](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



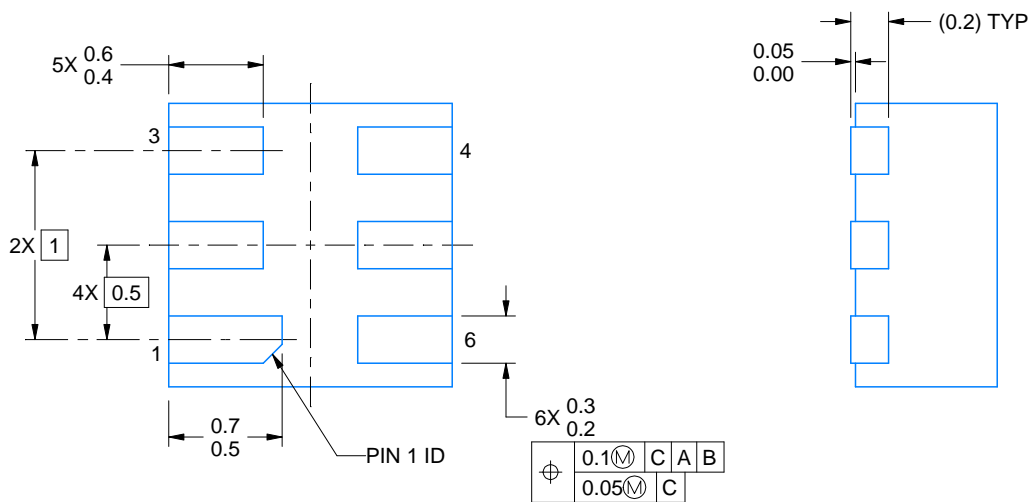
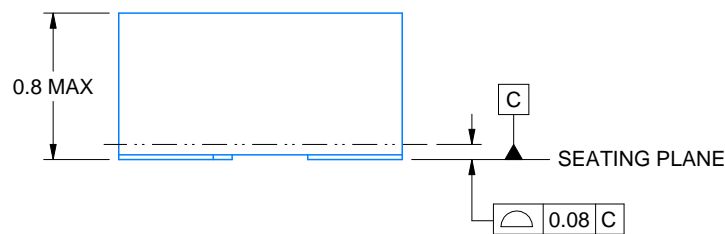
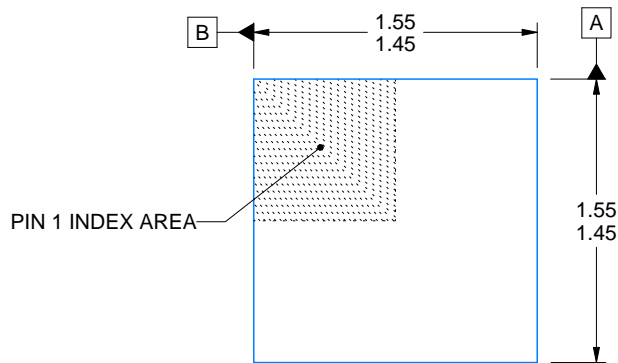
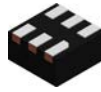
\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS389001QDSERQ1  | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389012QDSERQ1  | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389015QDSERQ1  | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389018QDSERQ1  | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389025QDSERQ1  | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389030QDSERQ1  | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389033GQDSERQ1 | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389033KQDSERQ1 | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389033QDSERQ1  | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389050GQDSERQ1 | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389050LQDSERQ1 | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |
| TPS389050QDSERQ1  | WSON         | DSE             | 6    | 3000 | 180.0              | 8.4                | 1.83    | 1.83    | 0.89    | 4.0     | 8.0    | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS389001QDSERQ1  | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389012QDSERQ1  | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389015QDSERQ1  | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389018QDSERQ1  | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389025QDSERQ1  | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389030QDSERQ1  | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389033GQDSERQ1 | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389033KQDSERQ1 | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389033QDSERQ1  | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389050GQDSERQ1 | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389050LQDSERQ1 | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |
| TPS389050QDSERQ1  | WSON         | DSE             | 6    | 3000 | 183.0       | 183.0      | 20.0        |



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

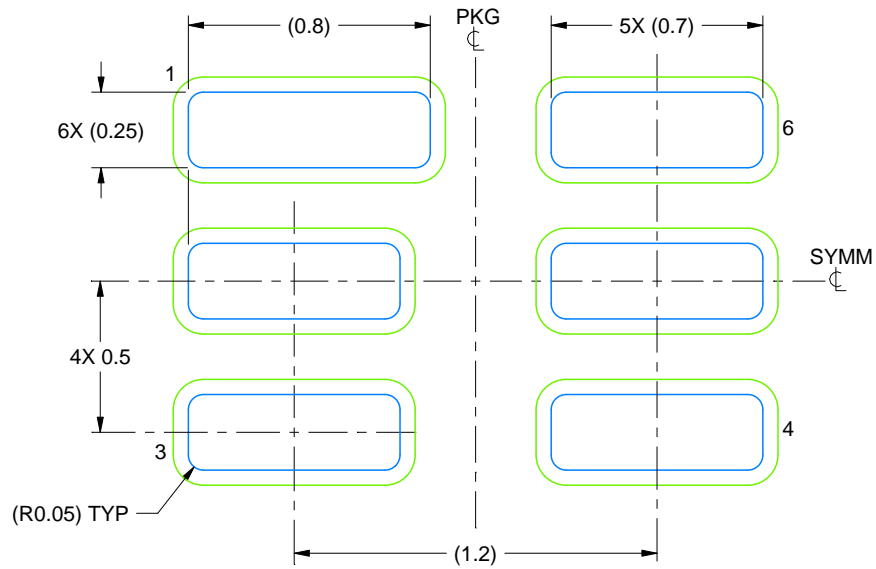


# EXAMPLE BOARD LAYOUT

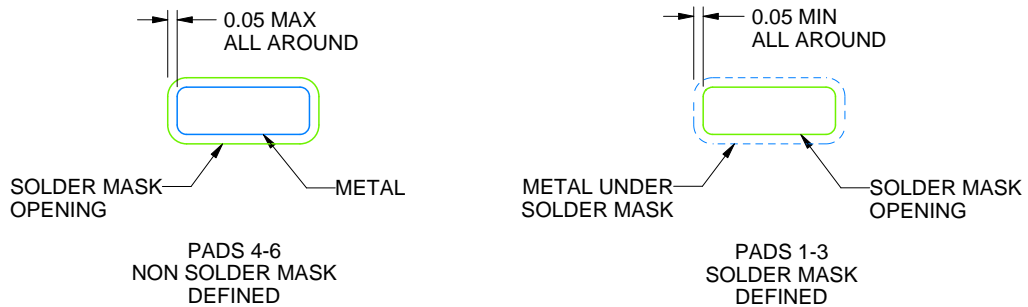
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS

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NOTES: (continued)

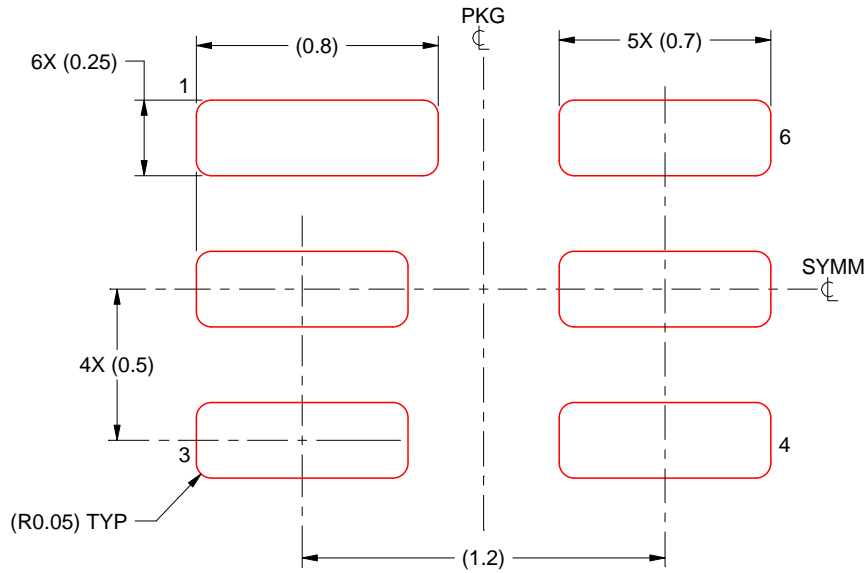
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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