

# 具有可调节延迟和看门狗计时器的 TPS386000 和 TPS386040 四路电源电压监视器

## 1 特性

- 4 个独立的电压监视器
- 通道 1:
  - 低至 0.4V 的可调节阈值
  - 手动复位 ( $\overline{\text{MR}}$ ) 输入
- 通道 2、3:
  - 低至 0.4V 的可调节阈值
- 通道 4:
  - 任何正或负电压的调节阈值
  - 窗口比较器
- 可调节复位延迟时间: 1.4ms 至 10s
- 阈值精度: 0.25% (典型值)
- 超低静态电流: 11 $\mu\text{A}$  (典型值)
- 具有专用输出的看门狗计时器
- 可在上电期间很好地控制输出
- TPS386000: 漏极开路  $\overline{\text{RESETn}}$  和  $\overline{\text{WDO}}$
- TPS386040: 推挽  $\overline{\text{RESETn}}$  和  $\overline{\text{WDO}}$
- 封装: 4mm × 4mm 20 引脚 VQFN

## 2 应用

- 所有 DSP 和微控制器 应用
- 所有 FPGA 和 ASIC 应用
- 电信和无线基础设施
- 工业设备
- 模拟定序

## 3 说明

TPS3860x0 系列电源监视器 (SVS) 可以在 0.25% (典型值) 的阈值精度下监控 4 个高于 0.4V 的电源轨和 1 个低于 0.4V (包括负电压) 的电源轨。当 SENSEm 输入电压下降至编程阈值以下时, 4 个监视电路中的每一个 (SVS-n) 都会给出  $\overline{\text{RESETn}}$  或  $\text{RESETn}$  输出信号。您可以使用外部电阻器对各个 SVS-n 的阈值进行编程 (其中  $n = 1、2、3、4$ ,  $m = 1、2、3、4\text{L}$ 、4H)。

每个 SVS-n 都具有释放  $\overline{\text{RESETn}}$  或  $\text{RESETn}$  之前的可编程延迟。您可以通过 CTn 引脚连接独立设置各个 SVS 的延迟时间, 允许的取值范围为 1.4ms 至 10s。只有 SVS-1 具有低电平有效手动复位 ( $\overline{\text{MR}}$ ) 输入; 当  $\overline{\text{MR}}$  得到的是逻辑低电平输入时, 会给出  $\overline{\text{RESET1}}$  或  $\text{RESET1}$ 。

SVS-4 使用两个比较器来监控阈值窗口。您可以将额外的比较器配置为第五个 SVS, 以通过电压基准输出 VREF 来监控负电压。

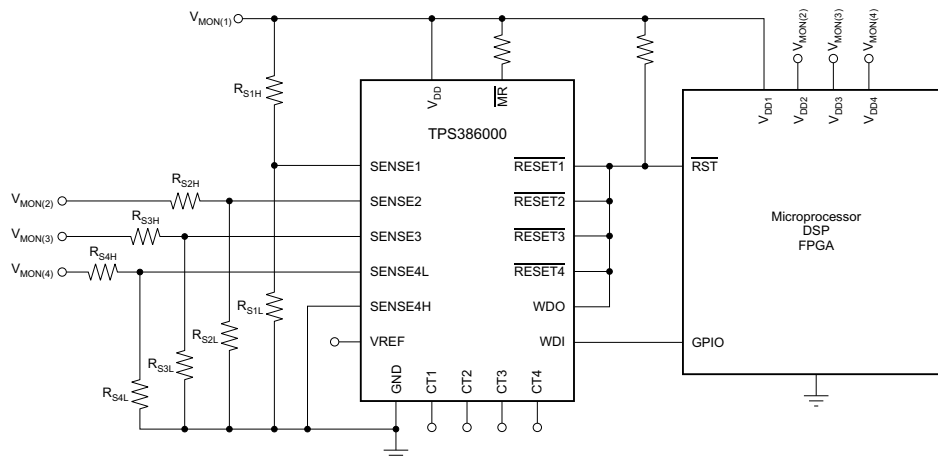
TPS3860x0 具有 11 $\mu\text{A}$  (典型值) 的超低静态电流, 且采用了小型 4mm × 4mm VQFN-20 封装。

器件信息<sup>(1)</sup>

| 器件型号      | 封装        | 封装尺寸 (标称值)      |
|-----------|-----------|-----------------|
| TPS3860x0 | VQFN (20) | 4.00mm × 4.00mm |

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

TPS386000 典型应用电路:  
监控 FPGA 的电源



## 目录

|     |                                         |    |      |                                      |    |
|-----|-----------------------------------------|----|------|--------------------------------------|----|
| 1   | 特性 .....                                | 1  | 8.3  | Feature Description .....            | 22 |
| 2   | 应用 .....                                | 1  | 8.4  | Device Functional Modes .....        | 23 |
| 3   | 说明 .....                                | 1  | 9    | Application and Implementation ..... | 25 |
| 4   | 修订历史记录 .....                            | 2  | 9.1  | Application Information .....        | 25 |
| 5   | Pin Configuration and Functions .....   | 4  | 9.2  | Typical Application .....            | 28 |
| 6   | Specifications .....                    | 6  | 10   | Power Supply Recommendations .....   | 29 |
| 6.1 | Absolute Maximum Ratings .....          | 6  | 11   | Layout .....                         | 30 |
| 6.2 | ESD Ratings .....                       | 6  | 11.1 | Layout Guidelines .....              | 30 |
| 6.3 | Recommended Operating Conditions .....  | 6  | 11.2 | Layout Example .....                 | 30 |
| 6.4 | Thermal Information .....               | 6  | 12   | 器件和文档支持 .....                        | 31 |
| 6.5 | Electrical Characteristics .....        | 7  | 12.1 | 器件支持 .....                           | 31 |
| 6.6 | Timing Requirements .....               | 8  | 12.2 | 文档支持 .....                           | 31 |
| 6.7 | Switching Characteristics .....         | 8  | 12.3 | 相关链接 .....                           | 31 |
| 6.8 | Typical Characteristics .....           | 14 | 12.4 | 社区资源 .....                           | 32 |
| 7   | Parameter Measurement Information ..... | 18 | 12.5 | 商标 .....                             | 32 |
| 8   | Detailed Description .....              | 19 | 12.6 | 静电放电警告 .....                         | 32 |
| 8.1 | Overview .....                          | 19 | 12.7 | 术语表 .....                            | 32 |
| 8.2 | Functional Block Diagrams .....         | 20 | 13   | 机械、封装和可订购信息 .....                    | 32 |

## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

| Changes from Revision E (October 2015) to Revision F                                                                                                                                                                     | Page |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed the text in the <i>Power Supply Recommendations</i> section from: This power supply should be less than 1.8 V in normal operation to: This power supply should not be less than 1.8 V in normal operation..... | 29   |

| Changes from Revision D (September 2013) to Revision E                                                                                                                                                                | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • 已添加 <i>ESD</i> 额定值表、特性说明部分、器件功能模式、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 .....                                                                                                                                | 1    |
| • 已更改有关通道 1、2、3 和 4 的“特性”项目 .....                                                                                                                                                                                     | 1    |
| • Changed all references of $V_{CC}$ (and $I_{CC}$ ) to $V_{DD}$ ( and $I_{DD}$ ) throughout the document .....                                                                                                       | 4    |
| • Changed the description of SENSE4L pin function .....                                                                                                                                                               | 4    |
| • Changed the description of SENSE4H pin function .....                                                                                                                                                               | 4    |
| • Changed the description of $\overline{MR}$ pin function .....                                                                                                                                                       | 4    |
| • Changed the description of WDI pin function .....                                                                                                                                                                   | 4    |
| • Moved ESD ratings from the <i>Absolute Maximum Ratings</i> table to the <i>ESD Ratings</i> table .....                                                                                                              | 6    |
| • Deleted the <i>Dissipation Ratings</i> table and added the <i>Thermal Information</i> table .....                                                                                                                   | 6    |
| • Moved timing and switching parameters ( $t_W$ , $t_D$ , $t_{WDT}$ ) from the <i>Electrical Characteristics</i> table to the respective <i>Timing Requirements</i> and <i>Switching Characteristics</i> tables ..... | 8    |
| • Changed the x-axis title notation from $CT$ to $CTn$ in the <i>TPS386040 RESETn Time-out Period vs CTn</i> graph .....                                                                                              | 14   |
| • Changed the <i>Watchdog Timer (WDT) Truth Table</i> ; deleted <i>RESET</i> condition column heading .....                                                                                                           | 24   |
| • Changed title of <i>SENSE INPUT</i> section to <i>Undervoltage Detection</i> .....                                                                                                                                  | 25   |
| • Changed Equation 1, Equation 2, and Equation 3 $V_{CC}$ notations to $V_{MON}$ .....                                                                                                                                | 25   |
| • Changed title of <i>Window Comparator</i> section to <i>Undervoltage and Overvoltage Detection</i> .....                                                                                                            | 25   |
| • Changed $V_{CC4}$ reference in first paragraph of <i>Undervoltage and Overvoltage Detection</i> section to $V_{MON(4)}$ .....                                                                                       | 25   |
| • Changed Equation 4 and Equation 5 $V_{CC4}$ references to $V_{MON(4)}$ .....                                                                                                                                        | 25   |
| • Changed the <i>SVS-4: Window Comparator</i> image .....                                                                                                                                                             | 25   |
| • Added $V_{CC}$ to $V_{MON(4)}$ in the <i>Window Comparator Operation</i> image .....                                                                                                                                | 26   |

|                                                                                                                   |    |
|-------------------------------------------------------------------------------------------------------------------|----|
| • Changed title of <i>Sensing Voltage Less Than 0.4 V</i> to <i>Sensing a Negative Voltage</i> .....              | 26 |
| • Changed <a href="#">Equation 6</a> and <a href="#">Equation 7</a> references to $V_{CC4}$ to $V_{MON(4)}$ ..... | 26 |
| • Changed the SVS4: <i>Negative Voltage Sensing</i> image .....                                                   | 26 |

|                                                            |             |
|------------------------------------------------------------|-------------|
| <b>Changes from Revision C (August 2011) to Revision D</b> | <b>Page</b> |
|------------------------------------------------------------|-------------|

|                                           |   |
|-------------------------------------------|---|
| • 从数据表中删除了 TPS386020 和 TPS386060 器件 ..... | 1 |
|-------------------------------------------|---|

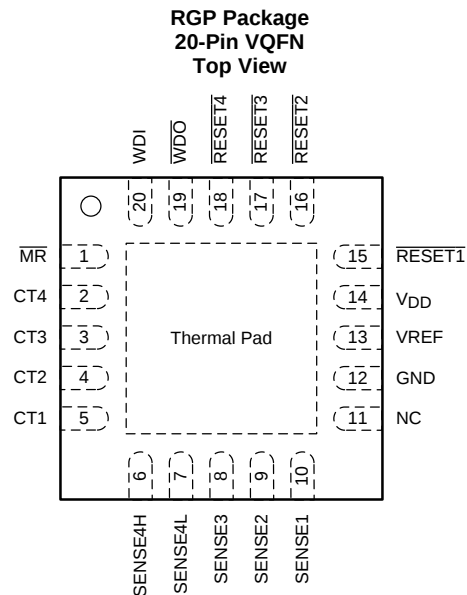
|                                                           |             |
|-----------------------------------------------------------|-------------|
| <b>Changes from Revision B (March 2011) to Revision C</b> | <b>Page</b> |
|-----------------------------------------------------------|-------------|

|                                           |    |
|-------------------------------------------|----|
| • Changed <a href="#">Figure 31</a> ..... | 21 |
|-------------------------------------------|----|

|                                                             |             |
|-------------------------------------------------------------|-------------|
| <b>Changes from Revision A (January 2010) to Revision B</b> | <b>Page</b> |
|-------------------------------------------------------------|-------------|

|                                                                                                                            |    |
|----------------------------------------------------------------------------------------------------------------------------|----|
| • 更改了数据表标题 .....                                                                                                           | 1  |
| • 更改了 特性 项目 .....                                                                                                          | 1  |
| • 已更改 应用 要点 .....                                                                                                          | 1  |
| • 更改了“说明”文本中第二段的第一句 .....                                                                                                  | 1  |
| • 在“说明”文本的最后一段中将低静态电流值从 12 $\mu$ A 更改为 11 $\mu$ A .....                                                                    | 1  |
| • 更改了首页的典型应用电路图 .....                                                                                                      | 1  |
| • Added sentence to pin 6 description in Pin Assignments table.....                                                        | 4  |
| • Changed last sentence of pin 13 description in Pin Assignments table.....                                                | 4  |
| • Added text to first sentence of first paragraph of <i>General Description</i> section. ....                              | 22 |
| • Changed link in <i>Window Comparator</i> section to new <a href="#">Figure 32</a> .....                                  | 25 |
| • Deleted typo in <a href="#">Equation 4</a> and moved <a href="#">Equation 4</a> to <i>Window Comparator</i> section..... | 25 |
| • Deleted typo in <a href="#">Equation 5</a> and moved <a href="#">Equation 5</a> to <i>Window Comparator</i> section..... | 25 |
| • Added <a href="#">Figure 32</a> .....                                                                                    | 25 |
| • Changed link in <i>Sensing Voltage Less Than 0.4V</i> section to new <a href="#">Figure 34</a> .....                     | 26 |
| • Added <a href="#">Figure 34</a> .....                                                                                    | 26 |
| • Changed caption for <a href="#">Figure 35</a> .....                                                                      | 28 |

## 5 Pin Configuration and Functions



### Pin Functions

| PIN             |     | I/O | DESCRIPTION                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                   |
|-----------------|-----|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME            | NO. |     |                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                   |
| V <sub>DD</sub> | 14  | I   | Supply voltage. TI recommends connecting a 0.1-μF ceramic capacitor close to this pin.                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                   |
| GND             | 12  | —   | Ground                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                   |
| SENSE1          | 10  | I   | Monitor voltage input to SVS-1                                                                                                                                                                                                                                                                                  | When the voltage at this terminal drops below the threshold voltage (V <sub>ITN</sub> ), RESET1 is asserted.                                                                                                                                                                                                                      |
| SENSE2          | 9   | I   | Monitor voltage input to SVS-2                                                                                                                                                                                                                                                                                  | When the voltage at this terminal drops below the threshold voltage (V <sub>ITN</sub> ), RESET2 is asserted.                                                                                                                                                                                                                      |
| SENSE3          | 8   | I   | Monitor voltage input to SVS-3                                                                                                                                                                                                                                                                                  | When the voltage at this terminal drops below the threshold voltage (V <sub>ITN</sub> ), RESET3 is asserted.                                                                                                                                                                                                                      |
| SENSE4L         | 7   | I   | Falling monitor voltage input to SVS-4. When the voltage at this terminal drops below the threshold voltage (V <sub>ITN</sub> ), RESET4 is asserted.                                                                                                                                                            |                                                                                                                                                                                                                                                                                                                                   |
| SENSE4H         | 6   | I   | Rising monitor voltage input to SVS-4. When the voltage at this terminal exceeds the threshold voltage (V <sub>ITP</sub> ), RESET4 is asserted. This pin can also be used to monitor the negative voltage rail in combination with VREF pin. Connect to GND if not being used.                                  |                                                                                                                                                                                                                                                                                                                                   |
| CT1             | 5   | —   | Reset delay programming pin for SVS-1                                                                                                                                                                                                                                                                           | Connecting this pin to V <sub>DD</sub> through a 40-kΩ to 200-kΩ resistor, or leaving it open, selects a fixed delay time (see the <a href="#">Electrical Characteristics</a> ). Connecting a capacitor > 220 pF between this pin and GND selects the programmable delay time (see the <a href="#">Reset Delay Time</a> section). |
| CT2             | 4   | —   | Reset delay programming pin for SVS-2                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                   |
| CT3             | 3   | —   | Reset delay programming pin for SVS-3                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                   |
| CT4             | 2   | —   | Reset delay programming pin for SVS-4                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                   |
| VREF            | 13  | O   | Reference voltage output. By connecting a resistor network between this pin and the negative power rail, SENSE4H can monitor the negative power rail. This pin is intended to only source current into resistor(s). Do not connect resistor(s) to a voltage higher than 1.2 V. Do not connect only a capacitor. |                                                                                                                                                                                                                                                                                                                                   |
| MR              | 1   | I   | Manual reset input for SVS-1. Logic low level of this pin asserts RESET1.                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                   |
| WDI             | 20  | I   | Watchdog timer (WDT) trigger input. Inputting either a positive or negative logic edge every 610 ms (typical) prevents WDT time out at the WDO or WDO pin. Timer starts from releasing event of RESET1.                                                                                                         |                                                                                                                                                                                                                                                                                                                                   |
| NC              | 11  | —   | Not internal connection. TI recommends connecting this pin to the GND pin (pin 12), which is next to this pin.                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                   |
| Thermal Pad     | PAD | —   | This pad is the IC substrate. This pad must be connected only to GND or to the floating thermal pattern on the printed-circuit board (PCB).                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                   |

### Pin Functions (continued)

| PIN       |     | I/O | DESCRIPTION                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                  |
|-----------|-----|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME      | NO. |     |                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                  |
| TPS386000 |     |     |                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                  |
| RESET1    | 15  | O   | Active low reset output of SVS-1                                                                                                                                                                   | RESETn is an open-drain output pin. When RESETn is asserted, this pin remains in a low-impedance state. When RESETn is released, this pin goes to a high-impedance state after the delay time programmed by CTn. A pullup resistor to VDD or another voltage source is required. |
| RESET2    | 16  | O   | Active low reset output of SVS-2                                                                                                                                                                   |                                                                                                                                                                                                                                                                                  |
| RESET3    | 17  | O   | Active low reset output of SVS-3                                                                                                                                                                   |                                                                                                                                                                                                                                                                                  |
| RESET4    | 18  | O   | Active low reset output of SVS-4                                                                                                                                                                   |                                                                                                                                                                                                                                                                                  |
| WDO       | 19  | O   | Watchdog timer output. This is an open-drain output pin. When WDT times out, this pin goes to a low-impedance state to GND. If there is no WDT time-out, this pin stays in a high-impedance state. |                                                                                                                                                                                                                                                                                  |
| TPS386040 |     |     |                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                  |
| RESET1    | 15  | O   | Active low reset output of SVS-1                                                                                                                                                                   | RESETn is a push-pull logic buffer output pin. When RESETn is asserted, this pin remains logic low. When RESETn is released, this pin goes to logic high after the delay time programmed by CTn.                                                                                 |
| RESET2    | 16  | O   | Active low reset output of SVS-2                                                                                                                                                                   |                                                                                                                                                                                                                                                                                  |
| RESET3    | 17  | O   | Active low reset output of SVS-3                                                                                                                                                                   |                                                                                                                                                                                                                                                                                  |
| RESET4    | 18  | O   | Active low reset output of SVS-4                                                                                                                                                                   |                                                                                                                                                                                                                                                                                  |
| WDO       | 19  | O   | Watchdog timer output. This is a push-pull output pin. When WDT times out, this pin goes to logic low. If there is no WDT time-out, this pin stays in logic high.                                  |                                                                                                                                                                                                                                                                                  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating junction temperature range, unless otherwise noted.<sup>(1)</sup>

|                   |                                                                                                                                                                           | MIN                                           | MAX            | UNIT |
|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------|----------------|------|
| Voltage           | Input, $V_{DD}$                                                                                                                                                           | −0.3                                          | 7              | V    |
|                   | CT pin, $V_{CT1}$ , $V_{CT2}$ , $V_{CT3}$ , $V_{CT4}$                                                                                                                     | −0.3                                          | $V_{DD} + 0.3$ |      |
|                   | $V_{RESET1}$ , $V_{RESET2}$ , $V_{RESET3}$ , $V_{RESET4}$ , $V_{MR}$ , $V_{SENSE1}$ , $V_{SENSE2}$ , $V_{SENSE3}$ , $V_{SENSE4L}$ , $V_{SENSE4H}$ , $V_{WDI}$ , $V_{WDO}$ | −0.3                                          | 7              |      |
| Current           | $\overline{RESETn}$ , $\overline{RESETn}$ , $\overline{WDO}$ , $\overline{WDO}$ , VREF pin                                                                                |                                               | 5              | mA   |
| Power dissipation | Continuous total                                                                                                                                                          | See <a href="#">Thermal Information</a> table |                |      |
| Temperature       | Operating virtual junction, $T_J^{(2)}$                                                                                                                                   | −40                                           | 150            | °C   |
|                   | Operating ambient, $T_A$                                                                                                                                                  | −40                                           | 125            |      |
|                   | Storage, $T_{stg}$                                                                                                                                                        | −65                                           | 150            |      |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that  $T_J = T_A$ .

### 6.2 ESD Ratings

|                                     |                                                                                | VALUE | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted).

|                   | MIN         | NOM | MAX         | UNIT       |
|-------------------|-------------|-----|-------------|------------|
| $V_{DD}$          | 1.8         |     | 6.5         | V          |
| $V_{SENSE}^{(1)}$ | 0           |     | $V_{DD}$    | V          |
| $WDI_{(HI)}$      | $0.7V_{DD}$ |     | $V_{DD}$    | V          |
| $WDI_{(LO)}$      | 0           |     | $0.3V_{DD}$ | V          |
| $V_{MR}$          | 0           |     | $V_{DD}$    | V          |
| CTn               | 0.22        |     | 1000        | nF         |
| $R_{PULL-UP}$     | 6.5         | 100 | 10000       | k $\Omega$ |
| $T_J$             | −40         | 25  | 125         | °C         |

- (1) All sense inputs.

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | TPS3860x0  | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGP (VQFN) |      |
|                               |                                              | 20 PINS    |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 46         | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 52.8       | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 22.4       | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 1.3        | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 22.4       | °C/W |
| $R_{\theta JC(bot)}$          | Junction-to-case (bottom) thermal resistance | 4.3        | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

## 6.5 Electrical Characteristics

Over the operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $1.8\text{ V} < V_{DD} < 6.5\text{ V}$ ,  $R_{\text{RESETn}}$  ( $n = 1, 2, 3, 4$ ) =  $100\text{ k}\Omega$  to  $V_{DD}$  (TPS386000 only),  $C_{\text{RESETn}}$  ( $n = 1, 2, 3, 4\text{L}, 4\text{H}$ ) =  $50\text{ pF}$  to GND,  $R_{\text{WDO}} = 100\text{ k}\Omega$  to  $V_{DD}$ ,  $C_{\text{WDO}} = 50\text{ pF}$  to GND,  $V_{\text{MR}} = 100\text{ k}\Omega$  to  $V_{DD}$ , WDI = GND, and CTn ( $n = 1, 2, 3, 4$ ) = open, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

| PARAMETER            |                                                                                        |                | TEST CONDITIONS                                                                                                                         | MIN                   | TYP   | MAX                | UNIT |
|----------------------|----------------------------------------------------------------------------------------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-------|--------------------|------|
| V <sub>DD</sub>      | Input supply range                                                                     |                |                                                                                                                                         | 1.8                   |       | 6.5                | V    |
| I <sub>DD</sub>      | Supply current (current into V <sub>DD</sub> pin)                                      |                | V <sub>DD</sub> = 3.3 V, $\overline{\text{RESETn}}$ or RESETn not asserted, WDI toggling <sup>(1)</sup> , no output load, and VREF open |                       | 11    | 19                 | μA   |
|                      |                                                                                        |                | V <sub>DD</sub> = 6.5 V, $\overline{\text{RESETn}}$ or RESETn not asserted, WDI toggling <sup>(1)</sup> , no output load, and VREF open |                       | 13    | 22                 |      |
|                      | Power-up reset voltage <sup>(2)(3)</sup>                                               |                | V <sub>OL</sub> (max) = 0.2 V, I <sub>RESETn</sub> = 15 μA                                                                              |                       |       | 0.9                | V    |
| V <sub>ITN</sub>     | Negative-going input threshold voltage                                                 |                | SENSE1, SENSE2, SENSE3, SENSE4L                                                                                                         | 396                   | 400   | 404                | mV   |
| V <sub>ITP</sub>     | Positive-going input threshold voltage                                                 |                | SENSE4H                                                                                                                                 | 396                   | 400   | 404                | mV   |
| V <sub>HYSN</sub>    | Hysteresis (positive-going) on V <sub>ITN</sub>                                        |                | SENSE1, SENSE2, SENSE3, SENSE4L                                                                                                         |                       | 3.5   | 10                 | mV   |
| V <sub>HYSN</sub>    | Hysteresis (negative-going) on V <sub>ITP</sub>                                        |                | SENSE4H                                                                                                                                 |                       | 3.5   | 10                 | mV   |
| I <sub>SENSE</sub>   | Input current at SENSEm pin                                                            |                | V <sub>SENSEm</sub> = 0.42 V                                                                                                            | −25                   | ±1    | +25                | nA   |
| I <sub>CT</sub>      | CTn pin charging current                                                               | CT1            | C <sub>CT1</sub> > 220 pF, V <sub>CT1</sub> = 0.5 V <sup>(4)</sup>                                                                      | 245                   | 300   | 355                | nA   |
|                      |                                                                                        | CT2, CT3, CT4  | C <sub>CTn</sub> > 220 pF, V <sub>CTn</sub> = 0.5 V <sup>(4)</sup>                                                                      | 235                   | 300   | 365                |      |
| V <sub>TH(CTn)</sub> | CTn pin threshold                                                                      |                | C <sub>CTn</sub> > 220 pF                                                                                                               | 1.18                  | 1.238 | 1.299              | V    |
| V <sub>IL</sub>      | $\overline{\text{MR}}$ and WDI logic low input                                         |                |                                                                                                                                         | 0                     |       | 0.3V <sub>DD</sub> | V    |
| V <sub>IH</sub>      | $\overline{\text{MR}}$ and WDI logic high input                                        |                |                                                                                                                                         | 0.7V <sub>DD</sub>    |       |                    | V    |
| V <sub>OL</sub>      | Low-level $\overline{\text{RESETn}}$ or RESETn output voltage                          |                | I <sub>OL</sub> = 1 mA                                                                                                                  |                       |       | 0.4                | V    |
|                      |                                                                                        |                | SENSEn = 0 V, 1.3 V < V <sub>DD</sub> < 1.8 V, I <sub>OL</sub> = 0.4 mA <sup>(2)</sup>                                                  |                       |       | 0.3                | V    |
|                      | Low-level WDO output voltage                                                           |                | I <sub>OL</sub> = 1 mA                                                                                                                  |                       |       | 0.4                |      |
| V <sub>OH</sub>      | High-level $\overline{\text{RESETn}}$ or RESETn output voltage                         | TPS386040 only | I <sub>OL</sub> = −1 mA                                                                                                                 | V <sub>DD</sub> − 0.4 |       |                    | V    |
|                      | High-level WDO output voltage                                                          | TPS386040 only | I <sub>OL</sub> = −1 mA                                                                                                                 | V <sub>DD</sub> − 0.4 |       |                    | V    |
|                      |                                                                                        |                | SENSEn = 0 V, 1.3 V < V <sub>DD</sub> < 1.8 V, I <sub>OL</sub> = −0.4 mA <sup>(2)</sup>                                                 | V <sub>DD</sub> − 0.3 |       |                    |      |
| I <sub>LKG</sub>     | $\overline{\text{RESETn}}$ , RESETn, $\overline{\text{WDO}}$ , and WDO leakage current | TPS386000 only | V <sub>RESETn</sub> = 6.5 V, $\overline{\text{RESETn}}$ , RESETn, $\overline{\text{WDO}}$ , and WDO are logic high                      | −300                  |       | 300                | nA   |
| V <sub>REF</sub>     | Reference voltage output                                                               |                | 1 μA < I <sub>VREF</sub> < 0.2 mA (source only, no sink)                                                                                | 1.18                  | 1.2   | 1.22               | V    |
| C <sub>IN</sub>      | Input pin capacitance                                                                  |                | CTn: 0 V to V <sub>DD</sub> , other pins: 0 V to 6.5 V                                                                                  |                       | 5     |                    | pF   |

- (1) Toggling WDI for a period less than  $t_{\text{WDT}}$  negatively affects  $I_{DD}$ .
- (2) These specifications are beyond the recommended  $V_{DD}$  range, and only define  $\overline{\text{RESETn}}$  or RESETn output performance during  $V_{DD}$  ramp up.
- (3) The lowest supply voltage ( $V_{DD}$ ) at which  $\overline{\text{RESETn}}$  or RESETn becomes active;  $t_{\text{RISE}(V_{DD})} \geq 15\text{ }\mu\text{s/V}$ .
- (4) CTn (where  $n = 1, 2, 3$ , or 4) are constant current charging sources working from a range of 0 V to  $V_{\text{TH(CTn)}}$ , and the device is tested at  $V_{CTn} = 0.5\text{ V}$ . For  $I_{CT}$  performance between 0 V and  $V_{\text{TH(CTn)}}$ , see Figure 28.

## 6.6 Timing Requirements

Over the operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $1.8\text{ V} < V_{DD} < 6.5\text{ V}$ ,  $R_{\text{RESET}n} (n = 1, 2, 3, 4) = 100\text{ k}\Omega$  to  $V_{DD}$  (TPS386000 only),  $C_{\text{RESET}n} (n = 1, 2, 3, 4\text{L}, 4\text{H}) = 50\text{ pF}$  to GND,  $R_{\text{WDO}} = 100\text{ k}\Omega$  to  $V_{DD}$ ,  $C_{\text{WDO}} = 50\text{ pF}$  to GND,  $V_{\text{MR}} = 100\text{ k}\Omega$  to  $V_{DD}$ ,  $\text{WDI} = \text{GND}$ , and  $\text{CT}n (n = 1, 2, 3, 4) = \text{open}$ , unless otherwise noted. Nominal values are at  $T_J = 25^{\circ}\text{C}$ .

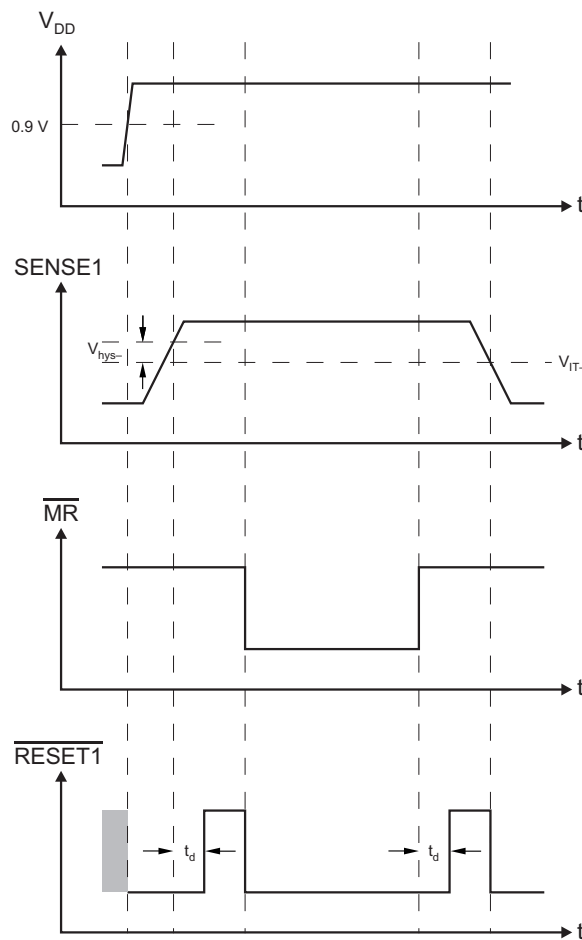
|       |                                         | MIN                                                                                                                    | TYP | MAX | UNIT          |
|-------|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------|-----|-----|---------------|
| $t_W$ | Input pulse width to SENSEm and MR pins | SENSEm: $1.05 V_{\text{ITN}} \rightarrow 0.95 V_{\text{ITN}}$ or $0.95 V_{\text{ITP}} \rightarrow 1.05 V_{\text{ITP}}$ |     | 4   | $\mu\text{s}$ |
|       |                                         | MR: $0.7 V_{DD} \rightarrow 0.3 V_{DD}$                                                                                |     | 1   | ns            |

## 6.7 Switching Characteristics

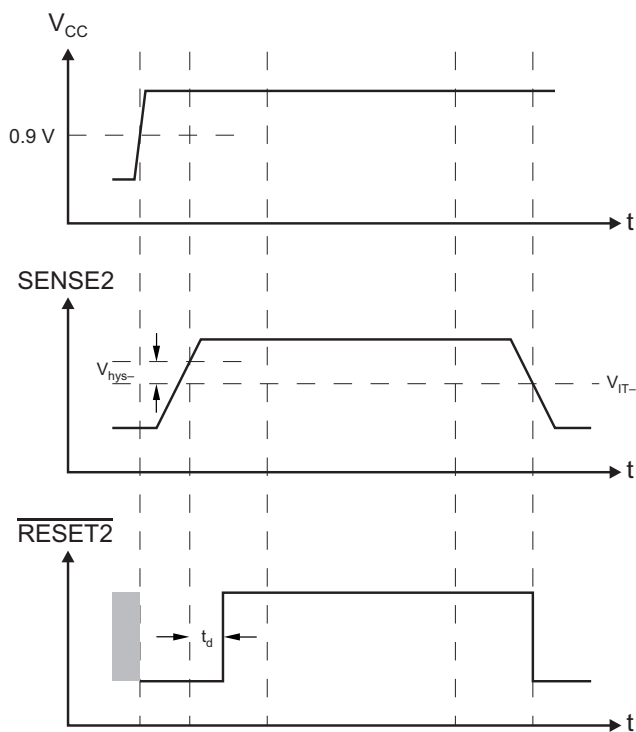
Over the operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $1.8\text{ V} < V_{DD} < 6.5\text{ V}$ ,  $R_{\text{RESET}n} (n = 1, 2, 3, 4) = 100\text{ k}\Omega$  to  $V_{DD}$  (TPS386000 only),  $C_{\text{RESET}n} (n = 1, 2, 3, 4\text{L}, 4\text{H}) = 50\text{ pF}$  to GND,  $R_{\text{WDO}} = 100\text{ k}\Omega$  to  $V_{DD}$ ,  $C_{\text{WDO}} = 50\text{ pF}$  to GND,  $V_{\text{MR}} = 100\text{ k}\Omega$  to  $V_{DD}$ ,  $\text{WDI} = \text{GND}$ , and  $\text{CT}n (n = 1, 2, 3, 4) = \text{open}$ , unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

| PARAMETER        | TEST CONDITIONS                                          | MIN            | TYP | MAX | UNIT |
|------------------|----------------------------------------------------------|----------------|-----|-----|------|
| $t_D$            | $\overline{\text{RESET}n}$ or $\text{RESET}n$ delay time | CTn = Open     | 14  | 20  | 24   |
|                  |                                                          | CTn = $V_{DD}$ | 225 | 300 | 375  |
| $t_{\text{WDT}}$ | Watchdog timer time-out period <sup>(1)</sup>            | 450            | 600 | 750 | ms   |

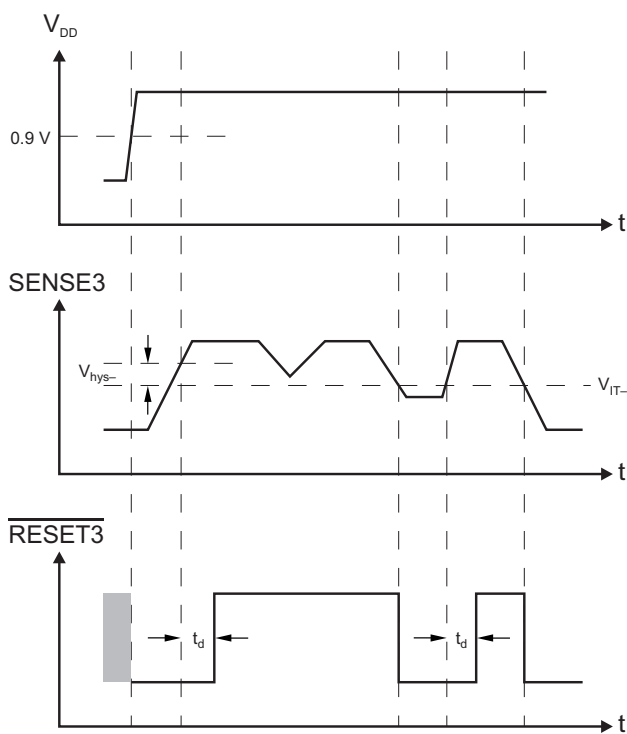
(1) Start from  $\overline{\text{RESET}1}$  or  $\text{RESET}1$  release or last WDI transition.



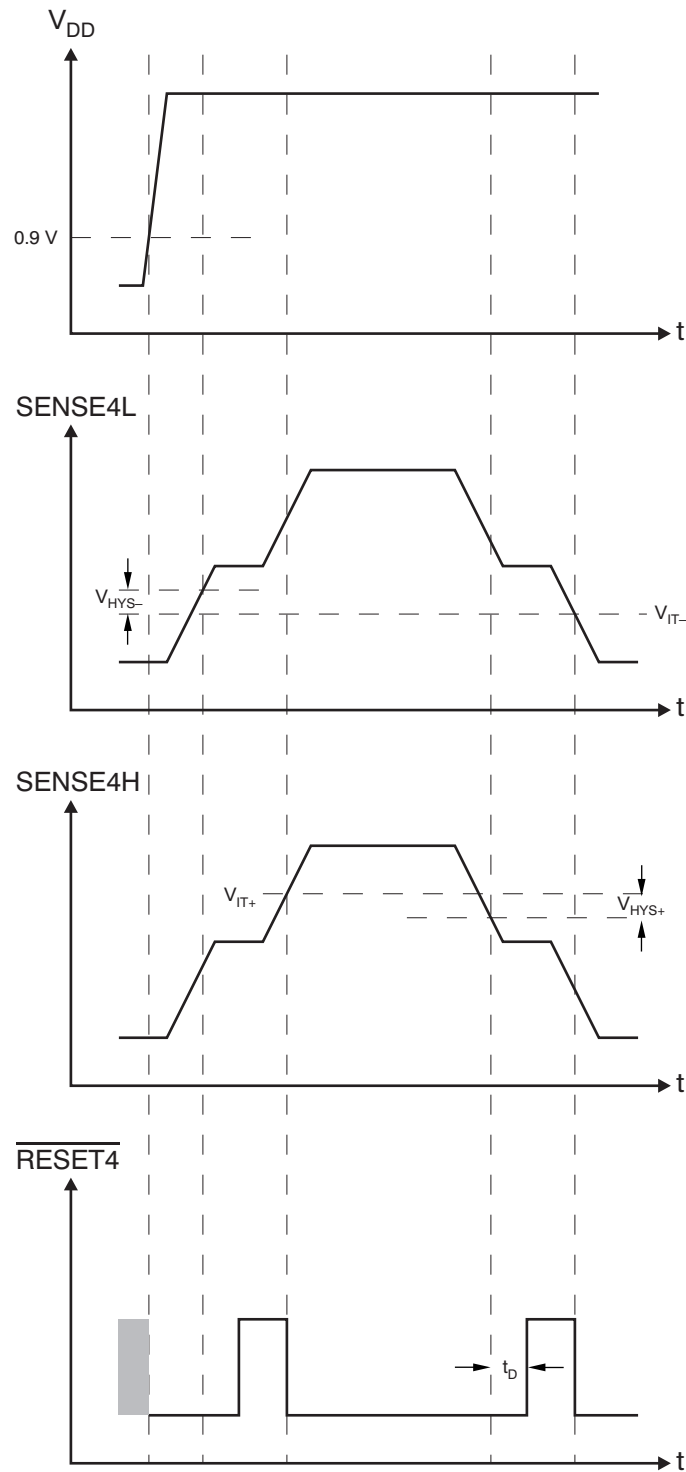
**Figure 1. SVS-1 Timing Diagram**



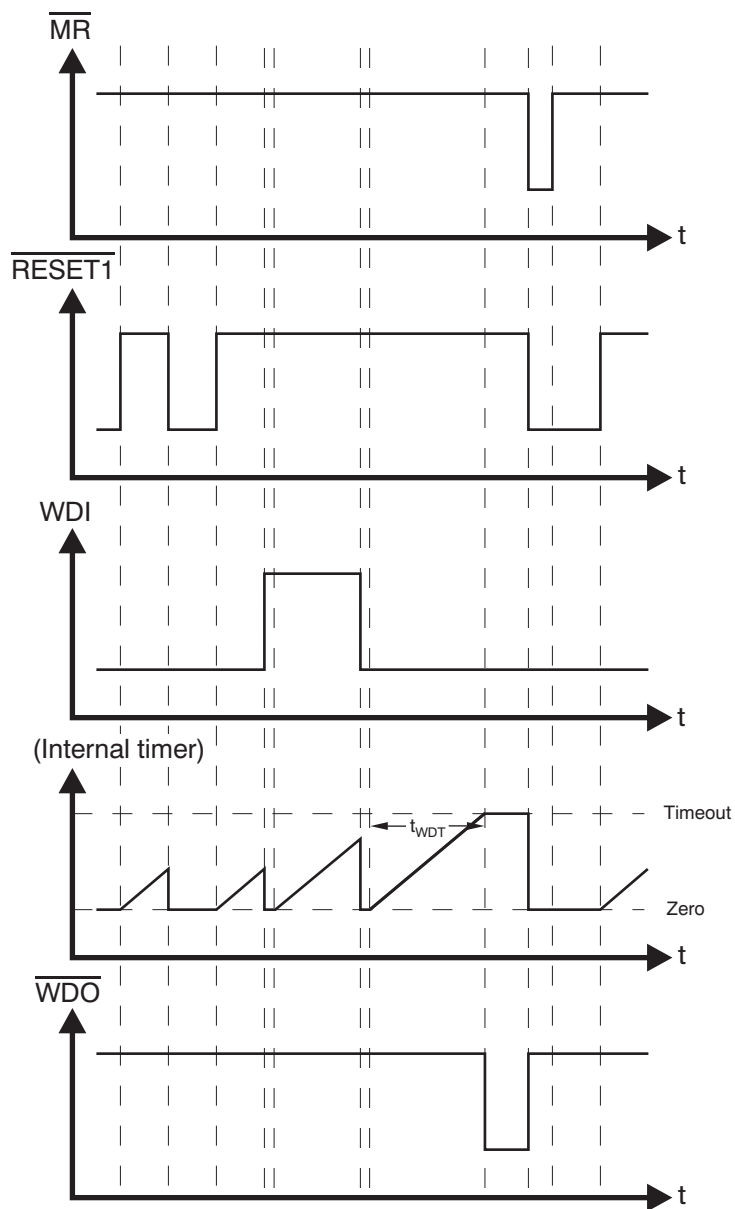
**Figure 2. SVS-2 Timing Diagram**



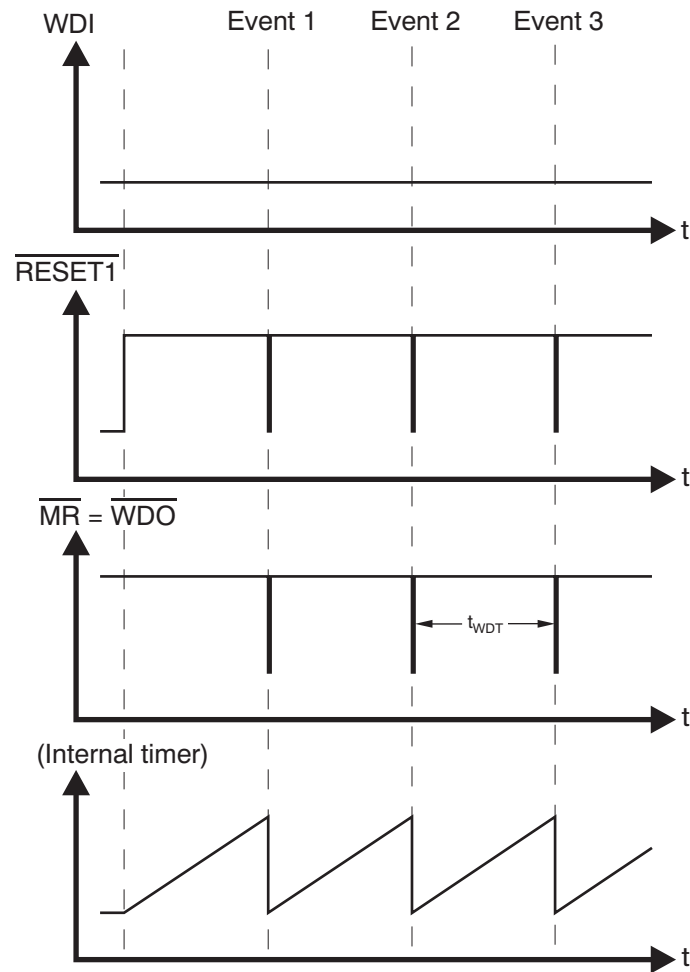
**Figure 3. SVS-3 Timing Diagram**



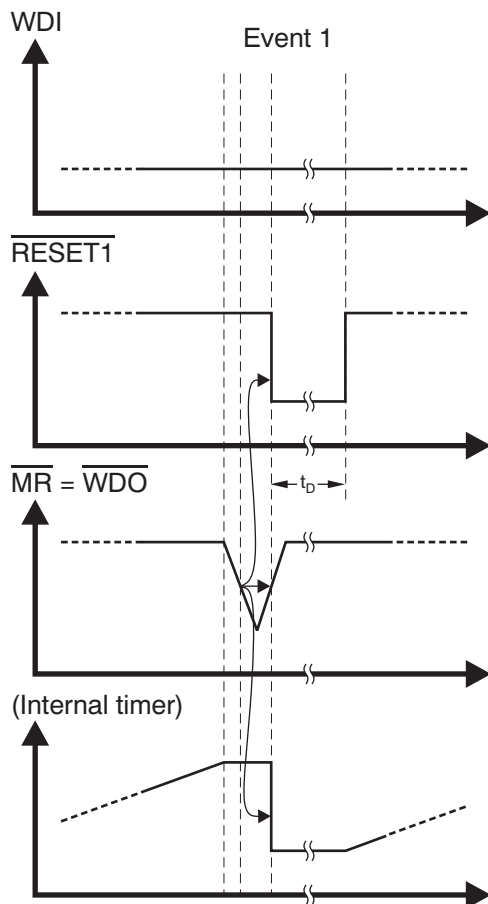
**Figure 4. SVS-4 Timing Diagram**



**Figure 5. WDT Timing Diagram**



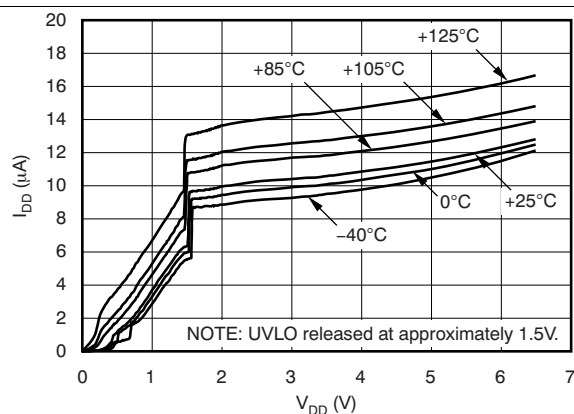
**Figure 6. Legacy WDT Configuration Timing Diagram**



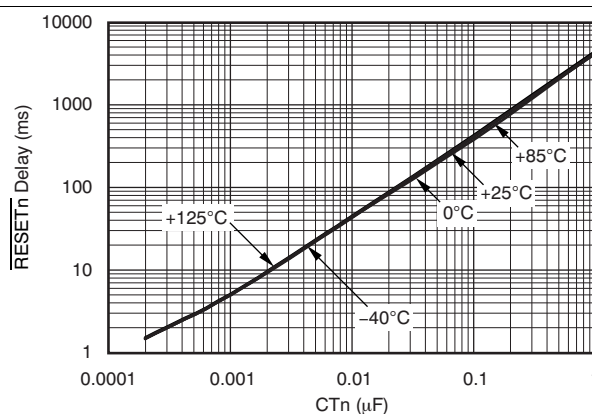
**Figure 7. Enlarged View of Event 1 from [Figure 6](#)**

## 6.8 Typical Characteristics

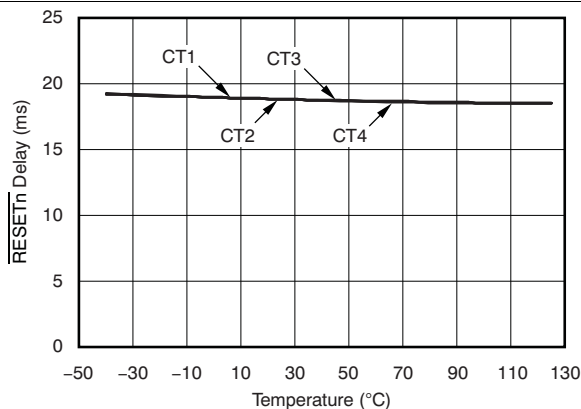
At  $T_A = 25^\circ\text{C}$ , and  $V_{DD} = 3.3\text{ V}$ , with both options (TPS386000 and TPS386040) having the same characteristics, unless otherwise noted.



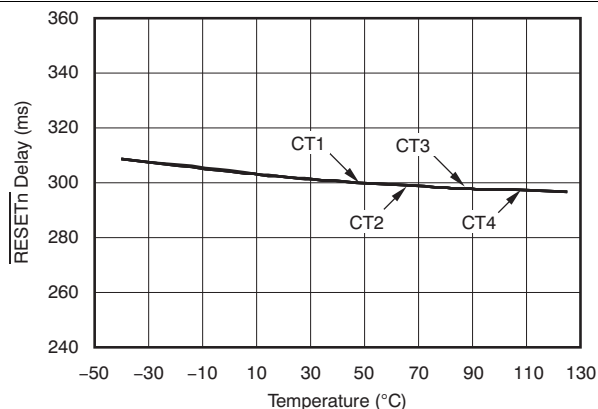
**Figure 8. TPS386040 Supply Current vs Supply Voltage**



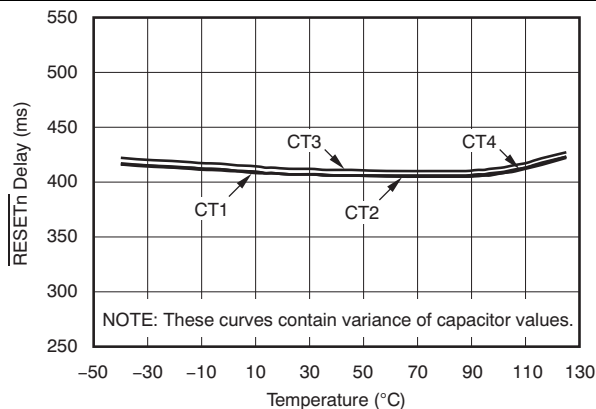
**Figure 9. TPS386040  $\overline{\text{RESETn}}$  Time-out Period vs  $\text{CTn}$**



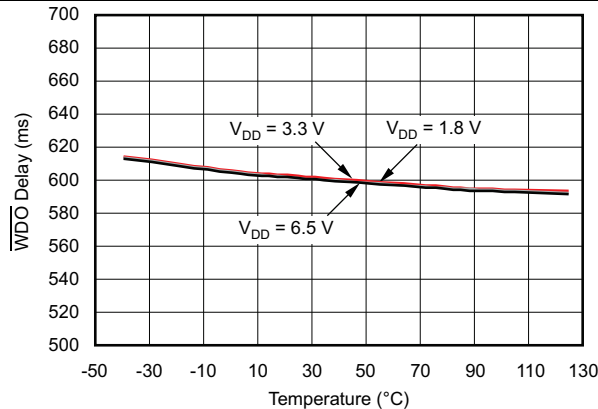
**Figure 10. TPS386040 ( $\text{CTn} = \text{Open}$ )  $\overline{\text{RESETn}}$  Time-out Period vs Temperature**



**Figure 11. TPS386040 ( $\text{CTn} = V_{DD}$ )  $\overline{\text{RESETn}}$  Time-out Period vs Temperature**



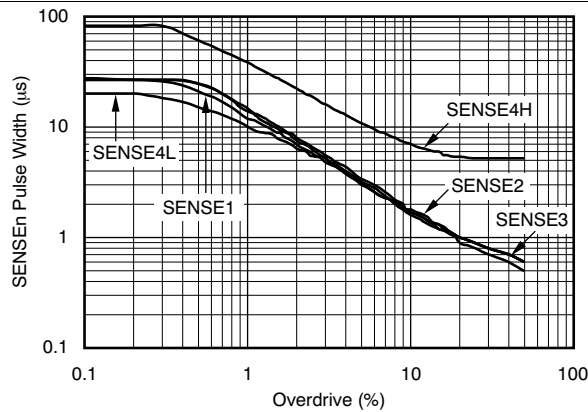
**Figure 12. TPS386040 ( $\text{CTn} = 0.1\text{ }\mu\text{F}$ )  $\overline{\text{RESETn}}$  Time-out Period vs Temperature**



**Figure 13. TPS386040  $\overline{\text{WDO}}$  Time-out Period vs Temperature**

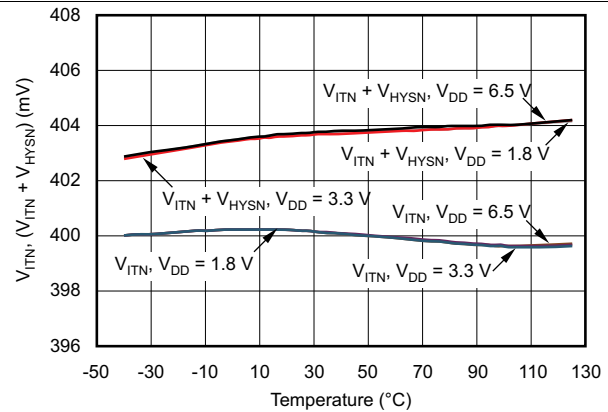
## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ , and  $V_{DD} = 3.3\text{ V}$ , with both options (TPS386000 and TPS386040) having the same characteristics, unless otherwise noted.

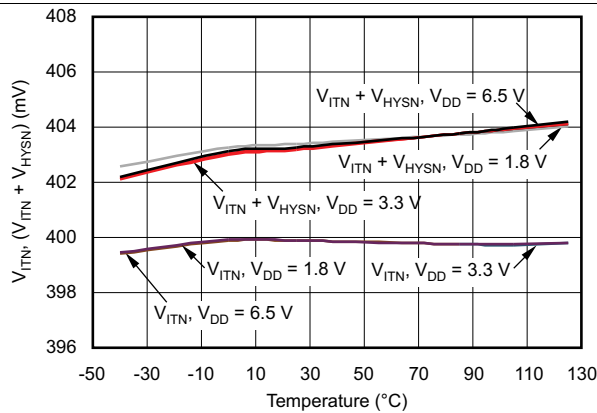


See Figure 29 for measurement technique

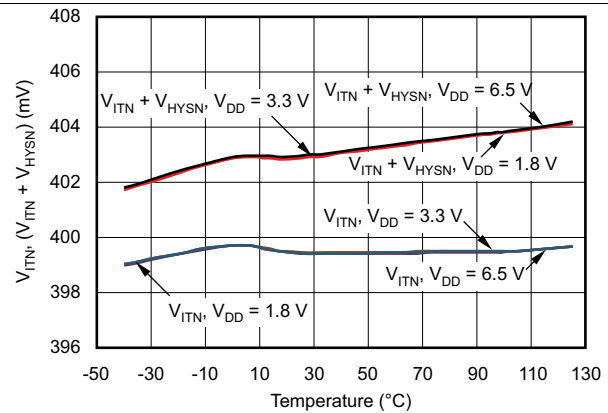
**Figure 14. TPS386040 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage**



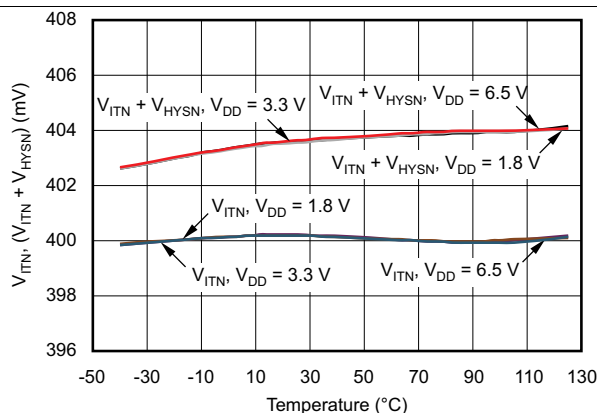
**Figure 15. TPS386040 SENSE1 Threshold Voltage vs Temperature**



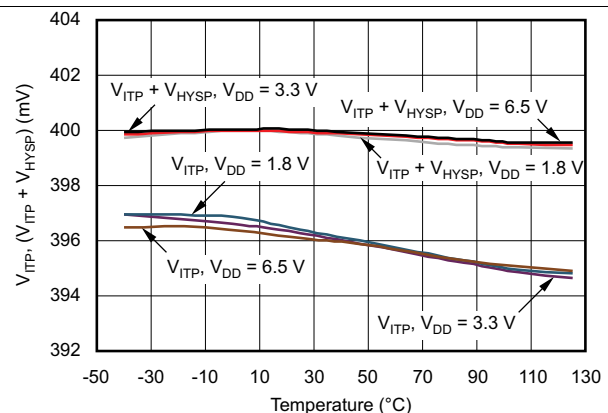
**Figure 16. TPS386040 SENSE2 Threshold Voltage vs Temperature**



**Figure 17. TPS386040 SENSE3 Threshold Voltage vs Temperature**



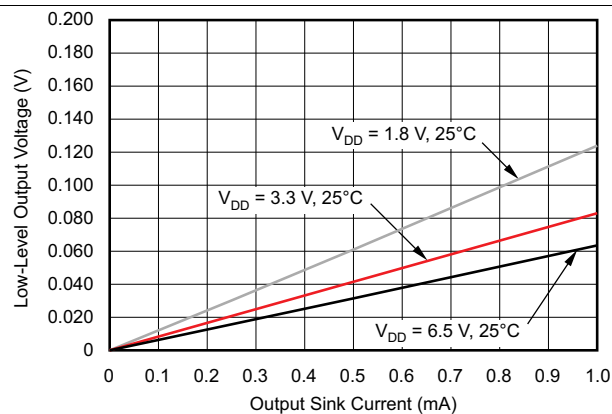
**Figure 18. TPS386040 SENSE4L Threshold Voltage vs Temperature**



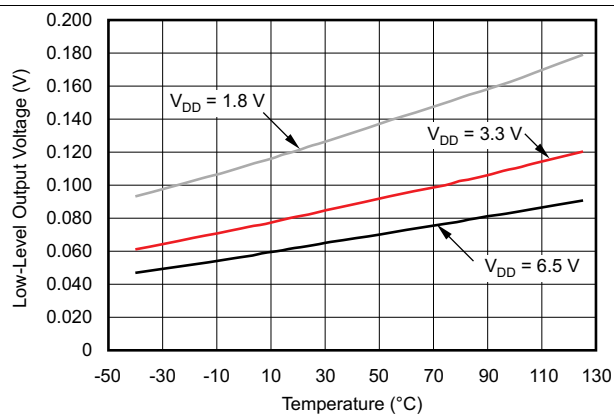
**Figure 19. TPS386040 SENSE4H Threshold Voltage vs Temperature**

## Typical Characteristics (continued)

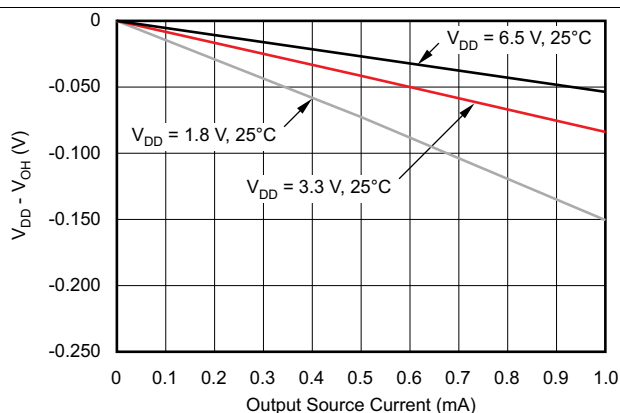
At  $T_A = 25^\circ\text{C}$ , and  $V_{DD} = 3.3\text{ V}$ , with both options (TPS386000 and TPS386040) having the same characteristics, unless otherwise noted.



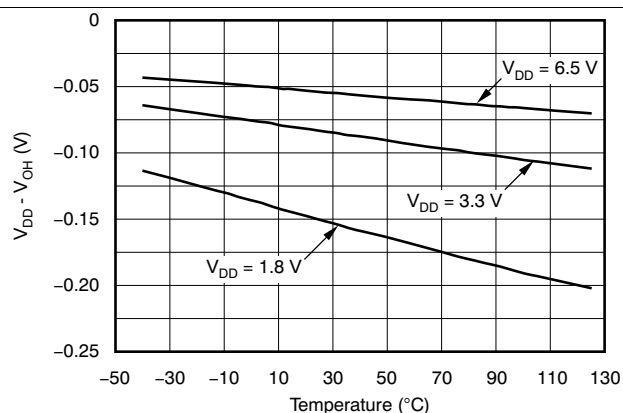
**Figure 20. Output Voltage Low vs Output Current**



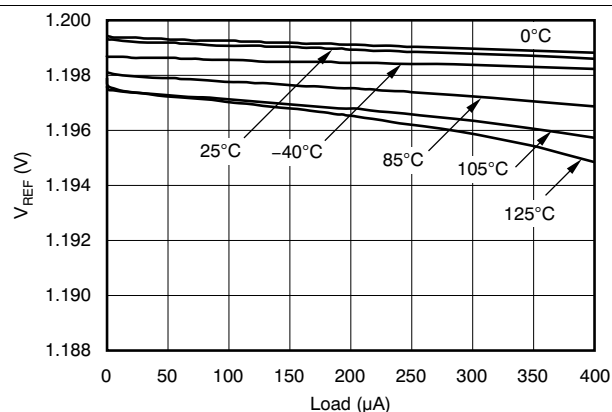
**Figure 21. Output Voltage Low at 1 mA vs Temperature**



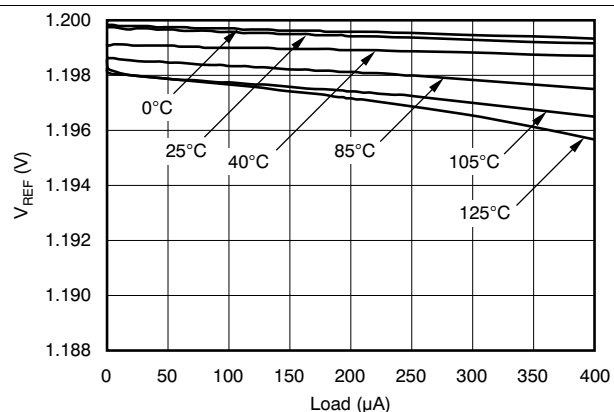
**Figure 22. Output Voltage High vs Output Current**



**Figure 23. Output Voltage High at 1 mA vs Temperature**



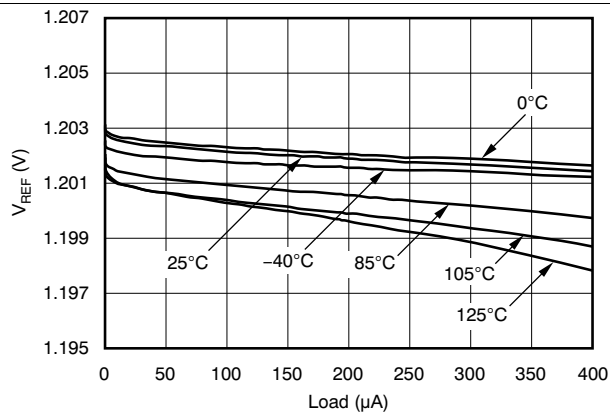
**Figure 24. TPS386040  $V_{REF}$  Output Load Regulation ( $V_{DD} = 1.8\text{ V}$ )**



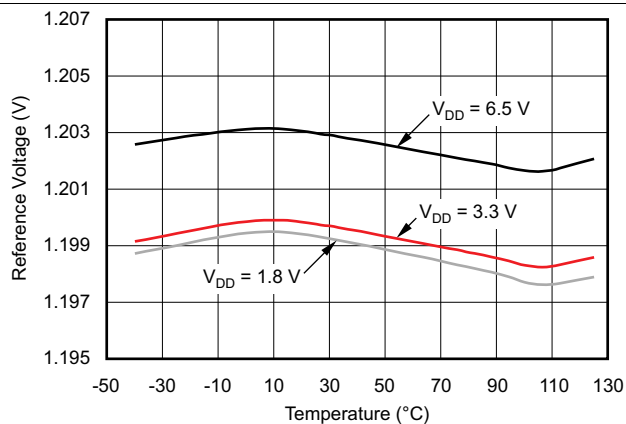
**Figure 25. TPS386040  $V_{REF}$  Output Load Regulation ( $V_{DD} = 3.3\text{ V}$ )**

## Typical Characteristics (continued)

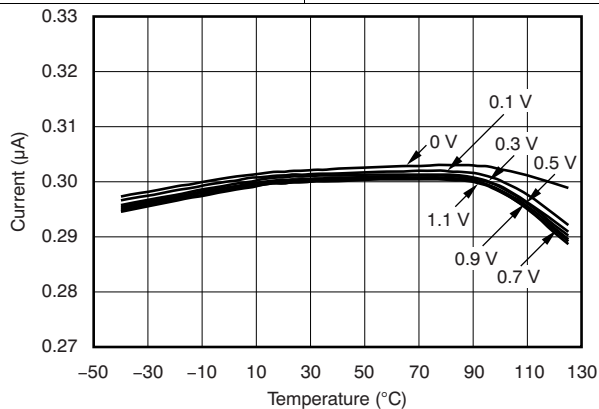
At  $T_A = 25^\circ\text{C}$ , and  $V_{DD} = 3.3\text{ V}$ , with both options (TPS386000 and TPS386040) having the same characteristics, unless otherwise noted.



**Figure 26. TPS386040  $V_{REF}$  Output Load Regulation ( $V_{DD} = 6.5\text{ V}$ )**

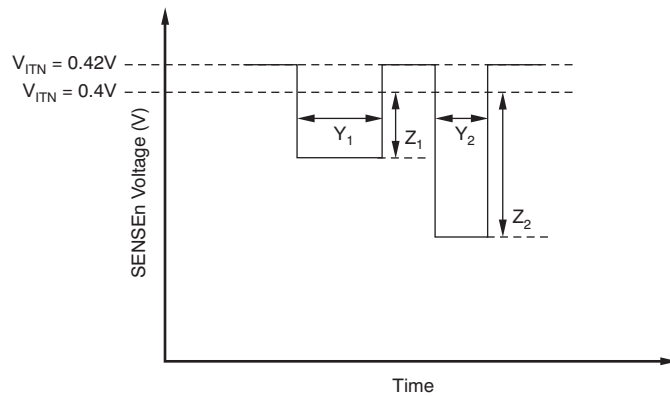


**Figure 27. TPS386040  $V_{REF}$  at  $0\text{ }\mu\text{A}$  vs Temperature**



**Figure 28. TPS386040 CT1 to CT4 Pin Charging Current vs Temperature Over CT Pin Voltage**

## 7 Parameter Measurement Information



$$X_1 = \frac{Z_1}{0.4} \times 100 (\%)$$

$$X_2 = \frac{Z_2}{0.4} \times 100 (\%)$$

$X_1$  and  $X_2$  are overdrive (%) values calculated from actual SENSEn voltage amplitudes measured as  $Z_1$  and  $Z_2$ .

$Y_N$  is the minimum pulse width that gives RESETn or  $\overline{\text{RESETn}}$  transition. Greater  $Z_N$  produces shorter  $Y_N$ .

For SENSE4H, this graph should be inverted 180 degrees on the voltage axis.

**Figure 29. Overdrive Measurement Method**

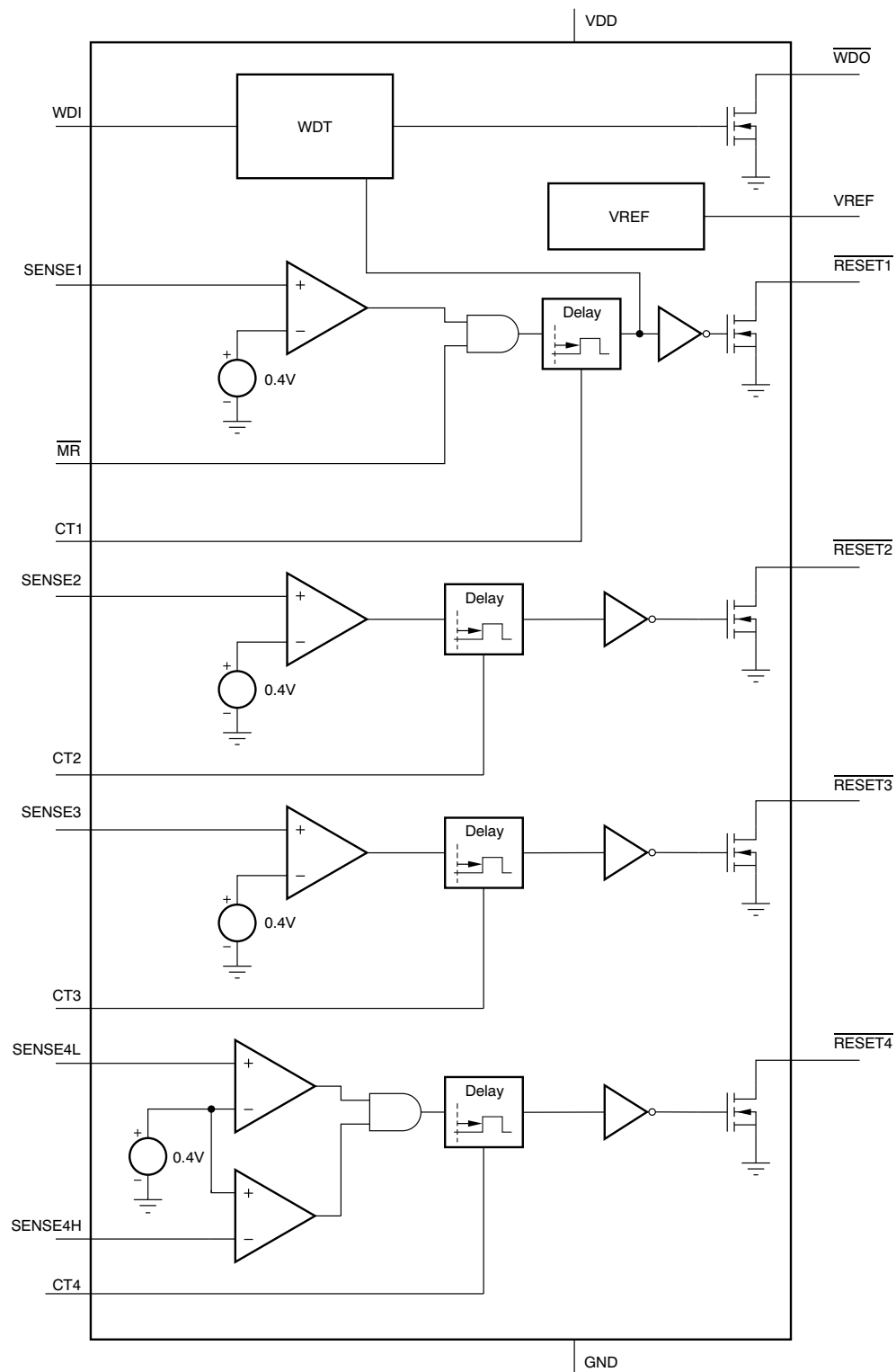
## 8 Detailed Description

### 8.1 Overview

The TPS3860x0 multi-channel supervisory family of devices combines four complete SVS function sets into one IC, along with a watchdog timer, a window comparator, and negative voltage sensing. The design of each SVS channel is based on the single-channel supervisory device series, [TPS3808](#). The TPS3860x0 is designed to assert  $\overline{\text{RESETn}}$  or RESETn signals, as shown in [Table 1](#), [Table 2](#), [Table 3](#), and [Table 4](#). The  $\overline{\text{RESETn}}$  or RESETn outputs remain asserted during a user-configurable delay time after the event of reset release (see the [Reset Delay Time](#) section).

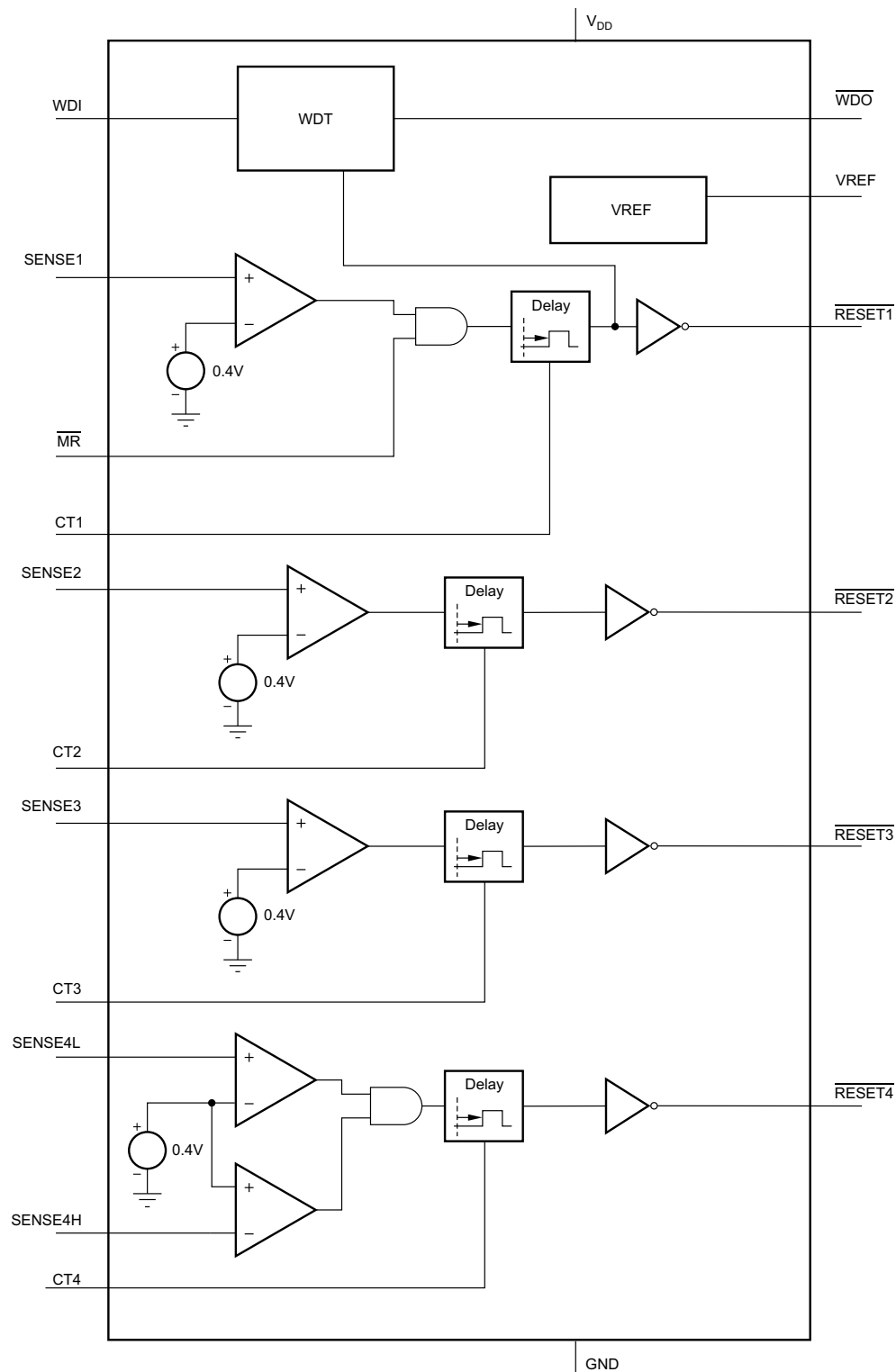
The TPS3860x0 has a very low quiescent current of 11  $\mu\text{A}$  (typical) and is available in a small, 4-mm  $\times$  4-mm, 20-Pin VQFN package.

## 8.2 Functional Block Diagrams



**Figure 30. TPS386000 Block Diagram**

## Functional Block Diagrams (continued)



**Figure 31. TPS386040 Block Diagram**

## 8.3 Feature Description

### 8.3.1 Voltage Monitoring

Each SENSE<sub>m</sub> (m = 1, 2, 3, 4L) pin can be set to monitor any voltage threshold above 0.4 V using an external resistor divider. The SENSE4H pin can be used for any overvoltage detection greater than 0.4 V, or for negative voltage detection using an external resistor divider (see the [Sensing a Negative Voltage](#) section). A broad range of voltage threshold and reset delay time adjustments can be supported, allowing these devices to be used in a wide array of applications.

The TPS3860x0 is relatively immune to short negative transients on the SENSE<sub>n</sub> pin. Sensitivity to transients depends on threshold overdrive, as shown in ([Figure 14](#)).

### 8.3.2 Manual Reset

The manual reset ( $\overline{\text{MR}}$ ) input allows external logic signal from other processors, logic circuits, and/or discrete sensors to initiate a device reset. Because  $\overline{\text{MR}}$  is connected to SVS-1, the  $\overline{\text{RESET1}}$  or RESET1 pin is intended to be connected to processor(s) as a primary reset source. A logic low at  $\overline{\text{MR}}$  causes  $\overline{\text{RESET1}}$  or RESET1 to assert. After  $\overline{\text{MR}}$  returns to a logic high and SENSE1 is above its reset threshold,  $\overline{\text{RESET1}}$  or RESET1 is released after the user-configured reset delay time. Unlike the [TPS3808](#) series, the TPS3860x0 does not integrate an internal pullup resistor between  $\overline{\text{MR}}$  and  $V_{\text{DD}}$ .

To control the  $\overline{\text{MR}}$  function from more than one logic signal, the logic signals can be combined by wired-OR into the  $\overline{\text{MR}}$  pin using multiple NMOS transistors and one pullup resistor.

### 8.3.3 Watchdog Timer

The TPS3860x0 provides a watchdog timer with a dedicated watchdog error output,  $\overline{\text{WDO}}$  or WDO. The  $\overline{\text{WDO}}$  or WDO output enables application board designers to easily detect and resolve the hang-up status of a processor. As with  $\overline{\text{MR}}$ , the watchdog timer function of the device is also tied to SVS-1. [Figure 5](#) shows the timing diagram of the WDT function. Once  $\overline{\text{RESET1}}$  or RESET1 is released, the internal watchdog timer starts its countdown. Inputting a logic level transition at WDI resets the internal timer count and the timer restarts the countdown. If the TPS3860x0 fails to receive any WDI rising or falling edge within the WDT period, the WDT times out and asserts  $\overline{\text{WDO}}$  or WDO. After  $\overline{\text{WDO}}$  or WDO is asserted, the device holds the status with the internal latch circuit. To clear this time-out status, a reset assertion of  $\overline{\text{RESET1}}$  or RESET is required. That is, a negative pulse to  $\overline{\text{MR}}$ , a SENSE1 voltage less than  $V_{\text{ITN}}$ , or a  $V_{\text{DD}}$  power down is required.

To reset the processor by WDT time-out,  $\overline{\text{WDO}}$  can be combined with  $\overline{\text{RESET1}}$  by using the wired-OR with the TPS386000 option.

For legacy applications where the watchdog timer time-out causes  $\overline{\text{RESET1}}$  to assert, connect  $\overline{\text{WDO}}$  to  $\overline{\text{MR}}$ ; see [Figure 35](#) for the connections and see [Figure 6](#) and [Figure 7](#) for the timing diagrams.

## Feature Description (continued)

### 8.3.4 Reset Output

In a typical TPS3860x0 application,  $\overline{\text{RESETn}}$  or RESETn outputs are connected to the reset input of a processor (DSP, CPU, FPGA, ASIC, and so forth), or connected to the enable input of a voltage regulator (DC-DC, LDO, and so forth).

The TPS386000 provides open-drain reset outputs. Pullup resistors must be used to hold these lines high when  $\overline{\text{RESETn}}$  is not asserted, or when RESETn is asserted. By connecting pullup resistors to the proper voltage rails (up to 6.5 V),  $\overline{\text{RESETn}}$  or RESETn output nodes can be connected to the other devices at the correct interface voltage levels. The pullup resistor should be no smaller than 10 k $\Omega$  to ensure the safe operation of the output transistors. By using wired-OR logic, any combination of  $\overline{\text{RESETn}}$  can be merged into one logic signal.

The TPS386040 provides pushpull reset outputs. The logic high level of the outputs is determined by the  $V_{DD}$  voltage. With this configuration, pullup resistors are not required and some board area can be saved. However, all the interface logic levels should be examined. All  $\overline{\text{RESETn}}$  or RESETn connections must be compatible with the  $V_{DD}$  logic level.

The  $\overline{\text{RESETn}}$  or RESETn outputs are defined for  $V_{DD}$  voltage higher than 0.9 V. To ensure that the target processor(s) are properly reset, the  $V_{DD}$  supply input should be fed by the available power rail as early as possible in application circuits. Table 1, Table 2, Table 3, and Table 4 are truth tables that describe how the outputs are asserted or released. Figure 1, Figure 2, Figure 3, and Figure 4 show the SVS-n timing diagrams. When the conditions are met, the device changes the state of SVS-n from asserted to released after a user-configurable delay time. However, the transitions from released-state to asserted-state are performed almost immediately with minimal propagation delay. Figure 3 describes the relationship between threshold voltages ( $V_{ITN}$  and  $V_{HYSN}$ ) and SENSEm voltage; and all SVS-1, SVS-2, SVS-3, and SVS-4 have the same behavior of Figure 3.

## 8.4 Device Functional Modes

The following tables show the state of the output and the status of the part under various conditions.

**Table 1. SVS-1 Truth Table**

| CONDITION                            |                           | OUTPUT                                   | STATUS                     |
|--------------------------------------|---------------------------|------------------------------------------|----------------------------|
| $\overline{\text{MR}} = \text{Low}$  | $\text{SENSE1} < V_{ITN}$ | $\overline{\text{RESET1}} = \text{Low}$  | Reset asserted             |
| $\overline{\text{MR}} = \text{Low}$  | $\text{SENSE1} > V_{ITN}$ | $\overline{\text{RESET1}} = \text{Low}$  | Reset asserted             |
| $\overline{\text{MR}} = \text{High}$ | $\text{SENSE1} < V_{ITN}$ | $\overline{\text{RESET1}} = \text{Low}$  | Reset asserted             |
| $\overline{\text{MR}} = \text{High}$ | $\text{SENSE1} > V_{ITN}$ | $\overline{\text{RESET1}} = \text{High}$ | Reset released after delay |

**Table 2. SVS-2 Truth Table**

| CONDITION                 | OUTPUT                                   | STATUS                     |
|---------------------------|------------------------------------------|----------------------------|
| $\text{SENSE2} < V_{ITN}$ | $\overline{\text{RESET2}} = \text{Low}$  | Reset asserted             |
| $\text{SENSE2} > V_{ITN}$ | $\overline{\text{RESET2}} = \text{High}$ | Reset released after delay |

**Table 3. SVS-3 Truth Table**

| CONDITION                 | OUTPUT                                   | STATUS                     |
|---------------------------|------------------------------------------|----------------------------|
| $\text{SENSE3} < V_{ITN}$ | $\overline{\text{RESET3}} = \text{Low}$  | Reset asserted             |
| $\text{SENSE3} > V_{ITN}$ | $\overline{\text{RESET3}} = \text{High}$ | Reset released after delay |

**Table 4. SVS-4 Truth Table**

| CONDITION                         |                                   | OUTPUT                                   | STATUS                     |
|-----------------------------------|-----------------------------------|------------------------------------------|----------------------------|
| $\text{SENSE4L} < V_{\text{ITN}}$ | $\text{SENSE4H} > V_{\text{ITP}}$ | $\overline{\text{RESET4}} = \text{Low}$  | Reset asserted             |
| $\text{SENSE4L} < V_{\text{ITN}}$ | $\text{SENSE4H} < V_{\text{ITP}}$ | $\overline{\text{RESET4}} = \text{Low}$  | Reset asserted             |
| $\text{SENSE4L} > V_{\text{ITN}}$ | $\text{SENSE4H} > V_{\text{ITP}}$ | $\overline{\text{RESET4}} = \text{Low}$  | Reset asserted             |
| $\text{SENSE4L} > V_{\text{ITN}}$ | $\text{SENSE4H} < V_{\text{ITP}}$ | $\overline{\text{RESET4}} = \text{High}$ | Reset released after delay |

**Table 5. Watchdog Timer (WDT) Truth Table**

| CONDITION               |      |                            |                                | OUTPUT                                | STATUS                  |
|-------------------------|------|----------------------------|--------------------------------|---------------------------------------|-------------------------|
| $\overline{\text{WDO}}$ | WDO  | $\overline{\text{RESET1}}$ | WDI PULSE INPUT                |                                       |                         |
| Low                     | High | Asserted                   | Toggling                       | $\overline{\text{WDO}} = \text{low}$  | Remains in WDT time-out |
| Low                     | High | Asserted                   | 610 ms after last WDI↑ or WDI↓ | $\overline{\text{WDO}} = \text{low}$  | Remains in WDT time-out |
| Low                     | High | Released                   | Toggling                       | $\overline{\text{WDO}} = \text{low}$  | Remains in WDT time-out |
| Low                     | High | Released                   | 610 ms after last WDI↑ or WDI↓ | $\overline{\text{WDO}} = \text{low}$  | Remains in WDT time-out |
| High                    | Low  | Asserted                   | Toggling                       | $\overline{\text{WDO}} = \text{high}$ | Normal operation        |
| High                    | Low  | Asserted                   | 610 ms after last WDI↑ or WDI↓ | $\overline{\text{WDO}} = \text{high}$ | Normal operation        |
| High                    | Low  | Released                   | Toggling                       | $\overline{\text{WDO}} = \text{high}$ | Normal operation        |
| High                    | Low  | Released                   | 610 ms after last WDI↑ or WDI↓ | $\overline{\text{WDO}} = \text{low}$  | Enters WDT timeout      |

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Undervoltage Detection

The SENSEm inputs are pins that allow any system voltages to be monitored. If the voltage at the SENSE1, SENSE2, SENSE3, or SENSE4L pins drops below  $V_{ITN}$ , then the corresponding reset outputs are asserted. If the voltage at the SENSE4H pin exceeds  $V_{ITP}$ , then RESET4 or RESET4 is asserted. The comparators have a built-in hysteresis to ensure smooth reset output assertions and deassertions. In noisy applications, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the SENSEm input to reduce sensitivity to transients, layout parasitics, and interference between power rails monitored by this device. A typical connection of resistor dividers are shown in Figure 35. All the SENSEm pins can be used to monitor voltage rails down to 0.4 V. Threshold voltages can be calculated using Equation 1 to Equation 3.

$$V_{MON(1)} = (1 + R_{S1H}/R_{S1L}) \times 0.4 \text{ (V)} \quad (1)$$

$$V_{MON(2)} = (1 + R_{S2H}/R_{S2L}) \times 0.4 \text{ (V)} \quad (2)$$

$$V_{MON(3)} = (1 + R_{S3H}/R_{S3L}) \times 0.4 \text{ (V)} \quad (3)$$

#### 9.1.2 Undervoltage and Overvoltage Detection

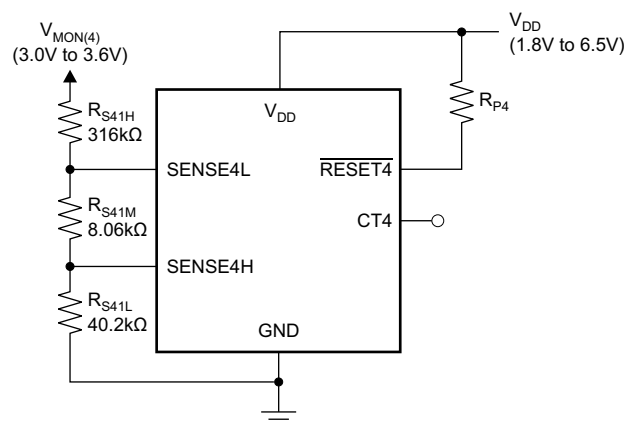
The comparator at the SENSE4H pin has the opposite comparison polarity to the other SENSEm pins. In the configuration shown in Figure 32, this comparator monitors overvoltage of the  $V_{MON(4)}$  node; combined with the comparator at SENSE4L, SVS-4 forms a window comparator.

$$V_{MON(4, UV)} = \{1 + R_{S4H}/(R_{S4M} + R_{S4L})\} \times 0.4 \text{ (V)} \quad (4)$$

$$V_{MON(4, OV)} = \{1 + (R_{S4H} + R_{S4M})/R_{S4L}\} \times 0.4 \text{ (V)}$$

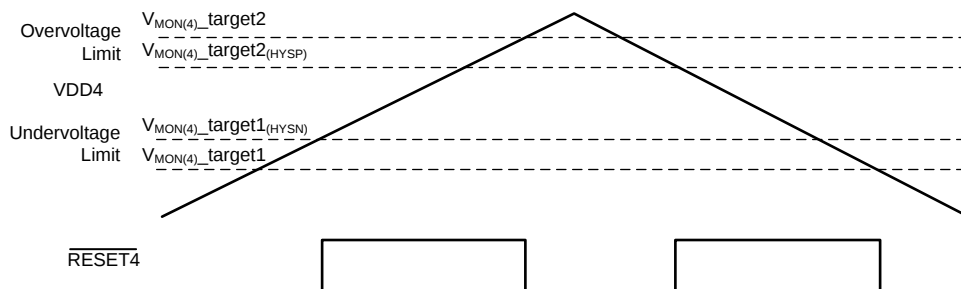
where

- $V_{MON(4, UV)}$  is the undervoltage threshold.
- $V_{MON(4, OV)}$  is the overvoltage threshold.



**Figure 32. SVS-4: Window Comparator**

## Application Information (continued)



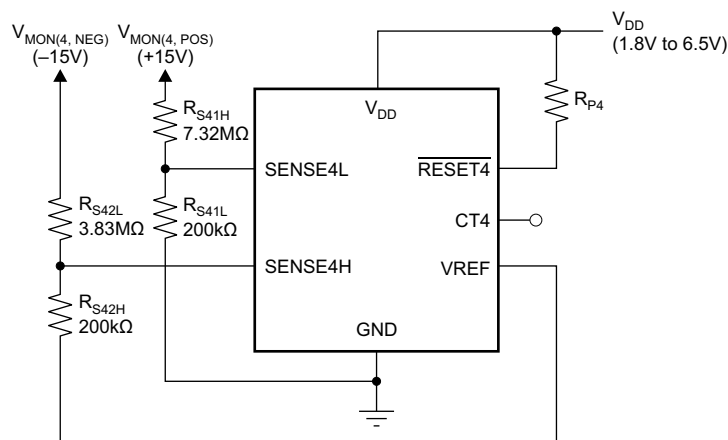
**Figure 33. Window Comparator Operation**

### 9.1.3 Sensing a Negative Voltage

By using voltage reference output VREF, the SVS-4 comparator can monitor negative voltage or positive voltage lower than 0.4V. [Figure 34](#) shows this usage in an application circuit. SVS-4 monitors the positive and negative voltage power rail (for example, 15-V and –15-V supply to an op amp) and the RESET4 or RESET4 output status continues to be as described in [Table 4](#).  $R_{S42H}$  is located at higher voltage position than  $R_{S42L}$ . The threshold voltage calculations are shown in [Equation 6](#) and [Equation 7](#).

$$V_{MON(4, NEG)} = (1 + R_{S41H}/R_{S41L}) \times 0.4 \text{ (V)} \quad (6)$$

$$V_{MON(4, POS)} = (1 + R_{S42L}/R_{S42H}) \times 0.4 - R_{S42L}/R_{S42H} \times V_{REF} = 0.4 - [R_{S42L}/R_{S42H} \times 0.8 \text{ (V)}] \quad (7)$$



**Figure 34. SVS4: Negative Voltage Sensing**

## Application Information (continued)

### 9.1.4 Reset Delay Time

Each of the SVS-n channels can be configured independently in one of three modes. [Table 6](#) describes the delay time settings.

**Table 6. Delay Timing Selection**

| CTn CONNECTION            | DELAY TIME       |
|---------------------------|------------------|
| Pullup to V <sub>DD</sub> | 300 ms (typical) |
| Open                      | 20 ms (typical)  |
| Capacitor to GND          | Programmable     |

To select the 300-ms fixed delay time, the CTn pin should be pulled up to V<sub>DD</sub> using a resistor from 40 kΩ to 200 kΩ. There is a pulldown transistor from CTn to GND that turns on every time the device powers on to determine and confirm CTn pin status; therefore, a direct connection of CTn to V<sub>DD</sub> causes a large current flow. To select the 20-ms fixed delay time, the CTn pin should be left open. To program a user-defined adjustable delay time, an external capacitor must be connected between CTn and GND. The adjustable delay time can be calculated by the following equation:

$$C_{CT} \text{ (nF)} = [t_{\text{DELAY}} \text{ (ms)} - 0.5 \text{ (ms)}] \times 0.242 \quad (8)$$

Using this equation, a delay time can be set to between 1.4 ms to 10 s. The external capacitor should be greater than 220 pF (nominal) so that the TPS3860x0 can distinguish it from an open CT pin. The reset delay time is determined by the time it takes an on-chip, precision 300-nA current source to charge the external capacitor to 1.24 V. When the  $\overline{\text{RESETn}}$  or  $\text{RESETn}$  outputs are asserted, the corresponding capacitors are discharged. When the condition to release  $\overline{\text{RESETn}}$  or  $\text{RESETn}$  occurs, the internal current sources are enabled and begin to charge the external capacitors. When the CTn voltage on a capacitor reaches 1.24 V, the corresponding  $\overline{\text{RESETn}}$  or  $\text{RESETn}$  pins are released. A low leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.



## 9.2.2 Detailed Design Procedure

Select the pullup resistors to be 100 k $\Omega$  to ensure that  $V_{OL} \leq 0.4$  V.

Use Equation 8 to set  $CT = 22$  nF for all channels to obtain an approximate start-up delay of 100 ms.

Select  $RSnL = 10$  k $\Omega$  for all channels to ensure DC accuracy.

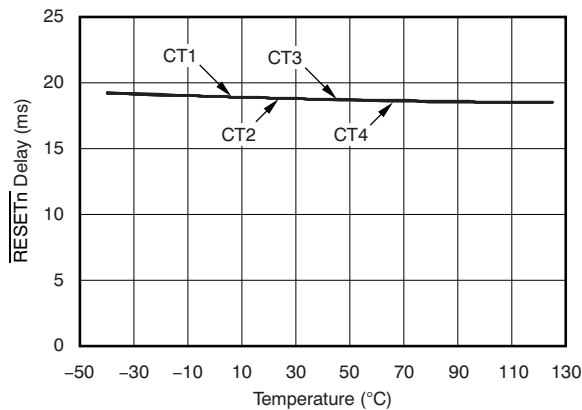
Use Equation 1 through Equation 5 to determine the values of  $RSnH$  and  $RS4M$ . Using standard 1% resistors, Table 8 shows the results.

**Table 8. Design Results**

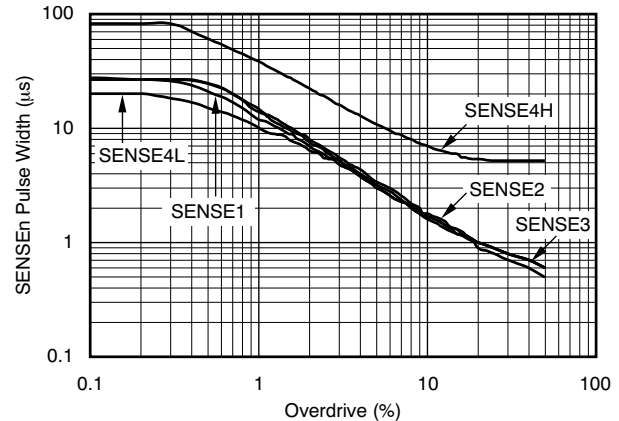
| RESISTOR | VALUE (k $\Omega$ ) |
|----------|---------------------|
| RS1H     | 32.4                |
| RS2H     | 25.5                |
| RS3H     | 18.7                |
| RS4H     | 14.3                |
| RS4M     | 1                   |

The FPGA does not have a separate watchdog failure input, so a legacy connection is used by connecting  $\overline{WDO}$  to MR.

## 9.2.3 Application Curves



**Figure 36. TPS386040 (CTn = Open)  $\overline{RESETn}$  Time-Out Period vs Temperature**



See Figure 29 for measurement technique

**Figure 37. TPS386040 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage**

## 10 Power Supply Recommendations

The TPS386000 can operate from a 1.8-V to a 6.5-V input supply. TI recommends placing a 0.1- $\mu$ F capacitor placed next to the  $V_{DD}$  pin to the GND node. This power supply should not be less than 1.8 V in normal operation to ensure that the internal UVLO circuit does not assert reset.

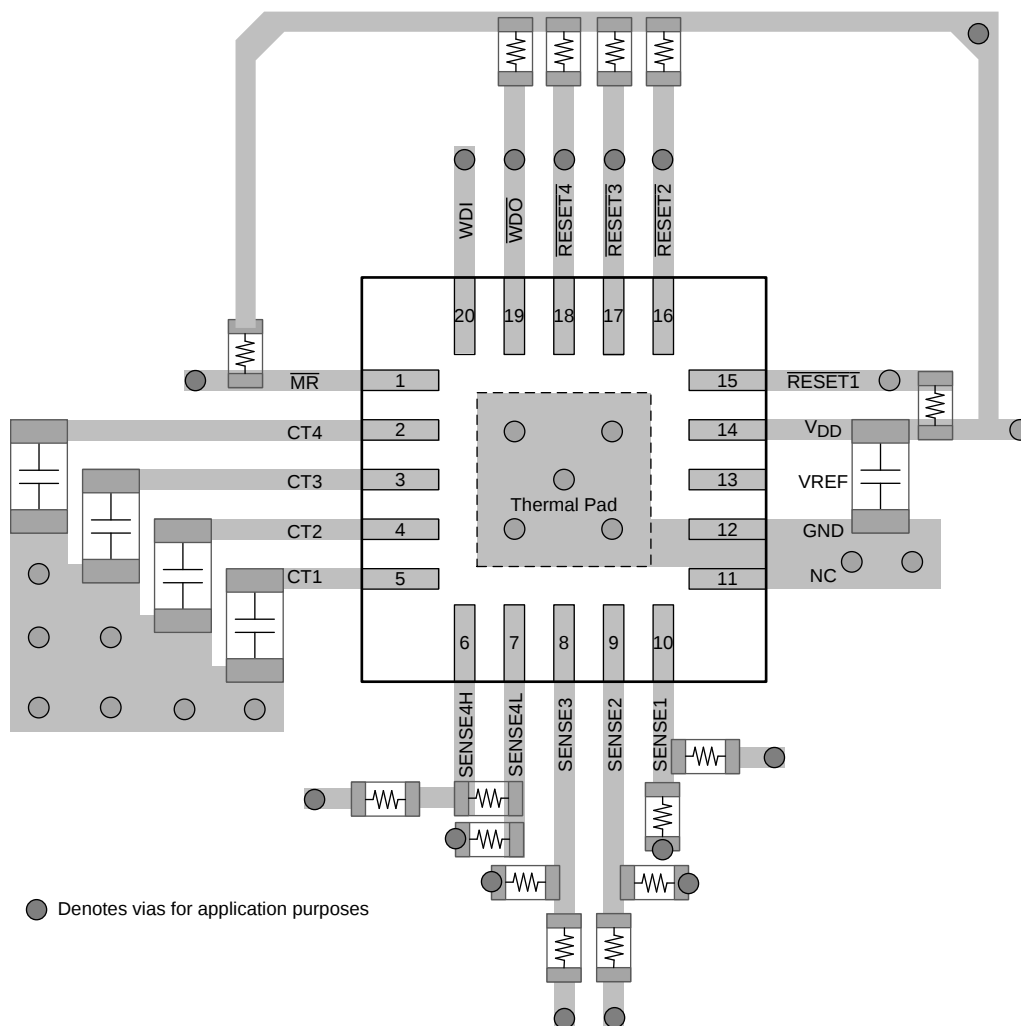
## 11 Layout

### 11.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit board (PCB) that is used for the TPS3860x family of devices.

- Keep the traces to the timer capacitors as short as possible to optimize accuracy.
- Avoid long traces from the SENSE pin to the resistor divider. Instead, run the long traces from the RSnH to  $V_{MON(n)}$ .
- Place the  $V_{DD}$  decoupling capacitor ( $C_{VDD}$ ) close to the device.
- Avoid using long traces for the  $V_{DD}$  supply node. The  $V_{DD}$  capacitor ( $C_{VDD}$ ), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum  $V_{DD}$  voltage.

### 11.2 Layout Example



**Figure 38. Example Layout (RGP Package)**

## 12 器件和文档支持

### 12.1 器件支持

#### 12.1.1 开发支持

##### 12.1.1.1 评估模块

有两个评估模块 (EVM) 可与 TPS3860x0 配套使用，帮助评估初始电路性能。您可以在德州仪器 (TI) 网站上的器件产品文件夹中申请 [TPS386000EVM-736 评估模块](#) 和 [TPS386040EVM 评估模块](#)，也可直接从 [TI 网上商店](#) 购买。

##### 12.1.1.2 Spice 模型

分析模拟电路和系统的性能时，使用 SPICE 模型对电路性能进行计算机仿真非常有用。您可以从器件产品文件夹中的 [仿真模型](#) 下获取 TPS3860x0 的 SPICE 模型。

#### 12.1.2 器件命名规则

**表 9. 器件命名规则<sup>(1)</sup>**

| 产品            | 说明                                                                                                              |
|---------------|-----------------------------------------------------------------------------------------------------------------|
| TPS3860x0yyyz | <b>x</b> 表示器件配置选项<br><b>x = 0</b> : 漏极开路，低电平有效<br><b>x = 4</b> : 推挽，低电平有效<br><b>yyy</b> 是封装符号<br><b>z</b> 是封装数量 |

(1) 要获得最新的封装和订购信息，请见本文档末尾的封装选项附录，或者访问 TI 网站 [www.ti.com.cn](#)。

## 12.2 文档支持

### 12.2.1 相关文档

请参阅如下相关文档：

- 《TPS3860xxEVM-736 用户指南》，[SLVU450](#)
- 《TPS386000 和 TPS386040 EVM 用户指南》，[SLVU341](#)

### 12.3 相关链接

[表 10](#) 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具与软件，以及申请样片或购买产品的快速链接。

**表 10. 相关链接**

| 器件        | 产品文件夹                 | 样片与购买                 | 技术文档                  | 工具与软件                 | 支持和社区                 |
|-----------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| TPS386000 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |
| TPS386040 | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> | <a href="#">请单击此处</a> |

## 12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

**TI E2E™ 在线社区** *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

## 12.5 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

## 12.6 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.7 术语表

**SLYZ022** — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable part number         | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|-------------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">TPS386000RGPR</a> | Active        | Production           | QFN (RGP)   20 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386000       |
| TPS386000RGPR.A               | Active        | Production           | QFN (RGP)   20 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386000       |
| TPS386000RGPRG4               | Active        | Production           | QFN (RGP)   20 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386000       |
| TPS386000RGPRG4.A             | Active        | Production           | QFN (RGP)   20 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386000       |
| <a href="#">TPS386000RGPT</a> | Active        | Production           | QFN (RGP)   20 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386000       |
| TPS386000RGPT.A               | Active        | Production           | QFN (RGP)   20 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386000       |
| <a href="#">TPS386040RGPR</a> | Active        | Production           | QFN (RGP)   20 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386040       |
| TPS386040RGPR.A               | Active        | Production           | QFN (RGP)   20 | 3000   LARGE T&R      | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386040       |
| <a href="#">TPS386040RGPT</a> | Active        | Production           | QFN (RGP)   20 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386040       |
| TPS386040RGPT.A               | Active        | Production           | QFN (RGP)   20 | 250   SMALL T&R       | Yes         | NIPDAU                               | Level-2-260C-1 YEAR               | -40 to 125   | TPS<br>386040       |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS386000 :**

- Automotive : [TPS386000-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

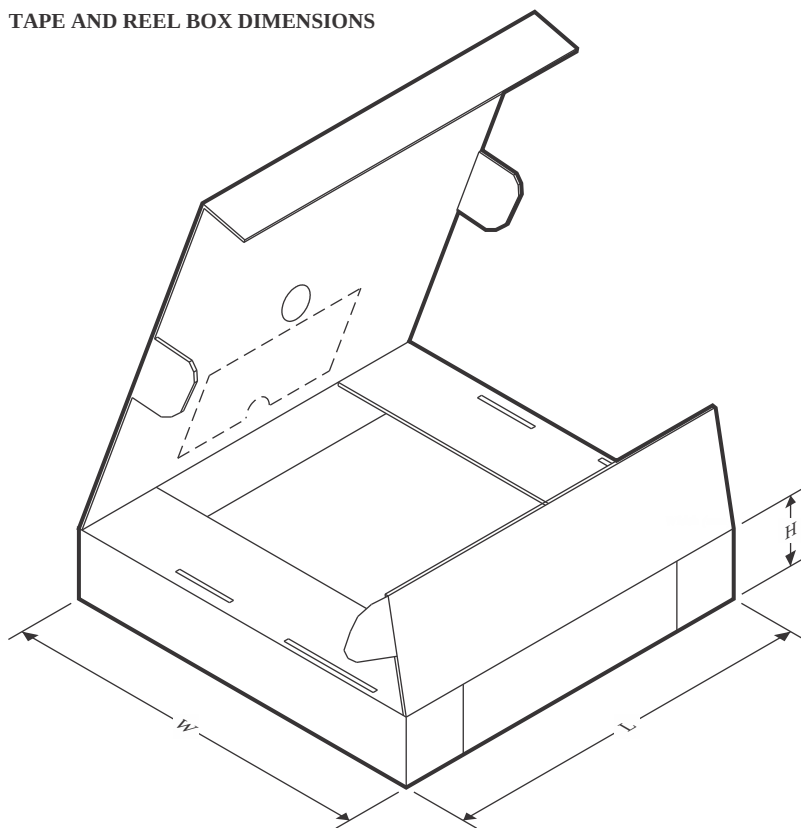
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS386000RGPR   | QFN          | RGP             | 20   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS386000RGPRG4 | QFN          | RGP             | 20   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS386000RGPT   | QFN          | RGP             | 20   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS386040RGPR   | QFN          | RGP             | 20   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |
| TPS386040RGPT   | QFN          | RGP             | 20   | 250  | 180.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS386000RGPR   | QFN          | RGP             | 20   | 3000 | 353.0       | 353.0      | 32.0        |
| TPS386000RGPRG4 | QFN          | RGP             | 20   | 3000 | 353.0       | 353.0      | 32.0        |
| TPS386000RGPT   | QFN          | RGP             | 20   | 250  | 213.0       | 191.0      | 35.0        |
| TPS386040RGPR   | QFN          | RGP             | 20   | 3000 | 353.0       | 353.0      | 32.0        |
| TPS386040RGPT   | QFN          | RGP             | 20   | 250  | 213.0       | 191.0      | 35.0        |

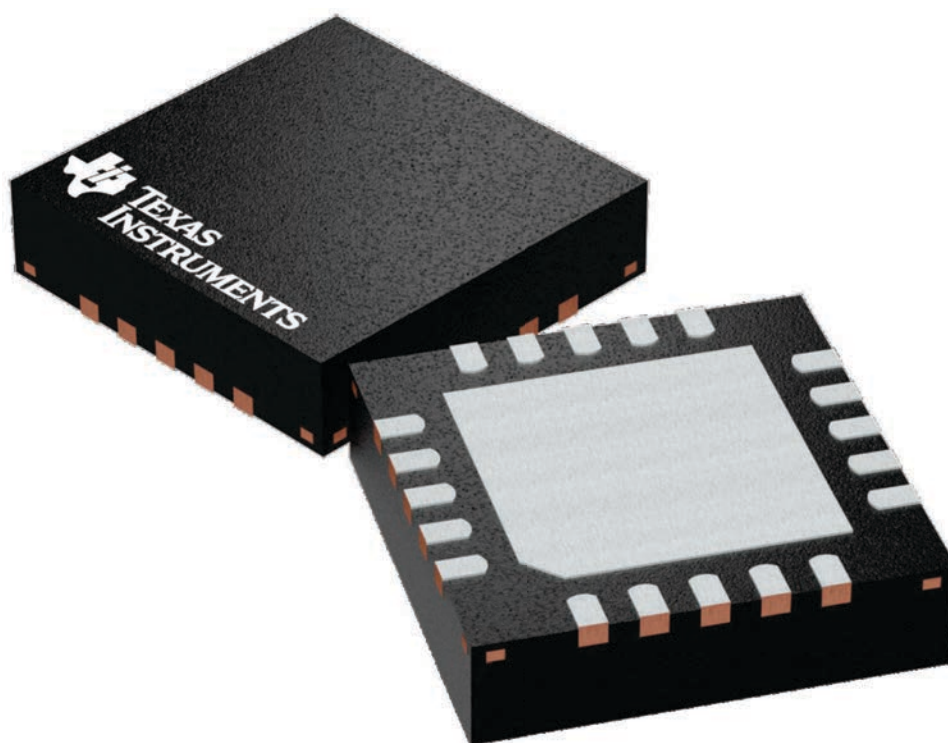
## GENERIC PACKAGE VIEW

**RGP 20**

**VQFN - 1 mm max height**

4 x 4, 0.5 mm pitch

VERY THIN QUAD FLATPACK

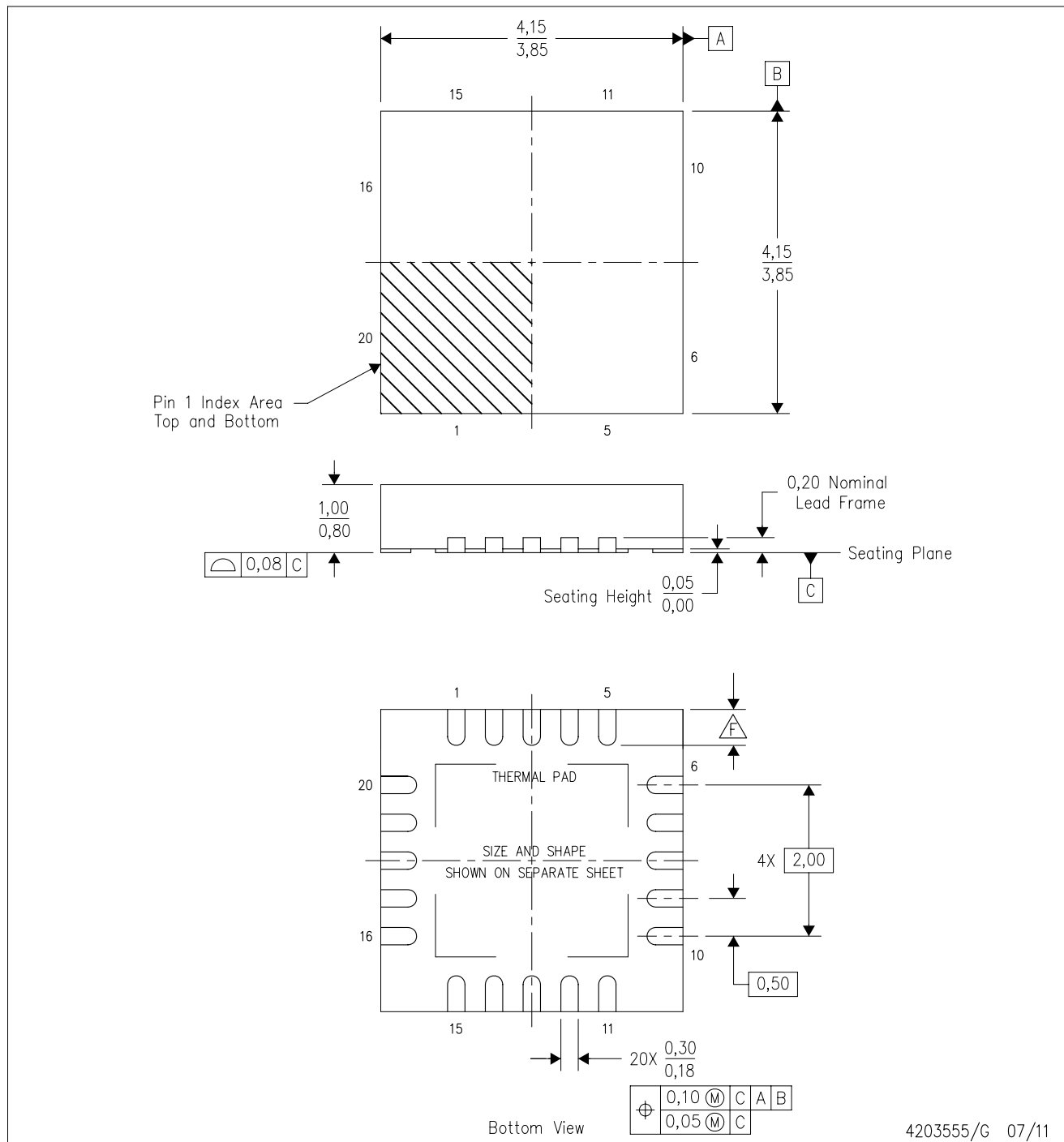


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224735/A

RGP (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



4203555/G 07/11

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - QFN (Quad Flatpack No-Lead) package configuration.
  - The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

RGP (S-PVQFN-N20)

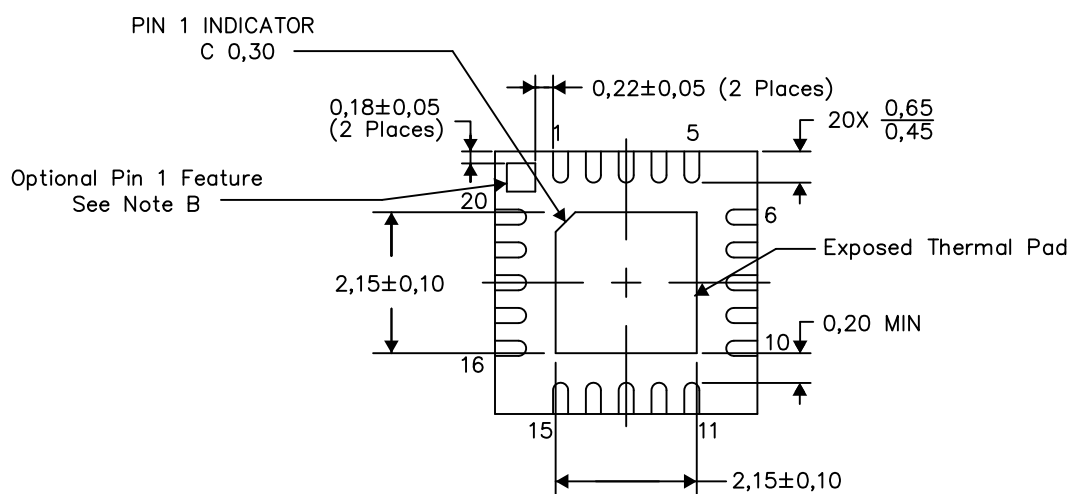
PLASTIC QUAD FLATPACK NO-LEAD

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

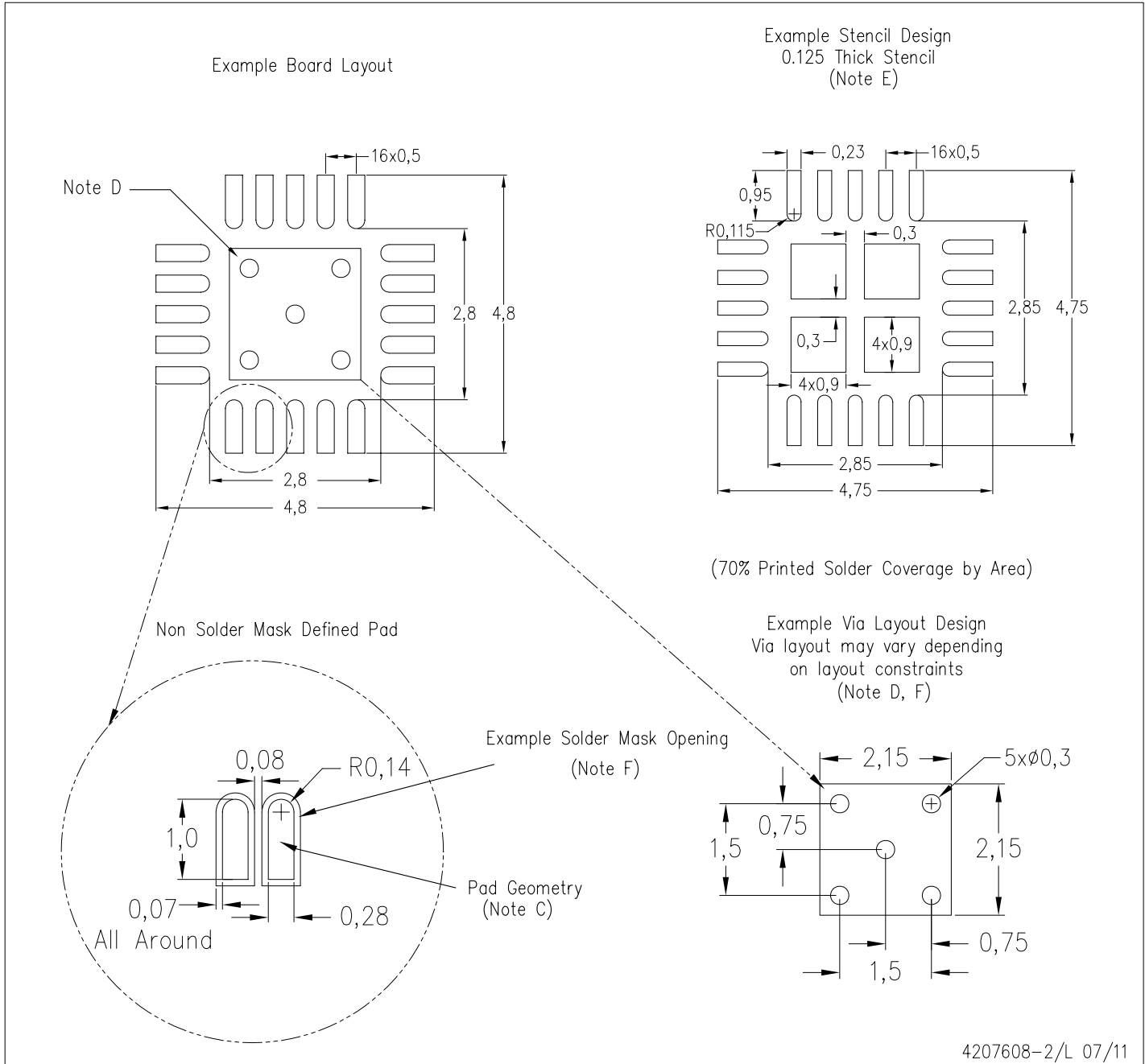
4206346-2/AA 11/13

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices. In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGP (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

## 重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2025，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月