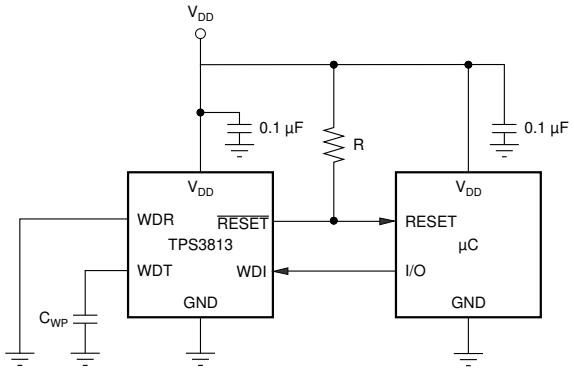
TPS3813xxx 系列具有窗口看门狗的处理器监控电路

1 特性

- 具有可编程延迟和窗口比率的窗口看门狗
- 6 引脚 SOT-23 封装
- 电源电流 9μA（典型值）
- 具有 25ms 固定延时时间的上电复位发生器
- 精密电源电压监测器 (V_{IT})：
  2.5V、3V、3.3V 和 5V
- 开漏复位输出
- 温度范围： -40°C 至 85°C

2 应用

- 有源天线系统 mMIMO (AAS)
- 存储区域网络
- 电表
- 安全关键型系统
- 输液泵
- HVAC 控制器



典型工作电路

3 说明

TPS3813xxx 系列监控电路主要为 DSP 和基于处理器的系统提供电路初始化和计时监测功能。

上电期间，当电源电压 (V_{DD}) 变得高于 1.1V 时，$\overline{RESET}$ 将置为有效。此后，只要 V_{DD} 保持在阈值电压 (V_{IT}) 以下，监控电路就会监视 V_{DD} 并使 $\overline{RESET}$ 保持有效状态。内部定时器将使输出延迟恢复至待机状态（高电平），以确保系统正常复位。延时时间 t_d = 25ms（典型值）在 V_{DD} 上升至高于阈值电压 (V_{IT}) 之后开始。当电源电压降至阈值电压 (V_{IT}) 以下时，输出再次变为有效状态（低电平）。无需外部组件。该系列中的所有器件均具有一个通过内部分压器设定的固定感应阈值电压 (V_{IT})。

对于安全关键型应用，TPS3813xxx 系列包含所谓的具备可编程延迟和窗口比率的窗口看门狗。可通过将 WDT 连接到 GND 或 V_{DD} 或使用外部电容器来设置看门狗超时的上限。可通过将 WDR 连接到 GND 或 V_{DD} 来设置下限和窗口比率。受监控的处理器现在需要在该窗口内触发 TPS3813xxx，从而使 $\overline{RESET}$ 失效。

该产品系列专为 2.5V、3V、3.3V 和 5V 电源电压而设计。这些电路采用 6 引脚 SOT-23 封装。

TPS3813xxx 器件的工作温度范围为 -40°C 至 +85°C。

器件信息

器件型号	封装 (1)	本体尺寸（标称值）(2)
TPS3813xxx	SOT-23 (6)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

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4 Device Comparison Table

T_A (1)	DEVICE NAME	THRESHOLD VOLTAGE	MARKING
–40°C to +85°C	TPS3813J25DBV	2.25V	PCDI
	TPS3813L30DBV	2.64V	PEZI
	TPS3813K33DBV	2.93V	PFAI
	TPS3813I50DBV	4.55V	PFBI

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the device product folder at www.ti.com.

5 Pin Configuration and Functions

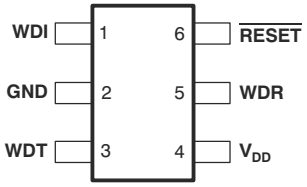


图 5-1. DBV Package
6-Pin SOT-23
Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	WDI	I	Watchdog timer input. This input must be driven at all times and not left floating.
2	GND	I	Ground
3	WDT	I	Programmable watchdog delay input
4	V_{DD}	I	Supply voltage and supervising input
5	WDR	I	Selectable watchdog window ratio input. This input must be tied to V_{DD} or GND and not left floating.
6	$\overline{\text{RESET}}$	O	Open-drain reset output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted). (1)

		MIN	MAX	UNIT
V_{DD}	Supply voltage (2)		6.5	V
	RESET	–0.3	V_{DD} + 0.3	V
	All other pins (2)	–0.3	6.5	V
I_{OL}	Maximum low output current		5	mA
I_{OH}	Maximum high output current		–5	mA
I_{IK}	Input clamp current (V_I < 0 or V_I > V_{DD})		±20	mA
I_{OK}	Output clamp current (V_O < 0 or V_O > V_{DD})		±20	mA
	Continuous total power dissipation	See 节 6.8		
	Soldering temperature		260	°C
T_A	Operating free-air temperature	–40	85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND. For reliable operation, the device must not be operated at 7V for more than t = 1000h continuously.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

At specified temperature range.

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2	6	V
V_I	Input voltage	0	V_{DD} + 0.3	V
V_{IH}	High-level input voltage	0.7 × V_{DD}		V
V_{IL}	Low-level input voltage		0.3 × V_{DD}	V
$\Delta t/\Delta V$	Input transition rise and fall rate		100	ns/V
t_w	Pulse width of WDI trigger pulse	50		ns
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS3813xxx DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	208.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	123.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage		V_{DD} = 2V to 6V, I_{OL} = 500µA			0.2	V
			V_{DD} = 3.3V I_{OL} = 2mA			0.4	
			V_{DD} = 6V, I_{OL} = mA			0.4	
V_{POR}	Power up reset voltage (1)		$V_{DD} \geqslant$ 1.1V, I_{OL} = 50µA			0.2	V
V_{IT}	Negative-going input threshold voltage (2)	TPS3813J25	T_A = – 40°C to +85°C	2.2	2.25	2.3	V
		TPS3813L30		2.58	2.64	2.7	
		TPS3813K33		2.87	2.93	3	
		TPS3813I50		4.45	4.55	4.65	
V_{HYS}	Hysteresis	TPS3813J25			30		mV
		TPS3813L30			35		
		TPS3813K33			40		
		TPS3813I50			60		
I_{IH}	High-level input current	WDI, WDR	WDI = V_{DD} = 6V, WDR = V_{DD} = 6V	– 25		25	nA
		WDT	WDT = V_{DD} = 6V, V_{DD} > V_{IT}, $\overline{RESET}$ = High	– 100		100	
I_{IL}	Low-level input current	WDI, WDR	WDI = 0V, WDR = 0V, V_{DD} = 6V	– 25		25	
		WDT	WDT = 0V, V_{DD} > V_{IT}, $\overline{RESET}$ = High	– 100		100	
I_{OH}	High-level output current		V_{DD} = V_{IT} + 0.2V, V_{OH} = V_{DD}			25	nA
I_{DD}	Supply current		V_{DD} = 2V output unconnected		9	13	µA
			V_{DD} = 5V output unconnected		20	25	
C_i	Input capacitance		V_I = 0V to V_{DD}		5		pF

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, $V_{DD} \geqslant$ 15µs/V.
(2) To provide best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1µF) must be placed near to the supply terminals.

6.6 Timing Requirements

At R_L = 1MΩ, C_L = 50pF, and T_A = – 40°C to +85°C.

			MIN	TYP	MAX	UNIT
t_{GI_VIT}	Glitch immunity V_{IT} (Pulse width at V_{DD})	V_{DD} = V_{IT} + 0.2V, V_{DD} = V_{IT} – 0.2V	3			µs

6.7 Switching Characteristics

At R_L = 1MΩ, C_L = 50pF, and T_A = –40°C to +85°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time		$V_{DD} \geqslant V_{IT}$ + 0.2V, See 图 6-1	20	25	30	ms
$t_{t(out)}$	Watchdog time-out	Upper limit	WDT = 0V	0.2	0.25	0.3	s
			WDT = V_{DD}	2	2.5	3	
			WDT = programmable (1)		See (2)		ms
	Watchdog window ratio		WDR = 0V, WDT = 0V		1:31.8		
			WDR = 0V, WDT = V_{DD}		1:32		
			WDR = 0V, WDT = programmable		1:25.8		
			WDR = V_{DD}, WDT = 0V		1:124.9		
			WDR = V_{DD}, WDT = V_{DD}		1:127.7		
			WDR = V_{DD}, WDT = programmable		1:64.5		
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$ delay	$V_{IL} = V_{IT}$ – 0.2V, $V_{IH} = V_{IT}$ + 0.2V		30	50	µs

(1) 155pF < $C_{(ext)}$ < 63nF
(2) ($C_{(ext)}$ ÷ 15.55pF + 1) × 6.25ms

6.8 Dissipation Ratings

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 80°C POWER RATING
DBV	437mW	3.5mW/°C	280mW	227mW

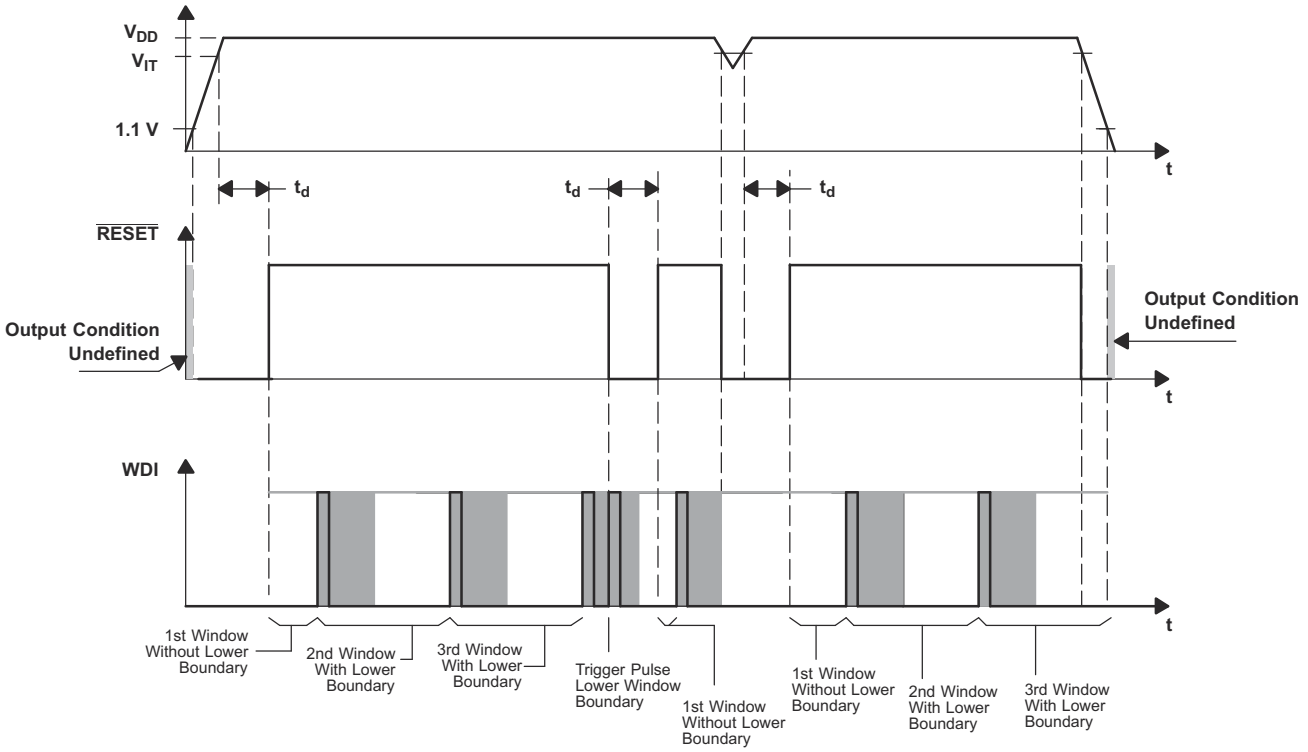


图 6-1. Timing Diagram

6.9 Typical Characteristics

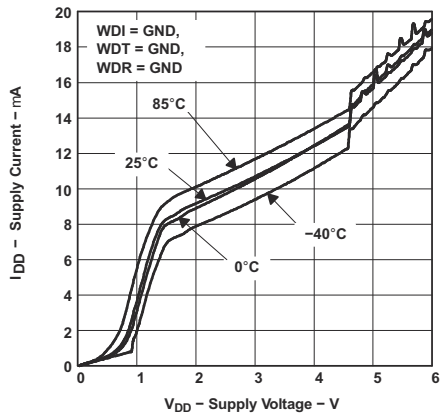


图 6-2. Supply Current vs Supply Voltage

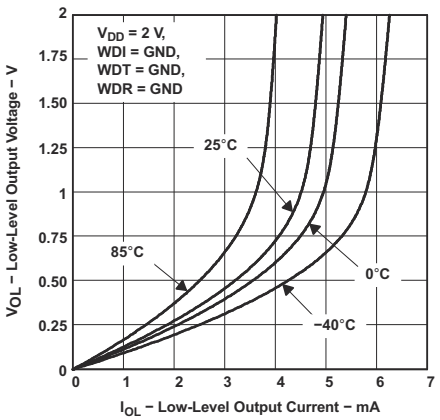


图 6-3. Low-Level Output Voltage vs Low-Level Output Current

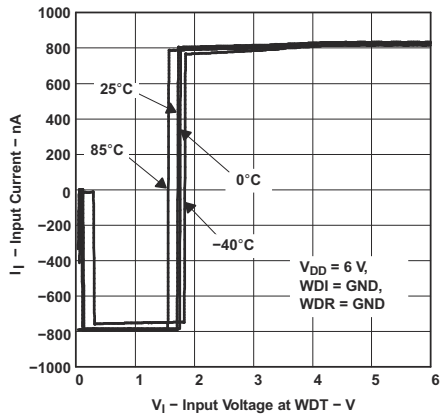


图 6-4. Input Current vs Input Voltage at WDT

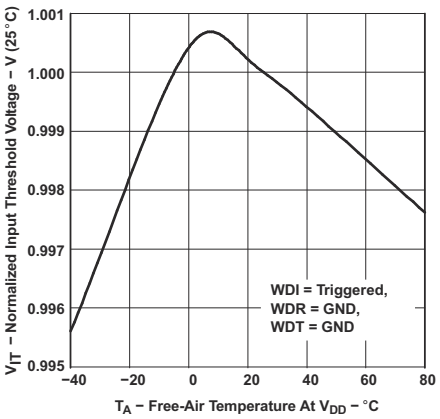


图 6-5. Normalized Input Threshold Voltage vs Free-Air Temperature at VDD

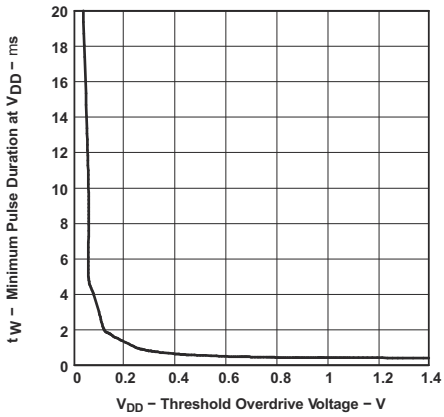


图 6-6. Minimum Pulse Duration at V_{DD} vs V_{DD} Threshold Overdrive Voltage

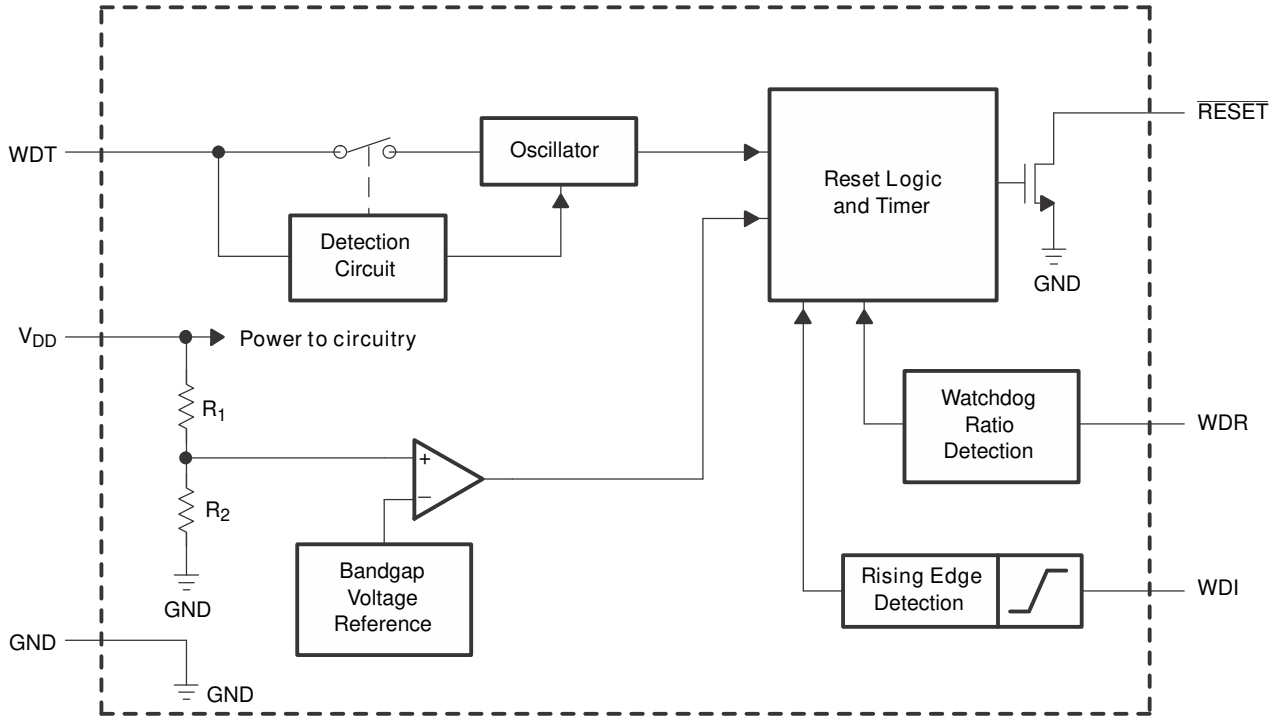
7 Detailed Description

7.1 Overview

The TPS3813xxx family of supervisory circuits provide circuit initialization and timing supervision signals. During power on, $\overline{\text{RESET}}$ is asserted (low) when the supply voltage (V_{DD}) increases above 1.1V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ low as long as V_{DD} remains below the threshold voltage (V_{IT}). Once V_{DD} increases above V_{IT}, an internal timer delays the deassertion of the output to allow for a proper system reset before $\overline{\text{RESET}}$ transitions to a high state. The delay time (t_d) is 25ms typical and starts after V_{DD} rises above the V_{IT}. When the supply voltage drops below V_{IT}, the output transitions low again. All the devices of this family have a fixed threshold voltage set by an internal voltage divider.

The TPS3813xxx family incorporates a so-called window-watchdog timer, which has a programmable delay and window ratio. The supervised processor must trigger the WDI pin of the TPS3813xxx within the user-programmable window to keep $\overline{\text{RESET}}$ from asserting. The upper limit of the watchdog time-out can be set by either connecting WDT to GND, V_{DD}, or using an external capacitor. The lower limit and thus the window ratio is set by connecting WDR to GND or V_{DD}.

7.2 Functional Block Diagram



7.3 Feature Description

The TPS3813xxx family incorporates both a voltage supervisor and a window-watchdog timer into a single device. The device monitors the input voltage and the supervised processor must trigger the WDI pin of the TPS3813xxx within the user-programmable window to keep RESET from asserting.

7.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator with integrated reference to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the following:

- Internal bandgap (reference voltage)
- Internal regulator
- State machine
- Buffers
- Other control logic blocks

Good design practice involves placing a 0.1µF to 1µF bypass capacitor at VDD input for noisy applications and to make sure enough charge is available for the device to power up correctly. The reset output is undefined when VDD is below V_{POR}.

7.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below the falling voltage threshold V_{IT}, the output reset is asserted. When the voltage at the VDD pin rises above the rising voltage threshold ($V_{IT+} = V_{IT} + V_{HYS}$), the output reset is deasserted after t_D reset time delay.

7.3.1.2 VDD Glitch Immunity

These devices are immune to quick voltage transient or excursion on VDD. Sensitivity to transients depends on both pulse duration (t_{GI_VIT}) found in *节 6.6* and transient overdrive. Overdrive is defined by how much VDD exceeds the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 方程式 1.

$$\text{Overdrive} = | ((VDD / V_{IT}) - 1) \times 100\% | \quad (1)$$

where

- $V_{IT} = V_{IT-}$ is the threshold voltage
- $V_{IT+} = V_{IT} + V_{HYS}$ is the rising threshold voltage
- VDD is the input voltage crossing V_{IT}

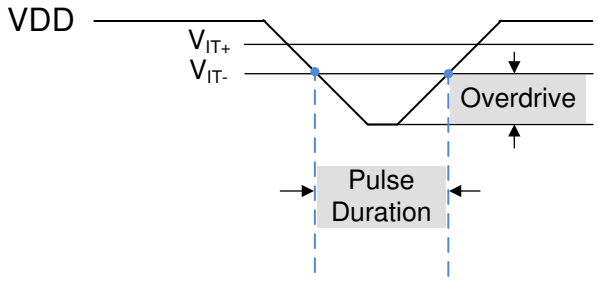


图 7-1. Overdrive Versus Pulse Duration

TPS3813xxx devices have built-in glitch immunity (t_{GI_VIT}) as shown in *节 6.6*. 图 7-1 shows that VDD must fall below V_{IT} for t_{GI_VIT}, otherwise the faling transistion is ignored. When VDD falls below V_{IT} for t_{GI_VIT}, $\overline{\text{RESET}}$ transitions low to indicate a fault condition after the propagation delay high-to-low (t_{PHL}). When VDD rises above $V_{IT+} = V_{IT} + V_{HYS}$, $\overline{\text{RESET}}$ deasserts to a logic high indicating there is no more fault condition only if VDD remains above V_{IT+} for longer than the reset delay (t_D).

7.3.2 User-Programmable Watchdog Timer (WDI)

The TPS3813xxx family of devices have a watchdog timer that must be periodically triggered by either a positive or negative transition at the WDI pin to avoid a reset signal being issued. When the supervising system fails to retrigger the watchdog circuit within the time-out interval, $t_{t(out)}$, $\overline{\text{RESET}}$ becomes asserts for the time period t_d. This event also reinitializes the watchdog timer. After the reset of the supervisor is released, the lower boundary of the first WDI window is disabled. After the first WDI low-to-high transition is detected, the lower boundary function of the window is enabled. All further WDI pulses must fit into the configured window frame.

Both the upper and lower boundary of the window can be adjusted by the user. See 节 7.5 for more details on how to set the upper and lower boundaries of the window.

7.3.3 $\overline{\text{RESET}}$ Output

$\overline{\text{RESET}}$ remains high (deasserted) as long as V_{DD} is above the threshold voltage (V_{IT}) and the user-programable watchdog timer criteria are met. If V_{DD} falls below the V_{IT} or if WDI is not triggered within the appropriate window, then RESET is asserted, driving the $\overline{\text{RESET}}$ pin to a low impedance.

When V_{DD} is once again above V_{IT}, a delay circuit is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period (t_d) which is 25ms typical. When the reset delay has elapsed, the $\overline{\text{RESET}}$ pin goes to a high-impedance state and uses a pullup resistor to hold $\overline{\text{RESET}}$ high. Connect the pullup resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level. $\overline{\text{RESET}}$ can be pulled up to any voltage up to 6V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor value and consider the required low-level output voltage (V_{OL}), the output capacitive loading, and the output leakage current.

7.4 Device Functional Modes

表 7-1 summarizes the various functional modes of the device.

表 7-1. TPS3813xxx Function/Truth Table

V_{DD}	WDI	$\overline{\text{RESET}}$
$V_{DD} < V_{POR}$	—	Undefined
$V_{POR} < V_{DD} < V_{IT}$	—	L
$V_{DD} > V_{IT}$	Outside window	L
$V_{DD} > V_{IT}$	Inside window	H

7.4.1 Normal Operation ($V_{DD} > V_{IT}$)

When V_{DD} is greater than V_{IT}, the $\overline{\text{RESET}}$ signal is determined by the last WDI pulse.

- WDI pulse inside window: as long as pulses occur within the user-programmable window, the $\overline{\text{RESET}}$ signal remains high.
- WDI pulse outside window: if a pulse occurs outside the user-programmable window or not at all, the $\overline{\text{RESET}}$ signal goes low.

7.4.2 Above Power-On Reset But Less Than Threshold ($V_{POR} < V_{DD} < V_{IT}$)

When the voltage on V_{DD} is less than the V_{IT} voltage, and greater than the power-on reset voltage (V_{POR}), the $\overline{\text{RESET}}$ signal is asserted regardless of the WDI signal.

7.4.3 Below Power-On Reset ($V_{DD} < V_{POR}$)

When the voltage on V_{DD} is lower than V_{POR}, the device does not have enough voltage to internally pull the asserted output low, and $\overline{\text{RESET}}$ is undefined and must not be relied upon for proper device function.

7.5 Programming

7.5.1 Implementing Window-Watchdog Settings

There are two ways to configure the watchdog timer window the most flexible is to connect a capacitor to WDT to set the upper boundary of the window watchdog while connecting WDR to either V_{DD} or GND, thus setting the lower boundary. The other way to configure the timing is by wiring the WDT and WDR pin to either V_{DD} or GND. By hard-wiring the pins to either V_{DD} or GND there are four different timings available; these settings are listed in 表 7-2.

表 7-2. Cap-Free Timer Settings

SELECTED OPERATION MODE		WINDOW FRAME	LOWER WINDOW FRAME
WDT = 0V	WDR = 0V	Max = 0.3s	Max = 9.46ms
		Typ = 0.25s	Typ = 7.86ms
		Min = 0.2s	Min = 6.27ms
	WDR = V_{DD}	Max = 0.3s	Max = 2.43ms
		Typ = 0.25s	Typ = 2ms
		Min = 0.2s	Min = 1.58ms
WDT = V_{DD}	WDR = 0V	Max = 3s	Max = 93.8ms
		Typ = 2.5s	Typ = 78.2ms
		Min = 2s	Min = 62.5ms
	WDR = V_{DD}	Max = 3s	Max = 23.5ms
		Typ = 2.5s	Typ = 19.6ms
		Min = 2s	Min = 15.6ms

To visualize the values named in the table, a timing diagram was prepared. It is used to describe the upper and lower boundary settings. For an application, the important boundaries are the $t_{boundary,max}$ and $t_{window,min}$. Within these values, the watchdog timer must be retriggered to avoid a time-out condition or a boundary violation in the event of a trigger pulse in the lower boundary. The values in the table above are typical and worst-case conditions and are valid over the whole temperature range of –40°C to +85°C.

The shaded areas shown in 图 7-2 are cases where undefined operation can happen. This device can not detect a violation if a WDI pulse occurs within these three shaded areas. The first shaded area addresses the situation of two consecutive rising edges occur within a quick amount of time. The typical time between rising edges must be more than 500µs. The second and third shaded areas are defined by the min and max variance of the lower boundary ($t_{boundary}$) and upper boundary (t_{window}). Set the WDI rising edge within the $t_{boundary,max}$ and $t_{window,min}$ for correct operation.

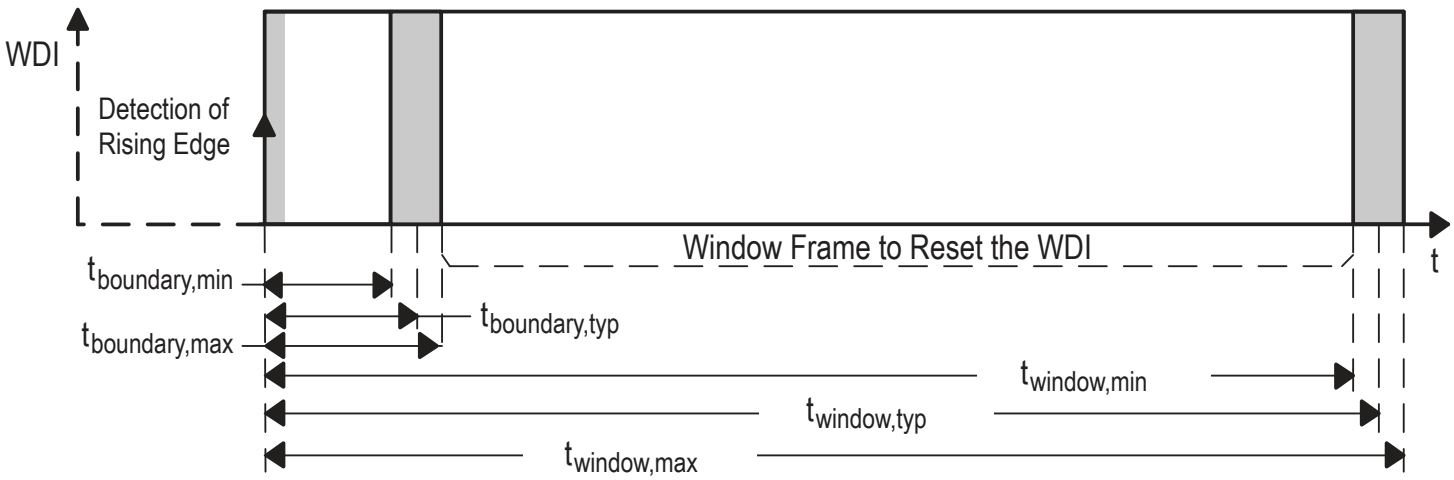


图 7-2. Upper and Lower Boundary Visualization

7.5.2 Programmable Window-Watchdog by Using an External Capacitor

The upper boundary of the watchdog timer can be set by an external capacitor connected between the WDT pin and GND. Common consumer electronic capacitors can be used to implement this feature. They must have low ESR, low leakage (< 5nA) and low tolerances because the tolerances have to be considered if the calculations are performed. The first formula is used to calculate the upper window frame. After calculating the upper window frame, the lower boundary can be calculated. As in the last example, the most important values are the $t_{boundary,max}$ and $t_{window,min}$. The trigger pulse has to fit into this window frame.

The external capacitor must have a value between a minimum of 155pF and a maximum of 63nF.

表 7-3. Setting Upper Window Using External Capacitor

SELECTED OPERATION MODE		WINDOW FRAME
WDT = external capacitor $C_{(ext)}$	WDR = 0V and WDR = V_{DD}	$t_{window,max} = 1.25 \times t_{window,typ}$
		$t_{window,min} = 0.75 \times t_{window,typ}$

$$t_{window,typ} = \left(\frac{C_{(ext)}}{15.55\ pF} + 1 \right) \times 6.25\ ms \quad (2)$$

7.5.3 Lower Boundary Calculation

The lower boundary can be calculated based on the values given in 节 6.7. Additionally, facts must be considered to verify that the lower boundary is where it is expected. Because the internal oscillator of the window watchdog is running free, any rising edge at the WDI pin is considered at the next internal clock cycle. This happens regardless of the external source. Because the shift between internal and external clock is not known, it is best to consider the worst-case condition for calculating this value.

表 7-4. Setting Lower Boundary Using External Cap

SELECTED OPERATION MODE		LOWER BOUNDARY OF FRAME
WDT = external capacitor $C_{(ext)}$	WDR = 0V	$t_{boundary,max} = t_{window,max} / 23.5$
		$t_{boundary,typ} = t_{window,typ} / 25.8$
		$t_{boundary,min} = t_{window,min} / 28.7$
	WDR = V_{DD}	$t_{boundary,max} = t_{window,max} / 51.6$
		$t_{boundary,typ} = t_{window,typ} / 64.5$
		$t_{boundary,min} = t_{window,min} / 92.7$

7.5.4 Watchdog Software Considerations

To benefit from the window watchdog feature and help the watchdog timer monitor the software execution more closely, TI recommends that the watchdog be set and reset at different points in the program rather than pulsing the watchdog input periodically by using the prescaler of a microcontroller or DSP. Furthermore, the watchdog trigger pulses must be set to different timings inside the window frame to release a defined reset, if the program must hang in any subroutine. This allows the window watchdog to detect time-outs of the trigger pulse, as well as pulses that distort the lower boundary.

7.5.5 Power-Up Considerations

Many microcontrollers use general-purpose input and output (GPIO) pins that can be programmed to be either inputs or outputs. During power-up, these I/O pins are typically configured as inputs. If a GPIO pin is used to drive the WDI input pin of the TPS3813xxx, then a pulldown resistor (shown as R2 in 图 8-1) must be added to keep the WDI pin from floating during power up.

8 Application and Implementation

备注

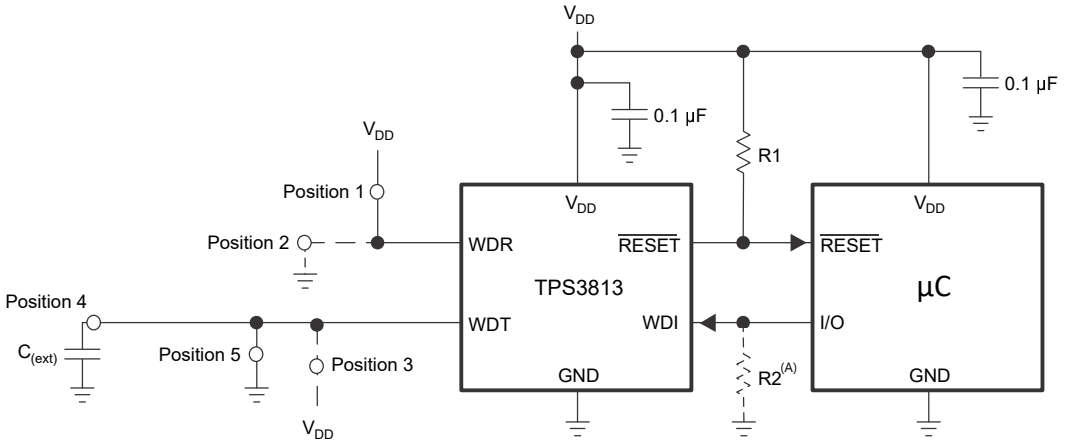
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS3813xxx is a voltage supervisor that incorporates a window-watchdog timer, allowing for comprehensive supervision of microcontrollers and other similar devices. The TPS3813xxx can be operated from a VDD rail of 2V to 6V with a user-programmable watchdog time-out from 0.25s to 2.5s. The following sections describe how to properly use this device, depending on the requirements of the final application.

8.2 Typical Application

A typical application example (see 图 8-1) is used to describe the function of the watchdog in more detail. To configure the window watchdog function, two pins are provided by the TPS3813xxx. These pins set the window time-out and ratio. The window watchdog ratio is a fixed ratio, which determines the lower boundary of the window frame. It can be configured in two different frame sizes.



A. Use this pulldown resistor if a GPIO pin is used to drive the WDI input pin of the TPS3813xxx to keep the WDI pin from floating during power up.

图 8-1. Application Example

8.2.1 Design Requirements

The TPS3813xxx $\overline{\text{RESET}}$ output can be used to drive the $\overline{\text{RESET}}$ pin of a microcontroller to initiate a reset event. The $\overline{\text{RESET}}$ pin of the TPS3813xxx can be pulled high with a 1MΩ resistor; the watchdog window timing is controlled by the WDT and WDR pins, and is set depending on the reset requirement times of the microprocessor.

8.2.2 Detailed Design Procedure

If the window watchdog ratio pin (WDR) is set to V_{DD}, Position 1 in 图 8-1, then the lower window frame is a value based on a ratio calculation of the overall window time-out size: For the watchdog time-out pin (WDT) connected to GND, it is a ratio of 1:124.9, for WDT connected to V_{DD}, it is a ratio of 1:127.7, and for an external capacitor connected to WDT, it is a ratio of 1:64.5.

If the window watchdog ratio pin (WDR) is set to GND, Position 2, the lower window frame is a value based on a ratio calculation of the overall window time-out size: For the watchdog time-out pin (WDT) connected to GND, it is a ratio of 1:31.8, for WDT connected to V_{DD} it is 1:32, and for an external capacitor connected to WDT it is 1:25.8.

The watchdog time-out can be set in two fixed timings of 0.25 seconds and 2.5 seconds for the window or can by programmed by connecting a external capacitor with a low leakage current at WDT.

Example: If the watchdog time-out pin (WDT) is connected to V_{DD}, the time-out is 2.5 seconds. If the window watchdog ratio pin (WDR) is set in this configuration to a ratio of 1:127.7 by connecting the pin to V_{DD}, the lower boundary is 19.6ms.

8.2.3 Application Curve

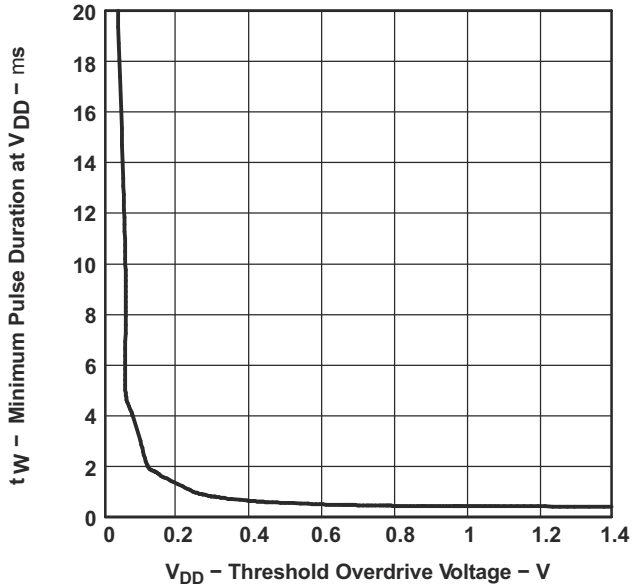


图 8-2. Minimum Pulse Duration at V_{DD} vs V_{DD} Threshold Overdrive Voltage

8.3 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range from 2V to 6V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1µF capacitor between the VDD pin and the GND pin. This device has a 7V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7V, additional precautions must be taken.

In applications where the WDI input can experience a negative voltage while V_{DD} is ramping from 0V to 0.8V, the V_{DD} slew rate in this range must be greater than 10V/s. A negative voltage on the WDI input along with a slew rate less than 10V/s can result in a greatly reduced watchdog window time and reset output delay time.

8.4 Layout

8.4.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1µF ceramic bypass capacitor near the VDD pin.

8.4.2 Layout Example

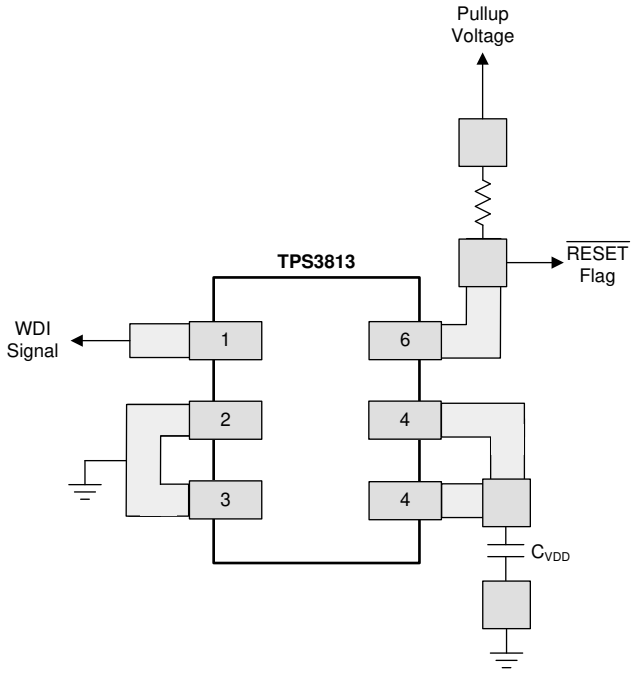


图 8-3. TPS3813xxx Layout Example

9 Device and Documentation Support

9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS3813J25	Click here	Click here	Click here	Click here	Click here
TPS3813L30	Click here	Click here	Click here	Click here	Click here
TPS3813K33	Click here	Click here	Click here	Click here	Click here
TPS3813I50	Click here	Click here	Click here	Click here	Click here

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (October 2021) to Revision J (October 2023)	Page
• Changed absolute maximum voltage rating to 6.5V	4
• Changed ESD HBM rating to 2000V post qualification	4
• Changed ESD CDM rating to 750V post qualification	4
• Updated 图 7-2 and description	11
• Updated external capacitor recommendation to have low leakage , ESR and tolerances	13

Changes from Revision H (February 2016) to Revision I (October 2021) **Page**

- Changed t_w parameter name to t_{GI_VIT} in *7.6 Timing Requirements* section and added *Glitch immunity* V_{IT} in parameter definition. 5
- Added Input Voltage (VDD), VDD Hysteresis, and VDD Glitch Immunity sections into datasheet..... 9

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3813I50DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	PFBI
TPS3813I50DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	PFBI
TPS3813I50DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	PFBI
TPS3813I50DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFBI
TPS3813J25DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	PCDI
TPS3813J25DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCDI
TPS3813J25DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	PCDI
TPS3813J25DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCDI
TPS3813K33DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	PFAI
TPS3813K33DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFAI
TPS3813K33DBVRG4	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TPS3813K33DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	PFAI
TPS3813K33DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PFAI
TPS3813L30DBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	PEZI
TPS3813L30DBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PEZI
TPS3813L30DBVT	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	PEZI
TPS3813L30DBVT.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PEZI

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS3813 :

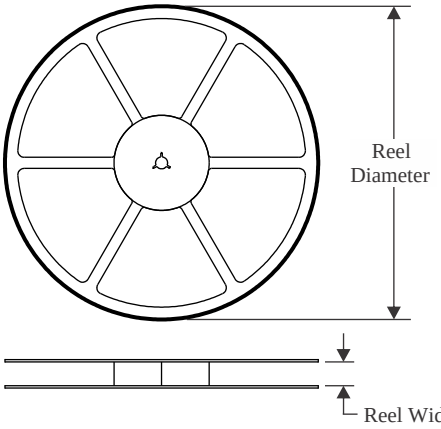
- Automotive : TPS3813-Q1

NOTE: Qualified Version Definitions:

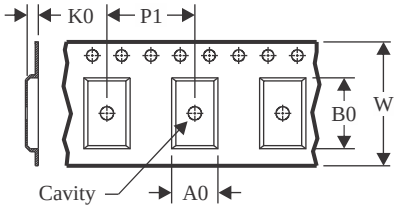
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

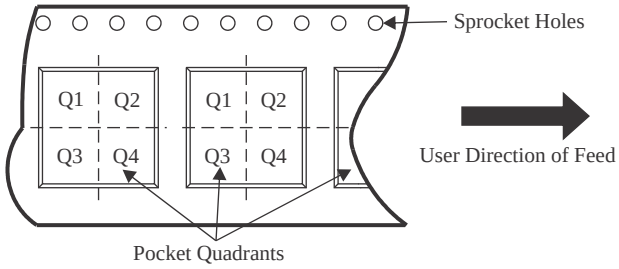


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

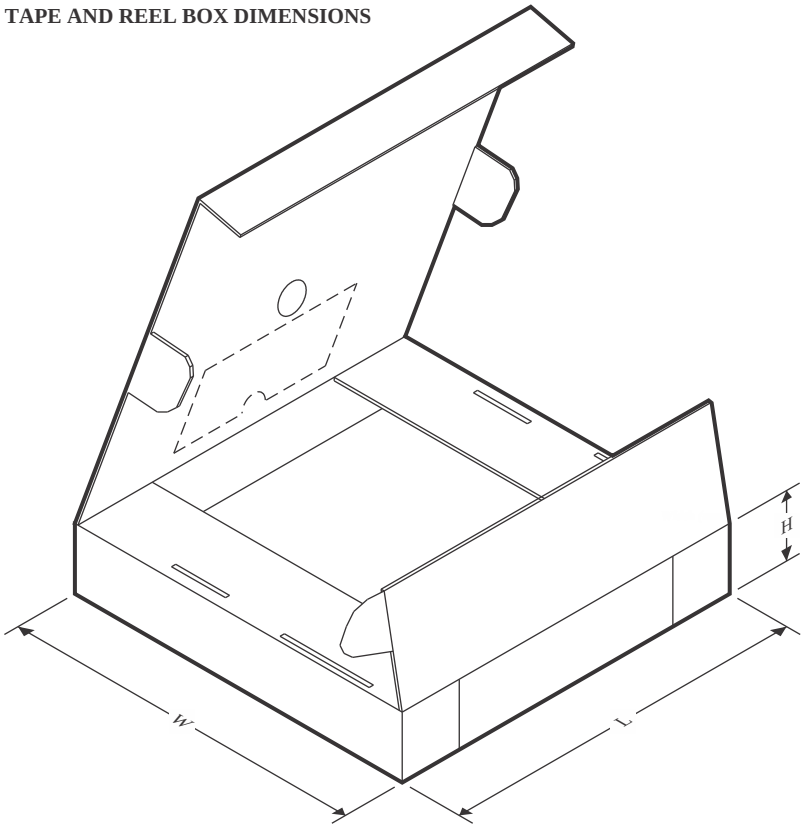
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3813I50DBVR	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3813I50DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3813I50DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3813J25DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3813J25DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3813J25DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3813J25DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3813K33DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3813K33DBVR	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3813K33DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3813L30DBVR	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3813L30DBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

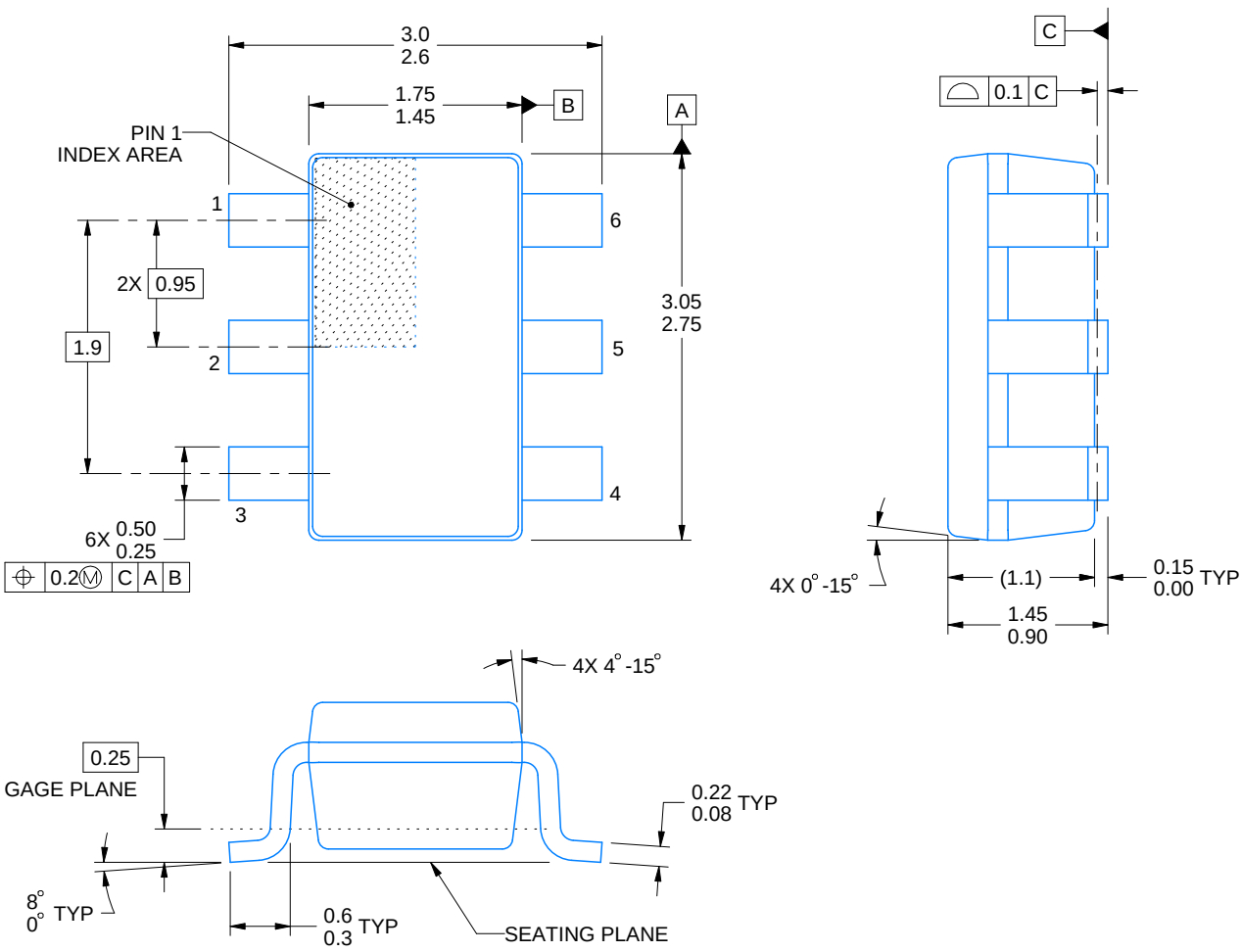
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3813I50DBVR	SOT-23	DBV	6	3000	208.0	191.0	35.0
TPS3813I50DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3813I50DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TPS3813J25DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3813J25DBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS3813J25DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TPS3813J25DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS3813K33DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3813K33DBVR	SOT-23	DBV	6	3000	208.0	191.0	35.0
TPS3813K33DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0
TPS3813L30DBVR	SOT-23	DBV	6	3000	208.0	191.0	35.0
TPS3813L30DBVT	SOT-23	DBV	6	250	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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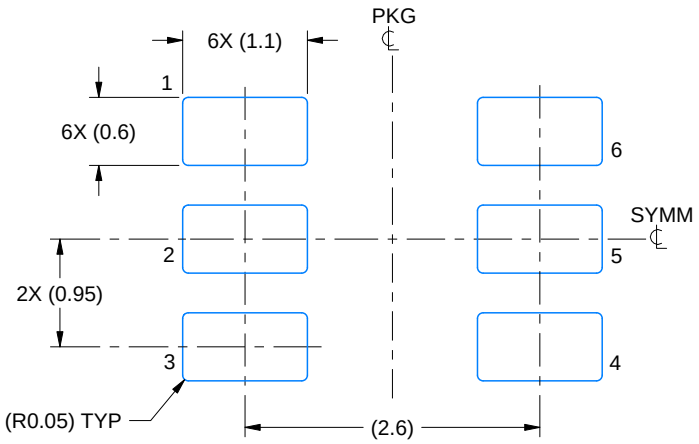
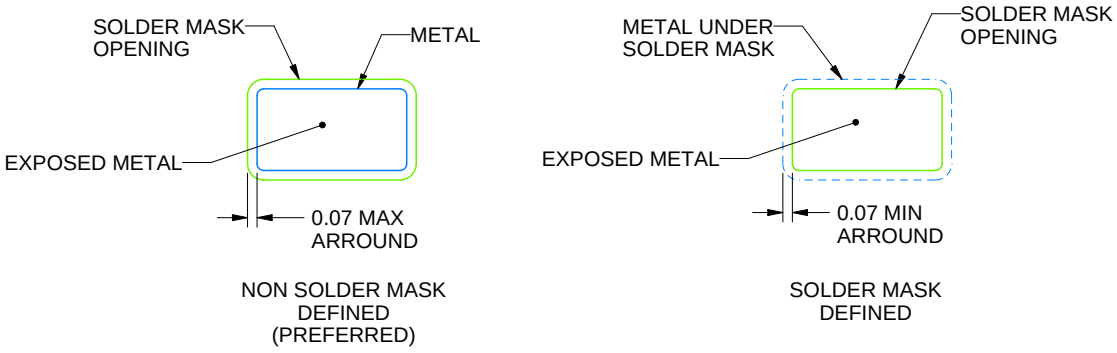
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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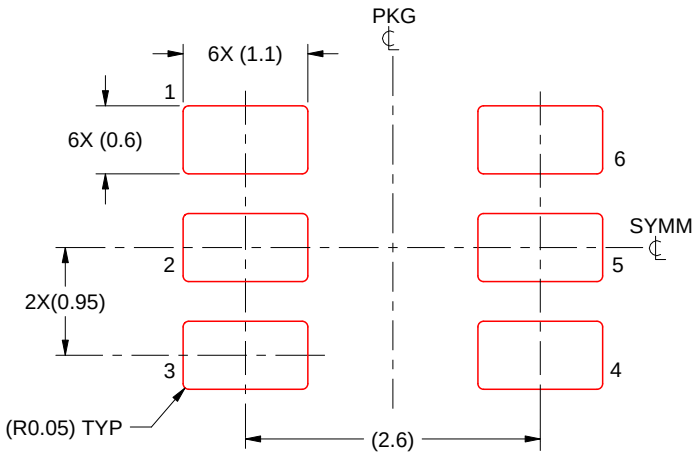
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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