

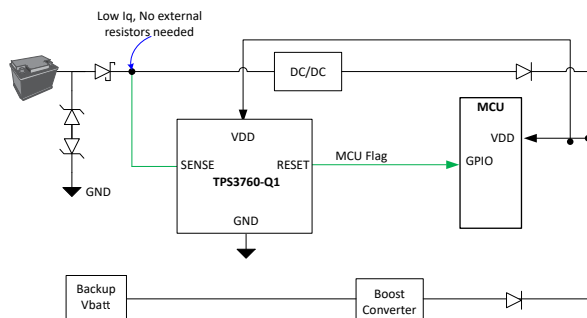
## TPS3760-Q1 适用于汽车、具有可编程检测和复位延迟功能的高电压监控器

### 1 特性

- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 +125°C 环境温度工作温度范围  $T_A$
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C7B
- 提供功能安全
  - 有助于进行功能安全系统设计的文档
- 宽电源电压范围：2.7V 至 65V
- SENSE 和 RESET 引脚为 65V 等级
- 低静态电流：1  $\mu\text{A}$  (典型值)
- 灵活而广泛的电压阈值选项
  - 表 10-1
  - 2.7V 至 36V (最高精度 1.5%)
  - 800 mV 选项 (最高精度 1%)
- 内置迟滞 ( $V_{HYS}$ )
  - 百分比选项：2% 至 13% (阶跃 1%)
  - 固定选项： $V_{TH} < 8V = 0.5V、1V、1.5V、2V、2.5V$
- 可编程复位延时时间
  - 10nF = 12.8ms、10  $\mu\text{F}$  = 12.8s
- 可编程感测延时时间
  - 10nF = 1.28ms、10  $\mu\text{F}$  = 1.28s
- 手动复位 ( $\overline{\text{MR}}$ ) 特性
- 输出复位锁存特性
- 输出拓扑：开漏或推挽

### 2 应用

- 远程信息处理控制单元
- 紧急呼叫系统
- 音频放大器
- 音响主机和组合仪表
- 传感器融合和摄像头
- 车身控制模块



典型应用电路

### 3 说明

TPS3760-Q1 是一款 65V 输入电压检测器， $I_{DD}$  为 1  $\mu\text{A}$ ，精度为 1%，检测时间短。该器件可直接连接到 12V/24V 汽车电池系统，用于持续监测过压 (OV) 或欠压 (UV) 情况；由于使用内部电阻分压器，它的总体解决方案尺寸非常小。由于提供了广泛的迟滞电压选项，可以忽略冷启动、启停和各种汽车电池电压瞬变。SENSE 引脚上的内置迟滞特性有助于在监测电源电压轨时防止出现错误的复位信号。

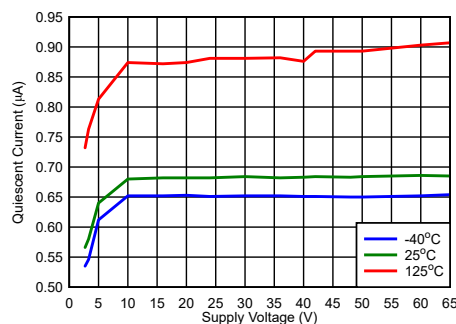
通过单独的 VDD 和 SENSE 引脚，可实现高可靠性汽车系统所需的冗余，并且 SENSE 引脚可以监控比 VDD 更高和更低的电压。SENSE 引脚的高阻抗输入支持使用可选的外部电阻器。通过 CTS 和 CTR 引脚，可以对 RESET 信号的上升沿和下降沿进行延迟调整。此外，CTS 可忽略受监控电压轨上产生的电压干扰，从而充当去抖动器；CTR 具有手动复位 ( $\overline{\text{MR}}$ ) 的作用，可用于强制系统复位。

TPS3760 采用 4.1mm × 1.9mm 14 引脚 SOT 封装。TPS3760 工作温度范围为 -40°C 至 +125°C  $T_A$ 。

#### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 (标称值)
TPS3760-Q1	SOT-23 (14) (DYY)	4.1 mm × 1.9 mm

(1) 如需了解封装详细信息，请参阅数据表末尾的机械制图附录。



典型  $I_{DD}$  与  $V_{DD}$



## Table of Contents

<b>1 特性</b> .....	<b>1</b>	8.3 Feature Description.....	<b>18</b>
<b>2 应用</b> .....	<b>1</b>	8.4 Device Functional Modes.....	<b>27</b>
<b>3 说明</b> .....	<b>1</b>	<b>9 Application and Implementation</b> .....	<b>28</b>
<b>4 Revision History</b> .....	<b>2</b>	9.1 Application Information.....	<b>28</b>
<b>5 Device Comparison</b> .....	<b>3</b>	9.2 Adjustable Voltage Thresholds.....	<b>28</b>
<b>6 Pin Configuration and Functions</b> .....	<b>4</b>	9.3 Typical Application.....	<b>29</b>
<b>7 Specifications</b> .....	<b>6</b>	9.4 Power Supply Recommendations.....	<b>32</b>
7.1 Absolute Maximum Ratings.....	<b>6</b>	9.5 Layout.....	<b>32</b>
7.2 ESD Ratings.....	<b>6</b>	<b>10 Device and Documentation Support</b> .....	<b>35</b>
7.3 Recommended Operating Conditions.....	<b>6</b>	10.1 Device Nomenclature.....	<b>35</b>
7.4 Thermal Information.....	<b>6</b>	10.2 接收文档更新通知.....	<b>36</b>
7.5 Electrical Characteristics.....	<b>7</b>	10.3 支持资源.....	<b>36</b>
7.6 Timing Requirements.....	<b>9</b>	10.4 Trademarks.....	<b>36</b>
7.7 Timing Diagrams.....	<b>10</b>	10.5 静电放电警告.....	<b>36</b>
7.8 Typical Characteristics.....	<b>13</b>	10.6 术语表.....	<b>36</b>
<b>8 Detailed Description</b> .....	<b>17</b>	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>36</b>
8.1 Overview.....	<b>17</b>		
8.2 Functional Block Diagram.....	<b>17</b>		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision * (March 2022) to Revision A (May 2023)</b>	<b>Page</b>
• Added Latch nomenclature.....	<b>3</b>
• Removed DSK pinout description.....	<b>4</b>
• Added CTS and CTR timing plots.....	<b>13</b>
• Added Reset latch mode information.....	<b>26</b>
• Added correct Package Outline figure.....	<b>36</b>

## 5 Device Comparison

Voltage Threshold Hysteresis

TPS3760
X
X
XX
X
DYY
R-Q1

**Topology**

Suffix	CH1
A	UV OD L
B	UV PP L
C	UV OD H
D	UV PP H
E	OV OD L
F	OV PP L
G	OV OD H
H	OV PP H

**LATCH**

Suffix	Name
L	LATCH
	NO LATCH

**Threshold Voltage**

100mV steps				400mV steps		500mV steps		1V steps	
Suffix	VIT	Suffix	VIT	Suffix	VIT	Suffix	VIT	Suffix	VIT
01	800mV	70	7.0V	A0	10.4V	D0	20.5V	F0	31.0V
27	2.7V	71	7.1V	A1	10.8V	D1	21.0V	F1	32.0V
28	2.8V	72	7.2V	A2	11.2V	D2	21.5V	F2	33.0V
29	2.9V	73	7.3V	A3	11.6V	D3	22.0V	F3	34.0V
30	3.0V	74	7.4V	A4	12.0V	D4	22.5V	F4	35.0V
31	3.1V	75	7.5V	A5	12.4V	D5	23.0V	F5	36.0V
32	3.2V	76	7.6V	A6	12.8V	D6	23.5V		
33	3.3V	77	7.7V	A7	13.2V	D7	24.0V		
34	3.4V	78	7.8V	A8	13.6V	D8	24.5V		
35	3.5V	79	7.9V	A9	14.0V	D9	25.0V		
36	3.6V	80	8.0V	B0	14.4V	E0	25.5V		
37	3.7V	81	8.1V	B1	14.8V	E1	26.0V		
38	3.8V	82	8.2V	B2	15.2V	E2	26.5V		
39	3.9V	83	8.3V	B3	15.6V	E3	27.0V		
40	4.0V	84	8.4V	B4	16.0V	E4	27.5V		
41	4.1V	85	8.5V	B5	16.4V	E5	28.0V		
42	4.2V	86	8.6V	B6	16.8V	E6	28.5V		
43	4.3V	87	8.7V	B7	17.2V	E7	29.0V		
44	4.4V	88	8.8V	B8	17.6V	E8	29.5V		
45	4.5V	89	8.9V	B9	18.0V	E9	30.0V		
46	4.6V	90	9.0V	C0	18.4V				
47	4.7V	91	9.1V	C1	18.8V				
48	4.8V	92	9.2V	C2	19.2V				
49	4.9V	93	9.3V	C3	19.6V				
50	5.0V	94	9.4V	C4	20.0V				
51	5.1V	95	9.5V						
52	5.2V	96	9.6V						
53	5.3V	97	9.7V						
54	5.4V	98	9.8V						
55	5.5V	99	9.9V						
56	5.6V	00	10.0V						
57	5.7V								
58	5.8V								
59	5.9V								
60	6.0V								
61	6.1V								
62	6.2V								
63	6.3V								
64	6.4V								
65	6.5V								
66	6.6V								
67	6.7V								
68	6.8V								
69	6.9V								

**Hysteresis**

Suffix	CH1
2	2%
3	3%
4	4%
5	5%
6	6%
7	7%
8	8%
9	9%
A	10%
B	11%
C	12%
D	13%
E	0.5V
F	1V
G	1.5V
H	2V
I	2.5V

**Package**

Suffix	Name
DYY	SOT-23

**Reel**

Suffix	Name
R	Large

**Rating**

Suffix	Name
Q1	AUTO
	INDUSTRIAL

1. Sense logic: OV = overvoltage; UV = undervoltage
2. Reset topology: PP = Push-Pull; OD = Open-Drain
3. Reset logic: L = Active-Low; H = Active-High
4. A to I hysteresis options are only available for 2.9 V to 8V threshold options
5. Suffix 01 with VIT of 800mV corresponds to the adjustable variant, does not have internal voltage divider

## 6 Pin Configuration and Functions

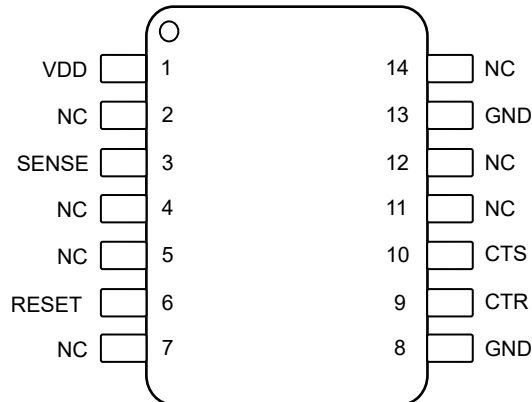


图 6-1. DYY Package,  
14-Pin SOT-23,  
TPS3760-Q1 (Top View)

表 6-1. Pin Functions

PIN NAME	SOT23 (DYY) NO.	I/O	DESCRIPTION
VDD	1	I	<b>Input Supply Voltage:</b> Bypass with a 0.1 $\mu$ F capacitor to GND.
SENSE	3	I	<b>Sense Voltage:</b> The voltage monitored by this pin is compared to the internal voltage threshold, $V_{th}$ , that is determined by an internal voltage divider for fixed variants or an external voltage divider for adjustable variants. When the SENSE pin detects a fault, $\overline{\text{RESET}}/\text{RESET}$ asserts after the sense time delay, set by CTS. When the voltage on the SENSE pin transitions back past $V_{th}$ and hysteresis, $V_{HYS}$ , $\overline{\text{RESET}}/\text{RESET}$ deasserts after the reset time delay, set by CTR. For noisy applications, placing a 10 nF to 100 nF ceramic capacitor close to this pin may be needed for optimum performance. <b>Sensing Topology: Overvoltage (OV) or Undervoltage (UV)</b>
$\overline{\text{RESET}}/\text{RESET}$	6	O	<b>Output Reset Signal:</b> See Device Comparison for output topology options. $\overline{\text{RESET}}/\text{RESET}$ asserts when SENSE crosses the voltage threshold after the sense time delay, set by CTS. $\overline{\text{RESET}}/\text{RESET}$ remains asserted for the reset time delay period after SENSE transitions out of a fault condition. For active low open-drain reset output, an external pullup resistor is required. Do not place external pullup resistors on push-pull outputs. <b>Output topology: Open Drain or Push Pull, Active Low or Active High</b>
CTS /LATCH	10	O	<b>SENSE Time Delay:</b> Capacitor programmable sense delay: CTS pin offers a user-adjustable sense delay time when asserting a reset condition. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}/\text{RESET}$ delay time to assert. <b>LATCH:</b> CTS functionality is disabled in latch capable devices. When latch mode is activated, $\overline{\text{RESET}}/\text{RESET}$ will not de-assert even if the fault is cleared. To activate latch mode, the LATCH pin has to be driven low, to at least 1.4V. It is recommended to have a 10k $\Omega$ pull-down to ground. To deactivate latch mode, a 2.1V or greater for 3 $\mu$ s has to be applied to the LATCH pin while SENSE pin is not detecting a fault. $\overline{\text{RESET}}/\text{RESET}$ will de-assert with delay $t_{ctr}$ starting on the rising edge of the deactivating signal.
CTR / $\overline{\text{MR}}$	9	-	<b>RESET Time Delay:</b> User-programmable reset time delay for $\overline{\text{RESET}}/\text{RESET}$ . Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. <b>Manual Reset:</b> If this pin is driven low, the $\overline{\text{RESET}}/\text{RESET}$ output will reset and become asserted. The pin can be left floating or be connected to a capacitor. This pin should not be driven high.

**表 6-1. Pin Functions (continued)**

PIN	SOT23 (DYY)	I/O	DESCRIPTION
NAME	NO.		
GND	8, 13	-	<b>Ground.</b> All GND pins must be electrically connected to the board ground.
NC	2, 4, 5, 7, 11,12, 14	-	NC stands for “No Connect.” The pins are to be left floating.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted <sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	V <sub>DD</sub> , V <sub>SENSE</sub> , V <sub>RESET</sub> , V <sub>RESET</sub>	- 0.3	70	V
Voltage	V <sub>CTS</sub> , V <sub>CTR</sub>	- 0.3	6	V
Current	I <sub>RESET</sub> , I <sub>RESET</sub>		10	mA
Temperature <sup>(2)</sup>	Operating junction temperature, T <sub>J</sub>	- 40	150	°C
Temperature <sup>(2)</sup>	Operating Ambient temperature, T <sub>A</sub>	- 40	150	°C
Temperature <sup>(2)</sup>	Storage, T <sub>stg</sub>	- 65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that T<sub>J</sub> = T<sub>A</sub>.

### 7.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V <sub>DD</sub>	2.7		65	V
Voltage	V <sub>SENSE</sub> , V <sub>RESET</sub> , V <sub>RESET</sub>	0		65	V
Voltage	V <sub>CTS</sub> , V <sub>CTR</sub>	0		5.5	V
Current	I <sub>RESET</sub> , I <sub>RESET</sub>	0		±5	mA
T <sub>J</sub>	Junction temperature (free air temperature)	- 40		125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS3760-Q1		UNIT
		DYY		
		14-PIN		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	131.5		°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	61.1		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	56.6		°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	3.4		°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	56.5		°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A		°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

At  $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$ ,  $CTR/\overline{MR} = CTS = \text{open}$ , output reset pull-up resistor  $R_{PU} = 10 \text{ k}\Omega$ , voltage  $V_{PU} = 5.5 \text{ V}$ , and load  $C_{LOAD} = 10 \text{ pF}$ . The operating free-air temperature range  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 16 \text{ V}$  and  $V_{IT} = 6.5 \text{ V}$  ( $V_{IT}$  refers to  $V_{ITN}$  or  $V_{ITP}$ ).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VDD</b>						
$V_{DD}$	Supply Voltage		2.7		65	V
UVLO <sup>(1)</sup>	Under Voltage Lockout	$V_{DD}$ Falling below $V_{DD(MIN)}$			2.7	V
$V_{POR}$	Power on Reset Voltage <sup>(2)</sup> RESET, Active Low (Open-Drain, Push-Pull )	$V_{OL(MAX)} = 300 \text{ mV}$ $I_{OUT(Sink)} = 15 \mu\text{A}$			1.4	V
$V_{POR}$	Power on Reset Voltage <sup>(2)</sup> RESET, Active High (Push-Pull )	$V_{OH(MIN)} = 0.8 \times V_{DD}$ $I_{OUT(Source)} = 15 \mu\text{A}$			1.4	V
$I_{DD}$	Supply current into VDD pin	$V_{IT} = 800 \text{ mV}$ $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$		1	2.6	$\mu\text{A}$
		$V_{IT} = 2.7 \text{ V to } 36 \text{ V}$ $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$		1	2	$\mu\text{A}$
<b>SENSE (Input)</b>						
$I_{SENSE}$	Input current	$V_{IT} = 800 \text{ mV}$			100	nA
$I_{SENSE}$	Input current	$V_{IT} < 10 \text{ V}$			0.8	$\mu\text{A}$
$I_{SENSE}$	Input current	$10 \text{ V} < V_{IT} < 26 \text{ V}$			1.2	$\mu\text{A}$
$I_{SENSE}$	Input current	$V_{IT} > 26 \text{ V}$			2	$\mu\text{A}$
$V_{ITN}$	Input Threshold Negative (Undervoltage)	$V_{IT} = 2.7 \text{ V to } 36 \text{ V}$	-1.5		1.5	%
		$V_{IT} = 800 \text{ mV}$ <sup>(3)</sup>	0.792	0.800	0.808	V
$V_{ITP}$	Input Threshold Positive (Overvoltage)	$V_{IT} = 2.7 \text{ V to } 36 \text{ V}$	-1.5		1.5	%
		$V_{IT} = 800 \text{ mV}$ <sup>(3)</sup>	0.792	0.800	0.808	V
$V_{HYS}$	Hysteresis Accuracy <sup>(4)</sup>	$V_{IT} = 0.8 \text{ V and } 2.7 \text{ V to } 36 \text{ V}$ $V_{HYS}$ Range = 2% to 13% (1% step)	-1.5		1.5	%
		$V_{IT} = 2.7 \text{ V to } 8 \text{ V}$ $V_{HYS} = 0.5 \text{ V, } 1 \text{ V, } 1.5 \text{ V, } 2 \text{ V, } 2.5 \text{ V}$ $(V_{ITP} - V_{HYS}) \geq 2.4 \text{ V, OV Only}$	-1.5		1.5	%
<b>RESET (Output)</b>						
$I_{lkg(OD)}$	Open-Drain leakage	$V_{RESET} = 5.5 \text{ V}$ $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
		$V_{RESET} = 65 \text{ V}$ $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$V_{OL}$ <sup>(5)</sup>	Low level output voltage	$2.7 \text{ V} \leq V_{DD} \leq 65 \text{ V}$ $I_{RESET} = 5 \text{ mA}$			300	mV
$V_{OH\_DO}$	High level output voltage dropout ( $V_{DD} - V_{OH} = V_{OH\_DO}$ ) (Push-Pull only)	$2.7 \text{ V} \leq V_{DD} \leq 65 \text{ V}$ $I_{RESET} = 500 \mu\text{A}$			100	mV
$V_{OH}$ <sup>(5)</sup>	High level output voltage (Push-Pull only)	$2.7 \text{ V} \leq V_{DD} \leq 65 \text{ V}$ $I_{RESET} = 5 \text{ mA}$	$0.8V_{DD}$			V

## 7.5 Electrical Characteristics (continued)

At  $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$ ,  $CTR/\overline{MR} = CTS = \text{open}$ , output reset pull-up resistor  $R_{PU} = 10 \text{ k}\Omega$ , voltage  $V_{PU} = 5.5 \text{ V}$ , and load  $C_{LOAD} = 10 \text{ pF}$ . The operating free-air temperature range  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 16 \text{ V}$  and  $V_{IT} = 6.5 \text{ V}$  ( $V_{IT}$  refers to  $V_{ITN}$  or  $V_{ITP}$ ).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Capacitor Timing (CTS, CTR)</b>						
$R_{CTR}$	Internal resistance (CTR / $\overline{MR}$ )		877	1000	1147	Kohms
$R_{CTS}$	Internal resistance (CTS)		88	100	122	Kohms
<b>Manual Reset (MR)</b>						
$V_{\overline{MR\_IH}}$	CTR / $\overline{MR}$ pin logic high input	$V_{DD} = 2.7 \text{ V}$	2200			mV
$V_{\overline{MR\_IH}}$	CTR / $\overline{MR}$ pin logic high input	$V_{DD} = 65 \text{ V}$	2500			mV
$V_{\overline{MR\_IL}}$	CTR / $\overline{MR}$ pin logic low input	$V_{DD} = 2.7 \text{ V}$			1300	mV
$V_{\overline{MR\_IL}}$	CTR / $\overline{MR}$ pin logic low input	$V_{DD} = 65 \text{ V}$			1300	mV

- (1) When  $V_{DD}$  voltage falls below UVLO, reset is asserted for Output.  $V_{DD}$  slew rate  $\leq 100 \text{ mV} / \mu\text{s}$
- (2)  $V_{POR}$  is the minimum  $V_{DD}$  voltage for a controlled output state. Below  $V_{POR}$ , the output cannot be determined.  $V_{DD} \text{ dv/dt} \leq 100 \text{ mV}/\mu\text{s}$
- (3) For adjustable voltage guidelines and resistor selection refer to **Adjustable Voltage Thresholds** in **Application and Implementation section**
- (4) Hysteresis is with respect to  $V_{ITP}$  and  $V_{ITN}$  voltage threshold.  $V_{ITP}$  has negative hysteresis and  $V_{ITN}$  has positive hysteresis.
- (5) For  $V_{OH}$  and  $V_{OL}$  relation to output variants refer to **Timing Figures after the Timing Requirement Table**



## 7.6 Timing Requirements

At  $V_{DD(MIN)} \leq V_{DD} \leq V_{DD(MAX)}$ ,  $C_{CTR/MR} = C_{TS} = \text{open}$  <sup>(1)</sup>, output reset pull-up resistor  $R_{PU} = 10 \text{ k}\Omega$ , voltage  $V_{PU} = 5.5\text{V}$ , and  $C_{LOAD} = 10 \text{ pF}$ . VDD and SENSE slew rate =  $1\text{V} / \mu\text{s}$ . The operating free-air temperature range  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , unless otherwise noted. Typical values are at  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 16 \text{ V}$  and  $V_{IT} = 6.5 \text{ V}$  ( $V_{IT}$  refers to either  $V_{ITN}$  or  $V_{ITP}$ ).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Common timing parameters</b>					
$t_{CTR}$	Reset release time delay (CTR/MR) <sup>(2)</sup>	VIT = 2.7 V to 36 V $C_{CTR} = \text{Open}$ 20% Overdrive from Hysteresis		100	$\mu\text{s}$
		VIT = 800 mV $C_{CTR} = \text{Open}$ 20% Overdrive from Hysteresis		40	$\mu\text{s}$
$t_{CTS}$	Sense detect time delay (CTS) <sup>(3)</sup>	VIT = 2.7 V to 36 V $C_{CTS} = \text{Open}$ 20% Overdrive from $V_{IT}$	34	90	$\mu\text{s}$
		VIT = 800 mV $C_{CTS} = \text{Open}$ 20% Overdrive from $V_{IT}$		8	17
$t_{SD}$	Startup Delay <sup>(4)</sup>	$C_{CTR/MR} = \text{Open}$		2	ms

- (1)  $C_{CTR}$  = Reset delay channel  
 $C_{CTS}$  = Sense delay channel
- (2) **CTR Reset detect time delay:**  
Overvoltage active-LOW output is measure from  $V_{ITP-HYS}$  to  $V_{OH}$   
Undervoltage active-LOW output is measure from  $V_{ITN+HYS}$  to  $V_{OH}$   
Overvoltage active-HIGH output is measure from  $V_{ITP-HYS}$  to  $V_{OL}$   
Undervoltage active-HIGH output is measure from  $V_{ITN+HYS}$  to  $V_{OL}$
- (3) **CTS Sense detect time delay:**  
Active-low output is measure from  $V_{IT}$  to  $V_{OL}$  (or  $V_{PULLUP}$ )  
Active-high output is measured from  $V_{IT}$  to  $V_{OH}$   
 $V_{IT}$  refers to either  $V_{ITN}$  or  $V_{ITP}$
- (4) During the power-on sequence, VDD must be at or above  $V_{DD(MIN)}$  for at least  $t_{SD}$  before the output is in the correct state based on  $V_{SENSE}$ .  
 $t_{SD}$  time includes the propagation delay ( $C_{CTR} = \text{Open}$ ). Capacitor on  $C_{CTR}$  will add time to  $t_{SD}$ .

### 7.7 Timing Diagrams

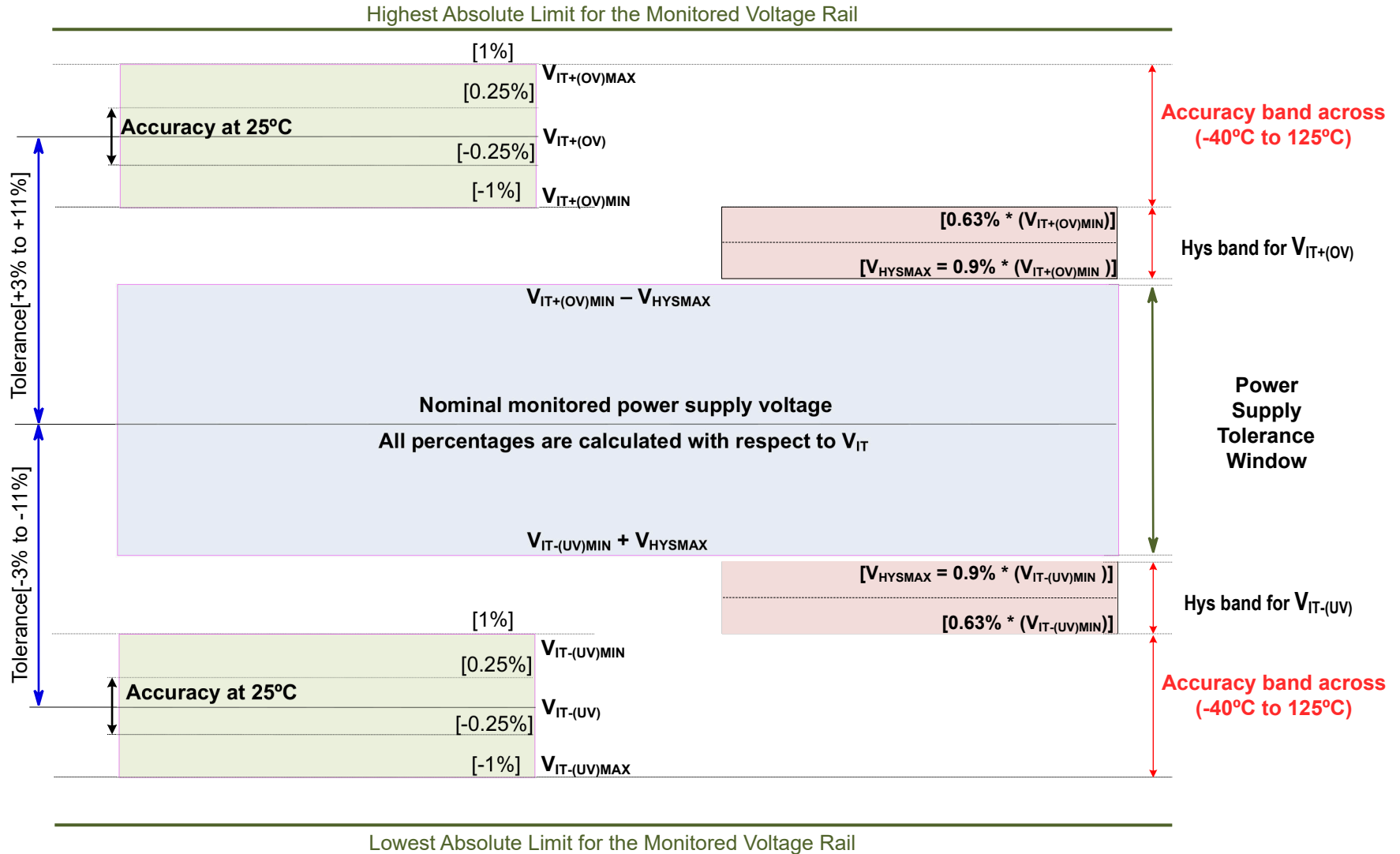
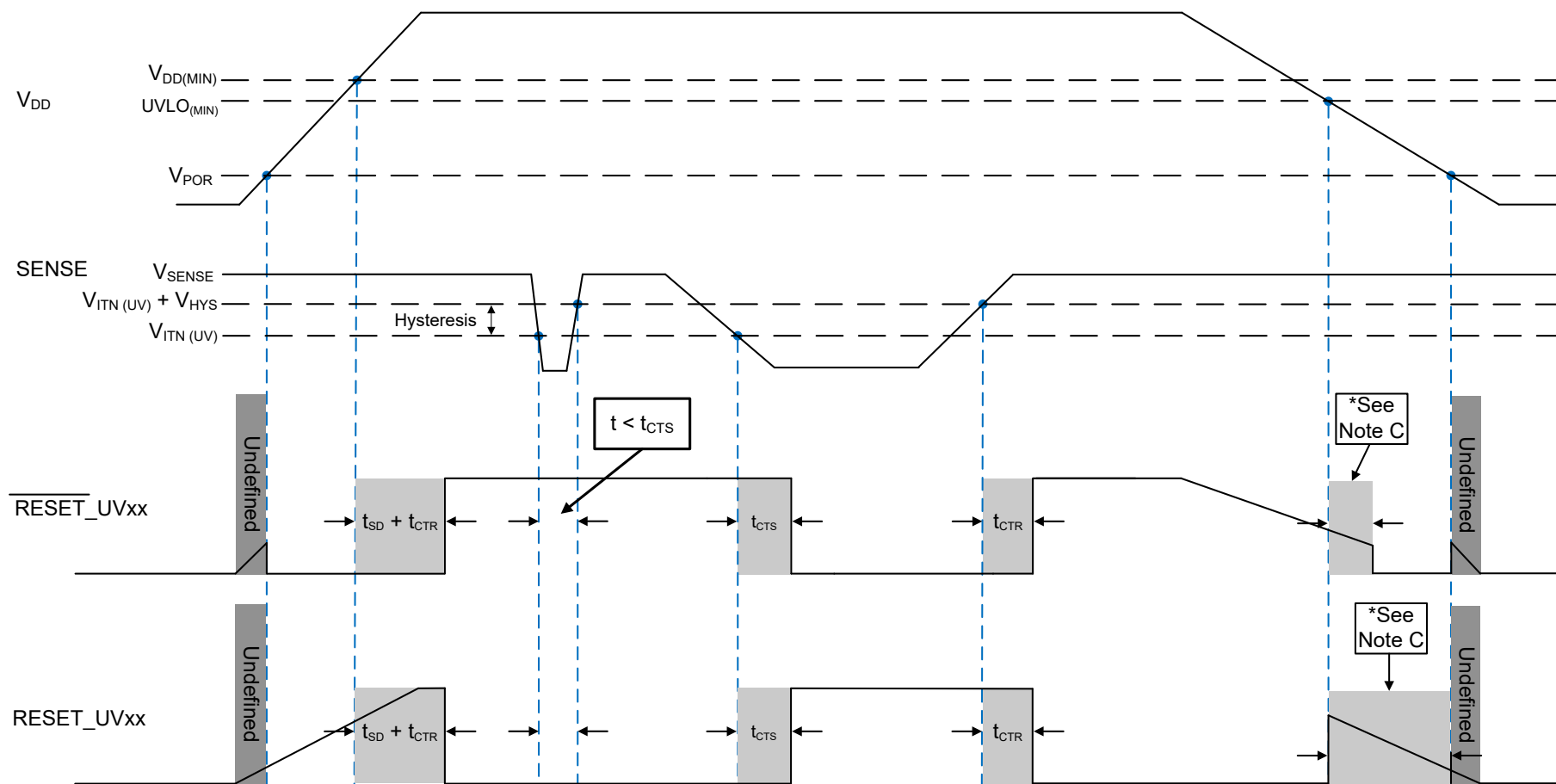
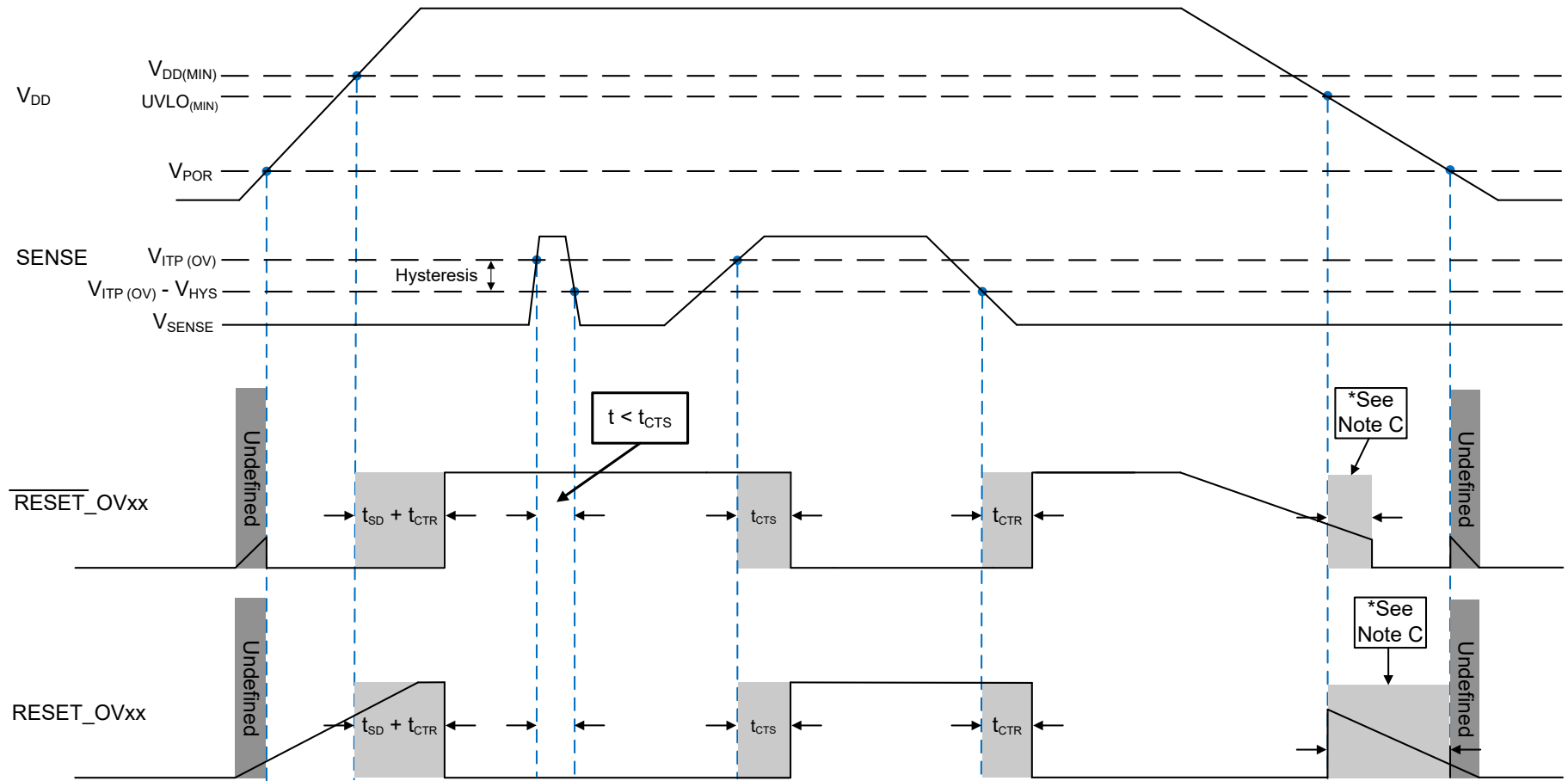


图 7-1. Voltage Threshold and Hysteresis Accuracy



- A. For open-drain output option, the timing diagram assumes the  $\overline{\text{RESET\_UVOD}}$  /  $\overline{\text{RESET\_UVOD}}$  pin is connected via an external pull-up resistor to VDD.
- B. Be advised that [Figure 7-2](#) shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay ( $t_{CTR}$ ) time.
- C.  $\overline{\text{RESET\_UVxx}}$  /  $\overline{\text{RESET\_UVxx}}$  is asserted when VDD goes below the  $\text{UVLO}_{(\text{MIN})}$  threshold after the time delay,  $t_{CTR}$ , is reached.

**图 7-2. SENSE Undervoltage (UV) Timing Diagram**



- A. For open-drain output option, the timing diagram assumes the RESET\_OVOD / RESET\_OVOD pin is connected via an external pull-up resistor to VDD.
- B. Be advised that [图 7-3](#) shows the VDD falling slew rate is slow or the VDD decay time is much larger than the propagation detect delay (t<sub>CTR</sub>) time.
- C. RESET\_OVxx / RESET\_OVxx is asserted when VDD goes below the UVLO<sub>(MIN)</sub> threshold after the time delay, t<sub>CTR</sub>, is reached.

**图 7-3. SENSE Overvoltage (OV) Timing Diagram**

## 7.8 Typical Characteristics

Typical characteristics show the typical performance of the TPS3760-Q1 device. Test conditions are  $T_A = 25^\circ\text{C}$ ,  $R_{PU} = 100\text{ k}\Omega$ ,  $C_{Load} = 50\text{ pF}$ , unless otherwise noted.

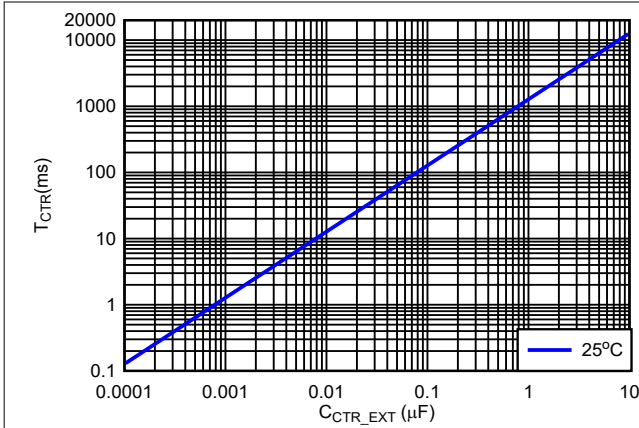


图 7-4.  $T_{CTR}$  vs  $C_{CTR}$

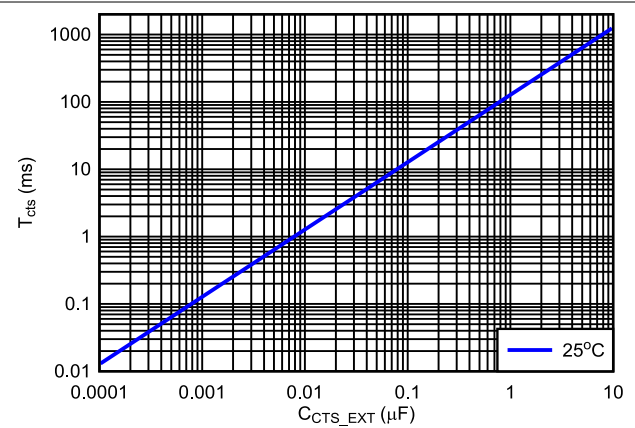


图 7-5.  $T_{CTS}$  vs  $C_{CTS}$

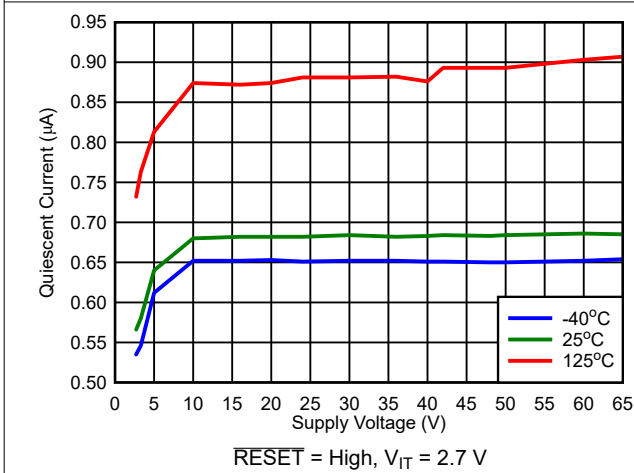


图 7-6.  $V_{DD}$  vs  $I_{DD}$  (RESET = High,  $V_{IT} = 2.7\text{ V}$ )

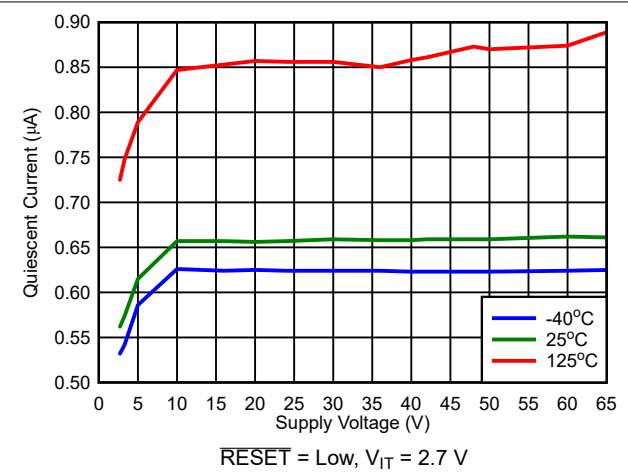


图 7-7.  $V_{DD}$  vs  $I_{DD}$  (RESET = Low,  $V_{IT} = 2.7\text{ V}$ )

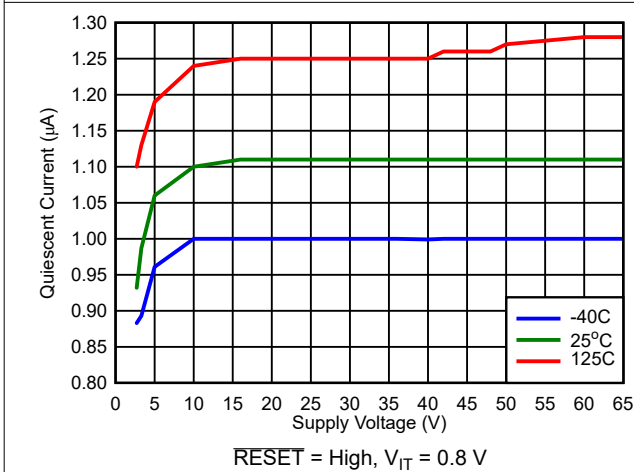


图 7-8.  $V_{DD}$  vs  $I_{DD}$  (RESET = High,  $V_{IT} = 0.8\text{ V}$ )

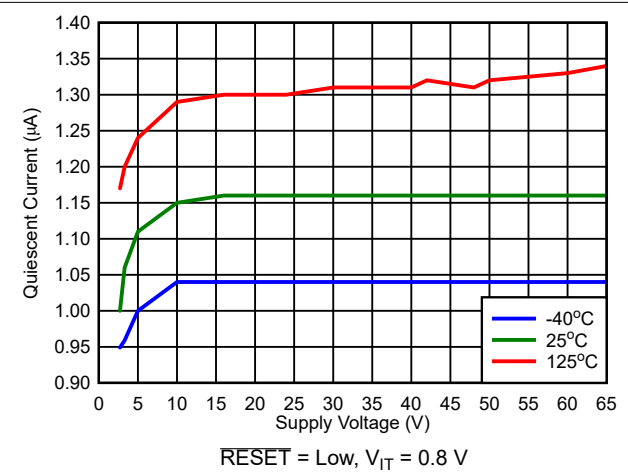


图 7-9.  $V_{DD}$  vs  $I_{DD}$  (RESET = Low,  $V_{IT} = 0.8\text{ V}$ )

### 7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3760-Q1 device. Test conditions are  $T_A = 25^\circ\text{C}$ ,  $R_{PU} = 100\text{ k}\Omega$ ,  $C_{Load} = 50\text{ pF}$ , unless otherwise noted.

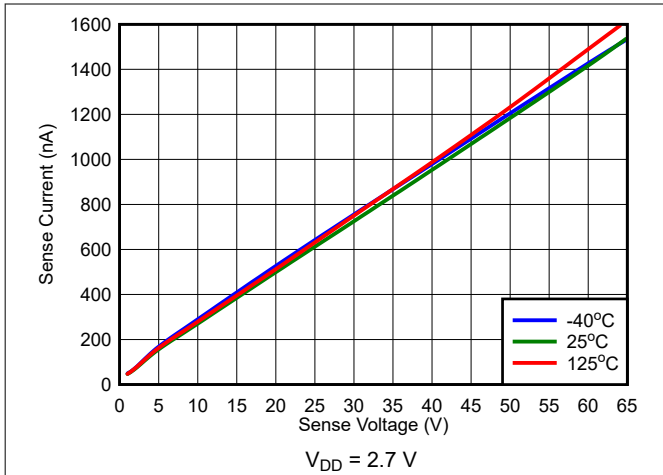


图 7-10.  $V_{SENSE}$  VS  $I_{SENSE}$

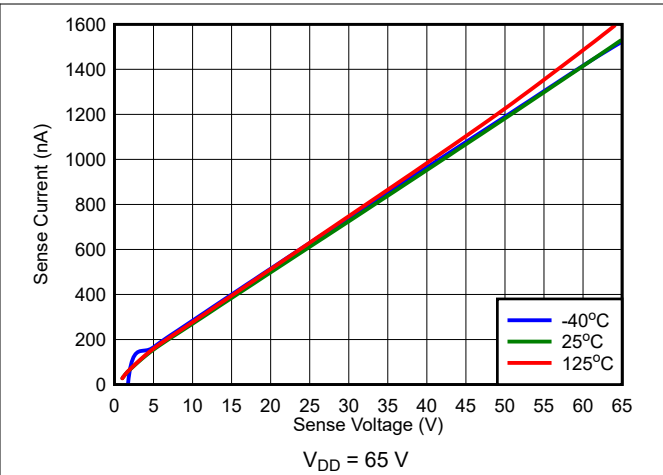


图 7-11.  $V_{SENSE}$  VS  $I_{SENSE}$

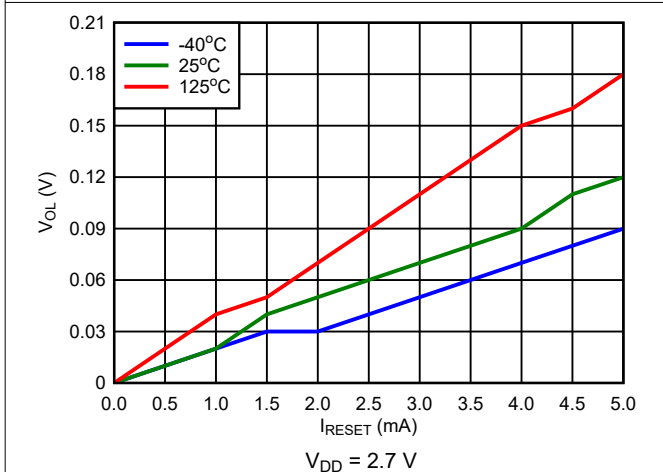


图 7-12. Open-Drain Active Low  $V_{OL}$  VS  $I_{RESET}$

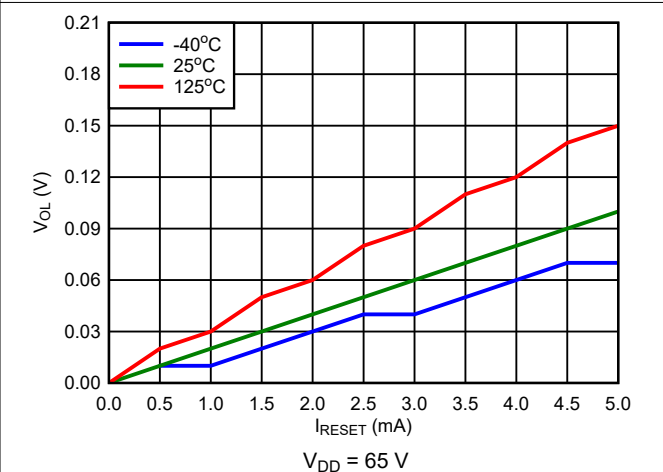


图 7-13. Open-Drain Active Low  $V_{OL}$  VS  $I_{RESET}$

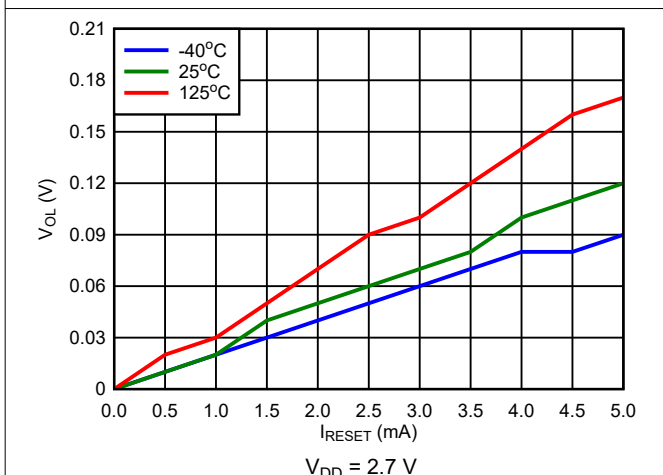


图 7-14. Open-Drain Active High  $V_{OL}$  VS  $I_{RESET}$

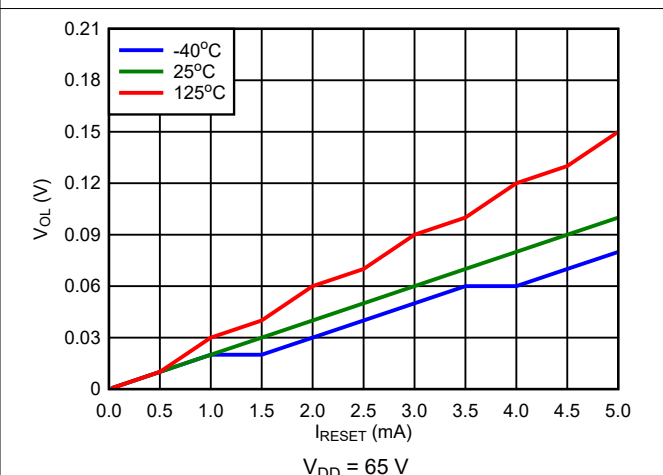


图 7-15. Open-Drain Active High  $V_{OL}$  VS  $I_{RESET}$

### 7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3760-Q1 device. Test conditions are  $T_A = 25^\circ\text{C}$ ,  $R_{PU} = 100\text{ k}\Omega$ ,  $C_{Load} = 50\text{ pF}$ , unless otherwise noted.

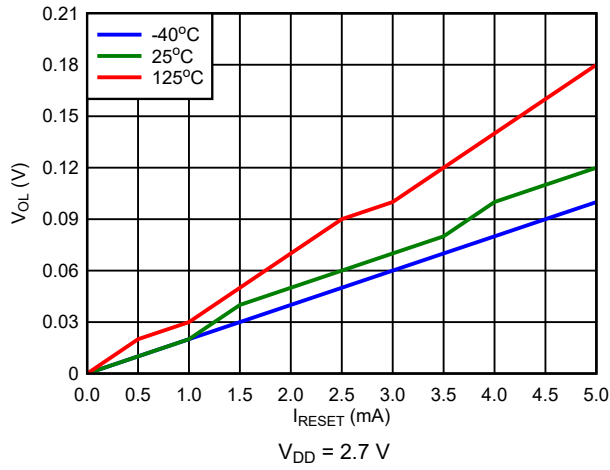


图 7-16. Push-Pull Active High  $V_{OL}$  vs  $I_{RESET}$

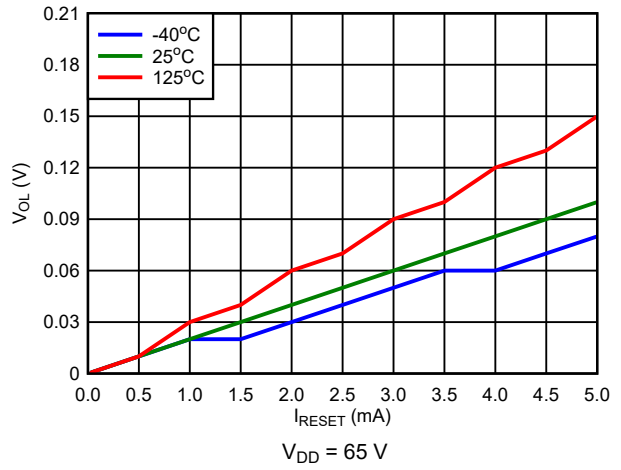


图 7-17. Push-Pull Active High  $V_{OL}$  vs  $I_{RESET}$

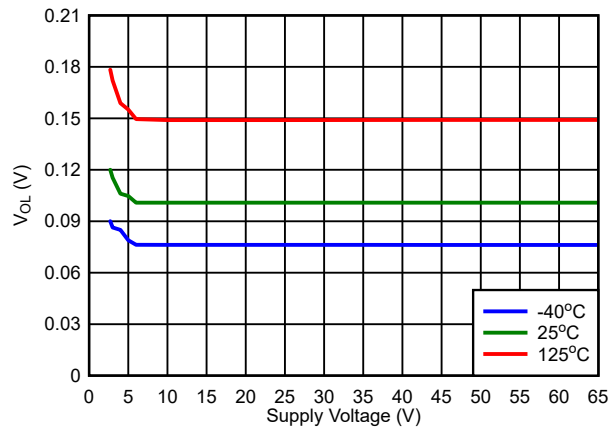


图 7-18. Open-Drain Active Low  $V_{OL}$  vs  $V_{DD}$

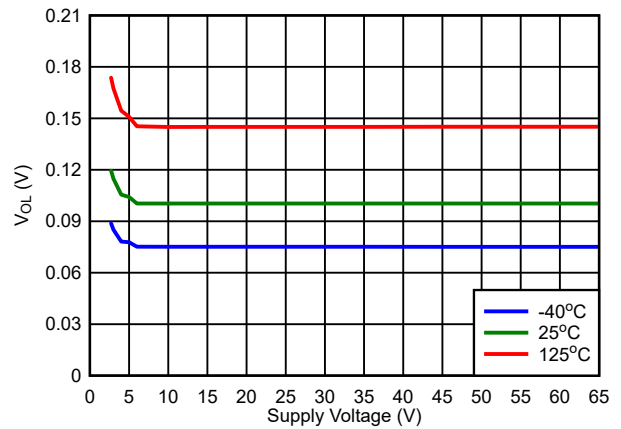


图 7-19. Open-Drain Active High  $V_{OL}$  vs  $V_{DD}$

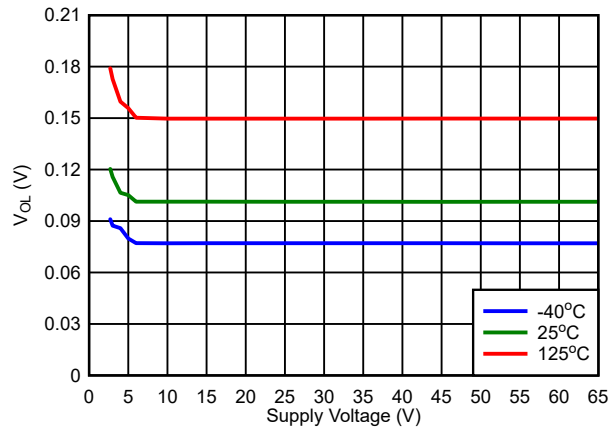


图 7-20. Push-Pull Active Low  $V_{OL}$  vs  $V_{DD}$

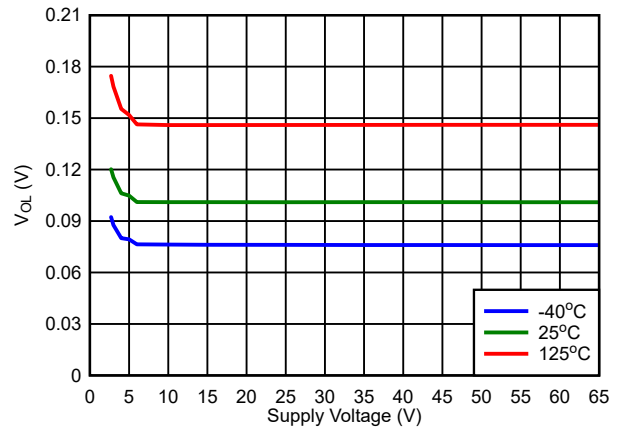
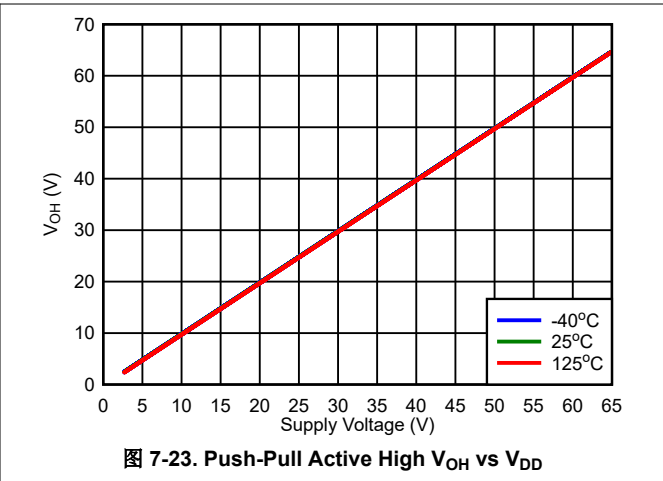
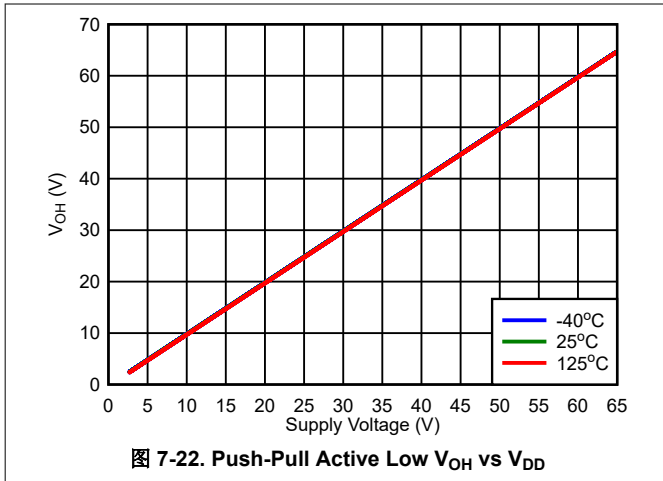


图 7-21. Push-Pull Active High  $V_{OL}$  vs  $V_{DD}$

### 7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3760-Q1 device. Test conditions are  $T_A = 25^\circ\text{C}$ ,  $R_{PU} = 100\text{ k}\Omega$ ,  $C_{Load} = 50\text{ pF}$ , unless otherwise noted.





## 8 Detailed Description

### 8.1 Overview

The TPS3760-Q1 is a family of high voltage and low quiescent current reset ICs with fixed threshold voltage. A voltage divider is integrated to eliminate the need for external resistors and eliminate leakage current that comes with resistor dividers. However, it can also support an external resistor if required by the application. The lowest threshold 800 mV (bypass internal resistor ladder) is recommended for external resistors use case to take advantage of faster detection time and lower  $I_{SENSE}$  current.

VDD, SENSE and RESET pins can support 65 V continuous operation; both VDD and SENSE voltage levels can be independent of each other, meaning VDD pin can be connected at 2.7 V while SENSE pins are connected to a higher voltage. Note, the TPS3760-Q1 does not have clamps within the device so external circuits or devices must be added to limit the voltages to the absolute maximum limit.

Additional features include programmable sense time delay (CTS) and reset delay time and manual reset (CTR /  $\overline{MR}$ ).

### 8.2 Functional Block Diagram

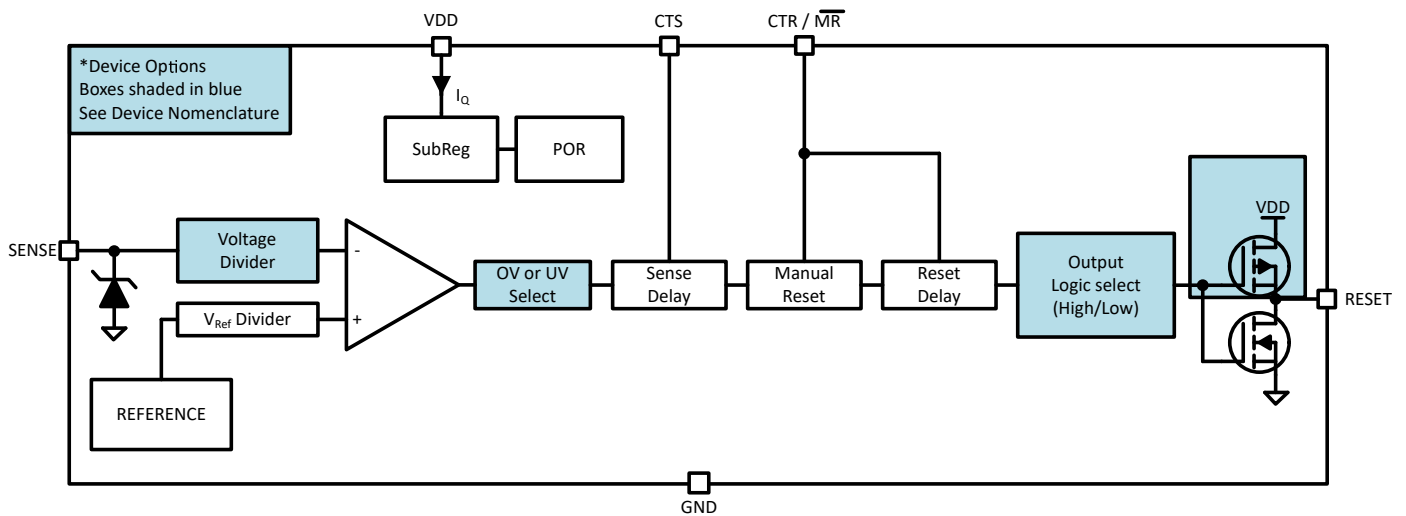


图 8-1. Functional Block Diagram <sup>1</sup>

<sup>1</sup> Refer to 节 5 for complete list of topologies and output logic combination

### 8.3 Feature Description

#### 8.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7 V to 65 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1  $\mu$ F capacitor between the VDD and GND.

VDD needs to be at or above  $V_{DD(MIN)}$  for at least the start-up time delay ( $t_{SD}$ ) for the device to be fully functional.



VDD voltage is independent of  $V_{SENSE}$  and  $V_{RESET}$ , meaning that VDD can be higher or lower than the other pins.

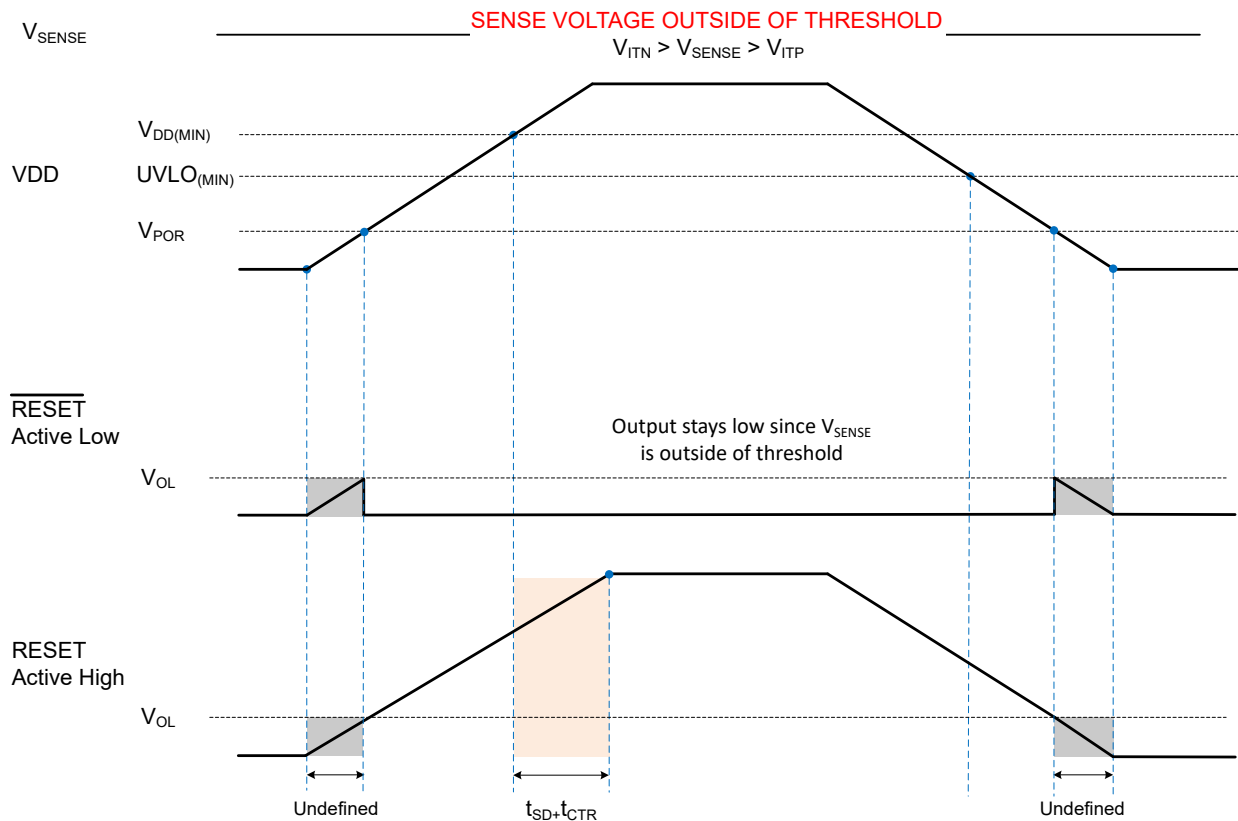
##### 8.3.1.1 Undervoltage Lockout ( $V_{POR} < V_{DD} < UVLO$ )

When the voltage on VDD is less than the UVLO voltage, but greater than the power-on reset voltage ( $V_{POR}$ ), the output pins will be in reset, regardless of the voltage at SENSE pins.

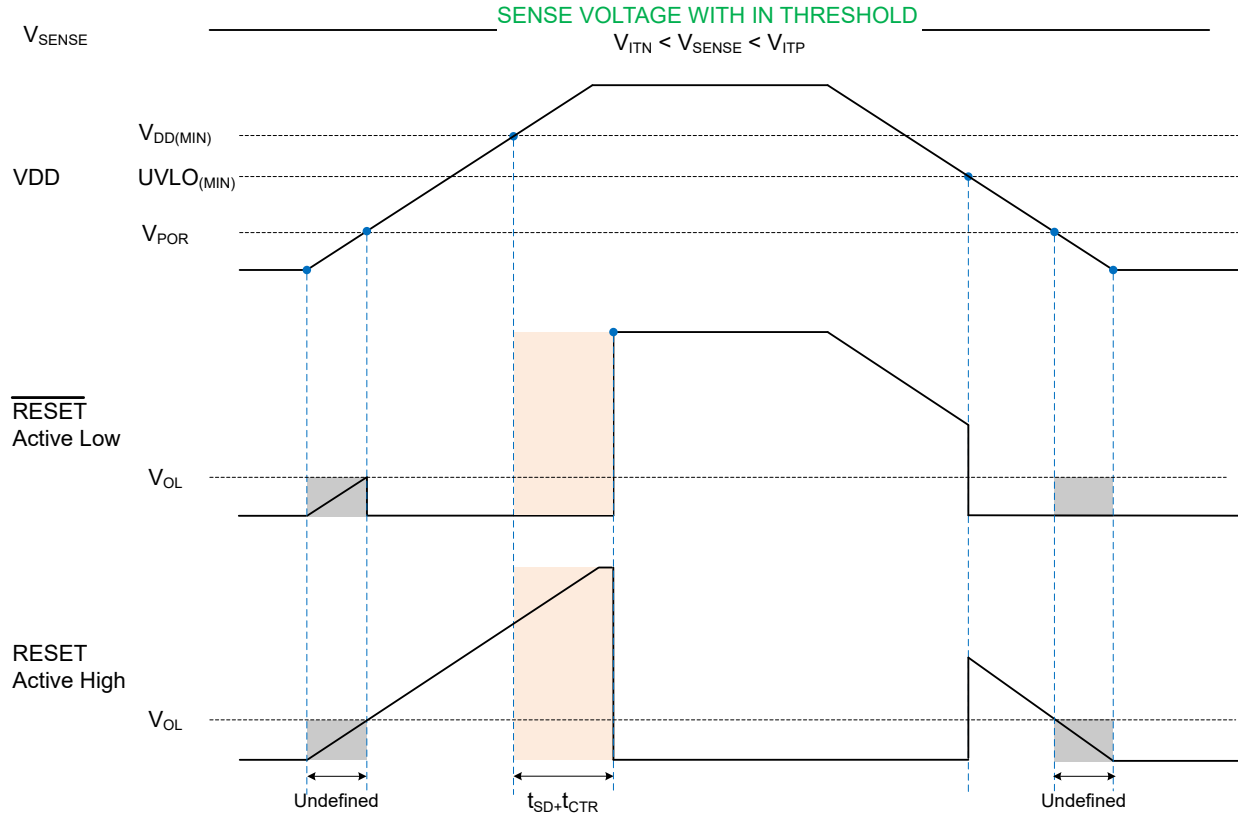
##### 8.3.1.2 Power-On Reset ( $V_{DD} < V_{POR}$ )

When the voltage on VDD is lower than the power on reset voltage ( $V_{POR}$ ), the output signal is undefined and is not to be relied upon for proper device function.

Note:  8-2 and  8-3 assume an external pull-up resistor is connected to the reset pin via VDD.



**图 8-2. Power Cycle (SENSE Outside of Nominal Voltage)**



**图 8-3. Power Cycle (SENSE Within Nominal Voltage)**

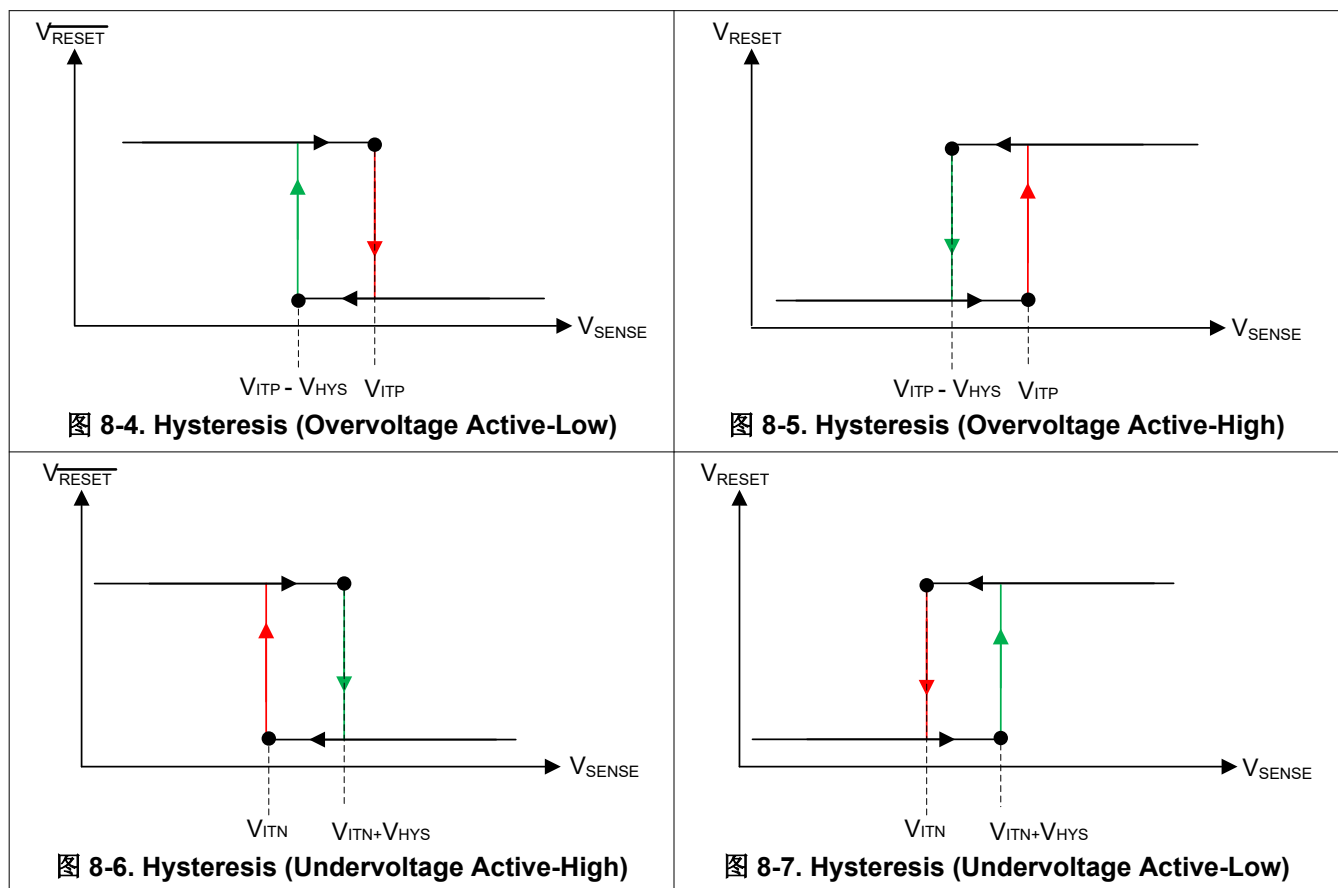
### 8.3.2 SENSE

The TPS3760-Q1 high voltage family integrates a voltage comparator, a precision reference voltage and a trimmed resistor divider. This configuration optimizes device accuracy because all resistor tolerances are accounted for in the accuracy and performance specifications. Device also has built-in hysteresis that provides noise immunity and ensures stable operation.

Although not required in most cases, for noisy applications good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSE inputs in order to reduce sensitivity to transient voltages on the monitored signal. SENSE can be connected directly to VDD pin.

#### 8.3.2.1 SENSE Hysteresis

Built-in hysteresis to avoid erroneous output reset release. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold ( $V_{ITP}$ ), for undervoltage options hysteresis is added to the negative threshold ( $V_{ITN}$ ).



**表 8-1. Common Hysteresis Lookup Table**

TARGET			DEVICE ACTUAL HYSTERESIS OPTION
DETECT THRESHOLD	TOPOLOGY	RELEASE VOLTAGE (V)	
18.0 V	Overvoltage	17.5 V	-3%
18.0 V	Overvoltage	16.0 V	-11%
17.0 V	Overvoltage	16.5 V	-3%
16.0 V	Overvoltage	15.0 V	-6%
15.0 V	Overvoltage	14.0 V	-7%
6.0 V	Undervoltage	6.5 V	0.5 V
5.5 V	Undervoltage	6 V	0.5 V
8 V	Undervoltage	9 V	1 V
5 V	Undervoltage	7.5 V	2.5 V

表 8-1 shows a sample of hysteresis and voltage options for the TPS3760-Q1. For threshold voltages ranging from 2.7 V to 8 V, one option is to select a fixed hysteresis value ranging from 0.5 V to 2.5 V in increments of 0.5 V. Additionally, a second option can be selected where the hysteresis value is a percentage of the threshold voltage. The percentage of voltage hysteresis ranges from 2% to 13%.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is  $(V_{ITN(UV)} + V_{HYS})$  and for the overvoltage (OV) channel is  $(V_{ITP(OV)} - V_{HYS})$ . The accuracy of the release voltage, or stated in the Electrical Characteristics as *Hysteresis Accuracy* is  $\pm 1.5\%$ . Expanding what is shown in 表 8-1, below are a few voltage hysteresis examples that include the hysteresis accuracy:

Undervoltage (UV) Channel

$$V_{ITN} = 0.8 \text{ V}$$

$$\text{Voltage Hysteresis } (V_{HYS}) = 5\% = 40 \text{ mV}$$

$$\text{Hysteresis Accuracy} = \pm 1.5\% = 39.4 \text{ mV or } 40.6 \text{ mV}$$

$$\text{Release Voltage} = V_{ITN} + V_{HYS} = 839.4 \text{ mV to } 840.6 \text{ mV}$$

Overvoltage (OV) Channel

$$V_{ITP} = 8 \text{ V}$$

$$\text{Voltage Hysteresis } (V_{HYS}) = 2 \text{ V}$$

$$\text{Hysteresis Accuracy} = \pm 1.5\% = 1.97 \text{ V or } 2.03 \text{ V}$$

$$\text{Release Voltage} = V_{ITN} - V_{HYS} = 5.97 \text{ V to } 6.03 \text{ V}$$

### 8.3.3 Output Logic Configurations

TPS3760-Q1 is a single channel device that has a single input sense pin and a single reset pin. The single channel is available as Open-Drain and Push-Pull.

The available output logic configuration combinations are shown in [表 8-2](#).

**表 8-2. TPS3760-Q1 Output Logic**

DESCRIPTION	NOMENCLATURE	VALUE
<b>GPN</b>	<b>TPS3760-Q1 (+ topology)</b>	<b>CHANNEL CONFIGURATION</b>
Topology (OV and UV only)	TPS3760A-Q1	UV OD L
• UV = Undervoltage	TPS3760B-Q1	UV PP L
• OV = Overvoltage	TPS3760C-Q1	UV OD H
• PP = Push-Pull	TPS3760D-Q1	UV PP H
• OD = Open-Drain	TPS3760E-Q1	OV OD L
• L = Active low	TPS3760F-Q1	OV PP L
• H = Active high	TPS3760G-Q1	OV OD H
	TPS3760H-Q1	OV PP H

#### 8.3.3.1 Open-Drain

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor consider system  $V_{OH}$  and the ( $I_{IKG}$ ) current provided in the electrical characteristics, high resistors values will have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS3760-Q1 open-drain output pin.

#### 8.3.3.2 Push-Pull

Push-Pull output does not require an external resistor since is the output is internally pulled-up to VDD during  $V_{OH}$  condition and output will be connected to GND during  $V_{OH}$  condition.

#### 8.3.3.3 Active-High (RESET)

RESET (active-high), denoted with no bar above the pin label. RESET remains low ( $V_{OL}$ , deasserted) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary ( $V_{ITN}$ ).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary ( $V_{ITP}$ ).

#### 8.3.3.4 Active-Low (RESET)

$\overline{\text{RESET}}$  (active low) denoted with a bar above the pin label.  $\overline{\text{RESET}}$  remains high voltage ( $V_{OH}$ , deasserted) (open-drain variant  $V_{OH}$  is measured against the pullup voltage) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary ( $V_{ITN}$ ).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary ( $V_{ITP}$ ).

### 8.3.4 User-Programmable Reset Time Delay

TPS3760-Q1 has adjustable reset release time delay with external capacitors.

- A capacitor in CTR /  $\overline{MR}$  programs the reset time delay of the output.
- No capacitor on this pin gives the fastest reset delay time indicated in the [节 7.6](#).

#### 8.3.4.1 Reset Time Delay Configuration

The time delay ( $t_{CTR}$ ) can be programmed by connecting a capacitor between CTR pin and GND.

The relationship between external capacitor  $C_{CTR\_EXT (typ)}$  and the time delay  $t_{CTR (typ)}$  is given by [方程式 1](#).

$$t_{CTR (typ)} = -\ln (0.28) \times R_{CTR (typ)} \times C_{CTR\_EXT (typ)} + t_{CTR (no\ cap)} \quad (1)$$

$R_{CTR (typ)}$  = is in kilo ohms (kOhms)

$C_{CTR\_EXT (typ)}$  = is given in microfarads ( $\mu F$ )

$t_{CTR (typ)}$  = is the reset time delay (ms)

The reset delay varies according to three variables: the external capacitor ( $C_{CTR\_EXT}$ ), CTR pin internal resistance ( $R_{CTR}$ ) provided in [节 7](#), and a constant. The minimum and maximum variance due to the constant is show in [方程式 2](#) and [方程式 3](#):

$$t_{CTR (min)} = -\ln (0.31) \times R_{CTR (min)} \times C_{CTR\_EXT (min)} + t_{CTR (no\ cap (min))} \quad (2)$$

$$t_{CTR (max)} = -\ln (0.25) \times R_{CTR (max)} \times C_{CTR\_EXT (max)} + t_{CTR (no\ cap (max))} \quad (3)$$

The recommended maximum reset delay capacitor for the TPS3760-Q1 is limited to 10  $\mu F$  as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 5% of the programmed reset time delay.

### 8.3.5 User-Programmable Sense Delay

TPS3760-Q1 has adjustable sense release time delay with external capacitors.

- A capacitor in CTS programs the excursion detection on SENSE.
- No capacitor on these pins gives the fastest detection time indicated in the [节 7.6](#).

#### 8.3.5.1 Sense Time Delay Configuration

The time delay ( $t_{CTS}$ ) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor  $C_{CTS\_EXT (typ)}$  and the time delay  $t_{CTS (typ)}$  is given by [方程式 4](#).

$$t_{CTS (typ)} = -\ln(0.28) \times R_{CTS (typ)} \times C_{CTS\_EXT (typ)} + t_{CTS (no\ cap)} \quad (4)$$

$R_{CTS}$  = is in kilo ohms (kOhms)

$C_{CTS\_EXT}$  = is given in microfarads ( $\mu F$ )

$t_{CTS}$  = is the sense time delay (ms)

The sense delay varies according to three variables: the external capacitor ( $C_{CTS\_EXT}$ ), CTS pin internal resistance ( $R_{CTS}$ ) provided in Electrical Characteristics, and a constant. The minimum and maximum variance due to the constant is show in [方程式 5](#) and [方程式 6](#):

$$t_{CTS (min)} = -\ln(0.31) \times R_{CTS (min)} \times C_{CTS\_EXT (min)} + t_{CTS (no\ cap (min))} \quad (5)$$

$$t_{CTS (max)} = -\ln(0.25) \times R_{CTS (max)} \times C_{CTS\_EXT (max)} + t_{CTSx (no\ cap (max))} \quad (6)$$

The recommended maximum sense delay capacitor for the TPS3760-Q1 is limited to 10  $\mu F$  as this ensures enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

When a voltage fault occurs, the previously charged up capacitor discharges and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay will be shorter than expected. The capacitor will begin charging from a voltage above zero and resulting in shorter than expected time delay. A larger delay capacitor can be used so long as the capacitor has enough time between fault events to fully discharge during the duration of the voltage fault. To ensure the capacitor is fully discharged, the time period or time duration between fault events needs to be greater than 10% of the programmed sense time delay.



### 8.3.6 Manual RESET (CTR / $\overline{MR}$ ) Input

The manual reset input allows a processor or other logic circuits to initiate a reset. In this section  $\overline{MR}$  is a generic reference to (CTR /  $\overline{MR}$ ). A logic low on  $\overline{MR}$  causes  $\overline{RESET}$  to assert on reset output. After  $\overline{MR}$  is left floating,  $\overline{RESET}$  will release the reset if the voltage at SENSE pin is at nominal voltage.  $\overline{MR}$  should not be driven high, this pin should be left floating or connected to a capacitor to GND, this pin can be left unconnected if is not used.

If the logic driving the  $\overline{MR}$  cannot tri-state (floating and GND) then a logic-level FET should be used as illustrated in 图 8-8.

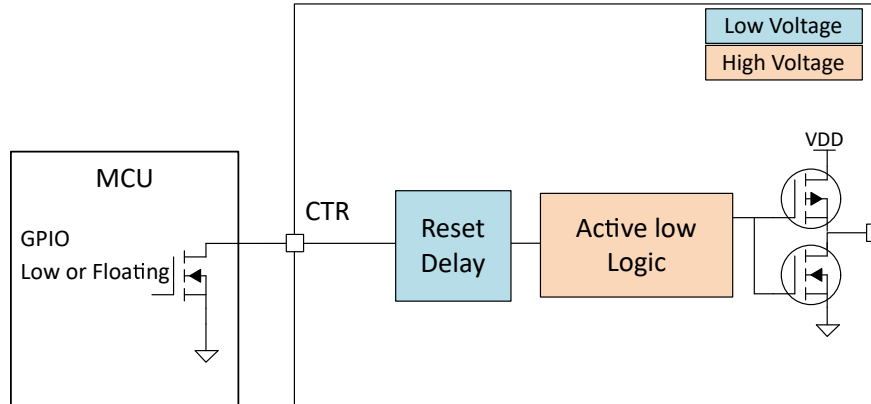


图 8-8. Manual Reset Implementation

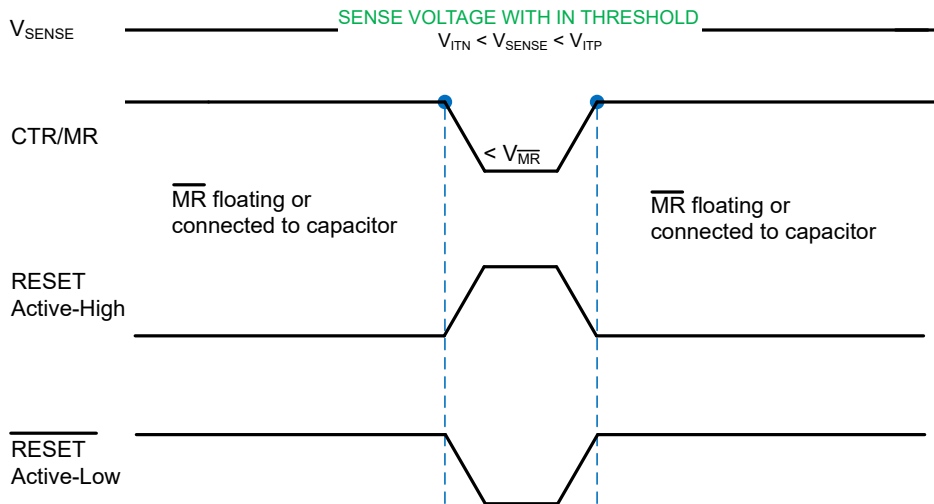


图 8-9. Manual Reset Timing Diagram

表 8-3.  $\overline{MR}$  Functional Table

MR	SENSE ON NOMINAL VOLTAGE	RESET STATUS
Low	Yes	Reset asserted
Floating	Yes	Fast reset release when SENSE voltage goes back to nominal voltage
Capacitor	Yes	Programmable reset time delay
High	Yes	NOT Recommended

### 8.3.7 RESET Latch Mode

The TPS3760 features a output latch mode on the RESET/RESET pin when connecting the LATCH pin to common ground. A pull-down resistor, 10 kΩ, is recommended to limit current consumption of the system. In latch mode, if the RESET/RESET pin is low or triggers low and less than 1.4V is applied to the LATCH pin, the RESET/RESET pin stays asserted regardless if VSENSE goes within the acceptable voltage boundaries ( $V_{SENSE} > V_{ITP} + V_{hyst}$  for UV or  $V_{SENSE} < V_{ITN} - V_{hyst}$  for OV). To unlatch the device a voltage greater than 2.1 V for greater than 3 μs is applied to the LATCH pin. This is recommended to maintain a proper unlatch. The RESET/RESET pin triggers high after the duration of  $t_{ctr}$ . TI recommends using a series resistance to limit current when an unlatch voltage is applied.

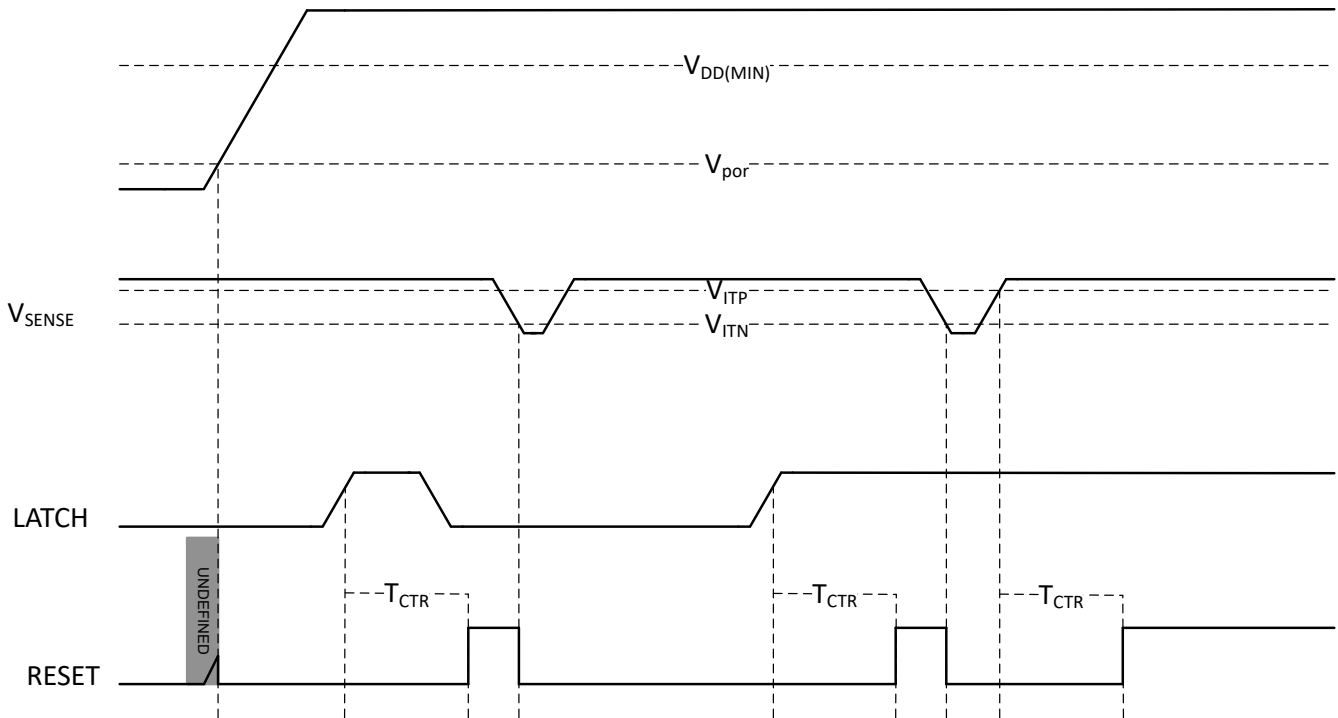


图 8-10. Latch Timing Diagram

## 8.4 Device Functional Modes

**表 8-4. Undervoltage Detect Functional Mode Truth Table**

DESCRIPTION	SENSE		CTR <sup>(1)</sup> / MR PIN	VDD PIN	OUTPUT <sup>(2)</sup> (RESET PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	$SENSE > V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Undervoltage Detection	$SENSE > V_{ITN(UV)}$	$SENSE < V_{ITN(UV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Undervoltage Detection	$SENSE < V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Normal Operation	$SENSE < V_{ITN(UV)}$	$SENSE > V_{ITN(UV)} + HYS$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Manual Reset	$SENSE > V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Low	$V_{DD} > V_{DD(MIN)}$	Low
UVLO Engaged	$SENSE > V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Open or capacitor connected	$V_{POR} < V_{DD} < V_{DD(MIN)}$	Low
Below $V_{POR}$ , Undefined Output	$SENSE > V_{ITN(UV)}$	$SENSE > V_{ITN(UV)}$	Open or capacitor connected	$V_{DD} < V_{POR}$	Undefined

(1) Reset time delay is ignored in the truth table.

(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

**表 8-5. Overvoltage Detect Functional Mode Truth Table**

DESCRIPTION	SENSE		CTR <sup>(1)</sup> / MR PIN	VDD PIN	OUTPUT <sup>(2)</sup> (RESET PIN)
	PREVIOUS CONDITION	CURRENT CONDITION			
Normal Operation	$SENSE < V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Overvoltage Detection	$SENSE < V_{ITN(OV)}$	$SENSE > V_{ITN(OV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Overvoltage Detection	$SENSE > V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	Low
Normal Operation	$SENSE > V_{ITN(OV)}$	$SENSE < V_{ITN(OV)} - HYS$	Open or capacitor connected	$V_{DD} > V_{DD(MIN)}$	High
Manual Reset	$SENSE < V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Low	$V_{DD} > V_{DD(MIN)}$	Low
UVLO Engaged	$SENSE < V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Open or capacitor connected	$V_{POR} < V_{DD} < UVLO$	Low
Below $V_{POR}$ , Undefined Output	$SENSE < V_{ITN(OV)}$	$SENSE < V_{ITN(OV)}$	Open or capacitor connected	$V_{DD} < V_{POR}$	Undefined

(1) Reset time delay is ignored in the truth table.

(2) Open-drain active low output requires an external pull-up resistor to a pull-up voltage.

## 9 Application and Implementation

### 备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The following sections describe in detail how to properly use this device. As this device has many applications and setups, there are many situations that this datasheet can not characterize in detail and will vary from these applications depending on the requirements of the final application

### 9.2 Adjustable Voltage Thresholds

方程式 7 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8 V voltage threshold device when using an adjustable voltage variant. This variant bypasses the internal resistor ladder.

For example, consider a 12 V rail being monitored  $V_{MON}$  for undervoltage (UV) using of the TPS3760A012DYRQ1 variant. Using 方程式 7 and shown in 方程式 8,  $R_1$  is the top resistor of the resistor divider that is between  $V_{MON}$  and  $V_{SENSE}$ ,  $R_2$  is the bottom resistor that is between  $V_{SENSE}$  and GND,  $V_{MON}$  is the voltage rail that is being monitored and  $V_{SENSE}$  is the input threshold voltage. The monitored UV threshold, denoted as  $V_{MON-}$ , where the device will assert a reset signal occurs when  $V_{SENSE} = V_{IT-(UV)}$  or, for this example,  $V_{MON-} = 10.8V$  which is 90% from 12 V. Using 方程式 7 and assuming  $R_2 = 10k\Omega$ ,  $R_1$  can be calculated shown in 方程式 8 where  $I_{R1}$  is represented in 方程式 9:

$$V_{SENSE} = V_{MON-} \times (R_2 \div (R_1 + R_2)) \quad (7)$$

$$R_1 = (V_{MON-} - V_{SENSE}) \div I_{R1} \quad (8)$$

$$I_{R1} = I_{R2} = V_{SENSE} \div R_2 \quad (9)$$

Substituting 方程式 9 into 方程式 8 and solving for  $R_1$  in 方程式 7,  $R_1 = 125k\Omega$ . The TPS3760A012DYRQ1 is typically meant to monitor a 0.8 V rail with  $\pm 2\%$  voltage threshold hysteresis. For the reset signal to become deasserted,  $V_{MON}$  would need to go above  $V_{IT-} + V_{HYS}$ . For this example,  $V_{MON} = 11.016 V$  when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that may affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance  $R_{SENSE}$  can be calculated by the SENSE voltage  $V_{SENSE}$  divided by the SENSE current  $I_{SENSE}$  as shown in 方程式 11.  $V_{SENSE}$  can be calculated using 方程式 7 depending on the resistor divider and monitored voltage.  $I_{SENSE}$  can be calculated using 方程式 10.

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \quad (10)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (11)$$

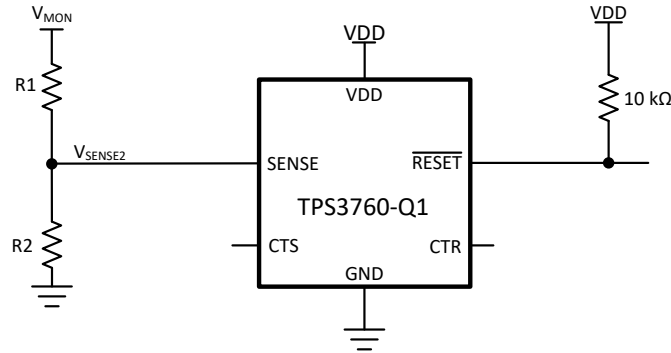


图 9-1. Adjustable Voltage Threshold with External Resistor Dividers

## 9.3 Typical Application

### 9.3.1 Design 1: Off-Battery Monitoring

This application is intended for the initial power stage in applications with the 12 V batteries. Variation of the battery voltage is common between 9 V and 16 V. Furthermore, if cold-cranking and load dump conditions are considered, voltage transients can occur as low as 3 V and as high as 42 V. In this design example, we are highlighting the ability for low power, direct off-battery voltage supervision.

图 9-5 illustrates an example of how the TPS3760 Q1 is monitoring the battery voltage while being powered by it, as well.

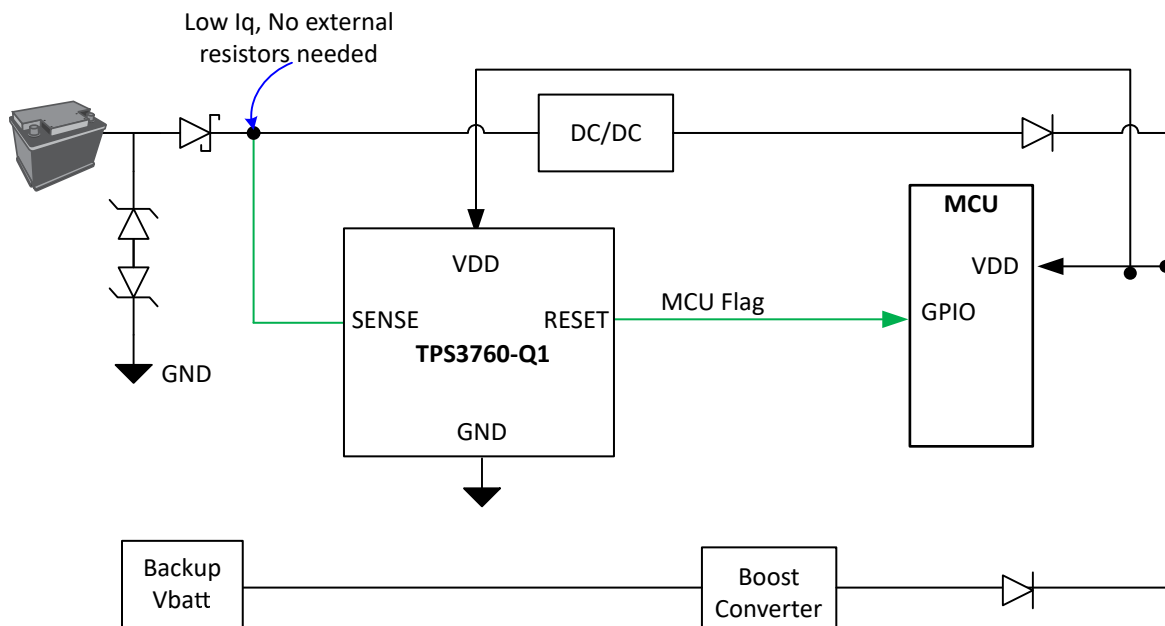


图 9-2. TPS3760-Q1 Overvoltage Supervisor with Direct Off-Battery Monitoring

### 9.3.1.1 Design Requirements

This design requires voltage supervision on a 12 V power supply voltage rail with possibility of the 12 V rail rising up as high as 42 V. The undervoltage fault occurs when the power supply voltage drops below 7.7 V.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Power Rail Voltage Supervision	Monitor 12-V power supply for undervoltage condition, trigger a undervoltage fault at 7.7 V.	TPS3760-Q1 provides voltage monitoring with 1.5% max accuracy with adjustable/non-adjustable variations.
Maximum Input Power	Operate with power supply input up to 42 V.	The TPS3760-Q1 can support a VDD of up to 65 V.
Output logic voltage	Open-Drain Output Topology	An open-drain output is recommended to provide the correct reset signal, but a push-pull can also be used.
Maximum system current consumption	2 $\mu$ A max when power supply is at 12 V typical	TPS3760-Q1 allows for $I_Q$ to remain low with support of up to 65 V. This allows for no external resistor divider to be required.
Voltage Monitor Accuracy	Maximum voltage monitor accuracy of 1.5%.	The TPS3760-Q1 has 1.5% maximum voltage monitor accuracy.
Delay when returning from fault condition	RESET delay of at least 12.8 ms when returning from a undervoltage fault.	$C_{CTR} = 10$ nF sets 12.8 ms delay

### 9.3.1.2 Detailed Design Procedure

The primary advantage of this application is being able to directly monitor a voltage on an automotive battery without needing external an resistor dividers on the SENSE input. This keeps the overall  $I_Q$  of the design low while still achieving the desired rail monitoring.

Voltage rail monitoring is done by connecting the SENSE input directly to the battery rail after the TVS protection diodes. The TPS3760-Q1 that is being used in this example is a fixed voltage variant where the SENSE threshold voltage has been set internally. Word of caution, the TVS protection diodes must be chosen such that the transient voltages on the monitored rails do not exceed the absolute max limit listed in [节 7.1](#).

To use this configuration, the specific voltage threshold variation of the device must be chosen according to the application. In this configuration, the '77' variation must be chosen for 7.7 V as shown in [节 5](#).

The device being able to handle 65 V on VDD means the monitored voltage rail can go as high as 42 V for the application transients and not violate the recommended maximum for the supervisor as it usually would. This is useful when monitoring a voltage rail that has a wide range that may go much higher than the nominal rail voltage such as in this case. Good design practice recommends using a 0.1  $\mu$ F capacitor on the VDD pin and this capacitance may need to increase if using an adjustable version with a resistor divider.

### 9.3.1.3 Application Curves

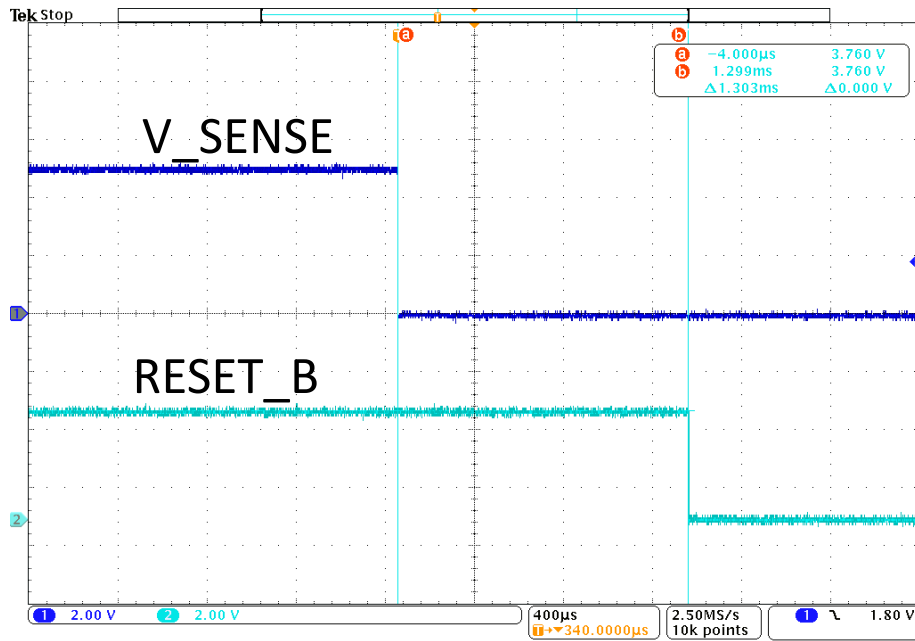


图 9-3. Undervoltage Reset Waveform

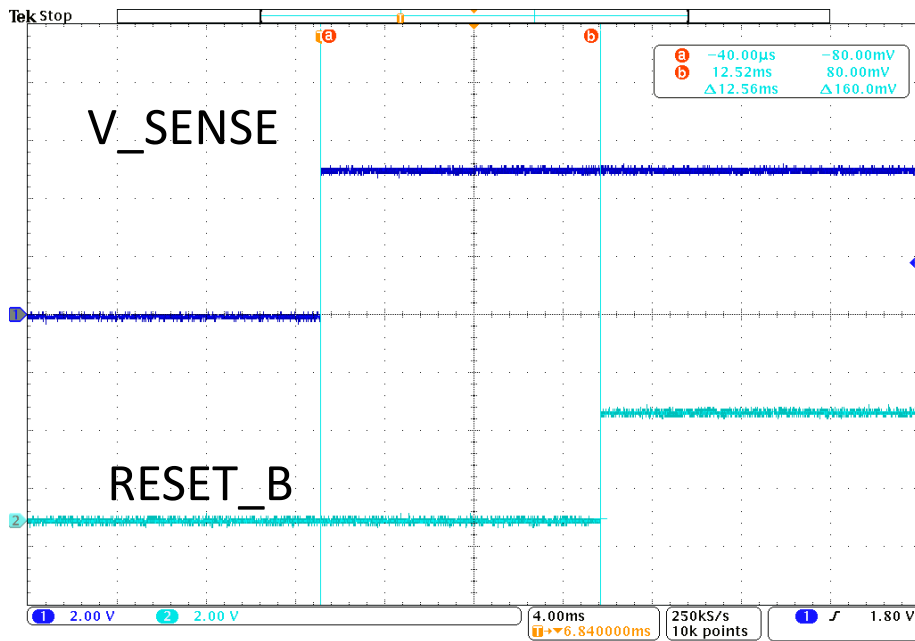


图 9-4. Undervoltage Recovery Waveform

## 9.4 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.4 V ( $V_{POR}$ ) to 65 V (maximum operation). Good analog design practice recommends placing a minimum 0.1  $\mu$ F ceramic capacitor as near as possible to the VDD pin.

### 9.4.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using [方程式 12](#):

$$P_{D-MAX} = ((T_{J-MAX} - T_A) / R_{\theta JA}) \quad (12)$$

The actual power being dissipated in the device can be represented by [方程式 13](#):

$$P_D = V_{DD} \times I_{DD} + P_{RESET} \quad (13)$$

$P_{RESET}$  is calculated by [方程式 14](#) or [方程式 15](#)

$$P_{RESET} (PUSH/PULL) = V_{DD} - V_{RESET} \times I_{RESET} \quad (14)$$

$$P_{RESET} (OPEN-DRAIN) = V_{RESET} \times I_{RESET} \quad (15)$$

[方程式 12](#) and [方程式 13](#) establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations should be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation ( $P_D$ ) and/or excellent package thermal resistance ( $R_{\theta JA}$ ) is present, the maximum ambient temperature ( $T_{A-MAX}$ ) may be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ( $T_{A-MAX}$ ) may have to be de-rated.  $T_{A-MAX}$  is dependent on the maximum operating junction temperature ( $T_{J-MAX-OP} = 125^\circ\text{C}$ ), the maximum allowable power dissipation in the device package in the application ( $P_{D-MAX}$ ), and the junction-to ambient thermal resistance of the part/package in the application ( $R_{\theta JA}$ ), as given by [方程式 16](#):

$$T_{A-MAX} = (T_{J-MAX-OP} - (R_{\theta JA} \times P_{D-MAX})) \quad (16)$$

## 9.5 Layout

### 9.5.1 Layout Guidelines

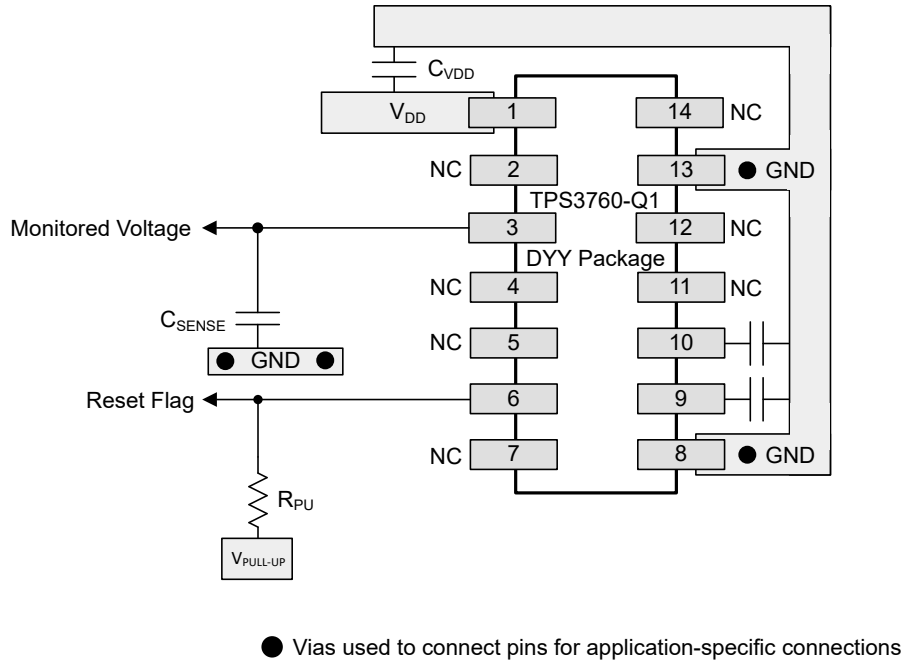
- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1  $\mu$ F ceramic capacitor as near as possible to the VDD pin.
- To further improve the noise immunity on the SENSE pins, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5 pF.
- For open-drain variants, place the pull-up resistors on  $\overline{RESET}$  as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces should be greater than 20 mils (0.5 mm).



- Do not have high voltage metal pads or traces closer than 20 mils (0.5 mm) to the low voltage metal pads or traces.

### 9.5.2 Layout Example

The layout example in [Figure 9-5](#) shows how the TPS3760-Q1 is laid out on a printed circuit board (PCB) with user-defined delays.



**Figure 9-5. TPS3760-Q1 Recommended Layout**

### 9.5.3 Creepage Distance

Per IEC 60664 Creepage is the shortest distance between two conductive parts or as shown in 图 9-6 the distance between high voltage conductive parts and grounded parts, the floating conductive part is ignored and subtracted from the total distance.

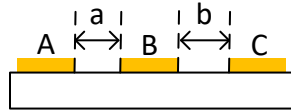


图 9-6. Creepage Distance

图 9-6 details

- A = Left pins (high voltage)
- B = Central pad (conductive not internally connected, can be left floating or connected to GND)
- C = Right pins (low voltages)
- Creepage distance =  $a + b$

## 10 Device and Documentation Support

### 10.1 Device Nomenclature

节 5 shows how to decode the function of the device based on its part number

表 10-1 shows TPS3760-Q1 possible voltage options per channel. Contact TI sales representatives or on TI's E2E forum for details and availability of other options; minimum order quantities apply.

表 10-1. Voltage Options

100 mV STEPS				400 mV STEPS		500 mV STEPS		1 V STEPS	
NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS
<b>01</b>	800 mV (divider bypass)	<b>70</b>	7.0 V	<b>A0</b>	10.4 V	<b>D0</b>	20.5 V	<b>F0</b>	31.0 V
<b>27</b>	2.7 V	<b>71</b>	7.1 V	<b>A1</b>	10.8 V	<b>D1</b>	21.0 V	<b>F1</b>	32.0 V
<b>28</b>	2.8 V	<b>72</b>	7.2 V	<b>A2</b>	11.2 V	<b>D2</b>	21.5 V	<b>F2</b>	33.0 V
<b>29</b>	2.9 V	<b>73</b>	7.3 V	<b>A3</b>	11.6 V	<b>D3</b>	22.0 V	<b>F3</b>	34.0 V
<b>30</b>	3.0 V	<b>74</b>	7.4 V	<b>A4</b>	12.0 V	<b>D4</b>	22.5 V	<b>F4</b>	35.0 V
<b>31</b>	3.1 V	<b>75</b>	7.5 V	<b>A5</b>	12.4 V	<b>D5</b>	23.0 V	<b>F5</b>	36.0 V
<b>32</b>	3.2 V	<b>76</b>	7.6 V	<b>A6</b>	12.8 V	<b>D6</b>	23.5 V		
<b>33</b>	3.3 V	<b>77</b>	7.7 V	<b>A7</b>	13.2 V	<b>D7</b>	24.0 V		
<b>34</b>	3.4 V	<b>78</b>	7.8 V	<b>A8</b>	13.6 V	<b>D8</b>	24.5 V		
<b>35</b>	3.5 V	<b>79</b>	7.9 V	<b>A9</b>	14.0 V	<b>D9</b>	25.0 V		
<b>36</b>	3.6 V	<b>80</b>	8.0 V	<b>B0</b>	14.4 V	<b>E0</b>	25.5 V		
<b>37</b>	3.7 V	<b>81</b>	8.1 V	<b>B1</b>	14.8 V	<b>E1</b>	26.0 V		
<b>38</b>	3.8 V	<b>82</b>	8.2 V	<b>B2</b>	15.2 V	<b>E2</b>	26.5 V		
<b>39</b>	3.9 V	<b>83</b>	8.3 V	<b>B3</b>	15.6 V	<b>E3</b>	27.0 V		
<b>40</b>	4.0 V	<b>84</b>	8.4 V	<b>B4</b>	16.0 V	<b>E4</b>	27.5 V		
<b>41</b>	4.1 V	<b>85</b>	8.5 V	<b>B5</b>	16.4 V	<b>E5</b>	28.0 V		
<b>42</b>	4.2 V	<b>86</b>	8.6 V	<b>B6</b>	16.8 V	<b>E6</b>	28.5 V		
<b>43</b>	4.3 V	<b>87</b>	8.7 V	<b>B7</b>	17.2 V	<b>E7</b>	29.0 V		
<b>44</b>	4.4 V	<b>88</b>	8.8 V	<b>B8</b>	17.6 V	<b>E8</b>	29.5 V		
<b>45</b>	4.5 V	<b>89</b>	8.9 V	<b>B9</b>	18.0 V	<b>E9</b>	30.0 V		
<b>46</b>	4.6 V	<b>90</b>	9.0 V	<b>C0</b>	18.4 V				
<b>47</b>	4.7 V	<b>91</b>	9.1 V	<b>C1</b>	18.8 V				
<b>48</b>	4.8 V	<b>92</b>	9.2 V	<b>C2</b>	19.2 V				
<b>49</b>	4.9 V	<b>93</b>	9.3 V	<b>C3</b>	19.6 V				
<b>50</b>	5.0 V	<b>94</b>	9.4 V	<b>C4</b>	20.0 V				
<b>51</b>	5.1 V	<b>95</b>	9.5 V						
<b>52</b>	5.2 V	<b>96</b>	9.6 V						
<b>53</b>	5.3 V	<b>97</b>	9.7 V						
<b>54</b>	5.4 V	<b>98</b>	9.8 V						
<b>55</b>	5.5 V	<b>99</b>	9.9 V						
<b>56</b>	5.6 V	<b>00</b>	10.0 V						
<b>57</b>	5.7 V								
<b>58</b>	5.8 V								
<b>59</b>	5.9 V								
<b>60</b>	6.0 V								

表 10-1. Voltage Options (continued)

100 mV STEPS				400 mV STEPS		500 mV STEPS		1 V STEPS	
NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS	NOMEN- CLATURE	VOLTAGE OPTIONS
61	6.1 V								
62	6.2 V								
63	6.3 V								
64	6.4 V								
65	6.5 V								
66	6.6 V								
67	6.7 V								
68	6.8 V								
69	6.9 V								

## 10.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 10.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

## 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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## 10.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 10.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3760A012DYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A012Q	<a href="#">Samples</a>
TPS3760AE95DYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AE95Q	<a href="#">Samples</a>
TPS3760E012DYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	E012Q	<a href="#">Samples</a>
TPS3760E335DYRQ1	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	E335Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPS3760-Q1 :**

- Catalog : [TPS3760](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3760A012DYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TPS3760AE95DYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TPS3760E012DYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TPS3760E335DYRQ1	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

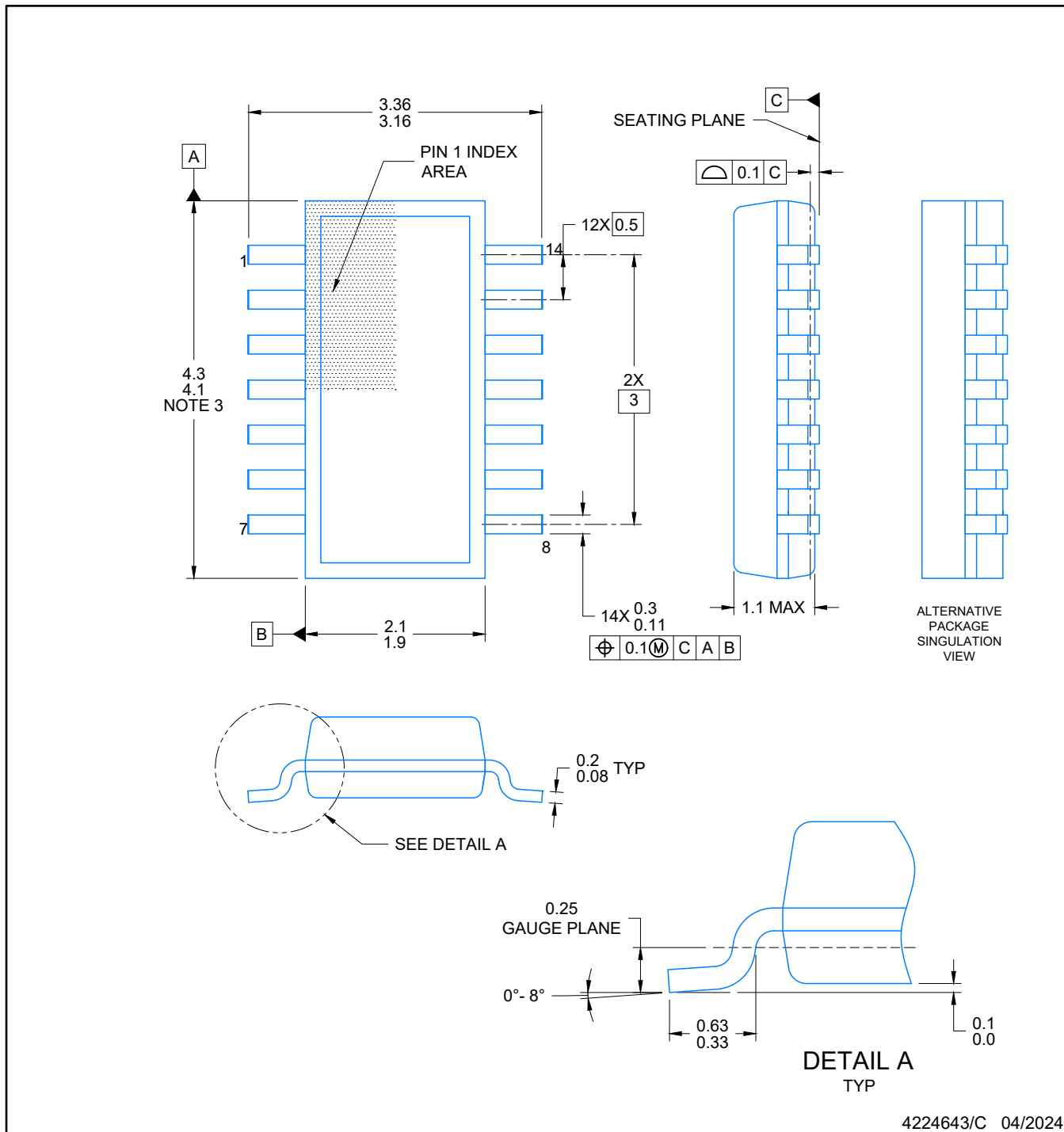
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3760A012DYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TPS3760AE95DYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TPS3760E012DYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TPS3760E335DYRQ1	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8

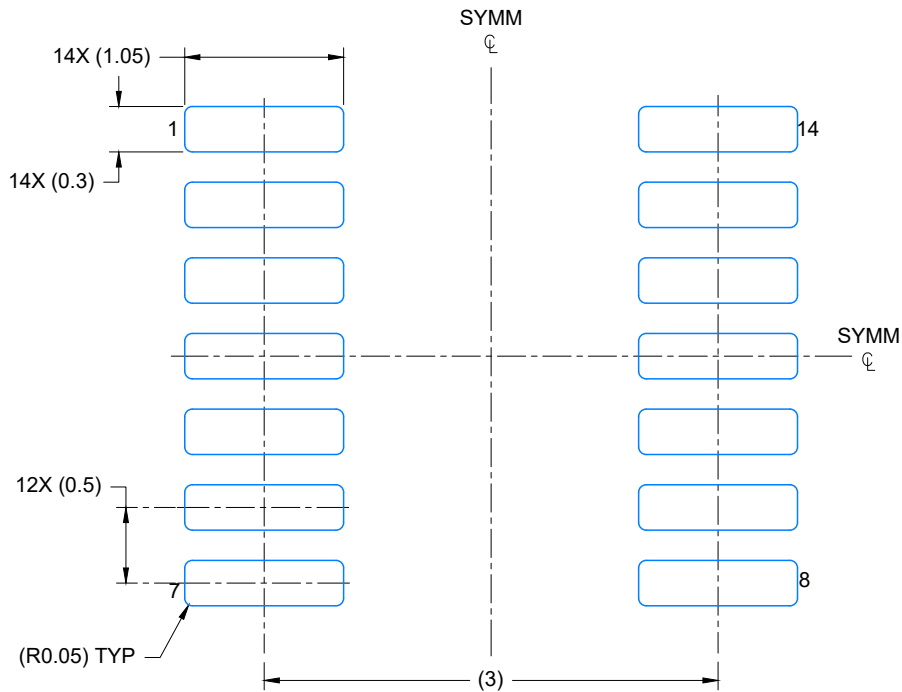




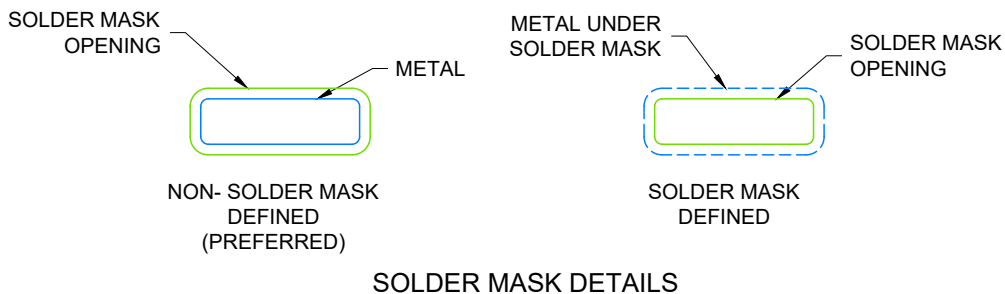
4224643/C 04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



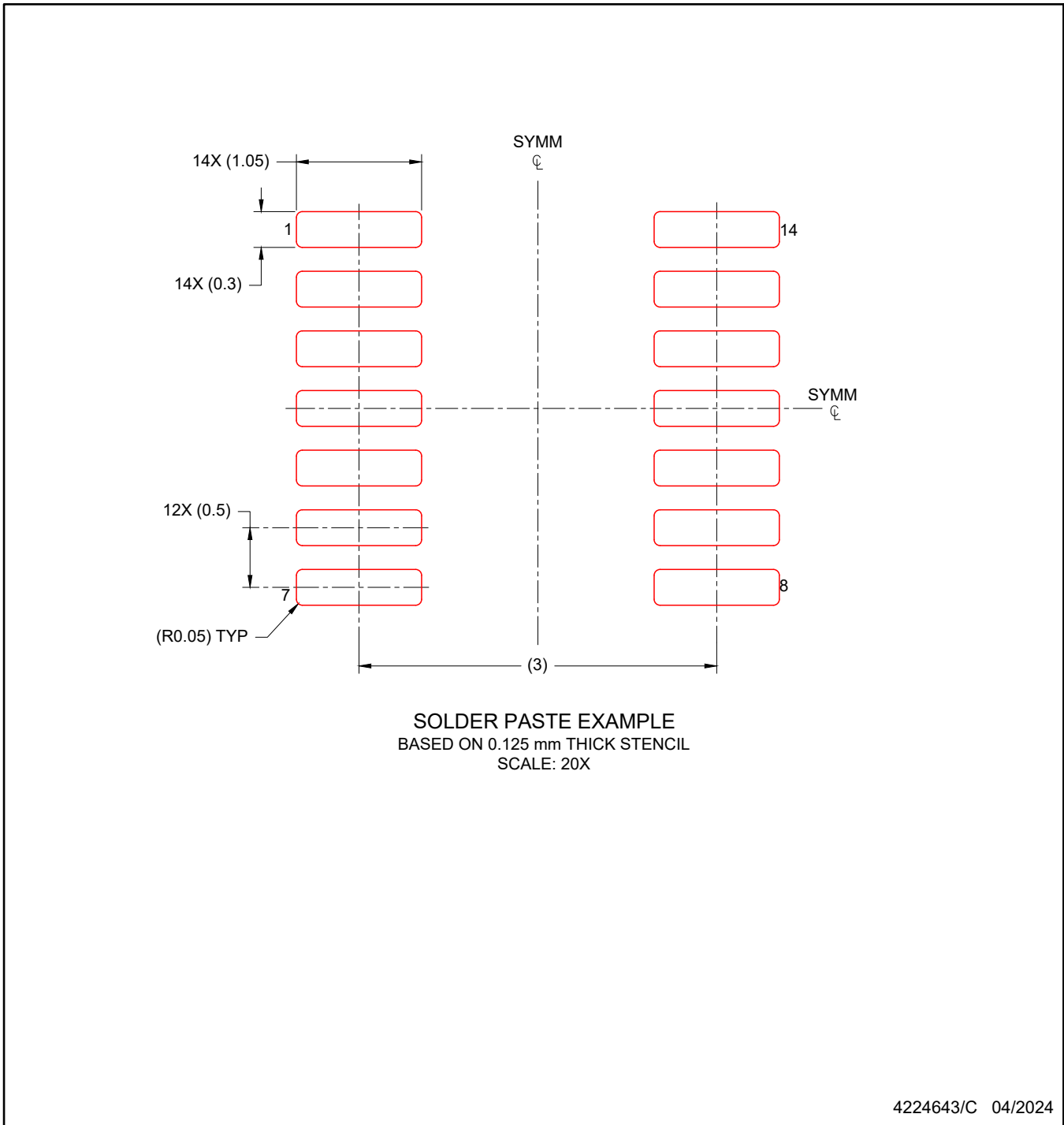
LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224643/C 04/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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