BATTERY-BACKUP SUPERVISOR FOR RAM RETENTION

FEATURES

- **Supply Current of 40 μA (Max)**
- **Battery Supply Current of 100 nA (Max)**
- **Precision 5-V Supply Voltage Monitor, Other Voltage Options on Request**
- **Backup-Battery Voltage Can Exceed V_{DD}**
- **Watchdog Timer With 800-ms Time-Out**
- **Power-On Reset Generator With Fixed 100-ms Reset Delay Time**
- **Voltage Monitor for Power-Fail or Low-Battery Monitoring**
- **Battery Freshness Seal (TPS3617 Only)**
- **8-Pin MSOP Package**
- **Temperature Range: –40° to +85°C**

APPLICATIONS

- **Fax Machines**
- **Set-Top Boxes**
- **Advanced Voice Mail Systems**
- **Portable Battery Powered Equipment**
- **Computer Equipment**
- **Advanced Modems**
- **Automotive Systems**
- **Portable Long-Time Monitoring Equipment**
- **Point-of-Sale Equipment**

DESCRIPTION

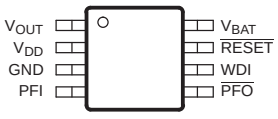
The TPS3617 and TPS3618 are battery-backup supervisors that monitor 5 V supplies. They provide a battery-backup function ideal for applications that require data retention of CMOS RAM during fault conditions. When the voltage at V_{DD} drops below a preset threshold (V_{IT}), the active low push-pull $\overline{\text{RESET}}$ output asserts, and V_{OUT} switches from V_{DD} to V_{BAT}. When V_{DD} rises above the trip threshold, V_{OUT} switches immediately from V_{BAT} to V_{DD}. The $\overline{\text{RESET}}$ output remains low until the delay time (t_d) expires. During power on, $\overline{\text{RESET}}$ is asserted when the supply voltage (V_{DD} or V_{BAT}) goes higher than 1.1 V.

The PFI and $\overline{\text{PFO}}$ pins are provided if additional voltage monitoring is needed. If the voltage at PFI is less than 1.15 V, the push-pull $\overline{\text{PFO}}$ pin will assert low. When the voltage at PFI exceeds the threshold voltage, $\overline{\text{PFO}}$ will go high.

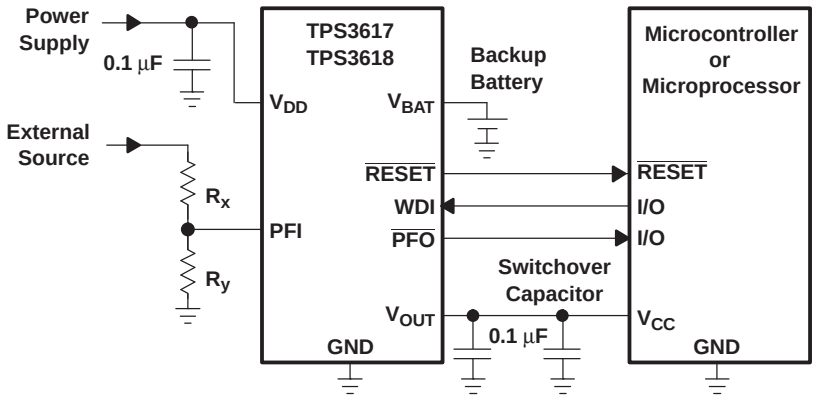
These devices also feature a watchdog timer pin (WDI) that monitors processor activity and asserts $\overline{\text{RESET}}$ if the the processor is inactive longer than the watchdog timeout period. If the watchdog timer is not used, the WDI pin should be left floating.

The TPS3617 and TPS3618 are available in an 8-pin MSOP package and are characterized for operation over a temperature range of –40°C to +85°C.

MSOP (DGK) Package
(TOP VIEW)



ACTUAL SIZE
3,05 mm x 4,98 mm



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE INFORMATION(1)

PRODUCT	NOMINAL SUPPLY VOLTAGE	THRESHOLD VOLTAGE (V_{IT})(2)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS3617-50	5V	4.55V	–40°C to +125°C	ASD	TPS3617-50DGK	Tube, 80
					TPS3617-50DGKR	Tape and Reel, 2500
TPS3618-50				ANK	TPS3618-50DGKT	Tape and Reel, 250
					TPS3618-50DGKR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or refer to our web site at www.ti.com.
(2) For other threshold votages, contact the local TI sales office for availability and lead time.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature (unless otherwise noted)(1)

	TPS3617, TPS3618	UNIT
Input voltage range, V_{DD}	–0.3 to 7	V
Input voltage range, PFI pin	–0.3 to (V_{DD} + 0.3)	V
WDI pin	–0.3 to (V_{DD} + 0.3)	V
Continuous output current at V_{OUT}, I_O	400	mA
All other pins, I_O	±10	mA
Operating junction temperature range, T_J(2)	–40 to +85	°C
Storage temperature range, T_{STG}	–65 to +150	°C
Lead temperature soldering 1,6 mm (1/16 inch) from case for 10 seconds	+260	°C
Continuous total power dissipation	See Dissipation Rating Table	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Due to the low dissipated power in this device, it is assumed that $T_J = T_A$.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq$ +25°C POWER RATING	DERATING FACTOR ABOVE T_A = +25°C	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
DGK	470 mW	3.76 mW/°C	301 mW	241 mW

ELECTRICAL CHARACTERISTICS

1.65 V ≤ V_{DD} ≤ 5.5 V, R_{LRESET} = 1 MΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = –40°C to +85°C), unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply range			1.65		5.5	V
I_{DD}	V_{DD} supply current	V_{OUT} = V_{DD}				40	µA
		V_{OUT} = V_{BAT}				40	
V_{BAT}	Battery supply range			1.5		5.5	V
I_{BAT}	V_{BAT} supply current	V_{OUT} = V_{DD}		–0.1		0.1	µ A
		V_{OUT} = V_{BAT}				0.5	
	Slew rate at V_{DD} or V_{BAT}					1	V/µs
V_I	Input volrage, any input			0		V_{DD} + 0.3	V
V_{OH}	High-level output voltage	$\overline{RESET}$	V_{DD} = 1.8 V, I_{OH} = –400 µA	V_{DD} – 0.2			V
			V_{DD} = 3.3 V, I_{OH} = –2 mA, V_{DD} = 5 V, I_{OH} = –3 mA	V_{DD} – 0.4			
		$\overline{PFO}$	V_{DD} = 1.8 V, I_{OH} = –20 µA	V_{DD} – 0.3			
			V_{DD} = 3.3 V, I_{OH} = –80 µA, V_{DD} = 5 V, I_{OH} = –120 µA	V_{DD} – 0.4			
V_{OL}	Low-level output voltage	$\overline{RESET}$ $\overline{PFO}$	V_{DD} = 1.8 V, I_{OL} = 400 µA			0.2	V
			V_{DD} = 3.3 V, I_{OL} = 2 mA, V_{DD} = 5 V, I_{OL} = 3 mA			0.4	
V_{RES}	Power-up reset voltage (1)		V_{BAT} > 1.1 V, or V_{DD} > 1.1 V, I_{OL} = 20 µA			0.4	V
V_{OUT}	Normal mode		I_O = 8.5 mA, V_{DD} = 1.8 V, V_{BAT} = 0 V	V_{DD} – 0.050			V
			I_O = 125 mA, V_{DD} = 3.3 V, V_{BAT} = 0 V	V_{DD} – 0.150			
			I_O = 200 mA, V_{DD} = 5 V, V_{BAT} = 0 V	V_{DD} – 0.200			
	Battery-backup mode		I_O = 0.5 mA, V_{BAT} = 1.5 V, V_{DD} = 0 V	V_{BAT} – 0.200			
			I_O = 7.5 mA, V_{BAT} = 3.3 V, V_{DD} = 0 V	V_{BAT} – 0.113			
$R_{DS(on)}$	V_{DD} to V_{OUT} on-resistance		V_{DD} = 5 V		0.6	1	Ω
	V_{BAT} to V_{OUT} on-resistance		V_{BAT} = 3.3 V		8	15	
I_O	Continuous output current at V_{OUT}					300	mA
V_{IT}	Negative-going input threshold voltage (2)	TPS3617-50	T_A = –40°C to +85°C	4.46	4.55		V
V_{PFI}		PFI		1.13	1.15	1.17	V
V_{HYS}	V_{IT} hysteresis		1.65 V < V_{IT} < 2.5 V		20		mV
			2.5 V < V_{IT} < 3.5 V		40		
			3.5 V < V_{IT} < 5.5 V		60		
	PFI hysteresis				12		
	V_{BSW} hysteresis (3)		V_{DD} = 1.8 V		55		
V_{IH}	WDI high-level input voltage			0.7 x V_{DD}			
V_{IL}	WDI low-level input voltage					0.3 x V_{DD}	
I_{IH}	WDI high-level input current (4)		WDI = V_{DD} = 5 V			150	µA
I_{IL}	WDI low-level input current (4)		WDI = 0 V, V_{DD} = 5 V			–150	µA
	WDI input transition rise and fall rate, Δt/ΔV					100	ns/V
I_I	PFI input current		PFI voltage < V_{DD}	–25		25	nA
I_{OS}	$\overline{PFO}$ short-circuit current		$\overline{PFO}$ = 0 V, V_{DD} = 1.8 V			–0.3	mA
			$\overline{PFO}$ = 0 V, V_{DD} = 3.3 V			–1.1	
			$\overline{PFO}$ = 0 V, V_{DD} = 5 V			–2.4	

(1) The lowest supply voltage at which $\overline{RESET}$ becomes active. t_r, V_{DD} ≥ 15 µs/V.
(2) To ensure the best stability of the threshold voltage, a bypass capacitor (ceramic, 0.1 µF) should be placed near the supply terminals.
(3) For V_{DD} < 1.6 V, V_{OUT} switches to V_{BAT} regardless of V_{BAT}.
(4) For details on how to optimize current consumption when using WDI, refer to the *Watchdog* section of this data sheet.

ELECTRICAL CHARACTERISTICS (continued)

1.65 V ≤ V_{DD} ≤ 5.5 V, R_{LRESET} = 1 MΩ, C_{LRESET} = 50 pF, over operating temperature range (T_J = –40°C to +85°C), unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance, any input		V_I = 0 V to 5 V		5		pF
t_w	Pulse Width	V_{DD}	$V_{IH} = V_{IT}$ + 0.2 V, $V_{IL} = V_{IT}$ – 0.2 V	6			µs
		WDI	$V_{DD} > V_{IT}$ + 0.2 V, V_{IL} = 0.3 x V_{DD}, V_{IH} = 0.7 x V_{DD}	100			ns
t_d	Delay time		$V_{DD} \geq V_{IT}$ + 0.2 V, See timing diagram	60	100	140	ms
$t_{(tout)}$	Watchdog time-out		$V_{DD} > V_{IT}$ + 0.2 V, See timing diagram	0.48	0.8	1.12	s
t_{PHL}	Propagation (delay) time, high-to-low-level output	V_{DD} to $\overline{RESET}$	$V_{IL} = V_{IT}$ – 0.2 V, $V_{IH} = V_{IT}$ + 0.2 V		2	5	µs
		PFI to $\overline{PFO}$	$V_{IL} = V_{PFI}$ – 0.2 V, $V_{IH} = V_{PFI}$ + 0.2 V		3	5	
Transition time		V_{DD} to V_{BAT}				3	µs

TIMING DIAGRAM

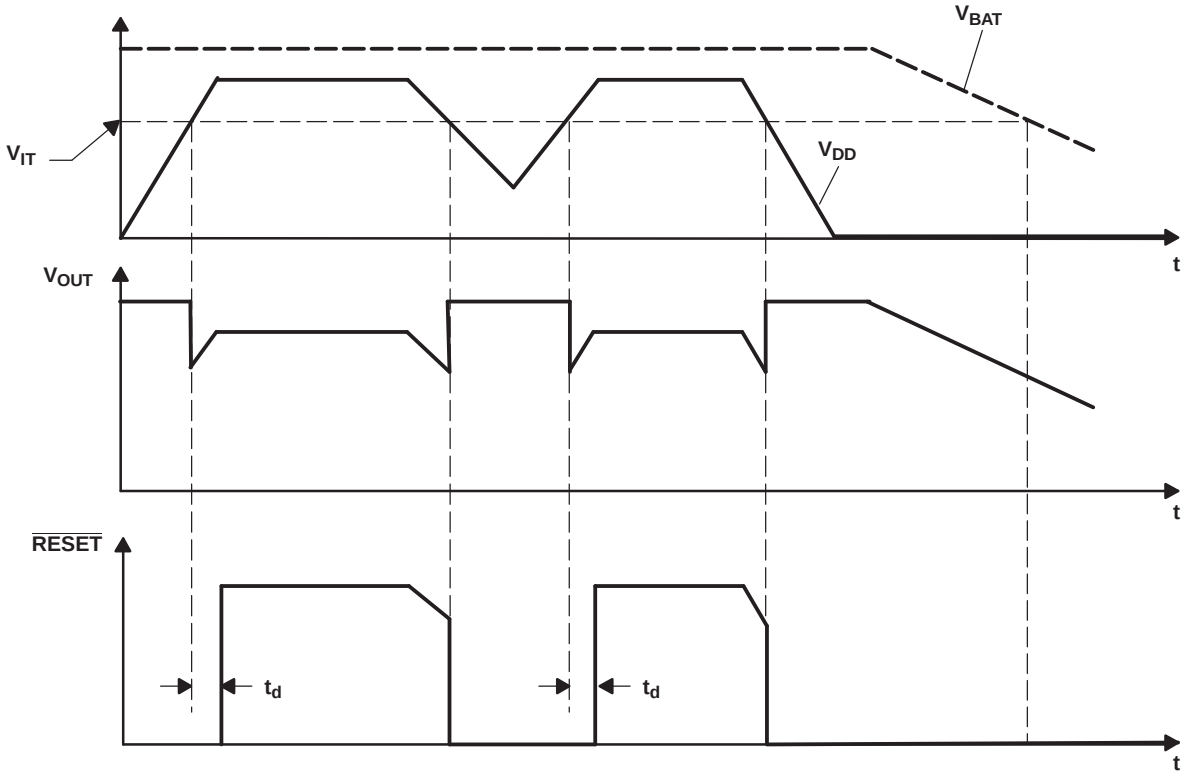


Table 1. FUNCTION TABLE

$V_{DD} > V_{IT}$	$V_{DD} > V_{BAT}$	V_{OUT}	$\overline{RESET}$
0	0	V_{BAT}	0
0	1	V_{DD}	0
1	0	V_{DD}	1
1	1	V_{DD}	1

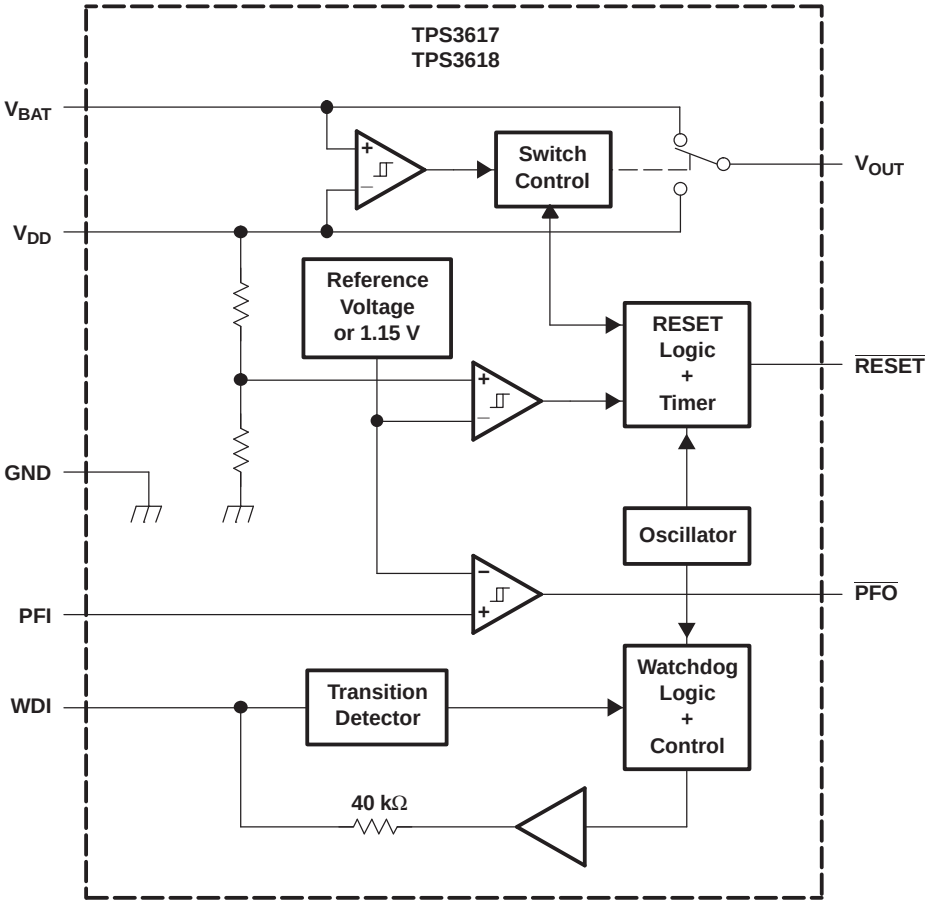
Table 2. $\overline{PFO}$ FUNCTION TABLE

PFI > V_{PFI}	$\overline{PFO}$
0	0
1	1
CONDITION: $V_{DD} > V_{DD(MIN)}$	

Table 3. TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	3	I	Ground
PFI	4	I	Power-fail comparator input
$\overline{PFO}$	5	O	Power-fail comparator output; asserts low when PFI < 1.15 V
$\overline{RESET}$	7	O	Active-low push-pull reset output
V_{BAT}	8	I	Backup-battery input
V_{DD}	2	I	Input supply voltage
V_{OUT}	1	O	Supply output
WDI	6	I	Watchdog input. Should be left floating if not used.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

			FIGURE
$r_{DS(on)}$	Static drain-source on-state resistance (V_{DD} to V_{OUT})	vs Output current	3
	Static drain-source on-state resistance (V_{BAT} to V_{OUT})	vs Output current	4
I_{DD}	Supply current	vs Supply voltage	5
V_{IT}	Input threshold voltage at $\overline{RESET}$	vs Free-air temperature	6
V_{OH}	High-level output voltage at $\overline{RESET}$	vs High-level output current	7, 8
	High-level output voltage at $\overline{PFO}$		9, 10
V_{OL}	Low-level output voltage at $\overline{RESET}$	vs Low-level output current	11, 12
	Minimum pulse duration at V_{DD}	vs Threshold voltage overdrive at V_{DD}	13
	Minimum pulse duration at PFI	vs Threshold voltage overdrive at PFI	14

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{DD} to V_{OUT}) vs OUTPUT CURRENT

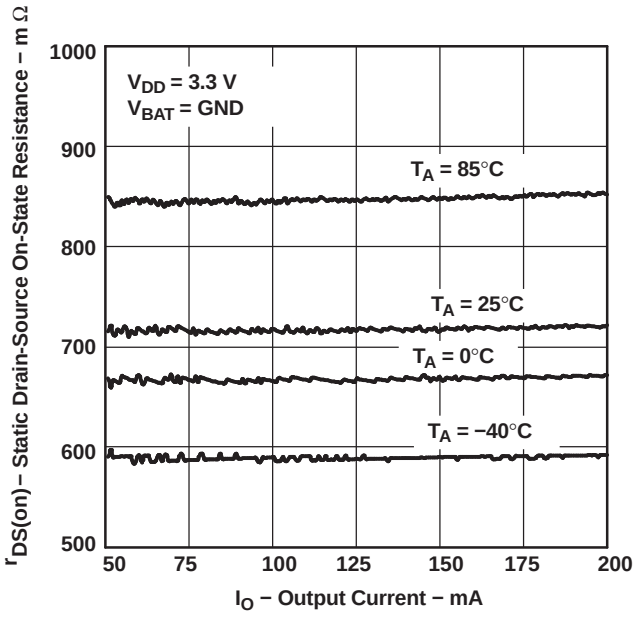


Figure 1.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE (V_{BAT} to V_{OUT}) vs OUTPUT CURRENT

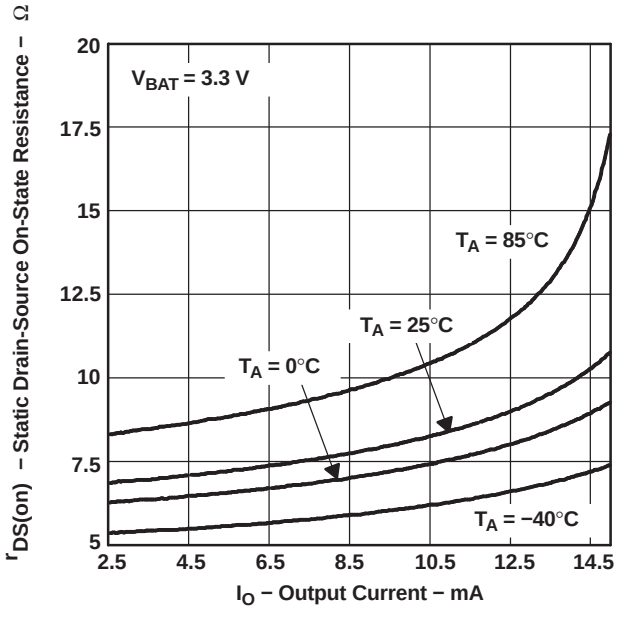


Figure 2.

SUPPLY CURRENT
vs
SUPPLE VOLTAGE

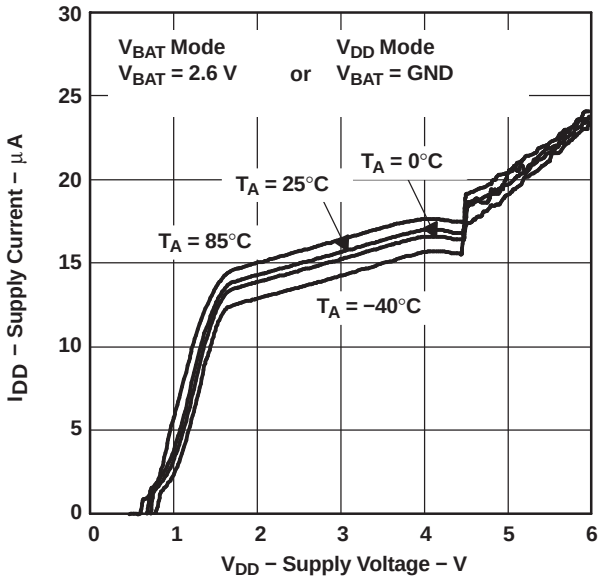


Figure 3.

INPUT THRESHOLD VOLTAGE AT $\overline{\text{RESET}}$
vs
FREE-AIR TEMPERATURE

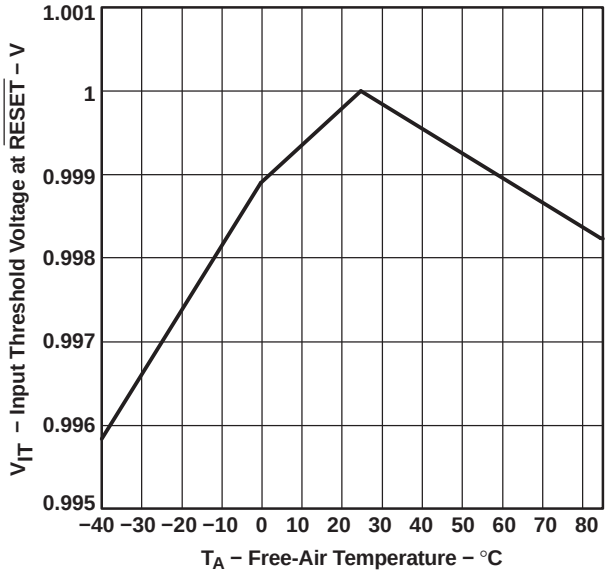


Figure 4.

HIGH-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
HIGH-LEVEL OUTPUT CURRENT

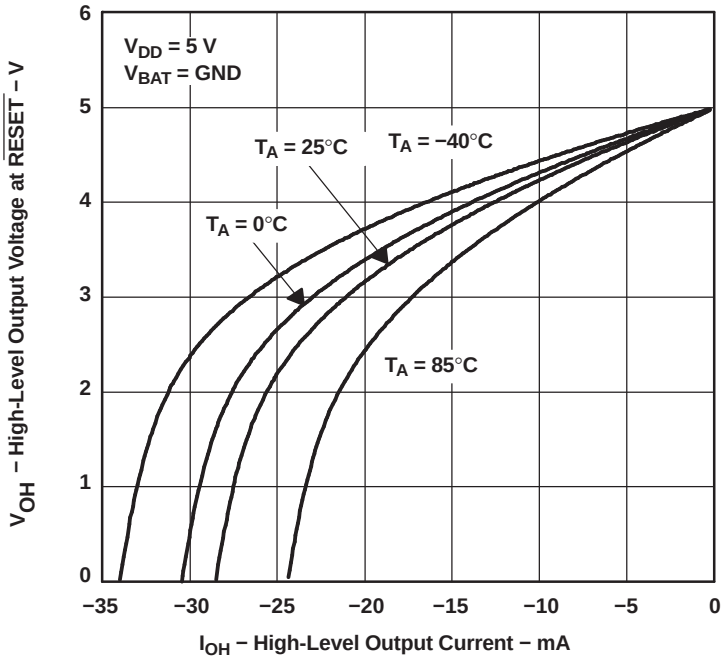


Figure 5.

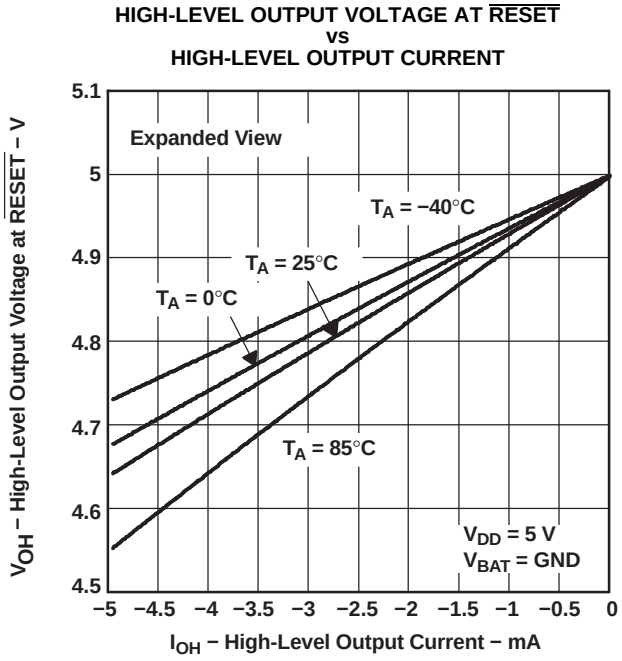


Figure 6.

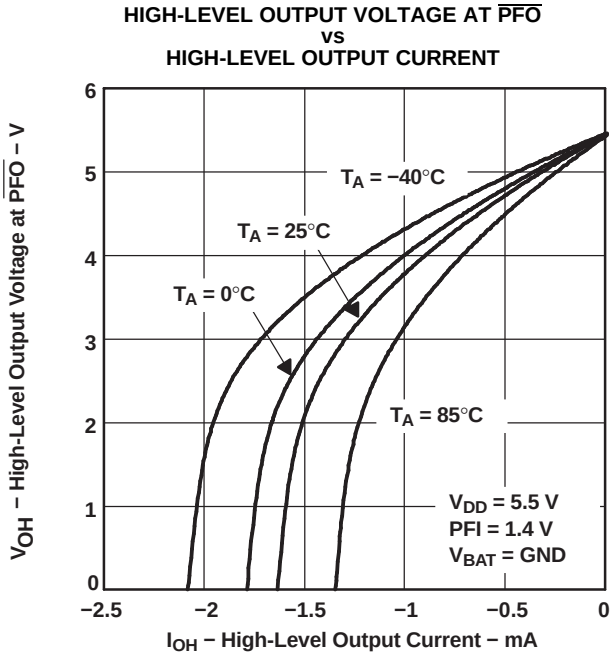


Figure 7.

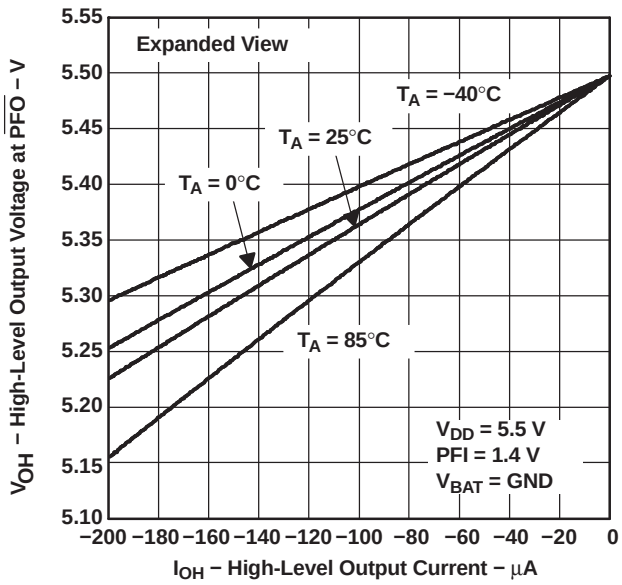


Figure 8.

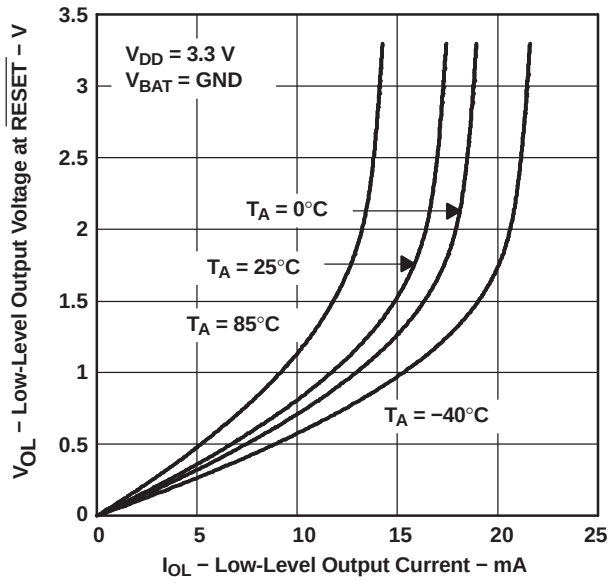


Figure 9.

LOW-LEVEL OUTPUT VOLTAGE AT $\overline{\text{RESET}}$
vs
LOW-LEVEL OUTPUT CURRENT

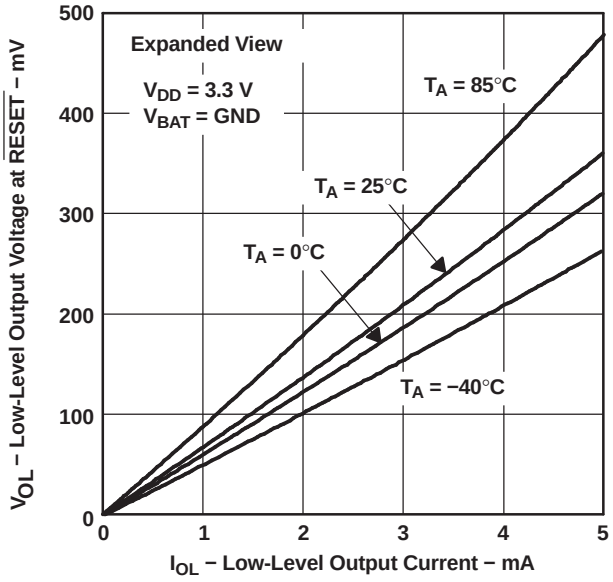


Figure 10.

MINIMUM PULSE DURATION AT V_{DD}
vs
THRESHOLD VOLTAGE OVERDRIVE AT V_{DD}

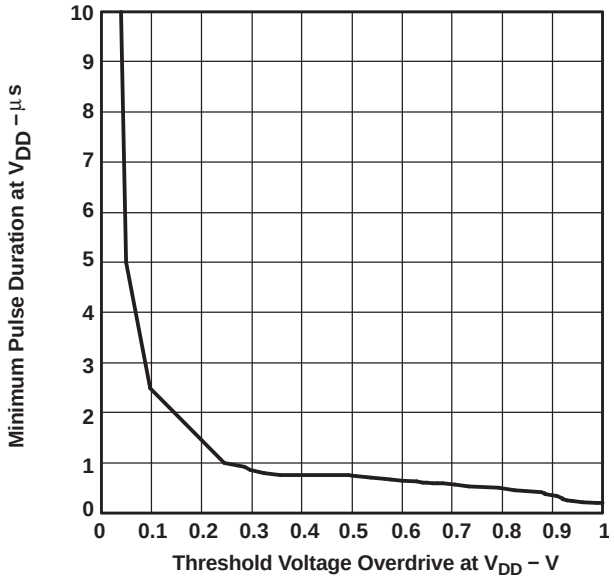


Figure 11.

MINIMUM PULSE DURATION AT PFI
vs
THRESHOLD VOLTAGE OVERDRIVE AT PFI

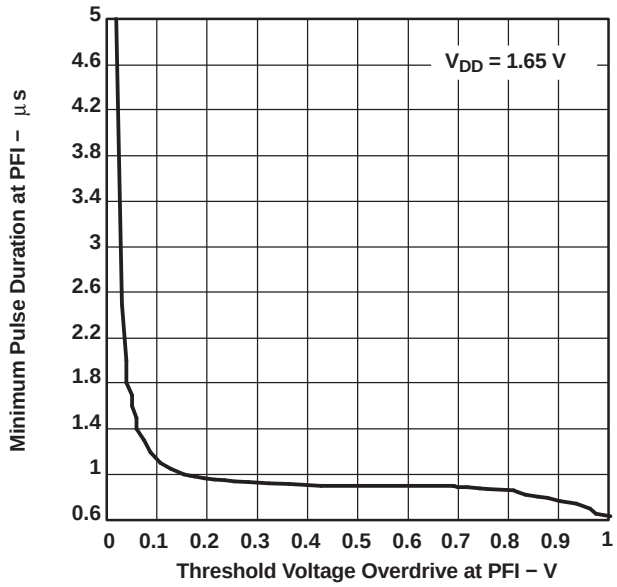


Figure 12.

DETAILED DESCRIPTION

BATTERY FRESHNESS SEAL (TPS3617 Only)

The battery freshness seal of the TPS3617 family disconnects the backup battery from the internal circuitry until it is needed. This ensures that the backup battery connected to V_{BAT} should be fresh when the final product is put to use. The following steps explain how to enable the freshness seal mode:

1. Connect V_{BAT} ($V_{BAT} > V_{BAT(min)}$).
2. Ground $\overline{PFO}$.
3. Connect PFI to V_{DD} (PFI = V_{DD}).
4. Connect V_{DD} to power supply ($V_{DD} > V_{IT}$) and keep connected for 5 ms < t < 35 ms.

The battery freshness seal mode is disabled by the positive-going edge of $\overline{RESET}$ when V_{DD} is applied.

POWER-FAIL COMPARATOR (PFI AND $\overline{PFO}$)

An additional comparator monitors voltages other than the nominal supply voltage. The power-fail-input (PFI) can be compared with an internal voltage reference of 1.15 V. If the input voltage falls below the power-fail threshold ($V_{(PFI)}$) of 1.15 V typical, the power-fail output ($\overline{PFO}$) goes low. If it goes above $V_{(PFI)}$ plus about 12-mV hysteresis, the output returns to high. By connecting two external resistors it is possible to supervise any voltages above $V_{(PFI)}$. The sum of both resistors should be about 1 MΩ, to minimize power consumption and also to ensure that the current in the PFI pin can be neglected compared with the current through the resistor network. The tolerance of the external resistors should be not more than 1% to ensure minimal variation of the sensed voltage. If the power-fail comparator is unused, connect PFI to ground and leave the $\overline{PFO}$ unconnected.

WATCHDOG

In a microprocessor- or DSP-based system, it is not only important to supervise the supply voltage, it is also important to ensure correct program execution. The task of a watchdog is to ensure that the program is not stalled in an indefinite loop. The microprocessor, microcontroller, or DSP has to toggle the watchdog input within 0.8 s typically, to avoid a timeout from occurring. Either a low-to-high or a high-to-low transition resets the internal watchdog timer. If the input is unconnected, the watchdog is disabled and should be retriggered internally. See Figure 13 for the watchdog timing diagram.

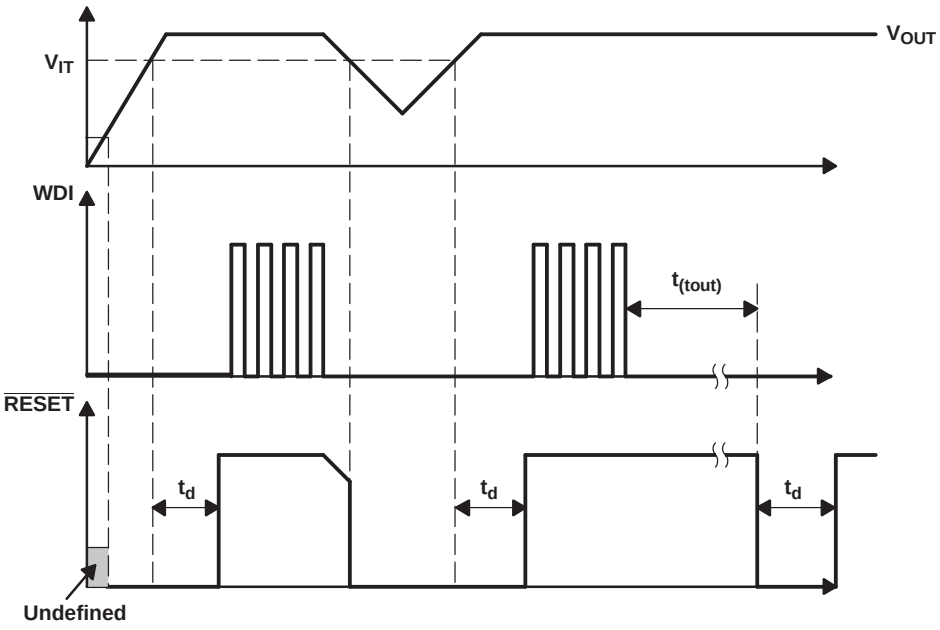


Figure 13. Watchdog Timing

DETAILED DESCRIPTION (continued)

SAVING CURRENT WHILE USING THE WATCHDOG

The watchdog input is internally driven low during the first 7/8 of the watchdog time-out period, then momentarily pulses high, resetting the watchdog counter. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog time-out period, pulsing it low-high-low once within 7/8 of the watchdog time-out period to reset the watchdog timer. If instead, WDI is externally driven high for the majority of the time-out period, a current of e.g. 5.0 V/40 kΩ ≈ 125 µA can flow into WDI.

BACKUP-BATTERY SWITCHOVER

In case of a brownout or power failure, it may be necessary to preserve the contents of RAM. If a backup battery is installed at V_{BAT}, the device automatically switches the connected RAM to backup power when V_{DD} fails. In order to allow the backup battery (e.g., a 3.6-V lithium cell) to have a higher voltage than V_{DD}, these supervisors should not connect V_{BAT} to V_{OUT} when V_{BAT} is greater than V_{DD}. V_{BAT} only connects to V_{OUT} (through a 15-Ω switch) when V_{DD} falls below V_{IT} and V_{BAT} is greater than V_{DD}. When V_{DD} recovers, switchover is deferred either until V_{DD} crosses V_{BAT}, or until V_{DD} rises above the reset threshold V_{IT}. V_{OUT} connects to V_{DD} through a 1-Ω (max) PMOS switch when V_{DD} crosses the reset threshold.

FUNCTION TABLE		
$V_{DD} > V_{BAT}$	$V_{DD} > V_{IT}$	V_{OUT}
1	1	V_{DD}
1	0	V_{DD}
0	1	V_{DD}
0	0	V_{BAT}

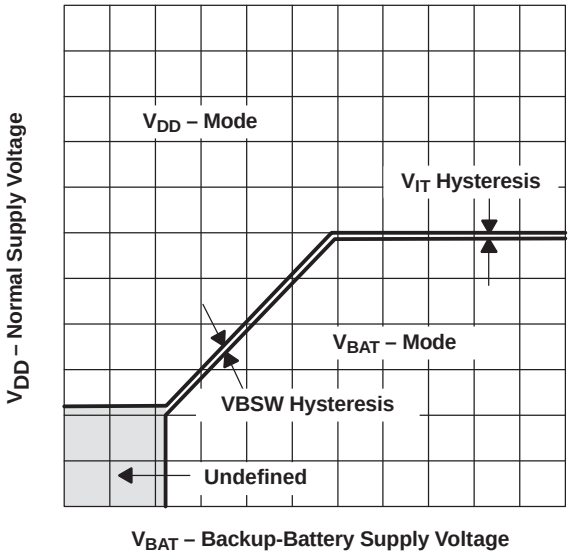


Figure 14. V_{DD} – V_{BAT} Switchover

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS3617-50DGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASD
TPS3617-50DGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ASD
TPS3618-50DGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANK
TPS3618-50DGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ANK

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

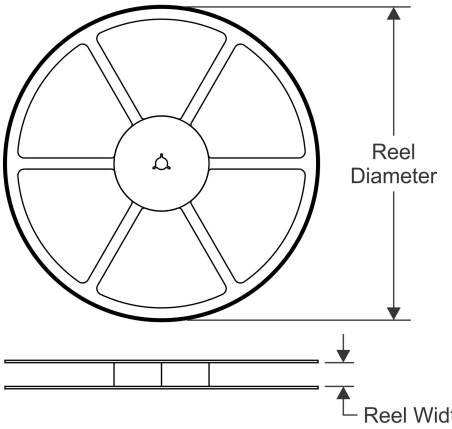
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

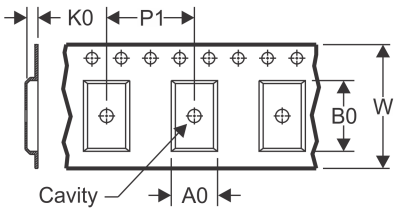
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

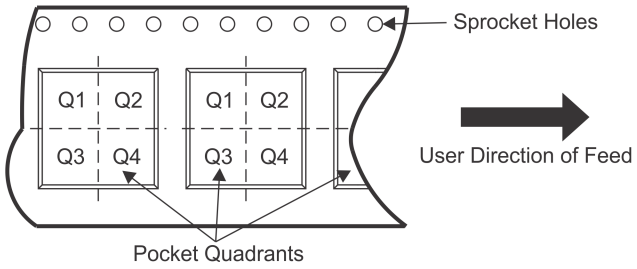


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

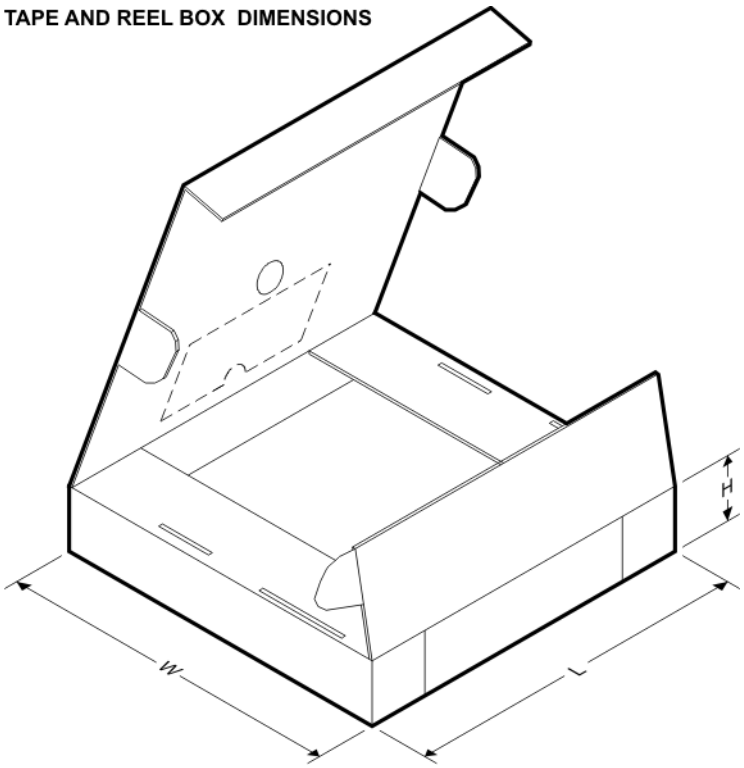
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3617-50DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS3618-50DGKT	VSSOP	DGK	8	250	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

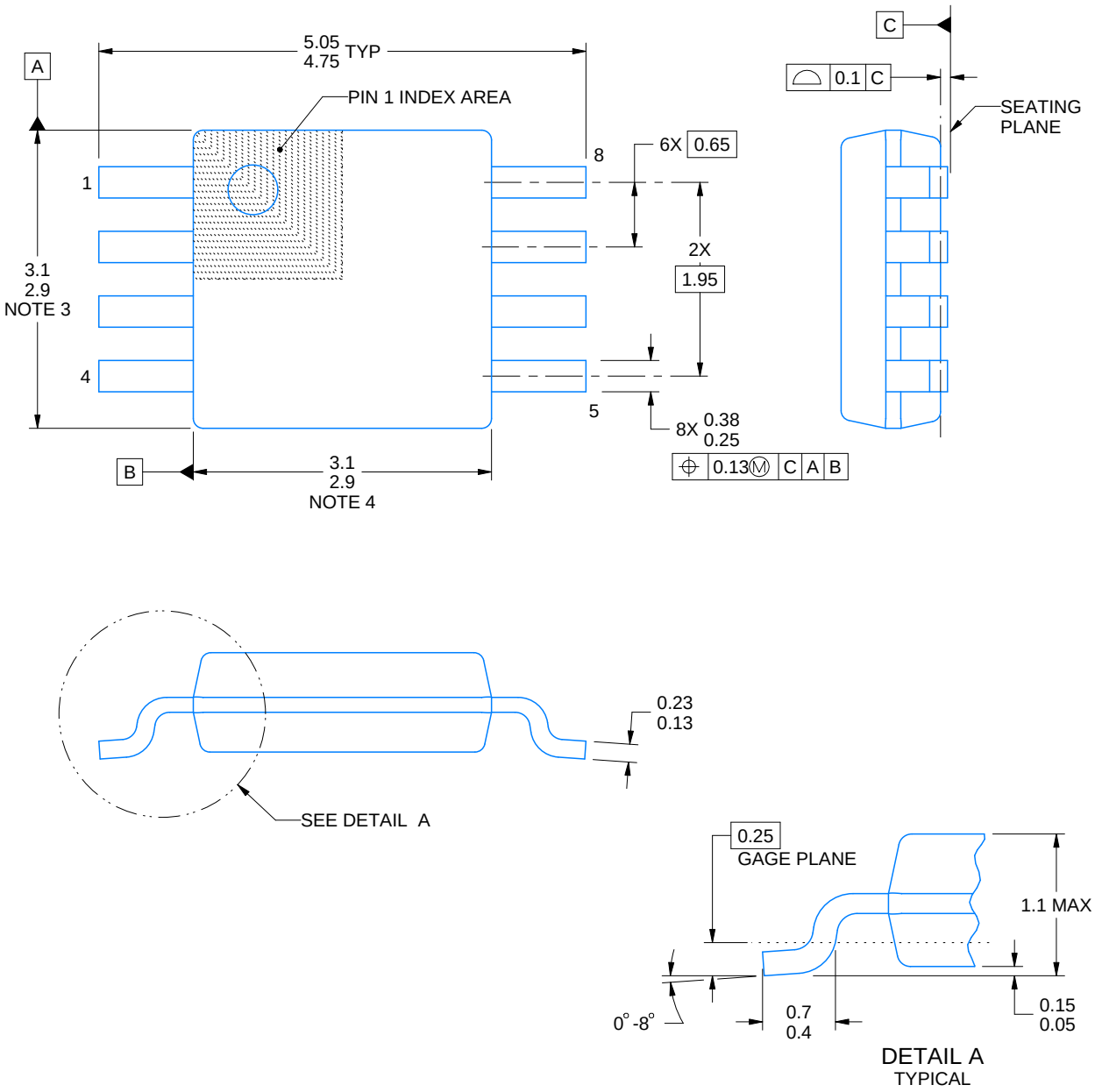
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3617-50DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
TPS3618-50DGKT	VSSOP	DGK	8	250	358.0	335.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

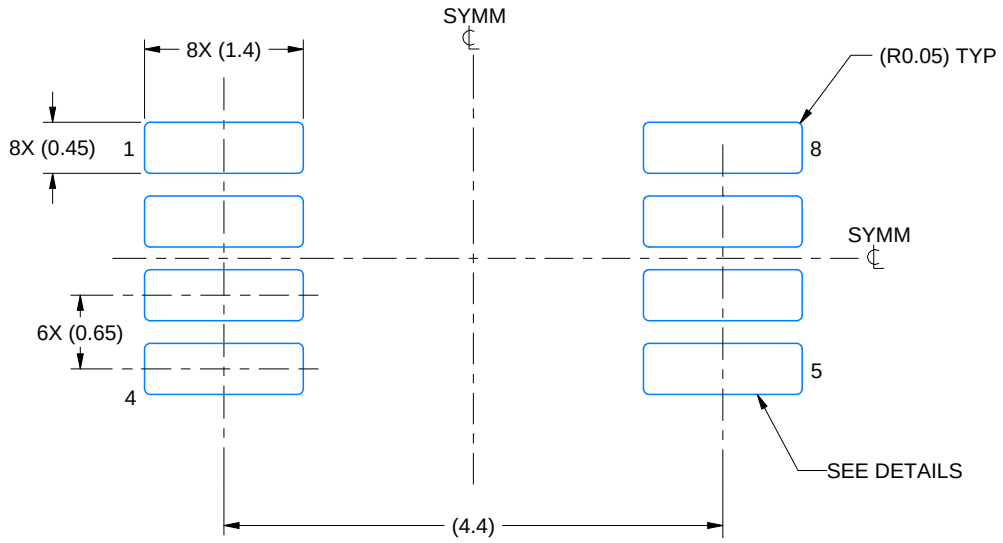
SMALL OUTLINE PACKAGE



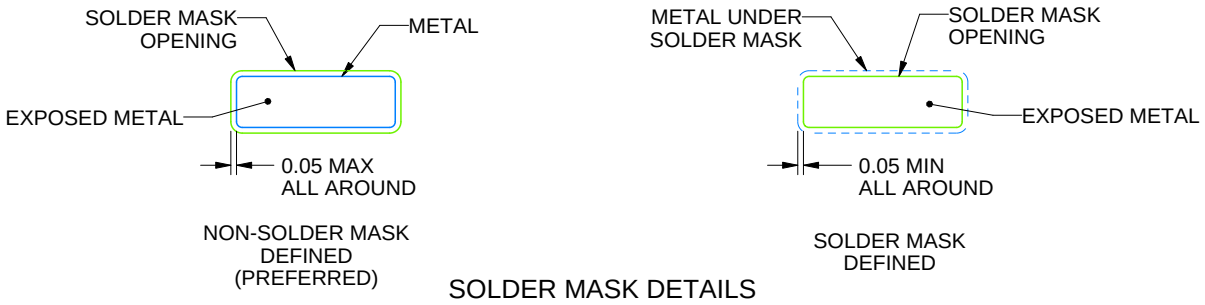
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

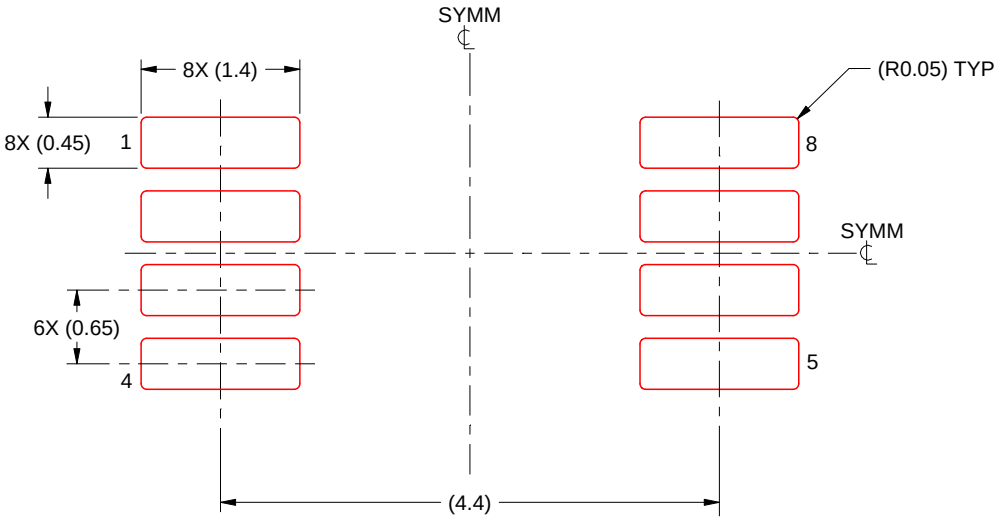


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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