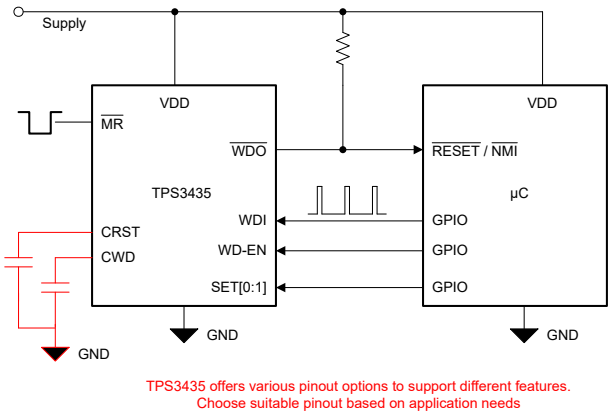
TPS3435 具有精密超时看门狗计时器的毫微级 IQ

1 特性

- 出厂编程或用户可编程的看门狗超时
  - ±10% 精确计时器（最大值）
  - 出厂编程：1 毫秒至 100 秒
- 出厂编程或用户可编程的复位延迟
  - ±10% 精确计时器（最大值）
  - 出厂编程选项：2 毫秒至 10 秒
- 输入电压范围：V_{DD} = 1.04 V 至 6.0 V
- 超低电源电流：I_{DD} = 250nA（典型值）
- 开漏、推挽；低电平有效输出
- 各种可编程选项：
  - 看门狗启用/禁用
  - 看门狗启动延迟：无延迟至 10 秒
  - 动态计时器扩展：1X 至 256X
  - 锁存输出选项
- $\overline{MR}$ 功能支持

2 应用

- 机器人伺服驱动器
- 混合模块（AI、AO、DI、DO）
- HVAC 控制器
- 电表
- 输液泵
- 外科手术设备



典型应用电路

3 说明

TPS3435 是一款超低功耗（典型值为 250nA）器件，可提供具有可编程超时看门狗计时器的。

TPS3435 可提供具有多种功能的高精度超时看门狗计时器，广泛适用于各种应用。该超时看门狗计时器可以进行出厂编程或由用户使用外部电容器进行编程。计时器值可以使用逻辑引脚的组合来动态更改。可以使用专用引脚或计时器扩展引脚的组合来启用或禁用看门狗功能。该器件还提供启动延迟选项，可在主机上电后立即禁用看门狗监控并保持固定时间。

$\overline{WDO}$ 延迟可设定为出厂编程的默认延迟设置或通过外部电容器进行编程。该器件还提供锁存输出操作，看门狗故障清除之前会锁存输出。

TPS3435 提供了 TPS3431 器件系列的性能升级替代产品。TPS3435 采用小型 6 引脚 WSON 和 8 引脚 SOT23 封装。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS3435	DDF (8)	2.90mm × 1.60mm
TPS3435	DSE (6) (2)	1.50mm x 1.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 预发布封装。

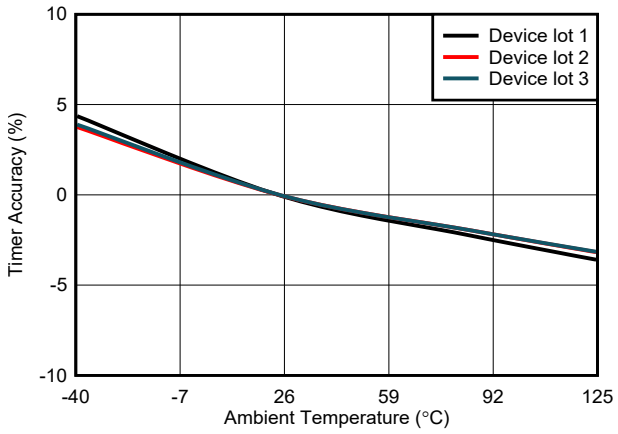


Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 器件比较

图 5-1 显示了 TPS3435 的器件命名规则。对于所有可能的输出类型、看门狗时间选项和输出断言延迟选项，请参阅节 8 了解更多详细信息。有关其他选项的详细信息和可用性，请联系 TI 销售代码或访问 TI 的 E2E 论坛。

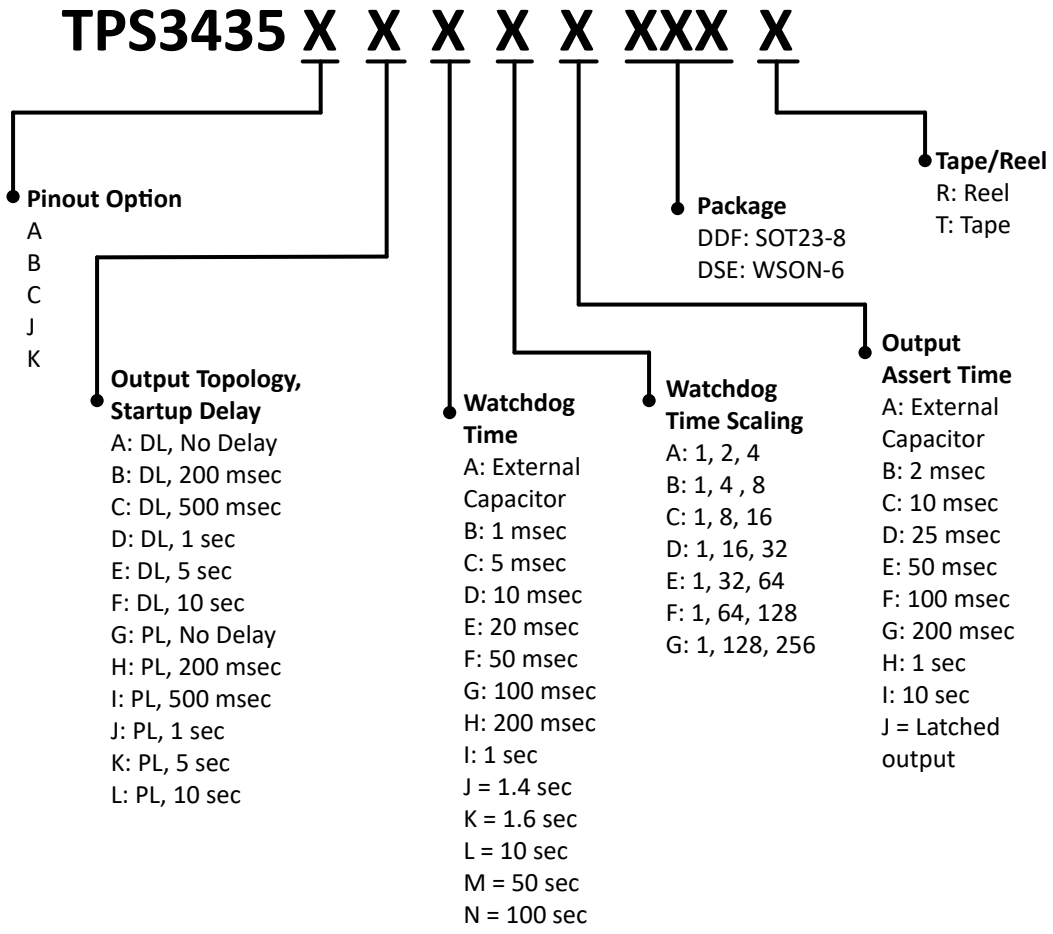


图 5-1. 器件命名规则

TPS3435 属于引脚兼容的器件系列，提供了不同的功能集，详见表 5-1。

表 5-1. 引脚兼容的器件系列

器件	电压监控器	看门狗类型
TPS35	是	Timeout
TPS36	是	窗口
TPS3435	否	Timeout
TPS3436	否	窗口

6 Pin Configuration and Functions

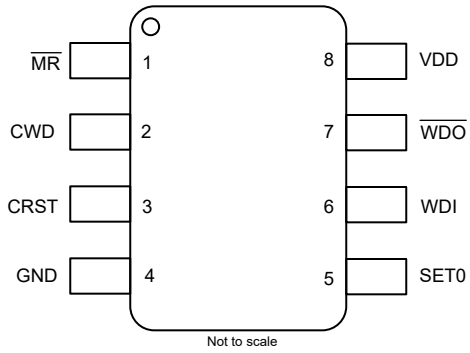


图 6-1. Pin Configuration Option A
DDF Package, 8-Pin SOT-23,
TPS3435 Top View

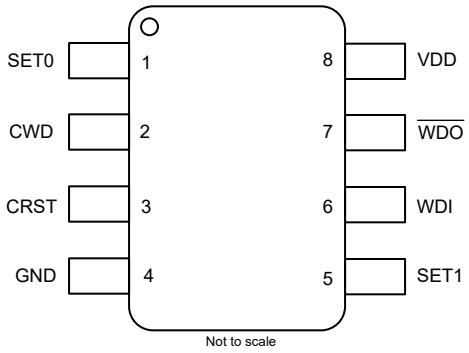


图 6-2. Pin Configuration Option B
DDF Package, 8-Pin SOT-23,
TPS3435 Top View

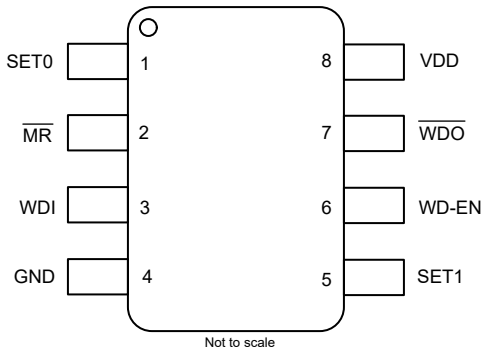


图 6-3. Pin Configuration Option C
DDF Package, 8-Pin SOT-23,
TPS3435 Top View

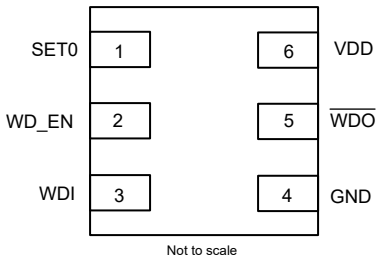


图 6-4. Pin Configuration Option J
DSE Package, 6-Pin WSON,
TPS3435 Top View

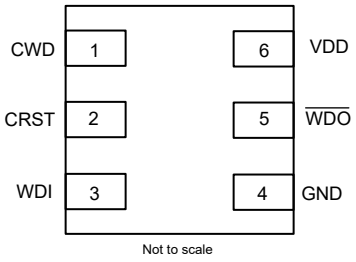


图 6-5. Pin Configuration Option K
DSE Package, 6-Pin WSON,
TPS3435 Top View

表 6-1. Pin Functions

PIN NAME	PIN NUMBER					I/O	DESCRIPTION
	PINOUT A	PINOUT B	PINOUT C	PINOUT J	PINOUT K		
CRST	3	3	—	—	2	I	Programmable WDO assert time pin. Connect a capacitor between this pin and GND to program the WDO assert time period. See 节 8.3.3 for more details.
CWD	2	2	—	—	1	I	Programmable watchdog timeout input. Watchdog timeout is set by connecting a capacitor between this pin and ground. See 节 8.3.1.1 for more details.
GND	4	4	4	4	4	—	Ground pin
$\overline{MR}$	1	—	2	—	—	I	Manual reset pin. A logic low on this pin asserts the $\overline{WDO}$ output. See 节 8.3.2 for more details.
$\overline{WDO}$	7	7	7	5	5	O	Watchdog output. Connect $\overline{WDO}$ to VDD using pull up resistance when using open drain output. $\overline{WDO}$ is asserted when a watchdog error occurs or $\overline{MR}$ pin is driven LOW. See 节 8.3.3 for more details.
SET0	5	1	1	1	—	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog timer scaling and enable-disable the watchdog; see 节 8.3.1.4 for more details.
SET1	—	5	5	—	—	I	Logic input. SET0, SET1, and WD-EN pins select the watchdog timer scaling and enable-disable the watchdog; see 节 8.3.1.4 for more details.
VDD	8	8	8	6	6	I	Supply voltage pin. For noisy systems, connecting a 0.1-µF bypass capacitor is recommended.
WD-EN	—	—	6	2	—	I	Logic input. Logic high input enables the watchdog monitoring feature. See 节 8.3.1.2 for more details.
WDI	6	6	3	3	3	I	Watchdog input. A falling transition (edge) must occur at this pin before the timeout expires in order for $\overline{WDO}$ to not assert. See 节 8.3.1 for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	6.5	V
Voltage	C_{WD}, C_{RST}, WD – EN, SETx, WDI, $\overline{MR}$ (2), $\overline{WDO}$ (Push Pull)	–0.3	V_{DD}+0.3 (3)	V
	$\overline{WDO}$ (Open Drain)	–0.3	6.5	
Current	$\overline{WDO}$ pin	–20	20	mA
Temperature (4)	Operating ambient temperature, T_A	–40	125	℃
Temperature (4)	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$.
(3) The absolute maximum rating is (VDD + 0.3) V or 6.5 V, whichever is smaller
(4) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD (Active Low output)	0.9		6	V
	C_{WD}, C_{RST}, WD – EN, SETx, WDI, $\overline{MR}$ (1)	0		VDD	
	$\overline{WDO}$(Open Drain)	0		6	
	$\overline{WDO}$ (Push Pull)	0		VDD	
Current	$\overline{WDO}$ pin current	–5		5	mA
C_{RST}	C_{RST} pin capacitor range	1.5		1800	nF
C_{WD}	C_{WD} pin capacitor range	1.5		1000	nF
T_A	Operating ambient temperature	–40		125	℃

(1) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$. V_{MR} should not be higher than V_{DD}.

7.4 Thermal Information

THERMAL METRIC(1)		TPS3435 DDF (SOT23-8) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	175.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At 1.04 V ≤ V_{DD} ≤ 6 V, $\overline{MR}$ = Open, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40℃ to 125℃, unless otherwise noted. VDD ramp rate ≤ 1 V/µs. Typical values are at T_A = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage	Active LOW output	1.04		6	V
I_{DD}	Supply current into VDD pin (1)	T_A = –40℃ to 85℃		0.25	0.8	µA
				0.25	3	
V_{IL}	Low level input voltage WD – EN, WDI, SETx, $\overline{MR}$ (1)				0.3V_{DD}	V
V_{IH}	High level input voltage WD – EN, WDI, SETx, $\overline{MR}$ (1)		0.7V_{DD}			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance			100		kΩ
$\overline{WDO}$ (Open-drain active-low)						
V_{OL}	Low level output voltage	V_{DD} =1.5 V $I_{OUT(Sink)}$ = 500 µA			300	mV
		V_{DD} = 3.3 V $I_{OUT(Sink)}$ = 2 mA			300	
$I_{lkg(OD)}$	Open-Drain output leakage current	V_{DD} = V_{PULLUP} = 6V T_A = –40℃ to 85℃		10	30	nA
		V_{DD} = V_{PULLUP} = 6V		10	60	nA
$\overline{WDO}$ (Push-pull active-low)						
V_{POR}	Power on $\overline{WDO}$ voltage (2)	$V_{OH(min)}$ = 0.8 VDD $I_{out\ (source)}$ = 15 µA			900	mV
V_{OL}	Low level output voltage	V_{DD} = 1.5 V $I_{OUT(Sink)}$ = 500 µA			300	mV
		V_{DD} = 3.3 V $I_{OUT(Sink)}$ = 2 mA			300	
V_{OH}	High level output voltage	V_{DD} = 1.8 V $I_{OUT(Source)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 3.3 V $I_{OUT(Source)}$ = 500 µA	0.8V_{DD}			
		V_{DD} = 6 V $I_{OUT(Source)}$ = 2 mA	0.8V_{DD}			

(1) If the logic signal driving $\overline{MR}$ is less than V_{DD}, then additional current flows into V_{DD} and out of $\overline{MR}$.
(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state

7.6 Timing Requirements

At 1.04 V ≤ V_{DD} ≤ 6 V, $\overline{MR}$ = Open, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output RESET / WDO load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40℃ to 125℃, unless otherwise noted. VDD ramp rate ≤ 1 V/µs. Typical values are at T_A = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\overline{MR}\_PW}$	$\overline{MR}$ pin pulse duration to assert output			100		ns
t_{P-WD}	WDI pulse duration to start next frame (1)		500			ns
$t_{HD-WDEN}$	WD – EN hold time to enable or disable WD operation (1)		200			µs
$t_{HD-SETx}$	SETx hold time to change WD timer setting (1)		150			µs
t_{WD}	Watchdog timeout period	Orderable Option TPS3435xxB	0.8	1	1.2	ms
		Orderable Option TPS3435xxC	4	5	6	
		Orderable Option TPS3435xxD	9	10	11	
		Orderable Option TPS3435xxE	18	20	22	
		Orderable Option TPS3435xxF	45	50	55	
		Orderable Option TPS3435xxG	90	100	110	
		Orderable Option TPS3435xxH	180	200	220	
		Orderable Option TPS3435xxI	0.9	1	1.1	s
		Orderable Option TPS3435xxJ	1.26	1.4	1.54	
		Orderable Option TPS3435xxK	1.44	1.6	1.76	
		Orderable Option TPS3435xxL	9	10	11	
		Orderable Option TPS3435xxM	45	50	55	
		Orderable Option TPS3435xxN	90	100	110	

(1) Not production tested

7.7 Switching Characteristics

At 1.04 V ≤ V_{DD} ≤ 6 V, $\overline{MR}$ = Open, $\overline{WDO}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output RESET / WDO load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40℃ to 125℃, unless otherwise noted. VDD ramp rate ≤ 1 V/µs. Typical values are at T_A = 25℃

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup delay (1)				500	µs
t_{SD}	Watchdog startup delay	Orderable part number TPS3435xA, TPS3435xG		0		ms
		Orderable part number TPS3435xB, TPS3435xH	180	200	220	
		Orderable part number TPS3435xC, TPS3435xI	450	500	550	
		Orderable part number TPS3435xD, TPS3435xJ	0.9	1	1.1	s
		Orderable part number TPS3435xE, TPS3435xK	4.5	5	5.5	
		Orderable part number TPS3435xF, TPS3435xL	9	10	11	
t_{WDO}	Watchdog assert time delay	Orderable part number TPS3435xxxxB	1.6	2	2.4	ms
		Orderable part number TPS3435xxxxC	9	10	11	ms
		Orderable part number TPS3435xxxxD	22.5	25	27.5	ms
		Orderable part number TPS3435xxxxE	45	50	55	ms
		Orderable part number TPS3435xxxxF	90	100	110	ms
		Orderable part number TPS3435xxxxG	180	200	220	ms
		Orderable part number TPS3435xxxxH	0.9	1	1.1	s
		Orderable part number TPS3435xxxxI	9	10	11	s
$t_{\overline{MR}\_WDO}$	Propagation delay from $\overline{MR}$ low to WDO assertion	V_{DD} ≥ 1.25 V, $\overline{MR}$ = $V_{\overline{MR}\_H}$ to $V_{\overline{MR}\_L}$		100		ns

(1) Specified by design parameter.

7.8 Timing Diagrams

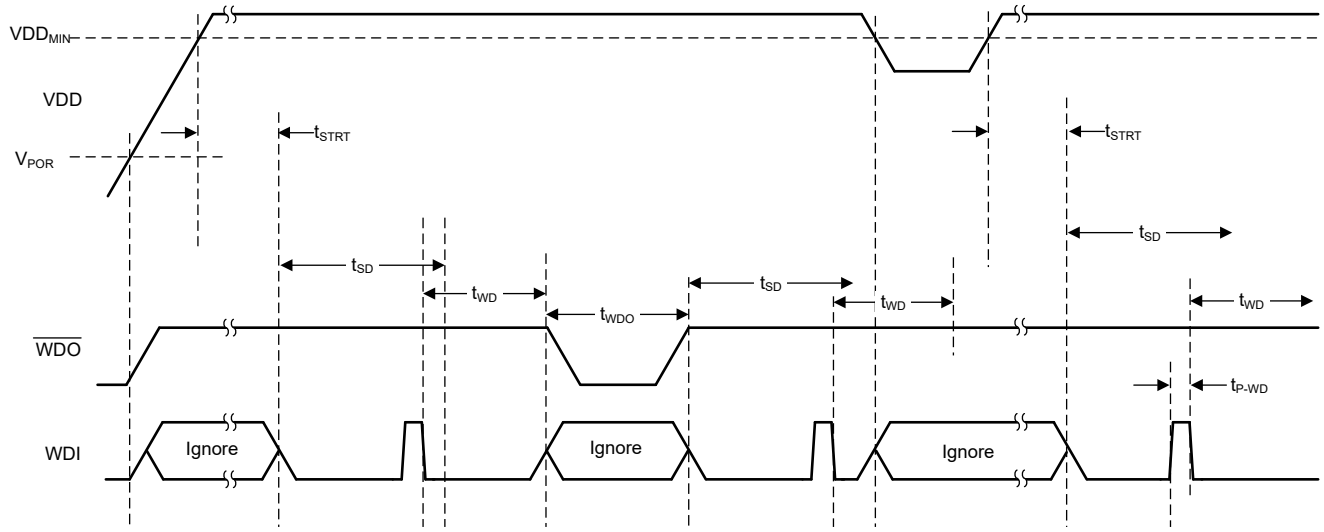


图 7-1. Functional Timing Diagram

7.9 Typical Characteristics

all curves are taken at T_A = 25°C (unless otherwise noted)

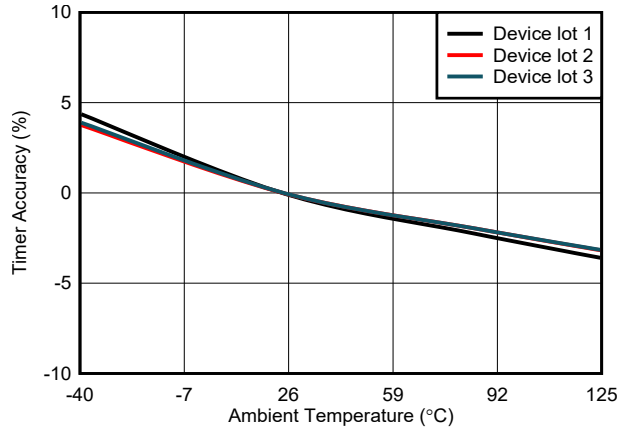


图 7-2. Timer Accuracy vs Temperature

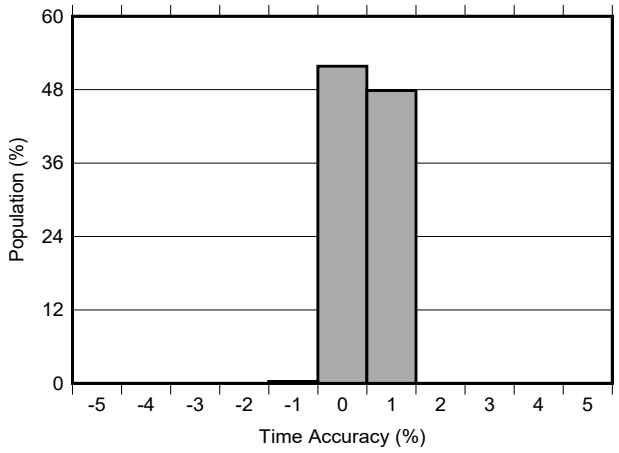


图 7-3. Timer Accuracy Histogram

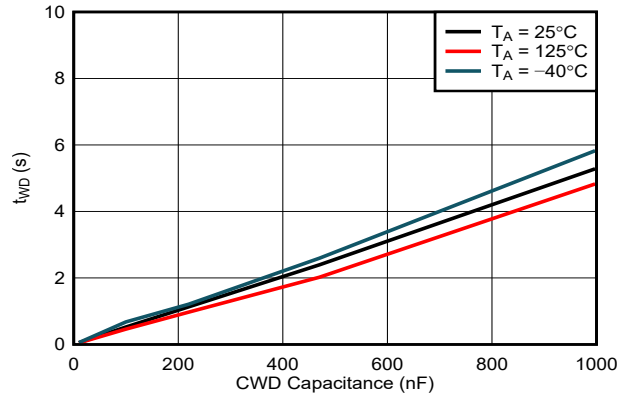


图 7-4. t_{WD} vs Capacitance

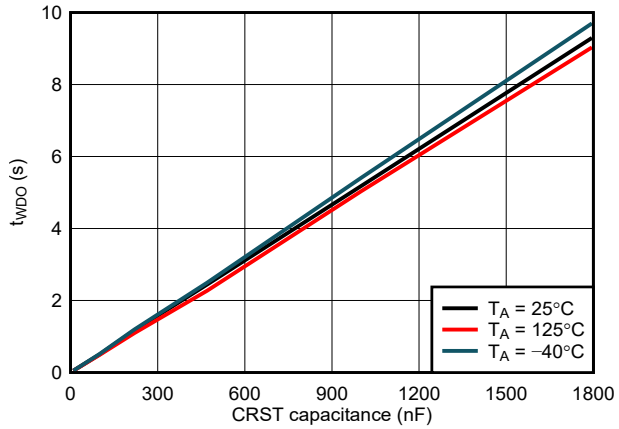


图 7-5. t_{WDO} vs Capacitance

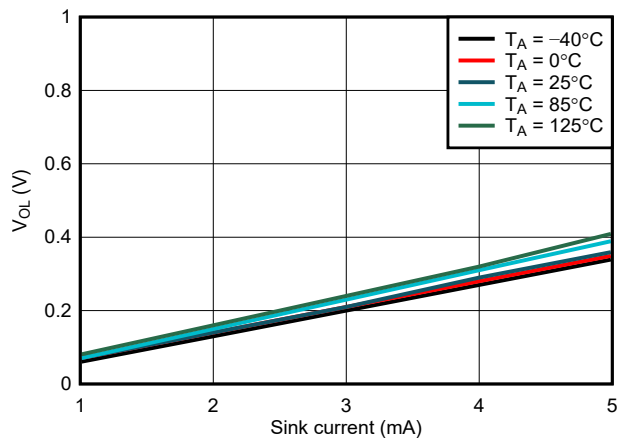


图 7-6. WDO V_{OL} vs I_{sink}, V_{DD} = 1.5 V

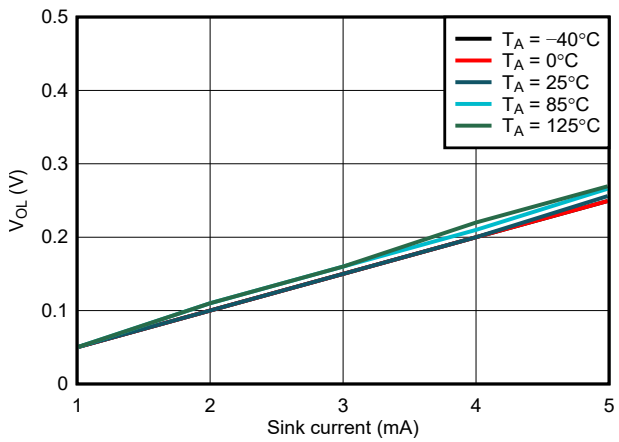


图 7-7. WDO V_{OL} vs I_{sink}, V_{DD} = 3.3 V

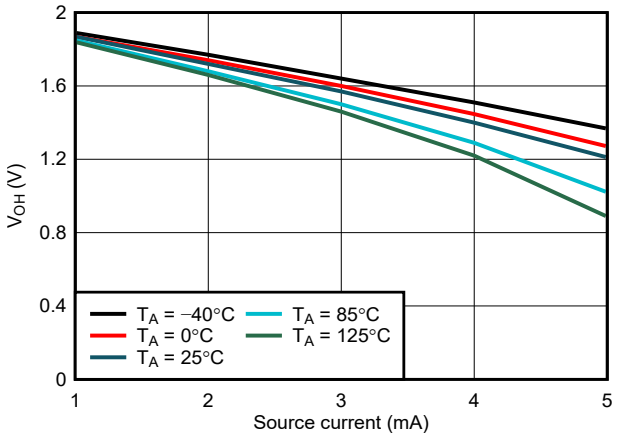


图 7-8. WDO V_{OH} vs I_{source}, V_{DD} = 2.0 V

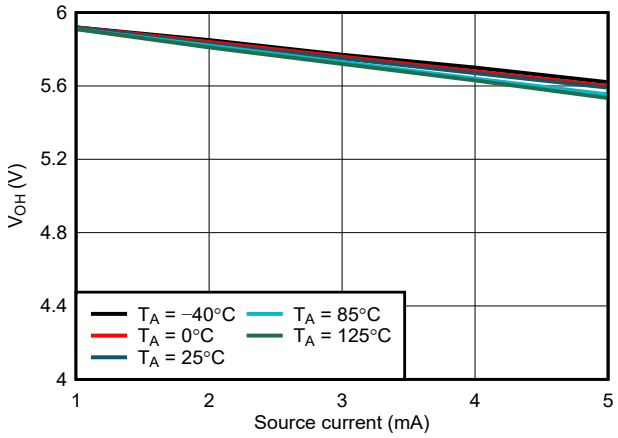


图 7-9. WDO V_{OH} vs I_{source}, V_{DD} = 6.0 V

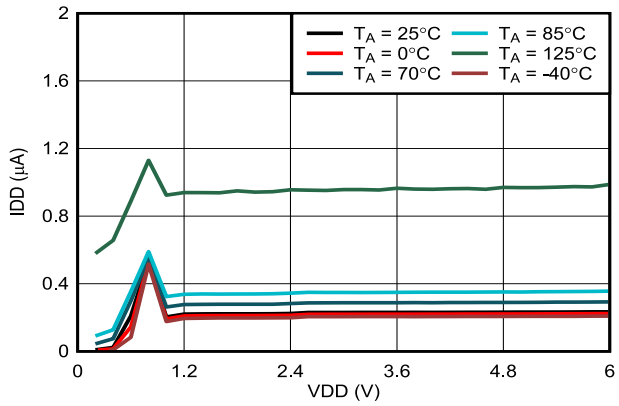


图 7-10. Supply Current vs Power-Supply Voltage

8 详细说明

8.1 Overview

The TPS3435 is a high-accuracy timeout watchdog timer device. The device family supports multiple features related to watchdog operation in a compact 6 pin WSON and 8 pin SOT23 package. The devices are available in 5 different pinout configurations. Each pinout offers access to different features to meet the various application requirements.

8.2 Functional Block Diagrams

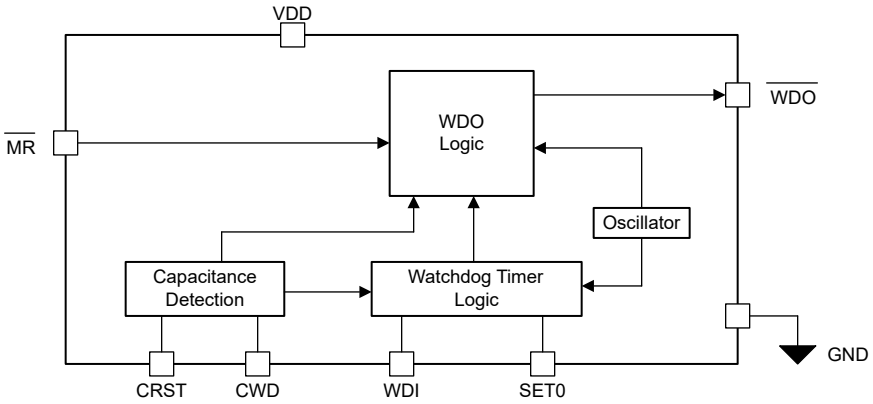


图 8-1. Pinout Option A

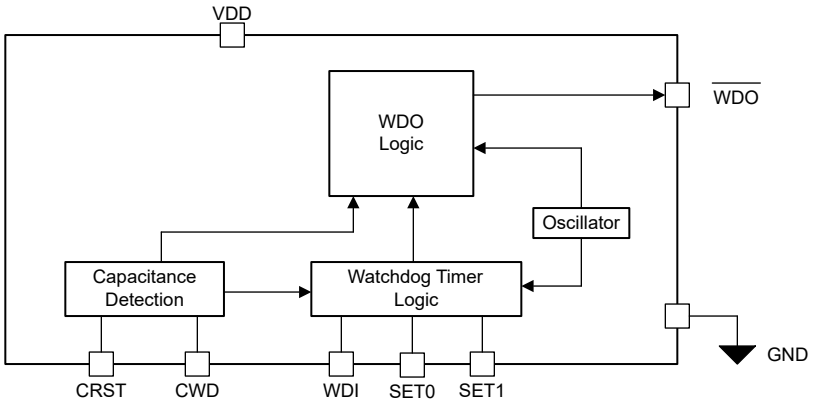


图 8-2. Pinout Option B

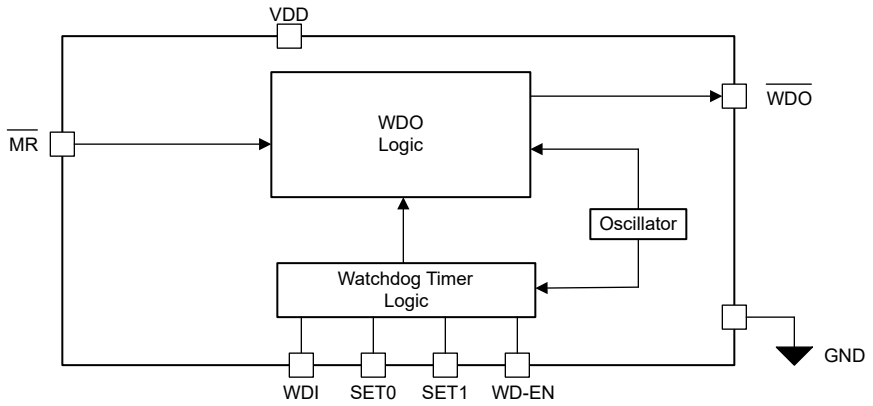


图 8-3. Pinout Option C

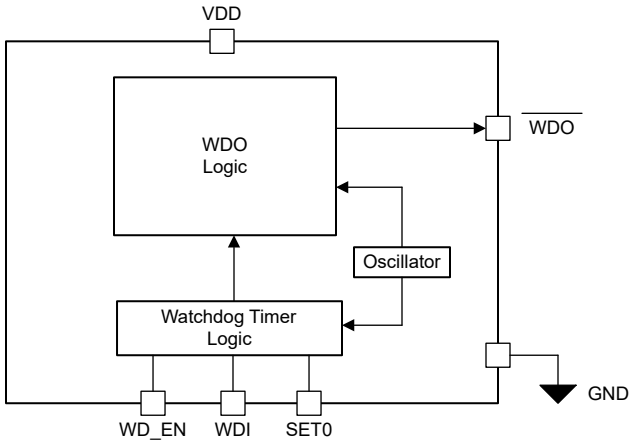


图 8-4. Pinout Option J

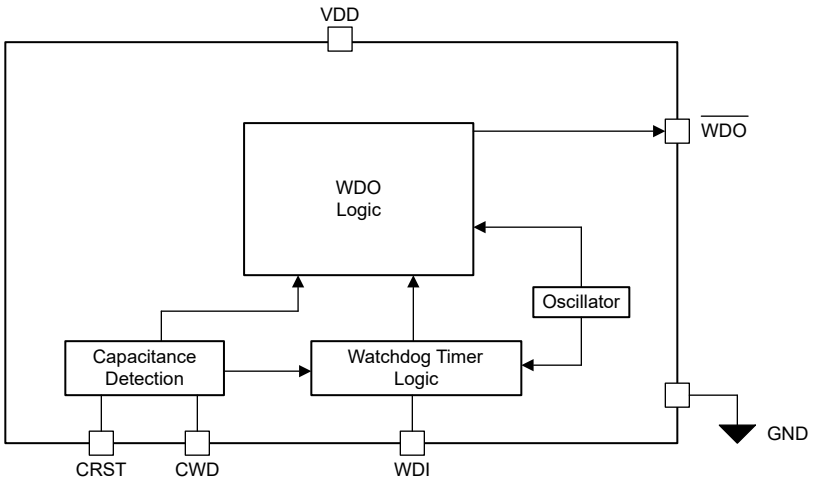


图 8-5. Pinout Option K

8.3 Feature Description

8.3.1 Timeout Watchdog Timer

The TPS3435 offers high precision timeout watchdog timer monitoring. The device is available in multiple pinout options A to K which support multiple features to meet ever expanding needs of various applications. Ensure a correct pinout is selected to meet the application needs.

The timeout watchdog is active when the VDD voltage is higher than the VDD_{MIN}, $\overline{MR}$ voltage is held higher than 0.7 x VDD and watchdog is enabled. TPS3435 family offers various startup time delay options to ensure enough time is available for the host to complete boot operation. Please refer *节 8.3.1.3* for additional details.

The timeout watchdog timer monitors the WDI pin for falling edge in the time frame defined by t_{WD} time period. Refer *节 8.3.1.1* section to arrive at the relevant t_{WD} value needed for application. The timer value is reset when a valid falling edge is detected on WDI pin in the t_{WD} time duration. When a valid WDI transition is not detected in t_{WD} time, the device asserts WDO output. The WDO is asserted for time t_{WDO}. Refer *节 8.3.3* to arrive at the relevant t_{WDO} value needed for application.

图 8-6 shows the basic operation for timeout watchdog timer operation. The TPS3435 watchdog functionality supports multiple features. Details are available in following sub sections.

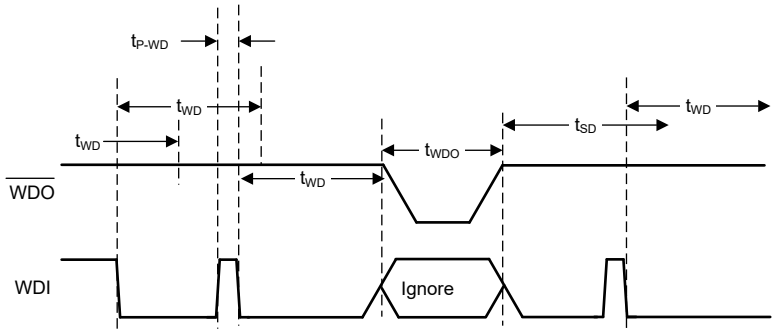


图 8-6. Timeout Watchdog Timer Operation

8.3.1.1 t_{WD} Timer

The t_{WD} timer for TPS3435 can be set using an external capacitor connected between CWD pin and GND pin. This feature is available with pinout options A or B or K. Applications which are space constrained or need timer values which meet offered timer options, can benefit when using pinout options C or J. The TPS3435 offers multiple fixed timer options ranging from 1 msec up-to 100 sec.

The TPS3435, when using capacitance based timer, senses the capacitance value during the power up. The capacitor is charged and discharged with known internal current source for one cycle to sense the capacitance value. The sensed value is used to arrive at t_{WD} timer for the watchdog operation. This unique implementation helps reduce the continuous charge and discharge current for the capacitor, thus reducing overall current consumption. Continuous charge and discharge of capacitance creates wider dead time (no watchdog monitor functionality) when capacitor is discharging. The dead time is higher for high value of capacitance. The unique implementation of TPS3435 helps avoid the dead time as the capacitance is not continuously charging or discharging under normal operation. Ensure C_{CWD} is < 200 x C_{CRST} for accurate calibration of capacitance. 方程式 1 highlights the relationship between t_{WD} in second and CWD capacitance in farad. The t_{WD} timer is 20% accurate for an ideal capacitor. Accuracy of the capacitance will have additional impact on the t_{WD} time. Ensure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

$$t_{WD}\ (\text{sec}) = 4.95 \times 10^{6} \times C_{CWD}\ (\text{F}) \quad (1)$$

The TPS3435 also offers wide selection of high accuracy fixed timer options starting from 1 msec to 100 sec including various industry standard values. The TPS3435 fixed time options are ±10% accurate for $t_{WD} \geqslant 10$ msec. For t_{WD} < 10 msec, the accuracy is ±20%. t_{WD} value relevant to application can be identified from the orderable part number. Refer 节 5 section to identify mapping of orderable part number to t_{WD} value.

The TPS3435 offers flexibility to change the t_{WD} value on the fly by controlling the logic levels on the SETx pins. 节 8.3.1.4 section explains the advantages offered by this feature and the device behavior with various SETx pin combinations.

8.3.1.2 Watchdog Enable Disable Operation

The TPS3435 supports watchdog enable or disable functionality. This functionality is critical for different use cases as listed below.

- Disable watchdog during firmware update to avoid host RESET.
- Disable watchdog during software step-by-step debug operation.
- Disable watchdog when performing critical task to avoid watchdog error interrupt.
- Keep watchdog disabled until host boots up.

The TPS3435 supports watchdog enable or disable functionality through either WD-EN pin or SET[1:0] = 0b'01 logic combination or by keeping WDI pin in the floating state. For a given pinout only one of these three methods is available for the user to disable watchdog operation.

For a pinout which offers a WD-EN pin, the watchdog enable disable functionality is controlled by the logic state of WD-EN pin. Drive WD-EN = 1 to enable the watchdog operation or drive WD-EN = 0 to disable the watchdog operation. The WD-EN pin can be toggled any time during the device operation. The 图 8-7 diagram shows timing behavior with WD-EN pin control.

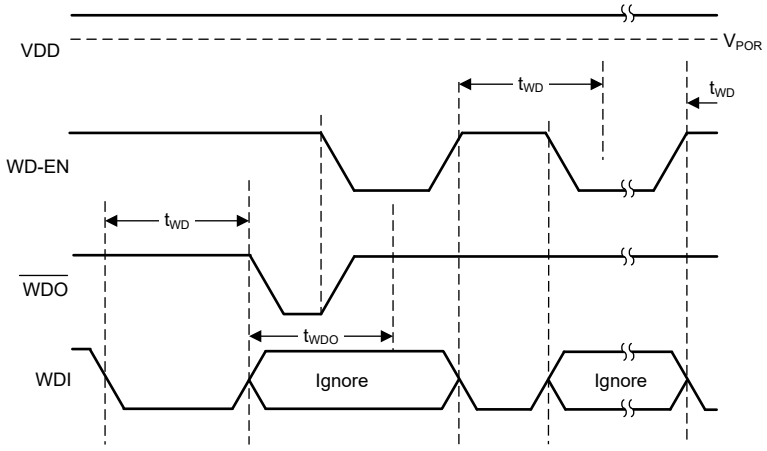


图 8-7. Watchdog Enable: WD-EN Pin Control

SET[1:0] = 0b'01 combination can be used to disable watchdog operation with a pinout which offers SET1 and SET0 pins, but does not include WD-EN pin. The SET pin logic states can be changed at any time during watchdog operation. Refer 节 *8.3.1.4* section for additional details regarding SET[1:0] pin behavior.

A pinout which does not offer WD-EN or SET[1:0] pins uses WDI float pin status to disable the watchdog operation. Users can float the WDI pin during normal operation to disable the watchdog. To enable watchdog, drive the WDI pin and apply a valid edge to trigger the watchdog. It is recommended to drive HIGH and then LOW when exiting the WDI float state.

Pinout options A, B, K offer watchdog timer control using a capacitance connected between CWD and GND pin. A capacitance value higher than recommended or connect to GND leads to watchdog functionality getting disabled. Note, capacitance value is detected and latched during start-up or after an error event. Changing capacitance on the fly does not enable or disable watchdog operation. A power supply recycle is needed to detect change in capacitance.

When watchdog is disabled the ongoing frame will be terminated and WDO will stay deasserted. When enabled the device will immediately enter t_{WD} frame and start watchdog monitoring operation.

8.3.1.3 t_{SD} Watchdog Start Up Delay

The TPS3435 supports watchdog startup delay feature. This feature is activated after power up or after WDO assert event. When t_{SD} frame is active, the device monitors the WDI pin but the WDO output is not asserted. This feature allows time for the host complete boot process before watchdog monitoring can take over. The start up delay helps avoid unexpected WDO assert events during boot. The t_{SD} time is predetermined based on the device part number selected. Refer 节 *5* section for details to map the part number to t_{SD} time. Pinout option A, B, K are available only in no delay or 10 sec start up delay options.

The t_{SD} frame is complete when the time duration selected for t_{SD} is over or host provides a valid transition on the WDI pin. The host must provide a valid transition on the WDI pin during t_{SD} time. The device exits the t_{SD} frame and enters watchdog monitoring phase after valid WDI transition. Failure to provide valid transition on WDI pin triggers the watchdog error by asserting the WDO output pin.

The t_{SD} frame is not initiated when the watchdog functionality is enabled using WD-EN pin or SET[1:0] pin or WDI float functionality as described in 节 *8.3.1.2* section.

图 8-8 diagram shows the operation for t_{SD} time frame.

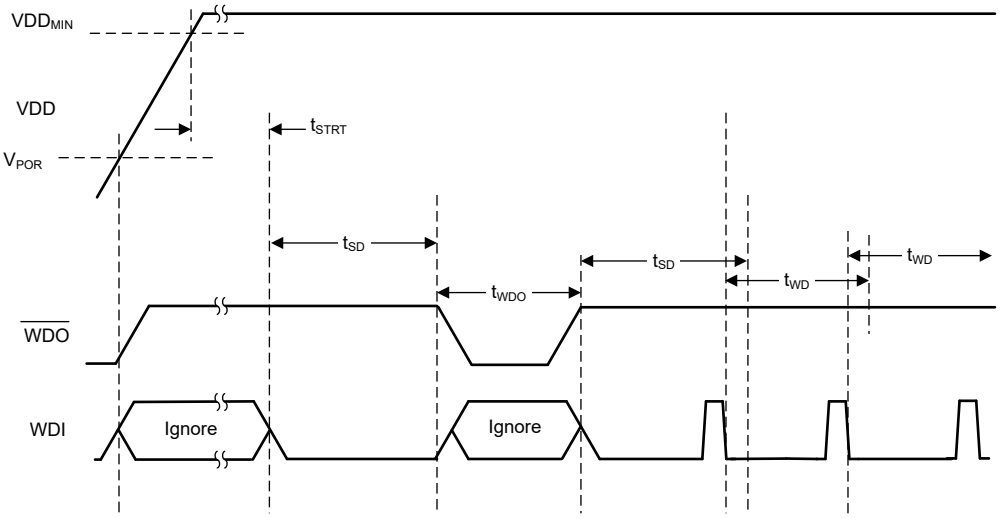


图 8-8. t_{SD} Frame Behavior

8.3.1.4 SET Pin Behavior

The TPS3435 offers one or two SET pins based on the pinout option selected. SET pins offer flexibility to the user to program the t_{WD} timer on the fly to meet various application requirements. Typical use cases where SET pin can be used are:

- Use wide timeout timer when host is in sleep mode, change to small timeout operation when host is operational. Watchdog can be used to wake up the host after long duration to perform the application related activities before going back to sleep.
- Change to wide timeout timer when performing system critical tasks to make sure the watchdog does not interrupt the critical task. Change timer to application specified interval after the critical task is complete.

The t_{WD} timer value for the device is combination of timer selection based on the CWD pin or fixed timer value along with SET pin logic level. The base t_{WD} timer value is decided based on the Watchdog Time selector in the *节 5* section. The SET pin logic level is decoded during the device power up. The SET pin value can be changed any time during the operation. SETx pin change which leads to change of watchdog timer value or enable disable state, terminates the ongoing watchdog frame immediately. SETx pins can be updated when WDO output is asserted as well. The updated t_{WD} timer value will be applied after output is deasserted and the t_{SD} timer is over or terminated.

For a pinout which offers only SET0 pin to the user, the t_{WD} multiplier value is decided based on the Watchdog Time Scaling selector in the *节 5* section. 表 8-1 showcases an example of the t_{WD} values for different SET0 logic levels when using Watchdog Time setting as option D = 10 msec.

表 8-1. t_{WD} Scaling with SET0 Pin Only

WATCHDOG TIME SCALING SELECTION	t_{WD}	
	SET0 = 0	SET0 = 1
A	10 msec	20 msec
B	10 msec	40 msec
C	10 msec	80 msec
D	10 msec	160 msec
E	10 msec	320 msec
F	10 msec	640 msec
G	10 msec	1280 msec

For pinouts which offer both SET0 & SET1 pins to the user, the t_{WD} multiplier value is decided based on the Watchdog Time Scaling selector in the *节 5* section. Two SETx pins offer 3 different time scaling options. The

SET[1:0] = 0b'01 combination disables the watchdog operation. 表 8-2 showcases an example of the t_{WD} values for different SET[1:0] logic levels when using Watchdog Time setting as option G = 100 msec. The package pin out selected does not offer WD-EN pin.

表 8-2. t_{WD} Scaling with SET0 & SET1 Pins, WD-EN Pin Not Available

WATCHDOG TIME SCALING SELECTION	t_{WD}			
	SET[1:0] = 0b'00	SET[1:0] = 0b'01	SET[1:0] = 0b'10	SET[1:0] = 0b'11
A	100 msec	Watchdog disable	200 msec	400 msec
B	100 msec	Watchdog disable	400 msec	800 msec
C	100 msec	Watchdog disable	800 msec	1600 msec
D	100 msec	Watchdog disable	1600 msec	3200 msec
E	100 msec	Watchdog disable	3200 msec	6400 msec
F	100 msec	Watchdog disable	6400 msec	12800 msec
G	100 msec	Watchdog disable	12800 msec	25600 msec

Selected pinout option can offer WD-EN pin along with SET[1:0] pins. With this pinout, the WD-EN pin controls watchdog enable and disable operation. The SET[1:0] = 0b'01 combination operates as SET[1:0] = 0b'00.

Make sure the t_{WD} value with SETx multiplier does not exceed 640 sec. If a selection of timer and multiplier results in t_{WD} > 640 sec, the timer value will be restricted to 640 sec.

图 8-9 to 图 8-11 diagrams show the timing behavior with respect to SETx status changes.

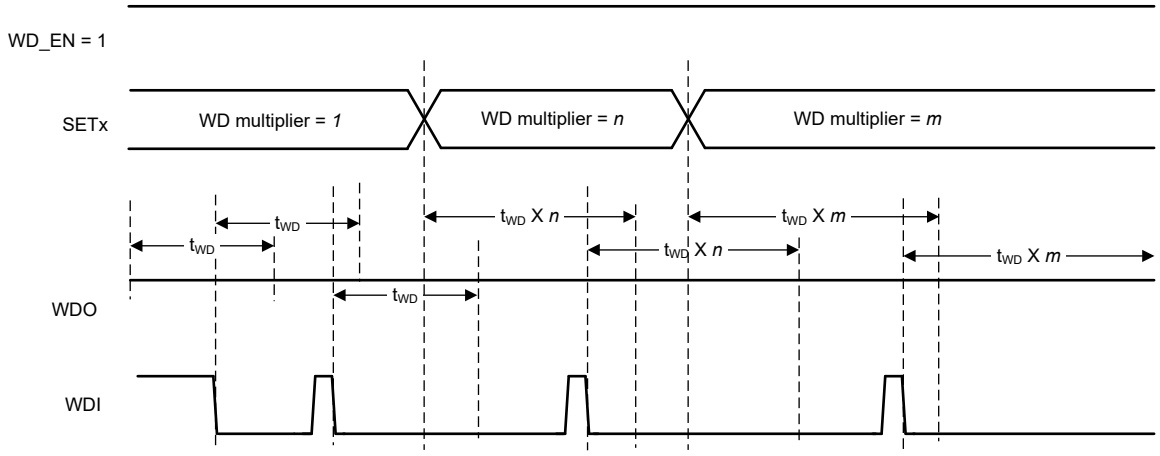


图 8-9. Watchdog Behavior with SETx Pin Status

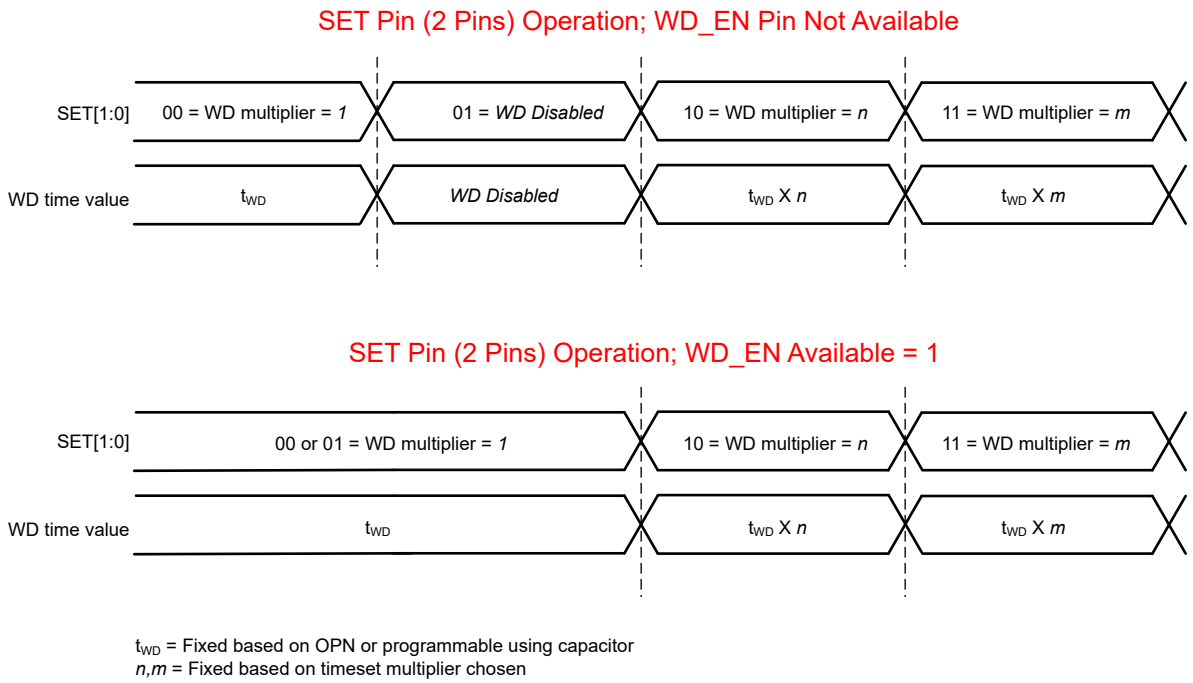


图 8-10. Watchdog Operation with 2 SET Pins

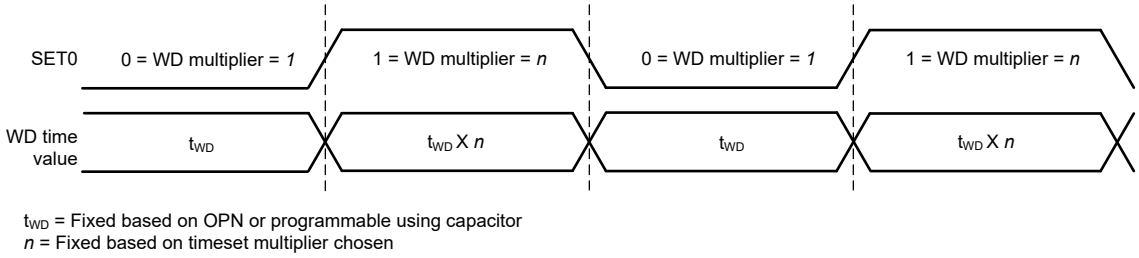


图 8-11. Watchdog Operation with 1 SET Pin

8.3.2 Manual RESET

The TPS3435 supports manual reset functionality using $\overline{MR}$ pin. $\overline{MR}$ pin when driven with voltage lower than 0.3 x VDD, asserts the WDO output. The $\overline{MR}$ pin has 100 kΩ pull up to VDD. The $\overline{MR}$ pin can be left floating. The internal pull up will ensure the output is not asserted due to $\overline{MR}$ pin trigger.

The output is deasserted after $\overline{MR}$ pin voltage rises above 0.7 x VDD voltage. Refer 图 8-12 for more details.

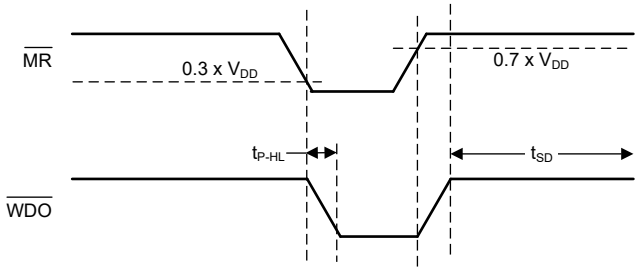


图 8-12. $\overline{MR}$ Pin Response

8.3.3 WDO Output

The TPS3435 device offers WDO output pin. WDO output is asserted when $\overline{MR}$ pin voltage is lower than 0.3 X VDD or watchdog timer error is detected.

The output will be asserted for t_{WDO} time when any relevant events described above are detected, except for $\overline{MR}$ event. The time t_{WDO} can be programmed by connecting a capacitor between CRST pin and GND or device will assert t_{WDO} for fixed time duration as selected by orderable part number. Refer 节 5 section for all available options.

方程式 2 describes the relationship between capacitor value and the time t_{WDO}. Ensure the capacitance meets the recommended operating range. Capacitance outside the recommended range can lead to incorrect operation of the device.

$$t_{WDO}\ (sec) = 4.95 \times 10^{6} \times C_{CRST}\ (F) \quad (2)$$

TPS3435 also offers a unique option of latched output. An orderable with latched output will hold the output in asserted state indefinitely until the device is power cycled or the error condition is addressed. If the output is latched due to $\overline{MR}$ pin low voltage, the output latch will be released when $\overline{MR}$ pin voltage rises above 0.7 x V_{DD} level. If the output is latched due to watchdog timer error, the output latch will be released when a WDI negative edge is detected or the device is shutdown and powered up again.

8.4 Device Functional Modes

表 8-3 summarizes the functional modes of the TPS3435.

表 8-3. Device Functional Modes

VDD	Watchdog Status	WDI	$\overline{WDO}$
$V_{DD} < V_{POR}$	Not Applicable	—	Undefined
$V_{POR} \leqslant V_{DD} < V_{DDmin}$	Not Applicable	Ignored	High
$V_{DD} \geqslant V_{DDmin}$	Disabled	Ignored	High
	Enabled	t_{pulse} (1) < $t_{WD(min)}$	High
	Enabled	t_{pulse} (1) > $t_{WD(max)}$	Low

(1) Where t_{pulse} is the time between falling edges on WDI.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

9.1.1 Output Assert Delay

The TPS3435 features two options for setting the output assert delay (t_{WDO}): using a fixed timing and programming the timing through an external capacitor.

9.1.1.1 Factory-Programmed Output Assert Delay Timing

Fixed output assert delay timings are available using pinout C and J. Using these timings enables a high-precision, 10% accurate output assert delay timing.

9.1.1.2 Adjustable Capacitor Timing

The TPS3435 also utilizes a programmable output assert delay, using a precision current source to charge an external capacitor upon device startup. By monitoring the voltage on the CRST pin, the TPS3435 can be programmed to have a desired output assert delay. The typical delay time resulting from a given external capacitance on the CRST pin can be calculated by 方程式 3, where t_{WDO} is the output assert delay time in seconds and C_{CRST} is the capacitance in microfarads.

$$t_{WDO}\ (sec) = 4.95 \times 10^{6} \times C_{CRST}\ (F) \quad (3)$$

Note that in order to minimize the difference between the calculated output assert delay time and the actual output assert delay time, use a high-quality ceramic dielectric COG, X5R, or X7R capacitor and minimize parasitic board capacitance around this pin. 表 9-1 lists the output assert delay time ideal capacitor values for C_{CRST}.

表 9-1. Output Assert Delay Time for Common Ideal Capacitor Values

C_{CRST}	OUTPUT ASSERT DELAY TIME (t_{WDO})			UNIT
	MIN(1)	TYP	MAX(1)	
10 nF	39.6	49.5	59.4	ms
100 nF	396	495	594	ms
1 µF	3960	4950	5940	ms

(1) Minimum and maximum values are calculated using ideal capacitors.

9.1.2 Watchdog Timer Functionality

The TPS3435 features two options for setting the watchdog timer (t_{WD}): using a fixed timing and programming the timing through an external capacitor.

9.1.2.1 Factory-Programmed Timing Options

Fixed watchdog timeout options are available using pinout C and J. Using these timings enables a high-precision, 10% accurate watchdog timer t_{WD}.

9.1.2.2 Adjustable Capacitor Timing

Adjustable t_{WD} timing is achievable by connecting a capacitor to the CWD pin. If this method is used, please consult 方程式 1 for calculating typical t_{WD} values using ideal capacitors. Capacitor tolerances cause the actual device timing to vary such that the minimum of t_{WD} can decrease and the maximum of t_{WD} can increase by the capacitor tolerance. For the most accurate timing, use ceramic capacitors with COG dielectric material.

9.2 Typical Applications

9.2.1 Design 1: Monitoring a Standard Microcontroller for Timeouts

This example application uses the TPS3435CDDBBDDFR to monitor a microcontroller to ensure it is not stalled during operation.

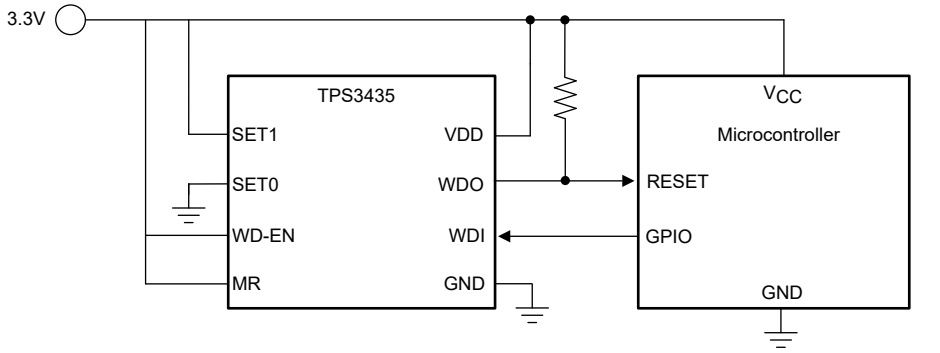


图 9-1. Microcontroller Watchdog Monitoring Circuit

9.2.1.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Watchdog Timeout Period	Typical timeout period of 40 ms	Typical timeout period of 40 ms
Watchdog Output Assert Delay	Typical output assert of 2 ms	Typical output assert of 2 ms
Startup Delay	Minimum startup delay of 700 ms	Minimum startup delay of 900 ms
Output logic voltage	Open-drain	Open-drain
Maximum device current consumption	20 µA	250 nA typical, 3.0 µA maximum(1)

(1) Only includes the current consumption of the TPS3435.

9.2.1.2 Detailed Design Procedure

9.2.1.2.1 Setting the Watchdog Timeout Period

The watchdog timeout design requirement can be met either by using a fixed-timeout version of the TPS3435 or by connecting a capacitor between the CWD pin and GND. The typical values can be met with preprogrammed fixed time options, hence a pinout offering fixed time options is selected. Please see the 节 7.6 for a list of fixed timeouts. If using the CWD feature, please refer to 节 8.3.1.1 for instructions on how to program the timout period. In this application example, the 40 ms timeout watchdog period is achieved by using watchdog time of 10ms (option D) and watchdog time scaling of 4 (option B). Connect SET[1:0] = 0b'10 to select watchdog time scaling of 4.

9.2.1.2.2 Setting Output Assert Delay

Please see the 节 7.7 for a list of fixed timeouts. Timeout option B was chosen in order to meet the design requirement for a 2 ms typical timeout.

9.2.1.2.3 Setting the Startup Delay

Startup delay option D is chosen, which offers a startup delay of 1 s. This accounts for the minimum specification of 700 ms.

9.2.1.2.4 Calculating the $\overline{\text{WDO}}$ Pullup Resistor

The TPS3435 uses an open-drain configuration for the $\overline{\text{WDO}}$ output, as shown in 图 9-2. When the FET is off, the resistor pulls the drain of the transistor to VDD and when the FET is turned on, the FET pulls the output to ground, thus creating an effective resistor divider. The resistors in this divider must be chosen to ensure that V_{OL} is below its maximum value. To choose the proper pullup resistor, there are three key specifications to keep in mind: the pullup voltage (V_{PU}), the recommended maximum $\overline{\text{WDO}}$ pin current (I_{Sink}), and V_{OL}. The maximum V_{OL} is 0.3 V, meaning that the effective resistor divider created must be able to bring the voltage on the reset pin below 0.3 V with I_{Sink} kept below 2 mA for $V_{DD} \geq 3$ V and 500 μA for V_{DD} = 1.5 V. For this example, with a V_{PU} =V_{DD} = 1.5 V, a resistor must be chosen to keep I_{Sink} below 500 μA because this value is the maximum consumption current allowed. To ensure this specification is met, a pullup resistor value of 10 kΩ was selected, which sinks a maximum of 150 μA when $\overline{\text{WDO}}$ is asserted.

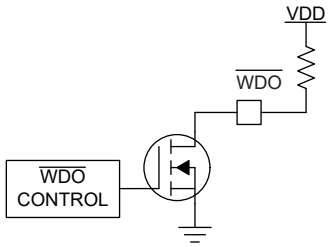


图 9-2. Open-Drain $\overline{\text{WDO}}$ Configuration

9.2.1.3 Application Curves

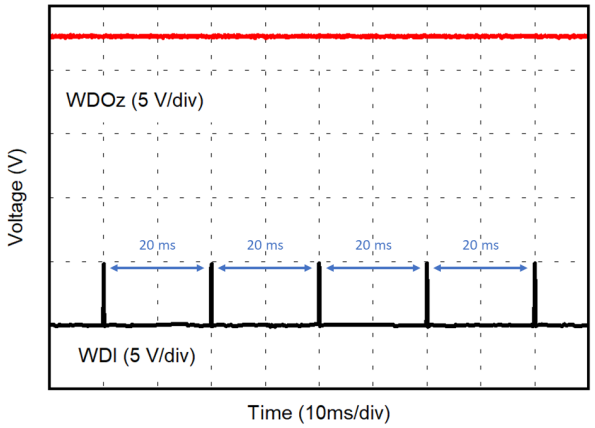


图 9-3. Typical WDI Pulse

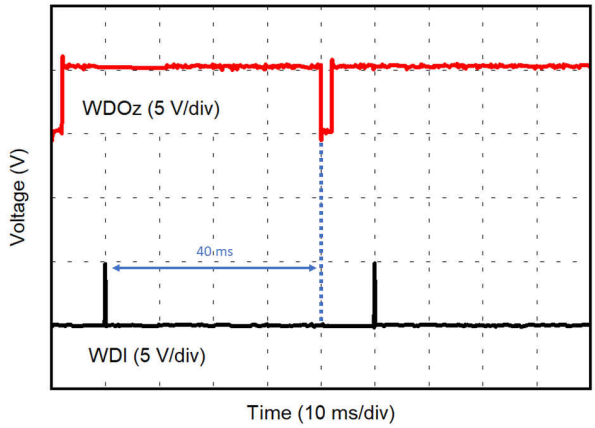


图 9-4. Watchdog Timeout Fault

10 Power Supply Recommendations

This device is designed to operate from an input supply with a voltage range between 1.04 V and 6.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1-μF capacitor between the VDD pin and the GND pin.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a 0.1-µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CRST pin, then minimize parasitic capacitance on this pin so the $\overline{WDO}$ delay time is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1-µF ceramic capacitor as near as possible to the VDD pin.
- Place C_{CRST} capacitor as close as possible to the CRST pin.
- Place C_{CWD} capacitor as close as possible to the CWD pin.
- Place the pullup resistor on the $\overline{WDO}$ pin as close to the pin as possible.

11.2 Layout Example

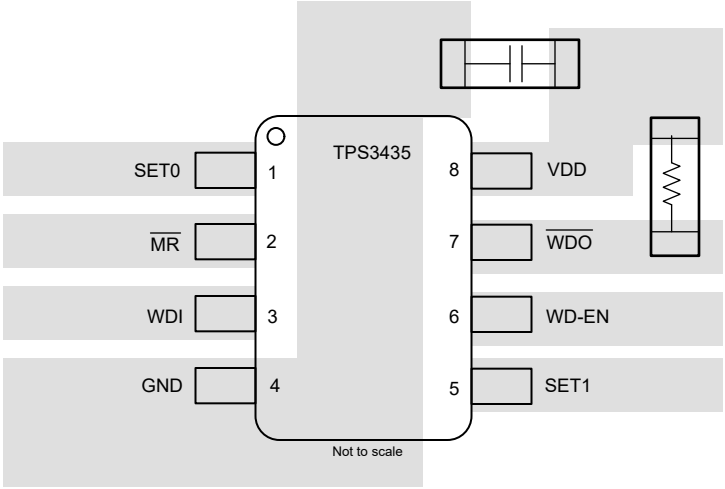


图 11-1. Typical Layout for the TPS3435

12 Device and Documentation Support

12.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3435CAIEGDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		NLHOG	Samples
TPS3435CAKAGDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	NLHOA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3435 :

- Automotive : TPS3435-Q1

NOTE: Qualified Version Definitions:

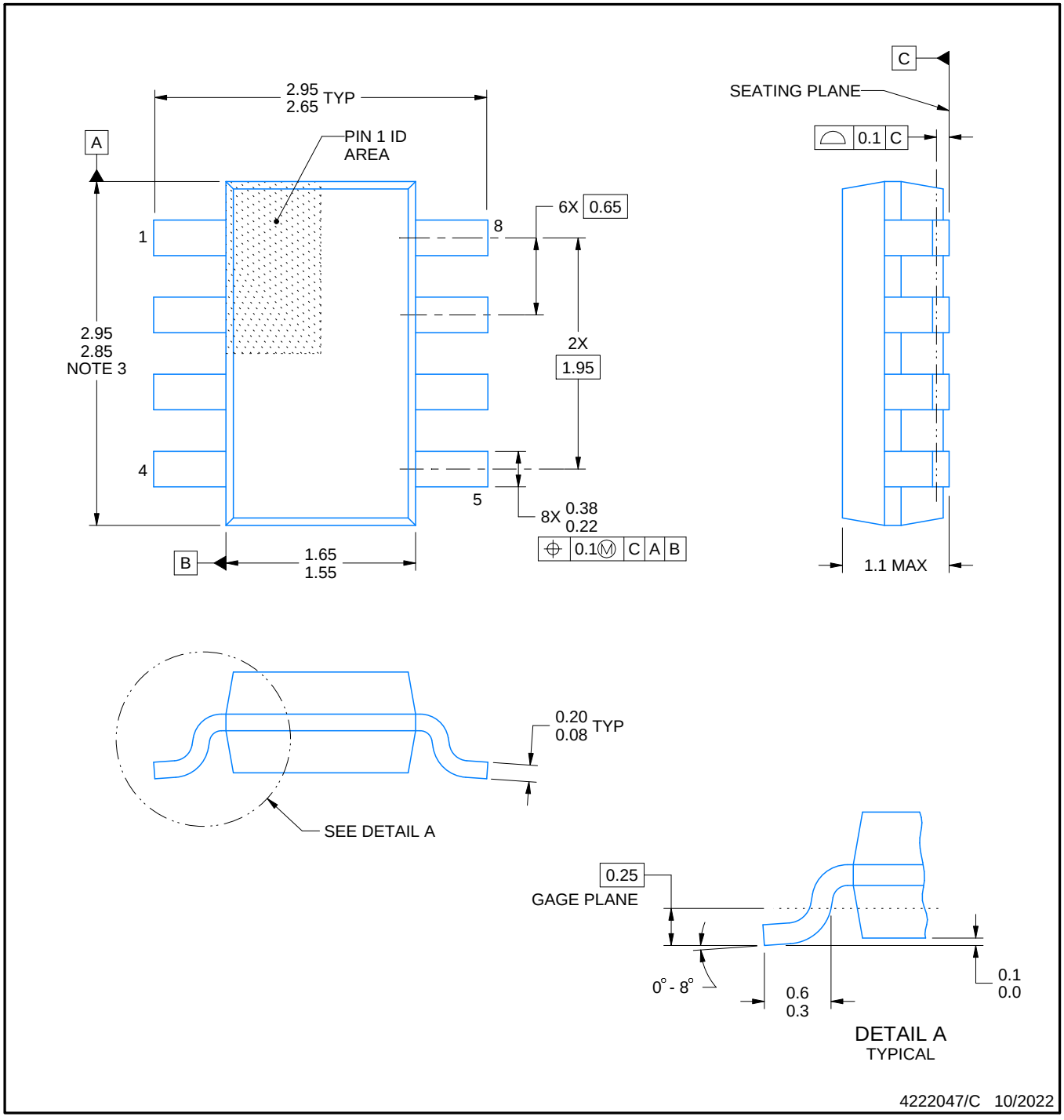
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

PACKAGE OUTLINE

DDF0008A

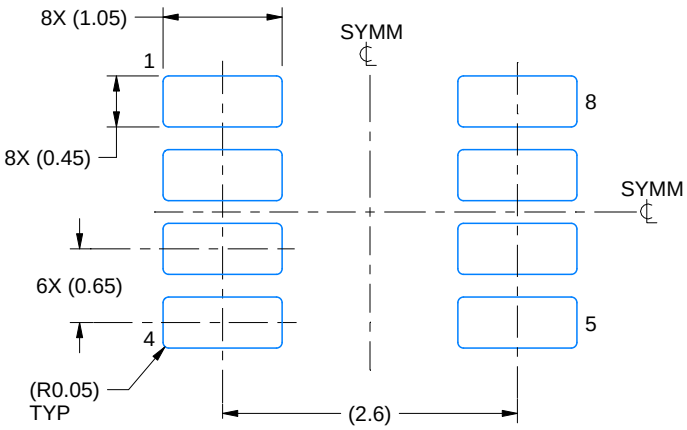
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X

NON SOLDER MASK
DEFINED

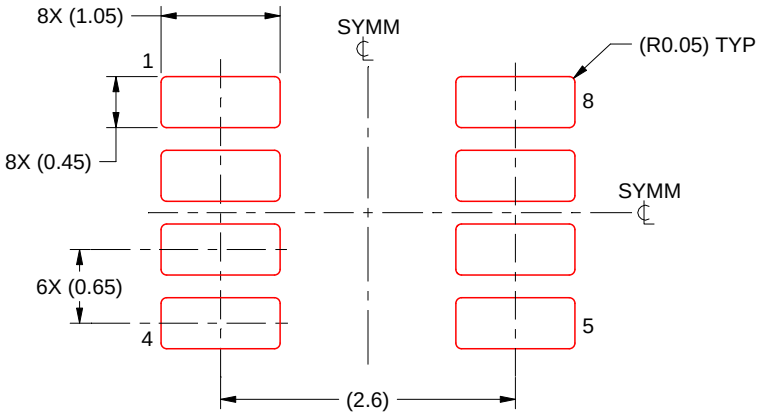
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265