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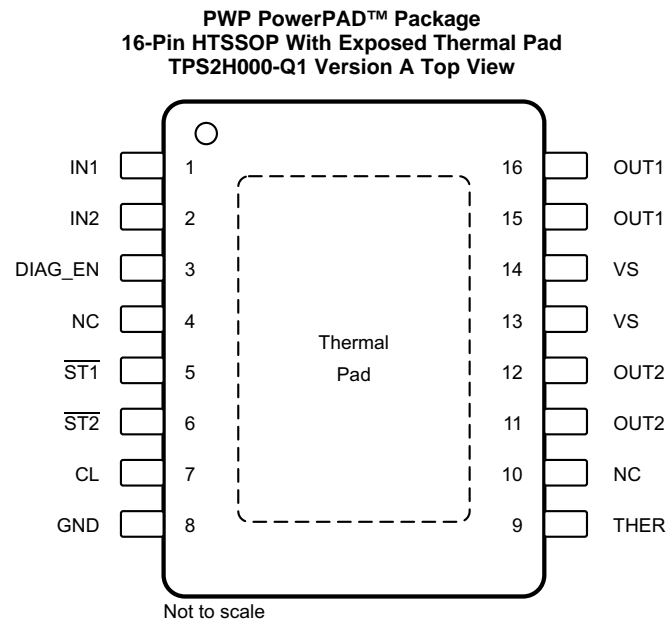
## 4 修订历史记录

<b>Changes from Revision C (July 2019) to Revision D</b> .....	<b>Page</b>
• 向 <a href="#">特性</a> 部分添加了提供功能安全的链接 .....	<b>1</b>
<b>Changes from Revision B (March 2018) to Revision C</b> .....	<b>Page</b>
• Changed the adjustable current limit from 2.5 A to 0.5 A in the <a href="#">Detailed Design Procedure</a> section .....	<b>28</b>
<b>Changes from Revision A (October 2016) to Revision B</b> .....	<b>Page</b>
• Added footnote 2 to the <a href="#">Electrical Characteristics</a> table .....	<b>8</b>
• Added reverse current protection information to the <a href="#">Reverse-Current Protection</a> section .....	<b>24</b>
<b>Changes from Original (December 2015) to Revision A</b> .....	<b>Page</b>
• 已将数据表状态由“产品预览”改为“量产数据” .....	<b>1</b>

## 5 Device Comparison Table

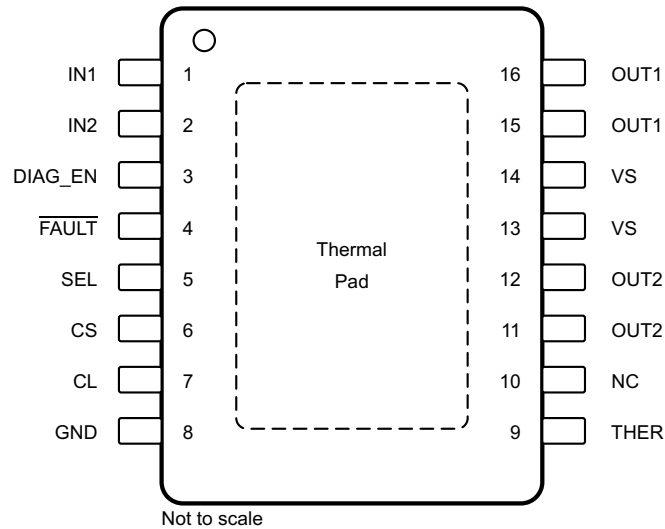
PART NUMBER	FAULT REPORTING MODE
TPS2H000-Q1 Version A	Open-drain digital output
TPS2H000-Q1 Version B	Current-sense analog output

## 6 Pin Configuration and Functions



NC – No internal connection

**PWP PowerPAD Package  
16-Pin HTSSOP With Exposed Thermal Pad  
TPS2H000-Q1 Version B Top View**



NC – No internal connection

**Pin Functions**

PIN			I/O	DESCRIPTION
NAME	NO.			
	VERSION A	VERSION B		
CL	7	7	O	Adjustable current limit. Connect to device GND if external current limit is not used.
CS	—	6	O	Current-sense output
DIAG_EN	3	3	I	Enable-disable pin for diagnostics; internal pulldown
$\overline{\text{FAULT}}$	—	4	O	Global fault report with open-drain structure, ORed logic for dual-channel fault conditions
GND	8	8	—	Ground pin
IN1	1	1	I	Input control for channel 1 activation; internal pulldown
IN2	2	2	I	Input control for channel 2 activation; internal pulldown
NC	4, 10	10	—	No internal connection
$\overline{\text{ST1}}$	5	—	O	Open-drain diagnostic status output for channel 1
$\overline{\text{ST2}}$	6	—	O	Open-drain diagnostic status output for channel 2
SEL	—	5	I	CS channel-selection bit; internal pulldown
THER	9	9	I	Thermal shutdown behavior control, latch off or auto-retry; internal pulldown
OUT1	15, 16	15, 16	O	Output of the channel 1 high side-switch, connected to the load
OUT2	11, 12	11, 12	O	Output of the channel 2 high side-switch, connected to the load
VS	13, 14	13, 14	I	Power supply
Thermal pad	—	—	—	Connect to device GND or leave floating

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) <sup>(1)(2)</sup>

		MIN	MAX	UNIT
Supply voltage	$t < 400 \text{ ms}$		45	V
Reverse polarity voltage <sup>(3)</sup>		–36		V
Current on GND pin	$t < 2 \text{ minutes}$	–100	250	mA
Voltage on INx, DIAG_EN, SEL, and THER pins		–0.3	7	V
Current on INx, DIAG_EN, SEL, and THER pins		–10	—	mA
Voltage on $\overline{\text{STx}}$ or $\overline{\text{FAULT}}$ pins		–0.3	7	V
Current on $\overline{\text{STx}}$ or $\overline{\text{FAULT}}$ pins		–30	10	mA
Voltage on CS pin		–2.7	7	V
Current on CS pin		—	30	mA
Voltage on CL pin		–0.3	7	V
Current on CL pin		—	6	mA
Inductive load switch-off energy dissipation, single pulse, single channel <sup>(4)</sup>		—	40	mJ
Operating junction temperature, $T_J$		–40	150	°C
Storage temperature, $T_{\text{stg}}$		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to the ground plane.
- (3) Reverse polarity condition:  $t < 60 \text{ s}$ , reverse current  $< I_{R(2)}$ ,  $V_{\text{INx}} = 0 \text{ V}$ , all channels reverse, GND pin 1-k $\Omega$  resistor in parallel with diode.
- (4) Test condition:  $V_{\text{VS}} = 13.5 \text{ V}$ ,  $L = 300 \text{ mH}$ ,  $T_J = 150^\circ\text{C}$ . FR4 2s2p board,  $2 \times 70\text{-}\mu\text{m Cu}$ ,  $2 \times 35\text{-}\mu\text{m Cu}$ . 600 mm<sup>2</sup> thermal pad copper area.

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{\text{(ESD)}}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	All pins	$\pm 4000$	V
	Charged-device model (CDM), per AEC Q100-011	All pins	$\pm 750$	
		Corner pins (1, 8, 9, and 16)	$\pm 750$	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{\text{VS}}$	Supply operating voltage	4	40	V
	Voltage on INx, DIAG_EN, SEL, and THER pins	0	5	V
	Voltage on $\overline{\text{STx}}$ and $\overline{\text{FAULT}}$ pins	0	5	V
	Nominal dc load current	0	0.75	A
$T_A$	Operating ambient temperature	–40	125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TPS2H000-Q1	UNIT
	PWP (HTSSOP)	
	16 PINS	
$R_{\theta\text{JA}}$ Junction-to-ambient thermal resistance	39.1	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## Thermal Information (continued)

THERMAL METRIC <sup>(1)</sup>		TPS2H000-Q1	UNIT
		PWP (HTSSOP)	
		16 PINS	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.9	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	22.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

## 7.5 Electrical Characteristics

5 V <  $V_{VS}$  < 40 V; -40°C <  $T_J$  < 150°C, unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OPERATING VOLTAGE</b>					
$V_{VS(nom)}$	Nominal operating voltage	4		40	V
$V_{VS(uvr)}$	Undervoltage turnon	3.5	3.7	4	V
$V_{VS(uvf)}$	Undervoltage shutdown	3	3.2	3.4	V
$V_{(uv,hys)}$	Undervoltage shutdown, hysteresis		0.5		V

## Electrical Characteristics (continued)

5 V < V<sub>VS</sub> < 40 V; -40°C < T<sub>J</sub> < 150°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I <sub>(op)</sub>	Nominal operating current <sup>(1)</sup>	V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = 5 V, V <sub>DIAG_EN</sub> = 0 V, I <sub>OUTx</sub> = 0.1 A, current limit = 0.5 A, all channels on			7	mA
I <sub>(off)</sub>	Standby current	V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = V <sub>DIAG_EN</sub> = V <sub>CS</sub> = V <sub>CL</sub> = V <sub>OUTx</sub> = THER = 0 V, T <sub>J</sub> = 25°C			0.5	μA
		V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = V <sub>DIAG_EN</sub> = V <sub>CS</sub> = V <sub>CL</sub> = V <sub>OUTx</sub> = THER = 0 V, T <sub>J</sub> = 125°C			3	
I <sub>(off,diag)</sub>	Standby current with diagnostic enabled	V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = 0 V, V <sub>DIAG_EN</sub> = 5 V, V <sub>VS</sub> – V <sub>OUTx</sub> > V <sub>(ol,off)</sub> , not in open-load mode			3	mA
t <sub>(off,diag)</sub>	Standby mode deglitch time <sup>(1)</sup>	IN from high to low, if deglitch time > t <sub>(off,deg)</sub> , the device enters into standby mode.	10	12.5	15	ms
I <sub>kg(out)</sub>	Output leakage current in off-state	V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = V <sub>OUTx</sub> = 0, V <sub>DIAG_EN</sub> = 5 V			2	μA
POWER STAGE						
r <sub>DS(on)</sub>	On-state resistance <sup>(1)</sup>	V <sub>VS</sub> ≥ 3.5 V, T <sub>J</sub> = 25°C		1000		mΩ
		V <sub>VS</sub> ≥ 3.5 V, T <sub>J</sub> = 150°C		2000		
I <sub>CL(int)</sub>	Internal current limit	Internal current limit value, CL pin connected to GND	1		1.6	A
I <sub>CL(TSD)</sub>	Current limit during thermal shutdown <sup>(1)</sup>	Internal current limit value under thermal shutdown		0.8		A
		External current limit value under thermal shutdown. The percentage of the external current limit setting value		60%		
V <sub>DS(clamp)</sub>	Drain-to-source internal clamp voltage		46		65	V
OUTPUT DIODE CHARACTERISTICS						
V <sub>F</sub>	Drain–source diode voltage	IN = 0, I <sub>OUTx</sub> = –0.15 A.	0.3	0.8	1	V
I <sub>R(1)</sub> , I <sub>R(2)</sub>	Continuous reverse current from source to drain <sup>(1)</sup>	t < 60 s, V <sub>INx</sub> = 0 V, T <sub>J</sub> = 25°C, single channel reversed, short-to-battery condition		1		A
		t < 60 s, V <sub>INx</sub> = 0 V, GND pin 1-kΩ resistor in parallel with diode. T <sub>J</sub> = 25°C. Reverse-polarity condition, all channels reversed		1		
LOGIC INPUT (INx, DIAG_EN, SEL, THER)						
V <sub>IH</sub>	Logic high-level voltage		2			V
V <sub>IL</sub>	Logic low-level voltage				0.8	V
R <sub>(logic,pd)</sub>	Logic-pin pulldown resistor	INx, SEL, THER, V <sub>INx</sub> = V <sub>SEL</sub> = V <sub>THER</sub> = 5 V	100	175	250	kΩ
		DIAG_EN. V <sub>VS</sub> = V <sub>DIAG_EN</sub> = 5 V	150	275	400	
DIAGNOSTICS						
I <sub>kg(GND_loss)</sub>	Output leakage current under GND loss condition				100	μA
V <sub>(ol,off)</sub>	Open-load detection threshold	IN = 0 V, when V <sub>VS</sub> – V <sub>OUTx</sub> < V <sub>(ol,off)</sub> , duration longer than t <sub>(ol,off)</sub> , then open load is detected, off state	1.6		2.6	V
t <sub>d(ol,off)</sub>	Open-load detection threshold deglitch time (see Figure 3)	IN = 0 V, when V <sub>VS</sub> – V <sub>OUTx</sub> < V <sub>(ol,off)</sub> , duration longer than t <sub>(ol,off)</sub> , then open load is detected, off state	300	600	800	μs
I <sub>(ol,off)</sub>	Off-state output sink current	V <sub>INx</sub> = 0 V, V <sub>DIAG_EN</sub> = 5 V, V <sub>VS</sub> = V <sub>OUTx</sub> = 13.5 V, T <sub>J</sub> = 125°C, open load	–75			μA
V <sub>OL(STx)</sub>	Status low-output voltage	I <sub>STx</sub> = 2 mA, version A only			0.2	V
V <sub>OL(FAULT)</sub>	Fault low-output voltage	I <sub>FAULT</sub> = 2 mA, version B only			0.2	V
t <sub>CL(deg)</sub>	Deglitch time when current limit occurs <sup>(1)</sup>	V <sub>INx</sub> = V <sub>DIAG_EN</sub> = 5 V, the deglitch time from current limit toggling to FAULT, STx, CS report.	80		180	μs
T <sub>(SD)</sub>	Thermal shutdown threshold <sup>(1)</sup>		160	175		°C
T <sub>(SD,rst)</sub>	Thermal shutdown status reset threshold <sup>(1)</sup>			155		°C
T <sub>(SW)</sub>	Thermal swing shutdown threshold <sup>(1)</sup>			60		°C
T <sub>(hys)</sub>	Hysteresis for resetting the thermal shutdown or thermal swing <sup>(1)</sup>			10		°C

(1) Value specified by design, not subject to production test

## Electrical Characteristics (continued)

5 V < V<sub>VS</sub> < 40 V; -40°C < T<sub>J</sub> < 150°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CURRENT SENSE (Version B) AND CURRENT LIMIT</b>						
K <sub>(CS)</sub>	Current-sense ratio			80		
K <sub>(CL)</sub>	Current-limit ratio			300		
V <sub>CL(th)</sub>	Current limit internal threshold <sup>(1)</sup>			0.8		V
dK <sub>(CS)</sub> / K <sub>(CS)</sub>	Current-sense accuracy, (I <sub>CS</sub> × K <sub>(CS)</sub> – I <sub>OUTx</sub> ) / I <sub>OUTx</sub> × 100	V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 1 mA	-50%		50%	
		V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 2 mA	-25%		25%	
		V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 5 mA	-10%		10%	
		V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 25 mA	-3%		3%	
		V <sub>VS</sub> = 13.5 V, I <sub>OUTx</sub> ≥ 100 mA	-2.5%		2.5%	
dK <sub>(CL)</sub> / K <sub>(CL)</sub>	External current limit accuracy <sup>(2)</sup> (I <sub>OUTx</sub> – I <sub>CL</sub> × K <sub>(CL)</sub> ) × 100 / (I <sub>CL</sub> × K <sub>(CL)</sub> )	V <sub>VS</sub> = 13.5 V, I <sub>(limit)</sub> ≥ 50 mA	-25%		25%	
		I <sub>(limit)</sub> ≥ 100 mA	-20%		20%	
		I <sub>(limit)</sub> ≥ 200 mA	-15%		15%	
		V <sub>VS</sub> = 13.5 V, 0.5 A ≤ I <sub>(limit)</sub> ≤ 0.9 A	-10%		10%	
V <sub>CS(lin)</sub>	Current-sense voltage linear range <sup>(1)</sup>	V <sub>VS</sub> ≥ 6.5 V	0		4	V
		5 V ≤ V <sub>VS</sub> < 6.5 V	0		V <sub>VS</sub> – 2.5	
I <sub>OUTx(lin)</sub>	Output-current linear range <sup>(1)</sup>	V <sub>VS</sub> = 13.5 V, V <sub>CS(lin)</sub> ≤ 4 V	0		0.75	A
		5 V ≤ V <sub>VS</sub> < 6.5 V, V <sub>CS(lin)</sub> ≤ V <sub>VS</sub> – 2.5 V	0		0.5	
V <sub>CS(H)</sub>	Current sense pin output voltage <sup>(1)</sup>	V <sub>VS</sub> ≥ 7 V, fault mode	4.5		6.5	V
		5 V ≤ V <sub>VS</sub> < 7 V, fault mode	Min(V <sub>VS</sub> – 2, 4.5)		6.5	V
I <sub>CS(H)</sub>	Current-sense pin output current	V <sub>CS</sub> = 4.5 V, V <sub>VS</sub> = 13.5 V	15			mA
I <sub>lkg(CS)</sub>	Current-sense leakage current in disabled mode	V <sub>DIAG_EN</sub> = 0 V, T <sub>J</sub> = 125°C			0.5	μA

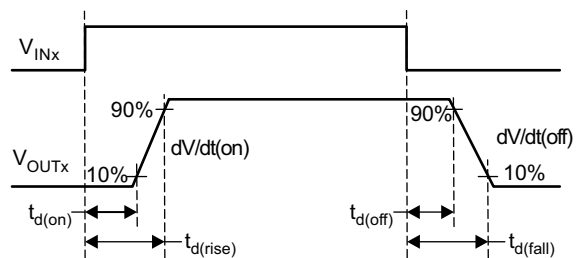
(2) External current limit accuracy is only applicable to overload conditions greater than 1.5 x the current limit setting

## 7.6 Switching Characteristics

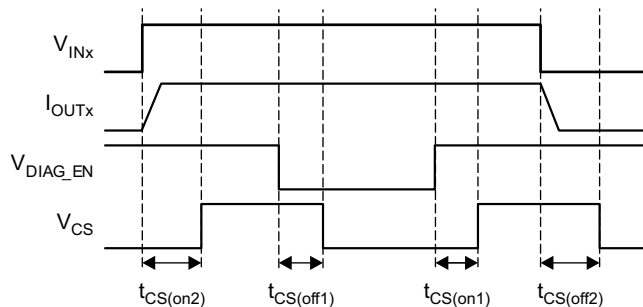
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>d(on)</sub>	Delay time, V <sub>OUTx</sub> 10% after V <sub>INx</sub> ↑ (See Figure 1.)	V <sub>VS</sub> = 13.5 V, V <sub>DIAG_EN</sub> = 5 V, I <sub>OUTx</sub> = 0.1 A, IN rising edge to 10% of V <sub>OUTx</sub>	10	30	60	μs
t <sub>d(off)</sub>	Delay time, V <sub>OUTx</sub> 90% after V <sub>INx</sub> ↓ (See Figure 1.)	V <sub>VS</sub> = 13.5 V, V <sub>DIAG_EN</sub> = 5 V, I <sub>OUTx</sub> = 0.1 A, IN falling edge to 90% of V <sub>OUTx</sub>	10	30	60	μs
dV/dt(on)	Turnon slew rate	V <sub>VS</sub> = 13.5 V, V <sub>DIAG_EN</sub> = 5 V, I <sub>OUTx</sub> = 0.1 A, V <sub>OUTx</sub> from 10% to 90%	0.1	0.25	0.5	V/μs
dV/dt(off)	Turnoff slew rate	V <sub>VS</sub> = 13.5 V, V <sub>DIAG_EN</sub> = 5 V, I <sub>OUTx</sub> = 0.1 A, V <sub>OUTx</sub> from 90% to 10%	0.3	0.5	0.9	V/μs
t <sub>d(match)</sub>	t <sub>d(rise)</sub> – t <sub>d(fall)</sub> (See Figure 1.)	V <sub>VS</sub> = 13.5 V, I <sub>L</sub> = 0.1 A. t <sub>d, rise</sub> is the IN rising edge to V <sub>OUTx</sub> = 90%. t <sub>d(fall)</sub> is the IN falling edge to V <sub>OUTx</sub> = 10%.	-60		60	μs
<b>CURRENT-SENSE CHARACTERISTICS (See Figure 2.)</b>						
t <sub>CS(off1)</sub>	CS settling time from DIAG_EN disabled <sup>(1)</sup>	V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = 5 V, I <sub>OUTx</sub> = 0.1 A. current limit = 0.5 A. DIAG_EN falling edge to 10% of V <sub>CS</sub> .			20	μs
t <sub>CS(on1)</sub>	CS settling time from DIAG_EN enabled <sup>(1)</sup>	V <sub>VS</sub> = 13.5 V, V <sub>INx</sub> = 5 V, I <sub>OUTx</sub> = 0.1 A. current limit is 0.5 A. DIAG_EN rising edge to 90% of V <sub>CS</sub> .			20	μs
t <sub>CS(off2)</sub>	CS settling time from IN falling edge	V <sub>VS</sub> = 13.5 V, V <sub>DIAG_EN</sub> = 5 V, I <sub>OUTx</sub> = 0.1 A. current limit = 0.5 A. IN falling edge to 10% of V <sub>CS</sub>			70	μs
t <sub>CS(on2)</sub>	CS settling time from IN rising edge	V <sub>VS</sub> = 13.5 V, V <sub>DIAG_EN</sub> = 5 V, I <sub>OUTx</sub> = 0.1 A. current limit = 0.5 A. IN rising edge to 90% of V <sub>CS</sub>	40		120	μs
t <sub>SEL</sub>	Multi-sense transition delay from channel to channel	V <sub>DIAG_EN</sub> = 5 V, current sense output delay when multi-sense pin SEL transitions from channel to channel			50	μs

(1) Value specified by design, not subject to production test

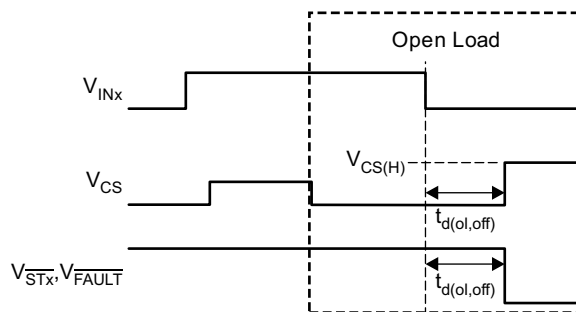




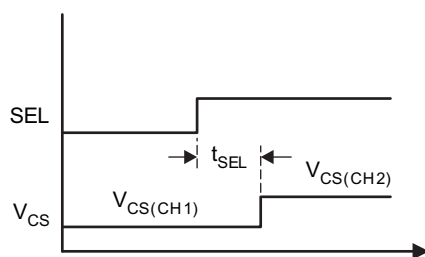
**Figure 1. Output Delay Characteristics**



**Figure 2. CS Delay Characteristics**



**Figure 3. Open-Load Blanking-Time Characteristics**



**Figure 4. Multi-Sense Transition Delay**

## 7.7 Typical Characteristics

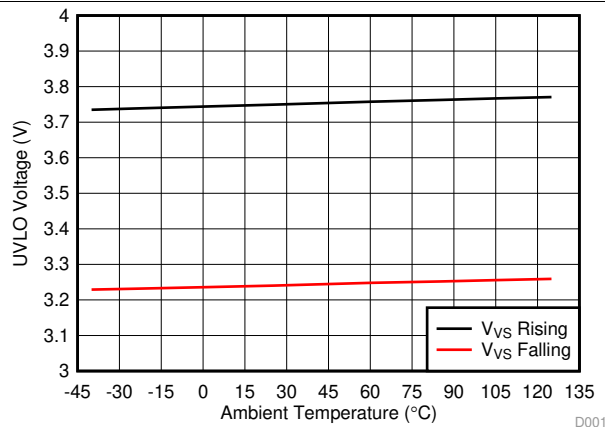


Figure 5. UVLO Voltage Threshold

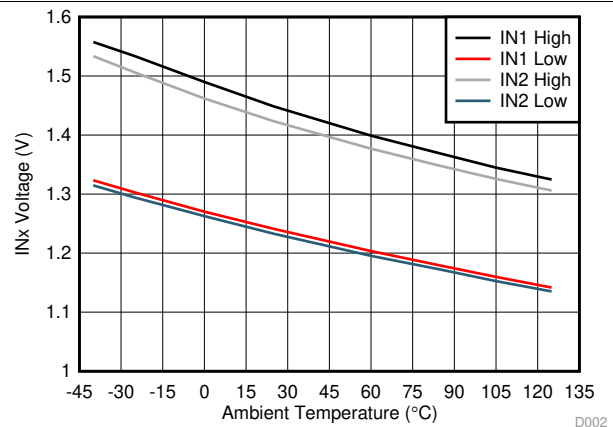


Figure 6. INx Voltage Threshold

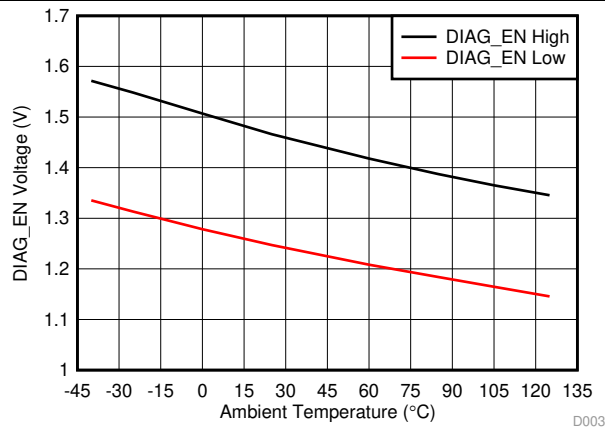


Figure 7. DIAG\_EN Voltage Threshold

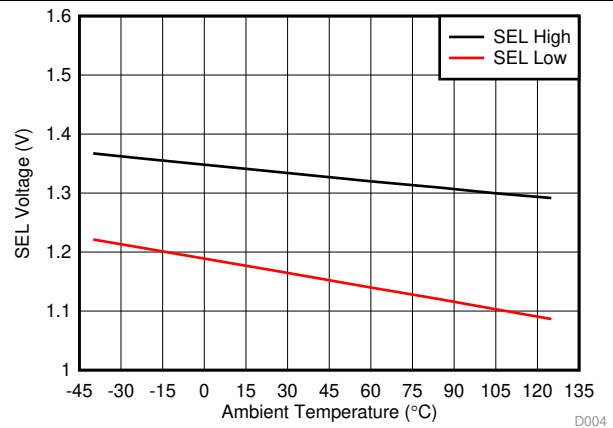


Figure 8. SEL Voltage Threshold

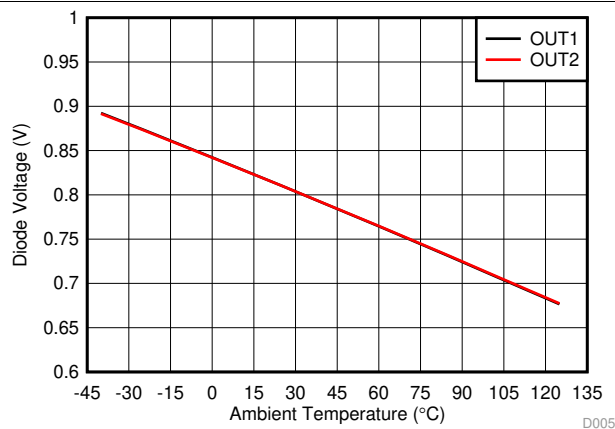


Figure 9. Body-Diode Forward Voltage

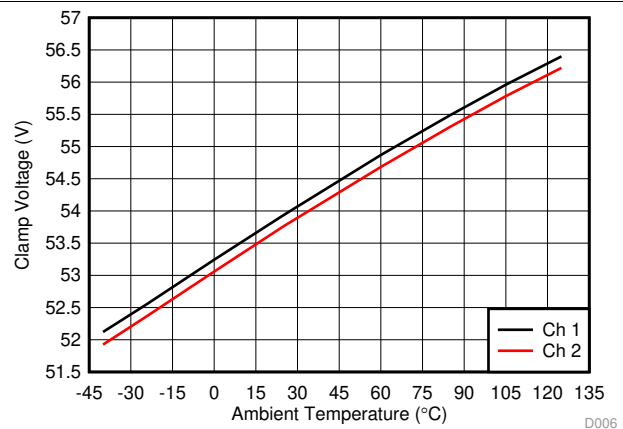
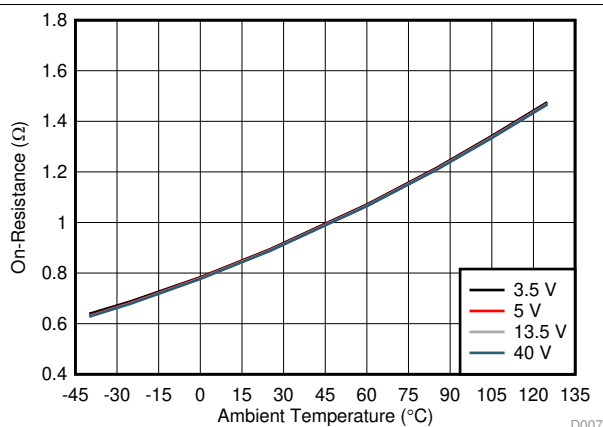
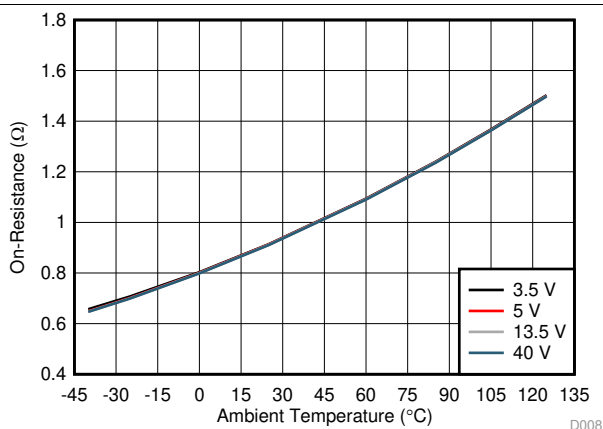


Figure 10. Drain-to-Source Clamp Voltage

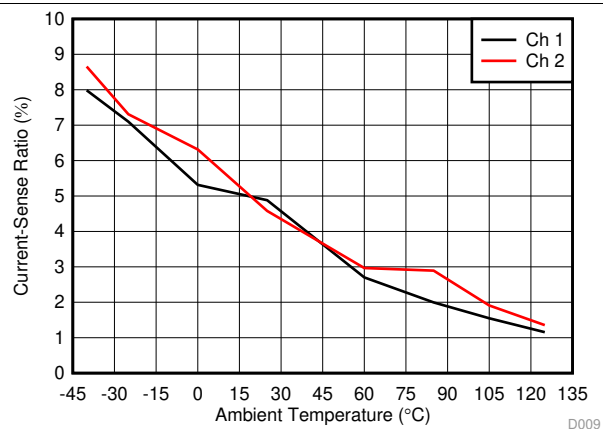
## Typical Characteristics (continued)



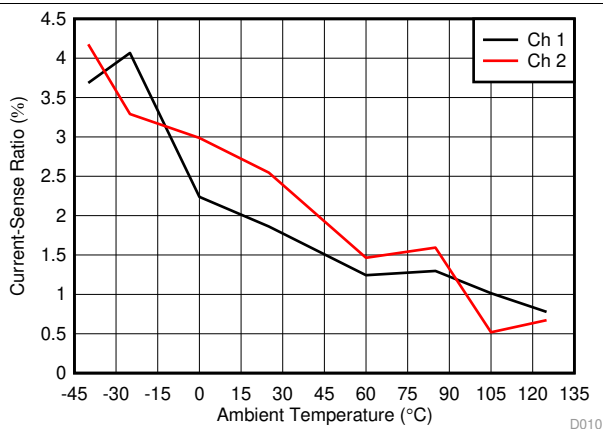
**Figure 11. Channel-1 FET On-Resistance**



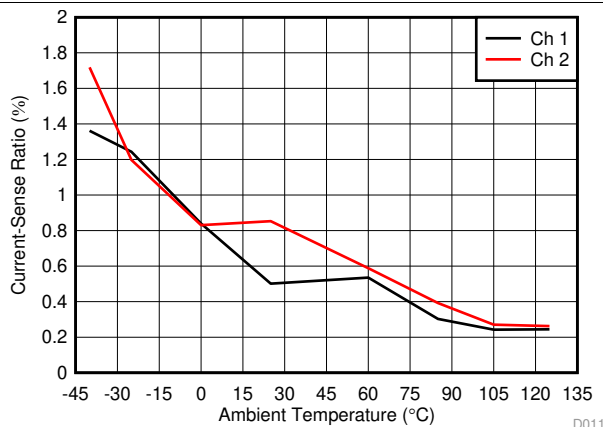
**Figure 12. Channel-2 FET On-Resistance**



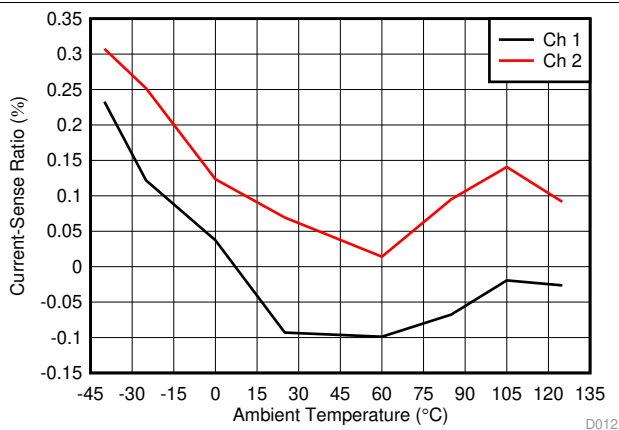
**Figure 13. Current-Sense Ratio at 1 mA**



**Figure 14. Current-Sense Ratio at 2 mA**



**Figure 15. Current-Sense Ratio at 5 mA**



**Figure 16. Current-Sense Ratio at 25 mA**

## Typical Characteristics (continued)

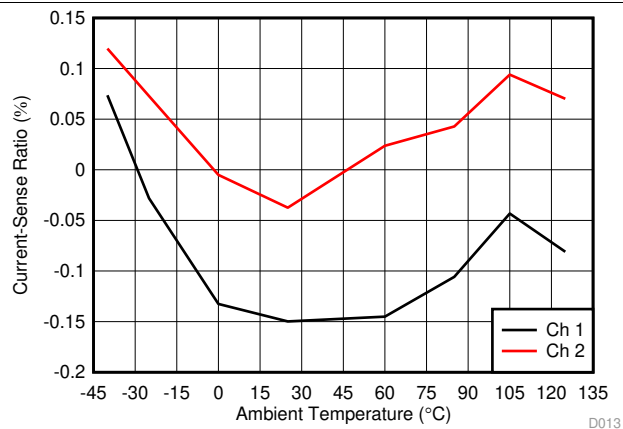


Figure 17. Current-Sense Ratio at 50 mA

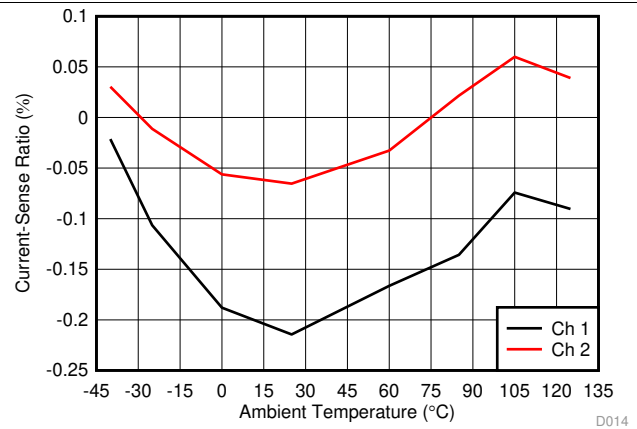


Figure 18. Current-Sense Ratio at 100 mA

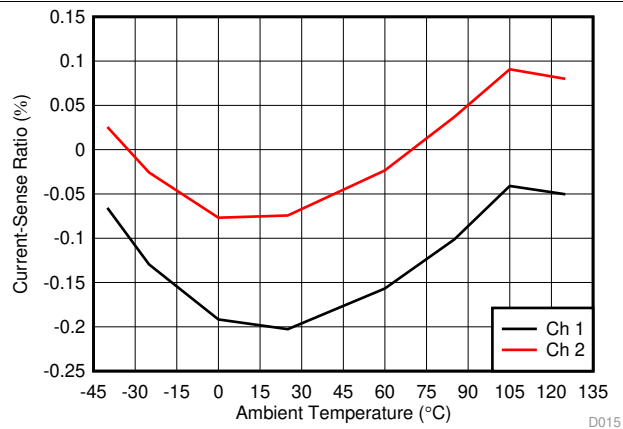


Figure 19. Current-Sense Ratio at 200 mA

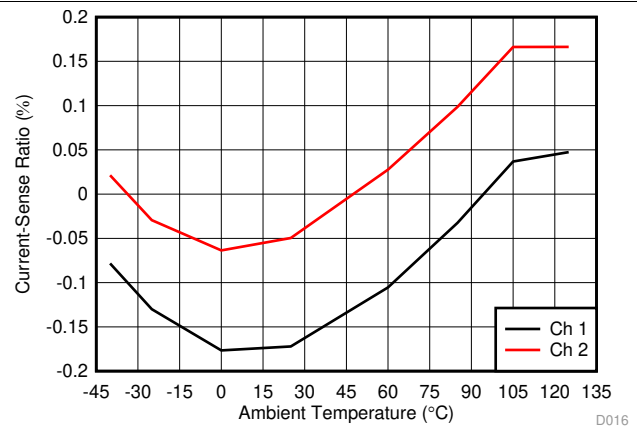


Figure 20. Current-Sense Ratio at 300 mA

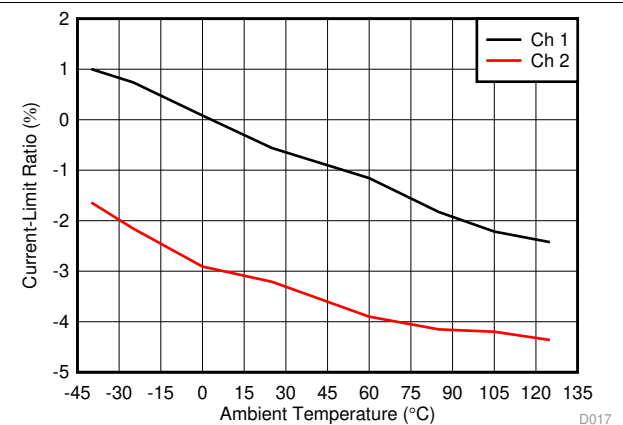


Figure 21. Current-Limit Ratio at 50 mA

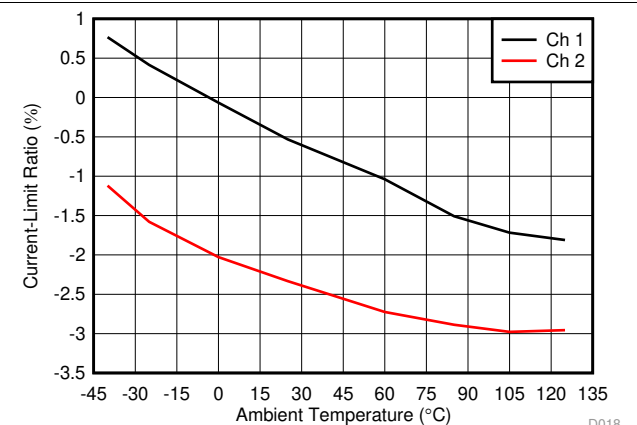
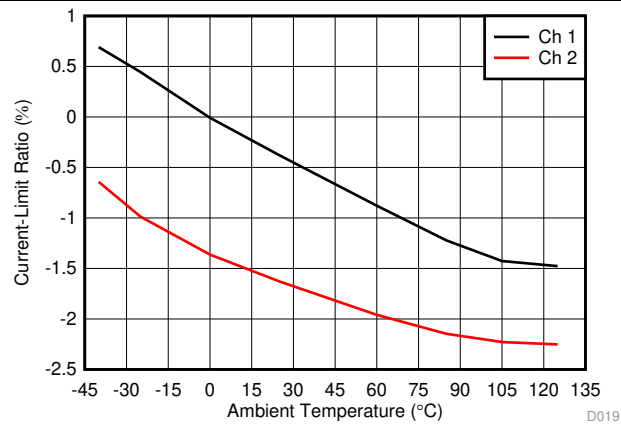
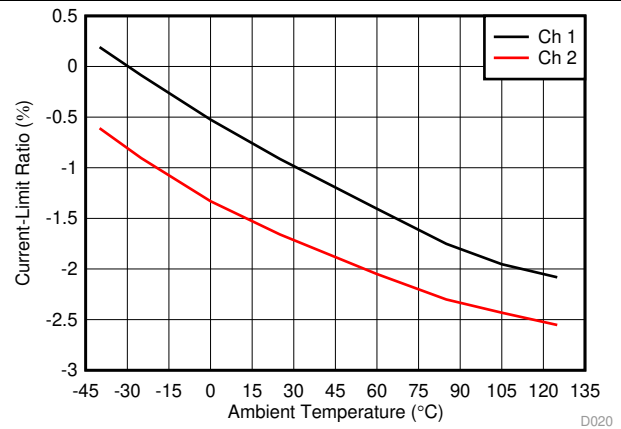


Figure 22. Current-Limit Ratio at 100 mA

## Typical Characteristics (continued)



**Figure 23. Current-Limit Ratio at 200 mA**



**Figure 24. Current-Limit Ratio at 500 mA**

## 8 Detailed Description

### 8.1 Overview

The TPS2H000-Q1 device is a smart high-side switch, with internal charge pump and dual-channel integrated NMOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of whole system. The device has two versions with different diagnostic reporting, the open-drain digital output (version A) and the current-sense analog output (version B).

For version A, the device implements the digital fault report with an open-drain structure. When a fault occurs, the device pulls  $\overline{STx}$  down to GND. A 3.3- or 5-V external pullup is required to match the microcontroller supply level. The digital status of each channel can report individually, or globally by connecting the  $\overline{STx}$  pins together.

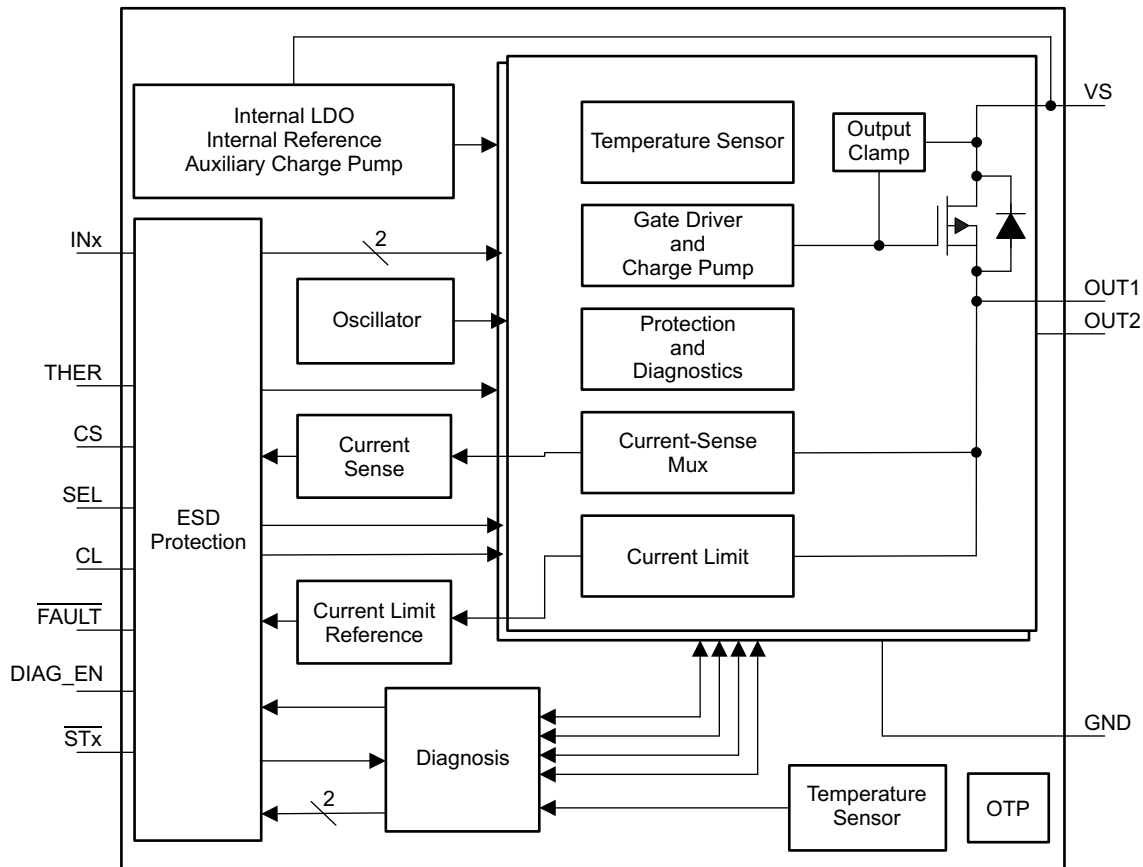
For version B, high-accuracy current sense makes the diagnostics more accurate without further calibration. One integrated current mirror can source  $1 / K_{(CS)}$  of the load current. The mirrored current flows into the CS-pin resistor to become a voltage signal.  $K_{(CS)}$  is a constant value across temperature and supply voltage. A wide linear region from 0 V to 4 V allows a better real-time load-current monitoring. The CS pin can also report a fault with pullup voltage of  $V_{CS(H)}$ .

The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. Besides, the device also implements an internal current limit with a fixed value.

For inductive loads (relays, solenoids, valves), the device implements an active clamp between drain and source to protect itself. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power and EMI to a minimum.

The TPS2H000-Q1 device is a smart high-side switch for a wide variety of resistive, inductive, and capacitive loads, including LEDs, relays, and sub-modules.

## 8.2 Functional Block Diagram

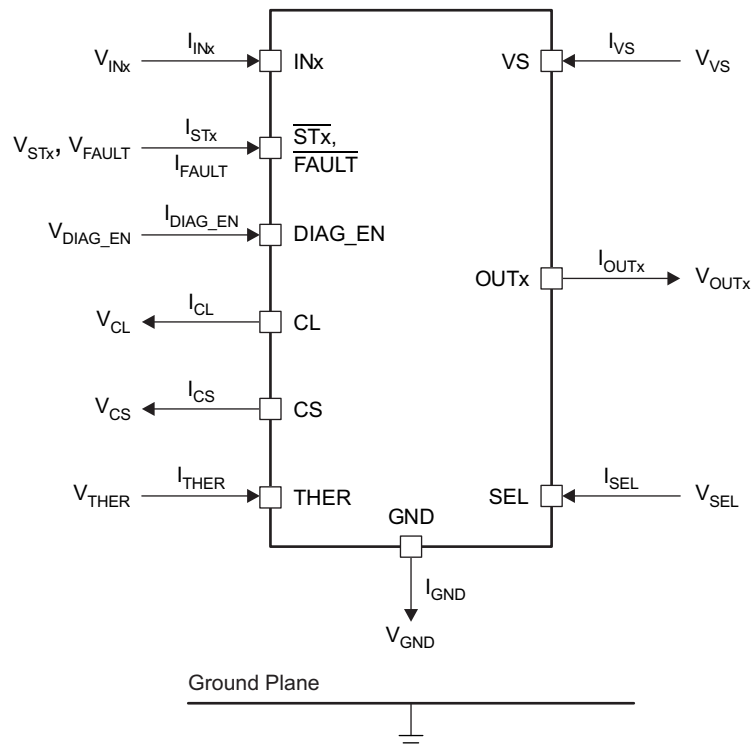


### 8.3 Feature Description

### 8.3.1 Pin Current and Voltage Conventions

For reference purposes throughout the data sheet, current directions on their respective pins are as shown by the arrows in [Figure 25](#). All voltages are measured relative to the ground plane.

## Feature Description (continued)

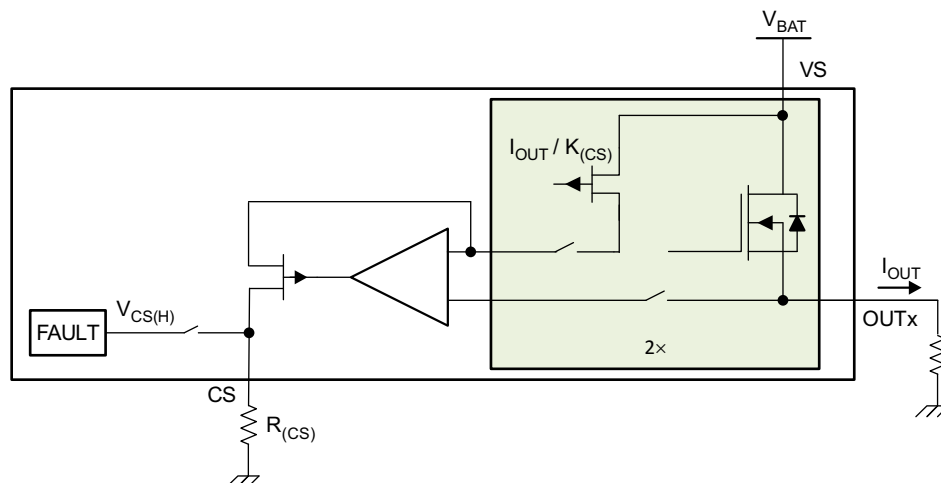


**Figure 25. Voltage and Current Conventions**

### 8.3.2 Accurate Current Sense

High-accuracy current sense is implemented in the version-B device. It allows a better real-time monitoring effect and more-accurate diagnostics without further calibration.

One integrated current mirror can source  $1 / K_{(CS)}$  of the load current, and the mirrored current flows into the external current sense resistor to become a voltage signal. The current mirror is shared by the dual channels.  $K_{(CS)}$  is the ratio of the output current and the sense current. It is a constant value across the temperature and supply voltage. Each device is calibrated accurately during production, so post-calibration is not required. See [Figure 26](#) for more details.

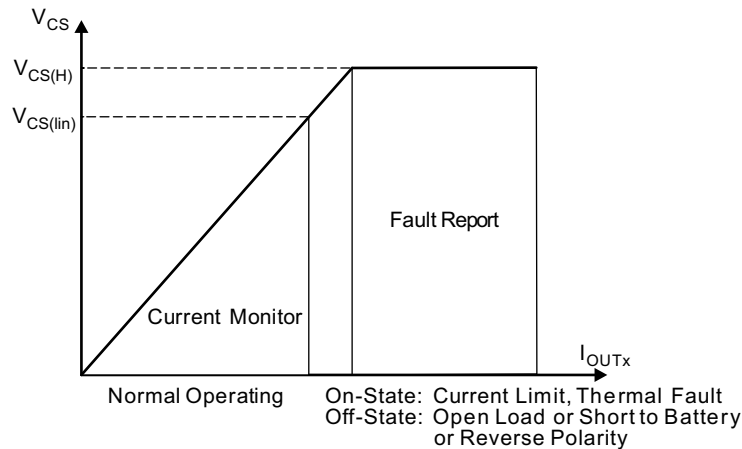


**Figure 26. Current-Sense Block Diagram**



## Feature Description (continued)

When a fault occurs, the CS pin also works as a fault report with a pullup voltage,  $V_{CS(H)}$ . See [Figure 27](#) for more details.



**Figure 27. Current-Sense Output-Voltage Curve**

Use [Equation 1](#) to calculate  $R_{(CS)}$ .

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUTx}} \quad (1)$$

Take the following points into consideration when calculating  $R_{(CS)}$ .

- Ensure  $V_{CS}$  is within the current-sense linear region ( $V_{CS}$ ,  $I_{OUTx(lin)}$ ) across the full range of the load current. Check  $R_{(CS)}$  with [Equation 2](#).

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \leq \frac{V_{CS(lin)}}{I_{CS}} \quad (2)$$

- In fault mode, ensure  $I_{CS}$  is within the source capacity of the CS pin ( $I_{CS(H)}$ ). Check  $R_{(CS)}$  with [Equation 3](#).

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} \geq \frac{V_{CS(H,min)}}{I_{CS(H,min)}} \quad (3)$$

### 8.3.3 Adjustable Current Limit

A high-accuracy current limit allows high reliability of the design. It protects the load and the power supply from overstressing during short-circuit-to-GND or power-up conditions. The current limit can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage.

When a current-limit threshold is hit, a closed loop activates immediately. The output current is clamped at the set value, and a fault is reported out. The device heats up due to the high power dissipation on the power FET. If thermal shutdown occurs, the current limit is set to  $I_{CL(TSD)}$  to reduce the power dissipation on the power FET. See [Figure 28](#) for more details.

The device has two current-limit thresholds.

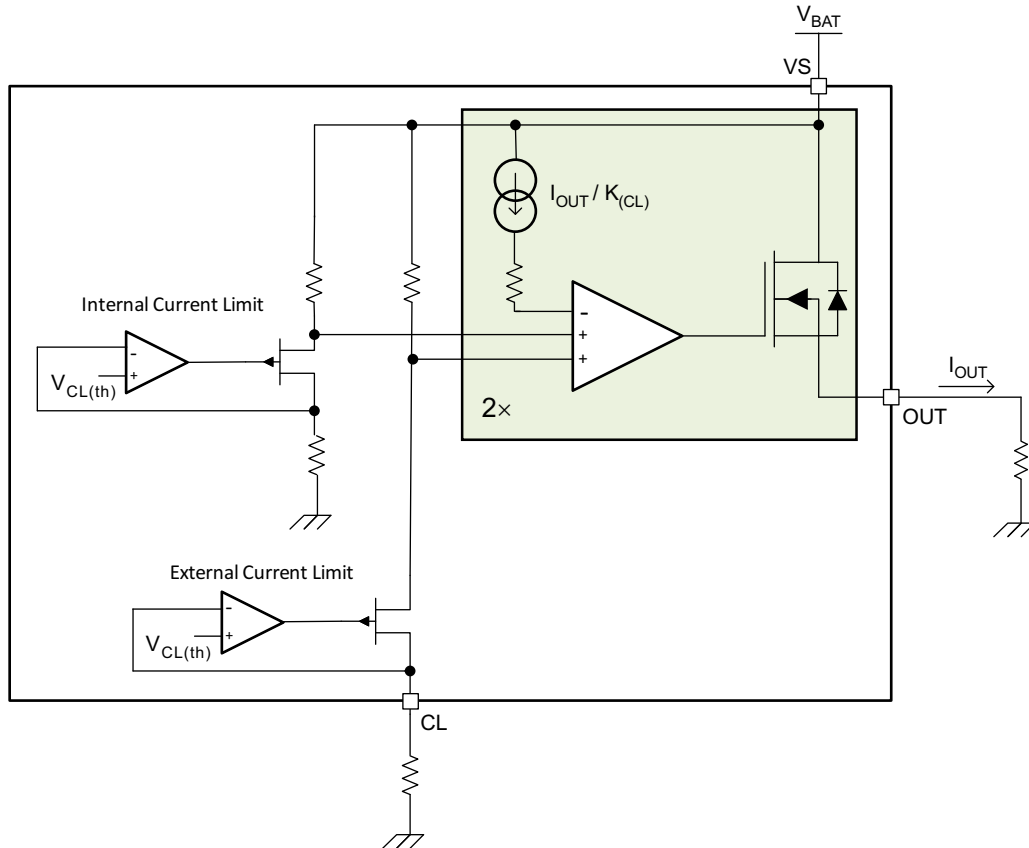
- Internal current limit** – The internal current limit is fixed at  $I_{CL(int)}$ . Tie the CL pin directly to the device GND for large-transient-current applications.
- External adjustable current limit** – An external resistor is used to set the current-limit threshold. Use the [Equation 4](#) to calculate the  $R_{(CL)}$ .  $V_{CL(th)}$  is the internal band-gap voltage.  $K_{(CL)}$  is the ratio of the output current and the current-limit set value. It is constant across the temperature and supply voltage. The external adjustable current limit allows the flexibility to set the current limit value by applications.

## Feature Description (continued)

$$I_{CL} = \frac{V_{CL(th)}}{R_{(CL)}} = \frac{I_{OUT}}{K_{(CL)}}$$

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}}$$

(4)



**Figure 28. Current-Limit Block Diagram**

Note that if using a GND network which causes a level shift between the device GND and board GND, the CL pin must be connected with device GND.

For better protection from a hard short-to-GND condition (when the INx pins are enabled, a short to GND occurs suddenly), the device implements a fast-trip protection to turn off the related channel before the current-limit closed loop is set up. The fast-trip response time is less than 1  $\mu$ s, typically. With this fast response, the device can achieve better inrush current-suppression performance.

### 8.3.4 Inductive-Load Switching-Off Clamp

When switching an inductive load off, the inductive reactance tends to pull the output voltage negative. Excessive negative voltage could cause the power FET to break down. To protect the power FET, an internal clamp between drain and source is implemented, namely  $V_{DS(clamp)}$ .

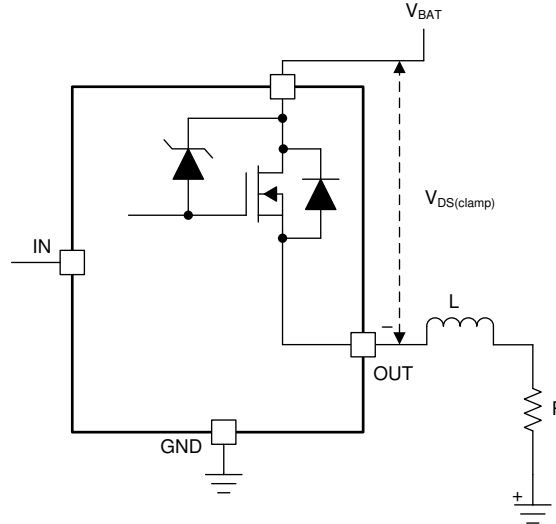
$$V_{DS(clamp)} = V_{VS} - V_{OUT} \quad (5)$$

During the period of demagnetization ( $t_{decay}$ ), the power FET is turned on for inductance-energy dissipation. The total energy is dissipated in the high-side switch. Total energy includes the energy of the power supply ( $E_{(VS)}$ ) and the energy of the load ( $E_{(load)}$ ). If resistance is in series with inductance, some of the load energy is dissipated on the resistance.

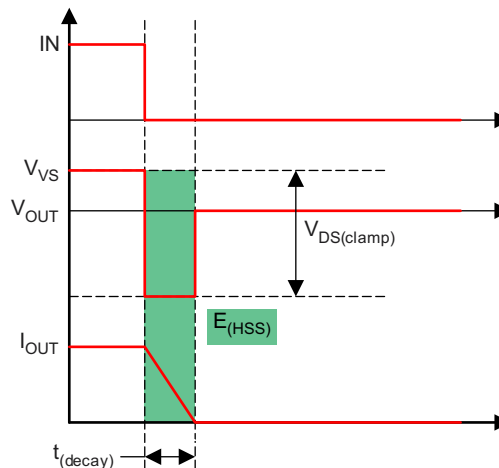
## Feature Description (continued)

$$E_{(HSS)} = E_{(VS)} + E_{(load)} = E_{(VS)} + E_{(L)} - E_{(R)} \quad (6)$$

When an inductive load switches off,  $E_{(HSS)}$  causes high thermal stressing on the device.. The upper limit of the power dissipation depends on the device intrinsic capacity, ambient temperature, and board dissipation condition.



**Figure 29. Drain-to-Source Clamping Structure**



**Figure 30. Inductive Load Switching-Off Diagram**

From the perspective of the high-side switch,  $E_{(HSS)}$  equals the integration value during the demagnetization period.

$$E_{(HSS)} = \int_0^{t_{(decay)}} V_{DS(clamp)} \times I_{OUT}(t) dt$$

$$t_{(decay)} = \frac{L}{R} \times \ln \left( \frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|} \right)$$

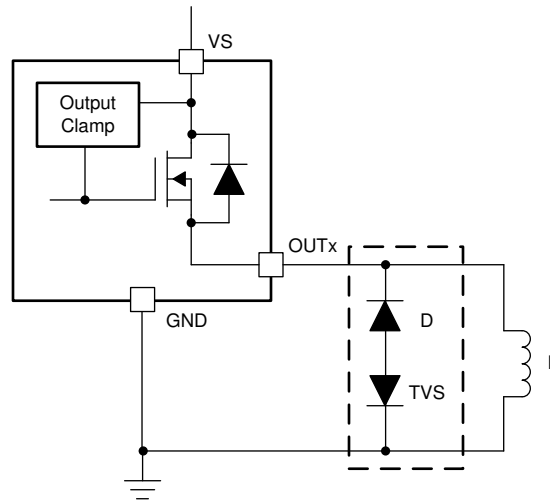
$$E_{(HSS)} = L \times \frac{V_{VS} + |V_{OUT}|}{R^2} \times \left[ R \times I_{OUT(max)} - |V_{OUT}| \ln \left( \frac{R \times I_{OUT(max)} + |V_{OUT}|}{|V_{OUT}|} \right) \right] \quad (7)$$

## Feature Description (continued)

When R approximately equals 0,  $E_{(HSD)}$  can be given simply as:

$$E_{(HSS)} = \frac{1}{2} \times L \times I_{OUT(max)}^2 \frac{V_{VS} + |V_{OUT}|}{|V_{OUT}|} \quad (8)$$

Note that for PWM-controlled inductive loads, it is recommended to add the external free-wheeling circuitry shown in [Figure 31](#) to protect the device from repetitive power stressing. TVS is used to achieve the fast decay. See [Figure 31](#) for more details.



**Figure 31. Protection With External Circuitry**

### 8.3.5 Fault Detection and Reporting

#### 8.3.5.1 Diagnostic Enable Function

The DIAG\_EN pin enables or disables the diagnostic functions. If multiple devices are used, but the ADC resource is limited in the microcontroller, the MCU can use GPIOs to set DIAG\_EN high to enable the diagnostics of one device while disabling the diagnostics of the other devices by setting DIAG\_EN low. In addition, the device can keep the power consumption to a minimum by setting DIAG\_EN and INx low.

#### 8.3.5.2 Multiplexing of Current Sense

For version B, SEL is used to multiplex the shared current-sense function between the two channels. See [Table 1](#) for more details.

**Table 1. Diagnosis Configuration Table**

DIAG_EN	INx	SEL	CS ACTIVATED CHANNEL	CS, $\overline{\text{FAULT}}$ , $\overline{\text{STx}}$	PROTECTIONS AND DIAGNOSTICS
L	H	—	—	High impedance	Diagnostics disabled, full protection
	L				Diagnostics disabled, no protection
H	—	0	Channel 1	See <a href="#">Table 2</a>	See <a href="#">Table 2</a>
		1	Channel 2		

### 8.3.5.3 Fault Table

Table 2 applies when the DIAG\_EN pin is enabled.

**Table 2. Fault Table**

CONDITIONS	IN <sub>x</sub>	OUT <sub>x</sub>	THER	CRITERION	$\overline{\text{STx}}$ (VER. A)	CS (VER. B)	$\overline{\text{FAULT}}$ (VER. B)	FAULT RECOVERY
Normal	L	L	—	—	H	0	H	—
	H	H	—	—	H	In linear region	H	—
Overload, short to ground	H	L	—	Current limit triggered	L	V <sub>CS(H)</sub>	L	Auto
Open load <sup>(1)</sup> , short to battery, reverse polarity	L	H	—	$V_{\text{VS}} - V_{\text{OUTx}} < V_{\text{(ol,off)}}$	L	V <sub>CS(H)</sub>	L	Auto
Thermal shutdown	H	—	L	T <sub>SD</sub> triggered	L	V <sub>CS(H)</sub>	L	Output auto-retry. Fault recovers when T <sub>J</sub> < T <sub>(SD,rst)</sub> or when IN <sub>x</sub> toggles.
			H					Output latch off. Fault recovers when IN <sub>x</sub> toggles.
Thermal swing	H	—	—	T <sub>SW</sub> triggered	L	V <sub>CS(H)</sub>	L	Auto

(1) An external pullup is required for open-load detection.

### 8.3.5.4 $\overline{\text{STx}}$ and $\overline{\text{FAULT}}$ Reporting

For version A, two individual  $\overline{\text{STx}}$  pins report the fault conditions, each pin for its respective channel. When a fault condition occurs, it pulls  $\overline{\text{STx}}$  down to GND. A 3.3- or 5-V external pullup is required to match the supply level of the microcontroller. The digital status of each channel can be reported individually, or globally by connecting all the  $\overline{\text{STx}}$  pins together.

For version B, a global  $\overline{\text{FAULT}}$  pin is used to monitor the global fault condition among all the channels. When a fault condition occurs on any channel, the  $\overline{\text{FAULT}}$  pin is pulled down to GND. A 3.3-V or 5-V external pullup is required to match the supply level of the microcontroller.

After the  $\overline{\text{FAULT}}$  report, the microcontroller can check and identify the channel in fault status by multiplexed current sensing. The CS pin also works as a fault report with an internal pullup voltage, V<sub>CS(H)</sub>.

## 8.3.6 Full Diagnostics

### 8.3.6.1 Short-to-GND and Overload Detection

When a channel is on, a short to GND or overload condition causes overcurrent. If the overcurrent triggers either the internal or external current-limit threshold, the fault condition is reported out. The microcontroller can handle the overcurrent by turning off the switch. The device heats up if no actions are taken. If a thermal shutdown occurs, the current limit is I<sub>CL(TSD)</sub> to keep the power stressing on the power FET to a minimum. The device automatically recovers when the fault condition is removed.

### 8.3.6.2 Open-Load Detection

#### 8.3.6.2.1 Channel On

When a channel on, benefiting from the high-accuracy current sense in a small current range, if an open-load event occurs, it can be detected as an ultralow V<sub>CS</sub> and handled by the microcontroller. Note that the detection is not reported on the  $\overline{\text{STx}}$  or  $\overline{\text{FAULT}}$  pins. The microcontroller must set the SEL pin to detect the channel-on open-load fault proactively.

#### 8.3.6.2.2 Channel Off

When a channel is off, if a load is connected, the output is pulled down to GND. But if an open load occurs, the output voltage is close to the supply voltage ( $V_{\text{VS}} - V_{\text{OUTx}} < V_{\text{(ol,off)}}$ ), and the fault is reported out.

The diagram illustrates a circuit for open-load detection during the off-state of a power MOSFET. The MOSFET's gate is driven by a pulse-width modulated signal. Its drain is connected to a load through a resistor labeled  $R_{(PU)}$ , which is supplied by a battery voltage  $V_{BAT}$ . A sense resistor is placed between the MOSFET drain and the load resistor. The MOSFET's source is connected to ground through another sense resistor. Two comparators are used for detection: one compares the drain-source voltage  $V_{DS}$  against a threshold  $V_{(ol,off)}$ , and the other compares the voltage across the source sense resistor against a reference voltage. The outputs of these comparators are combined via an OR gate to generate the 'Open Load' signal.

thermal shutdown fault signal is cleared when  $T_J < T_{(SD,rst)}$  or after toggling the related INx pin.

- When the THER pin is high, thermal shutdown operates in the latch mode. The output latches off when thermal shutdown occurs. When the THER pin goes from high to low, thermal shutdown changes to auto-retry mode. The thermal shutdown fault signal is cleared after toggling the related INx pin.

Thermal swing activates when the power FET temperature is increasing sharply, that is, when  $\Delta T = T_{(FET)} - T_{(Logic)} > T_{(sw)}$ , then the output turns off. The output automatically recovers and the fault signal clears when  $\Delta T = T_{(FET)} - T_{(Logic)} < T_{(sw)} - T_{(hys)}$ . Thermal swing function improves the device reliability when subjected to repetitive fast thermal variation. As shown in Figure 33, multiple thermal swings are triggered before thermal shutdown occurs.

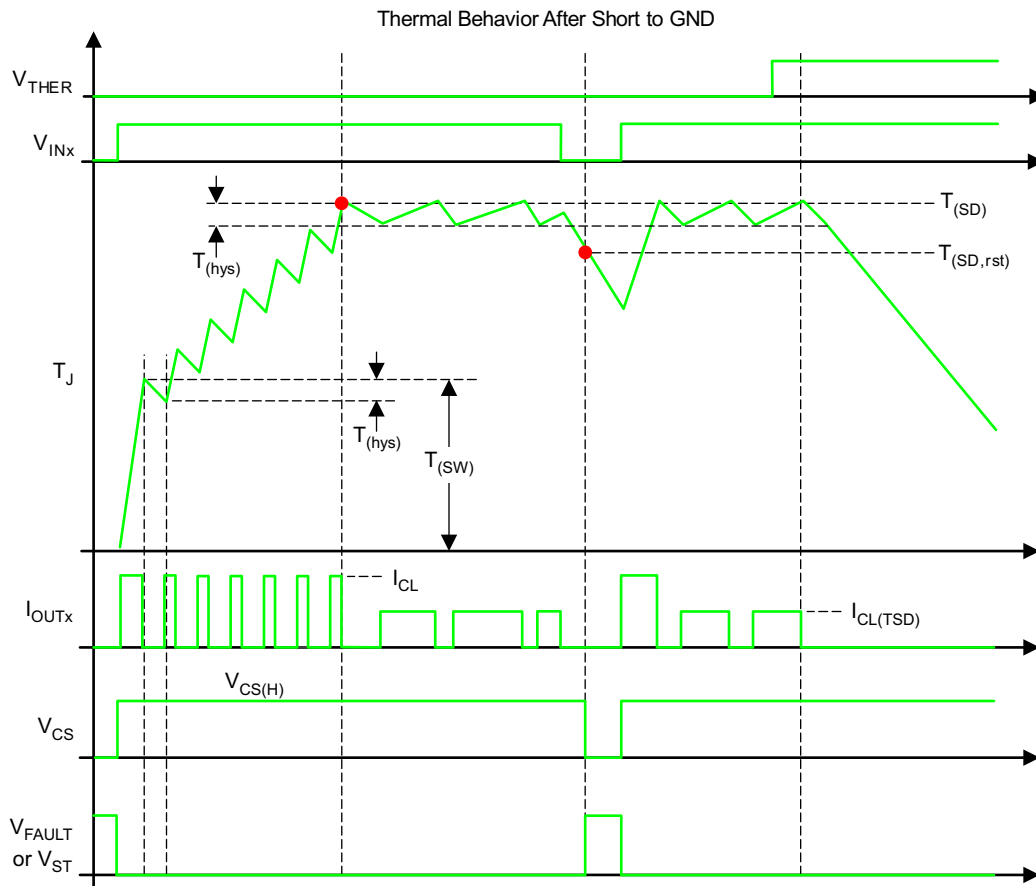


Figure 33. Thermal Behavior Diagram

### 8.3.7 Full Protections

#### 8.3.7.1 UVLO Protection

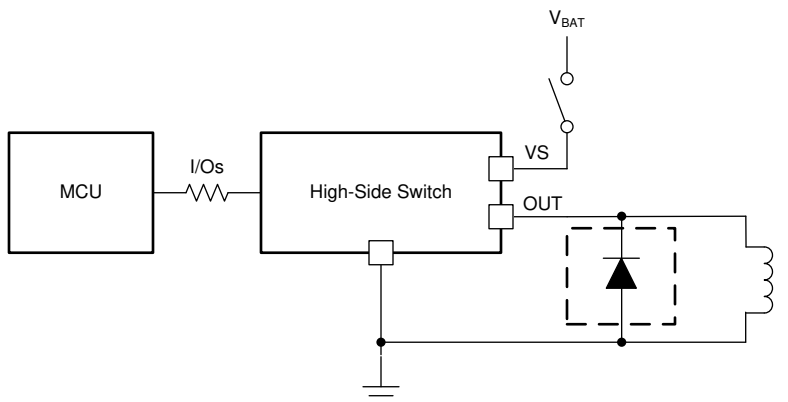
The device monitors the supply voltage  $V_{VS}$ , to prevent unpredicted behaviors when  $V_{VS}$  is too low. When  $V_{VS}$  falls down to  $V_{VS(uvf)}$ , the device shuts down. When  $V_{VS}$  rises up to  $V_{VS(uvr)}$ , the device turns on.

#### 8.3.7.2 Loss-of-GND Protection

When loss of GND occurs, output is shut down regardless of whether the INx pin is high or low. The device can protect against two ground-loss conditions, loss of device GND and loss of module GND.

### 8.3.7.3 Protection for Loss of Power Supply

When loss of supply occurs, the output is shut down regardless of whether the INx pin is high or low. For a resistive or a capacitive load, loss of supply has no risk. But for a charged inductive load, the current is driven from all the I/O pins to maintain the inductance current. To protect the system in this condition, TI recommends the external free-wheeling diode as shown in [Figure 34](#).



**Figure 34. Protection for Loss of Power Supply**

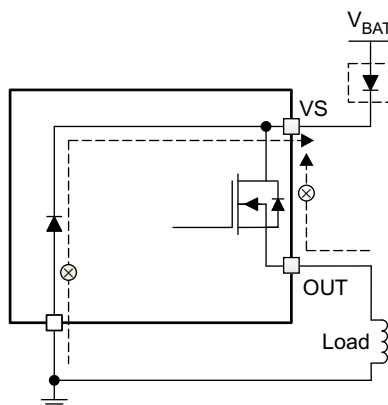
### 8.3.7.4 Reverse-Current Protection

Reverse current occurs in two conditions: short to battery and reverse polarity.

- When a short to the battery occurs, there is only reverse current through the body diode.  $I_{R(1)}$  specifies the limit of the reverse current.
- In a reverse-polarity condition, there are reverse currents through the body diode and the device GND pin.  $I_{R(2)}$  specifies the limit of the reverse current. The GND pin maximum current is specified in the [Absolute Maximum Ratings](#).

To protect the device, TI recommends two types of external circuitry.

- Adding a blocking diode. Both the IC and load are protected when in reverse polarity.



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**Figure 35. Reverse-Current External Protection, Method 1**

- Adding a GND network. The reverse current through the device GND is blocked. The reverse current through the FET is limited by the load itself. TI recommends a resistor in parallel with the diode as a GND network. The recommended selection are 1-k $\Omega$  resistor in parallel with an >100-mA diode. If multiple high-side switches are used, the resistor and diode can be shared among devices. The reverse current protection diode in the GND network forward voltage should be less than 0.6 V in any circumstances. In addition a minimum resistance of 4.7 K is recommended on the I/O pins.



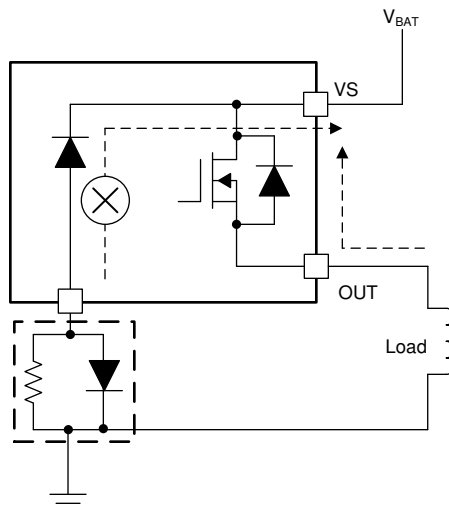


Figure 36. Reverse-Current External Protection, Method 2

### 8.3.7.5 MCU I/O Protection

In some severe conditions, such as the ISO7637-2 test or the loss of battery with inductive loads, a negative pulse occurs on the GND pin. This pulse can cause damage on the connected microcontroller. TI recommends serial resistors to protect the microcontroller, for example, 4.7-k $\Omega$  when using a 3.3-V microcontroller and 10-k $\Omega$  for a 5-V microcontroller.

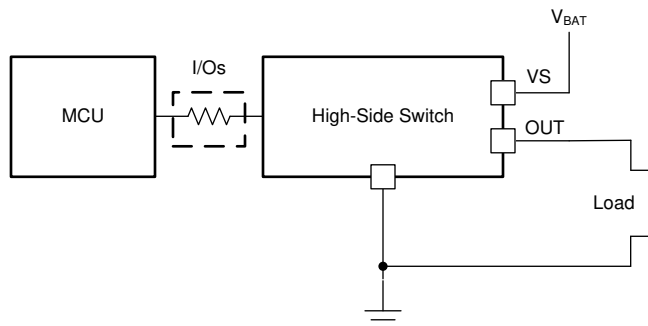


Figure 37. MCU I/O External Protection

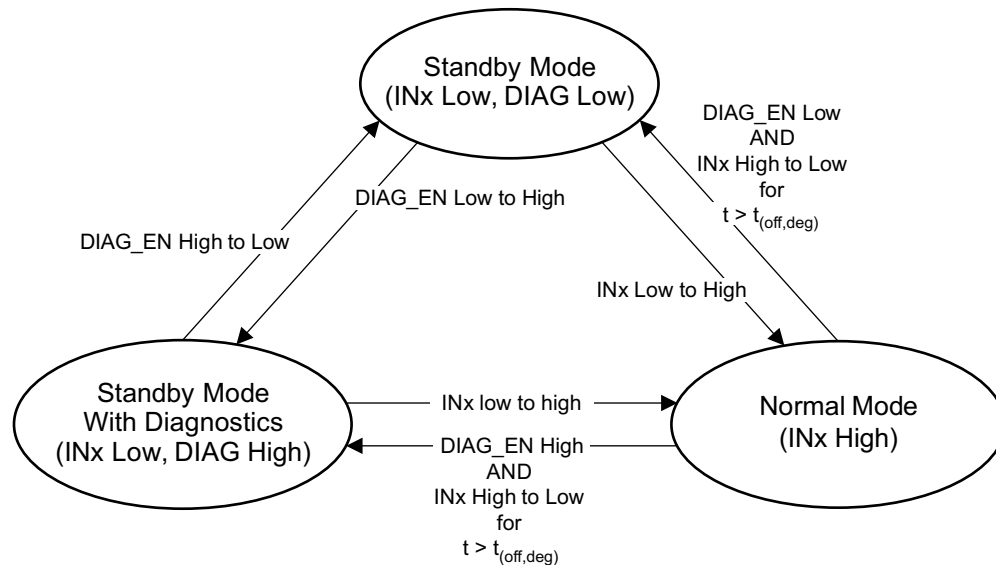
## 8.4 Device Functional Modes

### 8.4.1 Working Modes

The device has three working modes, the normal mode, the standby mode, and the standby mode with diagnostics.

Note that IN must be low for  $t > t_{(off,deg)}$  to enter the standby mode, where  $t_{(off,deg)}$  is the standby mode deglitch time used to avoid false triggering. [Figure 38](#) shows a working-mode diagram.

## Device Functional Modes (continued)



**Figure 38. Working Modes**

## 9 Application and Implementation

### NOTE

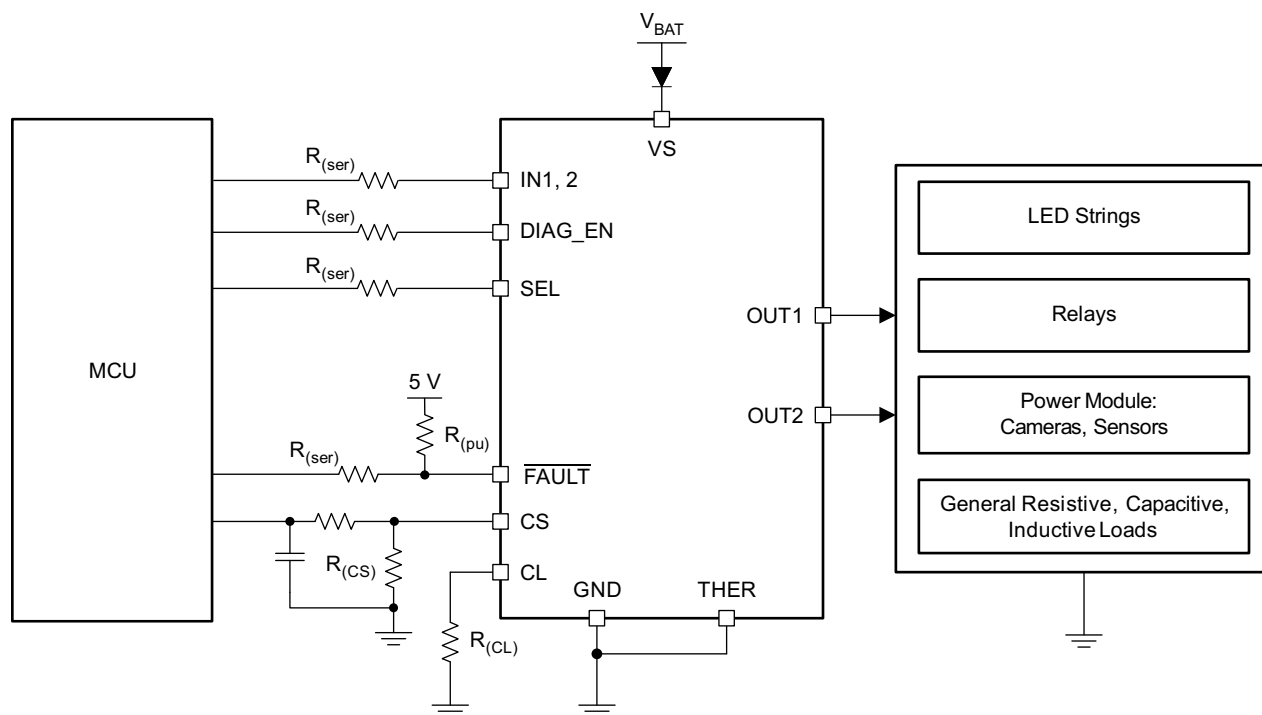
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS2H000-Q1 device is capable of driving a wide variety of resistive, inductive, and capacitive loads, including LEDs, relays, and sub-modules. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current.

### 9.2 Typical Application

The following figure shows an example of the external circuitry connections based on the version-B device.



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**Figure 39. Typical Application Diagram**

#### 9.2.1 Design Requirements

- $V_{VS}$  range from 9 V to 16 V
- Load range is from 0.1 A to 0.25 A for each channel
- Current sense for fault monitoring
- Expected current-limit value of 0.5 A
- Automatic recovery mode when thermal shutdown occurs
- Full diagnostics with 5-V MCU
- Reverse-voltage protection with a blocking diode in the power-supply line

## Typical Application (continued)

### 9.2.2 Detailed Design Procedure

To keep the 0.25-A nominal current in the 0 to 4-V current-sense range, calculate the  $R_{(CS)}$  resistor using Equation 9. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R_{(CS)} = \frac{V_{CS}}{I_{CS}} = \frac{V_{CS} \times K_{(CS)}}{I_{OUT}} = \frac{4 \times 80}{0.25} = 1280 \, \Omega \quad (9)$$

To set the adjustable current limit value at 0.5 A, calculate  $R_{(CL)}$  using Equation 10.

$$R_{(CL)} = \frac{V_{CL(th)} \times K_{(CL)}}{I_{OUT}} = \frac{0.8 \times 300}{0.5} = 480 \, \Omega \quad (10)$$

TI recommends  $R_{(ser)} = 10 \, k\Omega$  for 5-V MCU, and  $R_{(pu)} = 10 \, k\Omega$  as the pullup resistor.

### 9.2.3 Application Curves

Figure 40 shows a test example of soft-start when driving a big capacitive load. Figure 41 shows an expanded waveform of the output current.

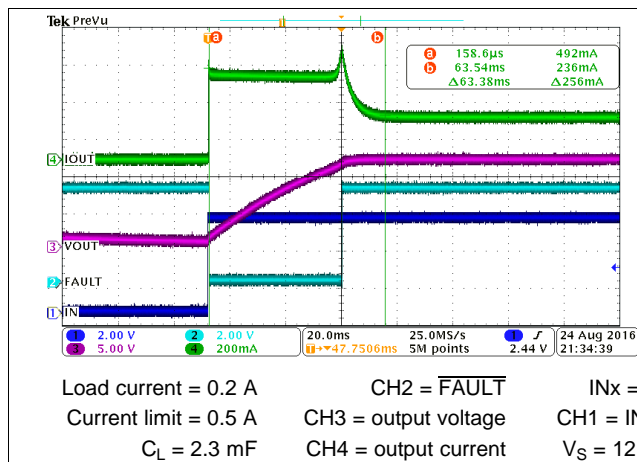


Figure 40. Driving a Capacitive Load

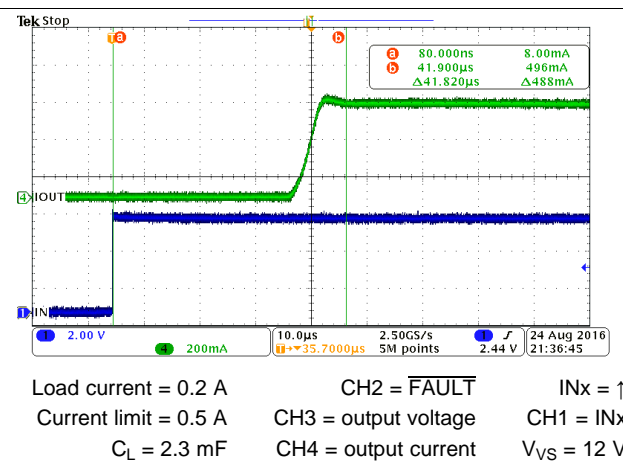
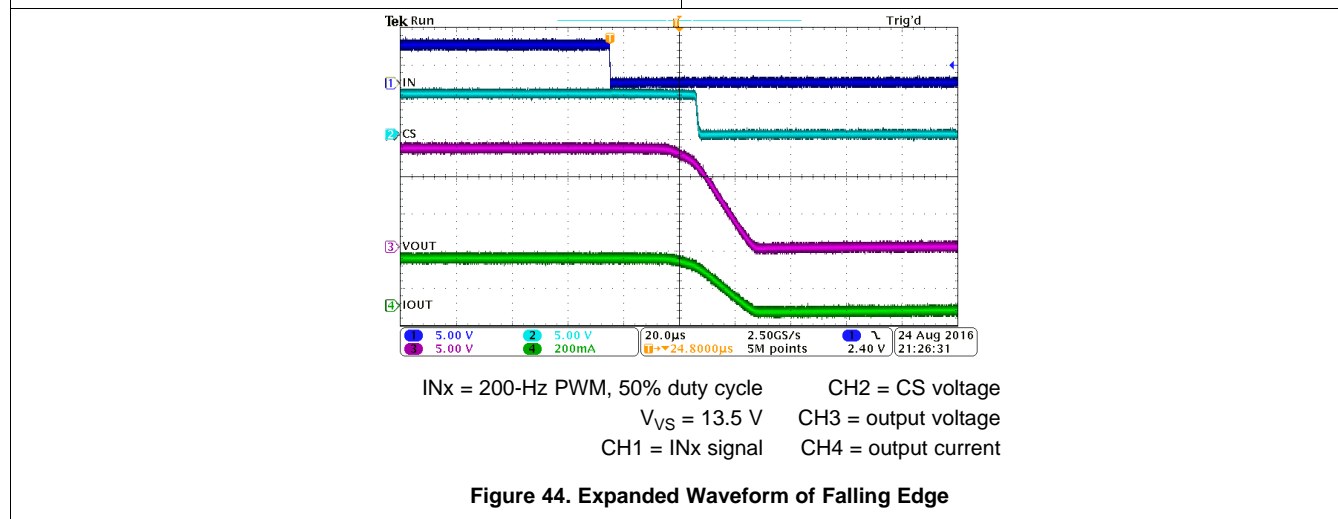
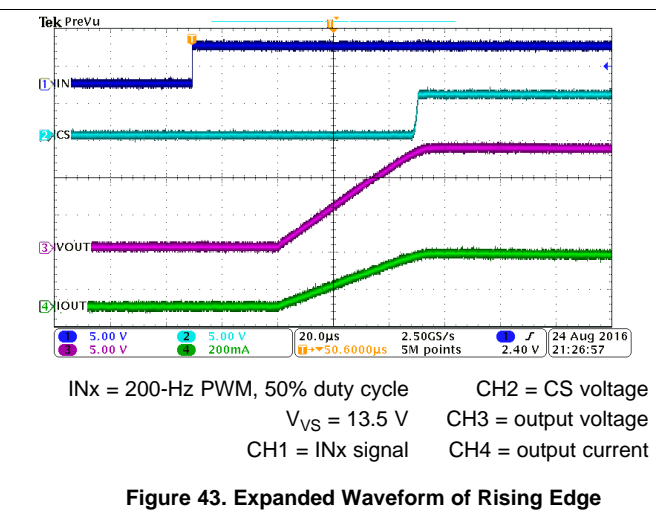
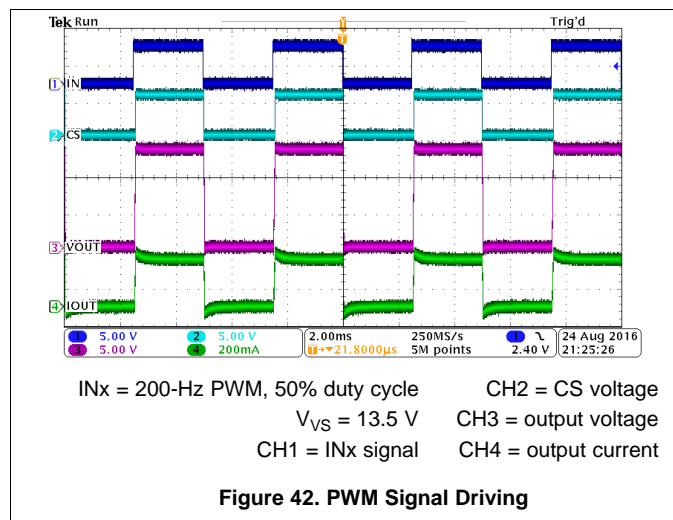


Figure 41. Driving a Capacitive Load, Expanded Waveform

## Typical Application (continued)

Figure 42 shows a test example of PWM-mode driving. Figure 43 shows the expanded waveform of the rising edge. Figure 44 shows the expanded waveform of the falling edge.



## 10 Power Supply Recommendations

The device is qualified for both automotive and industrial applications. The normal power supply connection is a 12-V automotive system or 24-V industrial system. Detailed supply voltage should be within the range specified in the [Recommended Operating Conditions](#).

## 11 Layout

### 11.1 Layout Guidelines

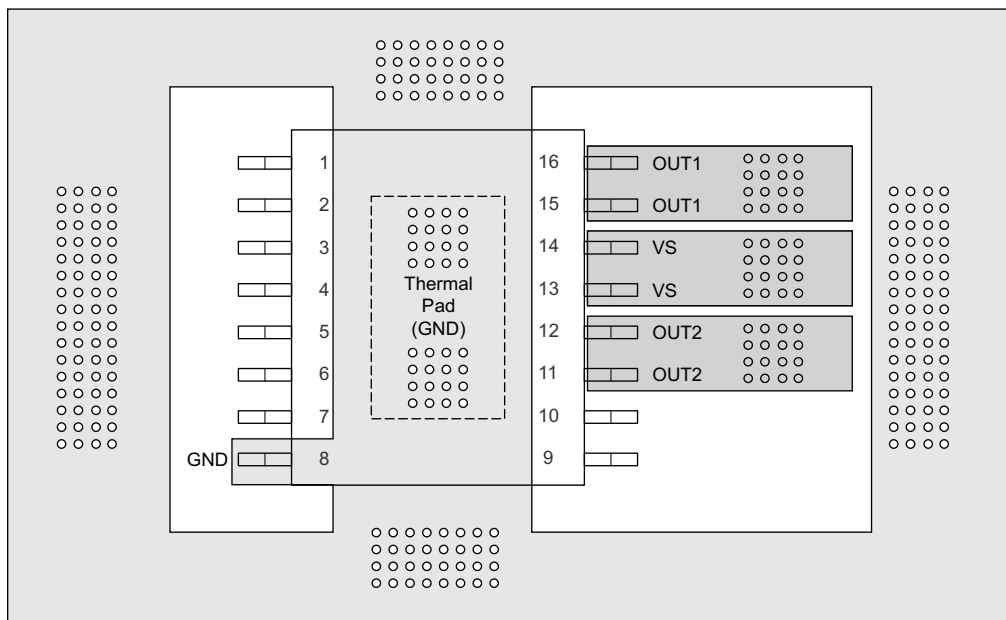
To prevent thermal shutdown,  $T_J$  must be less than 150°C. The HTSSOP package has good thermal impedance. However, the PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

- Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. The major heat flow path from the package to the ambient is through the copper on the PCB. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
- Add as many thermal vias as possible directly under the package ground pad to optimize the thermal conductivity of the board.
- All thermal vias should either be plated shut or plugged and capped on both sides of the board to prevent solder voids. To ensure reliability and performance, the solder coverage should be at least 85%.

### 11.2 Layout Examples

#### 11.2.1 Without a GND Network

Without a GND network, tie the thermal pad directly to the board GND copper for better thermal performance.

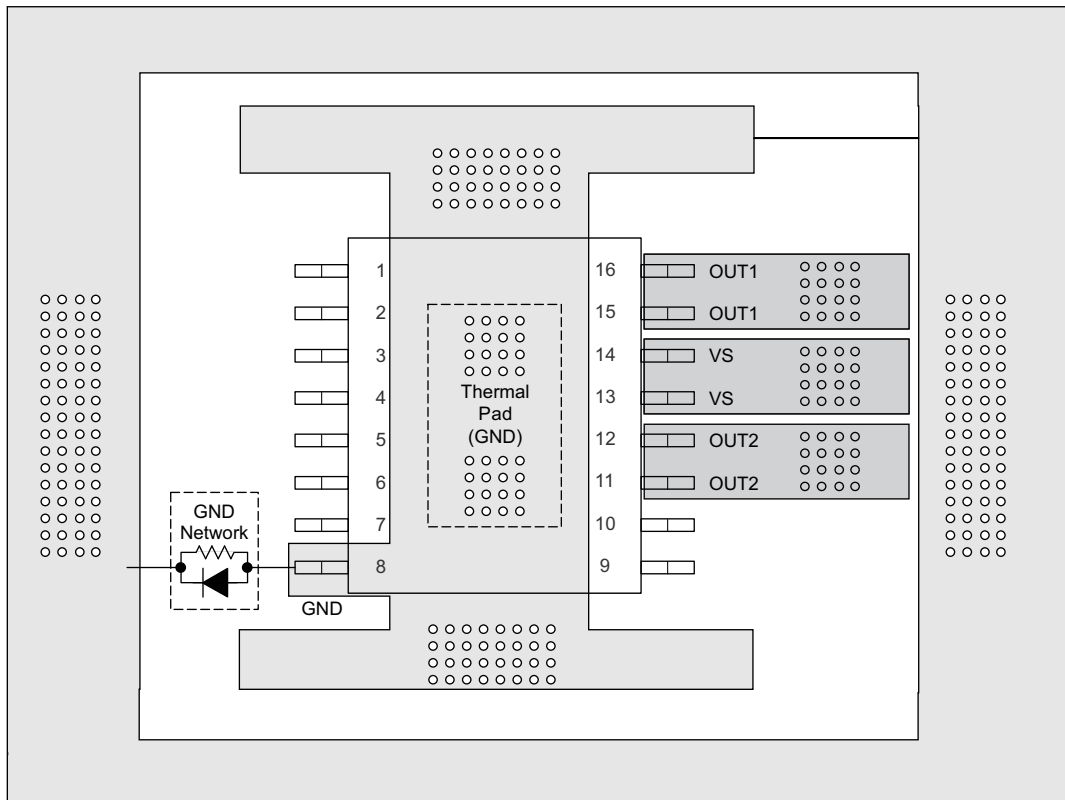


**Figure 45. Layout Example Without a GND Network**

## Layout Examples (continued)

### 11.2.2 With a GND Network

With a GND network, tie the thermal pad as one trace to the board GND copper.



**Figure 46. Layout Example With a GND Network**



## 12 器件和文档支持

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.3 商标

PowerPAD, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查看左侧的导航面板。

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS2H000AQPWPRQ1</a>	Active	Production	HTSSOP (PWP)   16	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2H000AQ
TPS2H000AQPWPRQ1.A	Active	Production	HTSSOP (PWP)   16	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2H000AQ
<a href="#">TPS2H000BQPWPRQ1</a>	Active	Production	HTSSOP (PWP)   16	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2H000BQ
TPS2H000BQPWPRQ1.A	Active	Production	HTSSOP (PWP)   16	2000   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	2H000BQ

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

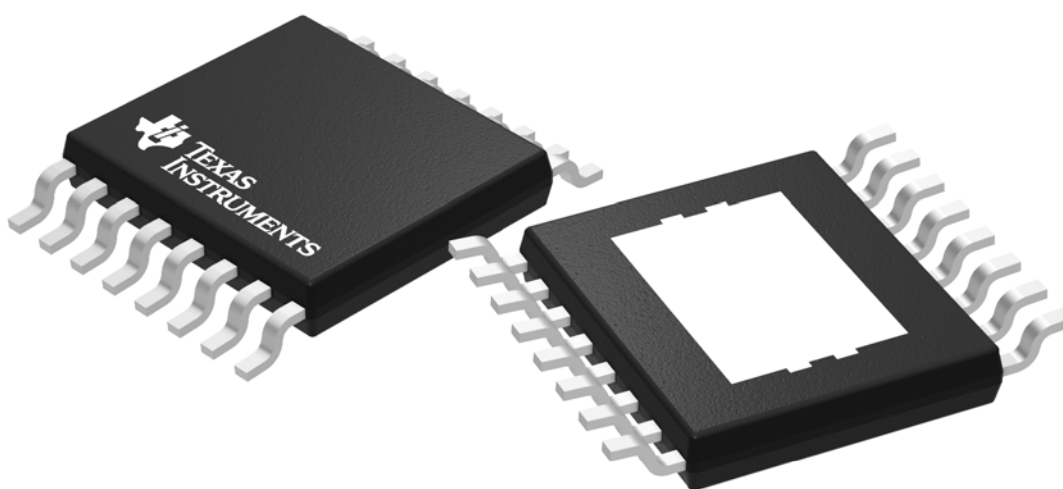
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2H000AQPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS2H000BQPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS



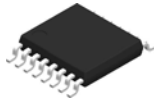
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2H000AQPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS2H000BQPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

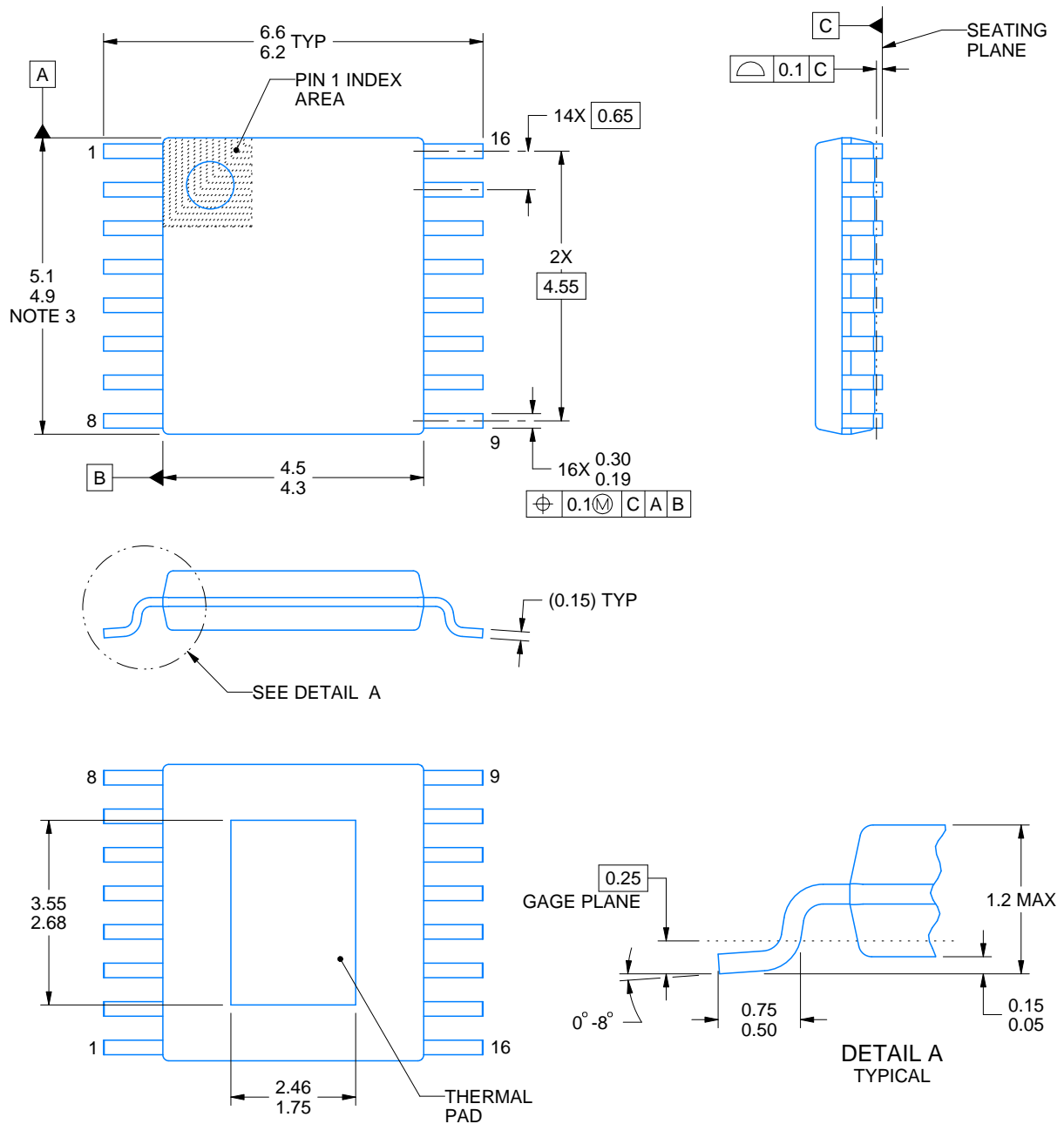
PWP0016J



# PACKAGE OUTLINE

## PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4223595/A 03/2017

### NOTES:

PowerPAD is a trademark of Texas Instruments.

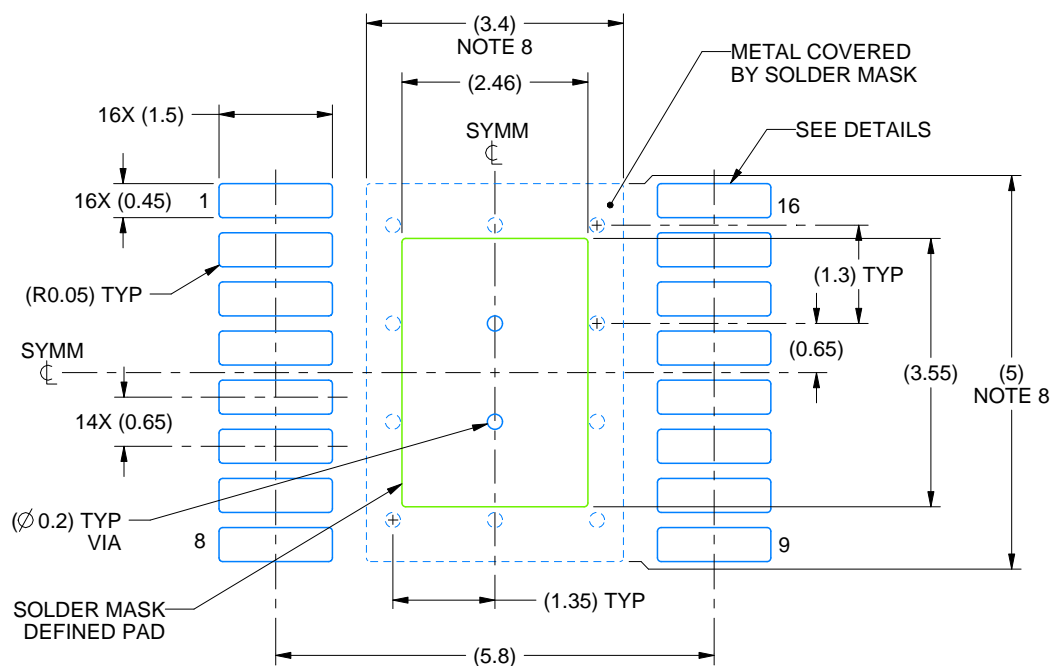
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

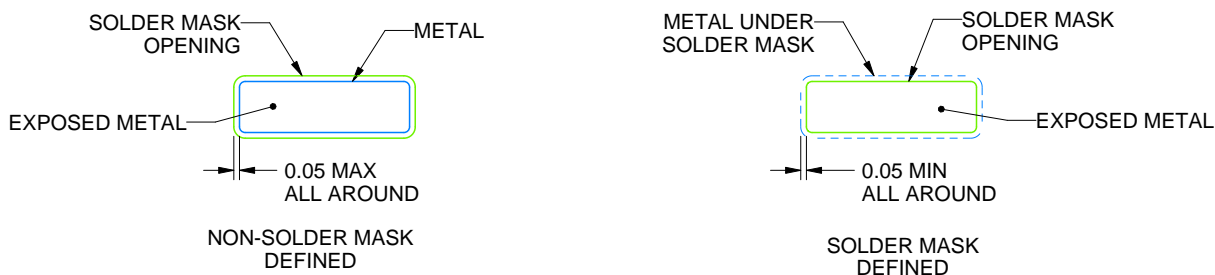
PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

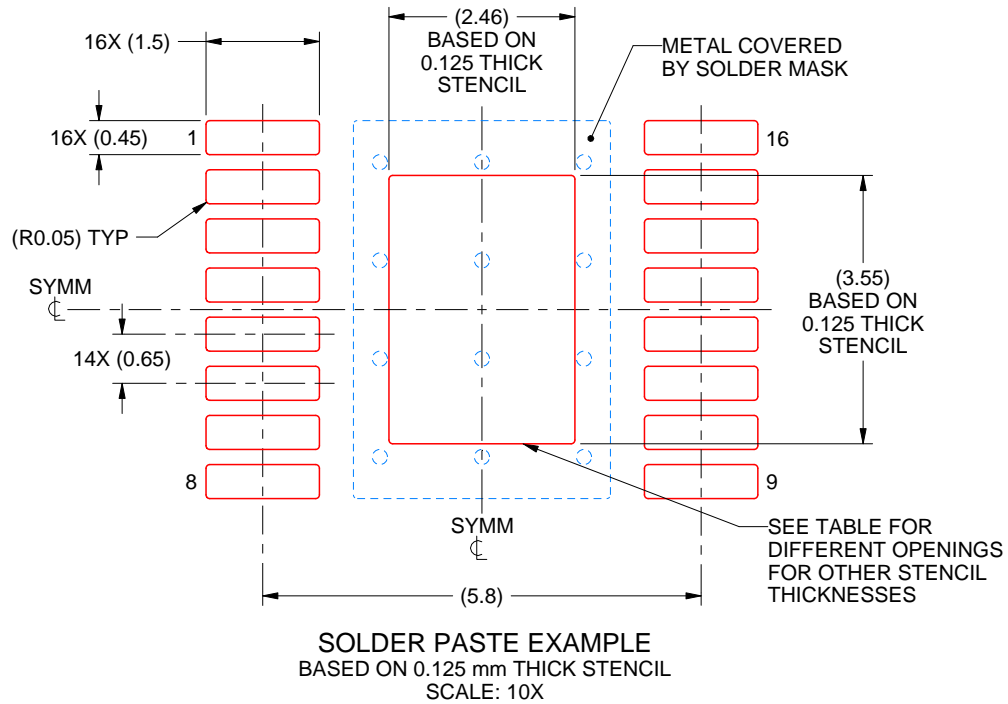
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.



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