TPS25961 具有可调节电流限值和短路保护功能的 2.7V 至 19V、106mΩ 电子保险丝

1 特性

- 宽输入电压范围：2.7V 至 19V
  - 绝对最大值为 21V
- 低导通电阻：Ron = 106mΩ（典型值）
- 具有可调节欠压锁定 (UVLO) 功能的高电平有效使能输入
- 快速过压保护钳位，响应时间为 1.3µs（典型值）
  - 固定内部阈值：5.98 V（典型值）
  - 可使用外部电阻分压器调节阈值
- 过流保护：
  - 可调节电流限制阈值：0.1A 至 2A
  - 电流限制准确度：
    - 整个电流范围内为 ±20%（典型值）
    - 1.45A 电流限值下为 ±18%（最大值），T_A = 25°C
- 短路保护，响应时间为 5µs（典型值）
- 输出压摆率控制 (dVdt)：5.17 V/ms（典型值）
- 提供过热保护 (OTP)
- 故障后自动重试
- 低静态电流：130µA（典型值）
- UL2367 认证（正在申请中）
- IEC 62368 CB 认证（正在申请中）
- 小尺寸：2mm × 2mm SON 封装

2 应用

- 适配器输入保护
- 能量计
- 智能扬声器
- 无线耳塞充电器
- 机顶盒
- IP 网络摄像头

3 说明

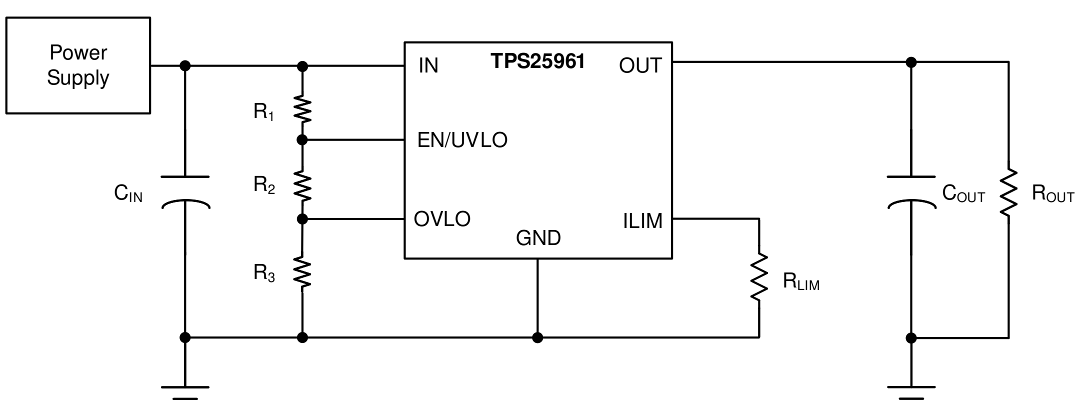
TPS25961 *电子保险丝*（集成式 FET 热插拔器件）是采用小型封装且高度集成的电路保护和电源管理解决方案。此类器件只需很少的外部元件即可提供多种保护模式，能够非常有效地抵御过载、短路、电压浪涌和过多浪涌电流。输出电流限制级别可通过单个外部电阻设定。浪涌电流在内部使用输出转换率控制进行管理。为了保护输入过压情况，该器件提供了一个选项，可以在外部设置用户定义的过压截止阈值或使用固定内部阈值。

这些器件的额定工作结温范围为 –40°C 至 +125°C。

器件信息

器件型号(1)	封装	封装尺寸（标称值）
TPS25961DRV	SON (6)	2.00mm × 2.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
December 2022	*	Initial Release

5 Pin Configuration and Functions

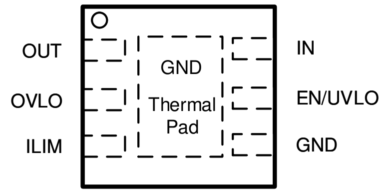


图 5-1. DRV Package, 6-Pin SON (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	Power	Power output.
OVLO	2	Analog Input	An external resistor divider from supply rail can be used to adjust the overvoltage lockout threshold. Connect to GND directly to use internal fixed overvoltage lockout threshold. **Do not leave floating.**
ILIM	3	Analog Output	An external resistor from this pin to GND sets the output current limit threshold. Leave it open to set the current limit threshold to minimum value.
GND	4	Ground	Connect to system electrical ground.
EN/UVLO	5	Analog Input	Active High Enable for the device. A resistor divider from supply rail can be used to adjust the undervoltage lockout threshold. **Do not leave floating.**
IN	6	Power	Power input.
GND	PAD	Thermal/ Ground	The exposed pad is used primarily for heat dissipation and must be connected to GND plane on the PCB.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range, –40℃ ≤ T_J ≤ 125℃	IN	–0.3	21	V
V_{OUT}	Maximum output voltage range, –40℃ ≤ T_J ≤ 125℃	OUT	–0.3	V_{IN} + 0.3	
$V_{EN/UVLO}$	Maximum EN/UVLO pin voltage range	EN/UVLO	–0.3	20	V
V_{OV}	Maximum OVLO pin voltage range	OVLO	–0.3	6.5	V
V_{ILIM}	Maximum ILIM pin voltage range	ILIM	Internally limited		V
I_{MAX}	Maximum continuous switch current	IN to OUT	Internally limited		A
T_J	Junction temperature		Internally limited		°C
T_{LEAD}	Maximum lead temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input voltage range	IN	2.7	19	V
V_{OUT}	Output voltage range	OUT		V_{IN}	V
$V_{EN/UVLO}$	EN/UVLO pin voltage range	EN/UVLO		5[(1)]	V
V_{OV}	OVLO pin voltage range	OVLO	0.5	1.5	V
R_{ILIM}	ILIM pin resistance to GND	ILIM	25		kΩ
I_{MAX}	Continuous switch current, T_J ≤ 125℃	IN to OUT		2	A
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V , it is recommended to use a resistor divider with minimum pull-up resistor value of 350 kΩ.

6.4 Thermal Information

THERMAL METRIC [(1)] [(2)]		TPS25961 DRV (SON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.1	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	80.4	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	16.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	38.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p)

6.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 1 V, ILIM = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$I_{Q(ON)}$	IN supply quiescent current		130	165	µA
$I_{Q(OFF)}$	IN supply OFF state current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		144	230	µA
I_{SD}	IN supply shutdown current (V_{EN} < $V_{SD(F)}$)		0.6	1.5	µA
$V_{UVP(R)}$	IN supply UVP rising threshold	2.46	2.54	2.61	V
$V_{UVP(F)}$	IN supply UVP falling threshold	2.31	2.42	2.54	V
$V_{OVP(R)}$	VIN fixed overvoltage rising threshold, OVLO = GND, T_J = 25℃	5.55	5.98	6.5	V
V_{OVPHys}	VIN fixed overvoltage hysteresis, OVLO = GND	85	111	135	mV
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Overcurrent threshold, ILIM = Open, T_J = 25℃		0.116		A
	Overcurrent threshold, R_{ILIM} = 250 kΩ, T_J = 25℃		0.212		A
	Overcurrent threshold, R_{ILIM} = 100 kΩ, T_J = 25℃		0.516		A
	Overcurrent threshold, R_{ILIM} = 62.5 kΩ, T_J = 25℃		0.856		A
	Overcurrent threshold, R_{ILIM} = 34.48 kΩ, T_J = 25℃	1.189	1.45	1.711	A
	Overcurrent threshold, R_{ILIM} = 25 kΩ, T_J = 25℃		2.36		A
I_{SC}	Fast-trip threshold		8.25		A
ON RESISTANCE (IN - OUT)					
R_{ON}	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 1 A, R_{ILIM} = 34.48 kΩ		132	240	mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 1 A, R_{ILIM} = 34.48 kΩ		106	177	mΩ
	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 0.1 A, R_{ILIM} = 100 kΩ, T_J = 25℃		243		mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 0.1 A, R_{ILIM} = 100 kΩ, T_J = 25℃		195		mΩ
	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 0.1 A, R_{ILIM} = 250 kΩ, T_J = 25℃		455		mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 0.1 A, R_{ILIM} = 250 kΩ, T_J = 25℃		367		mΩ
	2.7 ≤ V_{IN} < 4.5 V, I_{OUT} = 0.05 A, ILIM = Open, T_J = 25℃		833		mΩ
	4.5 ≤ V_{IN} ≤ 19 V, I_{OUT} = 0.05 A, ILIM = Open, T_J = 25℃		702		mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO rising threshold	1.2	1.24	1.27	V
$V_{UVLO(F)}$	EN/UVLO falling threshold	1.1	1.132	1.16	V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current	0.6			V
I_{ENLKG}	EN/UVLO pin leakage current	-0.1		0.1	µA
OVERVOLTAGE LOCKOUT (OVLO)					
$V_{OVLO(R)}$	OVLO rising threshold	1.2	1.24	1.27	V
$V_{OVLO(F)}$	OVLO falling threshold	1.1	1.13	1.161	V
I_{OVLKG}	OVLO pin leakage current	-0.1		0.1	µA
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown rising threshold, T_J ↑		170		°C
TSD_{HYS}	Thermal Shutdown hysteresis, T_J ↓		30		°C

6.6 Timing Requirements

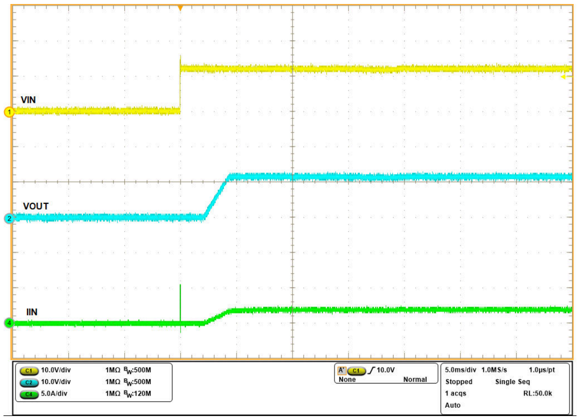
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	$V_{OVLO} > V_{OV(R)}$ to $V_{OUT} \downarrow$		1.3		µs
t_{LIM}	Current limit response time	$I_{OUT} > 1.5 \times I_{LIM}$ to I_{OUT} within 5% of I_{LIM}		30		µs
t_{SC}	Short-circuit response time	$I_{OUT} > I_{SC}$ to output current cut off		5		µs
$t_{TSD,RST}$	Thermal Shutdown auto-retry Interval	Device enabled and T_J < TSD – TSD_{HYS}		110		ms

6.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF.

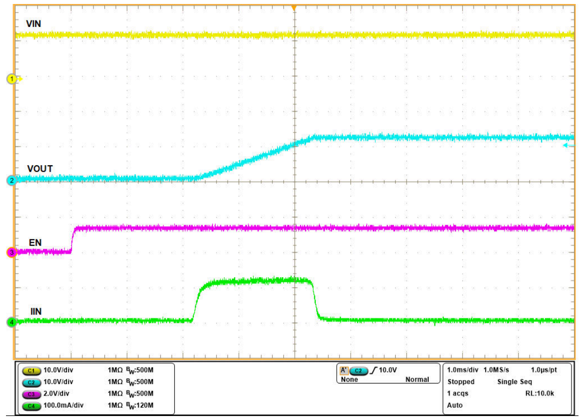
PARAMETER		V_{IN}	Typ	UNITS
SR_{ON}	Output rising slew rate	3.3 V	4.43	V/ms
		12 V	5.17	
		18 V	5.19	
$t_{D,ON}$	Turn on delay	3.3 V	2.14	ms
		12 V	2.37	
		18 V	2.50	
t_R	Rise time	3.3 V	0.58	ms
		12 V	1.83	
		18 V	2.67	
t_{ON}	Turn on time	3.3 V	2.71	ms
		12 V	4.2	
		18 V	5.17	
$t_{D,OFF}$	Turn off delay	3.3 V	15.00	µs
		12 V	14.22	
		18 V	12.44	

6.8 典型特性



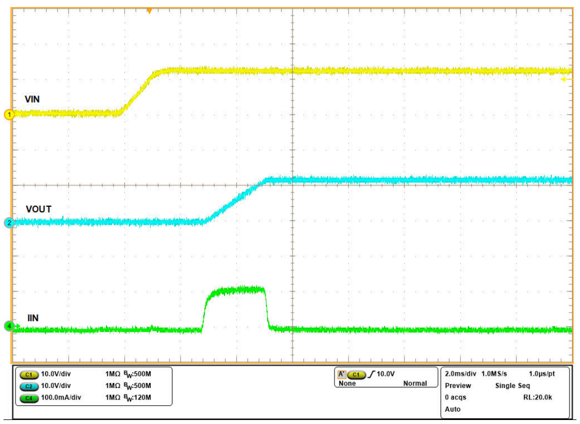
C_{OUT} = 22µF，R_{OUT} = 6Ω，IN 热插拔至 12V

图 **6-1.** 输入热插拔响应



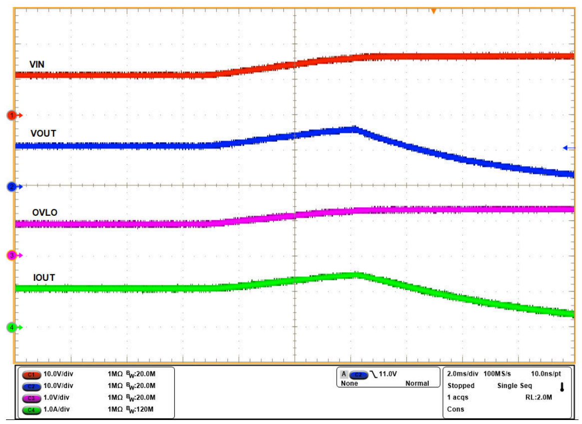
V_{IN} = 12V，C_{OUT} = 22µF，EN 引脚从 0V 升压至 1.5V

图 **6-2.** 通过使能引脚上电



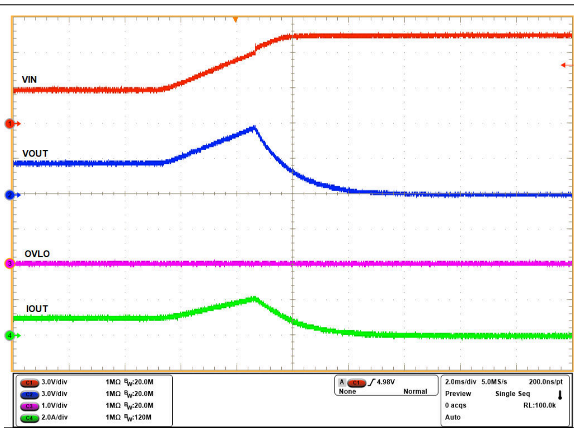
C_{OUT} = 22µF，EN 引脚保持高电平，V_{IN} 上升至 12V

图 **6-3.** 通过输入电源上电



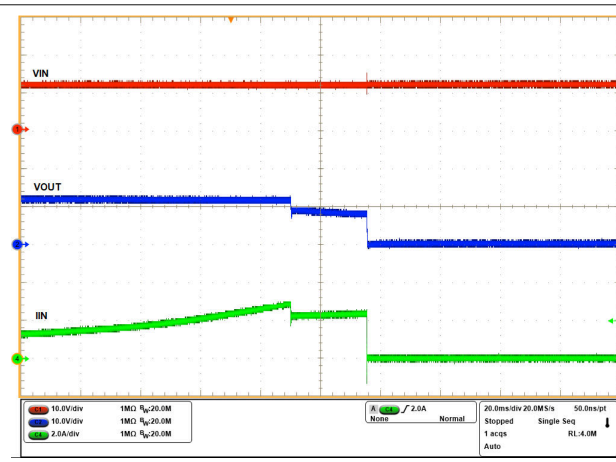
OVLO 阈值使用从 VIN 到 GND 的电阻梯设置为 16V，C_{OUT} = 470µF，R_{OUT} = 12Ω，V_{IN} 从 10V 增加到 17V

图 **6-4.** 过压锁定响应 - 可调节阈值



OVLO 引脚短接到 GND，C_{OUT} = 470µF，R_{OUT} = 3.3Ω，V_{IN} 从 2.7V 增加到 7.5V

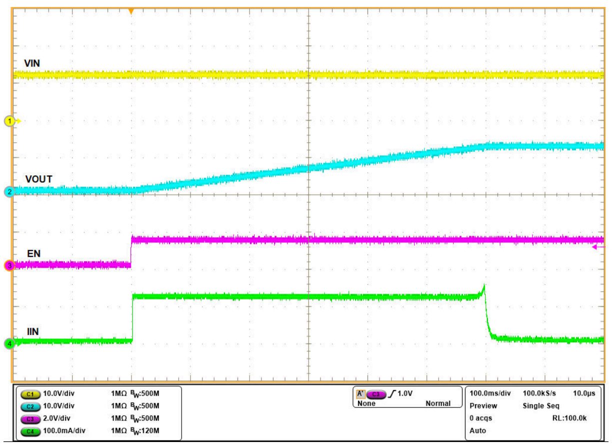
图 **6-5.** 过压锁定响应 - 内部固定阈值



V_{IN} = 12V，R_{ILIM} = 25kΩ，负载电流逐渐上升至 2.5A 以上

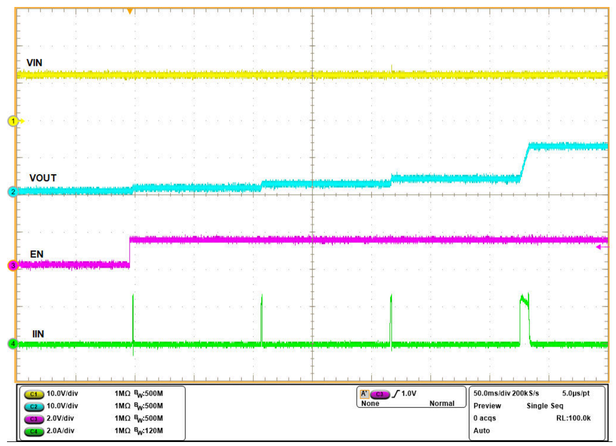
图 **6-6.** 电流限制后跟热关断

6.8 典型特性 (continued)



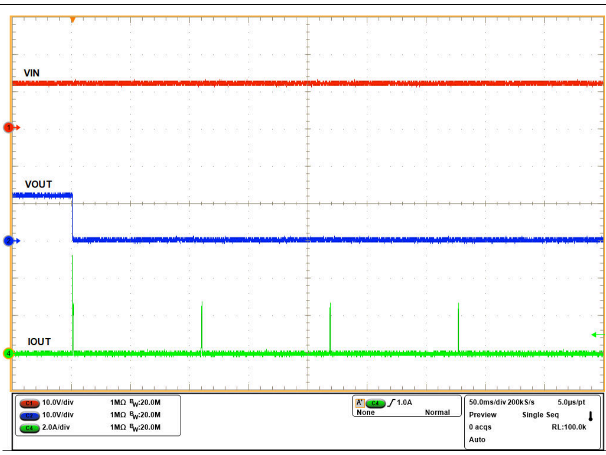
V_{IN} = 12V，C_{OUT} = 6400 µ F，R_{OUT} = 开路，R_{ILIM} = 开路，EN 引脚从低电平切换至高电平

图 6-7. 使用低电流限制设置为大电容器充电



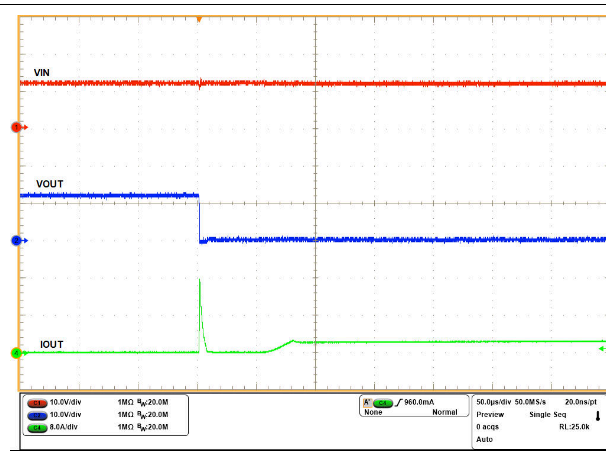
V_{IN} = 12V，C_{OUT} = 2200 µ F，R_{OUT} = 开路，R_{ILIM} = 25k Ω ，EN 引脚从低电平切换至高电平

图 6-8. 使用高电流限制设置为大电容器充电 - 断续模式



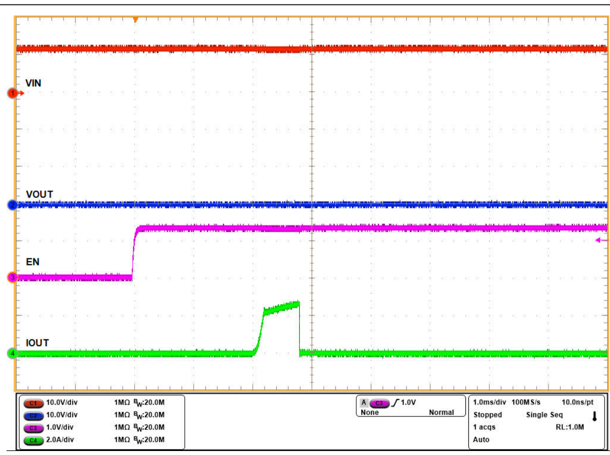
V_{IN} = 12V，R_{ILM} = 25k Ω ，OUT 引脚短接至 GND

图 6-9. 导通时输出短路



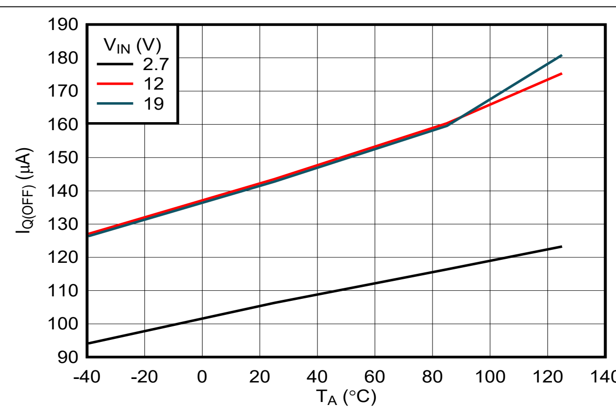
V_{IN} = 12V，R_{ILM} = 25k Ω ，OUT 引脚短接至 GND

图 6-10. 导通时短路（放大图）



V_{IN} = 12V，R_{ILM} = 25k Ω ，EN 引脚从低电平切换到高电平，OUT 引脚短接至 GND

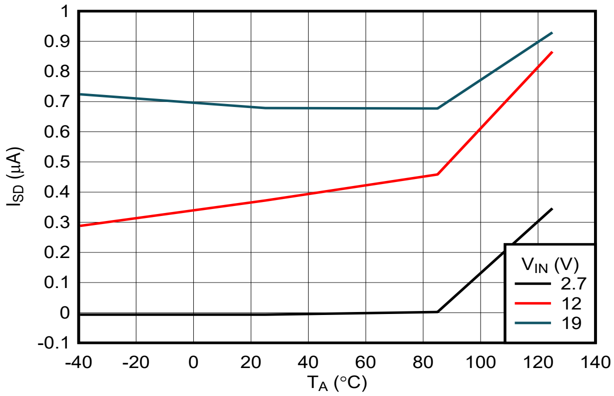
图 6-11. 上电至短路



EN/UVLO 引脚电压 > $V_{UVLO(R)}$

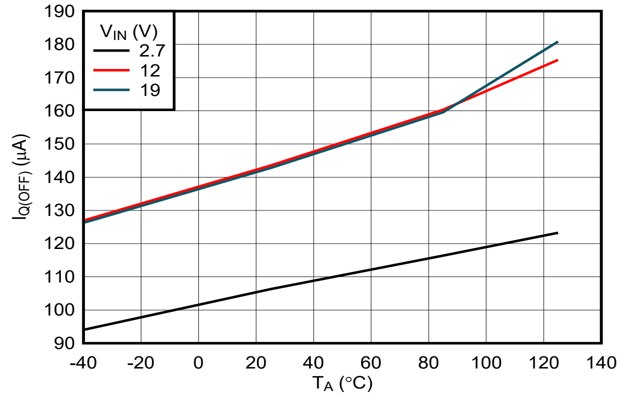
图 6-12. 稳态静态电流与温度间的关系

6.8 典型特性 (continued)



EN/UVLO 引脚电压 < $V_{SD(F)}$

图 6-13. 关断电流与温度间的关系



$V_{SD(F)}$ < EN/UVLO 引脚电压 < $V_{UVLO(F)}$

图 6-14. 关断状态电流与温度间的关系

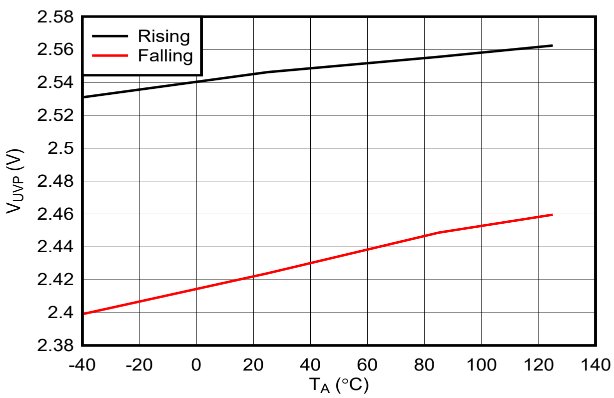


图 6-15. IN 电源欠压阈值与温度间的关系

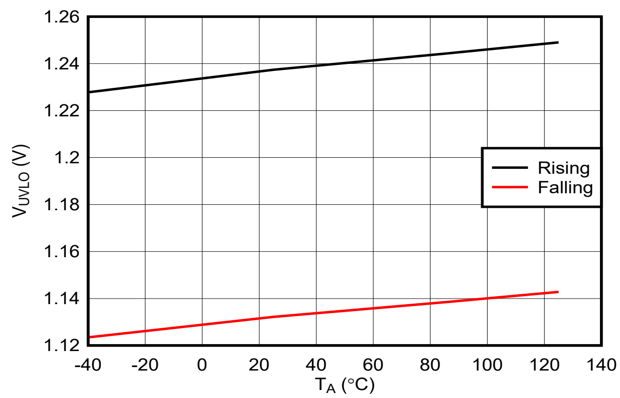


图 6-16. FET 开/关控制的 **EN/UVLO** 引脚阈值与温度间的关系

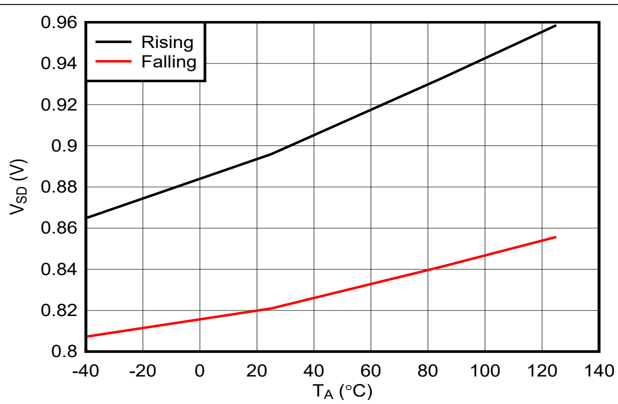


图 6-17. 最低关断电流的 **EN/UVLO** 引脚阈值与温度间的关系

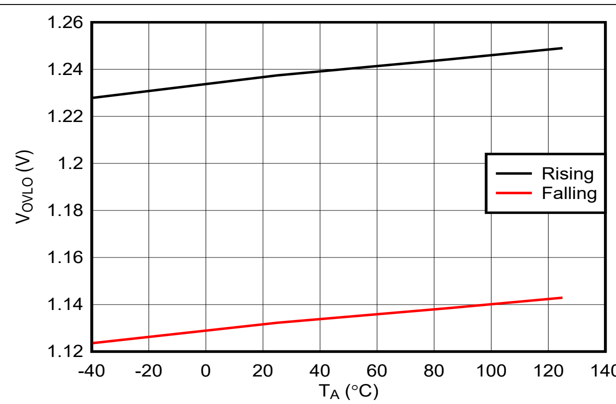


图 6-18. OVLO 引脚阈值与温度间的关系

6.8 典型特性 (continued)

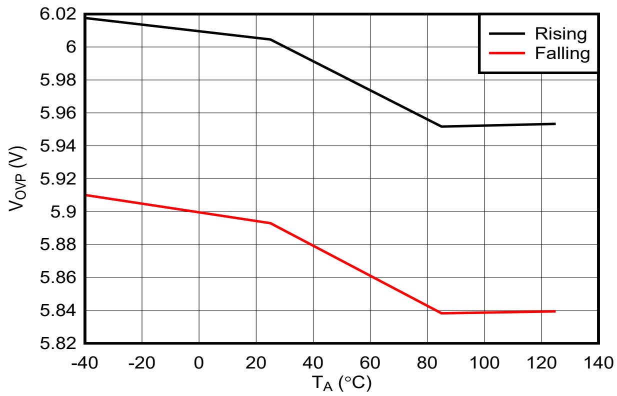
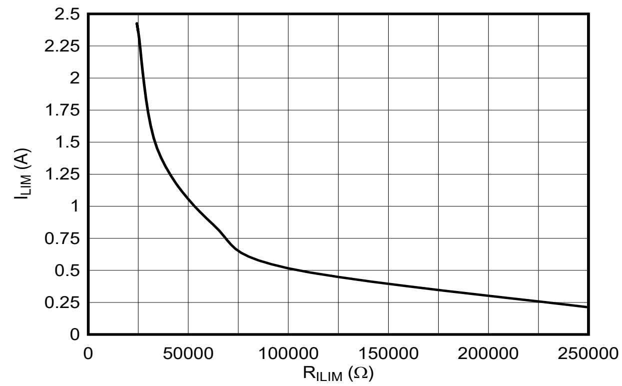
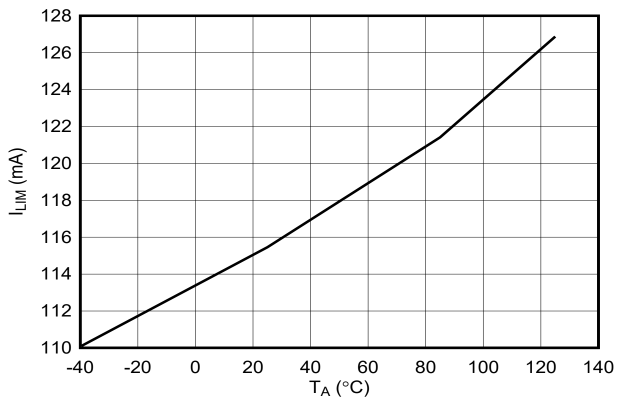


图 **6-19.** 内部固定过压阈值与温度间的关系



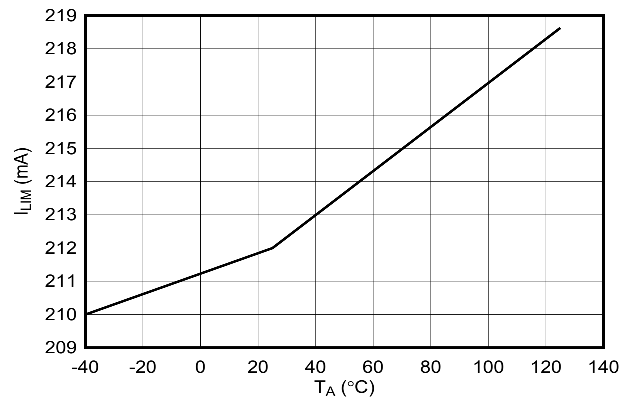
适用于 I_{LIM} > 0.2A，请参阅此部分了解更多注意事项。

图 **6-20.** 电流限制阈值与 **ILIM** 电阻器间的关系



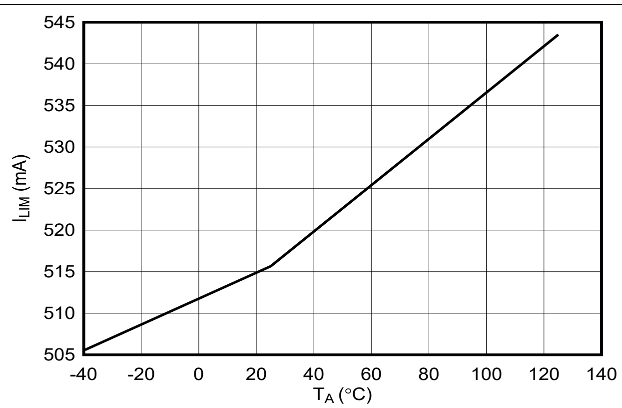
ILIM 引脚开路

图 **6-21.** 电流限制阈值与温度间的关系



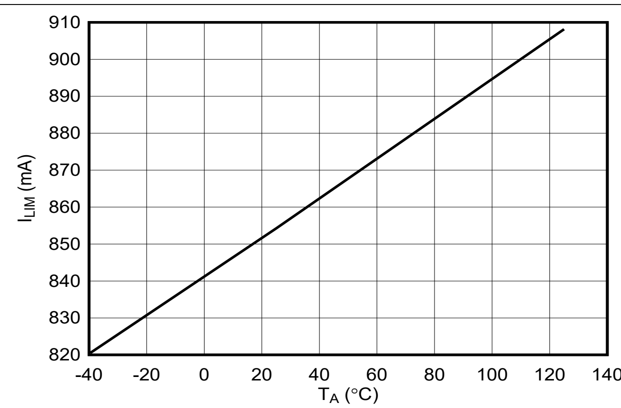
R_{ILIM} = 250kΩ

图 **6-22.** 电流限制阈值与温度间的关系



R_{ILIM} = 100kΩ

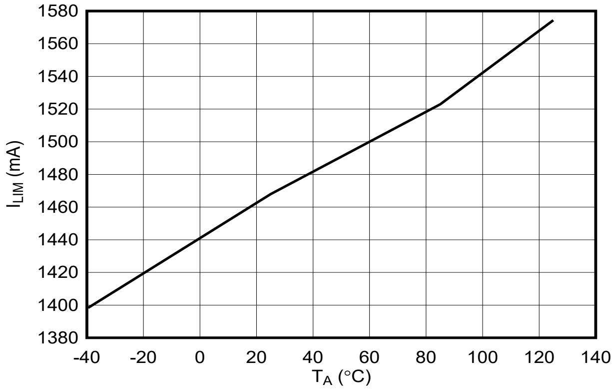
图 **6-23.** 电流限制阈值与温度间的关系



R_{ILIM} = 62.5kΩ

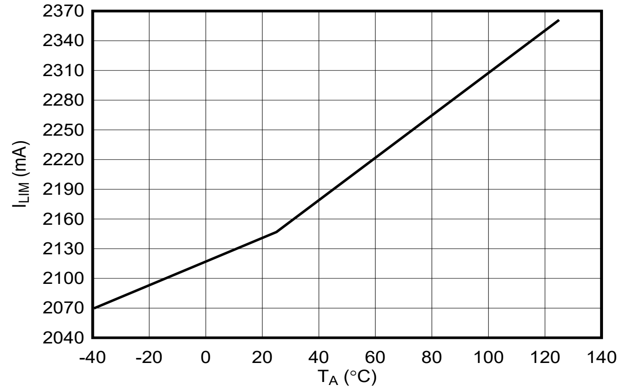
图 **6-24.** 电流限制阈值与温度间的关系

6.8 典型特性 (continued)



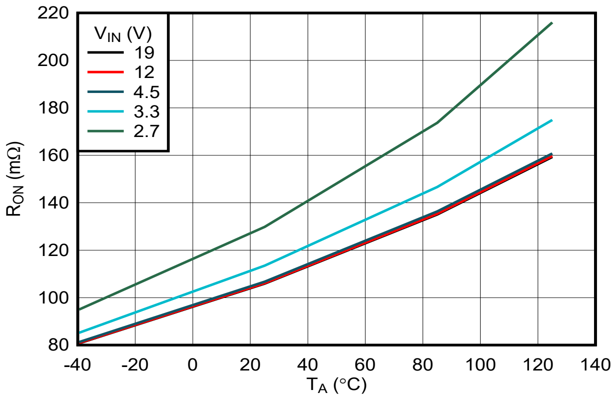
R_{ILIM} = 34.48k Ω

图 **6-25.** 电流限制阈值与温度间的关系



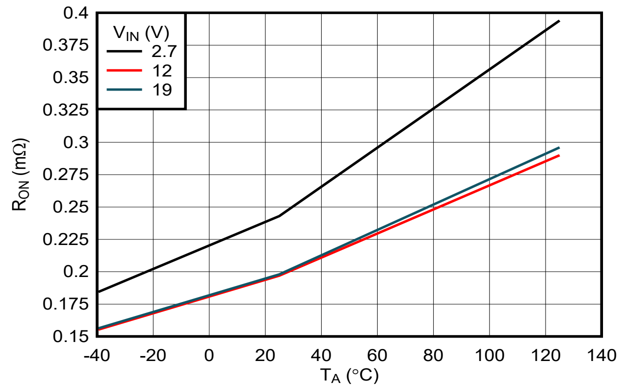
R_{ILIM} = 25k Ω

图 **6-26.** 电流限制阈值与温度间的关系



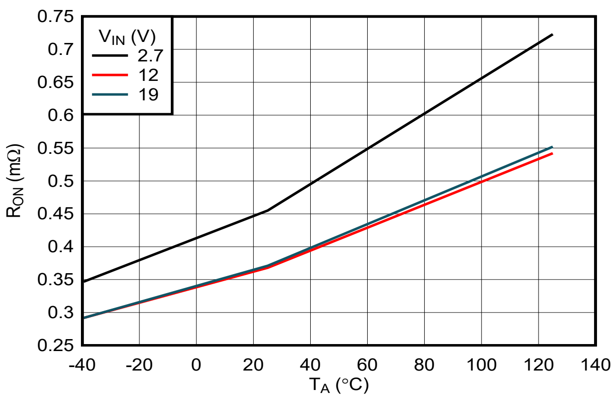
R_{ILIM} < 58.8k Ω

图 **6-27.** 导通电阻与温度间的关系



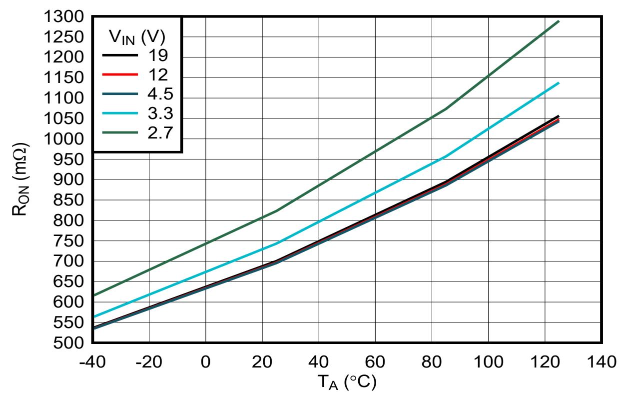
66.7k Ω < R_{ILIM} < 111k Ω

图 **6-28.** 导通电阻与温度间的关系



142k Ω < R_{ILIM} < 250k Ω

图 **6-29.** 导通电阻与温度间的关系



R_{ILIM} > 500k Ω

图 **6-30.** 导通电阻与温度间的关系

6.8 典型特性 (continued)

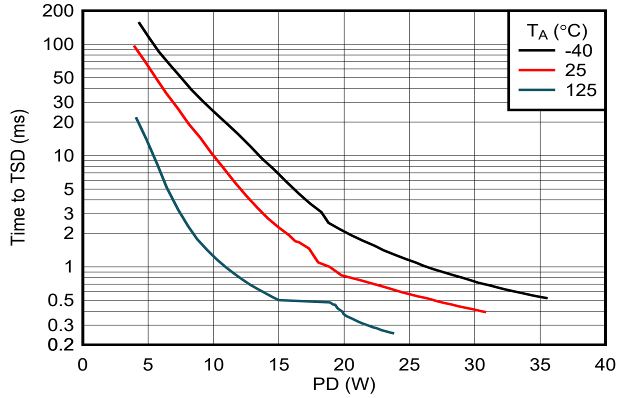


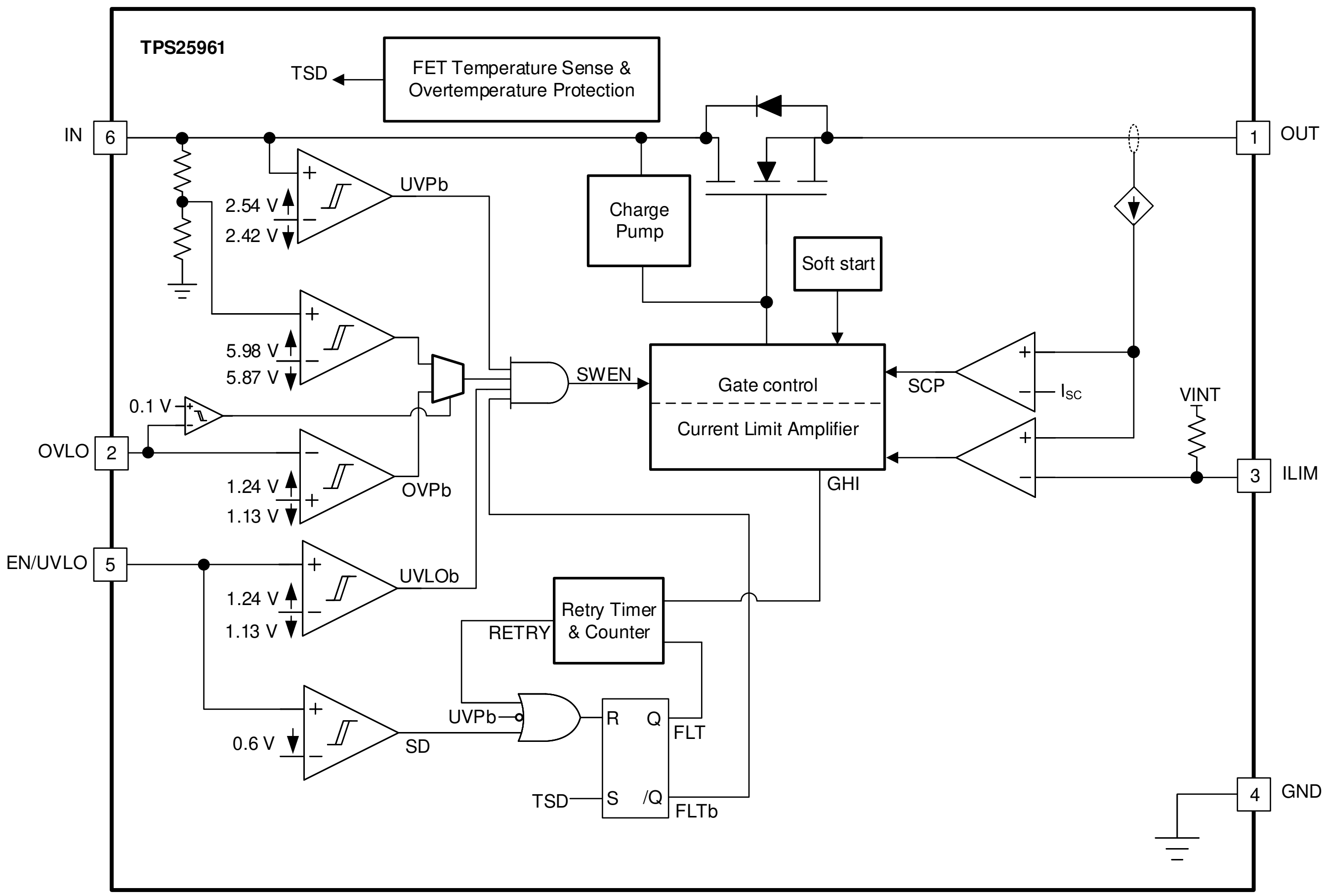
图 **6-31.** 热关断时间与功率耗散间的关系

7 Detailed Description

7.1 Overview

The TPS25961 is an integrated eFuse device that is used to manage load voltage and load current. The device provides various factory programmed settings and user manageable settings, which allow device configuration for handling different transient and steady state supply and load fault conditions, thereby protecting the input supply and the downstream circuits connected to the device. The device also uses an in-built thermal shutdown mechanism to protect itself during these fault events.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 欠压保护 (UVP) 和欠压锁定 (UVLO)

TPS25961 持续监控输入电源，以确保仅当电压处于足够的水平时才为负载加电。在启动条件期间，器件会等待输入电源上升到高于内部固定阈值 $V_{UVP(R)}$，然后再继续开启 FET。同样，在导通条件下，如果输入电源低于 UVP 阈值 $V_{UVP(F)}$，FET 将关闭。UVP 上升和下降阈值略有不同，从而提供一些迟滞并确保在阈值电压附近稳定运行。

TPS25961 还提供用户可调节的 UVLO 机制，以确保仅当电压达到特定系统要求的足够水平时才为负载上电。这可以通过对输入电源进行分频并将其馈送到 EN/UVLO 引脚来实现。每当 EN/UVLO 引脚上的电压降至阈值 $V_{UVLO(F)}$ 以下时，器件都会关断 FET。当电压上升到阈值 $V_{UVLO(R)}$ 以上时，FET 再次导通。该引脚上的上升和下降阈值略有不同，从而提供一些迟滞并确保在阈值电压附近稳定运行。

用户必须适当地选择电阻分压器值，以将所需的输入欠压电平映射到器件的 UVLO 阈值。

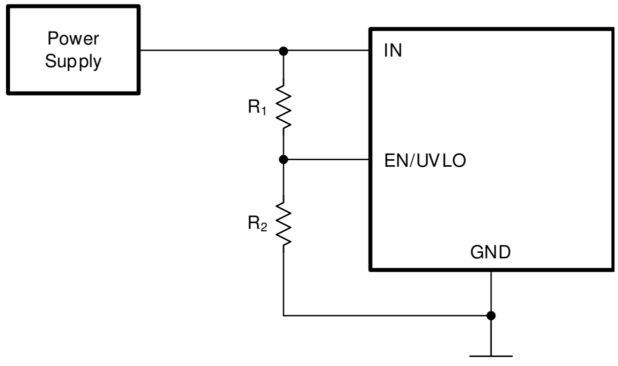


图 7-1. 可调节欠压锁定

下面的公式显示了用于设置给定电压电源的 UVLO 设置点的电阻分压器值的计算结果。

$$\mathrm{VIN(UV)} = \mathrm{VUVLO(F)} \times \frac{\mathrm{R1} + \mathrm{R2}}{\mathrm{R2}} \quad (1)$$

7.3.2 Overvoltage Protection

The TPS25961 implements Overvoltage Protection on V_{IN} in case the applied voltage becomes too high for the system or device to properly operate. The Overvoltage Protection has a default lockout threshold of V_{OVP} **,** which is achieved by connecting the OVLO pin to GND.

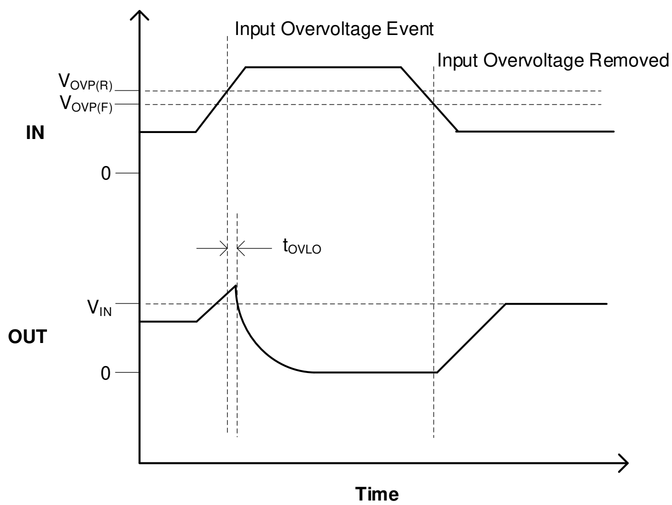


图 7-2. TPS25961 Fixed Overvoltage Lockout Response

It’s possible to override the default OVLO threshold and adjust it to an user defined value as per the system requirements. This can be achieved by dividing the input supply and feeding it to the OVLO pin. Whenever the voltage at the OVLO pin rises above a threshold $V_{OVLO(R)}$, the device turns OFF the FET. When the voltage at the OVLO pin falls below the threshold $V_{OVLO(F)}$, the FET is turned ON again. The rising and falling thresholds on this pin are slightly different, thereby providing some hysteresis and ensuring stable operation around the threshold voltage.

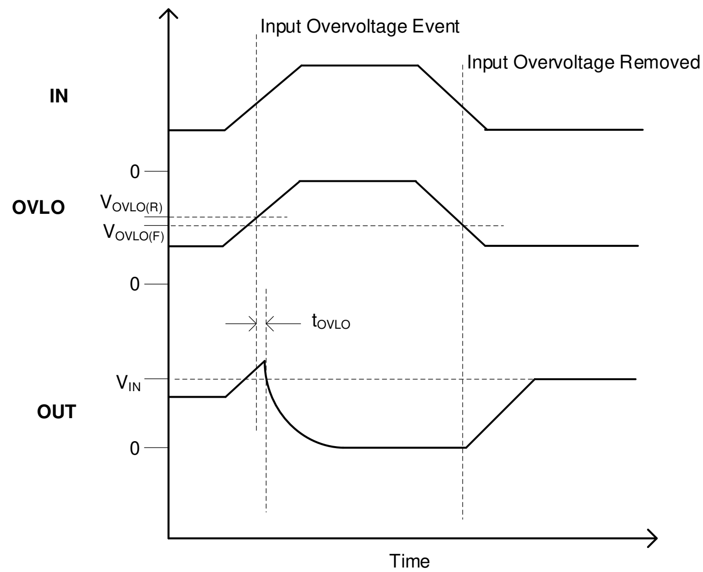


图 7-3. TPS25961 Adjustable Overvoltage Lockout Response

The user should choose the resistor divider values appropriately to map the desired input overvoltage level to the OVLO threshold of the part.

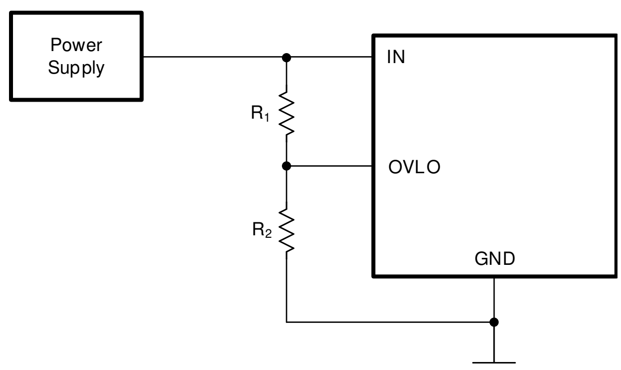


图 7-4. TPS25961 Adjustable Overvoltage Lockout

The equation below shows the calculations for the resistor divider values to be used to set the OVLO set-point for a given voltage supply.

$$VIN(OV) = VOVLO(F) \times \frac{R1 + R2}{R2} \quad (2)$$

7.3.3 Inrush Current, Overcurrent and Short Circuit Protection

The TPS25961 incorporates three levels of protection against overcurrent:

- Fixed slew rate for inrush current control (dVdt)
- Active current limiting with adjustable limit (I_{LIM}) for overcurrent protection
- Fast short-circuit response to protect against hard short-circuits

7.3.3.1 Slew Rate and Inrush Current Control (dVdt)

The inrush current during turn on is directly proportional to the load capacitance and rising slew rate.

$$IINRUSH = COUT \times SRON \quad (3)$$

TPS25961 provides a controlled turn on at a fixed slew rate (SR_{ON}) which helps to minimize the inrush current.

7.3.3.2 Active Current Limiting

The device responds to output overcurrent conditions by actively limiting the current.

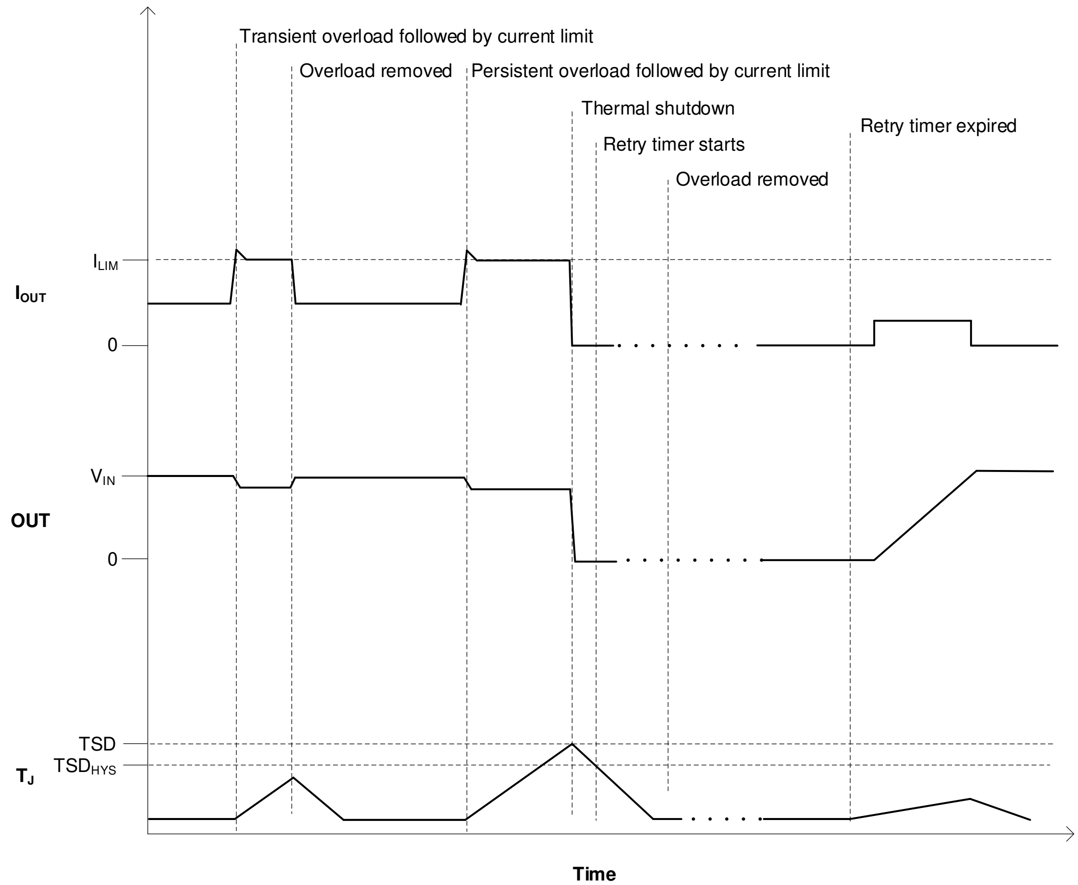


图 7-5. TPS25961 Overcurrent Response

In the current limiting state, the output voltage drops resulting in increased power dissipation in the internal FET leading to thermal shutdown if the condition persists for an extended period of time. In this case, the device performs 3 auto-retry attempts to allow the system to recover and then latches-off if the fault persists. See *Fault response* section for more details on device response after a fault.

The current limit threshold can be adjusted by pinstrapping the ILIM pin.

Use equation below to calculate the R_{ILIM} value for overcurrent thresholds < 200 mA.

$$\mathrm{RILIM} = \frac{50000}{\mathrm{ILIM} - 0.000002} \quad (4)$$

Use equation below to calculate the R_{ILIM} value for overcurrent thresholds ⩾ 200 mA.

$$\mathrm{RILIM} = \frac{50000}{\mathrm{ILIM}} \quad (5)$$

备注

1. Leaving the ILIM pin open sets the current limit to its minimum value.
2. The device scales the FET ON resistance in discrete steps according to the R_{ILIM} setting to provide optimum performance for the desired current level. At higher I_{LIM} settings, the ON resistance is lower and at lower I_{LIM} settings, the ON resistance is higher. However, for certain R_{ILIM} resistor values, the device may select an incorrect ON resistance scaling which is too high for the target load current leading to excessive voltage drop and power dissipation. To avoid this situation, it's recommended to avoid certain R_{ILIM} values as per 表 7-1.

表 7-1. R_{ILIM} Values to Avoid

ILIM Resistor Value	Device ON Resistance
250 kΩ < R_{ILIM} < 500 kΩ	Undefined
111 kΩ < R_{ILIM} < 142 kΩ	Undefined
58.8 kΩ < R_{ILIM} < 66.7 kΩ	Undefined

7.3.3.3 Short-Circuit Protection

The current through the device increases very rapidly during an output short-circuit event. In this event, the device engages a fast current clamping circuit to regulate down the current faster (t_{SCP}) as compared to the nominal overcurrent response time (t_{LIM}). Instead of completely turning off the power FET, the device tries to actively limit the current to ensure uninterrupted power in the event of transient overcurrents or supply transients. The device stops limiting the current once the load current falls below the programmed I_{LIM} threshold.

The output voltage drops in the current limiting state, resulting in increased power dissipation in the internal FET and might lead to thermal shutdown if the condition persists for an extended period of time. In this case, the device performs 3 auto-retry attempts to allow the system to recover and then latches-off if the fault persists. See *Fault response* section for more details on device response after a fault.

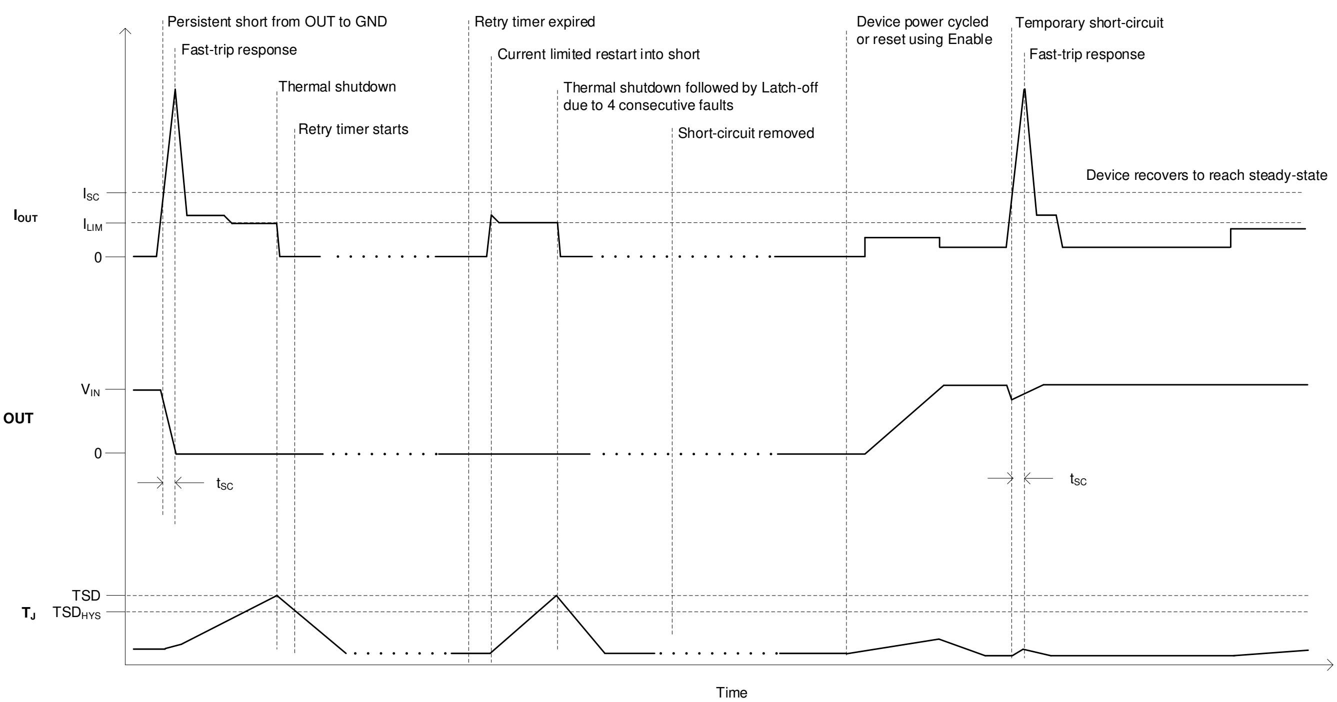


图 7-6. TPS25961 Short Circuit Response

7.3.4 Overtemperature Protection (OTP)

Thermal Shutdown occurs when the junction temperature (T_J) exceeds the thermal shutdown threshold (TSD). When the TPS25961 detects thermal overload, it shut downs and remains off until it has cooled down sufficiently. Once the TPS25961 junction has cooled down below TSD - TSD_{HYS}, it remains off for an additional delay of $t_{TSD,RST}$ after which it automatically retries to turn on. The device performs 3 auto-retry attempts to allow the system to recover before it latches-off if the fault persists. See *Fault response* section for more details on device response after a fault.

表 7-2. TPS25961 Thermal Shutdown

Enter TSD	Exit TSD
$T_J \geqslant$ TSD	T_J < TSD - TSD_{HYS} and $t_{TSD,RST}$ timer expired

7.3.5 Fault Response

表 7-3 summarizes the protection response to various fault conditions.

表 7-3. Fault Response

Event / Fault	Protection Response	Fault Latched Internally
Steady-state	N/A	N/A
Overtemperature	Shutdown	Yes
Undervoltage	Cut-off	No
Overvoltage	Cut-off	No
Overcurrent	Current Limit	No
Short-circuit	Current Limit	No

Once the device turns off due to a latched fault, power cycling the part or pulling the EN/UVLO pin voltage below $V_{SD(F)}$ clears the fault. Pulling the EN/UVLO just below the UVLO threshold has no impact on the device in this condition.

At the end of the $t_{TSD,RST}$ timer after a latched fault, the device will attempt to automatically restart 3 times. If the fault was caused by a transient condition which goes away and the device is able to recover and reach steady state, it clears the fault counter.

If the fault is persistent, the device will eventually shut down completely after 3 attempts and then remain latched-off till it's power cycled.

7.4 Device Functional Modes

The features of the device depend on the operating mode.

表 7-4. Overvoltage protection modes

OVLO pin	OVLO threshold
< 0.1 V or connected to GND	Fixed 5.98 V
Resistor ladder from IN	Adjustable

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS25961 device is an integrated eFuse that is typically used for input hot-swap and power rail protection applications for systems such as energy meters, set-top boxes, building automation and adapter input protection. The device operates from 2.7-V to 19-V with adjustable current limit, overvoltage and undervoltage protection. The device aids in controlling the inrush current and provides current limiting during overload conditions.

The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, TPS25961 Design Calculator, is available in the web product folder.

8.2 典型应用

8.2.1 Adapter input protection for set-top boxes

TPS25961 can be used for input power protection in set-top boxes. Operating voltage is generally around 12-V and can vary from 10-V to 14-V. During event like input voltage overshoot, TPS25961 overvoltage protection acts to cut off the path and protect downstream load from overvoltage. Also inrush current control and configurable current limit feature helps in preventing power supply from collapsing during events like hotplug and overload.

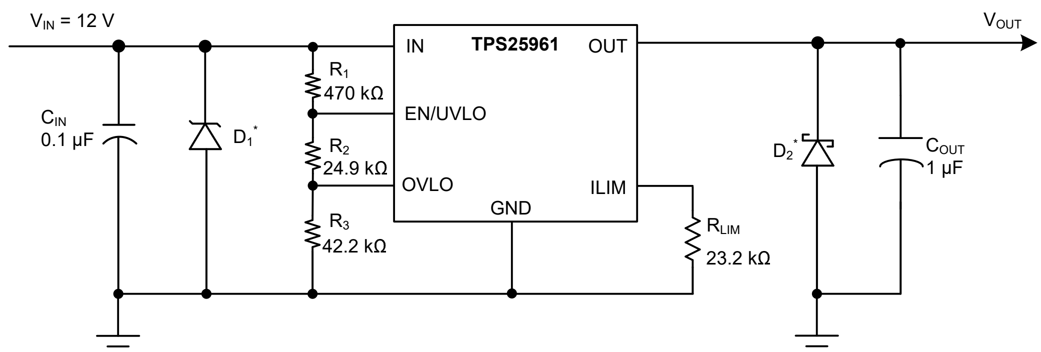


图 8-1. Typical Application Schematic

* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to Transient Protection section for details.

8.2.2 Design Requirements

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage , V_{IN}	12 V
Undervoltage lockout set point, V_{UV}	9 V
Overvoltage protection set point , V_{OV}	15.5 V
Current limit, I_{LIM}	2 A
Load capacitance, C_{OUT}	1 µF
Maximum ambient temperature, T_A	85°C

8.2.3 Detailed Design Procedure

8.2.3.1 Programming the Current-Limit Threshold: R_{ILM} Selection

The R_{ILM} resistor at the ILM pin sets the over load current limit. Since required current limit of 2 A is greater than 200 mA, below 方程式 6 for current limit can be used for calculating R_{ILIM}.

$$\text{RILIM} = \frac{50000}{\text{ILIM}} \tag{6}$$

Closest standard value resistor is 25.5 kΩ with 1% tolerance. It is recommended that final R_{ILM} selected does not lie in the ranges mentioned in 表 7-1. Final value of 25.5 kΩ does not lie in those non-recommended ranges and is fine to use in design.

8.2.3.2 欠压和过压锁定设定点

电源欠压和过压阈值通过电阻器 R1、R2 和 R3 进行设置，这些电阻器的值可通过公式 10 和公式 11 进行计算：

$$\text{VIN(UV)} = \frac{\text{VUVLO(R) x (R1 + R2 + R3)}}{\text{R2 + R3}} \tag{7}$$

$$\text{VIN(OV)} = \frac{\text{VOVLO(R) x (R1 + R2 + R3)}}{\text{R3}} \tag{8}$$

其中 $V_{UVLO(R)}$ 是 EN/UVLO 引脚上升阈值，$V_{OVLO(R)}$ 是 OVLO 引脚上升阈值。由于 R1、R2 和 R3 泄漏来自输入电源 VIN 的电流，因此必须根据来自输入电源 VIN 的可接受漏电流来选择这些电阻器。R1、R2 和 R3 从电源汲取的电流为 IR123 = VIN/(R1 + R2 + R3)。但是，由于连接到电阻器串的外部有源元件而产生的漏电流会增加这些计算的误差。因此，电阻串电流 IR123 必须选择为 EN/UVLO 和 OVLO 引脚上预期漏电流的 20 倍。根据器件电气规格，EN/UVLO 和 OVLO 漏电流均为 0.1 μA（最大值）、$V_{OVLO(R)}$ = 1.24V 且 $V_{UVLO(R)}$ = 1.24V。根据设计要求，VIN(OV) = 15.5V 且 VIN(UV) = 9V。要求解，请先选择 R1 = 470kΩ，并使用上面的公式计算 R2 = 31.5kΩ、R3 = 43.6kΩ。使用最接近的标准 1% 电阻器值，我们得到 R1 = 470kΩ、R2 = 31.6kΩ 且 R3 = 44.2kΩ。

8.2.3.3 Output Voltage Rise Time (tR)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to to determine that power dissipation is below a certain limit to avoid thermal shutdown during start-up.

Slew rate is 5 V/ms typically for TPS25961. The inrush current can be calculated as:

$$\text{IINRUSH (mA)} = \text{SR (V/ms) x COUT (μF)} = 5 \text{ x } 1 = 5 \text{ mA} \tag{9}$$

The average power dissipation inside the part during inrush can be calculated as:

$$\text{PDINRUSH (W)} = \frac{\text{IINRUSH (A) x VIN (V)}}{2} = \frac{0.005 \text{ x } 12}{2} = 0.03 \text{ W} \tag{10}$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. 图 8-2 shows the thermal shutdown limit, for 0.03 W of power, the shutdown time is very large as compared to t_R = 2.4 ms. Therefore this application will have successful startup.

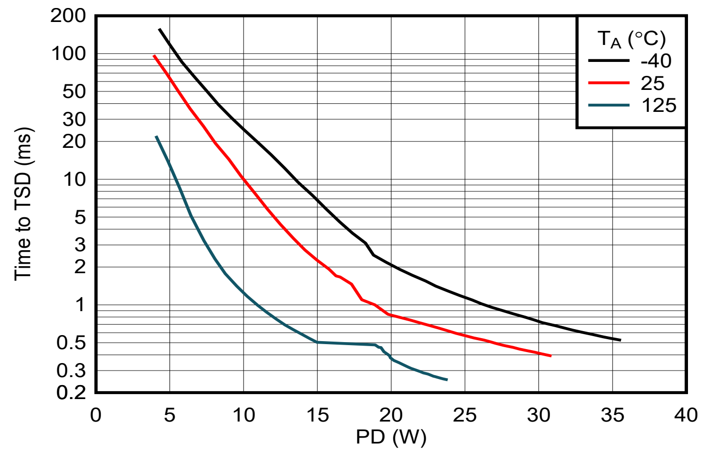


图 8-2. Time to Thermal Shutdown vs Power Dissipation

8.2.4 Application Curves

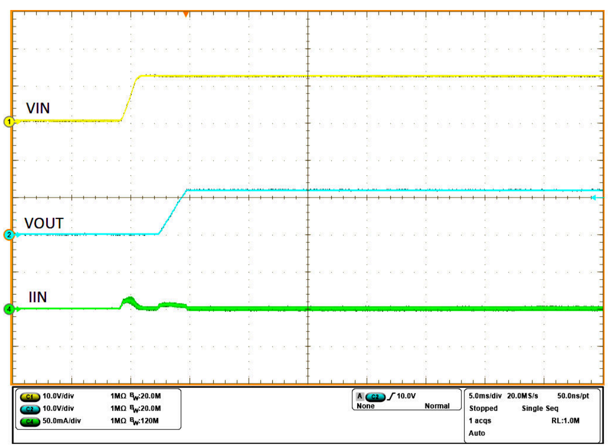


图 8-3. Output Ramp

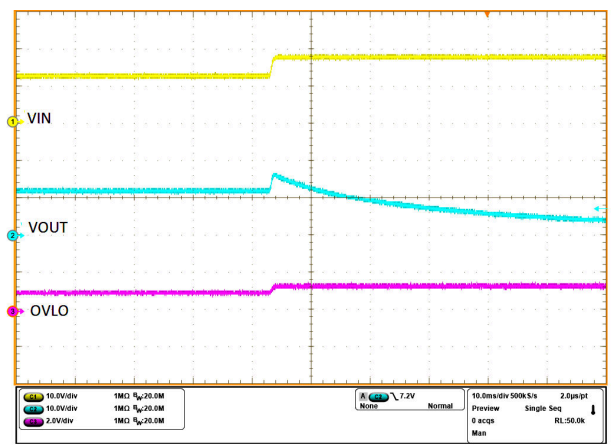


图 8-4. Overvoltage Protection (OVLO)

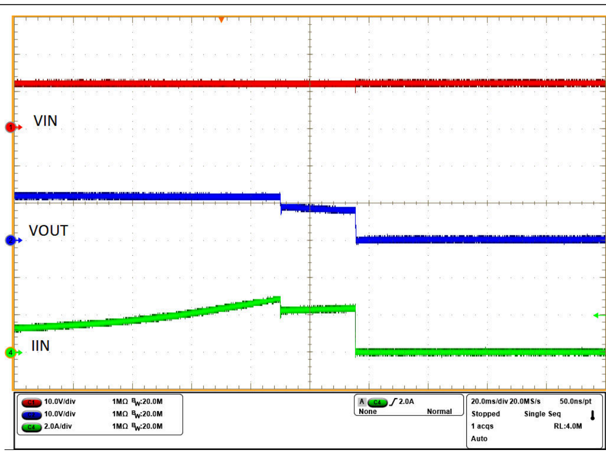


图 8-5. Overcurrent Protection

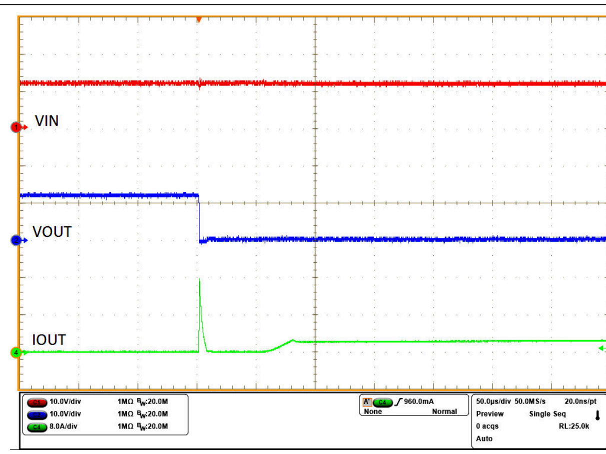


图 8-6. Short at Output Protection

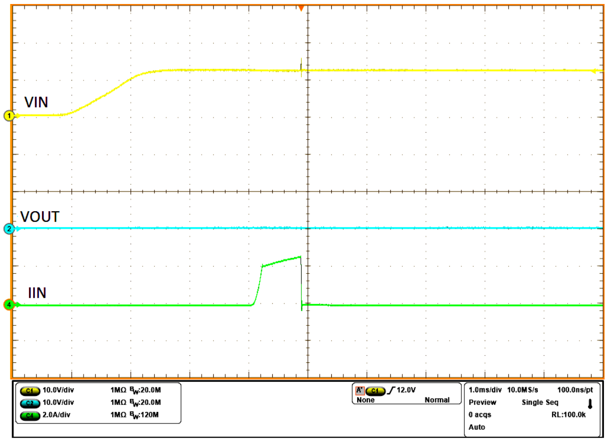


图 8-7. Wakeup in Short Protection

8.3 Application Example

TPS25961 can also be used as a low cost current limiter device replacing discrete PTC for memory card port protection in end equipments like IP camera, Laptop etc. Typical SD cards operate at 3.3-V and draw current less than 100 mA. TPS25961 can be configured for protection in this application without the need for many external components. Keeping OVLO pin grounded and ILIM pin open would set fixed overvoltage protection thresold of 5.98 V and current limit of 115 mA. EN pin can be tied to VIN pin through a pullup resistor. 图 8-9 shows example layout for TPS25961 for above mentioned configuration, achieved on a single layer board with minimum components.

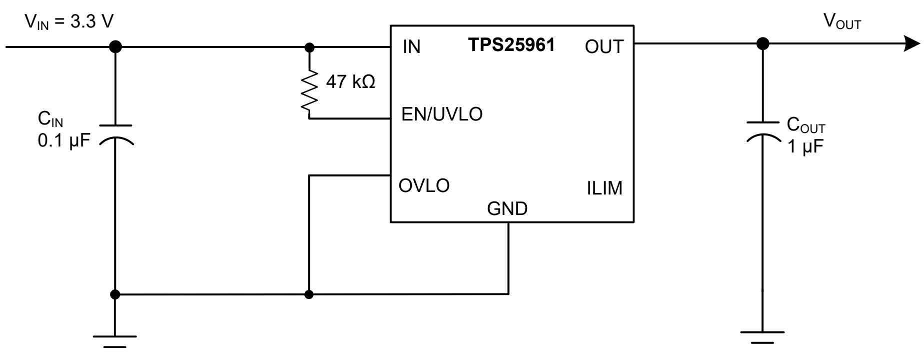


图 8-8. SD card port protection using TPS25961

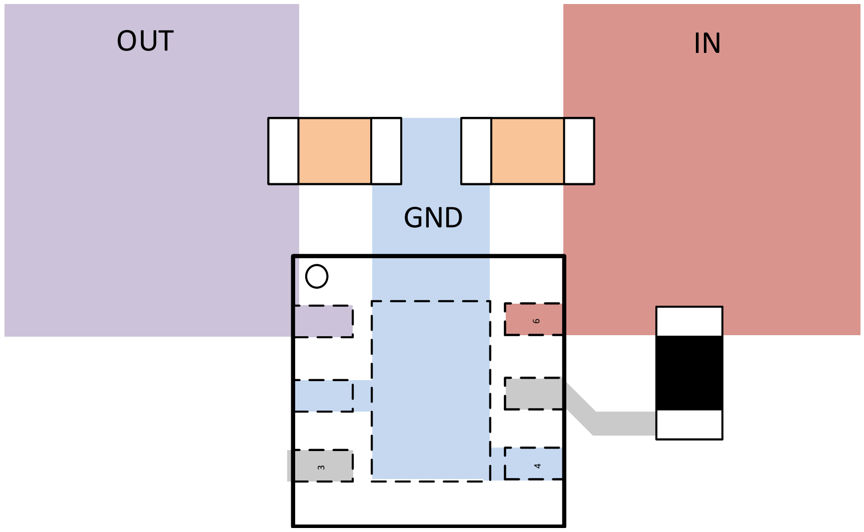


图 8-9. TPS25961 layout example for SD card port protection application

8.3.1 Application Curves

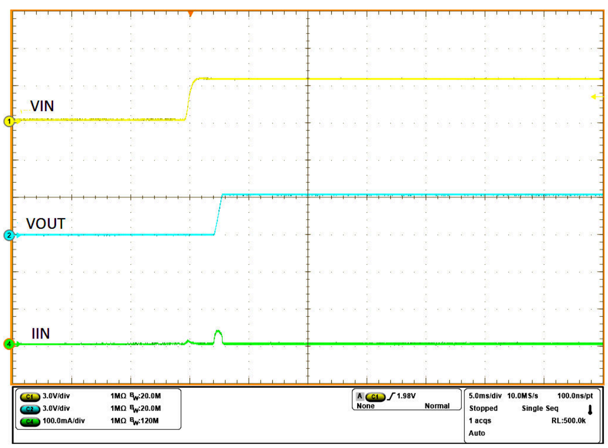


图 8-10. Output Ramp

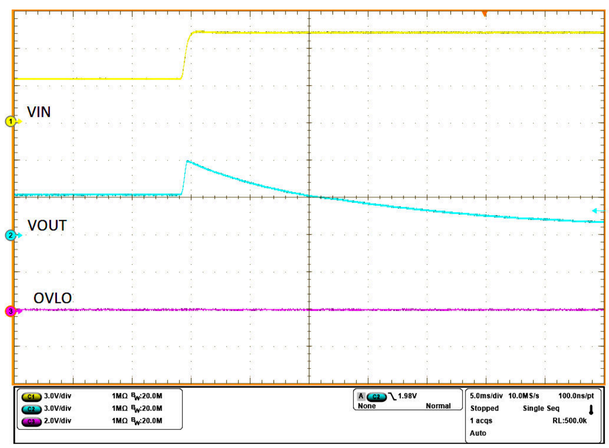


图 8-11. Overvoltage protection

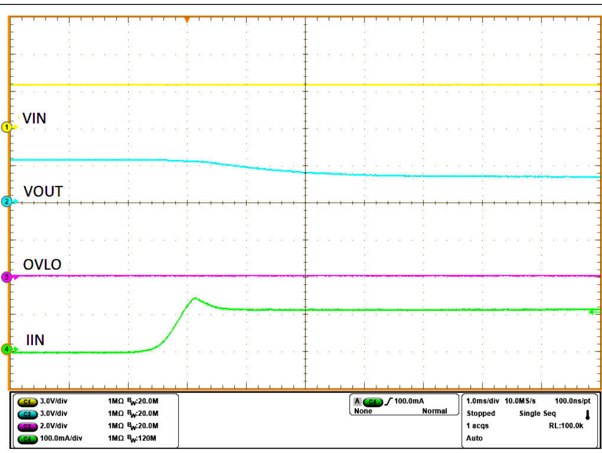


图 8-12. Overcurrent Protection

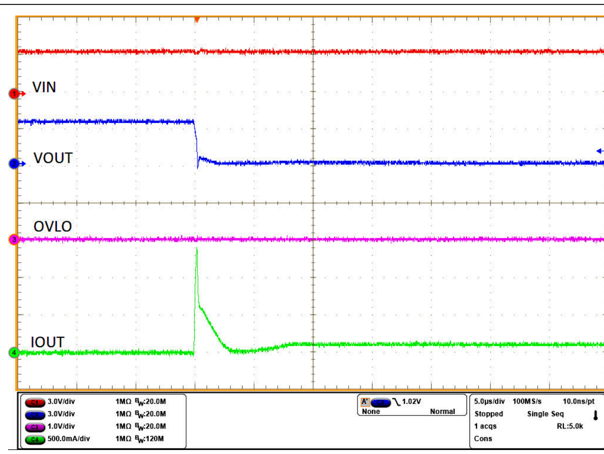


图 8-13. Short at Output Protection

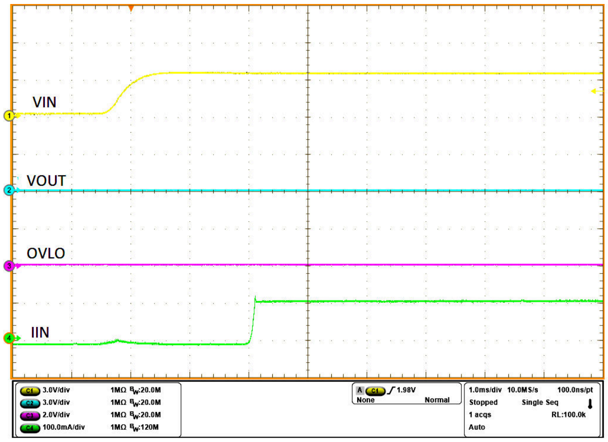


图 8-14. Wake up into Short Protection

8.4 Power Supply Recommendations

The TPS25961 devices are designed for a supply voltage range of 2.7-V ≤ V_{IN} ≤ 19-V. An input ceramic bypass capacitor higher than 0.1 µF is recommended if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

8.4.1 瞬态保护

在短路和过载电流限制情况下，当器件中断电流时，输入电感在输入端产生正电压尖峰，输出电感在输出端产生负电压尖峰。电压尖峰（瞬变）的峰值振幅取决于与器件输入或输出串联的电感值。如果未采取措施解决此问题，此类瞬变可能会超过器件的绝对最大额定值。解决瞬变的典型方法包括：

- 更大限度减少进出器件的引线长度和电感。
- 使用较大的 PCB GND 平面。
- 在输出端使用肖特基二极管来吸收负尖峰。
- 使用低值陶瓷电容器 C_{IN} = 0.1 µF 来吸收能量并抑制瞬变。输入电容的近似值可通过以下公式进行估算：

$$V_{峰值(绝对)} = VIN + I_{负载} \times \sqrt{\frac{LIN}{CIN}} \quad (11)$$

其中

- V_{IN} 是标称电源电压
- I_{LOAD} 是负载电流
- L_{IN} 等于在源中观察到的有效电感
- C_{IN} 是输入端存在的电容

备注

注：需要通过 IEC 61000-4-4 电气快速瞬变 (EFT) 抗扰度测试的系统应使用至少 2.2 µF 的 C_{IN}，以确保 TPS25961 在 EFT 突发期间不会关闭。

某些应用可能需要添加瞬态电压抑制器 (TVS)，以防止瞬变超过器件的绝对最大额定值。采用可选保护元件（陶瓷电容器、TVS 和肖特基二极管）的电路实现如图 8-15 所示。

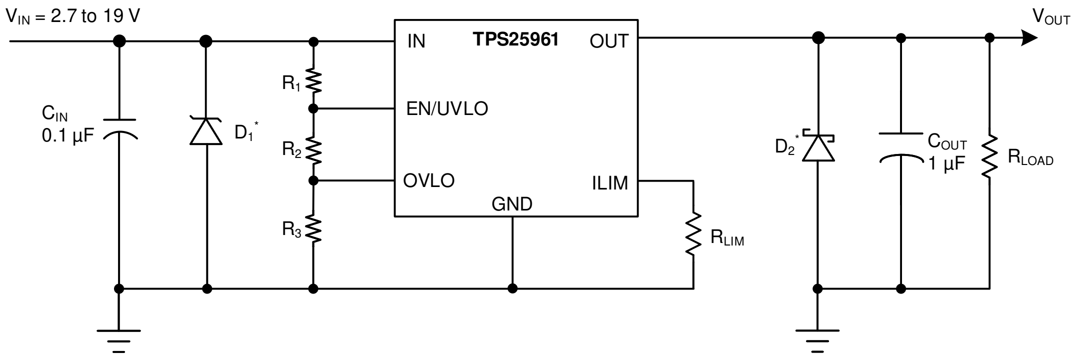


图 8-15. 带有可选保护元件的电路实现

8.4.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

8.5 Layout

8.5.1 Layout Guidelines

- For all applications, a ceramic decoupling capacitor of 0.1 µF or greater is recommended between the IN terminal and GND terminal. For hot-plug applications, where input power-path inductance is negligible, this capacitor can be eliminated or minimized.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground must be a copper plane or island on the board.
- Locate the following support components close to their connection pins:
  - R_{ILIM}
  - Resistor network for the EN/UVLO pin
  - Resistor network for the OVLO pin

  Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing from the components to the device pins must be as short as possible to reduce parasitic effects on the current limit and overvoltage response. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible. The example shown in 节 8.5.2 has been shown to produce good results and is intended as a guideline.

8.5.2 Layout Example

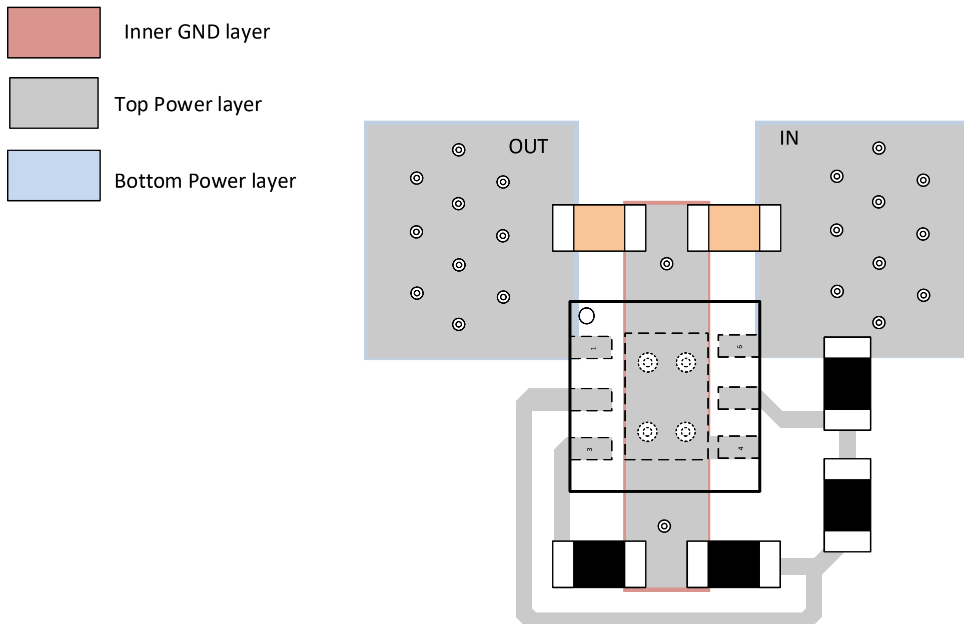


图 8-16. TPS25961 Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- TPS25961 Design Calculator
- TPS25961EVM eFuse Evaluation Board
- *Basics of eFuses*

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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9.4 商标

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 术语表

TI 术语表 　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25961DRVR	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T961
TPS25961DRVR.A	Active	Production	WSON (DRV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T961

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

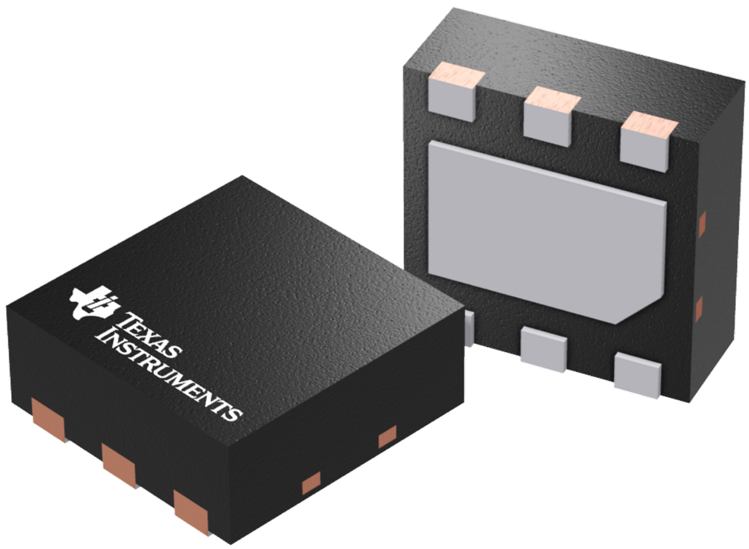
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

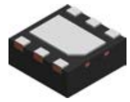
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



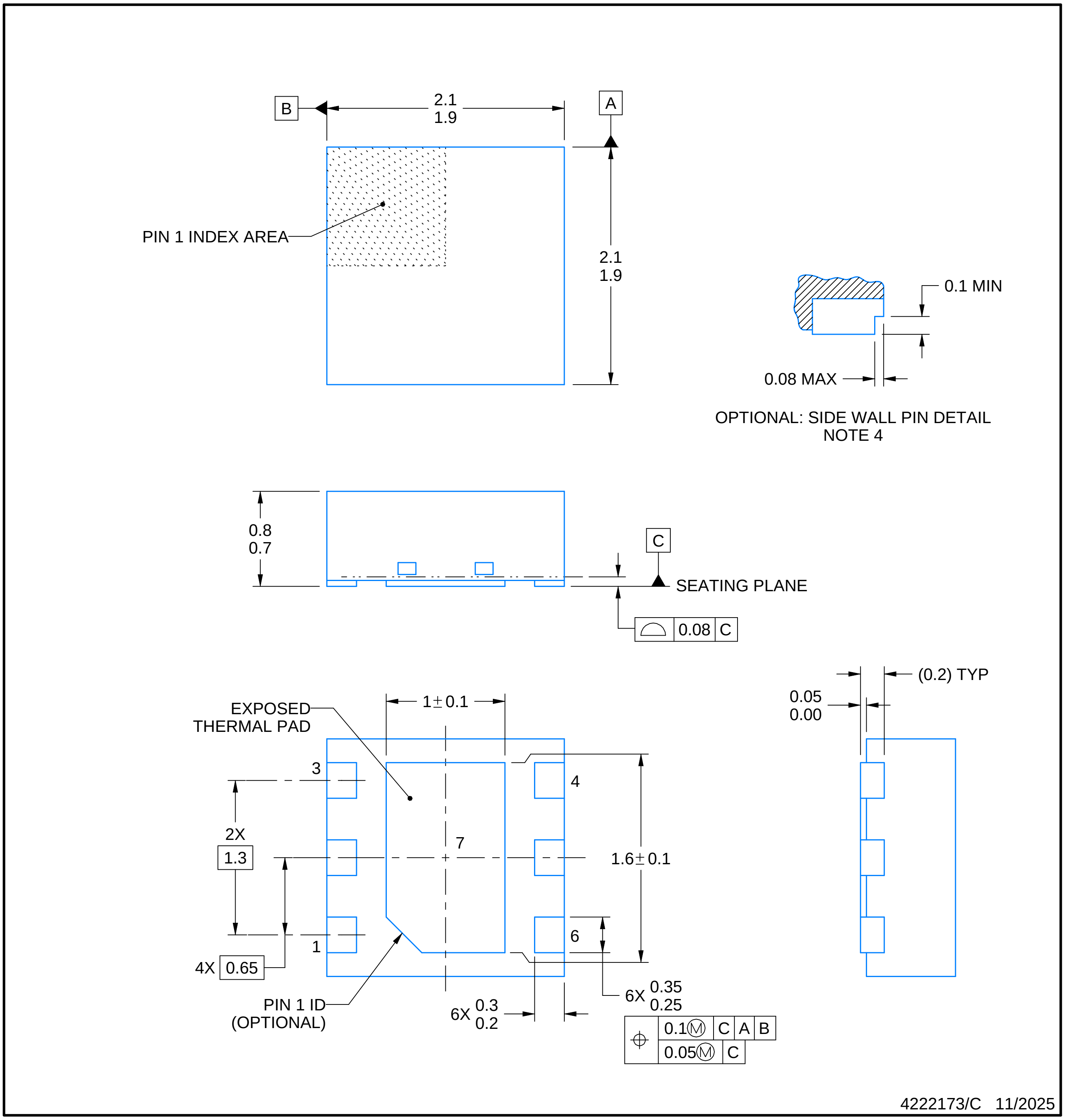
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

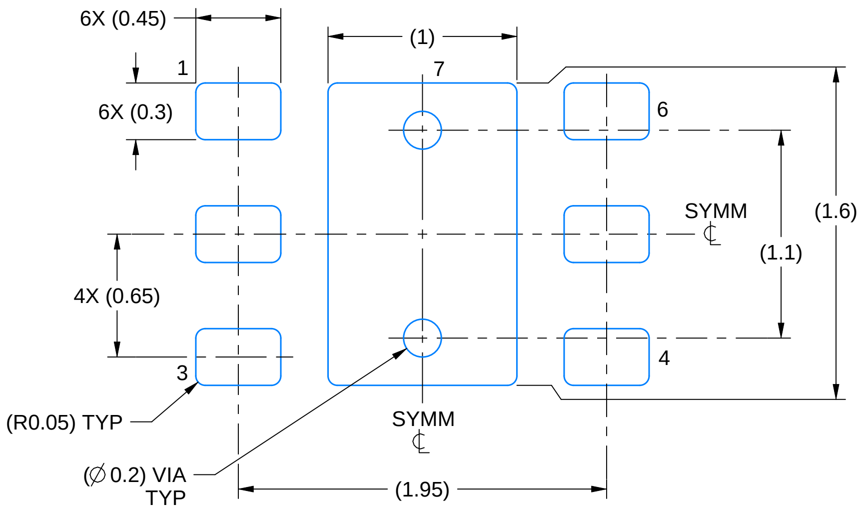
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

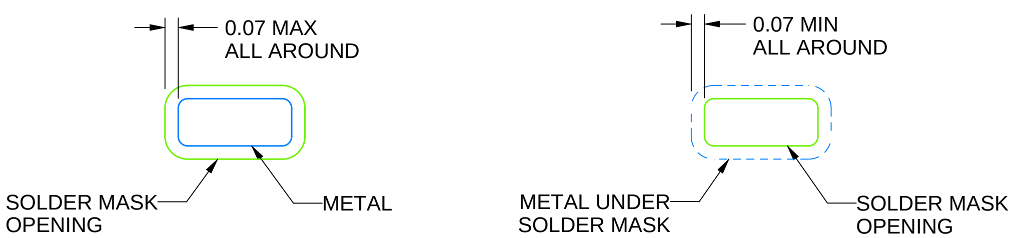


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Minimum 0.1 mm solder wetting on pin side wall. Available for wettable flank version only.



LAND PATTERN EXAMPLE
SCALE:25X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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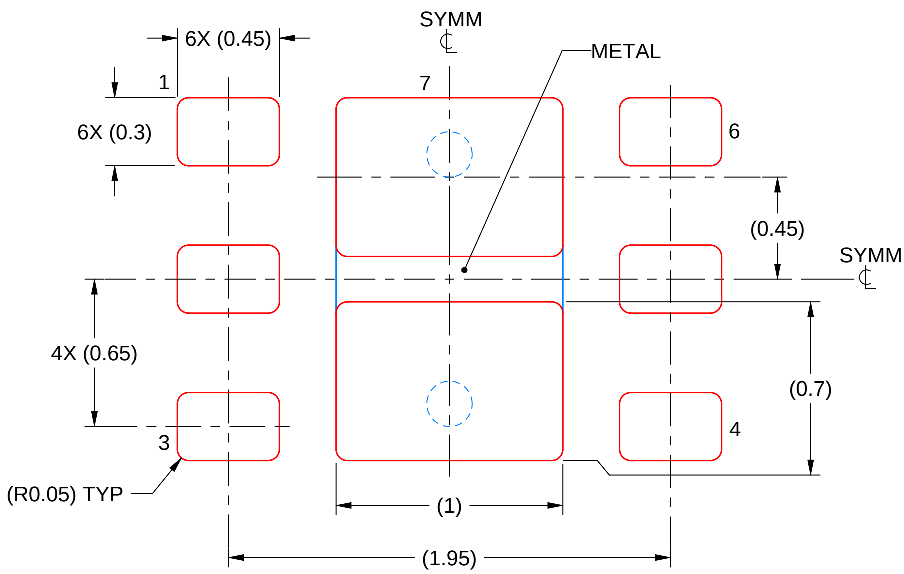
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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