TPS25752A USB Type-C® and USB PD Controller With Integrated Power Switches Optimized for Source Power Applications

1 Features

- This device is certified by the USB-IF for PD3.2
  - TPS25752A TID#: 15343
  - Article on PD2.0 vs. PD3.0
- Optimized for USB Type-C PD Source (DFP) power applications
  - Built in I2C control for TI DCDC controllers
  - Web-based GUI and pre-configured firmware
  - For a more extensive selection guide and getting started information, please refer to www.ti.com/usb-c
- Programmable power supply (PPS) and adjustable voltage supply (AVS)
  - Supports PPS source
  - Standalone PPS source control TI DC/DC
  - Supports AVS source
- Liquid detection
  - Measures directly at the Type-C connector
  - Integrated error handling and protection
- Integrated fully managed power paths
  - Integrated 5V, 3A, and 36mΩ sourcing switch
  - Integrated undervoltage and overvoltage protection and current limiting for inrush current protection for the 5V/3A source power path
  - 26V tolerant CC pins for robust protection when connected to non-compliant devices
- Additional features
  - 11 configurable GPIOs
  - BC1.2 charging support
  - 1 I2C controller port
  - 1 I2C target port

2 Applications

- HMI panel
- Wireless speaker
- Power stations
- Telematics
- Server racks

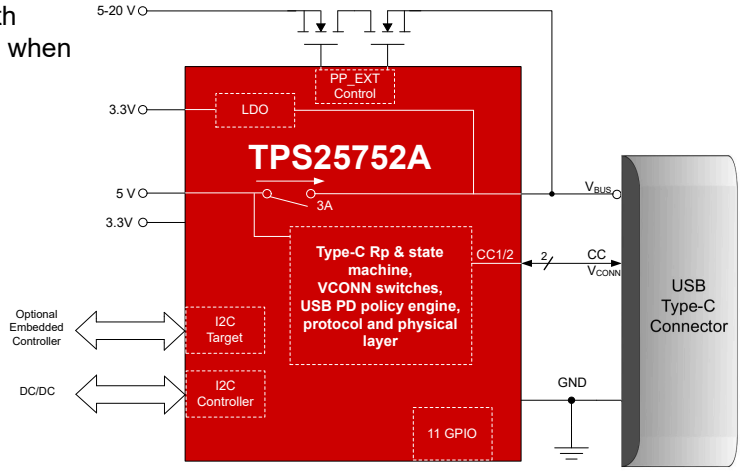
3 Description

The TPS25752A is a highly integrated stand-alone USB Type-C and power delivery (PD) controller optimized for applications supporting USB-C PD power. The TPS25752A integrates fully managed power paths with robust protection for a complete USB-C PD application. The TPS25752A also integrates I2C control for DC/DC ICs for added ease of use and reduced time to market. The intuitive web based GUI asks the user a few simple questions on the applications needs using clear block diagrams and simple multiple-choice questions. As a result, the GUI creates the configuration image for the user's application, reducing much of the complexity associated with USB PD applications.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS25752A	32-VQFN (RSM)	4.00mm x 4.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



TPS25752A Schematic

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4 Pin Configuration and Functions

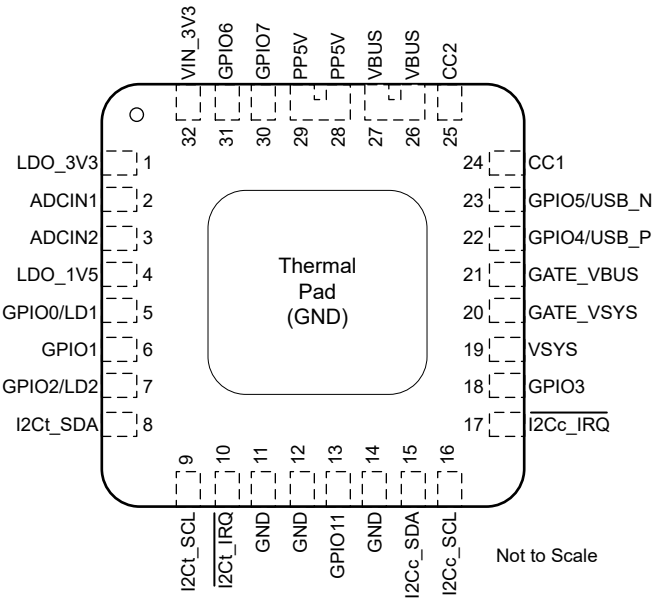


Figure 4-1. TPS25752A QFN Package, 32-Pin (Top View)

Table 4-1. TPS25752A Pin Functions

PIN		TYPE(1)	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration Input. Connect to a resistor divider to LDO_3V3.
CC1	24	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C_{CC}).
CC2	25	I/O	Hi-Z	I/O for USB Type-C. Filter noise with recommended capacitor to GND (C_{CC}).
GATE_VSYS	20	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VSYS
GATE_VBUS	21	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VBUS
GND	11, 12, 14	—	—	Ground. Connect to ground plane.
GPIO0/LD1	5	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected for liquid detection on Type-C connector. Tie to ground when pin is unused.
GPIO1	6	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
GPIO2/LD2	7	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected for liquid detection on Type-C connector. Tie to ground when pin is unused.
GPIO3	18	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
GPIO4/USB_P	22	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected to D+ for BC1.2 support. Tie to ground when pin is unused.
GPIO5/USB_N	23	GPIO	Hi-Z	General purpose digital I/O. Pin can be connected to D- for BC1.2 support. Tie to ground when pin is unused.
GPIO6	31	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
GPIO7	30	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
I2Ct_SCL	9	I	Hi-Z	I2C target serial clock input. Tie to pullup voltage through a resistor. Tie to ground if unused.
I2Ct_SDA	8	I/O	Hi-Z	I2C target serial data. Open-drain input/output. Tie to pullup voltage through a resistor. Tie to ground if unused.
$\overline{\text{I2Ct\_IRQ}}$	10	O	Hi-Z	I2C target interrupt. Active low. Connect to external voltage through a pull-up resistor. Pin can be re-configured to GPIO10. Tie to ground when unused.
I2Cc_SCL	16	O	Hi-Z	I2C controller serial clock. Open-drain output. Tie to pullup voltage through a resistor.
GPIO11	13	GPIO	Hi-Z	General purpose digital I/O. Tie to ground when pin is unused.
I2Cc_SDA	15	I/O	Hi-Z	I2C controller serial data. Open-drain input/output. Tie to pullup voltage through a resistor.
$\overline{\text{I2Cc\_IRQ}}$	17	I	Hi-Z	I2C controller interrupt. Active low. Connect to external voltage through a pull-up resistor. Pin can be re-configured to GPIO12.
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
PP5V	28, 29	I	—	5V system supply to VBUS, supply for CC_y pins as VCONN.
VSYS	19	I	—	System side high voltage sensing node.
VBUS	26, 27	I/O		5V to 20V input. Bypass with capacitance C_{VBUS} to GND.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance C_{VIN_3V3} to GND. Tie to GND if device is VBUS powered only.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

5 Specifications

5.1 Absolute Maximum Ratings

5.1.1 TPS25752A - Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

PARAMETER		MIN	MAX	UNIT
Input voltage range [2]	VIN_3V3	–0.3	4	V
	PP5V	-0.3	6	V
	ADCINx	–0.3	4	V
	VBUS[4]	–0.3	28	V
	CC1, CC2 [4]	–0.5	26	V
	GPIOx	–0.3	6	V
	I2Ct_SCL, I2Ct_SDA	–0.3	4	V
Output voltage range [2]	LDO_1V5[3]	–0.3	2	V
	LDO_3V3[3]	–0.3	4	
Source current	Source or Sink current VBUS		internally limited	A
	Positive source current for LDO_3V3, LDO_1V5		internally limited	
Source current	GPIOx		0.005	A
T_J Operating junction temperature		–40	175	°C
T_{STG} Storage temperature		–55	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent damage to the device. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the *Recommended Operating Conditions* but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(3) Do not apply voltage to these pins.
(4) A TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200.

5.1.2 TPS25752A - Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNIT
Output voltage range [1]	GATE_VBUS, GATE_VSYS [2]	–0.3	40	V
V_{GS}	V_{GATE_VBUS} - V_{VBUS}, V_{GATE_SYS} - V_{VSYS}	–0.5	12	V

(1) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(2) Do not apply voltage to these pins.

5.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 TPS25752A - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER			MIN	MAX	UNIT
V_I	Input voltage range(1)	VIN_3V3	3.0	3.6	V
V_I	Input voltage range(1)	PP5V	4.9	5.5	V
V_I	Input voltage range(1)	VBUS(2)	4	22	V
V_{IO}	I/O voltage range(1)	I2Cx_SDA, I2Cx_SCL, $\overline{\text{I2Cx\_IRQ}}$ ADCINx	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I_O	Output current (from PP5V)	VBUS		3	A
		CC1, CC2		315	mA
I_O	Output current (from LDO_3V3)	GPIOx		1	mA
I_O	Output current (from VBUS LDO)	Sum of current from LDO_3V3 and GPIOx		5	mA
T_J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.
(2) Short all VBUS pins together.

5.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{VIN_3V3}	Capacitance on VIN_3V3	6.3V	5	10		µF
C_{LDO_3V3}	Capacitance on LDO_3V3	6.3V	5	10	25	µF
C_{LDO_1V5}	Capacitance on LDO_1V5	4V	4.5		12	µF
C_{VBUS}	Capacitance on VBUS	25V	1	4.7	10	µF
C_{PP5V}	Capacitance on PP5V	10V	120(2)			µF
C_{CCy}	Capacitance on CCy pins(3)	6.3V	200	400	480	pF

(1) Capacitance values do not include any derating factors. For example, if 5µF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value is 10µF.
(2) Minimum capacitance is a requirement from USB PD (cSrcBulkShared). Keep at least 120µF tied directly to PP5V.
(3) Capacitance includes all external capacitance to the Type-C receptacle.

5.5 Thermal Information

THERMAL METRIC(1)		TPS25752A QFN (RSM) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance	24.5	°C/W
$R_{\theta JC}$	Junction-to-board (bottom) thermal resistance	2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted: 3.0V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN_3V3, VBUS						
V_{VBUS_UVLO}	VBUS UVLO threshold	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis		0.1		
V_{VIN3V3_UVLO}	Voltage required on VIN_3V3 for power on	rising, V_{VBUS} = 0	2.56	2.66	2.76	V
		falling, V_{VBUS} = 0	2.44	2.54	2.64	
		hysteresis		0.12		
LDO_3V3, LDO_1V5						
V_{LDO_3V3}	Voltage on LDO_3V3	V_{VIN_3V3} = 0V, 10µA ≤ I_{LOAD} ≤ 18mA, V_{VBUS} ≥ 3.9V	3.0	3.4	3.6	V
R_{LDO_3V3}	Rdson of VIN_3V3 to LDO_3V3	I_{LDO_3V3} = 50mA			1.4	Ω
V_{LDO_1V5}	Voltage on LDO_1V5	up to maximum internal loading condition	1.49	1.5	1.65	V

5.7 Power Consumption

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V, no GPIO loading

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VIN\_3V3,ActSrc}$	Current into VIN_3V3	Active Source mode: V_{VBUS} = 5V, V_{VIN_3V3} = 3.3V		3		mA
$I_{VIN\_3V3,ActSnk}$	Current into VIN_3V3	Active PPHV mode: 22V ≥ V_{VBUS} ≥ 4V, V_{VIN_3V3} = 3.3V		3	6	mA
$I_{VIN\_3V3,IdlSrc}$	Current into VIN_3V3	Idle Source mode: V_{VBUS} = 5V, V_{VIN_3V3} = 3.3V		1.0		mA
$I_{VIN\_3V3,IdlSnk}$	Current into VIN_3V3	Idle PPHV mode: 22V ≥ V_{VBUS} ≥ 4V, V_{VIN_3V3} = 3.3V		1.0		mA
$I_{PP5V,Sleep}$	Current into PP5V	Sleep mode: V_{PA_VBUS} = 0V, V_{VIN_3V3} = 3.3V		2		µA
$I_{VIN\_3V3,Sleep}$	Current into VIN_3V3	Sleep mode: V_{VBUS} = 0V, V_{VIN_3V3} = 3.3V		56		µA

5.8 PP_5V Power Switch Characteristics

Operating under these conditions unless otherwise noted: 3.0V ≤ V_{LDO_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3A, T_J = 25°C		36	38	mΩ
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A,T_J = 125°C		36	53	mΩ
I_{PP5V_REV}	VBUS to PP5V leakage current	V_{PP5V} = 0V, V_{VBUS} = 5.5V, PP_5V disabled, T_J ≤ 85°C, measure I_{PP5V}			5	µA
I_{PP5V_FWD}	PP5V to VBUS leakage current	V_{PP5V} = 5.5V, V_{VBUS} = 0V, PP_5V disabled, T_J ≤ 85°C, measure I_{VBUS}			15	µA
I_{LIM5V}	Current limit setting	Configure to setting 0	1.15		1.36	A
I_{LIM5V}	Current limit setting	Configure to setting 1	1.61		1.90	A
I_{LIM5V}	Current limit setting	Configure to setting 2	2.3		2.70	A
I_{LIM5V}	Current limit setting	Configure to setting 3	3.04		3.58	A
I_{LIM5V}	Current limit setting	Configure to setting 4	3.22		3.78	A
I_{VBUS}	PP5V to VBUS current sense accuracy	3.64A ≥ I_{VBUS} ≥ 1 A	3.05	3.5	3.75	A/V
$V_{PP\_5V\_RCP}$	RCP clears and PP_5V starts turning on when V_{VBUS} – V_{PP5V} < $V_{PP\_5V\_RCP}$. Measure V_{VBUS} – V_{PP5V}		10		20	mV

5.8 PP_5V Power Switch Characteristics (continued)

Operating under these conditions unless otherwise noted: 3.0V ≤ V_{LDO_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{iOS\_PP\_5V}$	Response time to VBUS short circuit	VBUS to GND through 10mΩ, C_{VBUS} = 0		1.15		µs
$t_{PP\_5V\_ovp}$	Response time to V_{VBUS} > $V_{OVP4RCP}$	Enable PP_5V, I_{RpDef} being drawn from PP5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4V to 20V at 100V/ms, C_{PP5V} = 2.5 µF, measure time from OVP detection until reverse current < 100mA		4.5		µs
$t_{PP\_5V\_uvlo}$	Response time to V_{PP5V} < V_{PP5V_UVLO}, PP_VBUS is deemed off when V_{VBUS} < 0.8V	R_L = 100Ω, no external capacitance on VBUS		4		µs
$t_{PP\_5V\_rcp}$	Response time to V_{PP5V} < V_{VBUS} + $V_{PP\_5V\_RCP}$	V_{PP5V} = 5.5V, I_{RpDef} being drawn from PP5V, enable PP_5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4V to 21.5V at 10 V/µs, measure V_{PP5V}. C_{PP5V} = 104µF, C_{VBUS}=10µF, measure time from RCP detection until reverse current < 100mA		0.7		µs
t_{ILIM}	Current clamping deglitch time			5.1		ms
t_{ON}	From enable signal to VBUS at 90% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L = 0	2.3	3.3	4.3	ms
t_{OFF}	From disable signal to VBUS at 10% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L = 0	0.30	0.45	0.6	ms
t_{RISE}	VBUS from 10% to 90% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L = 0	1.2	1.7	2.2	ms
t_{FALL}	VBUS from 90% to 10% of initial value	R_L = 100Ω, V_{PP5V} = 5V, C_L = 0	0.06	0.1	0.14	ms

5.9 PP_EXT Characteristics - TPS25752A

Operating under these conditions unless otherwise noted: , 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GATE_ON}	Gate driver sourcing current	0V ≤ V_{GATE_VSYS} - V_{VSYS} ≤ 6V, V_{VSYS} ≤ 22V, V_{VBUS} > 4V, measure I_{GATE_VSYS}	8.5		11.5	µA
		0V ≤ V_{GATE_VBUS} - V_{VBUS} ≤ 6V, 4V ≤ V_{VBUS} ≤ 22V, measure I_{GATE_VBUS}	8.5		11.5	µA
V_{GATE_ON}	Sourcing voltage (ON)	0V ≤ V_{VSYS} ≤ 22V, I_{GATE_VSYS} < 4µA, measure V_{GATE_VSYS} – V_{VSYS}, V_{VBUS} > 4V	6		12	V
		4V ≤ V_{VBUS} ≤ 22V, I_{GATE_VBUS} < 4µA, measure V_{GATE_VBUS} – V_{VBUS}	6		12	V

5.9 PP_EXT Characteristics - TPS25752A (continued)

Operating under these conditions unless otherwise noted: , 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GATE_OFF}	Sinking strength	Normal turnoff: V_{VSYS} = 5V, V_{GATE_VSYS} = 6V, measure I_{GATE_VSYS}	13			µA
		Normal turnoff: V_{VBUS} = V_{VSYS} = 5V, V_{GATE_VBUS} = 6V, measure I_{GATE_VBUS}	13			µA
R_{GATE_FSD}	Sinking strength	Fast turnoff: V_{VSYS} = 5V, V_{GATE_VSYS} = 6V, assert PPHV1_FAST_DISABLE, measure R_{GATE_VSYS}			85	Ω
		Fast turnoff: V_{VBUS} = V_{VSYS} = 5V, V_{GATE_VBUS} = 6V, assert PPHV1_FAST_DISABLE, measure R_{GATE_VBUS}			85	Ω
$R_{GATE\_OFF\_UVLO}$	Sinking strength in UVLO (safety)	V_{VIN_3V3} = 0V, V_{VBUS} = 3V, V_{GATE_VSYS} = 0.1V, measure resistance from GATE_VSYS to GND			1.5	MΩ
$t_{GATE\_VBUS\_OFF}$	Time allowed to disable the external FET via GATE_VBUS in normal shutdown mode.(1)	V_{VBUS} = 20V, Q_G of external FET = 40nC or C_{GATE_VBUS} < 3nF, gate is off when V_{GATE_VBUS} – V_{VBUS} < 1V		450	4000	µs
$t_{GATE\_VBUS\_OVP}$	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode ($V_{OVP4RCP}$ exceeded), this includes the response time of the comparator	OVP: $V_{OVP4RCP}$ = setting 57, V_{VBUS} = 20V initially, then raised to 23V in 50ns, Q_G of external FET = 40nC or C_{GATE_VBUS} < 3nF, gate is off when V_{GATE_VBUS} – V_{VBUS} < 1V		3	5	µs
$t_{GATE\_VSYS\_OFF}$	Time allowed to disable the external FET via GATE_VSYS in normal shutdown mode(1)	V_{VSYS}= 20V, Q_G of external FET = 40nC or C_{GATE_VBUS} < 3nF, gate is off when V_{GATE_VSYS} – V_{VSYS} < 1V		450	4000	µs
$t_{GATE\_VSYS\_FSD}$	Time allowed to disable the external FET via GATE_VSYS in fast shutdown mode (OVP)(1)	V_{VBUS} = 20V initially, then raised to 23V in 50ns, Q_G of external FET = 40 nC or C_{GATE_VBUS} < 3nF, gate is off when V_{GATE_VSYS} – V_{VSYS} < 1V, r_{OVP} = 1		0.25	20	µs
$t_{GATE\_VBUS\_ON}$	Time to enable GATE_VBUS (1)	Measure time from when V_{GS} = 0V until V_{GS} >3V, where V_{GS} = V_{GATE_VBUS} – V_{VBUS}		0.25	2	ms

(1) These values depend upon the characteristics of the external N-ch MOSFET. The typical values measured are when Px_GATE_VSYS and Px_GATE_VBUS are used to drive two CSD17571Q2 in common drain back-to-back configuration.

5.10 Power Path Supervisory

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{PP5V_UVLO}	Voltage required on PP5V	rising	3.9	4.1	4.3	V
		falling	3.8	4.0	4.2	
		hysteresis		0.1		

5.10 Power Path Supervisory (continued)

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OVP4RCP}$	VBUS overvoltage protection for RCP programmable range	OVP detected when V_{VBUS} > $V_{OVP4RCP}$	5.0		24	V
$V_{OVP4RCPH}$	Hysteresis		1.75	2	2.25	%
r_{OVP}	Ratio of OVP4RCP input used for OVP4VSYS comparator. r_{OVP} × $V_{OVP4VSYS}$ = $V_{OVP4RCP}$	Setting 0		1		V/V
		Setting 1		0.95		
		Setting 2		0.9		
		Setting 3		0.875		
$V_{OVP4VSYS}$	VBUS overvoltage protection range for VSYS protection	OVP detected when r_{OVP} × V_{VBUS} > $V_{OVP4RCP}$	5		27.5	V
$V_{OVP4VSYS}$	Hysteresis	VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 0	1.75	2	2.25	%
		VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 1	1.8	2.1	2.4	
		VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 2	1.9	2.2	2.5	
		VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 3	2	2.3	2.6	
I_{DSCH}	VBUS discharge current	V_{VBUS} = 22V, measure I_{VBUS}	4		15	mA

5.11 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Source (Rp pullup)						
$V_{OC\_3.3}$	Unattached CCy open circuit voltage while Rp enabled, no load	V_{LDO_3V3} > 2.302V, R_{CC} = 47kΩ	1.85			V
V_{OC_5}	Attached CCy open circuit voltage while Rp enabled, no load	V_{PP5V} > 3.802V, R_{CC} = 47kΩ	2.95			V
I_{Rev}	Unattached reverse current on CCy	V_{CCy} = 5.5V, V_{CCx} = 0V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6V, V_{PP5V} = 3.8V, measure current into CCy			10	µA
		V_{CCy} = 5.5V, V_{CCx} = 0V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6V, V_{PP5V} = 0V, T_J ≤ 85°C, measure current into CCy			10	
I_{RpDef}	Current source - USB Default	0 < V_{CCy} < 1V, measure I_{CCy}	64	80	96	µA
$I_{Rp1.5}$	Current source - 1.5A	4.75V < V_{PP5V} < 5.5V, 0V < V_{CCy} < 1.5V, measure I_{CCy}	166	180	194	µA
$I_{Rp3.0}$	Current source - 3.0A	4.75V < V_{PP5V} < 5.5V, 0 < V_{CCy} < 2.45V, measure I_{CCy}	304	330	356	µA
Common Comparator						
t_{CC}	deglitch time for comparators on Px_CCy			3.2		ms

5.12 CC VCONN Parameters

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_CABLE}	Rdson of the VCONN path	V_{PP5V} = 5V, I_L = 250mA, measure resistance from PP5V to CCy			1.2	Ω
I_{LIMVC}	Short circuit current limit	Setting 0, V_{PP5V} = 5V, R_L=10mΩ, measure I_{CCy}	350	410	470	mA
I_{LIMVC}	Short circuit current limit	Setting 1, V_{PP5V} = 5V, R_L=10mΩ, measure I_{CCy}	540	600	660	mA
$I_{CC2PP5V}$	Reverse leakage current through VCONN FET	VCONN disabled, T_J ≤ 85°C, V_{CCy} = 5.5V, V_{PP5V} = 0V, V_{VBUS} = 5V, LDO forced to draw from VBUS, measure I_{CCy}			10	µA
V_{VC_OVP}	Overvoltage protection threshold for PP_CABLE	V_{PP5V} rising	5.6	5.9	6.2	V
V_{VC_RCP}	Reverse current protection threshold for PP_CABLE, sourcing VCONN through CCx	V_{PP5V} ≥ 4.9V, V_{CCy} = V_{PP5V}, V_{CCx} rising	60	200	340	mV
		V_{PP5V} ≥ 4.9V, V_{CCy} ≤ 4V, V_{CCx} rising	210	340	470	mV
t_{VCILIM}	Current clamp deglitch time			1.3		ms
$t_{PP\_CABLE\_FSD}$	Time to disable PP_CABLE after V_{PP5V} > V_{VC_OVP} or V_{CCx} - V_{PP5V} > V_{VC_RCP}	C_L = 0		0.5		µs
$t_{PP\_CABLE\_off}$	From disable signal to CCy at 10% of final value	I_L = 250mA, V_{PP5V} = 5V, C_L = 0	100	200	300	µs
$t_{iOS\_PP\_CABLE}$	Response time to short circuit	V_{PP5V} = 5V, for short circuit R_L = 10mΩ		2		µs

5.13 CC PHY Parameters

Operating under these conditions unless otherwise noted: and (3V ≤ V_{VIN_3V3} ≤ 3.6V or V_{VBUS} ≥ 3.9V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
V_{TXHI}	Transmit high voltage on CCy	Standard External load	1.05	1.125	1.2	V
V_{TXLO}	Transmit low voltage on CCy	Standard External load	–75		75	mV
Z_{DRIVER}	Transmit output impedance while driving the CC line using CCy	measured at 750kHz	33	54	75	Ω
t_{Rise}	Rise time. 10% to 90% amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy} = 520pF	300			ns
t_{Fall}	Fall time. 90% to 10% amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy} = 520pF	300			ns
V_{PHY_OVP}	OVP detection threshold for USB PD PHY	0V ≤ V_{VIN_3V3} ≤ 3.6V, 0V ≤ V_{PP5V} ≤ 5.5V, V_{VBUS} ≥ 4V. Initially V_{CC1} ≤ 5.5V and V_{CC2} ≤ 5.5V, then V_{CCx} rises	5.5		8.5	V
Receiver						
Z_{BMCRX}	Receiver input impedance on CCy	Does not include pullup or pulldown resistance from cable detect. Transmitter is Hi-Z	1			MΩ

5.13 CC PHY Parameters (continued)

Operating under these conditions unless otherwise noted: and (3V ≤ V_{VIN_3V3} ≤ 3.6V or V_{VBUS} ≥ 3.9V)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{CC}	Receiver capacitance on CCy [1]	Capacitance looking into the CC pin when in receiver mode			120	pF
$V_{RX\_SRC\_R}$	Rising threshold on CCy for receiver comparator	Source mode (rising)	784	825	866	mV
$V_{RX\_SRC\_F}$	Falling threshold on CCy for receiver comparator	Source mode (falling)	523	550	578	mV

(1) C_{CC} includes only the internal capacitance on a CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding C_{CCy} externally.

5.14 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Temperature shutdown threshold	Temperature rising	145	160	175	°C
		Hysteresis		15		°C
T_{SD_PP5V}	Temperature controlled shutdown threshold. The power paths for each port sourcing from PP5V and PP_CABLE power paths have local sensors that disables them when the temperature is exceeded	Temperature rising	135	150	165	°C
		Hysteresis		10		°C

5.15 ADC Characteristics

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	Least significant bit	3.6V max scaling, voltage divider of 3		14		mV
		25.2V max scaling, voltage divider of 21		98		mV
		4.07A max scaling		16.5		mA
GAIN_ERR	Gain error	0.05V ≤ V_{ADCINx} ≤ 3.6V, V_{ADCINx} ≤ V_{LDO_3V3}	–2.7		2.7	%
		0.05V ≤ V_{GPIOx} ≤ 3.6V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7V ≤ V_{LDO_3V3} ≤ 3.6V	–2.4		2.4	
		0.6V ≤ V_{VBUS} ≤ 22V	–2.1		2.1	
		1A ≤ I_{VBUS} ≤ 3A	–2.1		2.1	
VOS_ERR	Offset error [1]	0.05V ≤ V_{ADCINx} ≤ 3.6V, V_{ADCINx} ≤ V_{LDO_3V3}	–4.1		4.1	mV
		0.05V ≤ V_{GPIOx} ≤ 3.6V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7V ≤ V_{LDO_3V3} ≤ 3.6V	–4.5		4.5	
		0.6V ≤ V_{VBUS} ≤ 22V	–4.1		4.1	
		1A ≤ I_{VBUS} ≤ 3A	–4.5		4.5	mA

(1) The offset error is specified after the voltage divider.

5.16 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO0-7 (Inputs)						
GPIO_VIH	GPIOx high-Level input voltage	V_{LDO_3V3} = 3.3V	1.3			V
GPIO_VIL	GPIOx low-level input voltage	V_{LDO_3V3} = 3.3V			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	V_{LDO_3V3} = 3.3V	0.09			V
GPIO_ILKG	GPIOx leakage current	V_{GPIOx} = 3.45V	–1		1	µA
GPIO_RPU	GPIOx internal pullup	Pullup enabled	50	100	150	kΩ
GPIO_RPD	GPIOx internal pulldown	Pulldown enabled	50	100	150	kΩ
GPIO_DG	GPIOx input deglitch			20	50	ns
GPIO0-7 (Outputs)						
GPIO_VOH	GPIOx output high voltage	V_{LDO_3V3} = 3.3V, I_{GPIOx}= -2mA	2.9			V
GPIO_VOL	GPIOx output low voltage	V_{LDO_3V3} = 3.3V, I_{GPIOx} = 2mA			0.4	V
ADCIN1, ADCIN2						
ADCIN_ILKG	ADCINx leakage current	V_{ADCINx} ≤ V_{LDO_3V3}	–1		1	µA
t_{BOOT}	Time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

5.17 BC1.2 Characteristics

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LGC_HI}	Threshold for no connection	V_{USB_P} ≥ V_{LGC_HI}, V_{LDO_3V3} = 3.3V, R_{USB_P} = 300kΩ	2		3.6	V
V_{LGC_LO}	Threshold for connection	V_{USB_N} ≤ V_{LGC_LO}, V_{LDO_3V3} = 3.3V, R_{USB_P} = 24.8kΩ	0		0.8	V
Advertisement						
V_{DX_SRC}	Source voltage	C_{GPIO4} ≤ 600pF	0.55	0.6	0.65	V
V_{DX_ILIM}	VDX_SRC current limit		250		400	µA
I_{DX_SNK}	Sink Current	V_{USB_P} ≥ 250mV	25	75	125	µA
R_{DCP_DAT}	Dedicated Charging Port Resistance	0.5V ≤ V_{USB_P} ≤ 0.7V, 25µA ≤ I_{USB_N} ≤ 175µA			200	Ω

5.18 I2C Requirements and Characteristics

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{I2Ct\_IRQ}}$						
OD_VOL_IRQ	Low level output voltage	I_{OL} = 2mA			0.4	V
OD_LKG_IRQ	Leakage Current	Output is Hi-Z, V_{I2Cx_IRQ} = 3.45V	–1		1	µA
$\overline{\text{I2Cc\_IRQ}}$						
IRQ_VIH	High-Level input voltage	V_{LDO_3V3} = 3.3V	1.3			V
IRQ_VIH_THRESH	High-Level input voltage threshold	V_{LDO_3V3} = 3.3V	0.72		1.3	V
IRQ_VIL	low-level input voltage	V_{LDO_3V3} = 3.3V			0.54	V
IRQ_VIL_THRESH	low-level input voltage threshold	V_{LDO_3V3} = 3.3V	0.54		1.08	V
IRQ_HYS	input hysteresis voltage	V_{LDO_3V3} = 3.3V	0.09			V
IRQ_DEG	input deglitch			20		ns

5.18 I2C Requirements and Characteristics (continued)

Operating under these conditions unless otherwise noted: 3V ≤ V_{LDO_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IRQ_ILKG	$\overline{\text{I2Cc\_IRQ}}$ leakage current	V_{I2Cc_IRQ} = 3.45V	–1		1	µA
SDA and SCL Common Characteristics (Common Characteristics)						
V_{IL}	Input low signal	V_{LDO_3V3} = 3.3V			0.54	V
V_{IH}	Input high signal	V_{LDO_3V3} = 3.3V	1.3			V
V_{HYS}	Input hysteresis	V_{LDO_3V3} = 3.3V	0.165			V
V_{OL}	Output low voltage	I_{OL} = 3mA			0.36	V
I_{LEAK}	Input leakage current	Voltage on pin = V_{LDO_3V3}	–3		3	µA
I_{OL}	Max output low current	V_{OL} = 0.4V	15			mA
I_{OL}	Max output low current	V_{OL} = 0.6V	20			mA
t_f	Fall time from 0.7 × V_{DD} to 0.3 × V_{DD}	V_{DD} = 1.8V, 10pF ≤ C_b ≤ 400pF	12		80	ns
		V_{DD} = 3.3V, 10pF ≤ C_b ≤ 400pF	12		150	ns
t_{SP}	I^2C pulse width suppressed				50	ns
C_I	Pin capacitance (internal)				10	pF
C_b	Capacitive load for each bus line (external)				400	pF
SDA and SCL Standard Mode Characteristics (Target)						
f_{SCLS}	Clock frequency for target	V_{DD} = 1.8V or 3.3V			100	kHz
$t_{VD;DAT}$	Valid data time	Transmitting Data, V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			3.45	µs
SDA and SCL Fast Mode Characteristics (Target)						
f_{SCLS}	Clock frequency for target	V_{DD} = 1.8V or 3.3V	100		400	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			0.9	µs
SDA and SCL Fast Mode Plus Characteristics (Target)						
f_{SCLS}	Clock frequency for Fast Mode Plus[1]	V_{DD} = 1.8V or 3.3V	400		800	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			0.55	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			0.55	µs

(1) Controller must control fSCLS to make sure tLOW > tVD; ACK.

5.19 Typical Characteristics

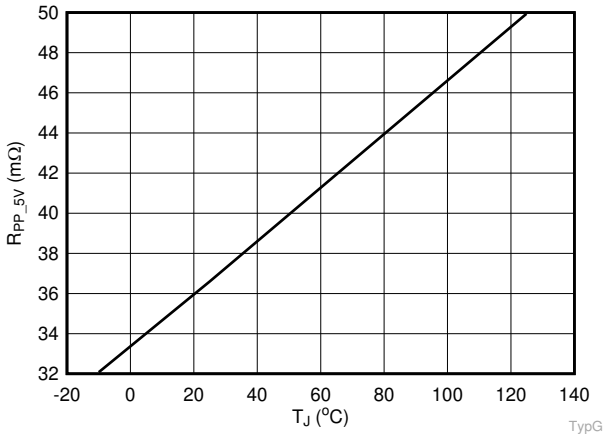


Figure 5-1. PP_5V Rdson vs Temperature

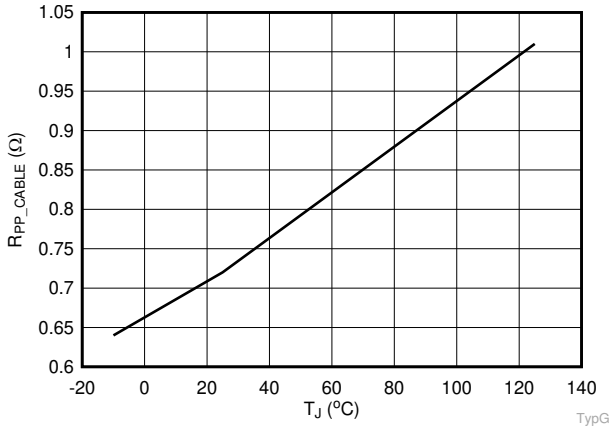


Figure 5-2. PP_CABLE Rdson vs Temperature

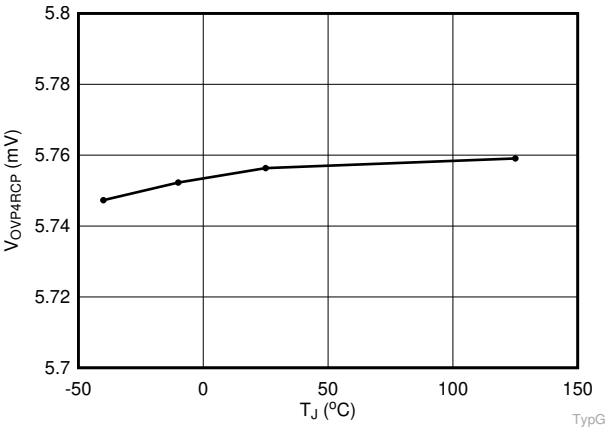


Figure 5-3. $V_{OVP4RCP}$ (Setting 2) vs Temperature

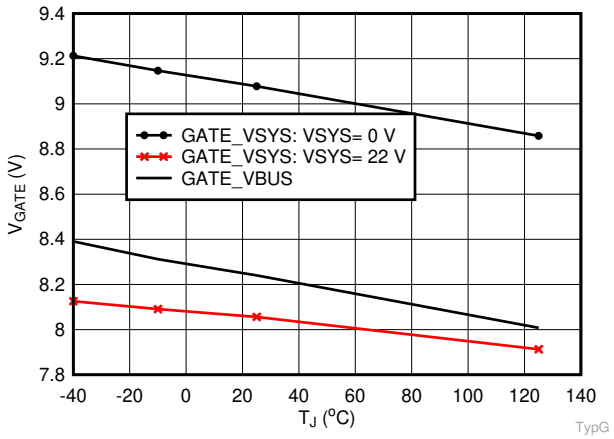


Figure 5-4. $V_{GATE\_VBUS\_ON}$ vs Temperature for TPS25752A

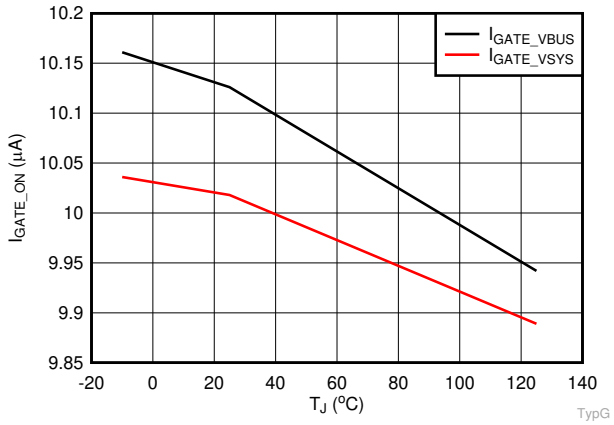


Figure 5-5. I_{GATE_ON} vs Temperature for TPS25752A

6 Parameter Measurement Information

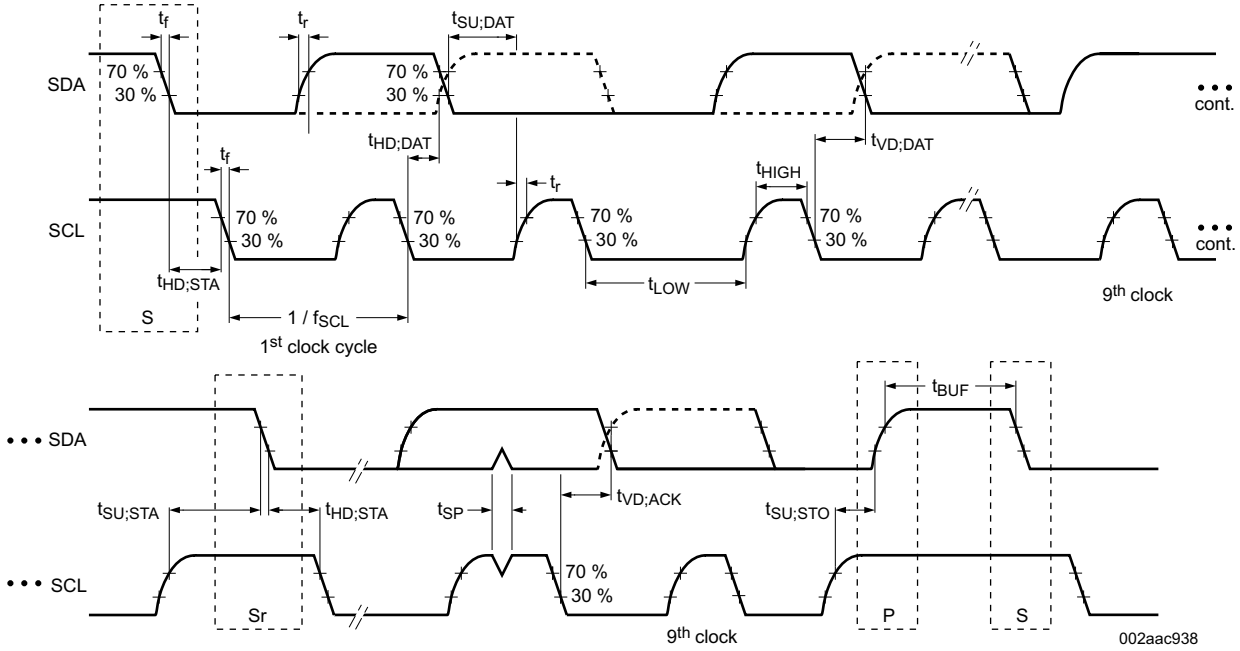


Figure 6-1. I²C Target Interface Timing

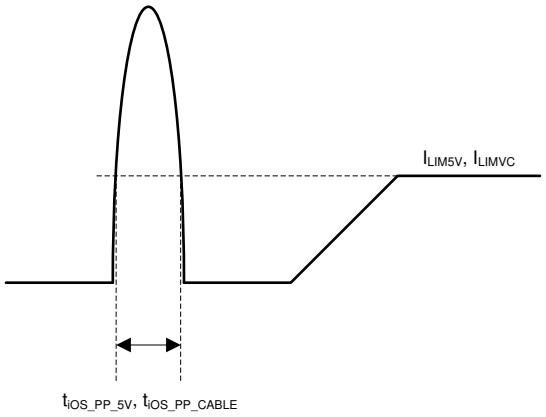


Figure 6-2. Short-circuit Response Time for Internal Power Paths PP_5V and PP_CABLE

7 Detailed Description

7.1 Overview

The TPS25752A is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for USB Type-C and PD receptacles. The TPS25752A communicates with the cable and another USB Type-C and PD device at the opposite end of the cable. The TPS25752A also a high voltage port power switch for sourcing.

The TPS25752A is divided into several main sections:

- USB-PD controller
- Cable plug and orientation detection circuitry
- Port power switches
- Power management circuitry
- Digital core

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the CC1 pin or the CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of features, and more detailed circuitry, see *USB-PD Physical Layer*.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of features, and more detailed circuitry, see *Cable Plug and Orientation Detection*.

The port power switches provide power to the VBUS pin and CC1 or CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of features, and more detailed circuitry, see *Power Paths*.

The power management circuitry receives and provides power to the TPS25752A internal circuitry and LDO_3V3 output. See *Power Management* for more information.

The digital core provides the engine for receiving, processing, and sending all USB-PD packets as well as handling control of all other TPS25752A functionality. A portion of the digital core contains ROM memory, which contains all the necessary firmware required to execute Type-C and PD applications. In addition, a section of the ROM, called boot code, is capable of initializing the TPS25752A, loading of the device configuration information, and loading any code patches into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of features, and more detailed circuitry, see *Digital Core*.

The TPS25752A has one I^2C controller to write to and read from external target devices such as a DC/DC or an optional external EEPROM memory (see *I2C Interface*).

The TPS25752A also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

7.2 Functional Block Diagram

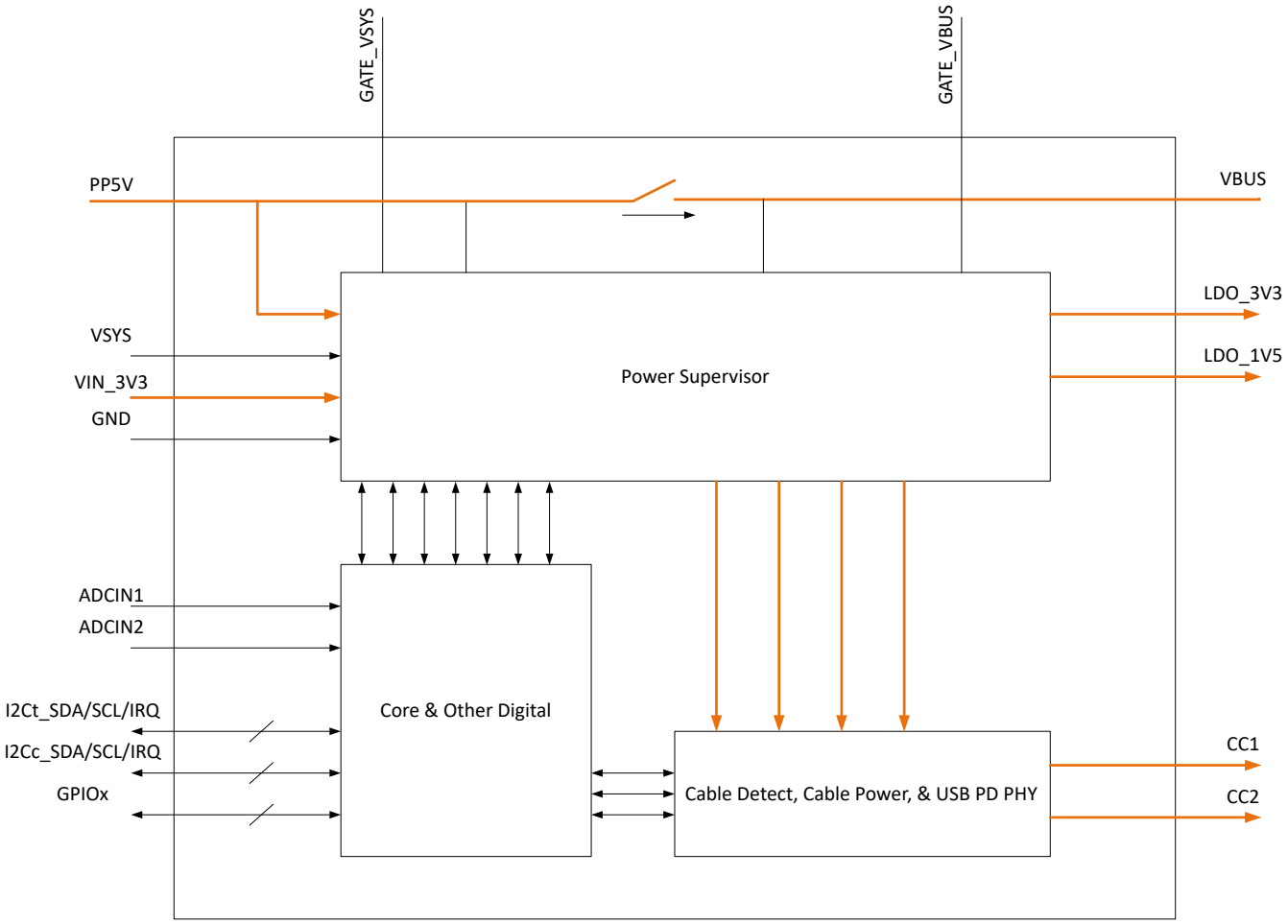


Figure 7-1. TPS25752A

7.3 Feature Description

7.3.1 USB-PD Physical Layer

Figure 7-2 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

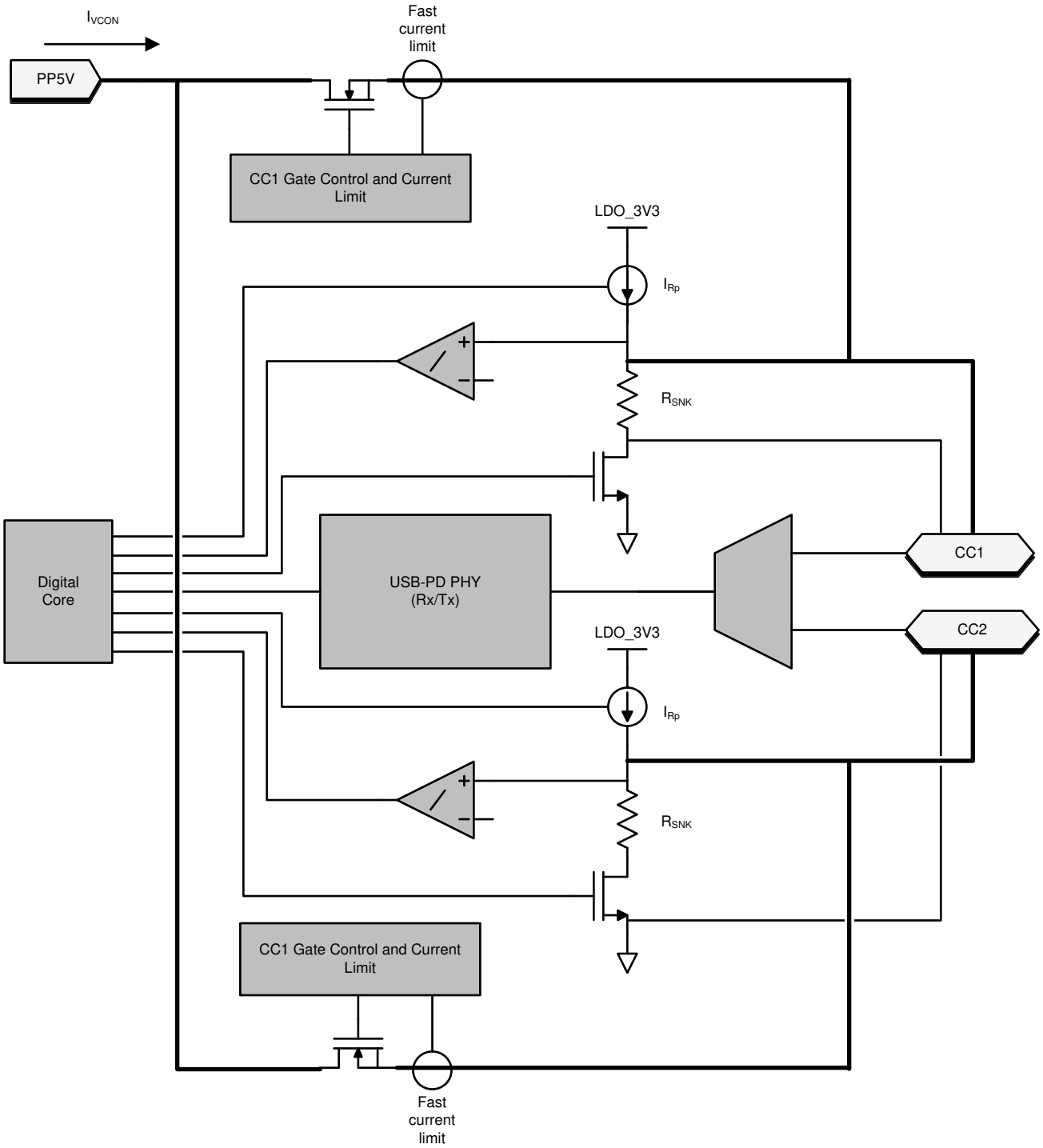


Figure 7-2. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (CC1 or CC2) that is DC biased due to the Rp (or Rd) cable attach mechanism.

7.3.1.1 USB-PD Encoding and Signaling

Figure 7-3 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 7-4 illustrates the high-level block diagram of the baseband USB-PD receiver.

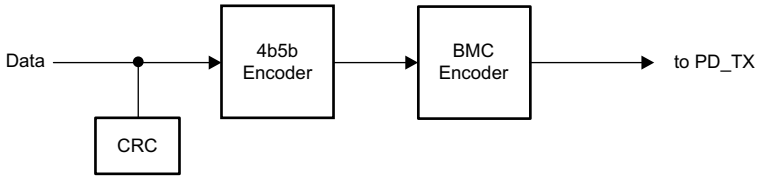


Figure 7-3. USB-PD Baseband Transmitter Block Diagram

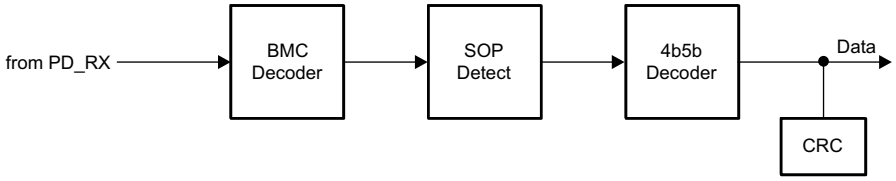


Figure 7-4. USB-PD Baseband Receiver Block Diagram

7.3.1.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS25752A is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). Biphase Mark Coding Example illustrates Biphase Mark Coding.

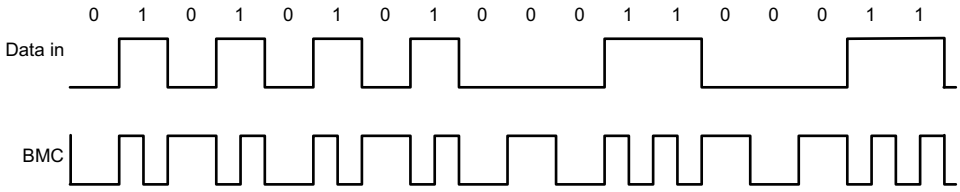


Figure 7-5. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the CC1 or CC2 pin with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to make sure the receiver clocks the final bit of EOP.

7.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Because a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate

that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the *USB-PD Specifications* for more details.

7.3.1.4 USB-PD BMC Transmitter

The TPS25752A transmits and receives USB-PD data over one of the CCy pins for a given CC pin pair (one pair per USB Type-C port). The CCy pins are also used to determine the cable orientation and maintain the cable/device attach detection. Thus, a DC bias exists on the CCy pins. The transmitter driver overdrives the CCy DC bias while transmitting, but returns to a Hi-Z state, allowing the DC voltage to return to the CCy pin when not transmitting. While either CC1 or CC2 can be used for transmitting and receiving, during a given connection only, the one that mates with the CC pin of the plug is used, so there is no dynamic switching between CC1 and CC2. USB-PD BMC TX/RX Block Diagram shows the USB-PD BMC TX and RX driver block diagram.

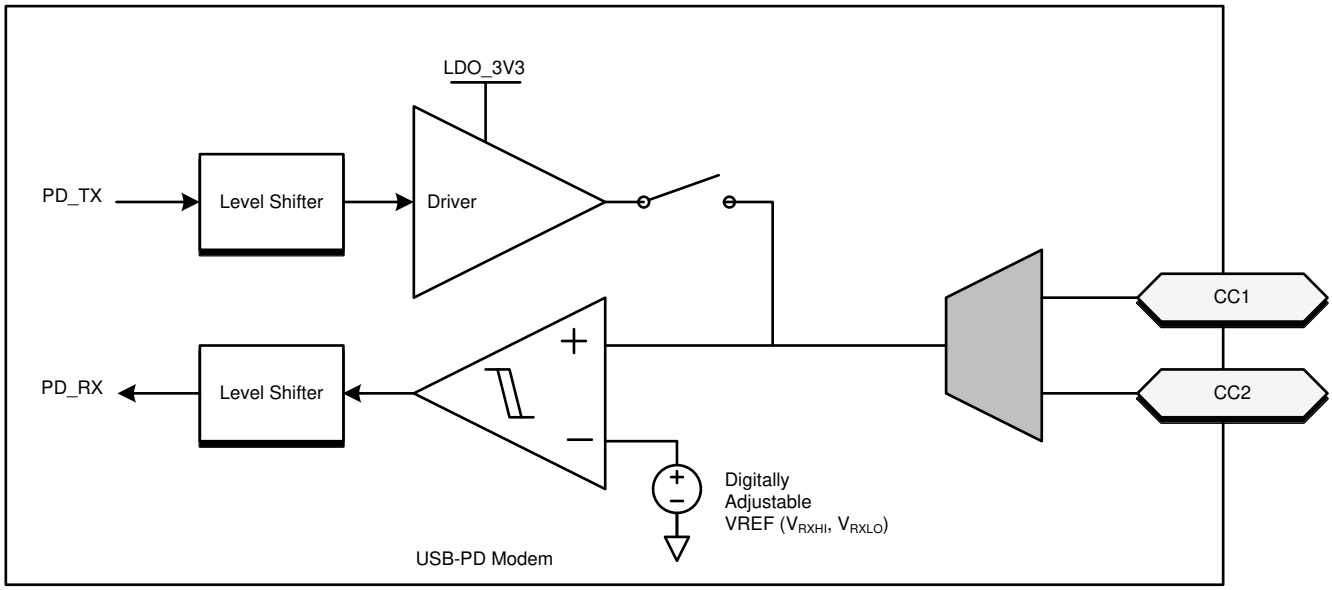


Figure 7-6. USB-PD BMC TX/RX Block Diagram

Figure 7-7 shows the transmission of the BMC data on top of the DC bias. Note that the DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach. This note means that the DC bias can be above or below the VOH of the transmitter driver.

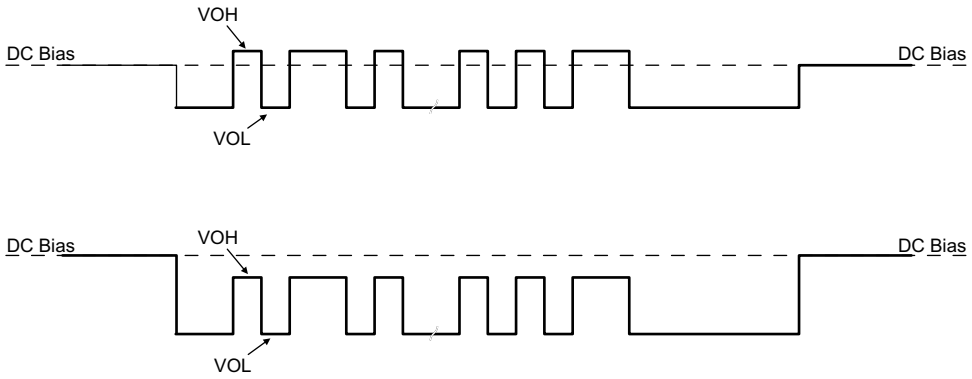


Figure 7-7. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the CCy lines. The signal peak, V_{TXHI}, is set to meet the TX masks defined in the *USB-PD Specifications*. Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of Z_{DRIVER}. Z_{DRIVER} is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. Z_{DRIVER} impacts the noise ingression in the cable.

ZDRIVER Circuit shows the simplified circuit determining Z_{DRIVER}. The circuit is specified such that noise at the receiver is bounded.

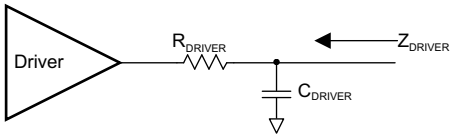


Figure 7-8. ZDRIVER Circuit

7.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS25752A receives a signal that follows the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

Example USB-PD Multi-Drop Configuration shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (Z_{BMCRX}). The *USB-PD Specification* also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

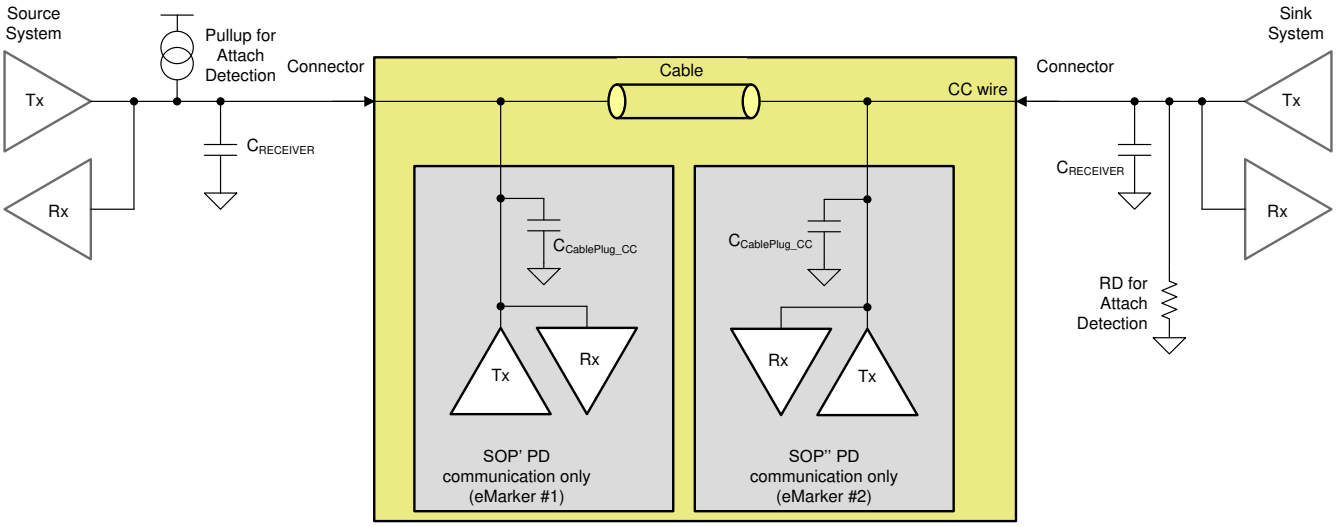


Figure 7-9. Example USB-PD Multi-Drop Configuration

7.3.1.6 Squelch Receiver

The TPS25752A has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification.

7.3.2 Power Management

The TPS25752A power management block receives power and generates voltages to provide power to the TPS25752A internal circuitry. These generated power rails are LDO_3V3 and LDO_1V5. LDO_3V3 can also be used as a low power output for external EEPROM memory. The power supply path is shown in Figure 7-10.

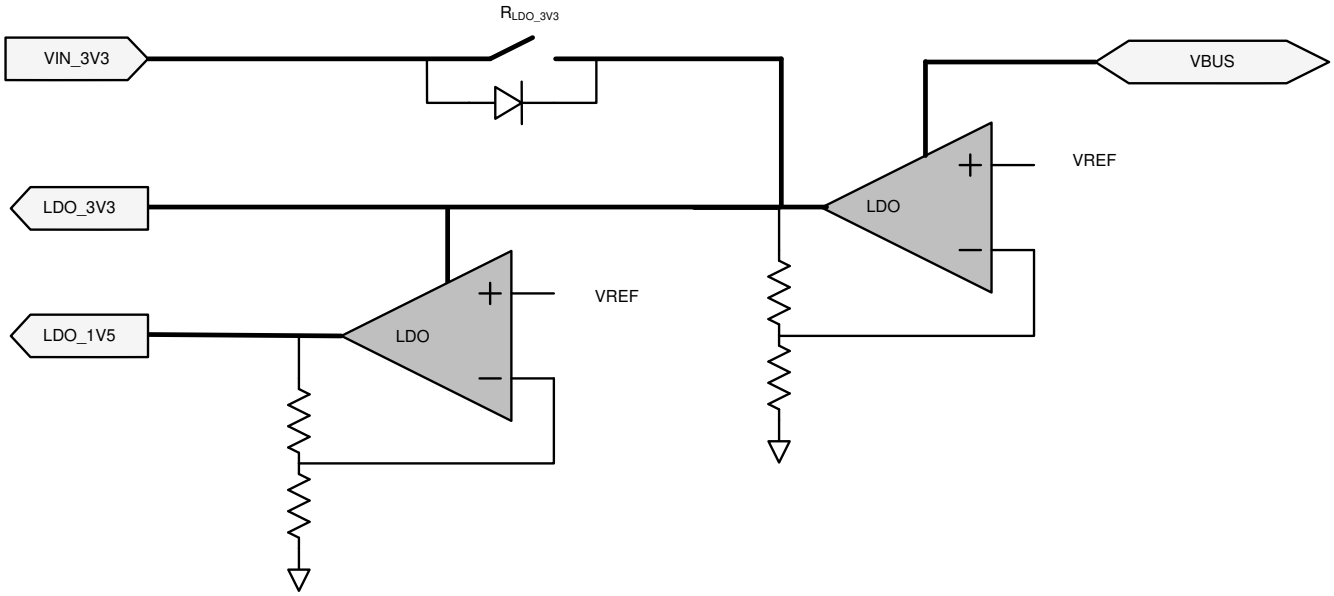


Figure 7-10. Power Supplies

The TPS25752A is powered from either VIN_3V3 or VBUS. The normal power supply input is VIN_3V3. When powering from VIN_3V3, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3V circuitry and I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V5 to power the 1.5V core digital circuitry. When powering from a VBUS input, the voltage on VBUS is stepped down through an LDO to LDO_3V3.

7.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

7.3.3 Power Paths

TPS25752A has a high voltage gate driver for power path control: PP_EXT. Each power path is described in detail in this section.

7.3.3.1 Internal Sourcing Power Paths

Figure 7-11 shows the TPS25752A internal sourcing power paths available in TPS25752A . The TPS25752A features two internal 5V sourcing power paths. The path from PP5V to VBUS is called PP_5V. The path from PP5V to CCx is called PP_CABLE. Each path contains two back-to-back common drain N-FETs, with current clamping protection, overvoltage protection, UVLO protection, and temperature sensing circuitry. PP_5V can conduct up to 3A continuously, while PP_CABLE can conduct up to 315mA continuously. When disabled, the blocking FET protects the PP5V rail from high-voltage that can appear on VBUS.

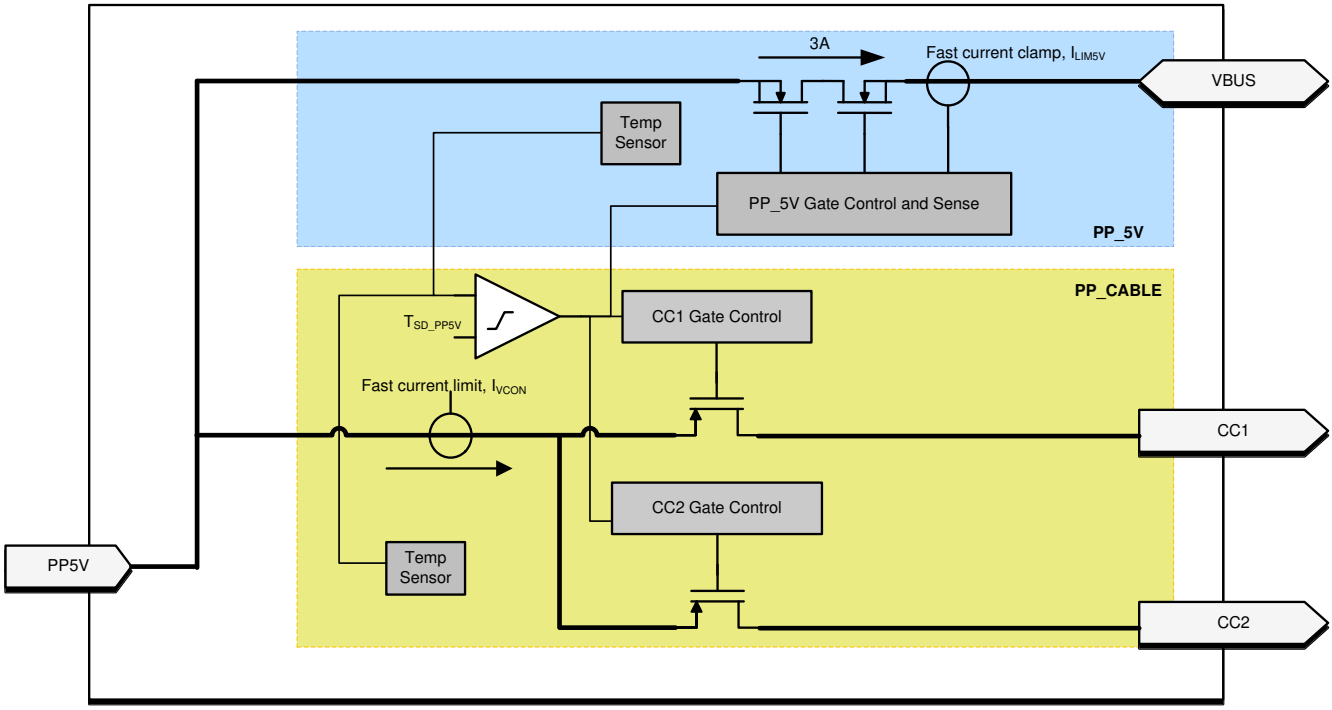


Figure 7-11. Port Power Switches

7.3.3.1.1 PP_5V Current Clamping

The current through the internal PP_5V path are current limited to I_{LIM5V}. The I_{LIM5V} value is configured by application firmware. When the current through the switch exceeds I_{LIM5V}, the current limiting circuit activates within $t_{iOS\_PP\_5V}$ and the path behaves as a constant current source. If the duration of the overcurrent event exceeds t_{ILIM}, the PP_5V switch is disabled.

7.3.3.1.2 PP_5V Local Overtemperature Shut Down (OTSD)

When PP_5V clamps the current, the temperature of the switch begin to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that $T_J > T_{SD\_PP5V}$, the PP_5V switch is disabled and the affected port enters the USB Type-C ErrorRecovery state.

7.3.3.1.3 PP_5V OVP

The overvoltage protection level is automatically configured based on the expected maximum V_{BUS} voltage, which depends upon the USB PD contract. When the voltage on the VBUS pin of a port exceeds the configured value ($V_{OVP4RCP}$) while PP_5V is enabled, then PP_5V is disabled within $t_{PP\_5V\_ovp}$ and the port enters into the Type-C ErrorRecovery state.

7.3.3.1.4 PP_5V UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}) while PP_5V is enabled, then PP_5V is disabled within $t_{PP\_5V\_uvlo}$ and the port that had PP_5V enabled enters into the Type-C ErrorRecovery state.

7.3.3.1.5 PP_5V Reverse Current Protection

If V_{VBUS} - V_{PP5V} > $V_{PP\_5V\_RCP}$, then the PP_5V path is automatically disabled within $t_{PP\_5V\_rcp}$. If the RCP condition clears, then the PP_5V path is automatically enabled within t_{ON}.

7.3.3.1.6 PP_CABLE Current Clamp

When enabled and providing VCONN power, the TPS25752A PP_CABLE power switch clamps the current to I_{VCON}. When the current through the PP_CABLE switch exceeds I_{VCON}, the current clamping circuit activates within $t_{iOS\_PP\_CABLE}$ and the switch behaves as a constant current source.

7.3.3.1.7 PP_CABLE Local Overtemperature Shut Down (OTSD)

When PP_CABLE clamps the current, the temperature of the switch begins to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that $T_J > T_{SD\_PP5V}$, the PP_CABLE switch is disabled and latched off within $t_{PP\_CABLE\_off}$. The port then enters the USB Type-C ErrorRecovery state.

7.3.3.1.8 PP_CABLE UVLO

If the PP5V pin voltage falls below the undervoltage lock out threshold (V_{PP5V_UVLO}), then the PP_CABLE switch is automatically disabled within $t_{PP\_CABLE\_off}$.

7.3.3.2 External Powerpath Control PP_EXT

The TPS25752A has two N-ch gate drivers designed to control a sourcing path from VSYS to VBUS. The charge pump for these gate drivers requires VBUS to be above V_{VBUS_UVLO}. The TPS25752A senses the VSYS and VBUS voltages to control the gate voltages to enable or disable the external FETs.

The high voltage power path control includes overvoltage protection (OVP), and reverse current protection (RCP). Adding resistance in series with a GATE pin of the TPS25752A and the gate pin of the N-ch MOSFET slows down the turnoff time when OVP or RCP occurs. Any such resistance must be minimized, and not allowed to exceed 3Ω.

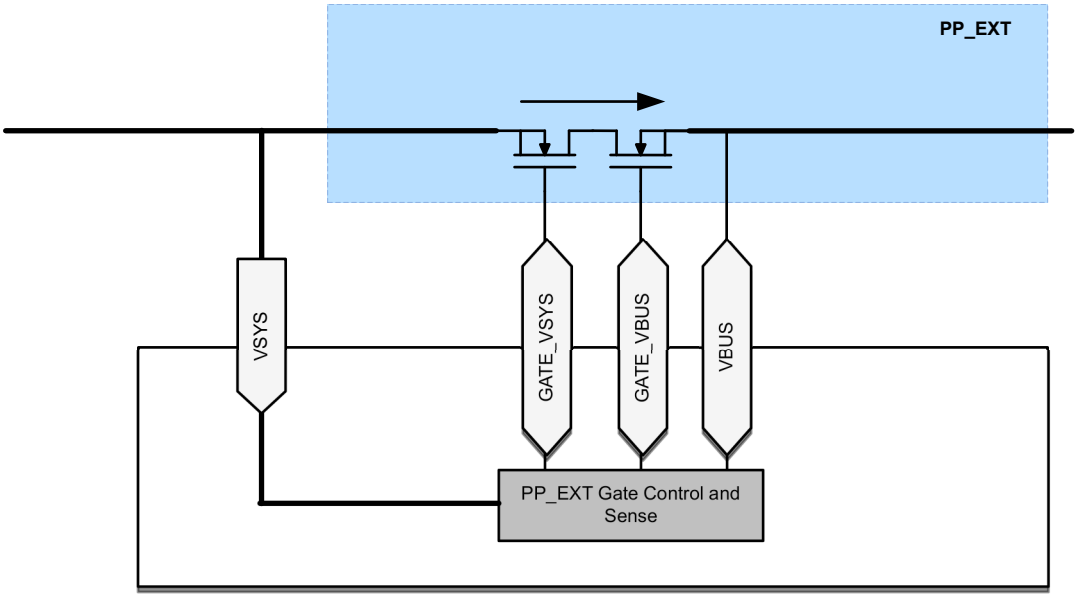


Figure 7-12. PP_EXT External Powerpath Control

Details of the VSYS Gate Driver shows the GATE_VSYS gate driver in more detail.

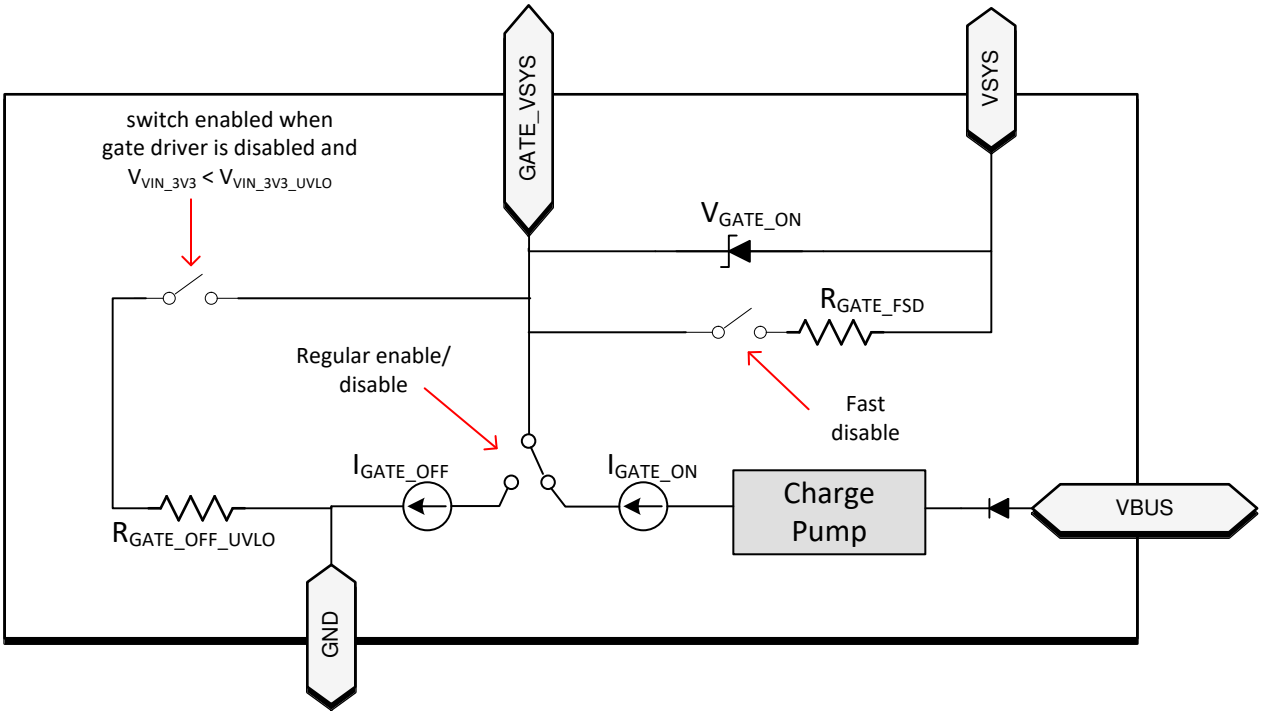


Figure 7-13. Details of the VSYS Gate Driver

7.3.3.2.1 Overvoltage Protection (OVP)

The application firmware enables the OVP and configures the device based on the expected VBUS voltage. When the VBUS voltage surpasses the overvoltage protection parameters, the external powerpath is disabled. If the voltage on VBUS surpasses the configured threshold $V_{OVP4VSYS}$ = $V_{OVP4RCP}/r_{OVP}$, then GATE_VSYS is automatically disabled within t_{PPHV_FSD} to protect the system.

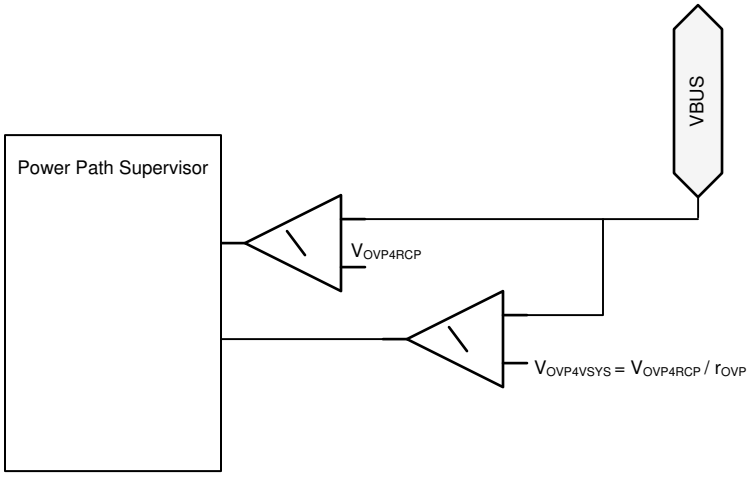


Figure 7-14. Diagram for OVP Comparators

7.3.3.2.2 VBUS UVLO

The TPS25752A monitors VBUS voltage and detects when the voltage falls below V_{VBUS_UVLO}. When the UVLO condition is detected, GATE_VBUS is disabled within t_{PPHV_RCP}. When the UVLO condition is cleared, GATE_VBUS is re-enabled within t_{PPHV_ON}.

7.3.3.2.3 Discharging VBUS to Safe Voltage

The TPS25752A has an integrated active pulldown (I_{DSCH}) on VBUS for discharging from high voltage to VSAFE0V (0.8V). This discharge is applied when the device is in an Unattached Type-C state.

7.3.4 Cable Plug and Orientation Detection

Figure 7-15 shows the plug and orientation detection block at each CCy pin (CC1, CC2). Each pin has identical detection circuitry.

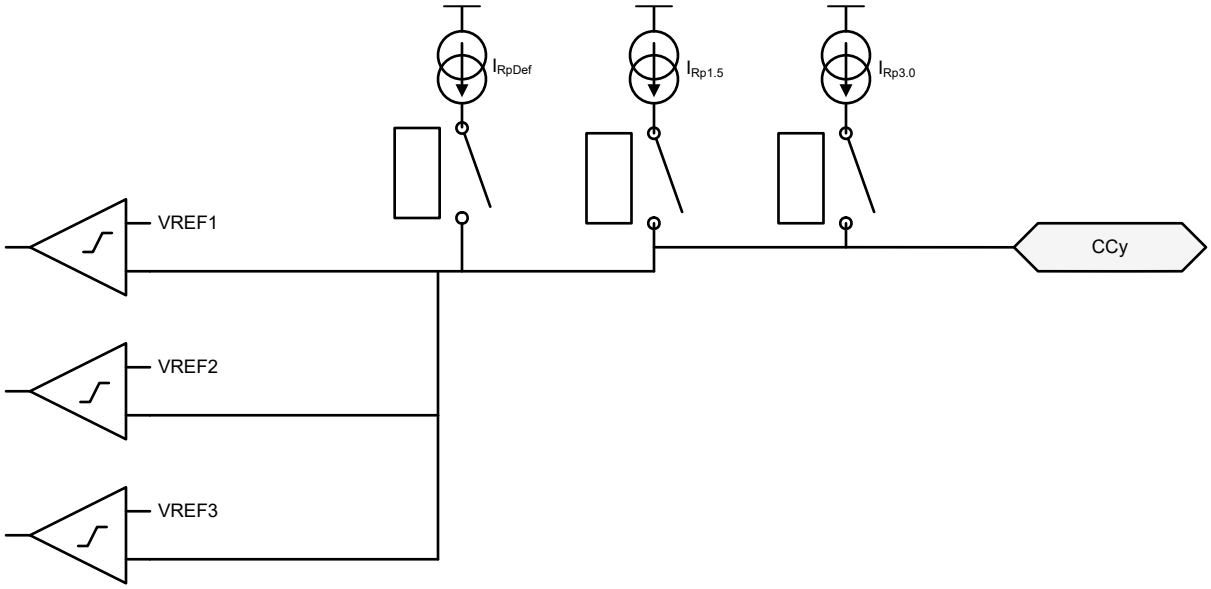


Figure 7-15. Plug and Orientation Detection Block

7.3.4.1 Configured as a Source

When configured as a source, the TPS25752A detects when a cable or a Sink is attached using the CC1 and CC2 pins. When in a disconnected state, the TPS25752A monitors the voltages on these pins to determine what, if anything, is connected. See *USB Type-C Specification* for more information.

Cable Detect States for a Source shows the cable detect states for a source.

Table 7-1. Cable Detect States for a Source

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both CCy pins for attach. Power is not applied to VBUS or VCONN.
Rd	Open	Sink attached	Monitor CC1 for detach. Power is applied to VBUS but not to VCONN (CC2).
Open	Rd	Sink attached	Monitor CC2 for detach. Power is applied to VBUS but not to VCONN (CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor CC2 for a Sink attach and CC1 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Open	Ra	Powered Cable-No UFP attached	Monitor CC1 for a Sink attach and CC2 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN CC1) then monitor CC2 for a Sink detach. CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (CC2) then monitor CC1 for a Sink detach. CC2 is not monitored for a detach.

Table 7-1. Cable Detect States for a Source (continued)

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Rd	Rd	Debug Accessory Mode attached	Sense either CCy pin for detach.
Ra	Ra	Corrosion Mitigation	Sense either CCy pin for detach.

When a TPS25752A port is configured as a Source, a current I_{RpDef} is driven out each CCy pin and each pin is monitored for different states. When a Sink is attached to the pin, a pulldown resistance of Rd to GND exists. The current I_{RpDef} is then forced across the resistance Rd, generating a voltage at the CCy pin. The TPS25752A applies I_{RpDef} until the device closes the switch from PP5V to VBUS, at which time application firmware can change to $I_{Rp1.5A}$ or $I_{Rp3.0A}$.

When the CCy pin is connected to an active cable VCONN input, the pulldown resistance is different (Ra). In this case, the voltage on the CCy pin lowers the PD controller recognizes the pulldown as an active cable.

The voltage on CCy is monitored to detect a disconnection depending upon which Rp current source is active. When a connection has been recognized and the voltage on CCy subsequently rises above the disconnect threshold for t_{CC}, the system registers a disconnection.

7.3.5 Overvoltage Protection (CC1, CC2)

The TPS25752A detects when the voltage on the CC1 or CC2 pin is too high or there is reverse current into the PP5V pin and takes action to protect the system. The protective action is to disable PP_CABLE within $t_{PP\_CABLE\_FSD}$ and disable the USB PD transmitter.

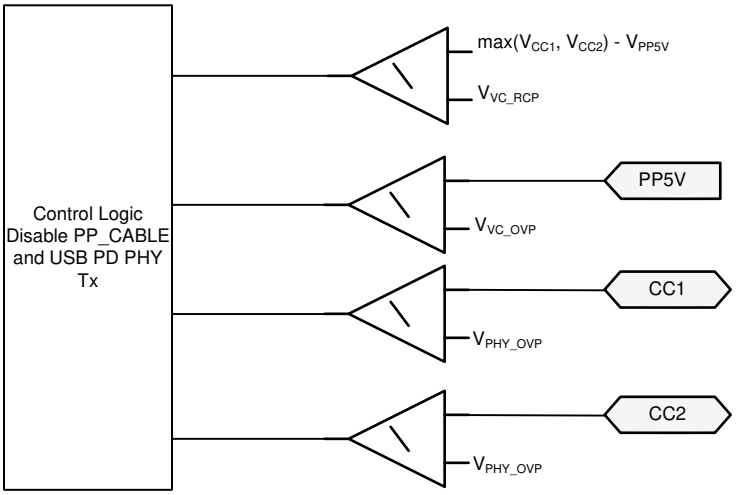


Figure 7-16. Overvoltage and Reverse Current Protection for CC1 and CC2

7.3.6 Default Behavior Configuration (ADCIN1, ADCIN2)

Note

This functionality is firmware controlled and subject to change.

The ADCINx pins must be externally tied to the LDO_3V3 pin via a resistive divider as shown in the following figure. At power-up the ADC converts the ADCINx voltage and the digital core uses these two values to determine start-up behavior. The available start-up configurations include options for I^2C target address of I2Ct_SCL/SDA, and default configuration.

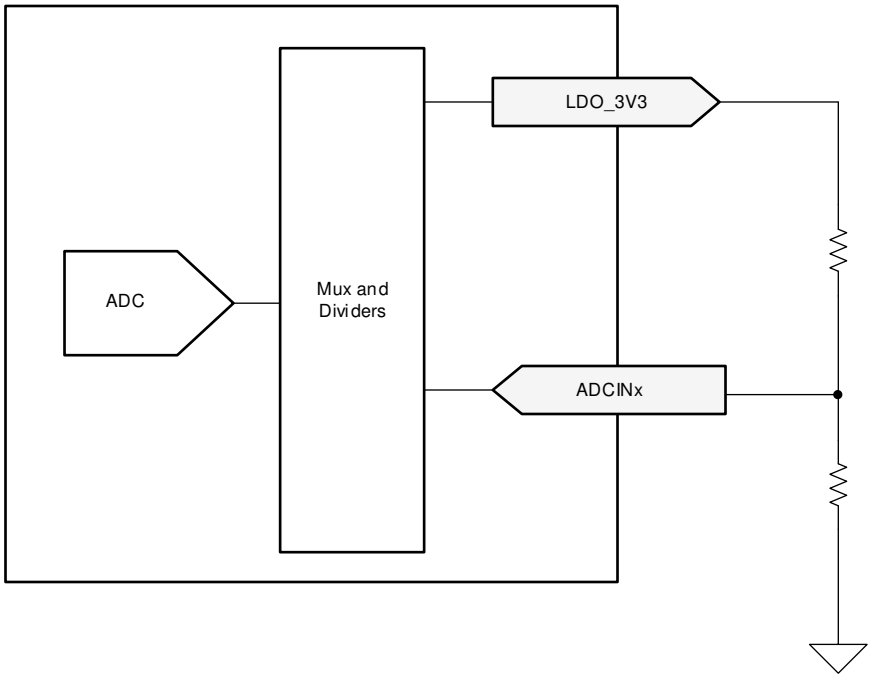


Figure 7-17. ADCINx Resistor Divider

The device behavior is determined in several ways depending upon the decoded value of the ADCIN1 and ADCIN2 pins. The following table shows the decoded values for different resistor divider ratios. See *Pin Strapping to Configure Default Behavior* for details on how the ADCINx configurations determine default device behavior. See *I²C Address Setting* for details on how ADCINx decoded values affects default I²C target address.

Table 7-2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1)			Without Using R_{UP} or R_{DOWN}	ADCINx Decoded Value(2)
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

(1) See *I²C Address Setting* to see the exact meaning of I²C Address Index.
(2) See *Pin Strapping to Configure Default Behavior* for how to configure a given ADCINx decoded value.

7.3.7 ADC

The TPS25752A ADC is shown in Figure 7-18. The ADC is an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware.

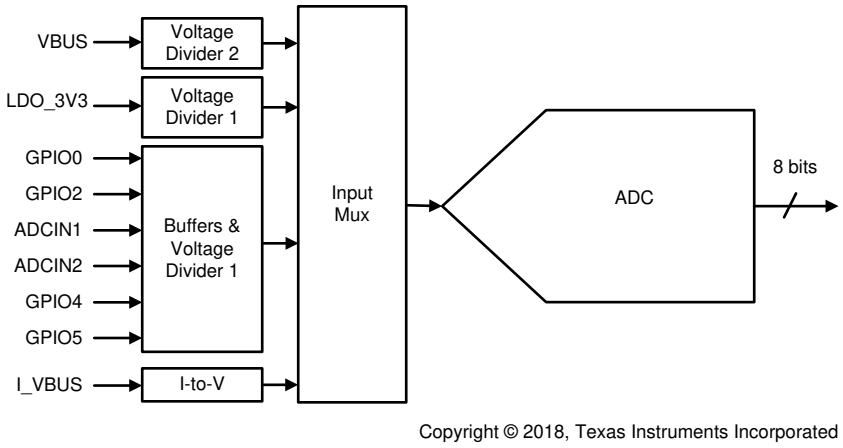


Figure 7-18. SAR ADC

7.3.8 Liquid Detection

The TPS25752A features liquid detection and corrosion mitigation through monitoring the voltage on pins from the connector. The device monitors pins periodically checking for variations on the pin voltage indicating a short. When configured for corrosion mitigation, the PD controller disconnects from the far end device and monitors for voltage readings indicating the liquid is no longer present.

For additional information, refer to the Section 8 section.

7.3.9 BC 1.2 (USB_P, USB_N)

The TPS25752A supports BC 1.2 as a Downstream Port using the hardware shown in .

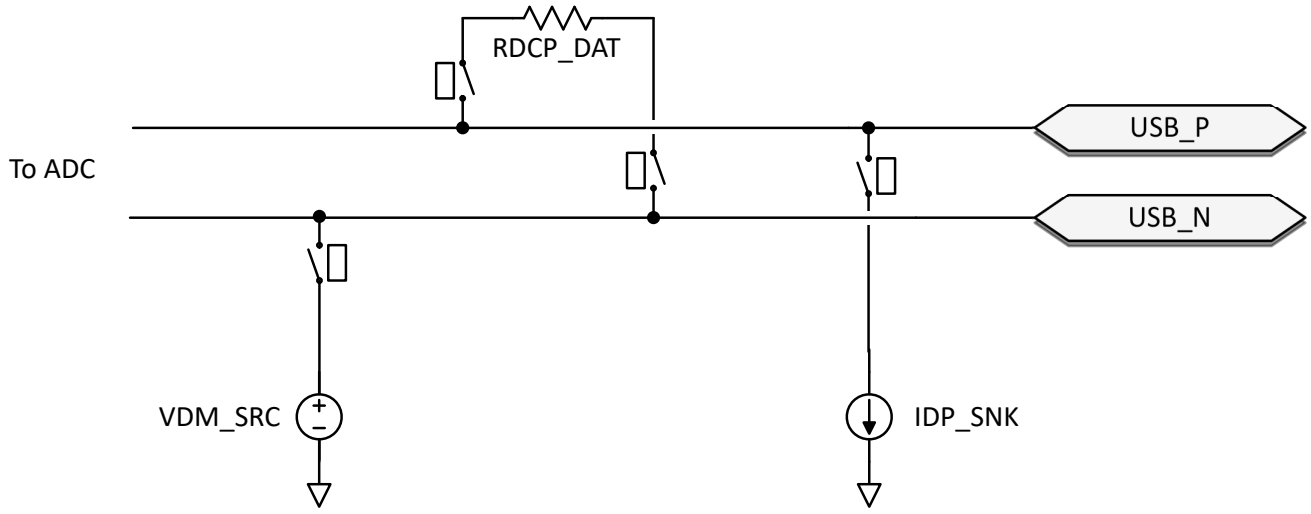


Figure 7-19. BC1.2 Hardware Components

7.3.10 Digital Interfaces

The TPS25752A contains several different digital interfaces which can be used for communicating with other devices. The available interfaces include one I^2C controller, one I^2C target and additional GPIOs.

7.3.10.1 General GPIO

GPIOx pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input. The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO_RPU resistance in series with the drain. The supply voltage to the output buffer is LDO_3V3 and LDO_1V5 to the input buffer. When interfacing with non 3.3V I/O devices the output buffer can be configured as an open drain output and an external pull-up resistor attached to the GPIO pin. The pull-up and pull-down output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

Table 7-3. GPIO Functionality Table

PIN NAME	TYPE	SPECIAL FUNCTIONALITY
GPIO0	I/O	General-purpose input or output, or LD1 for Liquid Detection
GPIO1	I/O	General-purpose input or output
GPIO2	I/O	General-purpose input or output, or LD2 for Liquid Detection
GPIO3	I/O	General-purpose input or output
GPIO4	I/O	D+, general-purpose input or output
GPIO5	I/O	D-, general-purpose input or output
GPIO6	I/O	General-purpose input or output
GPIO7	I/O	General-purpose input or output
$\overline{\text{I2Ct\_IRQ}}$(GPIO10)	O	IRQ for optional I2Ct, or used as a general-purpose output
GPIO11	O	General-purpose output
$\overline{\text{I2Cc\_IRQ}}$(GPIO12)	I	IRQ for I2Cc, or used as a general-purpose input

7.3.10.2 I²C Interface

The TPS25752A features two I²C interfaces that use an I²C I/O driver like the one shown in Figure 7-20. This I/O consists of an open-drain output and an input comparator with de-glitching.

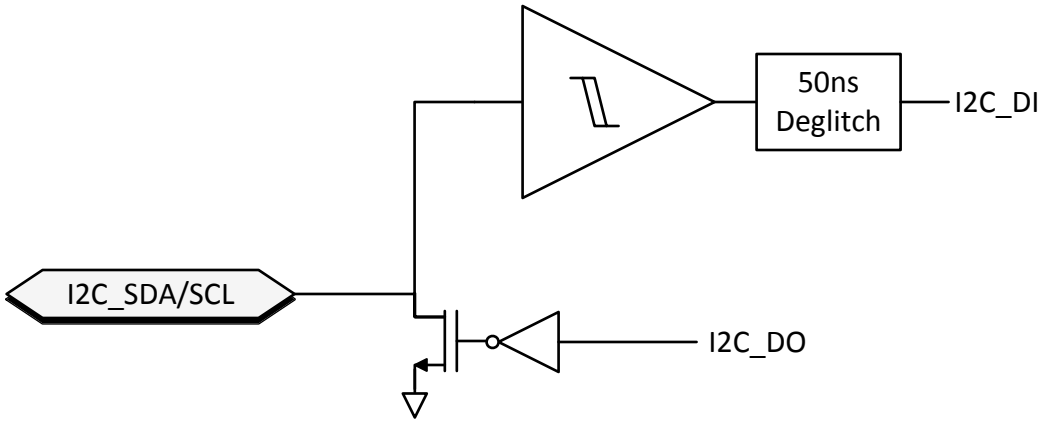


Figure 7-20. I²C Buffer

The TPS25752A has one I2C target interface ports: I2Ct. I2C port I2Ct is comprised of the I2Ct_SDA, I2Ct_SCL, and $\overline{\text{I2Ct\_IRQ}}$ pins. This interface provide general status information about the TPS25752A, as well as the ability to control the TPS25752A behavior, supporting communications to/from a connected device and/or cable supporting BMC USB-PD, and providing information about connections detected at the USB-C receptacle.

When the TPS25752A is in 'APP' mode TI recommends to use standard mode or Fast mode (that is a clock speed no higher than 400kHz). However, in the BOOT mode when a patch bundle is loaded Fast Mode Plus can be used (see f_{SCLS}).

The TPS25752A has one I²C controller interface port. I²C is comprised of the I2Cc_SDA, I2Cc_SCL, and $\overline{\text{I2Cc\_IRQ}}$ pins. This interface can be used to read from or write to external target devices.

During boot, the TPS25752A attempts to read patch and Application Configuration data from an external EEPROM with a 7-bit target address of 0x50. The EEPROM must be at least 32 kilo-bytes.

Table 7-4. I²C Summary

I²C BUS	TYPE	TYPICAL USAGE
I2Ct	Target	Optionally can be connected to an external MCU. Also used to load the patch and application configuration.
I2Cc	Controller	Connect to a I²C EEPROM, DC/DC. Use the LDO_3V3 pin as the pullup voltage. Multi-controller configuration is not supported.

7.3.10.2.1 I²C Interface Description

The TPS25752A supports Standard and Fast mode I²C interfaces. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pullup resistor. Data transfer can be initiated only when the bus is not busy.

A controller sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The controller sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a target receiver is addressed, it must generate an ACK after each byte is received. Similarly, the controller must generate an ACK after each byte that it receives from the target transmitter. Setup and hold times must be met for proper operation.

A controller receiver signals an end of data to the target transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the target by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

Figure 7-21 shows the start and stop conditions of the transfer. Figure 7-22 shows the SDA and SCL signals for transferring a bit. Figure 7-23 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

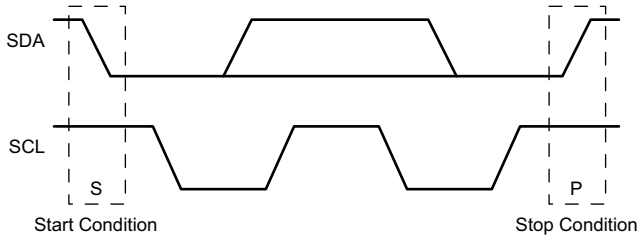


Figure 7-21. I²C Definition of Start and Stop Conditions

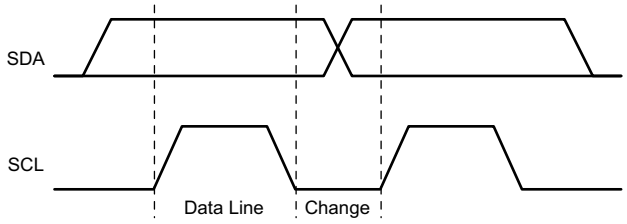


Figure 7-22. I²C Bit Transfer

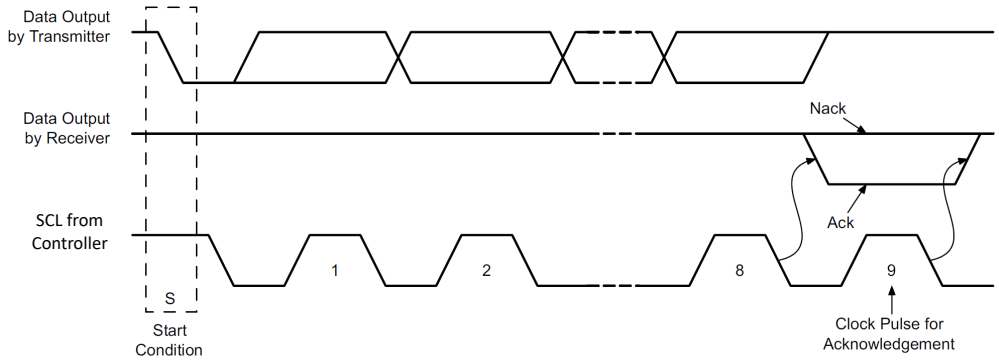


Figure 7-23. I²C Acknowledgment

7.3.10.2.1.1 I²C Clock Stretching

The TPS25752A features clock stretching for the I²C protocol. The TPS25752A target I²C port can hold the clock line (SCL) low after receiving (or sending) a byte, indicating that the bus is not yet ready to process more data. The controller communicating with the target must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the target is clock stretching, the clock line remains low.

The controller must wait until the clock line transitions high plus an additional minimum time (4µs for standard 100kbps I²C) before pulling the clock low again.

Any clock pulse can be stretched and typically the clock pulse before or after the acknowledgment bit is stretched.

7.3.10.2.1.2 I²C Address Setting

The I2C controller must only use I2Ct_SCL/SDA for loading a patch bundle.

Once the boot process is complete, the port has a unique target address on the I2Ct_SCL/SDA bus as selected by the ADCINx pins.

Table 7-5. I²C Default Target Address for I2Ct_SCL/SDA.

I²C ADDRESS INDEX (DECODED FROM ADCIN1 AND ADCIN2)(1)	TARGET ADDRESS								AVAILABLE DURING BOOT
	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	
#1	0	1	0	0	0	0	0	R/W	Yes
#2	0	1	0	0	0	0	1	R/W	Yes
#3	0	1	0	0	0	1	0	R/W	Yes
#4	0	1	0	0	0	1	1	R/W	Yes

(1) See *Pin Strapping to Configure Default Behavior* details about ADCIN1 and ADCIN2 decoding.

7.3.10.2.1.3 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C controller and a single TPS25752A. The I²C target sub-address is used to receive or respond to Host Interface protocol commands. Figure 7-24 and Figure 7-25 show the write and read protocol for the I²C target interface, and a key is included in Figure 7-26 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

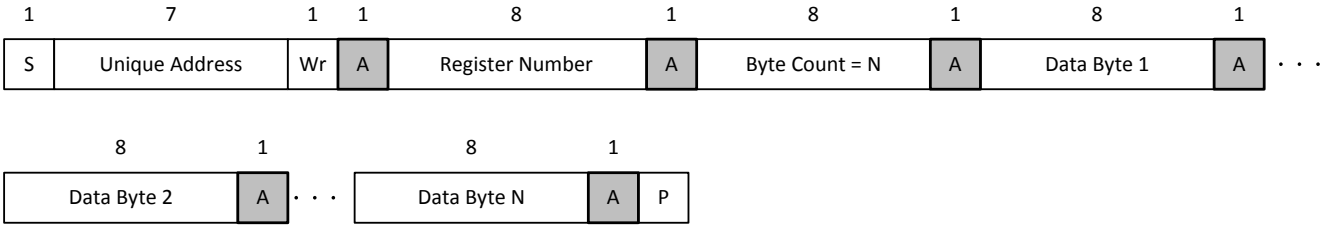


Figure 7-24. I²C Unique Address Write Register Protocol

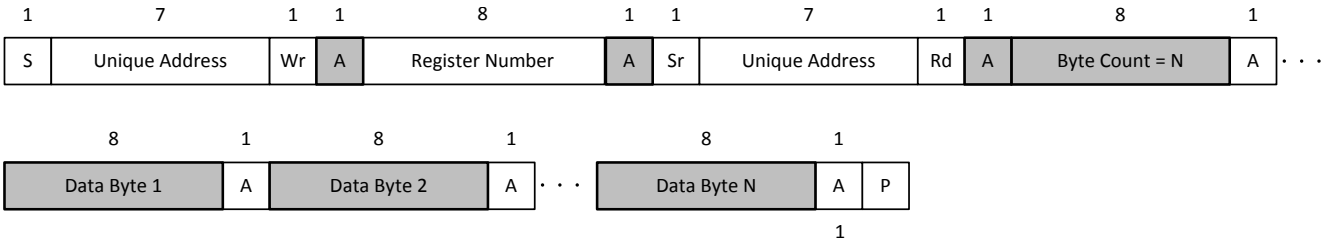
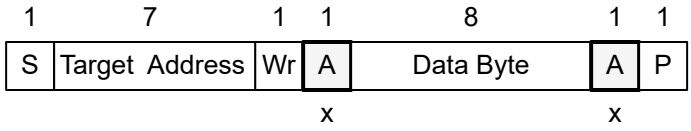


Figure 7-25. I²C Unique Address Read Register Protocol



S Start condition
SR Repeated start condition
Rd Read (bit value of 1)
Wr Write (bit value of 0
X Field is required to have the value x
A Acknowledge (this bit position is either 0 for an ACK or 1 for a NACK)
P Stop condition

Controller-to-target

Target-to-controller

• • • Continuation of protocol

Figure 7-26. I²C Read/Write Protocol Key

7.3.10.2.1.4 Pin Strapping to Configure Default Behavior

During the boot procedure, the device reads the ADCINx pins and set the configurations based on the table below. The device then attempts to load a configuration from an external EEPROM on the I2Cc bus. If no EEPROM is detected, then the device waits for an external host to load a configuration.

When an external EEPROM is used, each device is connected to a unique EEPROM, and cannot be shared for multiple devices. The external EEPROM is set at 7-bit target address 0x50.

Table 7-6. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 DECODED VALUE[2]	ADCIN2 DECODED VALUE[2]	I²C ADDRESS INDEX[1]
7	0	#1
0	0	#2
6	0	#3
5	7	#4

(1) See Table 7-5 to see the exact meaning of I²C Address Index.
(2) See Decoding of ADCIN1 and ADCIN2 for how to configure a given ADCINx decoded value.

7.3.11 Digital Core

Figure 7-27 shows a simplified block diagram of the digital core.

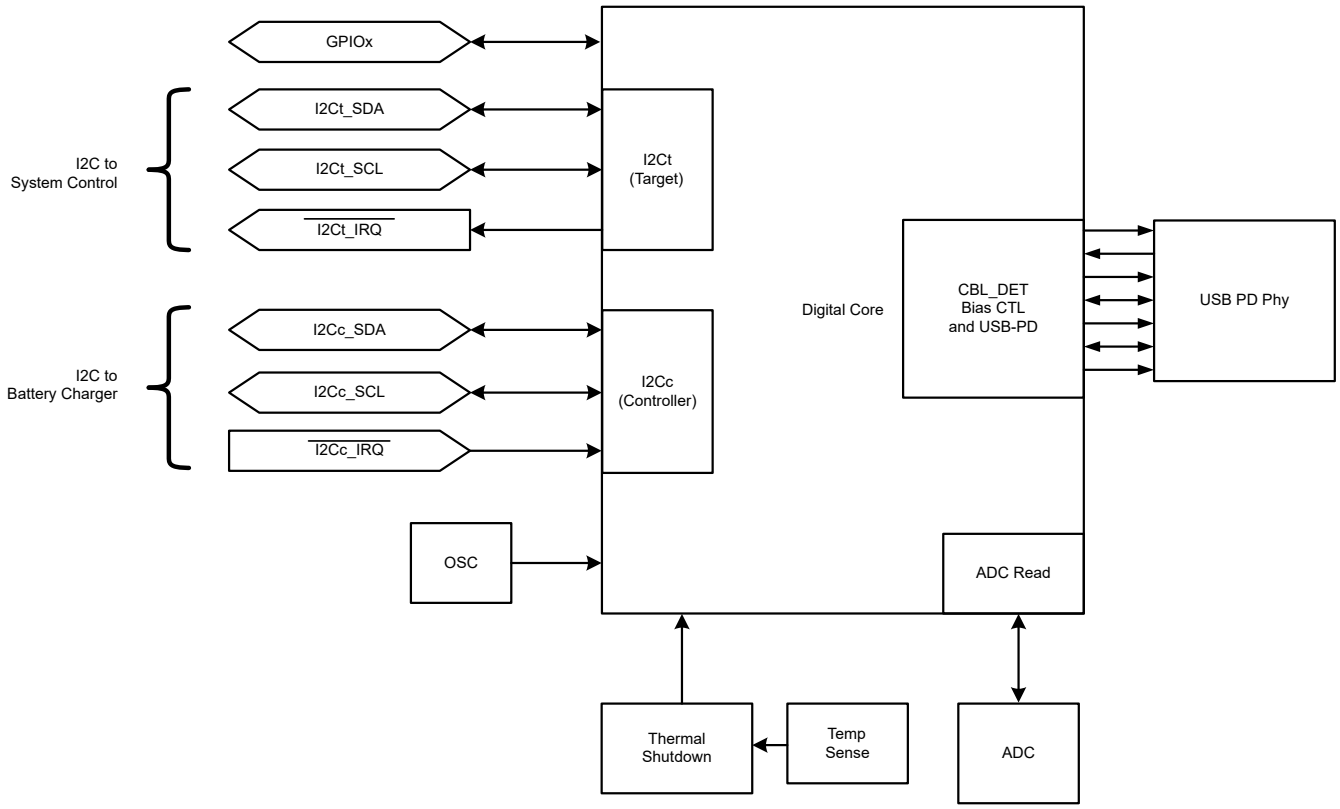


Figure 7-27. Digital Core Block Diagram

7.4 Device Functional Modes

7.4.1 Power States

The TPS25752A can operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in Section 5.7. The device automatically transitions between the three power states based on the circuits that are active and required. See Figure 7-28. In the Sleep state, the TPS25752A detects a Type-C connection. Transitioning between the Active mode to Idle mode requires a period of time (T) without any of the following activity:

- Incoming USB PD message
- Change in CC status
- GPIO input event
- I^2C transactions
- Voltage alert
- Fault alert

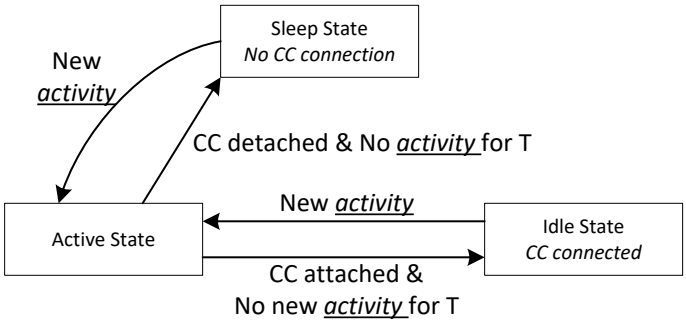


Figure 7-28. Flow Diagram for Power States

Table 7-7. Power Consumption States

	ACTIVE PP_5V SOURCE MODE(1)	ACTIVE PP_HV SOURCE MODE3	IDLE PP_5V SOURCE MODE	IDLE PP_HV SOURCE MODE	SLEEP MODE2
PP_5V	Enabled	Disabled	Enabled	Disabled	Disabled
PP_EXT (TPS25752A)	Enabled	Enabled	Enabled	Enabled	Disabled
PP_CABLE	Enabled	Enabled	Enabled	Enabled	Disabled
External CC1 Termination	Rd	Rd	Rd	Rd	Open
External CC2 Termination	Open	Open	Open	Open	Open

(1) This mode is used for: $I_{VIN\_3V3,ActSrc}$
(2) This mode is used for: $I_{VIN\_3V3,Sleep}$
(3) This mode is used for: $I_{VIN\_3V3,ActSnk}$

7.4.2 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS25752A during sudden disconnects due to inductive effects in a cable, TI recommends that a Schottky diode be placed from VBUS to ground.

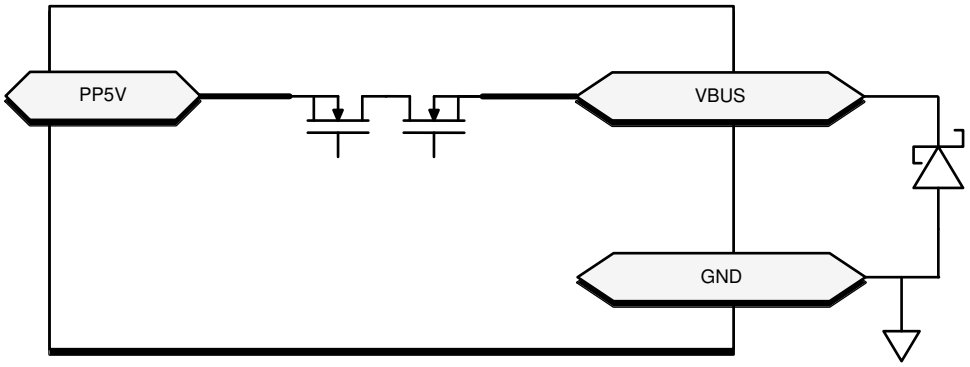


Figure 7-29. TPS25752AS Schottky for Current Surge Protection

7.4.3 Thermal Shutdown

The TPS25752A features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of T_{SD_MAIN}. The temperature shutdown has a hysteresis of T_{SD_MAIN} and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal PP5V-to-VBUS power path and disables both power paths and the VCONN power path when either exceeds T_{SD_PP5V}. The temperature shutdown has a hysteresis of T_{SD_PP5V} and when the temperature falls back below this value, the path can be configured to resume operation or remain disabled until re-enabled by firmware.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS25752A is a stand-alone Type-C PD controller for power-only USB-PD applications. The USBCPD Application Customization Tool provides a graphical interface for configuring the TPS25752A including power role, data role, external DCDC integration, GPIO, and liquid detection. The Web Tool generates a binary image that is programmed onto the device during boot. The PD controller loads the device configuration from an external EEPROM or MCU through the I²C interface.

The TPS25752A is applicable in single port power applications supporting the following PD architectures.

- Designs for Power Provider (Source)

8.2 Typical Application

The following block diagram provides an example of a complete system architecture; certain blocks may not be applicable in all designs.

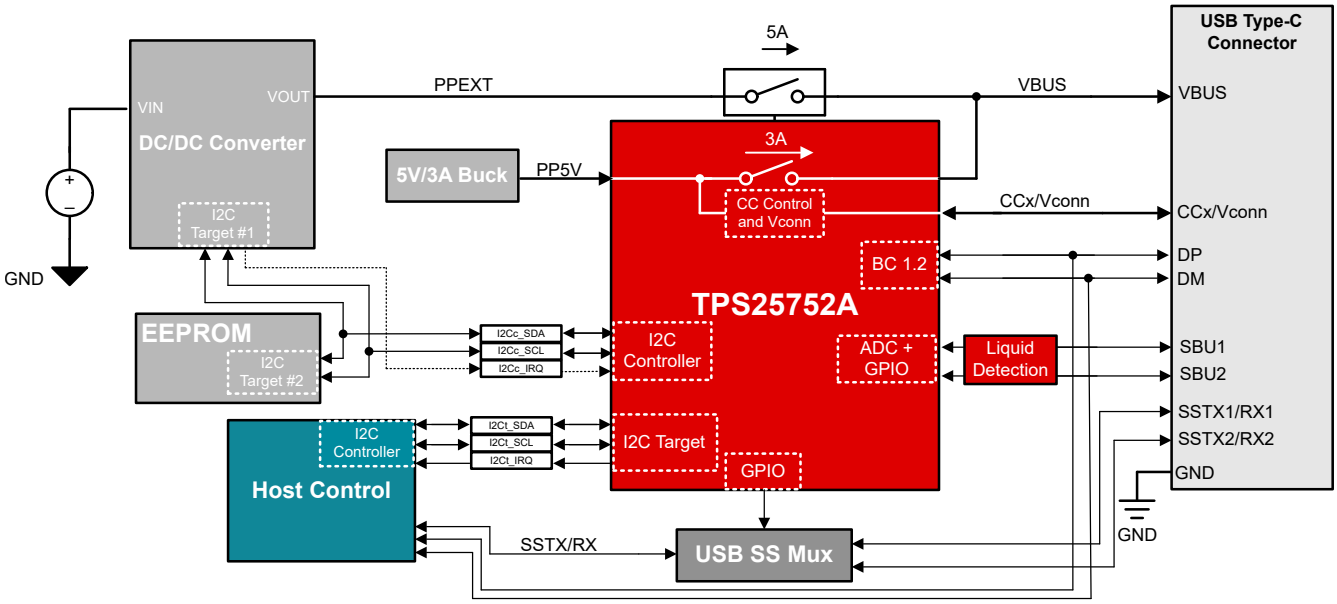


Figure 8-1. TPS25752A DC/DC Converter and Full System Block Diagram

8.2.1 Design Requirements

8.2.1.1 Liquid Detection Design Requirements

Liquid detection is a safety and protection mechanism used in USB Type-C ports to detect the presence of moisture or debris. The TPS25752A supports detecting liquid by measuring the leakage voltage between pins on the Type-C connector using dedicated internal ADC pins. Table 8-1 shows examples of various shorts that can occur in both connected and unconnected states.

Table 8-1. Liquid Detection Resistive Short Examples

Resistor	Description
RSaV	Resistive short to VBUS
RSaCC	Resistive short to CC
RSaG	Resistive short to GND

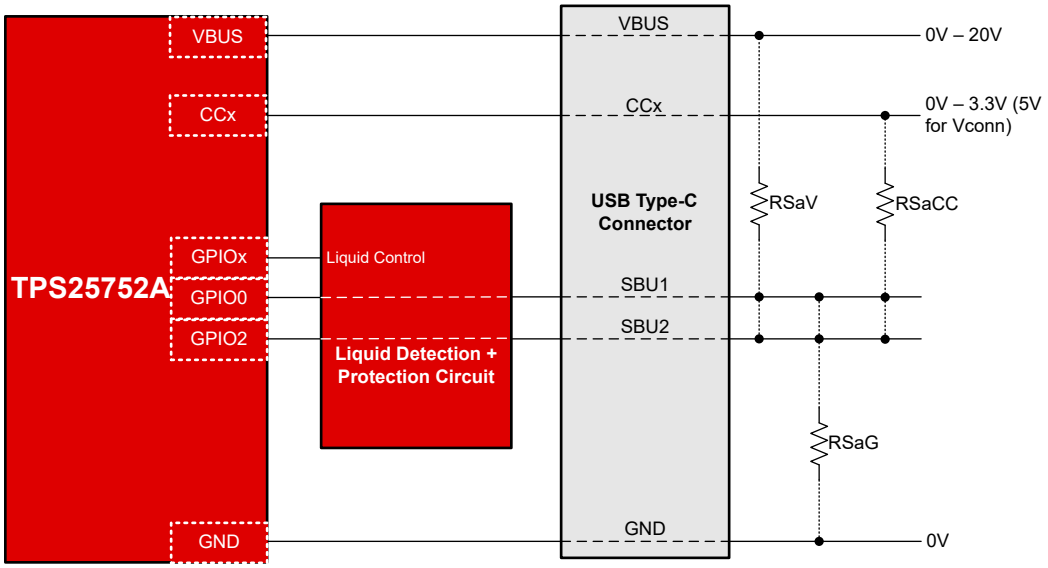


Figure 8-2. Liquid Detection Cases

8.2.1.2 BC1.2 Application Design Requirements

The PD controller uses the USB D+ and D- pins to provide BC1.2 detection and advertisement. The USB D+ and D- are connected to the USB Host (DFP) or USB Device (UFP) from the Type-C connector for Charging Data Port applications.

8.2.1.3 USB Data Support Design Requirements

For USB3 operation, the SSTX/RX are muxed to the Type-C connector. A SuperSpeed Mux generally has two control signals; enable and plug orientation. The PD controller determines when a connection is detected and drives the required GPIO to control the SuperSpeed Mux.

8.2.2 Detailed Design Procedure

8.2.2.1 Liquid Detection

The TPS25752A supports liquid detection using the built-in internal ADC and GPIO with external circuitry. TPS25752A Liquid Detection Block Diagram - CC1 and CC2 Monitor Pins and TPS25752A Liquid Detection Block Diagram - SBU1 and SBU2 Monitor Pins show the hardware implementation using CC1/2 and SBU1/2 pins for liquid detection with the TPS25752A. The TPD4S201 is used to protect the ADC pins from over voltage conditions when there is liquid shorting VBUS to the monitoring pins. When liquid is detected, the TPS25752A takes action to protect the Type-C port. Systems using an embedded host controller can leverage the Host Interface for additional notification and control.

Table 8-2. Liquid Detection GPIO Pin Function

Pin	Function
GPIO0 and GPIO2	Internal ADC to measure the biased voltage on the monitoring pins.
GPIOx	Output GPIO that controls the biasing voltage that drives the monitoring pins High and Low.

Table 8-2. Liquid Detection GPIO Pin Function (continued)

Pin	Function
GPIOy	Input GPIO that initiates Type-C Error Recovery when a fault is detected by the protection device.

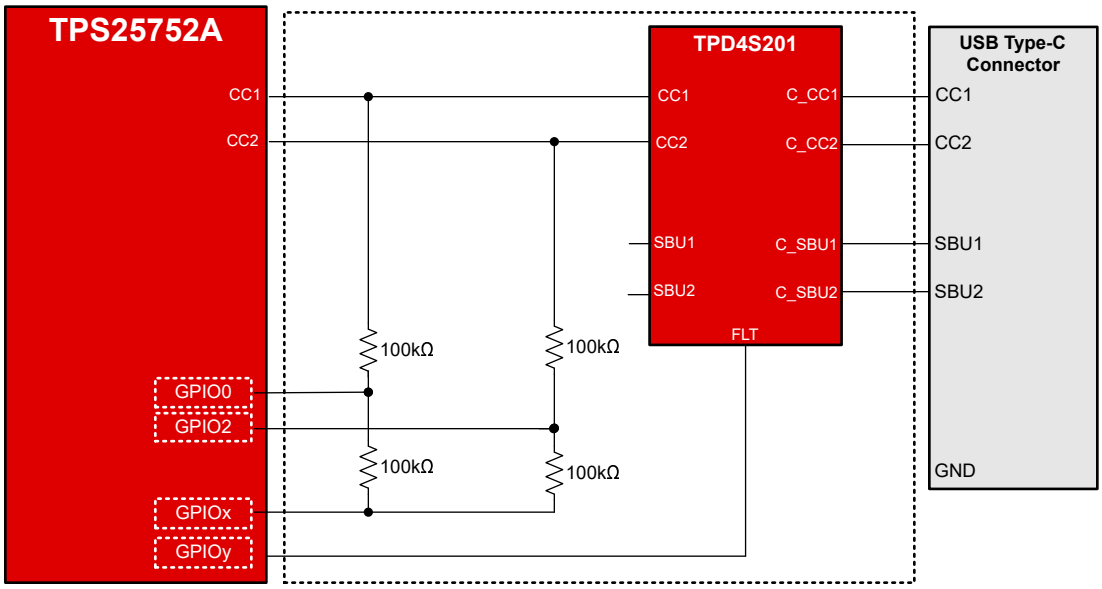


Figure 8-3. TPS25752A Liquid Detection Block Diagram - CC1 and CC2 Monitor Pins

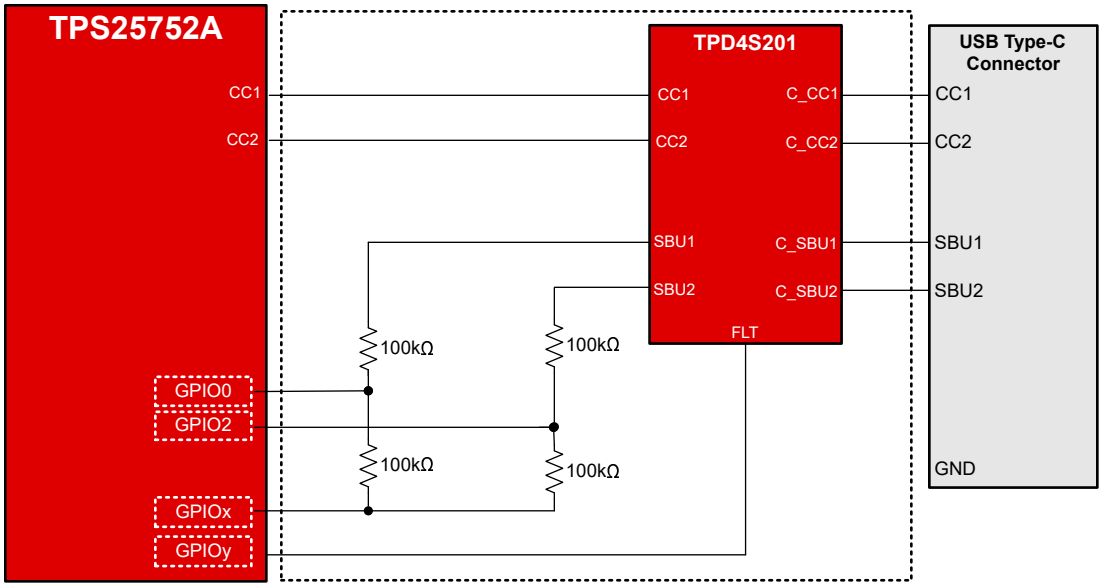


Figure 8-4. TPS25752A Liquid Detection Block Diagram - SBU1 and SBU2 Monitor Pins

8.2.2.2 BC1.2 Application

The TPS25752A supports BC1.2 advertisement modes and are configurable through the Web Tool.

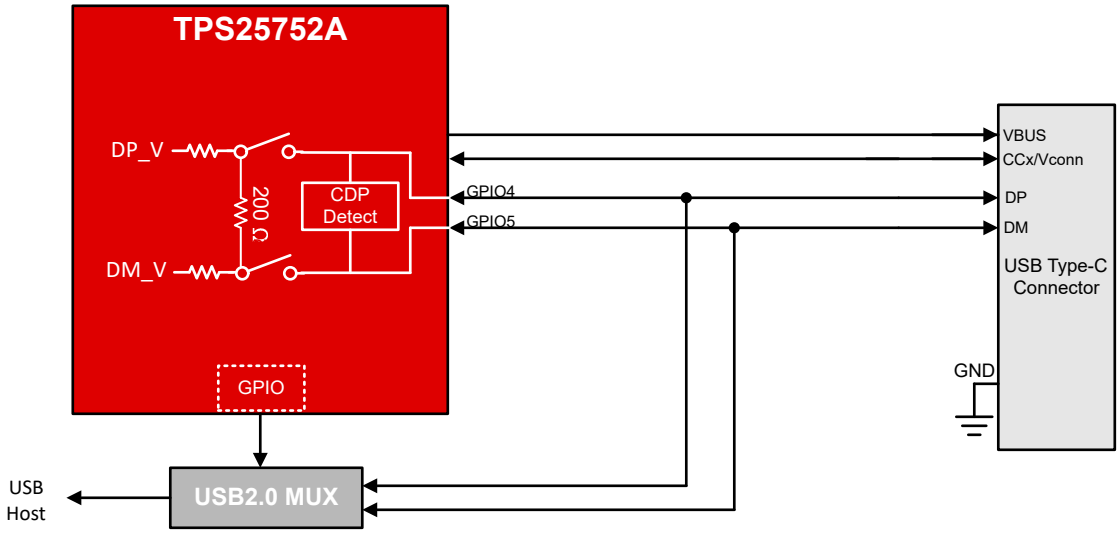


Figure 8-5. BC1.2 Application Block Diagram

8.2.2.3 USB Data Support

The TPS25752A supports USB data speed up to USB 3.2Gen 2. When entering USB enumeration, the TPS25752A controls USB SuperSpeed Mux (TUSB1142) using GPIO controls. The GPIO control is configured through using the Application Customization Tool, GPIO events are found in the Technical Reference Manual.

8.2.3 Application Curves

8.2.3.1 Liquid Detection Application Curves

The figures below show the liquid detection behavior with corrosion mitigation disabled and enabled. Liquid is detected on both Liquid Detection Behavior - No Corrosion Mitigation and Liquid Detection Behavior - Corrosion Mitigation on the SBU2 pin. The number of samples, timing, and hysteresis voltage range of liquid detection is configurable through the Web Tool.

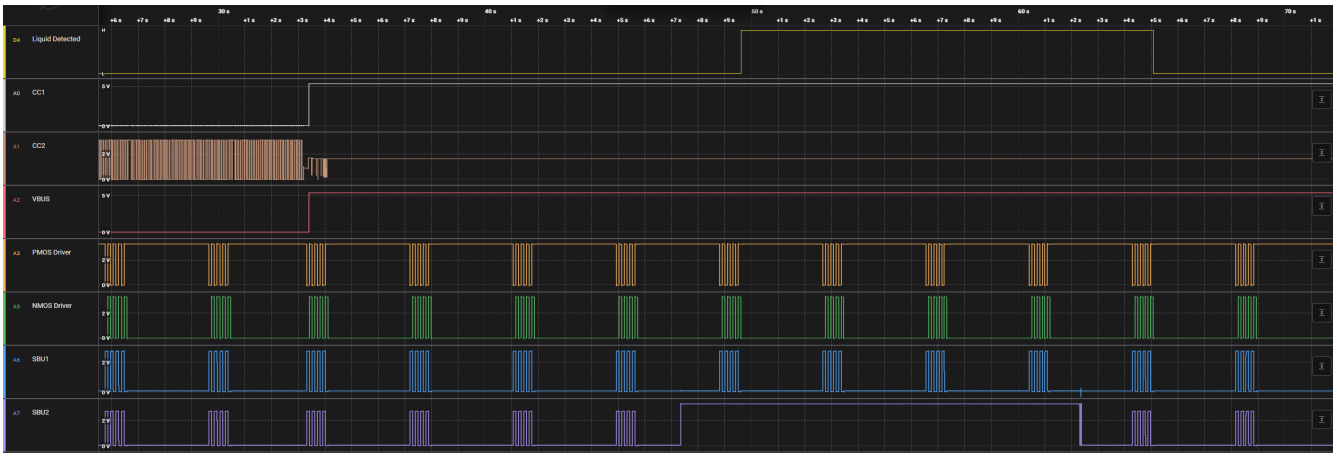


Figure 8-6. Liquid Detection Behavior - No Corrosion Mitigation

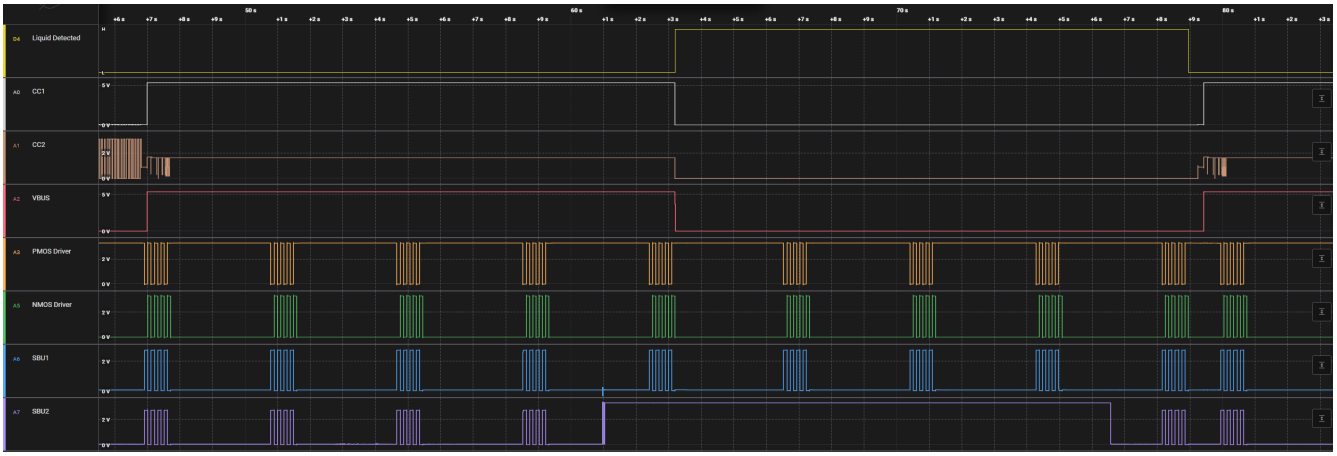


Figure 8-7. Liquid Detection Behavior - Corrosion Mitigation

8.3 Power Supply Recommendations

8.3.1 3.3V Power

8.3.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply of the TPS25752A device. The VIN_3V3 switch (see *Section 7.3.2*) is a uni-directional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when the 3.3V supply is available . The recommended capacitance C_{VIN_3V3} (see *Section 5.4*) must be connected from the VIN_3V3 pin to the GND pin. Do not power VIN_3V3 from VBUS.

8.3.2 1.5V Power

The internal circuitry is powered from 1.5V. The 1.5V LDO steps the voltage down from LDO_3V3 to 1.5V. The 1.5V LDO provides power to all internal low-voltage digital circuits which includes the digital core and memory. The 1.5V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance C_{LDO_1V5} (see *Section 5.4*) from the LDO_1V5 pin to the GND pin.

8.3.3 Recommended Supply Load Capacitance

Section 5.4 lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowed for tolerances and voltage derating ensuring proper operation.

8.4 Layout

8.4.1 Layout Guidelines

Proper routing and placement maintain signal integrity for high speed signals and improve the heat dissipation from the power paths. The combination of power and high speed data signals are easily routed if the following guidelines are followed. Best practice is to consult with board manufacturing to verify manufacturing capabilities.

8.4.1.1 Recommended Via Size

Proper via stitching is recommended to carrying current for the VBUS power paths and grounding. The recommended minimum via size is shown below, but larger vias are an option for low density PCB designs. A single via is capable of carrying 1A, verify the tolerance with the board manufacturing. Vias are recommended to be tented when located close to the PD controller.

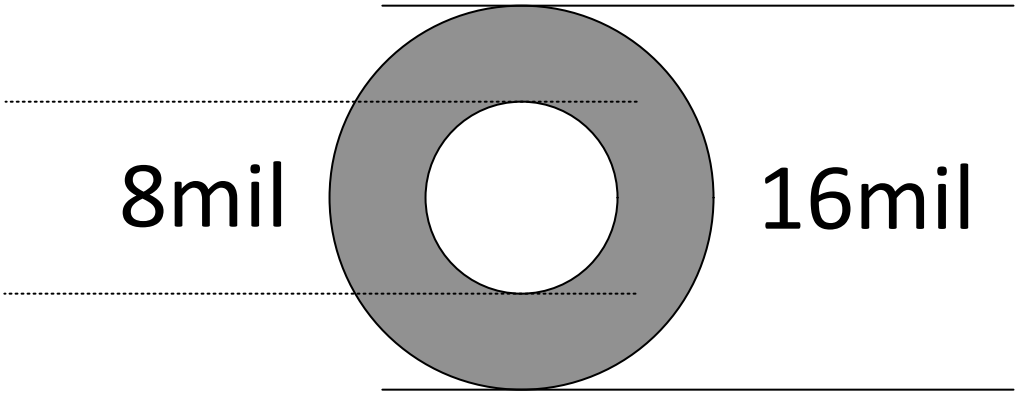


Figure 8-8. Recommend Minimum Via Size

8.4.1.2 Minimum Trace Widths

Below are the minimum trace widths for analog and digital pins. The trace width limitations are also defined by the board manufacturing process used. Consult with manufacturing for determining the minimum trace widths and tolerance.

Table 8-3. Minimum Trace Width

Route	Minimum Width (mils)
CC1, CC2	10
VIN_3V3, LDO	10
Component GND	16
GPIO	4

8.4.2 Layout Example

8.4.2.1 Schematic

Follow the differential impedances for Super / High Speed signals defined by their specifications (USB2.0). All I/O are fanned out to provide an example for routing out all pins, not all designs utilize all of the I/O on the TPS25752A.

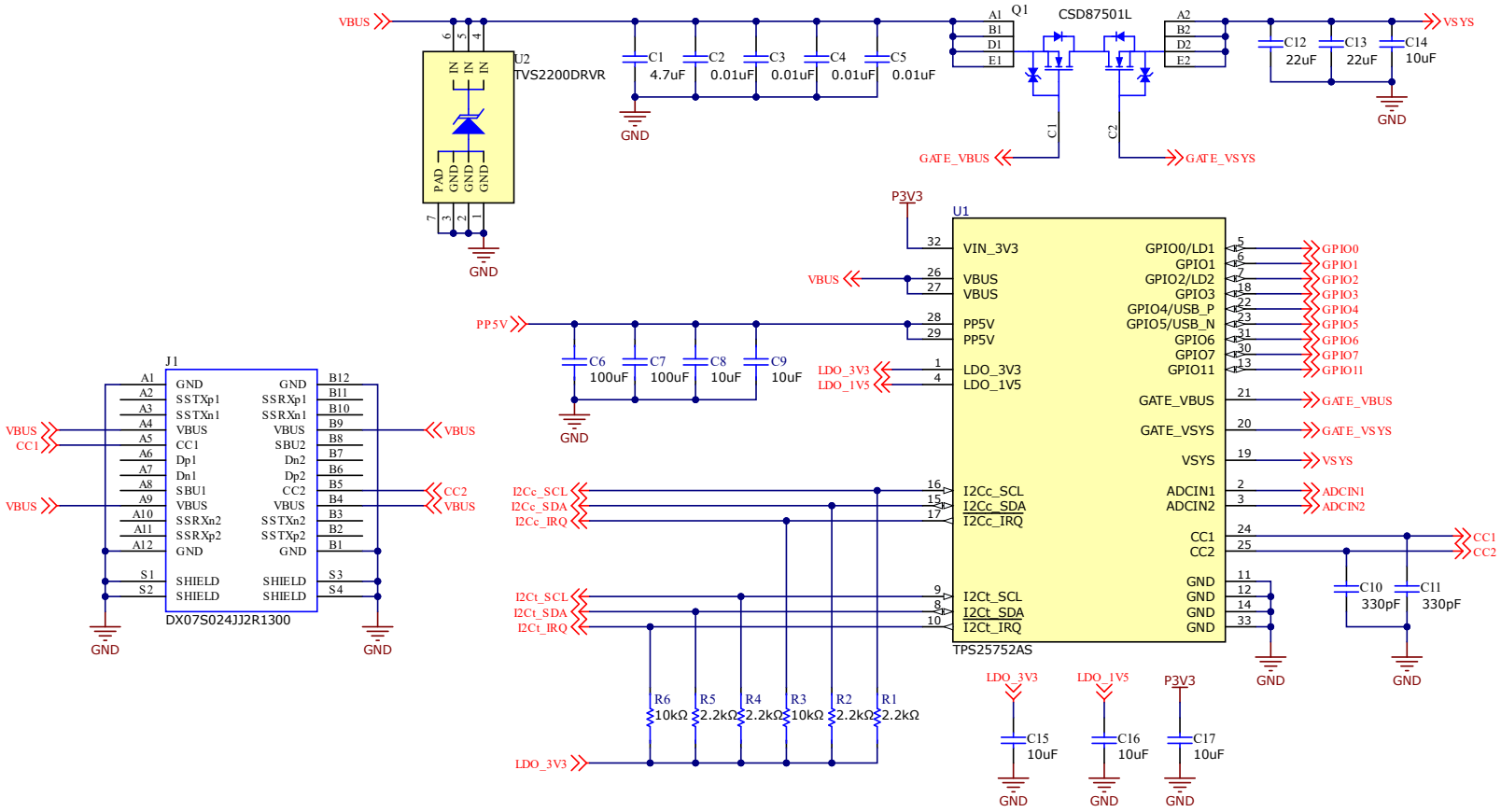


Figure 8-9. Example Schematic

8.4.2.2 PCB Plots

The following TPS25752A PCB Layout figures show the recommended layout, placement, and routing.

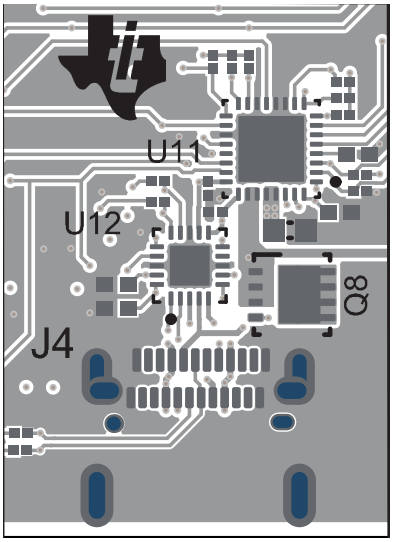


Figure 8-10. PCB Layout - Top Composite

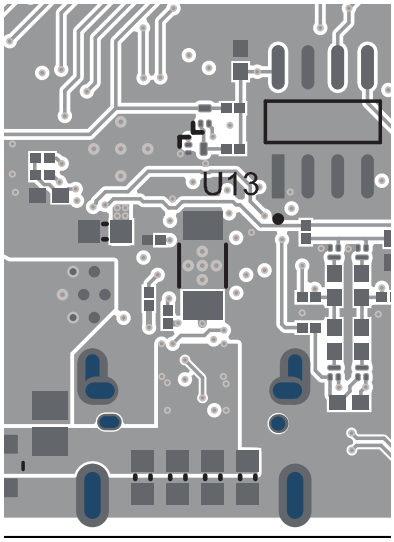


Figure 8-11. PCB Layout - Bottom Composite

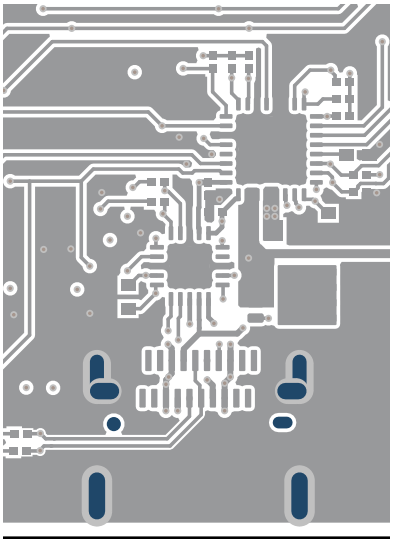


Figure 8-12. PCB Layout - Top Layer 1

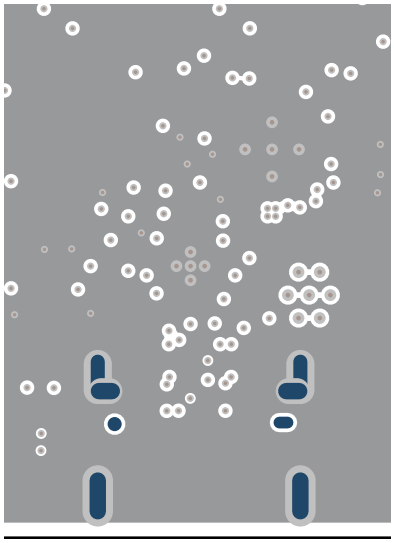


Figure 8-13. PCB Layout - GND Layer 2

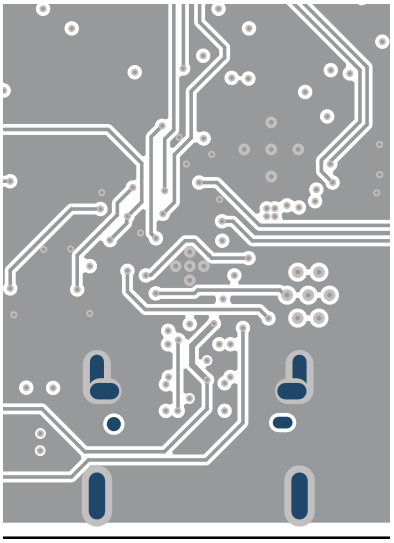


Figure 8-14. PCB Layout - Signal Layer 3

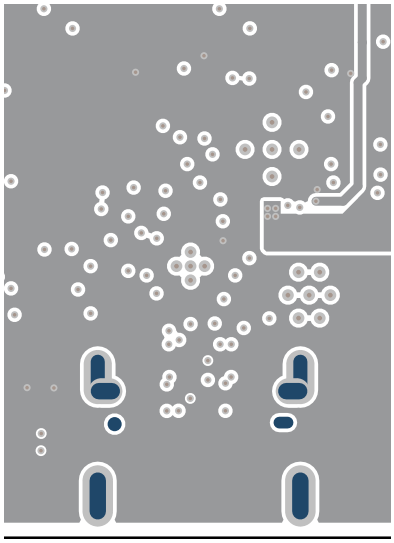


Figure 8-15. PCB Layout - Signal Layer 4

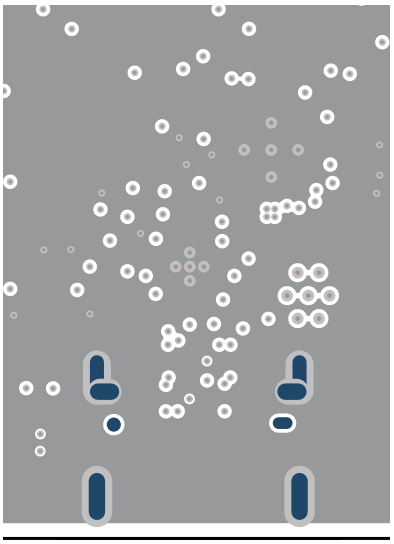


Figure 8-16. PCB Layout - GND Layer 5

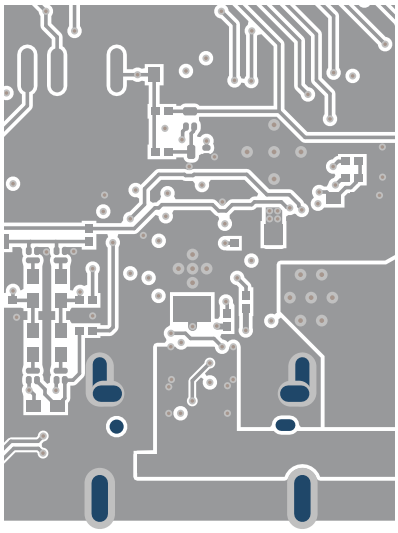


Figure 8-17. PCB Layout - Bottom Layer 6

8.4.2.2.1 Component Placement

LDO_1V5 (pin 4), LDO_3V3 (pin 1), and VIN_3V3 (pin 32)

The decoupling capacitors for LDO_3V3, LDO_1V5, and VIN_3V3 (C15, C16, and C17 respectively) need to be placed as close as possible to TPS25752A device for optimal performance. For this example to minimize solution size, the decoupling capacitors are placed on the bottom layer with their ground pads directly underneath the ground pad of TPS25752A. Use a maximum of one via per pin from TPS25752A to the decoupling capacitors if placed on a different layer. Use a minimum of 10mil trace width to route these three traces, preferably with 16mil trace width if possible.

CC1 (pin 24) and CC2 (pin 25)

CC1 (C11) and CC2 (C10) capacitors need to be placed as close as possible to their respective pins and on the same layer as the TPS25752A device. When routing the CCx traces, DO NOT via to another layer in between the CCx pins of the TPS25752A to the CCx capacitors. Check to make sure the CCx capacitors are not place outside the CC trace creating an antenna, instead have the traces pass directly through the CCx capacitor pads as shown in the example layout. Use a minimum of 10mil trace width for Vconn support (5V/0.6A).

8.4.2.2.2 PP5V

The 10uF decoupling capacitor (C8) need to be placed as close as possible to the PP5V pins of TPS25752A. DO NOT use traces for PP5V. The PP5V power plane needs to be sized to support up to 3.6A (up to 3A for sourcing, 600mA for Vconn). When connecting the PP5V pins (pins 28 and 29) to the 5V power plane, use a minimum of 4 vias in parallel and close to the device to improve current sharing. Minimize the bottle necks caused by other vias or traces, large bottle necks reduce the efficiency of the power plane. The bulk capacitors (C6, C7, and C9) represent capacitances from the system 5V rail, these are placed further away from TPS25752A on the same PP5V power plane.

8.4.2.2.3 PP_EXT

Place the PP_EXT decoupling capacitors as close as possible to TPS25752A, these do not need to be on the same layer as the device. The PP_EXT power plane needs to be sized to support up to 5A of current. When connecting the PP_EXT plane to a different layer, use a minimum of 6 vias in parallel per layer change. Place more than 6 vias if possible for layer change to improve current sharing and efficiency.

8.4.2.2.4 VBUS

VBUS (pins 26 and 27)

Place the VBUS decoupling capacitor (C37) as close as possible to the VBUS pin of the external NMOS transistor (Q8), the capacitor does not need to be on the same layer as the device. The VBUS power plane need to be sized to support up to 3A of current if the 5V power path is utilized. If this 5V power path is not utilized, then the power path can be sized to support 100mA of current. When connecting the VBUS pins (pins 26 and 27) plane to a different layer, use a minimum of 3 vias per layer change.

At the Type-C port/connector, keep a minimum of 6 vias from the connector VBUS pins for layer changes. Place the 10nF caps as close as possible to the connector VBUS pins.

When implemented with the TPD4S480, the TPS25752A does not require an external TVS protection device. Refer to the data sheet of the switch selected to make sure that any protection requirements are met and if the power switch used in the system requires the addition of a TVS protection diode.

The VBUS line of the type C connector needs to be routed to the external power path in a manner that supports current and voltage needs. Please refer to the datasheet of the switch selected to make sure that any routing and current requirements are met.

8.4.2.2.5 I/O

I2C, ADCIN1/2, and GPIO pins

Fan these traces out from the TPS25752A, use vias to connect the net to a routing layer if needed. For these nets, use 4mil to 10mil trace width.

I2Cc_SDA/SCL/IRQ (pins 8, 9, and 10) and I2Ct_SCL/SDA/IRQ (pins 15, 16, and 17)

Minimize trace width changes to avoid I2C communication issues.

ADCIN1 and ADCIN2 (pins 2 and 3)

Keep the ADCINx traces away from switching elements. If a resistor divider is used, place the divider close to LDO_3V3 or LDO_1V5.

GPIO (pins 5, 6, 7, 18, 22, 23, 31, 30, and 13)

Separate GPIO traces running in parallel by a trace width. Keep the GPIOx traces away from switching elements.

8.4.2.2.6 PPEXT Gate Driver

GATE_VSYS (pin 20)

The GATE_VSYS pin (pin 20) can be connected with a trace (recommended 6mil trace width) to the gate pins of the N-ch MOSFET with source tied to PPHV. It is recommended to **NOT** via directly to the gate pin of the N-ch MOSFET, instead use via(s) to connect the GATE_VSYS pin from the TPS25752AS to the gate pin of the N-ch MOSFET. Refer to figure 10-21 and figure 10-22 for examples on how to connect the traces.

GATE_VBUS (pin 21)

The GATE_VBUS pin (pin 21) can be connected with a trace (recommended 6mil trace width) to the gate pins of the N-ch MOSFET with source tied to VBUS. It is recommended to **NOT** via directly to the gate pin of the N-ch MOSFET, instead use via(s) to connect the GATE_VBUS pin from the TPS25752AS to the gate pin of the N-ch MOSFET. Refer to figure 10-21 and figure 10-22 for examples on how to connect the traces.

8.4.2.2.7 GND

The GND pad is used to dissipate heat for the TPS25752A device. Connect the GND pins (11, 12, 14 and 31) to the Ground pad (39) underneath the TPS25752A device. Connect the through hole vias from the ground pad on the top layer to a copper pour on the bottom layer to help dissipate heat. Additional vias can be added to improve thermal dissipation.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.2 Documentation Support

9.2.1 Related Documentation

- *USB-PD Specifications*
- *USB Power Delivery Specification*

9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25752ASRSMR	Active	Production	VQFN (RSM) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25752A S

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

GENERIC PACKAGE VIEW

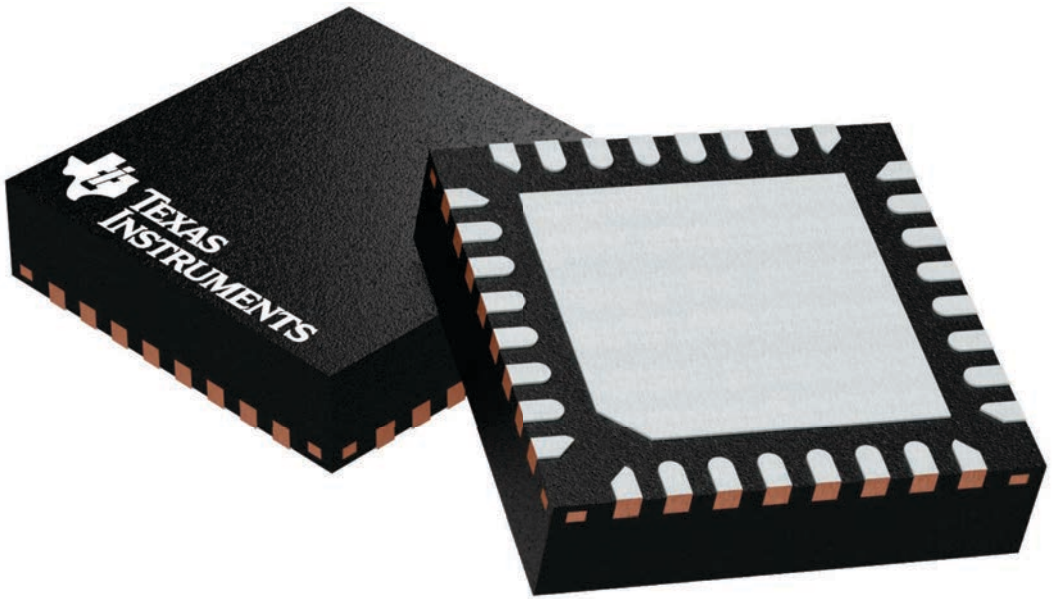
RSM 32

VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



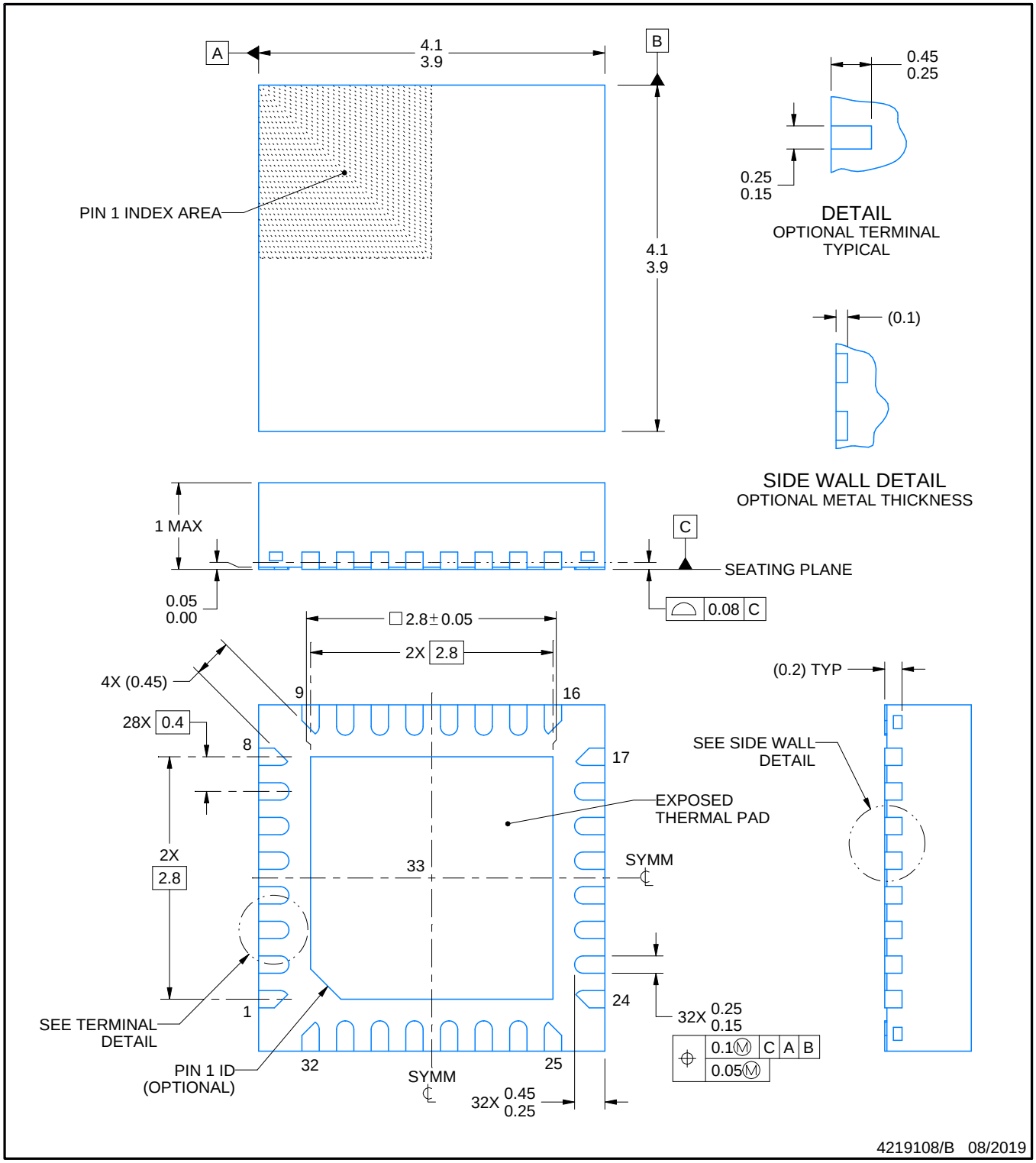
4224982/A

PACKAGE OUTLINE

RSM0032B

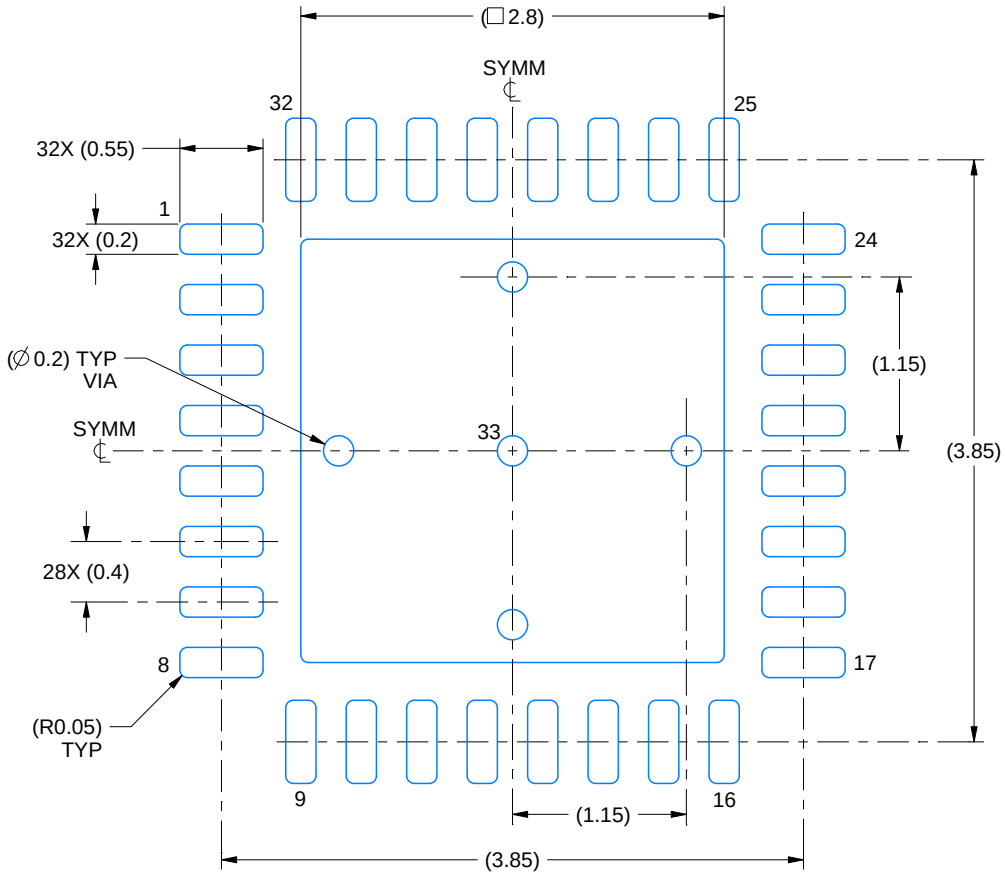
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

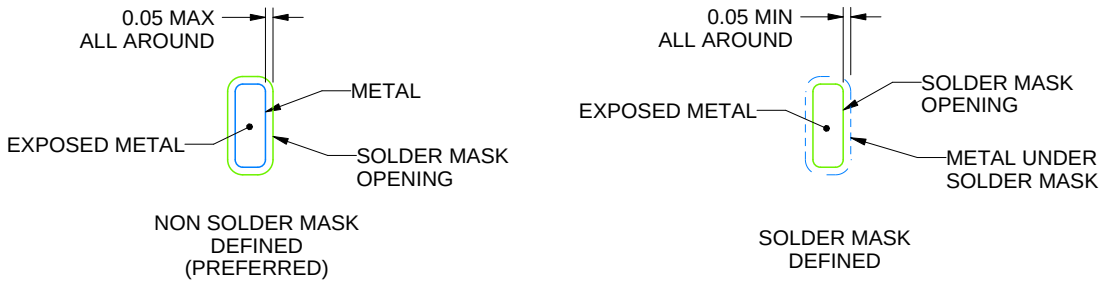


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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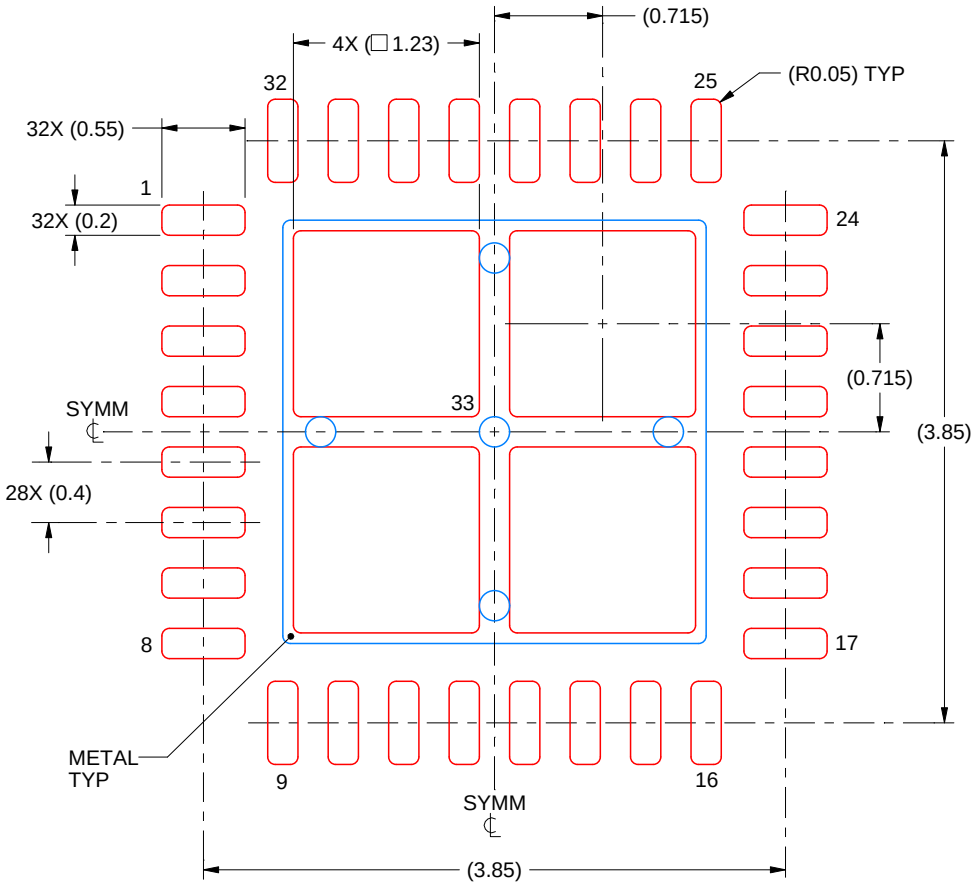
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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