

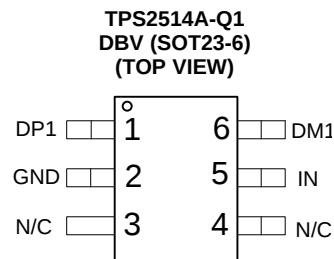
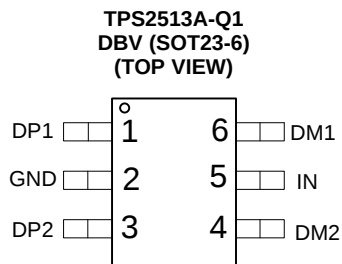
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5 修订历史记录

Changes from Original (May 2014) to Revision A	Page
• 已将 TPA2514A-Q1 器件添加至数据表	1
• 已将特性从：双路 USB 端口控制器更改为：双路 USB 充电端口控制器，TPS2513A-Q1	1
• 已添加特性“单路 USB 充电端口控制器，TPS2514A-Q1”	1
• 已将“说明”部分的文本从：“利用 TPS2561A-Q1 可提供一套低损耗、..”更改为：“搭配使用 TPS2561A-Q1 与 TPS2513A-Q1（双通道）、TPS2557-Q1 与 TPS2514A-Q1（单通道）可提供一套低损耗、..”	1
• 已更改器件信息表	1
• Added the TPS2514A-Q1 pin out image and table	3
• Changed the Handling Ratings table to the ESD Ratings table	4
• Added Figure 5	8
• Changed list item in Layout Guidelines "When USB power switch is used,..”	14
• Changed list item in Layout Guidelines "Regarding TPS2561A-Q1 layout guidelines,..”	14

6 Pin Configuration and Functions



Pin Functions, TPS2513A-Q1

NO.	NAME	TYPE ⁽¹⁾	DESCRIPTION
1	DP1	I/O	Connected to the D+ line of USB connector, provide the correct voltage with attached portable equipment for DCP detection.
2	GND	G	Ground connection
3	DP2	I/O	Connected to the D+ line of USB connector, provide the correct voltage with attached portable equipment for DCP detection.
4	DM2	I/O	Connected to the D– line of USB connector, provide the correct voltage with attached portable equipment for DCP detection.
5	IN	P	Power supply. Connect a ceramic capacitor with a value of 0.1-μF or greater from the IN pin to GND as close to the device as possible.
6	DM1	I/O	Connected to the D– line of USB connector, provide the correct voltage with attached portable equipment for DCP detection.

(1) G = Ground, I = Input, O = Output, P = Power

Pin Functions, TPS2514A-Q1

NO.	NAME	TYPE ⁽¹⁾	DESCRIPTION
1	DP1	I/O	Connected to the D+ line of USB connector, provide the correct voltage with attached portable equipment for DCP detection.
2	GND	G	Ground connection
3	N/C	–	No connect pin, can be grounded or left floating.
4	N/C	–	No connect pin, can be grounded or left floating
5	IN	P	Power supply. Connect a ceramic capacitor with a value of 0.1-μF or greater from the IN pin to GND as close to the device as possible.
6	DM1	I/O	Connected to the D– line of USB connector, provide the correct voltage with attached portable equipment for DCP detection.

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

Over recommended junction temperature range, voltages are referenced to GND (unless otherwise noted)

		MIN	MAX	UNIT
Voltage range	IN	−0.3	7	V
	DP1, DP2 output voltage, DM1, DM2 output voltage	−0.3	5.8	
	DP1, DP2 input voltage, DM1, DM2 input voltage	−0.3	5.8	
Continuous output sink current	DP1, DP2 input current, DM1, DM2 input current		35	mA
Continuous output source current	DP1, DP2 output current, DM1, DM2 output current		35	mA
Operating Junction Temperature, T_J		−40	125	°C
Storage temperature range, T_{stg}		−65	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Voltages are referenced to GND (unless otherwise noted), positive current are into pins.

		MIN	MAX	UNIT
V_{IN}	Input voltage of IN	4.5	5.5	V
$V_{(DP1)}$	DP1 data line input voltage	0	5.5	V
$V_{(DM1)}$	DM1 data line input voltage	0	5.5	V
$I_{(DP1)}$	Continuous sink or source current		±10	mA
$I_{(DM1)}$	Continuous sink or source current		±10	mA
V_{DP2}	DP2 data line input voltage	0	5.5	V
$V_{(DM2)}$	DM2 data line input voltage	0	5.5	V
$I_{(DP2)}$	Continuous sink or source current		±10	mA
$I_{(DM2)}$	Continuous sink or source current		±10	mA
T_J	Operating junction temperature	−40	125	°C

7.4 Thermal Information

	THERMAL METRIC ⁽¹⁾	DBV (6 PINS)	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	179.9	°C/W
$R_{\theta Jctop}$	Junction-to-case (top) thermal resistance	117.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	41.9	
Ψ_{JT}	Junction-to-top characterization parameter	17.2	
Ψ_{JB}	Junction-to-board characterization parameter	41.5	
$R_{\theta Jcbot}$	Junction-to-case (bottom) thermal resistance	N/A	

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

7.5 Electrical Characteristics

Conditions are $-40^{\circ}\text{C} \leq (T_J = T_A) \leq 125^{\circ}\text{C}$, $4.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$. Positive current are into pins. Typical values are at 25°C . All voltages are with respect to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
UNDERVOLTAGE LOCKOUT						
V_{UVLO}	IN rising UVLO threshold voltage		3.9	4.1	4.3	V
	Hysteresis ⁽¹⁾			100		mV
SUPPLY CURRENT						
I_{IN}	IN supply current	$4.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		155	220	μA
BC 1.2 DCP MODE (SHORT MODE)						
$R_{(DPM_SHORT1)}$	DP1 and DM1 shorting resistance	$V_{DP1} = 0.8\text{ V}$, $I_{DM1} = 1\text{ mA}$		157	200	Ω
$R_{(DCHG_SHORT1)}$	Resistance between DP1/DM1 and GND	$V_{DP1} = 0.8\text{ V}$	350	656	1150	k Ω
$V_{(DPL_TH_DETACH1)}$	Voltage threshold on DP1 under which the device goes back to divider mode		310	330	350	mV
$V_{(DPL_TH_DETACH_HYS1)}$	Hysteresis ⁽¹⁾			50		mV
$R_{(DPM_SHORT2)}$	DP2 and DM2 shorting resistance	$V_{DP2} = 0.8\text{ V}$, $I_{DM2} = 1\text{ mA}$		157	200	Ω
$R_{(DCHG_SHORT2)}$	Resistance between DP2/DM2 and GND	$V_{DP2} = 0.8\text{ V}$	350	656	1150	k Ω
$V_{(DPL_TH_DETACH2)}$	Voltage threshold on DP2 under which the device goes back to divider mode		310	330	350	mV
$V_{(DPL_TH_DETACH_HYS2)}$	Hysteresis ⁽¹⁾			50		mV
DIVIDER MODE						
$V_{(DP1_2.7V)}$	DP1 output voltage	$V_{IN} = 5\text{ V}$	2.57	2.7	2.84	V
$V_{(DM1_2.7V)}$	DM1 output voltage	$V_{IN} = 5\text{ V}$	2.57	2.7	2.84	V
$R_{(DP1_PAD1)}$	DP1 output impedance	$I_{DP1} = -5\text{ }\mu\text{A}$	24	30	36	k Ω
$R_{(DM1_PAD1)}$	DM1 output impedance	$I_{DM1} = -5\text{ }\mu\text{A}$	24	30	36	k Ω
$V_{(DP2_2.7V)}$	DP2 output voltage	$V_{IN} = 5\text{ V}$	2.57	2.7	2.84	V
$V_{(DM2_2.7V)}$	DM2 output voltage	$V_{IN} = 5\text{ V}$	2.57	2.7	2.84	V
$R_{(DP2_PAD1)}$	DP2 output impedance	$I_{DP2} = -5\text{ }\mu\text{A}$	24	30	36	k Ω
$R_{(DM2_PAD1)}$	DM2 output impedance	$I_{DM2} = -5\text{ }\mu\text{A}$	24	30	36	k Ω
1.2 V / 1.2 V MODE						
$V_{(DP1_1.2V)}$	DP1 output voltage	$V_{IN} = 5\text{ V}$	1.12	1.2	1.28	V
$V_{(DM1_1.2V)}$	DM1 output voltage	$V_{IN} = 5\text{ V}$	1.12	1.2	1.28	V
$R_{(DM1_PAD2)}$	DP1 output impedance	$I_{DP1} = -5\text{ }\mu\text{A}$	80	102	130	k Ω
$R_{(DP1_PAD2)}$	DM1 output impedance	$I_{DM1} = -5\text{ }\mu\text{A}$	80	102	130	k Ω
$V_{(DP2_1.2V)}$	DP2 output voltage	$V_{IN} = 5\text{ V}$	1.12	1.2	1.28	V
$V_{(DM2_1.2V)}$	DM2 output voltage	$V_{IN} = 5\text{ V}$	1.12	1.2	1.28	V
$R_{(DP2_PAD2)}$	DP2 output impedance	$I_{DP2} = -5\text{ }\mu\text{A}$	80	102	130	k Ω
$R_{(DM2_PAD2)}$	DM2 output impedance	$I_{DM2} = -5\text{ }\mu\text{A}$	80	102	130	k Ω

(1) Parameters provided for reference only, and do not constitute part of TI's published device specifications for purposes of TI's product warranty

7.6 Typical Characteristics

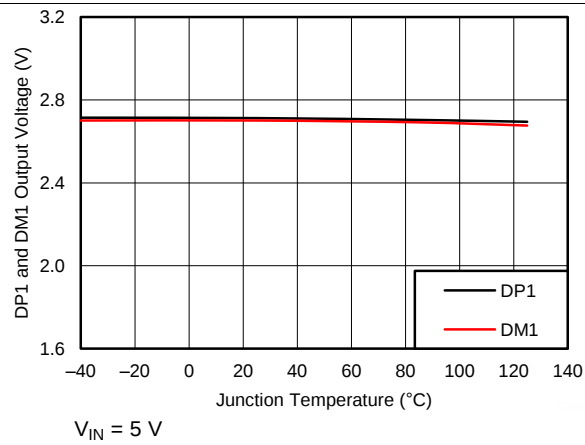


Figure 1. DP1 and DM1 Output Voltage vs Temperature

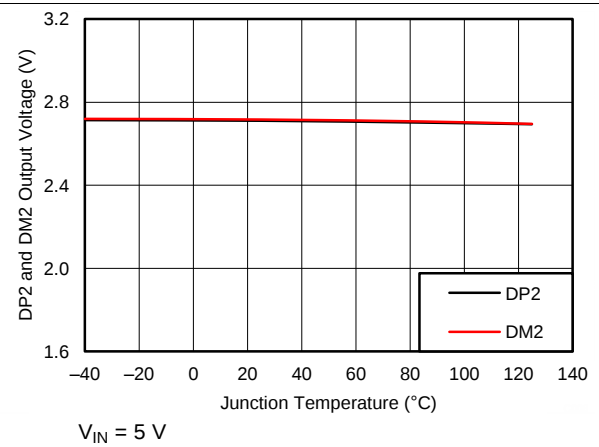


Figure 2. DP2 and DM2 Output Voltage vs Temperature

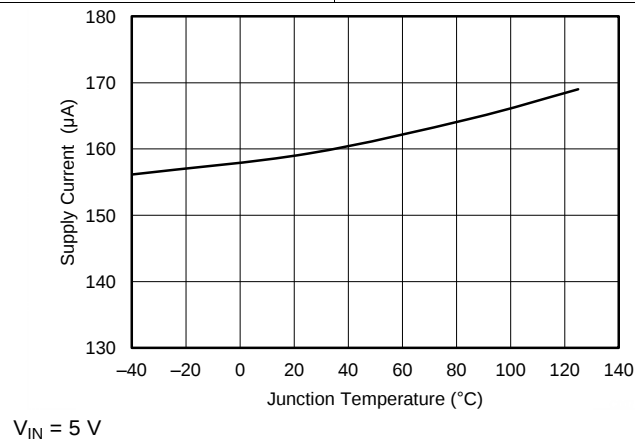


Figure 3. Supply Current vs Temperature

8 Detailed Description

8.1 Overview

TPS2513A-Q1 and TPS2514A-Q1 are dedicated charging port controllers, used for the charging of most popular mobile phones and tablets.

The following overview references various industry standards. It is always recommended to consult the latest standard to ensure the most recent and accurate information.

Rechargeable portable equipment requires an external power source to charge its batteries. USB ports are convenient locations for charging because of an available 5-V power source. Universally accepted standards are required to ensure host and client-side devices meet the power management requirements. Traditionally, USB host ports following the USB 2.0 Specification must provide at least 500 mA to downstream client-side devices. Because multiple USB devices can be attached to a single USB port through a bus-powered hub, it is the responsibility of the client-side device to negotiate the power allotment from the host to guarantee the total current draw does not exceed 500 mA. In general, each USB device can subsequently request more current, which is granted in steps of 100 mA up 500 mA total. The host may grant or deny the request based on the available current.

Additionally, the success of the USB technology makes the micro-USB connector a popular choice for wall adapter cables. This allows a portable device to charge from both a wall adapter and USB port with only one connector.

One common difficulty has resulted from this. As USB charging has gained popularity, the 500-mA minimum defined by the USB 2.0 Specification or 900 mA defined in the USB 3.0 Specification, has become insufficient for many handsets, tablets and personal media players (PMP) which have a higher rated charging current. Wall adapters and car chargers can provide much more current than 500 mA or 900 mA to fast charge portable devices. Several new standards have been introduced defining protocol handshaking methods that allow host and client devices to acknowledge and draw additional current beyond the 500 mA (defined in the USB 2.0 Specification) or 900 mA (defined in the USB 3.0 Specification) minimum while using a single micro-USB input connector.

TPS2513A-Q1, TPS2514A-Q1

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8.2 Functional Block Diagram

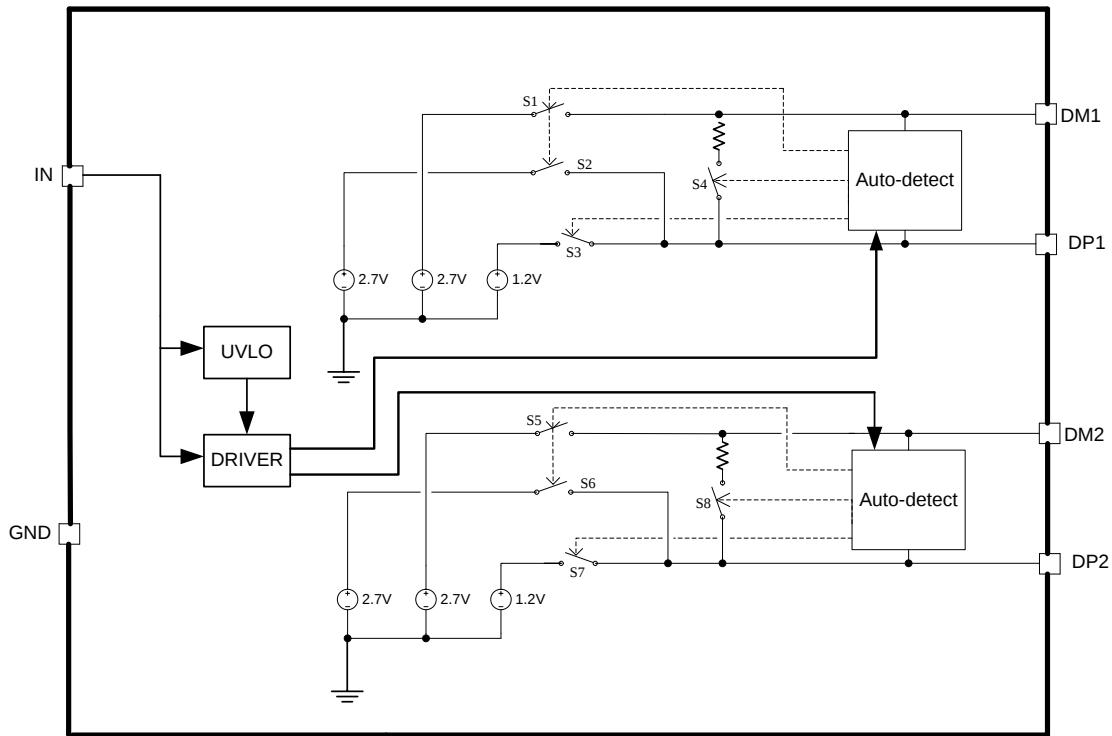


Figure 4. TPS2513A-Q1 Functional Block Diagram

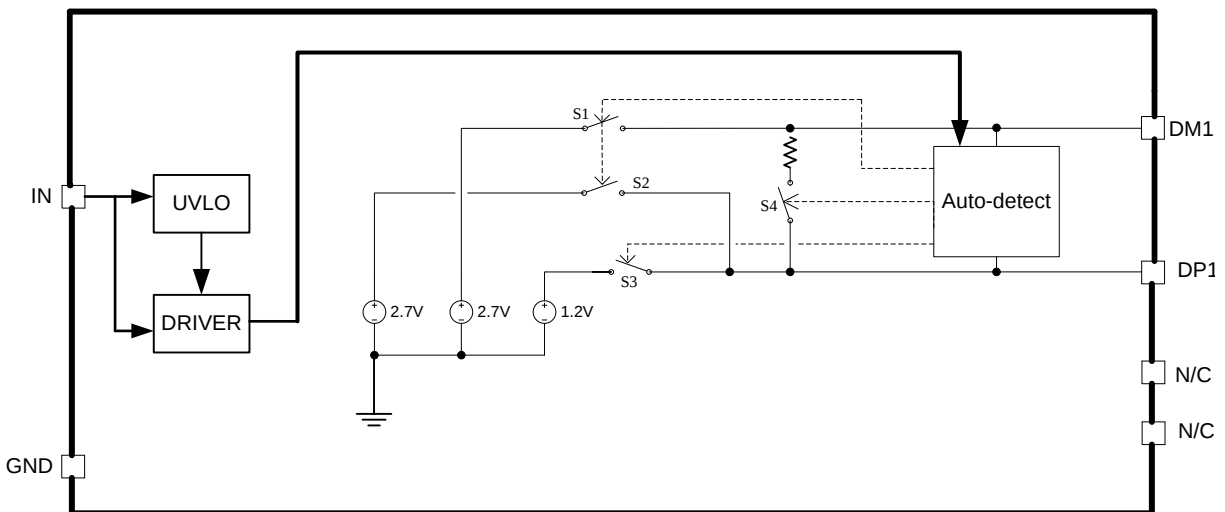


Figure 5. TPS2514A-Q1 Functional Block Diagram

8.3 Feature Description

8.3.1 BC1.2

TPS2513A-Q1 and TPS2514A-Q1 support four of the most common protocols:

- USB Battery Charging Specification, Revision 1.2 (BC1.2)
- Chinese Telecommunications Industry Standard YD/T 1591-2009
- Divider Mode
- 1.2 V Mode

YD/T 1591-2009 is a subset of the BC1.2 specification supported by the vast majority of devices that implement USB charging. Divider and 1.2-V charging schemes are supported in devices from specific yet popular device makers. BC1.2 has three different port types, listed as follows.

- Standard downstream port (SDP)
- Charging downstream port (CDP)
- Dedicated charging port (DCP)

The BC1.2 Specification defines a charging port as a downstream facing USB port that provides power for charging portable equipment.

Table 1 shows different port operating modes according to the BC1.2 Specification.

Table 1. Operating Modes Table

PORT TYPE	SUPPORTS USB2.0 COMMUNICATION	MAXIMUM ALLOWABLE CURRENT DRAWN BY PORTABLE EQUIPMENT (A)
SDP (USB 2.0)	Yes	0.5
SDP (USB 3.0)	Yes	0.9
CDP	Yes	1.5
DCP	No	1.5

The BC1.2 Specification defines the protocol necessary to allow portable equipment to determine what type of port it is connected to so that it can allot its maximum allowable current drawn. The hand-shaking process is two steps. During step one, the primary detection, the portable equipment outputs a nominal 0.6 V output on its D+ line and reads the voltage input on its D– line. The portable device concludes it is connected to a SDP if the voltage is less than the nominal data detect voltage of 0.3 V. The portable device concludes that it is connected to a Charging Port if the D– voltage is greater than the nominal data detect voltage of 0.3V and less than 0.8 V. The second step, the secondary detection, is necessary for portable equipment to determine between a CDP and a DCP. The portable device outputs a nominal 0.6 V output on its D– line and reads the voltage input on its D+ line. The portable device concludes it is connected to a CDP if the data line being remains is less than the nominal data detect voltage of 0.3 V. The portable device concludes it is connected to a DCP if the data line being read is greater than the nominal data detect voltage of 0.3 V and less than 0.8 V.

8.3.2 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) circuit disables DP1, DM1, DP2 and DM2 output voltage until the input voltage reaches the UVLO turn-on threshold. Built-in hysteresis prevents unwanted oscillations due to input voltage drop from large current surges.

8.3.3 DCP Auto-Detect

TPS2513A-Q1 and TPS2514A-Q1 integrate an auto-detect feature to support Divider 3 mode, shorted mode and 1.2 V modes. If a divider device is attached, 2.7 V is applied to the DP pin and 2.7 V is applied to the DM pin. If a BC1.2-compliant device is attached, the TPS251xA-Q1 automatically switches into shorted mode. If a device compliant with the 1.2 V / 1.2 V charging scheme is attached, 1.2 V is applied on both the DP pin and the DM pin. The functional diagram of DCP auto-detect feature (DM1 and DP1) is shown in Figure 6. DCP auto-detect feature (DM2 and DP2) has the same functional configuration.

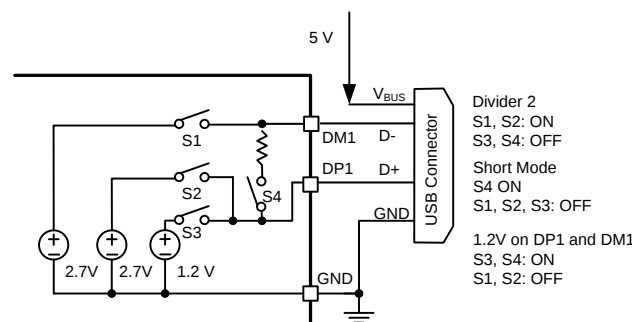


Figure 6. DCP Auto-Detect Functional Diagram

8.4 Device Functional Modes

8.4.1 Shorted Mode

The USB BC1.2 Specification and the Chinese Telecommunications Industry Standard YD/T 1591-2009 specify that the D+ and D– data lines should be shorted together with a maximum series impedance of 200 Ω . This is shown in Figure 7.

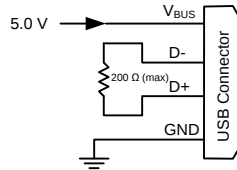


Figure 7. Shorted Mode

8.4.2 Divider Mode

There are three charging schemes for divider mode. They are named after Divider 1, Divider 2, and Divider 3 that are shown in Figure 8, Figure 9, and Figure 10. The Divider 1 charging scheme is used for 5-W adapters, and applies 2 V to the D+ line and 2.7 V to the D– data line. The Divider 2 charging scheme is used for 10-W adapters, and applies 2.7 V on the D+ line and 2 V is applied on the D– line. The Divider 3 charging scheme is used for 12-W adapters, and applies 2.7 V on D+ and D– lines. TPS2513A-Q1 and TPS2514A-Q1 only integrate Divider 3 charging scheme.

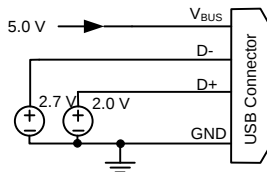


Figure 8. Divider 1

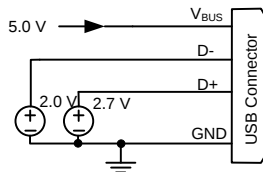


Figure 9. Divider 2

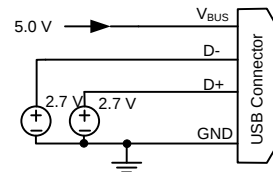


Figure 10. Divider 3

8.4.3 1.2 V Mode

As shown in Figure 11, some tablet USB chargers require 1.2 V on the shorted data lines of the USB connector. The maximum resistance between the D+ line and the D– line is 200 Ω .

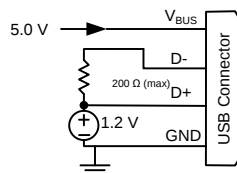


Figure 11. 1.2 V Mode

The device is a USB dedicated charging port (DCP) controllers. Applications include vehicle power charger, wall adapters with USB DCP and other USB chargers. The device DCP controllers have the auto-detect feature that monitors the D+ and D– line voltages of the USB connector, providing the correct electrical signatures on the DP and DM pins for the correct detections of compliant portable devices to fast charge. These portable devices include smart phones, 5-V tablets and personal media players.

9 Applications and Implementation

9.1 Application Information

The device is a dual channel USB charging port controller. It can be used for automotive USB charging port to support universal charging.

9.2 Typical Application

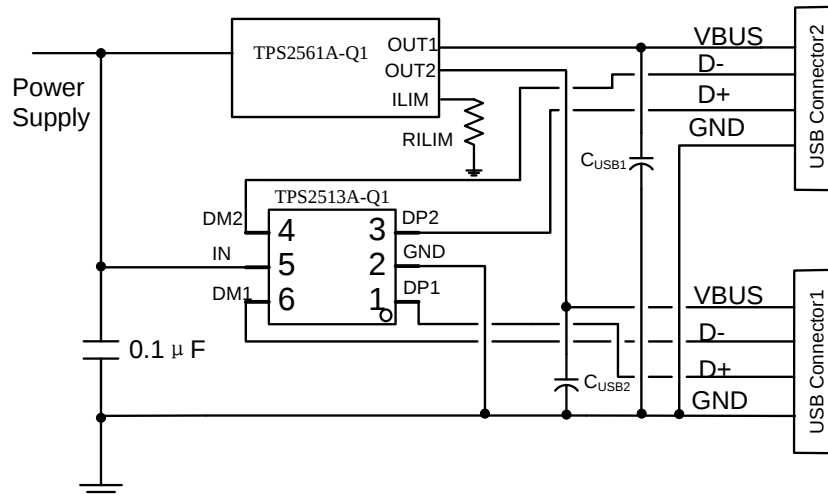


Figure 12. Typical Application Schematic, Dual Ports Charger

9.2.1 Design Requirements

For dual USB ports, request that both ports support fast charge portable device compatible with divider 3, 1.2 V, and BC1.2 shorted mode.

9.2.2 Detailed Design Procedure

9.2.2.1 USB Power Switch

Some chargers requests that the USB port have an overcurrent protection when short circuits are encountered, TPS2561A-Q1 ([SLVSCC6](#)) is recommended.

The TPS2513A-Q1 divider 3 mode can support a maximum charging current up to 2.4 A.

When set, the TPS2561A-Q1 current limit (R_{ILIM}) should keep each channel current limit above 2.4 A. For the correct current limit setting, refer to the TPS2561A-Q1 data sheet.

Typical Application (continued)

9.2.3 Application Curves

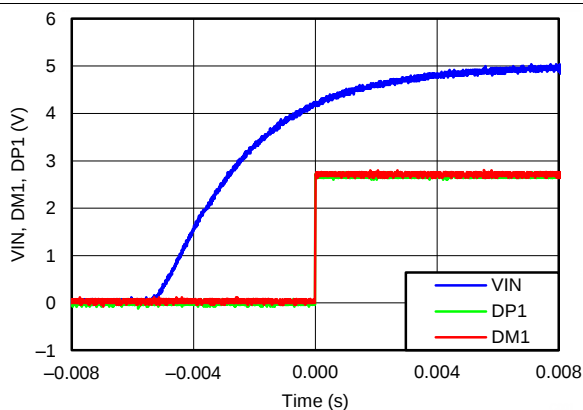


Figure 13. Power On (DM1 and DP1)

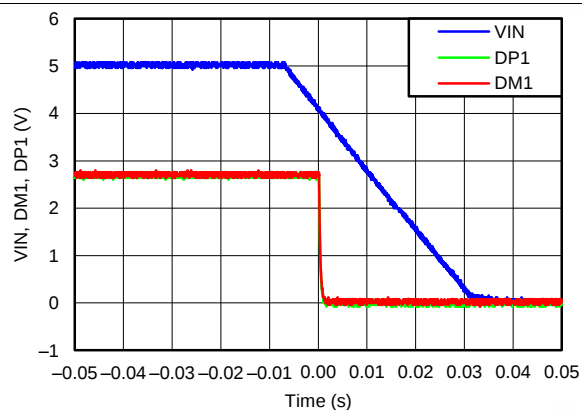


Figure 14. Power Off (DM1 and DP1)

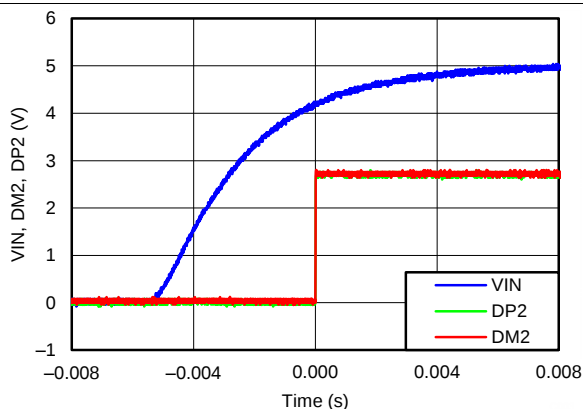


Figure 15. Power On (DM2 and DP2)

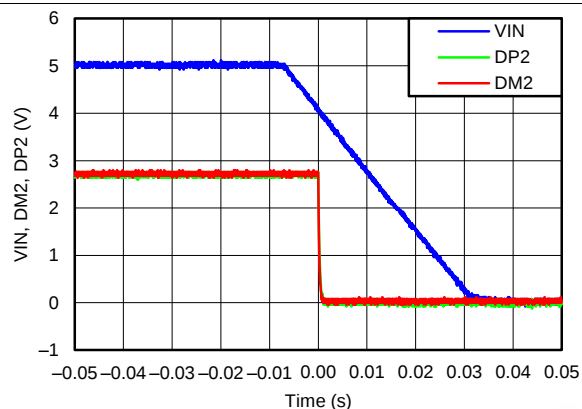


Figure 16. Power Off (DM2 and DP2)

10 Power Supply Recommendations

The devices only provide the correct electrical signatures on the data line of USB charger port and do not provide any power for the V_{BUS} . If a USB power switch is needed as an overcurrent protector, the TPS2561A-Q1 (SLVSCC6) is recommend.

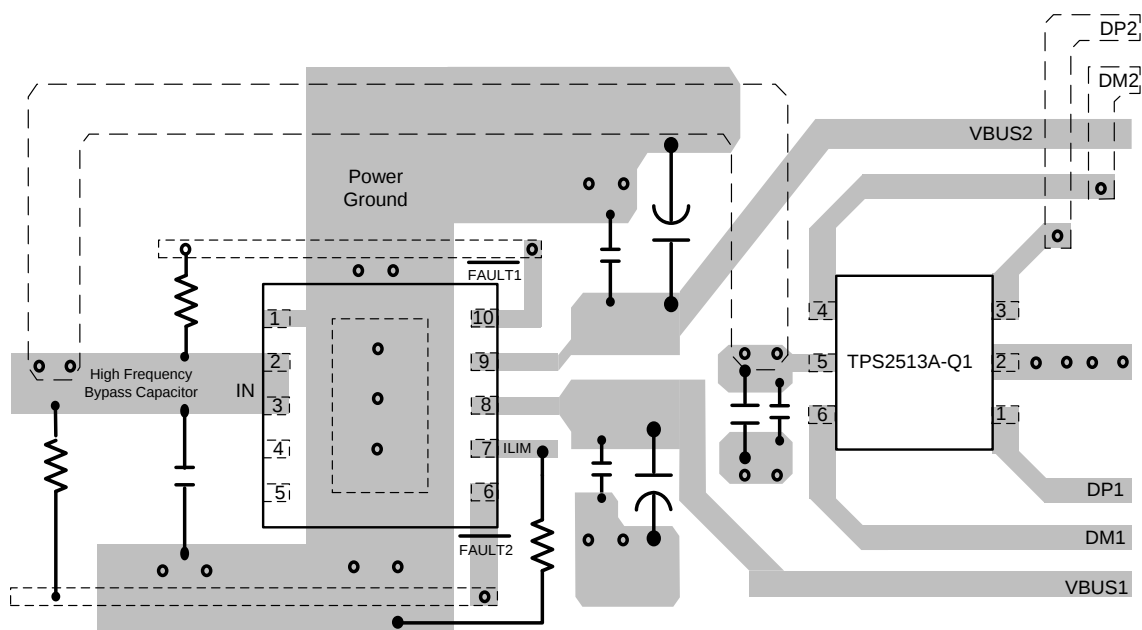
11 Layout

11.1 Layout Guidelines

- For all applications, a 0.1- μ F or greater ceramic bypass capacitor between IN and GND is recommended as close to the device as possible for local noise decoupling.
- When USB power switch is used, recommend connect TPS2513A-Q1 and TPS2514A-Q1 IN pin together with USB power switch IN pin. For TPS2513A-Q1, Dual channel USB power switch recommend TPS2561A-Q1, for TPS2514A-Q1, single channel USB power switch recommend TPS2557-Q1.
- Regarding TPS2561A-Q1 layout guidelines, see the TPS2561A-Q1 data sheet ([SLVSCC6](#)). Regarding TPS2557-Q1 layout guidelines, see the TPS2557-Q1 data sheet ([SLVSC97](#)).
- DP1 and DM1 provide one charging port controller, DP2 and DM2 provide another one charging port controller, when routing the trace, need consider the matching between DP and DM.

11.2 Layout Example

- VIA to Power Ground Plane



12 器件和文档支持

12.1 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS2513A-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS2514A-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.2 商标

All trademarks are the property of their respective owners.

12.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2513AQDBVRQ1	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	PB6Q
TPS2513AQDBVRQ1.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PB6Q
TPS2513AQDBVTQ1	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PB6Q
TPS2513AQDBVTQ1.A	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	PB6Q
TPS2514AQDBVRQ1	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	ZBAW
TPS2514AQDBVRQ1.A	Active	Production	SOT-23 (DBV) 6	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBAW
TPS2514AQDBVTQ1	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	ZBAW
TPS2514AQDBVTQ1.A	Active	Production	SOT-23 (DBV) 6	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	ZBAW

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS2513A-Q1, TPS2514A-Q1 :

- Catalog : [TPS2513A](#), [TPS2514A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2513AQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2513AQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2513AQDBVTQ1	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2514AQDBVRQ1	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS2514AQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2514AQDBVTQ1	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS2514AQDBVTQ1	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

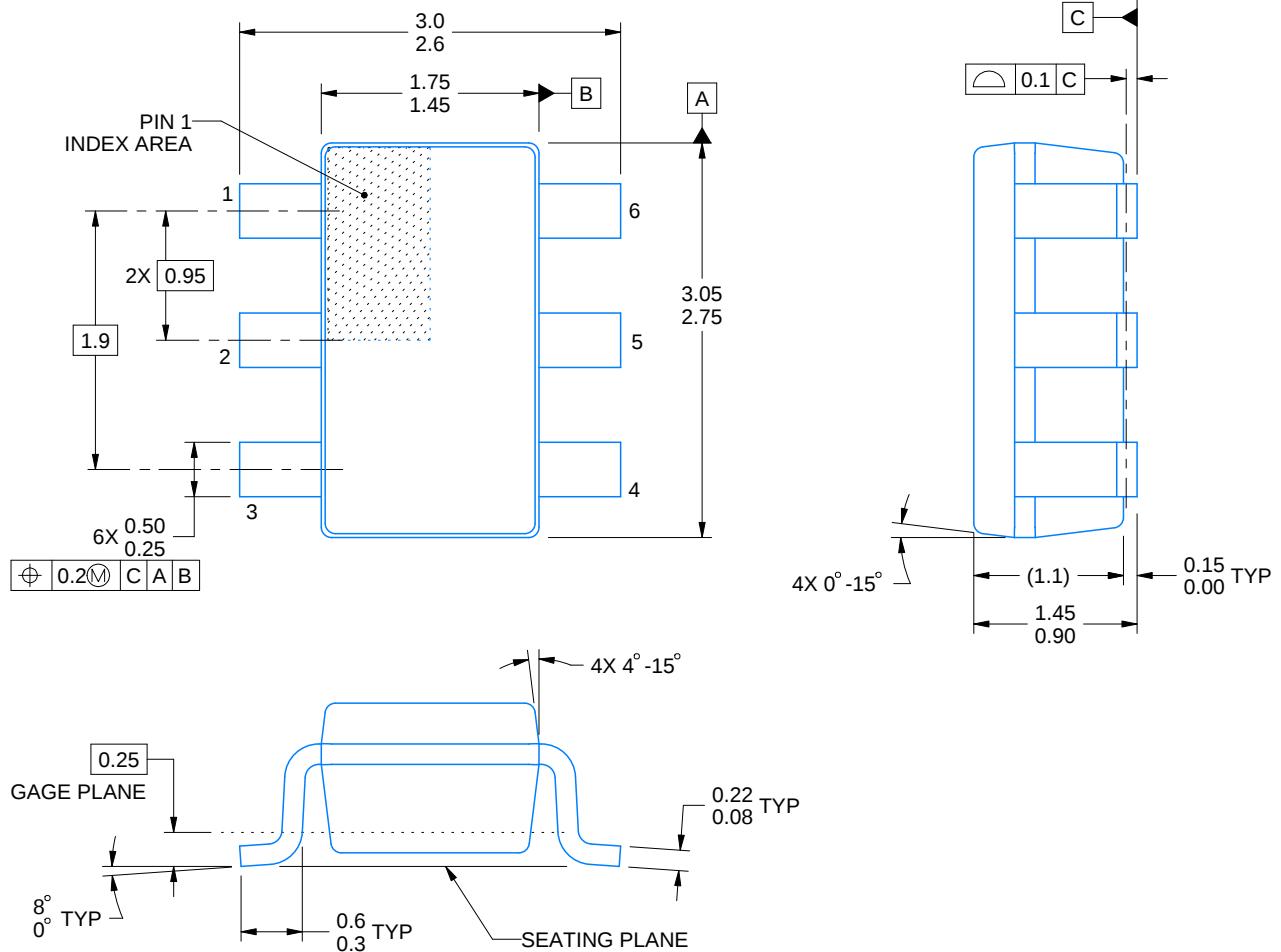


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2513AQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS2513AQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS2513AQDBVTQ1	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS2514AQDBVRQ1	SOT-23	DBV	6	3000	210.0	185.0	35.0
TPS2514AQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS2514AQDBVTQ1	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS2514AQDBVTQ1	SOT-23	DBV	6	250	210.0	185.0	35.0

DBV0006A**PACKAGE OUTLINE****SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



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NOTES:

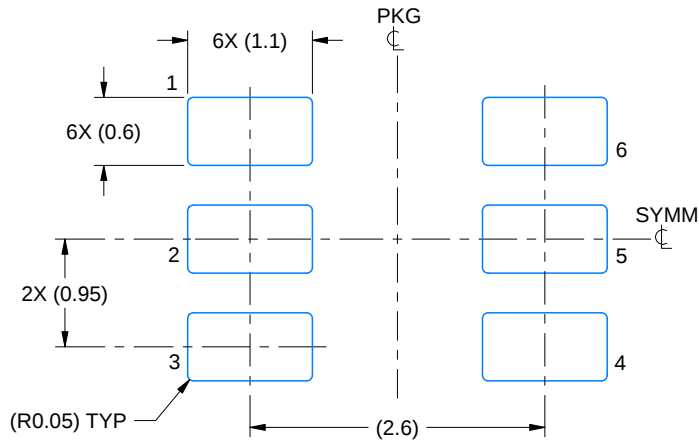
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

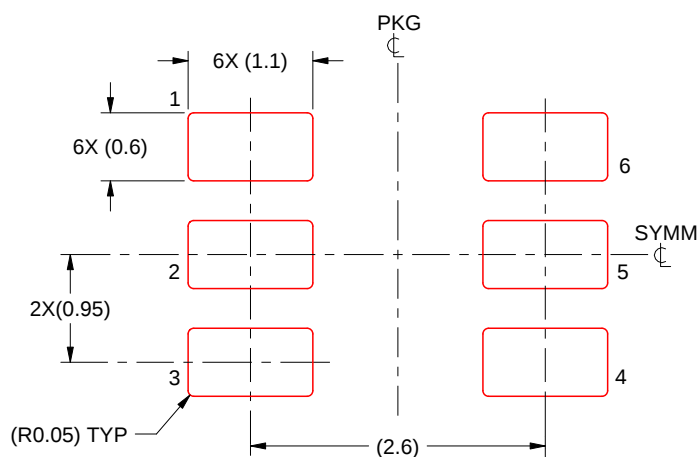
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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