TEXAS INSTRUMENTS
TPS22999
ZHCST55A – SEPTEMBER 2023 – REVISED NOVEMBER 2023

TPS22999 具有稳压浪涌电流的 4.5V、1.5A、7.5mΩ 导通电阻快速导通负载开关

1 特性

- 输入电压范围 (V_{IN})：0.1V - 4.5V
- 偏置电压范围：2.3V - 5.5V
- 最大持续电流：1.5A
- 导通电阻 (R_{ON})：7.5mΩ（典型值）
- 稳压浪涌电流
- 集成式快速输出放电：5.3Ω
- 开漏电源正常 ($\overline{PG}$) 信号
- 导通时间：V_{IN} = 1.0V 时低于 200µs
- 热关断
- VBIAS 欠压锁定 (UVLO)
- 低功耗：
  - 导通状态 (I_Q)：10µA（典型值）
  - 关闭状态 (I_{SD})：2.7µA（典型值）
- EN 引脚智能下拉电阻（$R_{PD,EN}$）
  - EN ≥ V_{IH} (I_{ON})：25nA（典型值）
  - EN ≤ V_{IL} ($R_{PD,ON}$)：500kΩ（典型值）

2 应用

- 可穿戴
- 固态硬盘
- PC 和笔记本电脑
- 工业 PC
- 光学模块

3 说明

TPS22999 是一款单通道负载开关，旨在实现快速导通时间和较低的浪涌电流。该器件包含一个可在 0.1V 至 V_{BIAS} - 1.0V 输入电压范围内运行的 N 沟道 MOSFET，并可支持高达 1.5A 的连续电流。

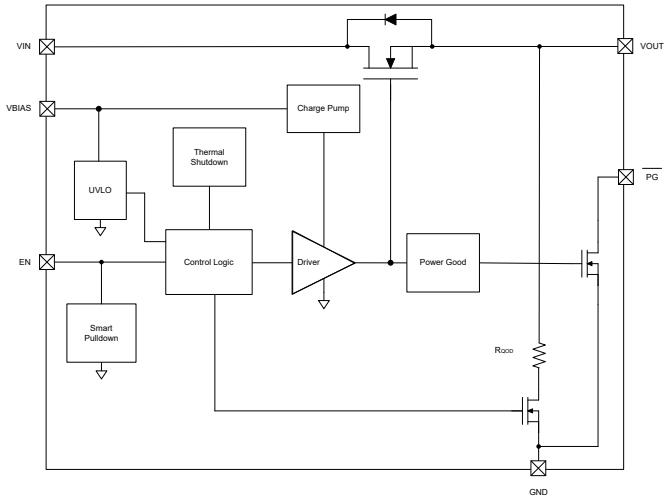
该开关由使能引脚 (EN) 控制，该引脚能够直接连接低电压 GPIO 信号 (V_{IH} = 0.8V)。TPS22999 器件在开关关闭时具有集成式 5.3Ω 快速输出放电路径，可实现可靠的系统运行。器件上有一个电源正常 ($\overline{PG}$) 信号，指示主 MOSFET 何时完全稳定至最低电阻路径，可用于启用下游负载。集成式热关断功能可确保在高温环境中提供保护。

TPS22999 采用间距为 0.35mm 的 8 引脚 WCSP 封装 (YCH)，并可在自然通风条件下的 -40°C 至 +105°C 温度范围内运行。

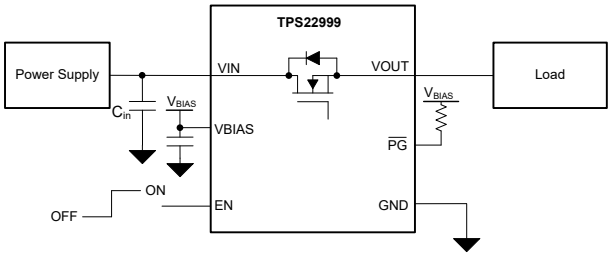
封装信息

器件型号	封装(1)	封装尺寸(2)
TPS22999	YCH（DSBGA，8）	1.4mm × 0.7mm

(1) 有关详细信息，请参阅 节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



TPS22999 方框图



TPS22999 典型应用

Table of Contents

4 Pin Configuration and Functions

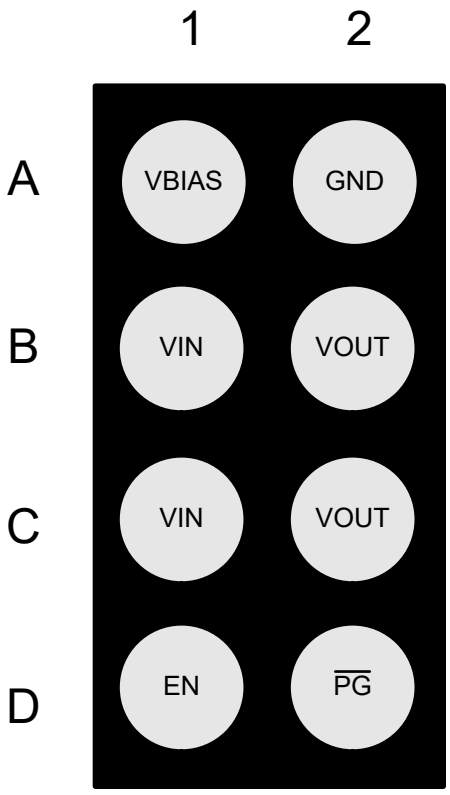


图 4-1. TPS22999 YCH Package, 8-Pin DSBGA (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VBIAS	A1	I	Device bias supply. Connect a 0.1-µF capacitor to ground.
GND	A2	—	Device ground
VIN	B1, C1	I	Switch input
VOUT	B2, C2	O	Switch output
EN	D1	I	Switch enable
$\overline{PG}$	D2	O	Open drain power-good signal, asserted low when the MOSFET has been fully enhanced. Connect to ground if unused.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	V_{IN} + 0.3	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{EN}, V_{PG}	Control pin voltage	–0.3	6	V
I_{MAX}	Maximum current		1.5	A
I_{MAX_PLS}	Maximum current (24 hours)		4.5	A
T_J	Junction temperature		Internally Limited	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	0.1		V_{BIAS} – 1.0	V
V_{OUT}	Output voltage, EN > V_{IH}	0.1		V_{IN}	V
V_{BIAS}	Bias voltage	2.3		5.5	V
V_{IH}	EN pin high voltage range	0.8		5.5	V
V_{IL}	EN pin low voltage range	0		0.35	V
C_{OUT}	Output capacitor(1)	0		70	µF
V_{PG}	$\overline{PG}$ pin voltage	0		5.5	V
T_A	Ambient temperature	–40		105	°C

(1) Effective output capacitance required for stability

5.4 Thermal Information

THERMAL METRIC(1) (2)		TPS22999 YCH (DSBGA) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	121.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Y_{JB}	Junction-to-board characterization parameter	34.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) The thermal parameters are based on a 4-layer PCB according to the JESD51-5 and JESD51-7 standards.

5.5 Electrical Characteristics (VBIAS = 5.5 V)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Power Consumption							
$I_{SD,VBIAS}$	VBIAS shutdown current	EN = 0 V	25°C		2.7		µA
			–40°C to 85°C			4	µA
			–40°C to 105°C			5	µA
$I_{Q,VBIAS}$	VBIAS quiescent current	EN > V_{IH}	25°C		10		µA
			–40°C to 85°C			18	µA
			–40°C to 105°C			20	µA
$I_{Q,VIN}$	VIN quiescent current	EN > V_{IH}	25°C		0.1		µA
			–40°C to 85°C			1	µA
			–40°C to 105°C			1.5	µA
$I_{SD,VIN}$	VIN shutdown current	EN = 0 V, V_{IN} = 4.5 V	25°C		0.1		µA
			–40°C to 85°C			1	µA
			–40°C to 105°C			3	µA
I_{EN}	EN pin leakage	EN = VBIAS	–40°C to 105°C		0.1		µA
Performance							

5.5 Electrical Characteristics (VBIAS = 5.5 V)（续）

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
R_{ON}	On-resistance	VIN = 4.5 V	25°C		7.5		mΩ
			– 40°C to 85°C			12	mΩ
			– 40°C to 105°C			15	mΩ
		VIN = 3.3 V	25°C		7.5		mΩ
			– 40°C to 85°C			12	mΩ
			– 40°C to 105°C			15	mΩ
		VIN = 1.8 V	25°C		7.5		mΩ
			– 40°C to 85°C			12	mΩ
			– 40°C to 105°C			15	mΩ
		VIN = 1.0 V	25°C		7.5		mΩ
			– 40°C to 85°C			12	mΩ
			– 40°C to 105°C			15	mΩ
		VIN = 0.78 V	25°C		7.5		mΩ
			– 40°C to 85°C			12	mΩ
			– 40°C to 105°C			15	mΩ
		VIN = 0.5 V	25°C		7.5		mΩ
			– 40°C to 85°C			12	mΩ
			– 40°C to 105°C			15	mΩ
$V_{OL,PG}$	Power-Good VOL	I_{PG} = 500uA	-40°C to 105°C			0.2	V
V_{BIAS_UVLO}	V_{BIAS} undervoltage lockout	Falling	– 40°C to 105°C	1.65	1.85	2.05	V
		Hysteresis	– 40°C to 105°C		0.150		V
		Rising	– 40°C to 105°C	1.8	2.0	2.2	V
I_{INRUSH}	Regulated inrush current	C_L = 60uF, V_{IN} ⩽ 1 V	– 40°C to 105°C		0.95	1.33	A
		C_L = 60uF, V_{IN} > 1 V	– 40°C to 105°C		0.95	1.4	A
$V_{HYS,EN}$	Enable pin hysteresis	VIN = 4.5 V	– 40°C to 105°C		75		mV
$R_{PD,EN}$	Smart pulldown Resistance	EN < V_{IL}	25°C		500		kΩ
			– 40°C to 105°C			750	kΩ
R_{QOD}	QOD resistance	VIN = 1.0 V	25°C		5.3		Ω
			– 40°C to 105°C			10	Ω
Protection							
TSD	Thermal shutdown		-	116	131	146	°C

5.6 Electrical Characteristics (VBIAS = 3.4 V)

over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Power Consumption							
$I_{SD,VBIAS}$	VBIAS shutdown current	EN = 0 V	25°C		2.2		μA
			– 40°C to 85°C			4	μA
			– 40°C to 105°C			5	μA

5.6 Electrical Characteristics (VBIAS = 3.4 V)（续）

over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$I_{Q,VBIAS}$	VBIAS quiescent current	EN > V_{IH}	25°C		10		μA
			–40°C to 85°C			18	μA
			–40°C to 105°C			20	μA
$I_{Q,VIN}$	VIN quiescent current	EN > V_{IH}	25°C		0.1		μA
			–40°C to 85°C			1	μA
			–40°C to 105°C			1.5	μA
$I_{SD,VIN}$	VIN shutdown current	EN = 0 V, V_{IN} = 2.4 V	25°C		0.1		μA
			–40°C to 85°C			1	μA
			–40°C to 105°C			2	μA
I_{EN}	EN pin leakage	EN = VBIAS	–40°C to 105°C		0.1		μA
Performance							
R_{ON}	On-resistance	VIN = 2.4 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 1.8 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 1.0 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.78 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.5 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
I_{INRUSH}	Regulated inrush current	C_L = 60 μF, V_{IN} ≤ 1 V	–40°C to 105°C		0.95	1.33	A
		C_L = 60 μF, V_{IN} > 1 V	–40°C to 105°C		0.95	1.4	A
$V_{OL,PG}$	Power-Good V_{OL}	I_{PG} = 500 μA	–40°C to 105°C			0.2	V
$V_{HYS,EN}$	Enable pin hysteresis	VIN = 2.4 V	–40°C to 105°C		75		mV
$R_{PD,EN}$	Smart pulldown resistance	EN < V_{IL}	25°C		500		kΩ
			–40°C to 105°C			750	kΩ
R_{QOD}	QOD resistance	VIN = 1.0 V	25°C		8.3		Ω
			–40°C to 105°C			19	Ω
Protection							

5.7 Electrical Characteristics (VBIAS = 2.3 V)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
Power Consumption							
$I_{SD,VBIAS}$	VBIAS shutdown current	EN = 0 V	25°C		2.1		μA
			–40°C to 85°C			3.5	μA
			–40°C to 105°C			4	μA
$I_{Q,VBIAS}$	VBIAS quiescent current	EN > V_{IH}	25°C		7.5		μA
			–40°C to 85°C			18	μA
			–40°C to 105°C			20	μA
$I_{Q,VIN}$	VIN quiescent current	EN > V_{IH}	25°C		0.1		μA
			–40°C to 85°C			1	μA
			–40°C to 105°C			1.5	μA
$I_{SD,VIN}$	VIN shutdown current	EN = 0 V, V_{IN}= 1.3 V	25°C		0.1		μA
			–40°C to 85°C			1	μA
			–40°C to 105°C			2	μA
I_{EN}	EN pin leakage	EN = VBIAS	–40°C to 105°C		0.1		μA
Performance							
R_{ON}	On-resistance	VIN = 1.3 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 1.0 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.78 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
		VIN = 0.5 V	25°C		7.5		mΩ
			–40°C to 85°C			12	mΩ
			–40°C to 105°C			15	mΩ
I_{INRUSH}	Regulated inrush current	C_L = 60 μF	–40°C to 105°C		0.9	1.33	A
$V_{OL,PG}$	Power-Good VOL	I_{PG} = 500 μA	–40°C to 105°C			0.2	V
$V_{HYS,EN}$	Enable pin hysteresis	VIN = 1.3 V	–40°C to 105°C		75		mV
$R_{PD,EN}$	Smart pulldown Resistance	EN < V_{IL}	25°C		500		kΩ
			–40°C to 105°C			750	kΩ
R_{QOD}	QOD resistance	VIN = 1.0 V	25°C		16		Ω
			–40°C to 105°C			35	Ω
Protection							
TSD	Thermal shutdown		-	116	131	146	°C

5.8 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). Measured 350 µs after Vbias > 2.3 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN = 4.5 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			440	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		200		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		40		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		850		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 3.3 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			365	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		170		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		30		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		750		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 1.8 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			255	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		95		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		30		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		900		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 1.0 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			200	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		60		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		27		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		800		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 0.78 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			182	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		40		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		30		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		780		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs
VIN = 0.5 V						
tON	Turn ON time	R_L = 100 Ω, C_L = 60 µF			170	µs
tRISE	Rise time	R_L = 100 Ω, C_L = 60 µF		30		µs
tD	Delay time	R_L = 100 Ω, C_L = 60 µF		27		µs
tFALL	Fall time	R_L = 100 Ω, C_L = 60 µF		750		µs
tOFF	Turn OFF time	R_L = 100 Ω, C_L = 60 µF			5	µs

5.9 Timing Diagrams

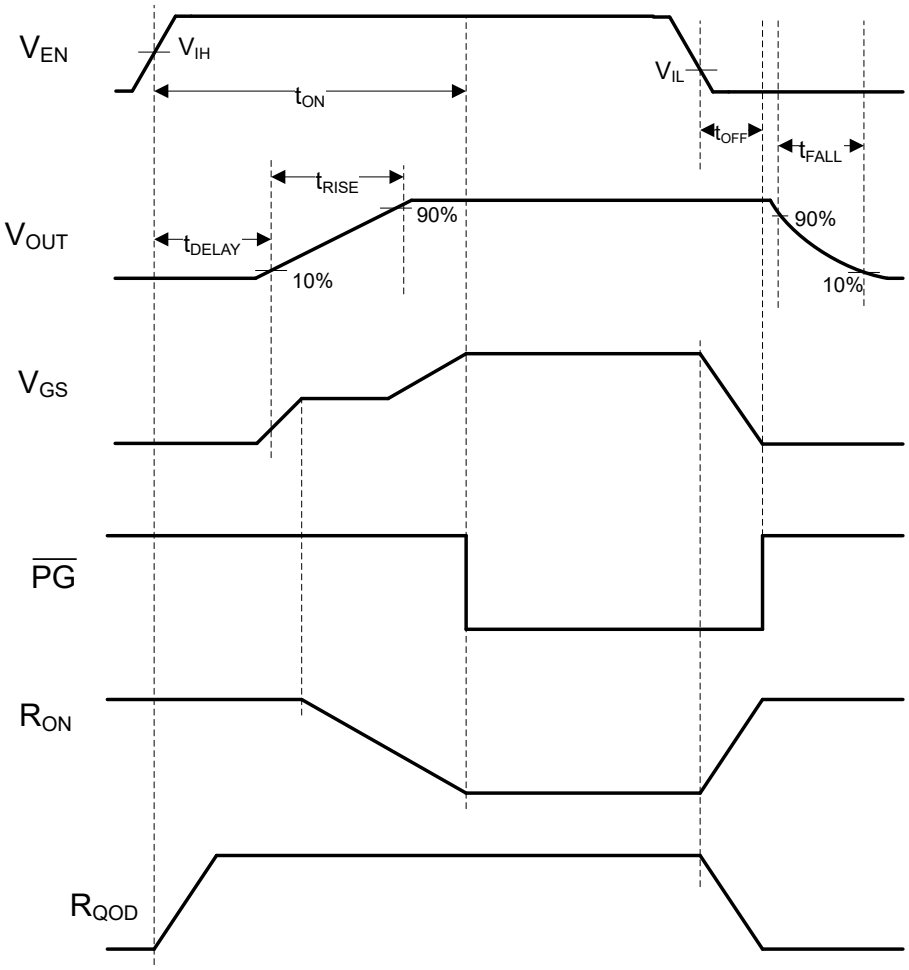
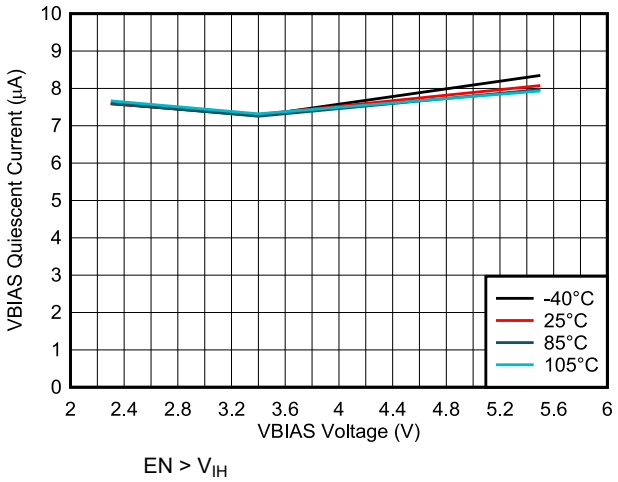


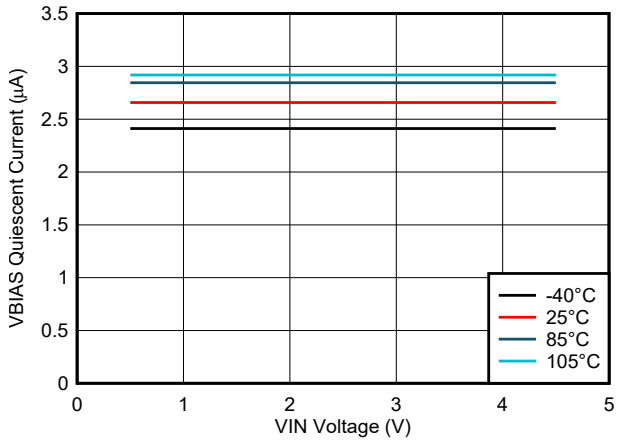
图 5-1. TPS22999 Timing Diagram

5.10 Typical Characteristics



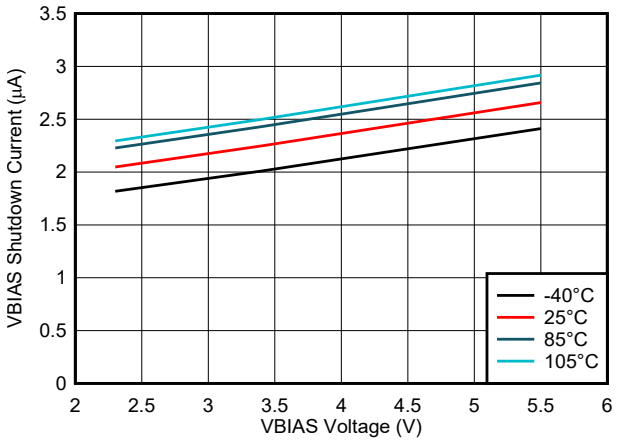
EN > V_{IH}

图 5-2. VBIAS Quiescent Current vs VBIAS Voltage



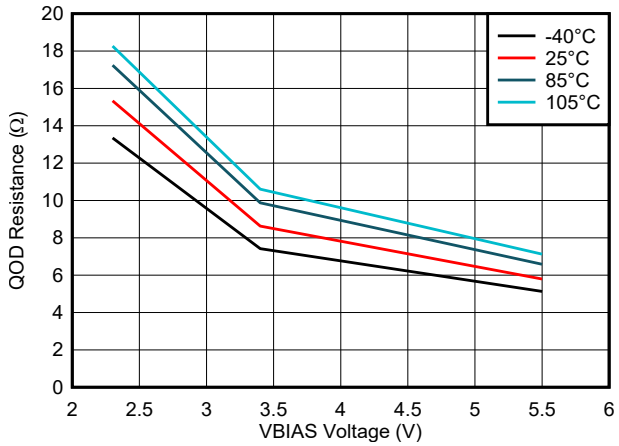
EN > V_{IH} VOUT = Open

图 5-3. VBIAS Quiescent Current vs VIN Voltage



EN = 0 V

图 5-4. VBIAS Shutdown Current vs VBIAS Voltage



EN = 0 V

图 5-5. QOD Resistance vs VBIAS Voltage

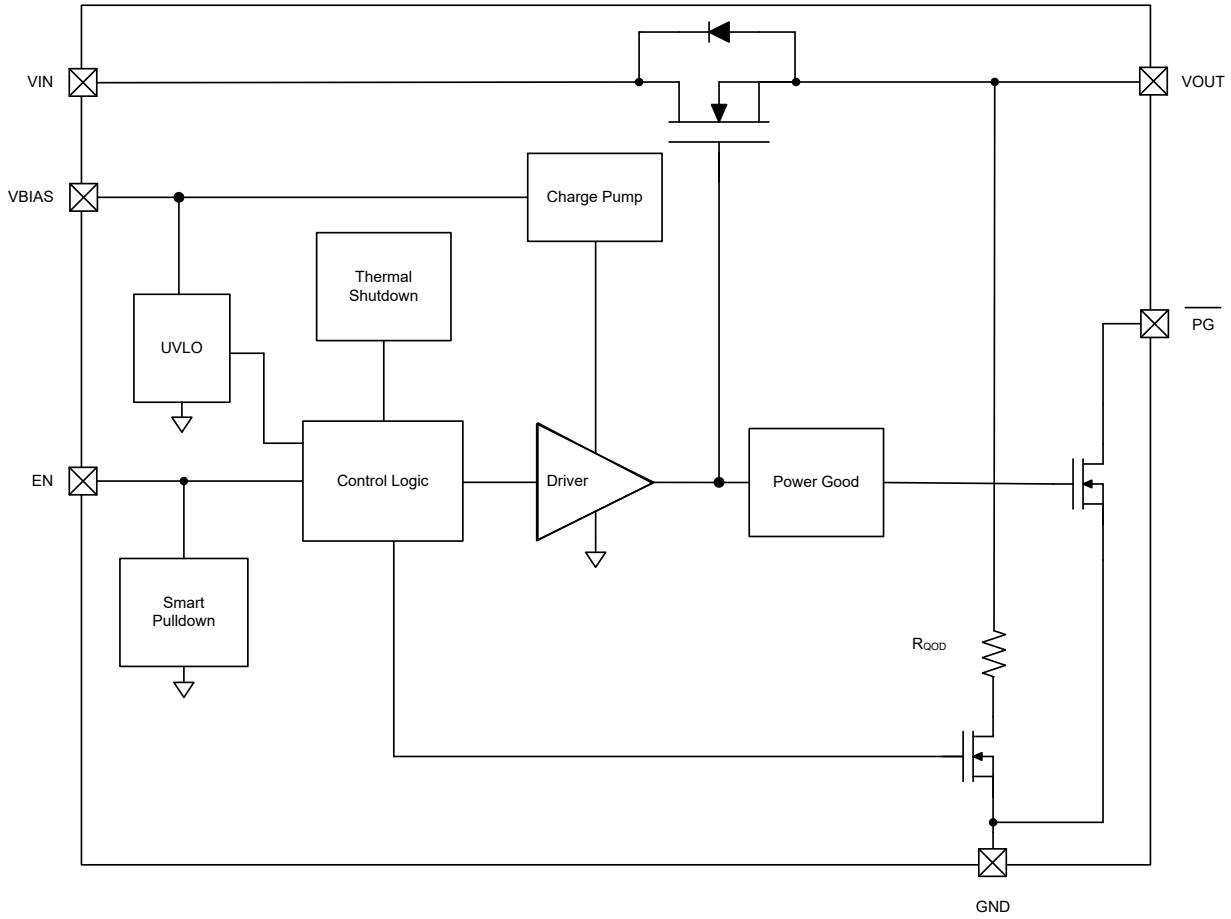
6 Detailed Description

6.1 Overview

The TPS22999 device is a single-channel load switch with a 7.5-mΩ power MOSFET designed to operate up to 1.5 A. The voltage range is 0.1 V to 4.5 V. The device regulates inrush current upon turn-on while providing a fast turn-on time.

The switch is controlled by an enable pin (EN), which is capable of interfacing directly with low voltage GPIO signals down to the V_{IH} level of 0.8 V. The TPS22999 device has an integrated 10-Ω quick output discharge when switch is turned off. There is a Power-Good ($\overline{PG}$) signal on the device that indicates when the main MOSFET is fully turned on and the on-resistance is at final value.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 ON and OFF Control

The EN pin controls the state of the switch. The EN pin is compatible with standard GPIO logic threshold so the EN pin can be used in a wide variety of applications. When power is first applied to VIN, a Smart Pulldown is used to keep the EN pin from floating until the system sequencing is complete. After the EN pin is deliberately driven high ($\geq V_{IH}$), the Smart Pulldown is disconnected to prevent unnecessary power loss. See the following table for when the EN Pin Smart Pulldown is active.

EN Pin Voltage	EN Pin Function
⩽ V_{IL}	Pulldown active
⩾ V_{IH}	No pulldown

6.3.2 Regulated Inrush Current

Depending on the rise time at power-up, output load capacitances can cause large inrush currents that are limited only by parasitic resistance and inductances present in wiring and interconnections. These high currents can cause input voltage supply droop which can harm or cause malfunction in other circuits in the system.

To prevent these problems, TPS22999 regulates the inrush current(I_{INRUSH}) to a 1-A typical during the turn-on phase. This regulation enables the system to operate reliably while maintaining a fast turn-on time.

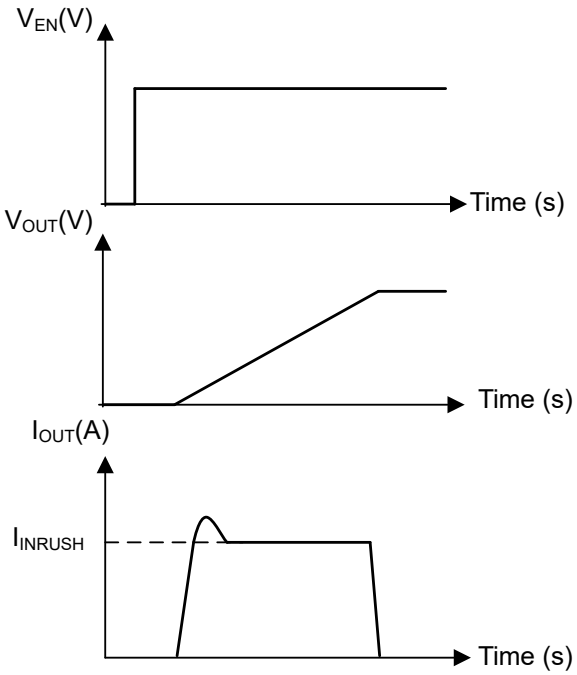


图 6-1. Regulated Inrush Current Behavior

6.3.3 Integrated Quick Output Discharge

TPS22999 integrates Quick Output Discharge (QOD). When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 10 Ω and prevents the output from floating while the switch is disabled while helping safely discharge output capacitances to ground.

6.3.4 Thermal Shutdown

When the device temperature reaches 131°C (typical), the device latches itself off to prevent thermal damage. The $\overline{PG}$ pin is deasserted to signal the output has been latched off. While T_J is over the T_{ABS} threshold, the output remains disabled even if the EN pin is toggled. After T_J decreases below the T_{ABS} threshold, the device does not enable the channel until the EN pin is toggled.

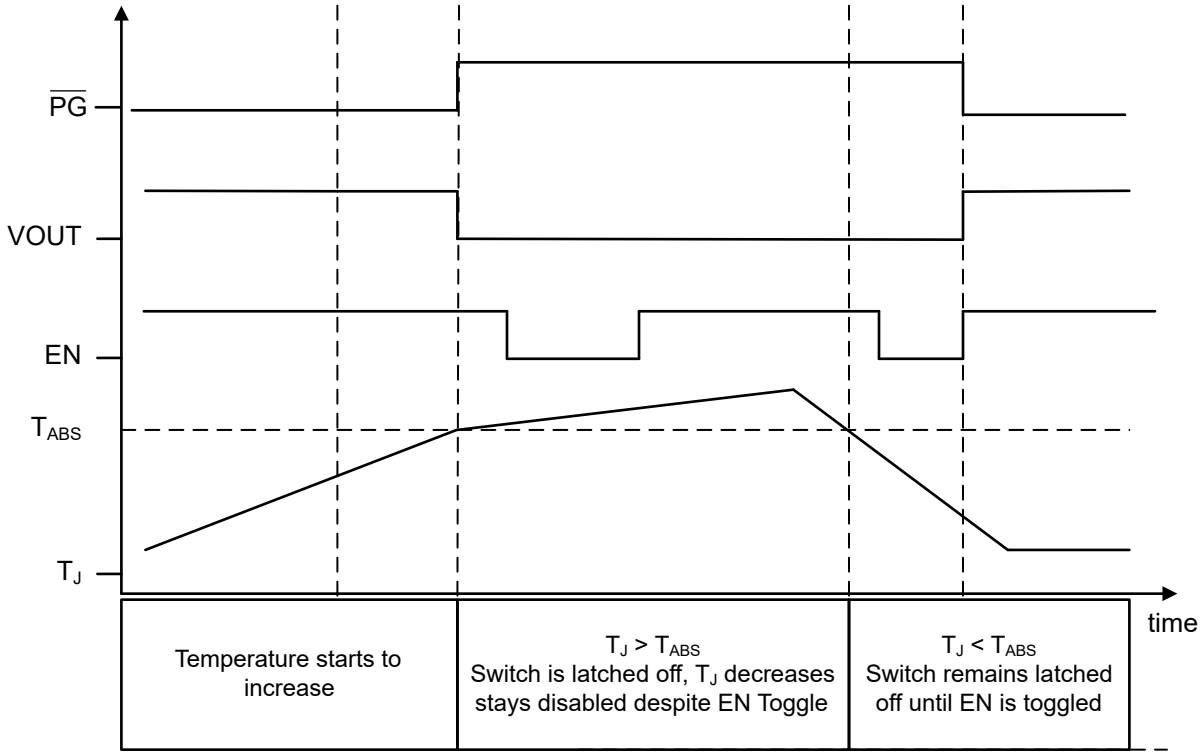


图 6-2. Thermal Shutdown Behavior

6.3.5 Power-Good (PG) Signal

The TPS22999 device has a Power-Good ($\overline{PG}$) output signal to indicate the gate of the pass FET is driven high and the switch is on with the on-resistance close to final value (full load ready). The signal is an active low and open drain output which can be connected to a voltage source through an external pullup resistor, R_{PU}. This voltage source can be VOUT from the TPS22999 device or another external voltage. VBIAS is required for PG to have a valid output.

6.4 Device Functional Modes

The following table summarizes the device functional modes:

EN	Fault Condition	VOUT State	nPG
L	N/A	Hi-Z	Hi-Z
H	None	V_{IN} (through R_{ON})	LO
X	Thermal shutdown	Hi-Z	Hi-Z

7 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

7.2 Typical Application

This typical application demonstrates how to use the TPS22999 device to limit start-up inrush current.

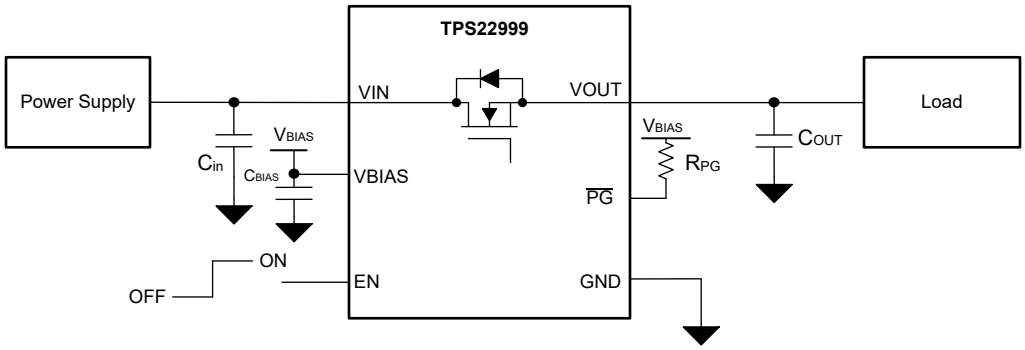


图 7-1. TPS22999 Basic Application

表 7-1. Component Descriptions

DESIGN PARAMETER	TYPICAL VALUES	DESCRIPTION
C_{IN}	1 μF	Filtering voltage transients
C_{OUT}	100 nF	Filtering voltage transients
C_{BIAS}	0.1 μF	Filtering voltage transients and noises
R_{PG}	10 kΩ	Pullup resistor for the open-drain output

7.2.1 Design Requirements

For this example, the values below are used as the design parameters.

表 7-2. Design Parameters

PARAMETER	VALUE
V_{BIAS}	3.4 V
V_{IN}	1.8 V
Load capacitance	60 μF
Inrush current	1 A

7.2.2 Detailed Design Procedure

When the switch is enabled, the switch charges up the output capacitance from 0 V to the set value (1.8 V in this example). This charge arrives in the form of inrush current. As the inrush current is controlled by the device, the time to fully charge up a capacitor can be calculated with the following formula:

$t_{charge}=V_{IN} / I_{inrush} \times C_L$

where:

- C_L is the output capacitance.
- I_{inrush} is the inrush current limited internally by the device
- V_{IN} is the input voltage

The TPS22999 offers an internally set inrush current limit (0.9-A typical with 3.4-V V_{BIAS}), which allows the customer to calculate the time to fully charge up a load capacitance.

$$t_{charge} = 1.8\ V / 0.9\ A \times 60\ \mu F \quad (1)$$

$$t_{charge} = 130\ \mu s \quad (2)$$

With TPS22999, the time to charge up a 60-μF capacitor to 1.8-V V_{IN} voltage is 130-μs typical at 3.4-V V_{BIAS} voltage.

7.3 Power Supply Recommendations

The TPS22999 device is designed to operate with a VIN range of 0.1 V to V_{BIAS} – 1 V. Regulate the VIN power supply well and place as close to the device terminal as possible. The power supply must be able to withstand all transient load current steps. In most situations, using an input capacitance (C_{IN}) of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance can be required on the input. TI recommends to connect a 0.1-uF capacitance to V_{BIAS}.

7.4 Layout

7.4.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, place the input and output capacitors close to the device to minimize the effects that parasitic trace inductances can have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

7.4.2 Layout Example

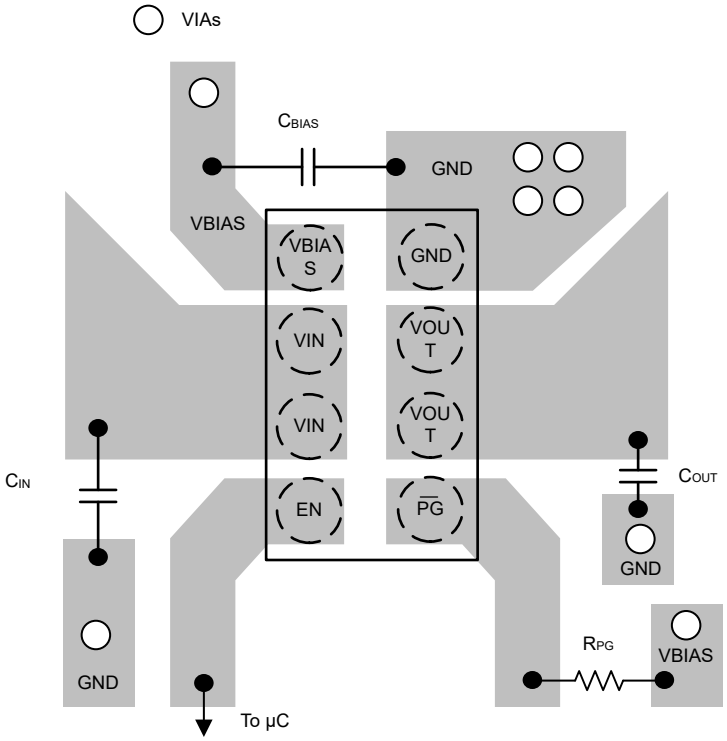


图 7-2. TPS22999 Layout Example

8 Device and Documentation Support

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 Trademarks

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8.4 静电放电警告

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (September 2023) to Revision A (November 2023)	Page
• 将文档状态从“预告信息”更改为“量产数据”	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22999YCHR	Active	Production	DSBGA (YCH) | 8	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	R
TPS22999YCHR.A	Active	Production	DSBGA (YCH) | 8	12000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 105	R

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

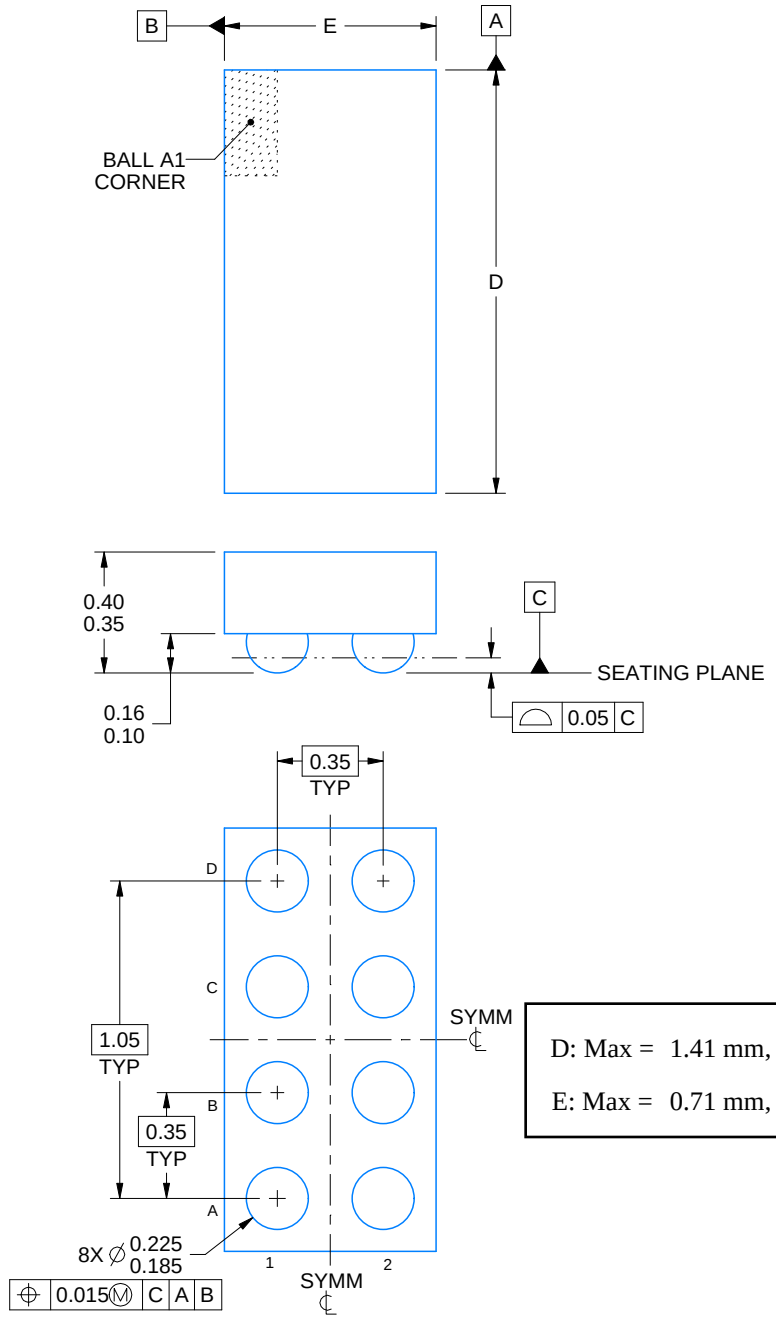
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

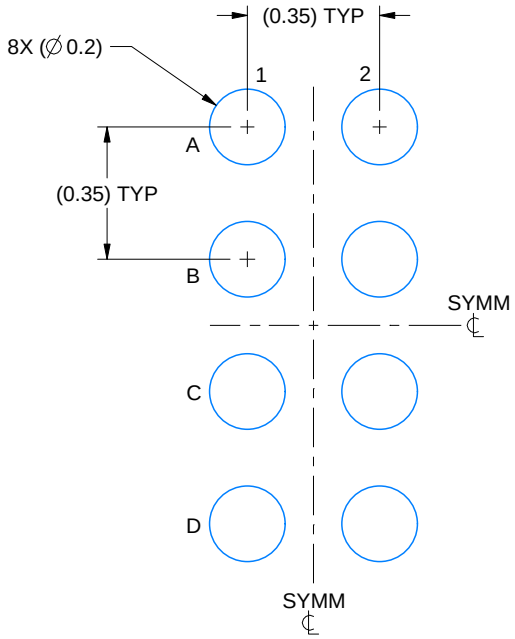
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

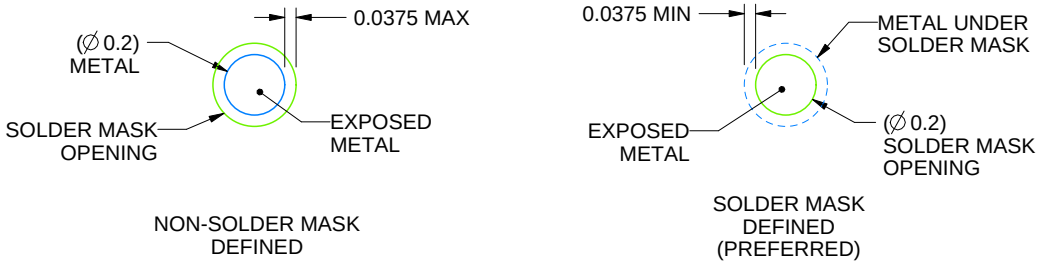


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

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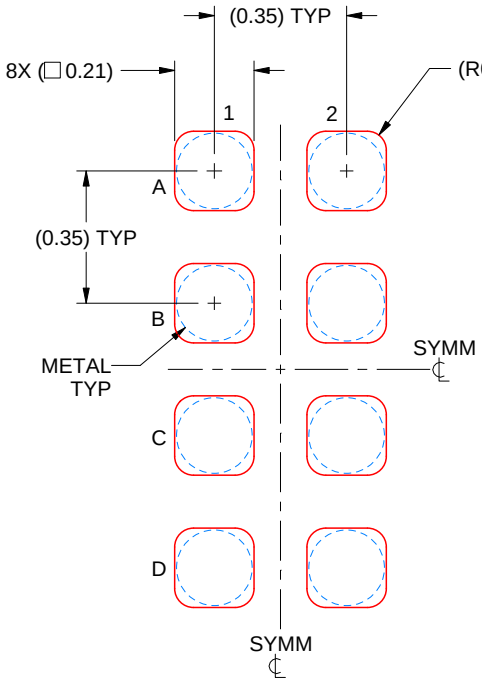
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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