Thunderbolt™ 电源选择集成电路 (IC)

查询样品: TPS22986

特性

- **2.8V** 至 **19.8V** 输入
- 自动选择 **3.3V** 电源
- **>10mA** 低功率开关
- **>500mA** 高功率开关
- 从 **OUT** 至 **VDD** 的反向电流阻止
- 通用异步收发器 **(UART)** 输入活动上唤醒
- **UART RX** 和 **TX** 缓冲器

应用范围

- **Thunderbolt™** 线缆
- 笔记本电脑
- 台式机
- 电源管理系统

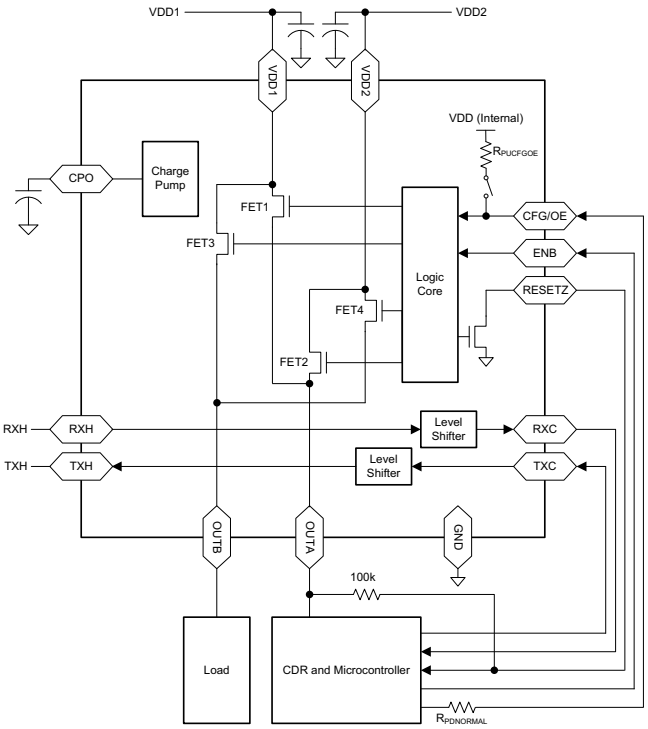


图 **1.** 典型应用

说明

TPS22986 是一款用于有源 Thunderbolt™ 线缆的电源选择器件。 此器件从两个可用的电源中选择一个 3.3V 输入并将选中的输入连接至两个输出，OUTA 和 OUTB。 当 3.3V 电源未出现时，输出变成高阻抗。

TPS22986 有两个运行模式，正常模式和控制模式。在正常模式下，当一个有效电源出现时，OUTA 一直接通。 当 ENB 输入为高电平时，OUTB 被连接至一个有效电源。

在控制模式中，OUTA 运行方式与正常模式下一样而 OUTB 由VDD1 及 VDD2 上的受监控输入和有效电源组合控制。 当一个有效 VDD 可用时，此器件在 ENB 上等待一个上升输入，然后在下一个下降 RXH 转变到来前，断开 OUTB。 一旦下一个下降 RXH 转变发生时，此器件重新连接 OUTB。

在任一模式下，当一个有效 VDD 不可用时，TPS22986 打开所有开关并且输出 OUTA 和 OUTB 变成高阻抗。 当被连接的 VDD 超过 3.6V 时，它从输出上断开。

TPS22986 采用 1.6mm x 1.6mm 晶圆级芯片 (WCSP) 封装。

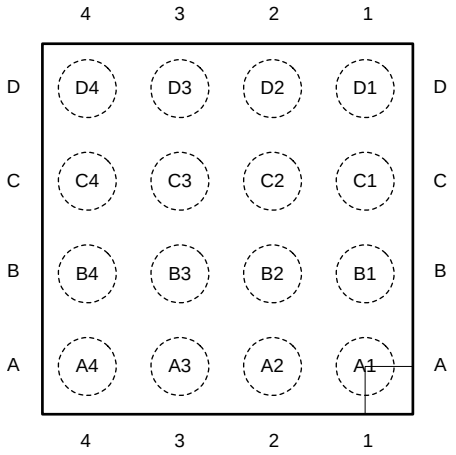
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

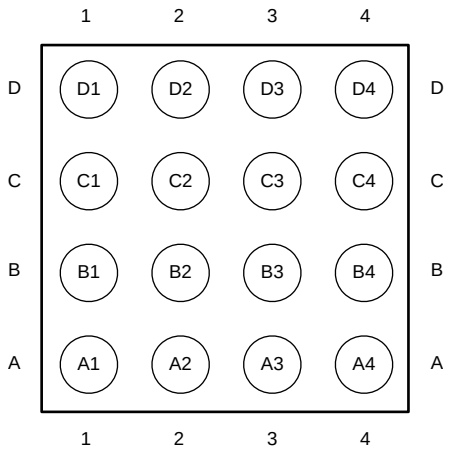
PART NUMBER	PACKAGE MARKING(1)	PACKAGE	DEVICE SPECIFIC FEATURES
TPS22986YFP	YMDDJS	YFP	WCSP

(1) Y=Year, M=Month, D=Sequence Code, DJ=TPS22986 Device Code, S=Wafer Fab/Assembly Site Code

Top View/Footprint



Bump View



Die Size: 1.6mm x 1.6mm
Bump Size: 0.25mm
Bump Pitch: 0.4mm

TPS22986 Pin Mapping (Top View)

	4	3	2	1
D	VDD1	VDD1	VDD2	VDD2
C	OUTA	OUTB	OUTB	GND
B	RXH	TXH	RESETZ	CPO
A	RXC	TXC	ENB	CFG/OE

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE θ_{JA}	THERMAL RESISTANCE(1) θ_{JB}	POWER RATING T_A = 25°C	DERATING FACTOR ABOVE(2) T_A = 25°C
YFP	95°C/W	63°C/W	1050 mW	10.5 mW/°C

(1) Simulated with high-K board
(2) Maximum power dissipation is a function of $T_{J(max)}$, θ_{JA} and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_{J(max)} – T_A) / \theta_{JA}$.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)(2)

		VALUE	UNIT
V_I	Voltage range on VDD1, VDD2(3)	–0.3 to 20	V
	Voltage range on OUTA, OUTB(3)	–0.3 to 4.0	V
	Voltage range on RXC, TXH, RESETZ, CFG/OE, ENB (3) (4) (VDD is the active valid 3.3V input at VDD1 or VDD2)	–0.3 to VDD+0.3	V
	Voltage range on CPO(3)	–0.3 to 13	V
	Voltage range on RXH, TXC(3)	–0.3 to 4.0	V
T_A	Operating ambient temperature range	–40 to 85	°C
$T_{J\ (MAX)}$	Maximum operating junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 150	°C
	Charge Device Model (JESD 22 C101)	500	V
	Human Body Model (JESD 22 A114)	2	kV
	Contact discharge on VDD1, VDD2 (IEC 61000-4-2)(5)	4.4	kV

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [$T_{A(max)}$] is dependent on the maximum operating junction temperature [$T_{J(max)}$], the maximum power dissipation of the device in the application [$P_{D(max)}$], and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.
(3) All voltage values are with respect to network ground terminal.
(4) All inputs must be connected to a supply that is less than the max of VDD1 and VDD2
(5) IEC tests are run with 0.1µF on VDD1 and VDD2. IEC rating is non-destructive.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD1}	Supply voltage range		2.8	19.8	V
V_{DD2}			2.8	19.8	V
$I_{LIM1/2}$	FET1 and FET2 Switch current range			10	mA
$I_{LIM3/4}$	FET3 and FET4 Switch current range			500	mA
V_{IH}	Input logic high	RXH, TXC, CFG/OE, ENB	2		V
V_{IL}	Input logic low	RXH, TXC, CFG/OE, ENB		0.8	V
V_{OH}	Output logic high	RXC, TXH, RESETZ	2.25		V
V_{OL}	Output logic low	RXC, TXH, RESETZ		0.4	V
C_{OUT}	Output capacitance on OUTA		1	4	µF
	Output capacitance on OUTB		4	22	
C_{CPO}	Output capacitance on CPO		2	10	nF
T_A	Operating temperature range		–40	85	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temp –40°C ≤ T_J ≤ 85°C. Typical values are for V_{DD} = 3.3V and T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
$V_{DD1/2}$	Input voltage range			2.8		19.8	V
I_{DD-1}	VDD1 Quiescent current	V_{DD1} = 2.8 to 15V	$V_{DD1} > V_{DD2}$		250	500	µA
			$V_{DD1} < V_{DD2}$		20		
I_{DD-2}	VDD2 Quiescent current	V_{DD2} = 2.8 to 15V	$V_{DD2} > V_{DD1}$		250	500	µA
			$V_{DD2} < V_{DD1}$		20		
I_{IN-ENB}	ENB Input current	V_{IN} = 1.8V to 3.6V				1	µA
$I_{IN-UART}$	RXH and TXC input current	V_{IN} = 1.8V to 3.6V				6	µA
$I_{IN-CFGOE}$	CFG/OE Input current after mode selection	V_{IN} = 1.8V to 3.6V				3	µA
$I_{IN-RESETZ}$	RESETZ Input current	V_{RESETZ} = 100 mV		0.8	2	3	mA
SWITCH AND RESISTANCE CHARACTERISTICS							
$R_{F1/2}$	FET1/2 On resistance	V_{DD} = 3.3V, I_{OUT} = 10mA			1	3	Ω
$R_{F3/4}$	FET3/4 On resistance	V_{DD} = 3.3V, I_{OUT} = 350mA			120	175	mΩ
$R_{PDRESETZ}$	RESETZ Pull-down resistance	RESETZ asserted		33	50	100	Ω
$R_{PUCFGOE}$ (1)	CFG/OE Pull-up resistance			15	20	25	kΩ
R_{PDUART}	TXC and RXH	See the UART RX and TX Section		0.6	1	1.75	MΩ
	Pull-down resistance						
$R_{PDNORMAL}$	Series CFG/OE Resistance to enter normal mode	See Mode Selection Section		35	50		kΩ
$R_{PDCONTROL}$	CFG/OE Resistance to GND to enter control mode	See Mode Selection Section			10	12	kΩ
VOLTAGE THESHOLDS AND AMPLITUDES							
V_{HVLO}	High voltage lockout	3.3V Supply Rising		3.5	3.55	3.6	V
	Hysteresis			20	40	60	mV
V_{UVLO}	Under voltage lockout	3.3V Supply Rising		2.7	2.75	2.8	V
		3.3V Supply Falling		2.4	2.45	2.5	
V_{CPO}	Charge pump voltage	C_{CPO} = 2nF, I_{CPO} = 0mA		8	9	11	V
V_{OS}	Voltage overshoot on OUTA/B	C_{OUTB} = 4µF, I_{OUTB} = 0mA, C_{OUTA} = 1µF, I_{OUTA} = 0mA, VDD1 $SR_{3.3→4V}$ = 10mV/µs				200	mV
TRANSITION TIMING							
t_d	UVLO To FETn open time	COUTB = 4µF				200	µs
t_e	UVLO To FETn closed time	COUTA = 1µF				2	ms
t_{dh}	HVLO To FETn open time					20	µs
t_{eh}	HVLO To FETn closed time	See The Supply Switch-Over During HVLO Section					
TRANSITION TIMING (NORMAL MODE)							
t_{eb}	ENB To FET3/4 closed time	COUTB = 4µF				2	ms
t_{db}	ENB To FET3/4 open time	COUTA = 1µF				200	µs
t_{E2R}	ENB to RESETZ time					6	ms

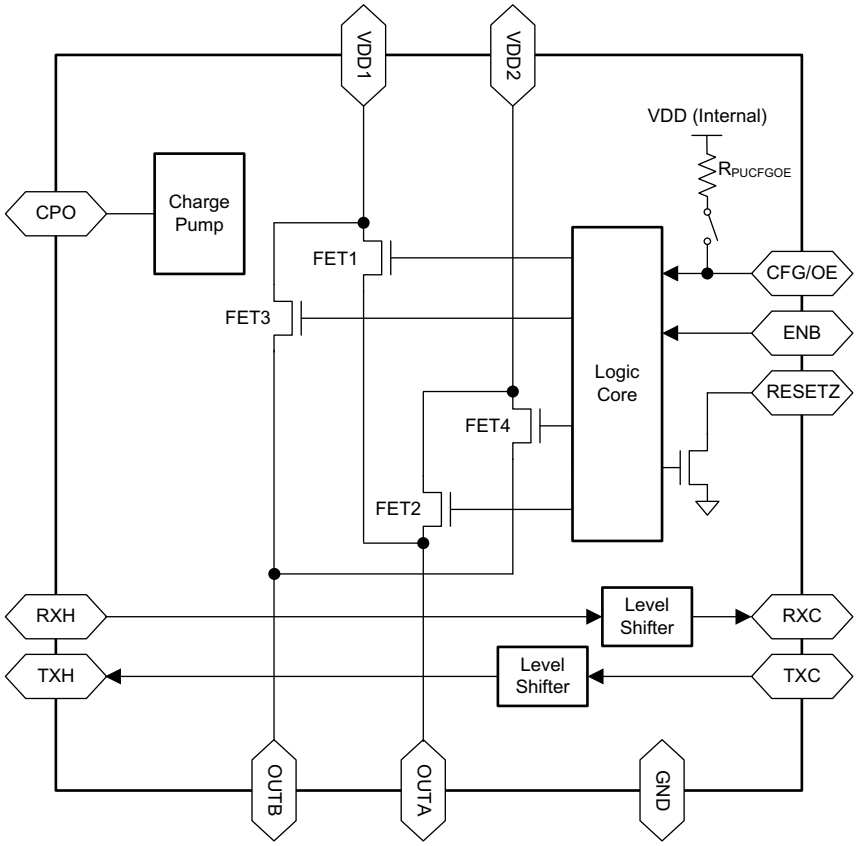
(1) CFG/OE is pulled to the internal VDD (VDD1 or VDD2) through the resistance $R_{PUCFGOE}$ only during mode selection at power-up.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted the specification applies over the V_{DD} range and operating junction temp –40°C ≤ T_J ≤ 85°C. Typical values are for V_{DD} = 3.3V and T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSITION TIMING (CONTROL MODE)						
t_{U2R}	UVLO to RESETZ time		5	6	7	ms
t_{E2R}	ENB to RESETZ time			2	10	µs
t_{E2O}	ENB to FET3/4 open time	COUTB = 4µF, COUTA = 1µF		100	200	µs
t_{RX2O}	RX to FET3/4 closed time	COUTB = 4µF, COUTA = 1µF		0.8	2	ms
t_{RX2R}	RX to RESETZ time		5	6	7	ms
t_{OE2TX}	OE to TXH valid time	RTXH = 100kΩ to GND			20	µs
t_{OE2TXZ}	OE to TXH Hi-Z time	RTXH = 100kΩ to GND			20	µs
TXC / TXH / RXC / RXH I/O						
V_{IH}	TXC, RXH Input logic high		2			V
V_{IL}	TXC, RXH Input logic low				0.8	V
V_{OH}	TXH, RXC Output logic high		2.25			V
V_{OL}	TXH, RXC Output logic low				0.4	V
T_R / T_F	TXH, RXC rise/fall time	10-90% CL = 20pF	5		70	ns
Z_O	TXH Output impedance		45	70	90	Ω
Z_O	RXC Output impedance		29	32	35	Ω
f_{MAX}	TXC, RXH Signal frequency				1	Mb/s
DC	TXC, RXH Duty cycle		40%		60%	
THERMAL SHUTDOWN						
T_{SD}	Shutdown temperature		110		130	°C
T_{SDHYST}	Shutdown hysteresis			15		°C

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTIONS

PIN NAME	TYPE	DESCRIPTION
VDD1	Supply	**Device Supply 1**. 0V to 19.8V Input.
VDD2	Supply	**Device Supply 2.** 0V to 19.8V Input.
OUTA	Output	**Output A.** 10mA capable output. Refer to the OUTA Supply Selection section for more information
OUTB	Output	**Output B.** 500mA capable output. Refer to the OUTB Supply Selection section for more information
CPO	Output	**Charge Pump Output.** This pin is the output of the internal charge pump. It drives the gates fo the internal FET switches. Connect a capacitor of at least 2nF between this pin and GND.
CFG/OE	Input	**Mode Configuration/Output Enable.** When CFG is floating or pulled high, the device is in Normal Mode. When CFG is ground, the device is in Control Mode (see Application Description section for more information), the mode is latched at power-up. Refer to the Mode Selection section for more information. After the mode is latched, this pin becomes the output enable for the UART TXH output. Refer UART RX and TX section for more information.
RXH	Input	**UART RX Input.** This input is buffered and level-shifted on RXC. In Control Mode, this pin in monitored for a high to low transition to enable the outputs. Refer UART RX and TX section for more information.
RXC	Output	**UART RX Output.** This output is a level shifted version of RXH. RXC is referenced to OUTA. Refer UART RX and TX section for more information.
TXC	Input	**UART TX Input.** This input is buffered and level-shifted on TXH. Refer the UART RX and TX section for more information.
TXH	Output	**UART TX Output.** This output is a buffered version of TXC. TXH is referenced to OUTA. Refer UART RX and TX section for more information.
RESETZ	Output	**Active Low Reset Output.** This pin is a delayed reset signal indicating OUTB is connected to a valid VDD. RESETZ is low when OUTB is high impedance. RESETZ is an open drain output.
ENB	Input	**OUTB Enable.** In Normal Mode, this pin is the active-high OUTB enable. In Control Mode, this pin opens OUTB when asserted high and latches this condition.
GND	Supply	**Device ground.**

APPLICATION INFORMATION

OUTA Supply Selection

The TPS22986 chooses between two different power supplies, VDD1 or VDD2, and connects these to OUTA. When a valid VDD (V_{UVLO} < VDD < V_{HVLO}) is present on VDD1 or VDD2, the valid VDD is connected to OUTA. When VDD1 > V_{HVLO} and a valid VDD is present on VDD2, the TPS22986 connects OUTA to VDD2. VDD1 will always take priority over VDD2. VDD2 will only be connected to OUTA when VDD1 < V_{UVLO} or VDD1 > V_{HVLO}. When OUTA is connected to VDD2 and VDD1 becomes valid (V_{UVLO} < V_{DD} < V_{HVLO}), the TPS22986 will disconnect OUTA from VDD2 and connect it to VDD1. Note, VDD1 and VDD2 may power up in any order. Figure 2 shows a flow diagram illustrating the selection of VDD1 or VDD2 as the appropriate supply to connect to OUTA.

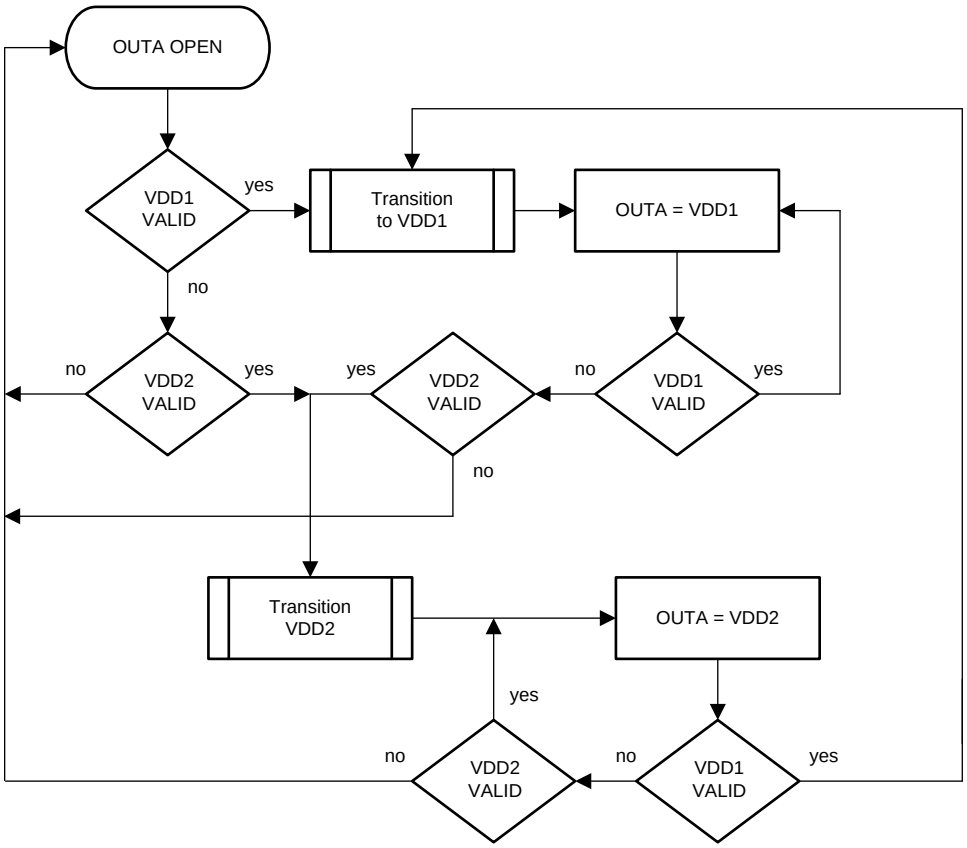


Figure 2. OUTA Supply Selection

OUTB Supply Selection

The TPS22986 chooses between two different power supplies, VDD1 or VDD2, and connects these to OUTB. At initial power-up, when a valid VDD (V_{UVLO} < VDD < V_{HVLO}) is present on VDD1, VDD1 connects to OUTB. When VDD1 > V_{HVLO} and a valid VDD is present on VDD2, the TPS22986 will connect OUTB to VDD2. Note, OUTB is also opened and closed by other digital inputs, ENB and RXH, depending on the mode of the TPS22986. See the Normal Mode and Control Mode sections for more information on the control of OUTB. VDD1 will always take priority over VDD2. VDD2 will only be connected to OUTB when VDD1 > V_{HVLO}. When OUTB is connected to VDD2 and VDD1 drops below V_{HVLO}, the TPS22986 will disconnect OUTB from VDD2 and connect it to VDD1. Note, VDD1 and VDD2 may power up in any order. Figure 3 shows a flow diagram illustrating the selection of VDD1 or VDD2 as the appropriate supply to connect to OUTB. Note, this diagram shows only the dependence on the VDD values and does not show the enabling and disabling of OUTB by the ENB and RXH input signals.

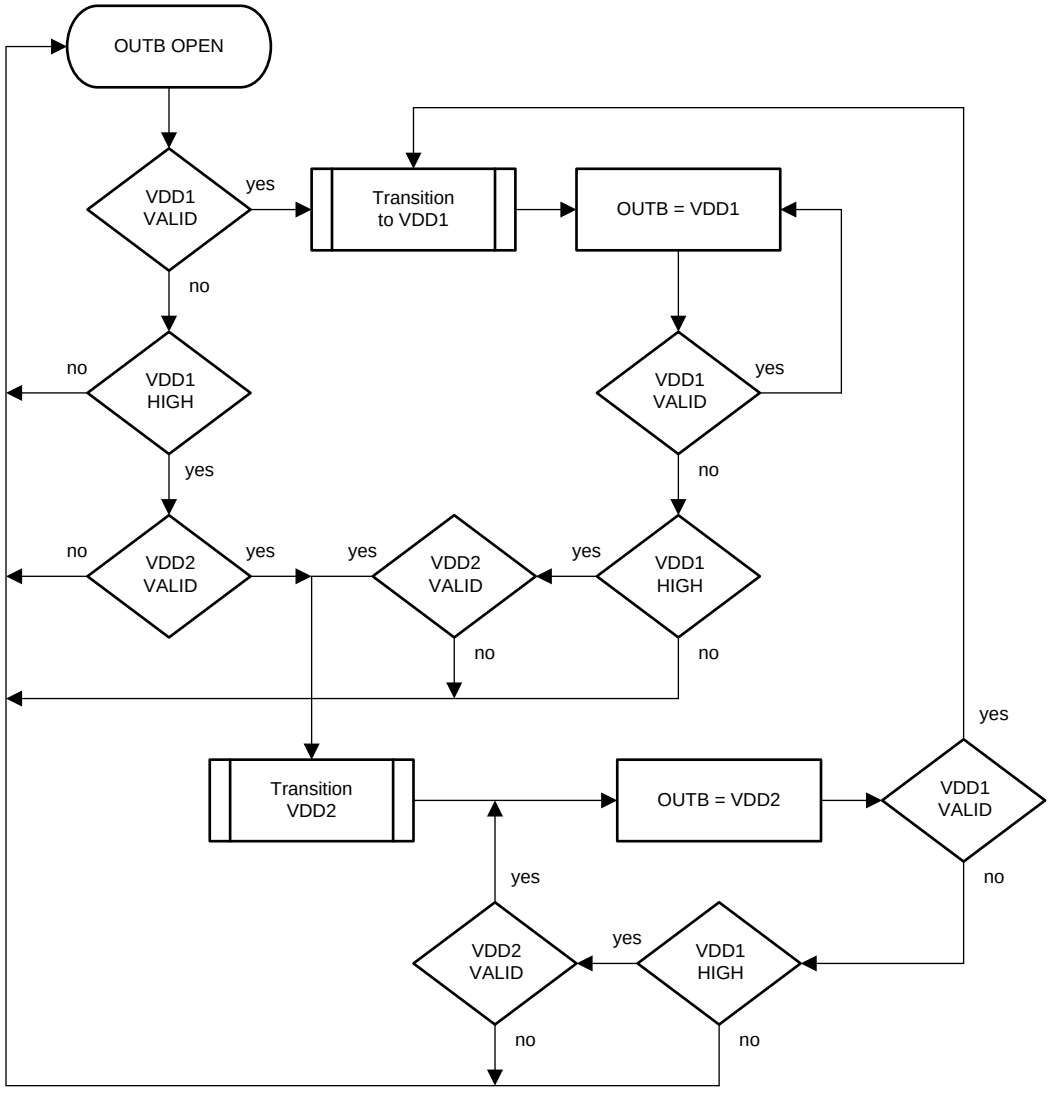


Figure 3. OUTB Supply Selection

Valid VDD at Inputs

A valid VDD on either input occurs when the voltage on VDD1 or VDD2 is between V_{UVLO} and V_{HVLO} (V_{UVLO} < VDD < V_{HVLO}). The VDD voltage is invalid when outside of this range. A VDD is considered high when VDD > V_{HVLO}. Table 1 shows the relationship between the output voltages and the input voltages. Note, other factors also determine whether OUTA and OUTB are open. Table 1 only shows the relationship to the voltage at the inputs VDD1 and VDD2.

Table 1. Output Voltages vs Input Voltages

VDD1	VDD2	OUTA	OUTB
Invalid	Invalid	Open	Open
Valid	Valid or Invalid	VDD1	VDD1
Invalid	Valid	VDD2	Open
High	Valid	VDD2	VDD2

Mode Selection

The TPS22986 has two modes of operation, Normal and Control. Refer to the Normal Mode and Control Mode sections for the operational description of each mode. At power-up, the TPS22986 determines which mode the device will operate in. At power-up, the resistance $R_{PUCFGOE}$ is switched to the CFG/OE pin. The external resistance connected to the pin determines the mode.

To enter Normal Mode, leave this pin floating or ensure that any external pull-down resistance on this pin is equal to or greater than $R_{PDNORMAL}$. When the UART buffers/level-shifters are used in this mode, the CFG/OE pin will also be the output enable for the TXH output. The $R_{PDNORMAL}$ resistance is recommended in series with the driver of the CFG/OE pin to prevent this driver from loading CFG/OE during power-up.

To enter Control Mode, the CFG/OE pin must be pulled low during power-up. Connect a resistance less than or equal to $R_{PDCONTROL}$ between CFG/OE and ground that will pull the pin low during power-up. Again, the CFG/OE pin is the output enable for the TXH output. The $R_{PDCONTROL}$ resistance should be chosen such that the device driving CFG/OE can overdrive this resistance.

Normal Mode

When the CFG/OE pin is floating or pulled high at power-up, the device enters Normal Mode. In Normal Mode, the TPS22986 provides power through OUTA and OUTB. OUTA is connected whenever a valid VDD is present on either VDD1 or VDD2. OUTB is connected whenever a valid VDD is present on VDD1 or VDD1 > V_{HVLO} and VDD2 is a valid VDD, and the GPIO control signal ENB is high. If a valid VDD is not present, the TPS22986 enters into a shutdown mode and blocks current flow through the switches.

After the device is latched into Normal Mode, the CFG/OE pin becomes the output enable for the TX buffer/level-shifter. See the UART RX and TX section for more information.

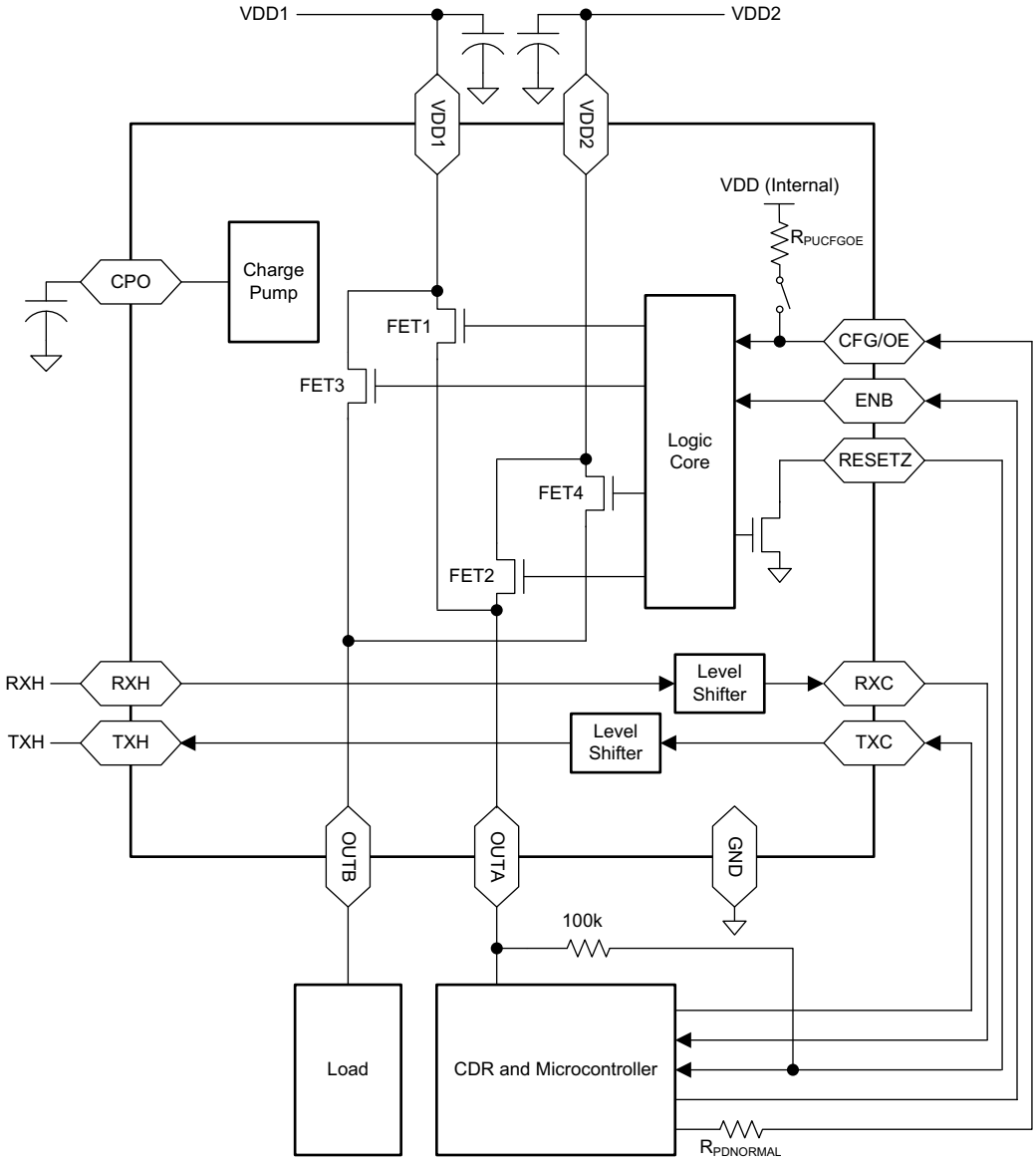


Figure 4. Normal Mode Typical Application

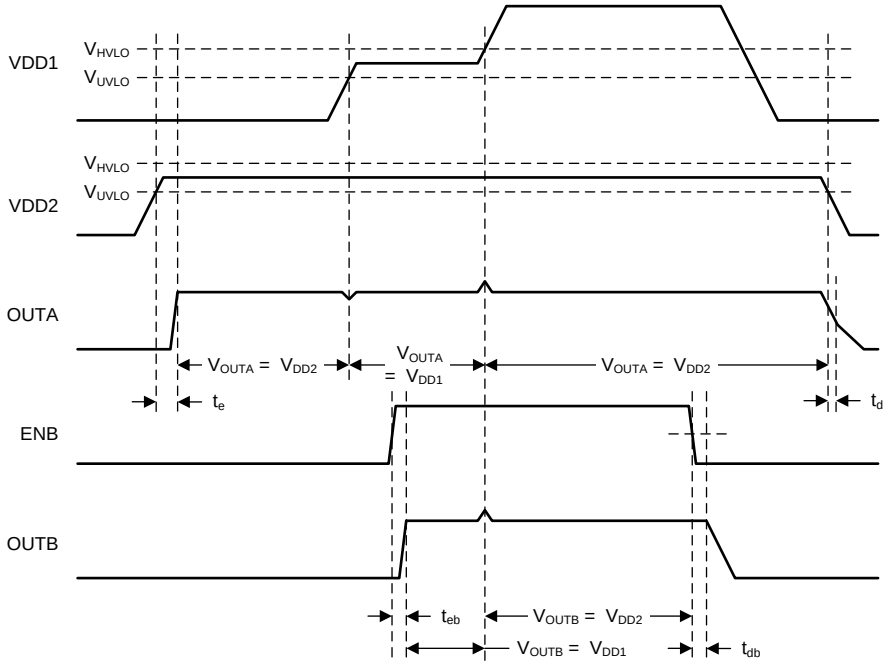


Figure 5. Timing During Normal Mode

Control Mode

When CFG/OE is grounded at power-up, the device latches into Control Mode. When a valid VDD connected, OUTA and OUTB are connected to the VDD. Note, a valid VDD is different for OUTA than OUTB. See Table 1 for the output voltages versus input conditions. OUTB remains connected to VDD until ENB transitions high. OUTA remains connected to VDD as long as a valid VDD exists. RESETZ indicates that a valid VDD is available at OUTB. When RESETZ is low, OUTB is high-impedance or is transitioning from high-impedance to an on-state. During power-up, when a valid supply becomes available, RESETZ remains asserted low for the time t_{U2R} to allow settling of ENB. ENB is masked during this interval until RESETZ is high. When RESETZ is high, a valid VDD is available at OUTB and ENB is monitored.

When either VDD is not in UVLO for more than t_{U2R}, the device monitors ENB for a high transition. When ENB transitions high, RESETZ will assert low after time t_{E2R}, and OUTB will open after time t_{E2O}. After the time t_{E2O}, the TPS22986 starts monitoring RXH for a falling edge. When a falling RXH is detected, OUTB is connected to the valid VDD after time t_{RX2O} and RESETZ transitions from low to high after time t_{RX2R}. The device then begins to monitor ENB again for a low to high transition. When a valid VDD is not available, RESETZ is asserted low and the TPS22986 blocks current flow through the switches. When both VDDs are in UVLO, the device clears any wait state and does not monitor ENB or RXH.

After the device is latched into Control Mode, the CFG/OE pin becomes the output enable for the TX buffer/level-shifter. See the UART RX and TX section for more information.

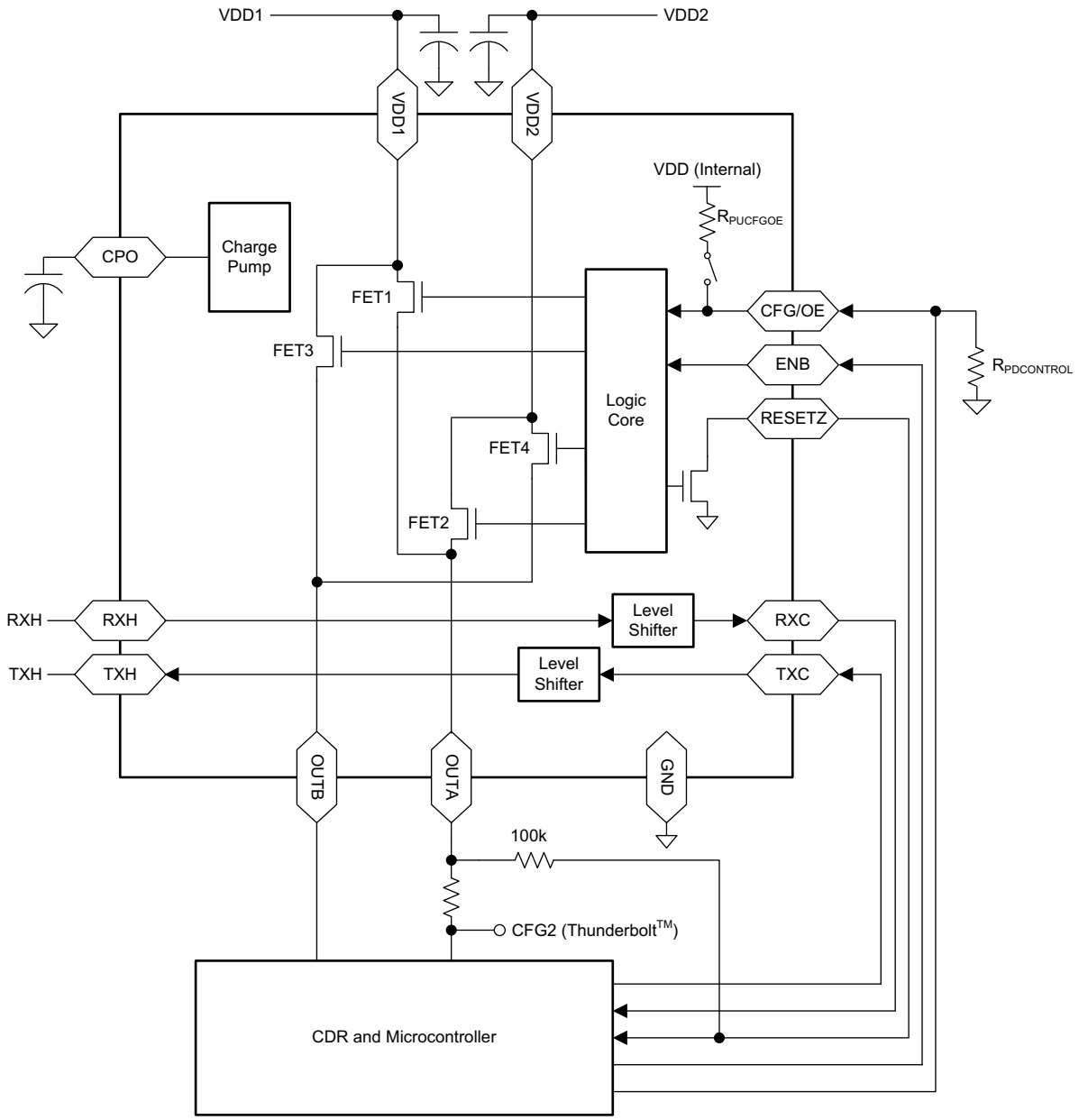


Figure 6. Control Mode Typical Application

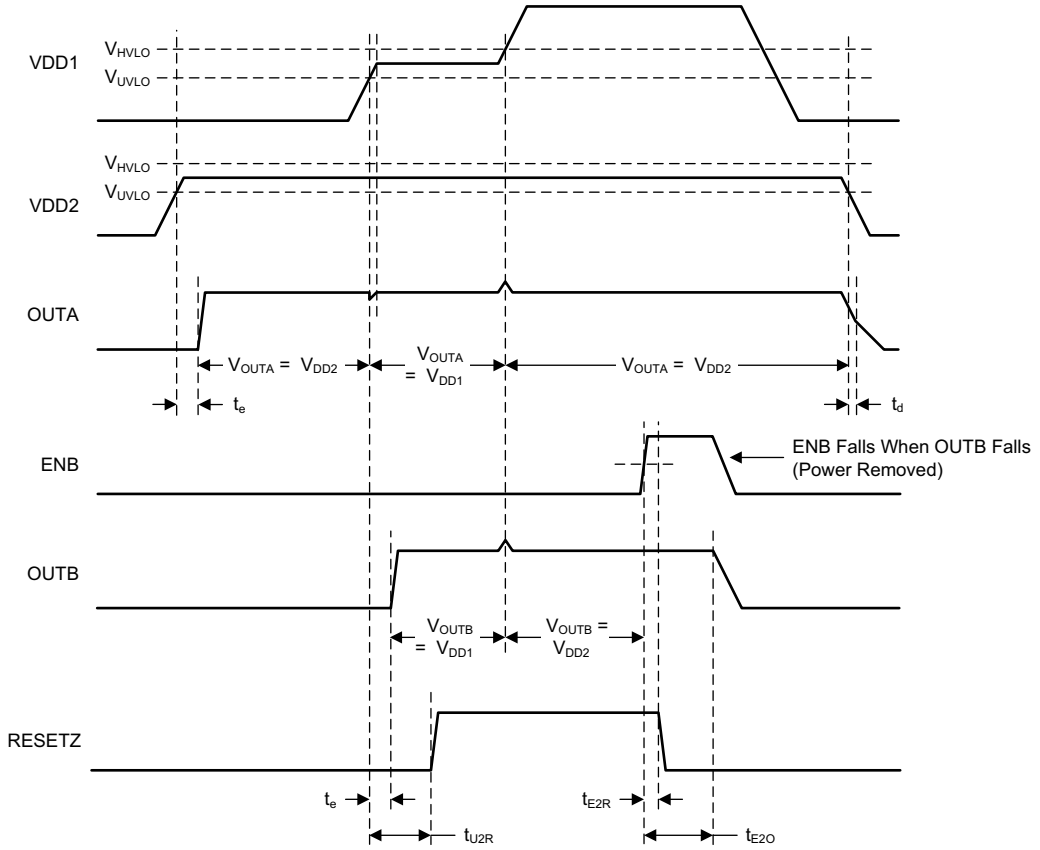


Figure 7. Timing During Control Mode

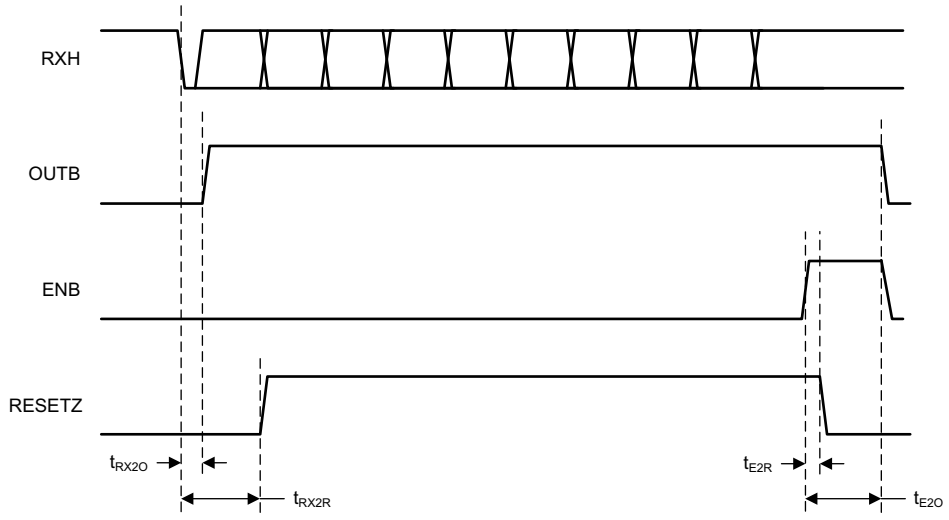


Figure 8. Timing During Control Mode Continued

Typical Startup

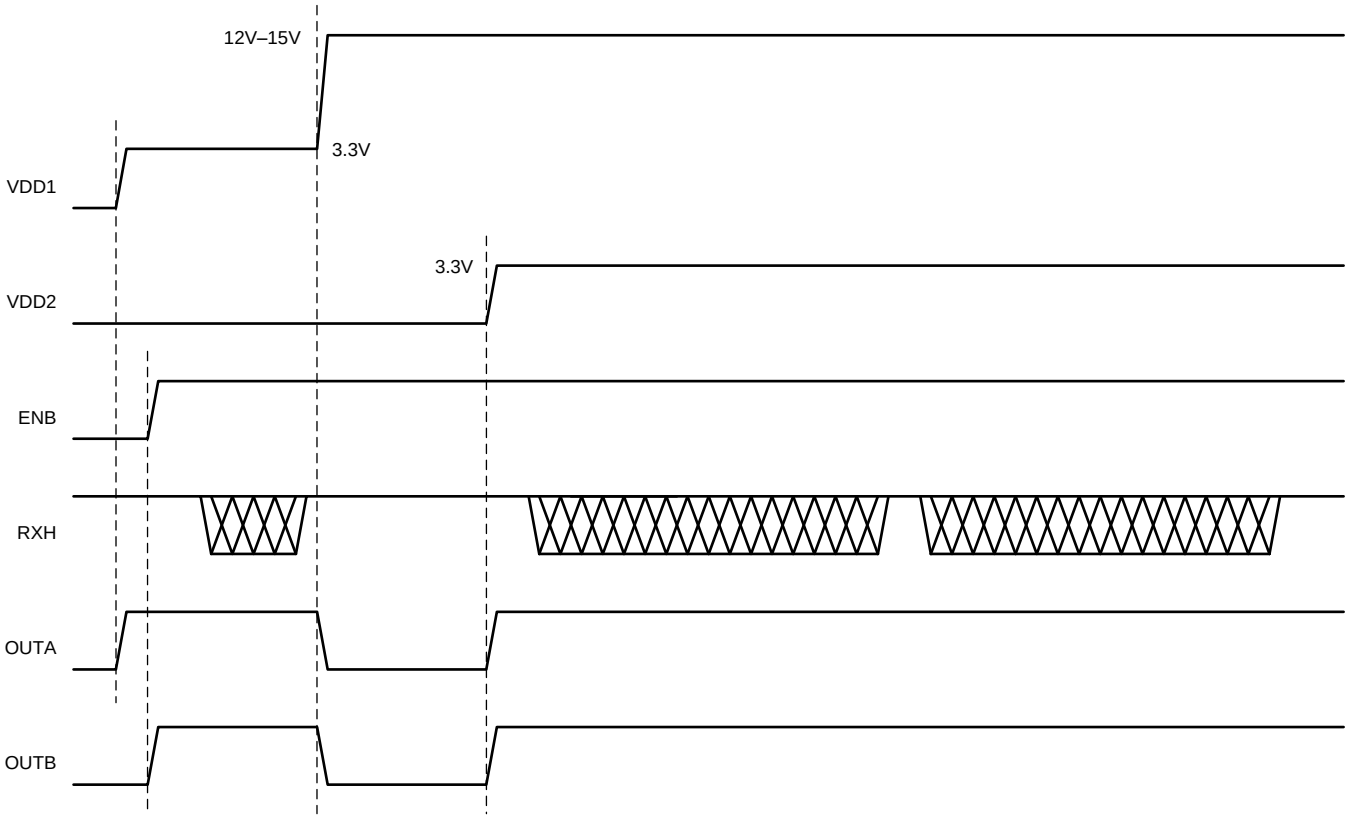


Figure 9. Typical Startup in Normal Mode

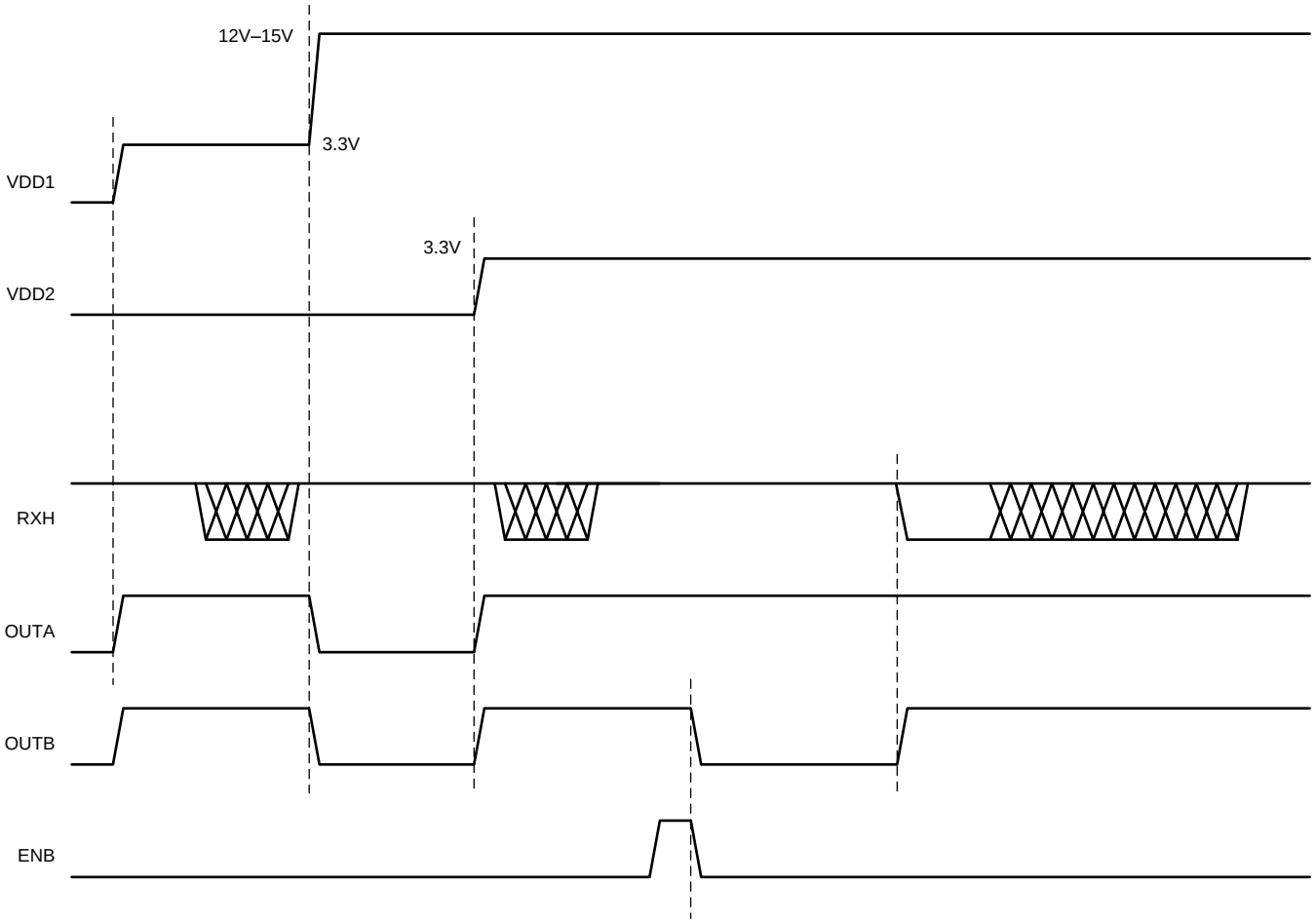


Figure 10. Typical Startup Timing for Control Mode

Soft Start

To prevent inrush current to the load, the TPS22986 soft starts OUTA and OUTB. When OUTA and OUTB are first enabled, the resistance of the FET switches (FET1, FET2, FET3, and FET4) starts high and reduces every 250µs in four steps. Figure 11 shows the nominal resistance ramp profile for OUTB. Figure 12 shows the flow diagram of the transition of the outputs.

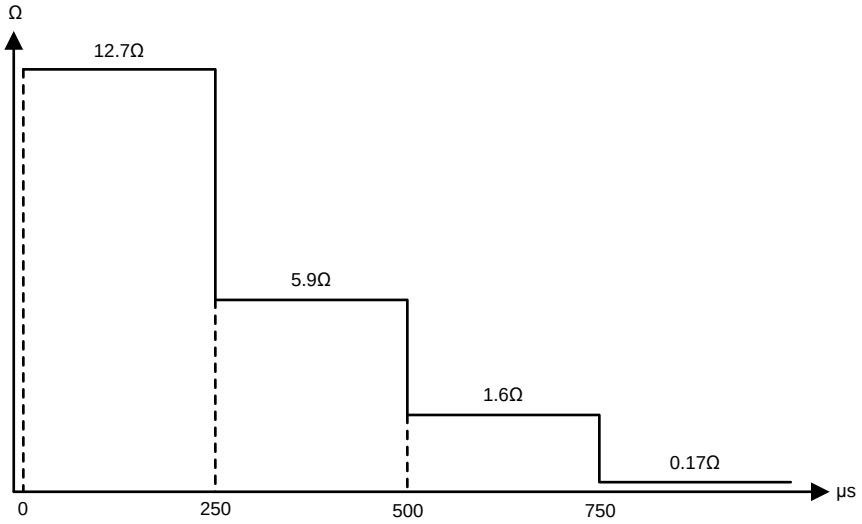


Figure 11. OUTB Soft Start Resistance vs Time profile (FET3 and FET4 resistance)

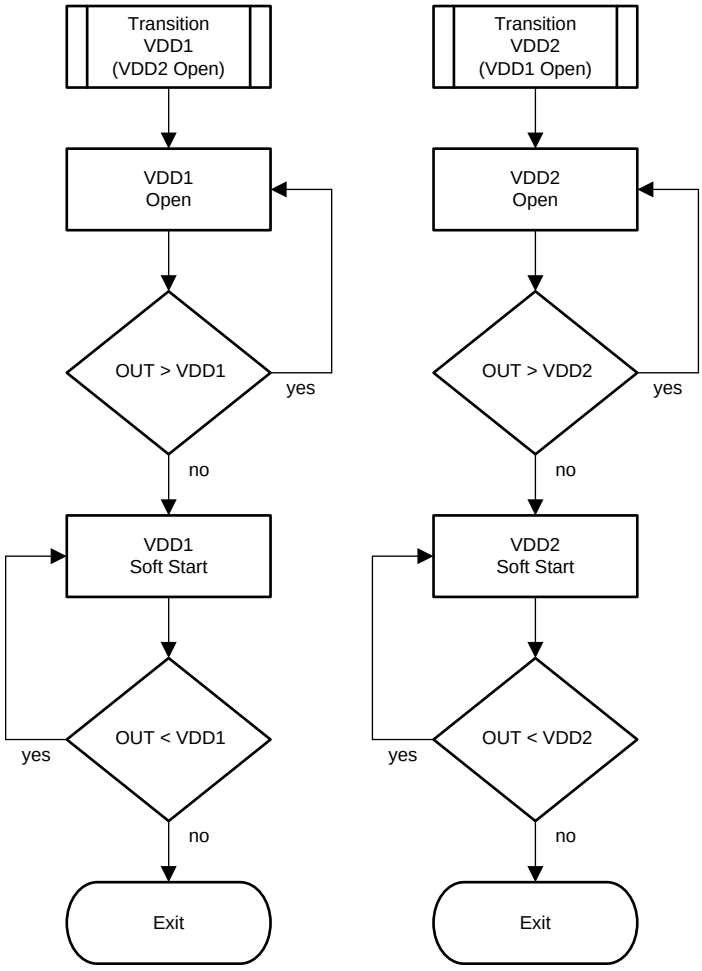


Figure 12. Transition of OUTA and OUTB to VDD1 or VDD2

Supply Switch-Over During HVLO

When OUTA and OUTB are connected to VDD1 and VDD1 crosses V_{HVLO}, the TPS22986 opens the FET1/3 switches. Due to the delay t_{dh}, the output will overshoot V_{HVLO} by V_{OS}. When a valid VDD is present on VDD2, OUTA and OUTB will connect to VDD2 after time t_{eh}. Figure 13 illustrates this switch-over event.

The overshoot V_{OS} will occur when the VDD (VDD1 or VDD2) that is connected to the output transitions above V_{HVLO}. V_{OS} is set by the delay t_{dh} and the slew rate of the connected VDD.

The following equation determines the overshoot V_{OS}.

Equation 1: $V_{OS} = SR_{VDD} \times t_{dh}$

SR_{VDD} is the slew rate of the supply that is transitioning above V_{HVLO}. As an example, when SR_{VDD} is 10mV/µs and t_{dh} is 20µs, V_{OS} is 200mV.

When switching to VDD2 due to an HVLO event on VDD1, the outputs OUTA and OUTB are discharged by their respective loads until they reach the VDD2 voltage. This prevents in-rush current when charging the output caps. The discharge time t_{eh} is variable and is determined by the following equation.

Equation 2: $t_{eh} = t_{dh} + (V_{HVLO} + V_{OS} - V_{DD2}) \times C_{LOAD}/I_{LOAD}$

In this equation, V_{OS} is determined by Equation 1, C_{LOAD} is the load capacitance at the respective output, and I_{LOAD} is the load current flowing out of the same output. As an example, when V_{DD2} is 3.3V, t_{dh} is 20µs, V_{OS} is 200mV, C_{LOAD} is 4µF, and I_{LOAD} is 350mA, the resulting t_{eh} is 25.7 µs.

Note, when VDD1 transitions above V_{HVLO} and a valid VDD is not present on VDD2, the outputs will open and will discharge through each respective load.

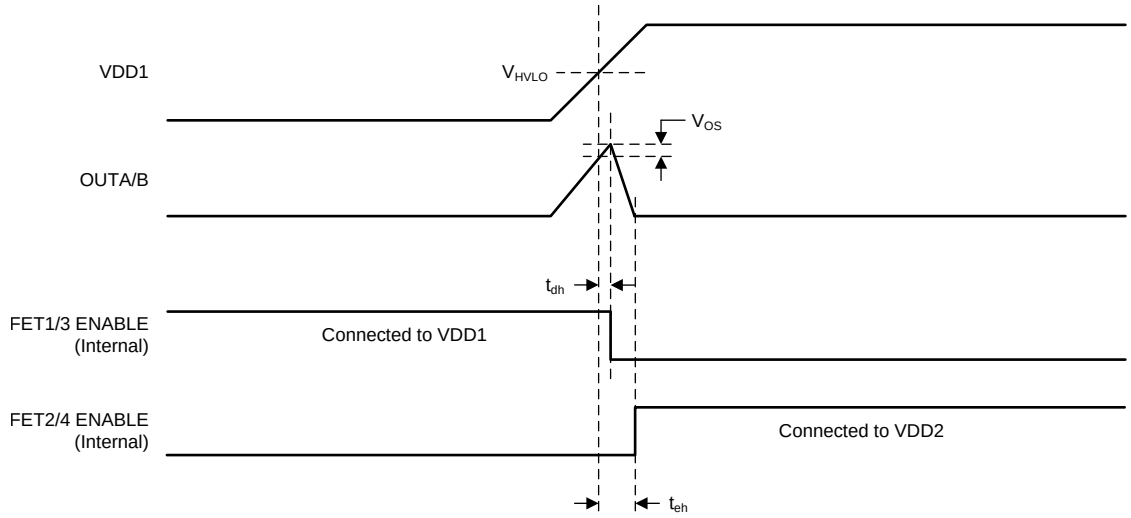


Figure 13. VDD Switch-over at VDD1 Rising Above V_{HVLO}

When VDD1 drops from a HVLO condition, the TPS22986 may brownout at OUTA and OUTB before switching the outputs to VDD1.

UART RX and TX

The TPS22986 provides failsafe buffers for digital UART RX and TX lines. The failsafe mechanism prevents the RX and TX lines from being loaded when power is removed from the device. The RX line is divided into a host side RXH input and a cable side RXC output. The TX line is divided into host side TXH output and a cable side TXC input. The inputs RXH and TXC have a weak pull-down resistance R_{PDUART} to allow each to be left floating if unused in the application.

When the TPS22986 is unpowered or when RESETZ is asserted low, the TXH output is high impedance. This prevents loading the system TX line and allowing other devices on the UART bus to communicate.

Figure 14 illustrates the TXH control. When RESETZ is high, CFG/OE controls TXH. When CFG/OE is low, TXH is high impedance. When CFG/OE is high, TXH is a buffered/level-shifted TXC. The CFG/OE input is ignored when RESETZ is asserted low. Figure 15 shows the delay from CFG/OE to TXH.

Note, the UART buffers are powered from OUTA. When OUTA is disconnected, the UART buffers are unpowered. When there are no valid supplies connected or when the device is in Thermal Shutdown, OUTA will disconnect and the buffers will be unpowered.

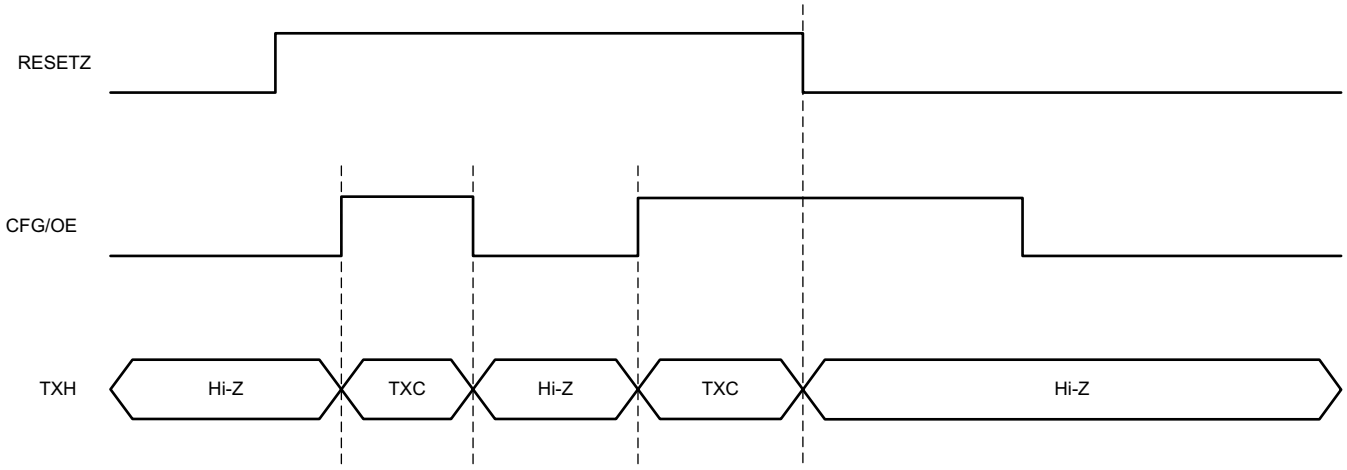


Figure 14. UART RX and TX Buffer Control

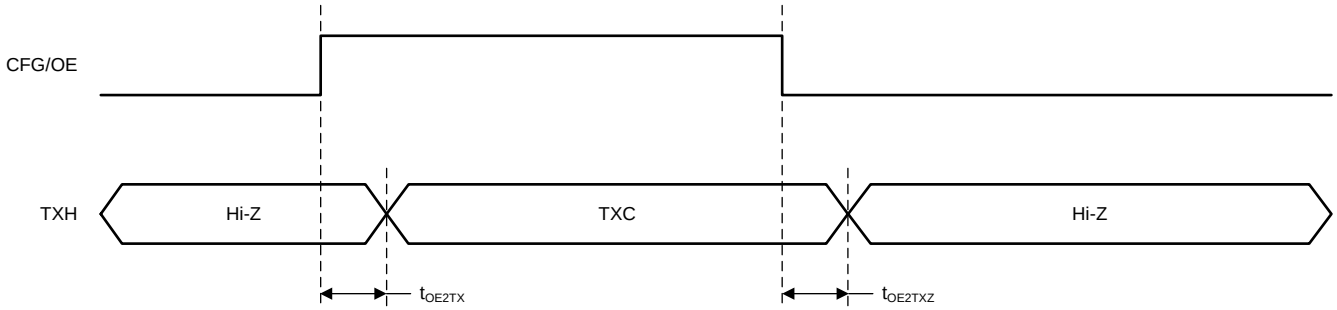


Figure 15. CFG/OE to TXH Timing

Thunderbolt System with TPS22981/TPS22986

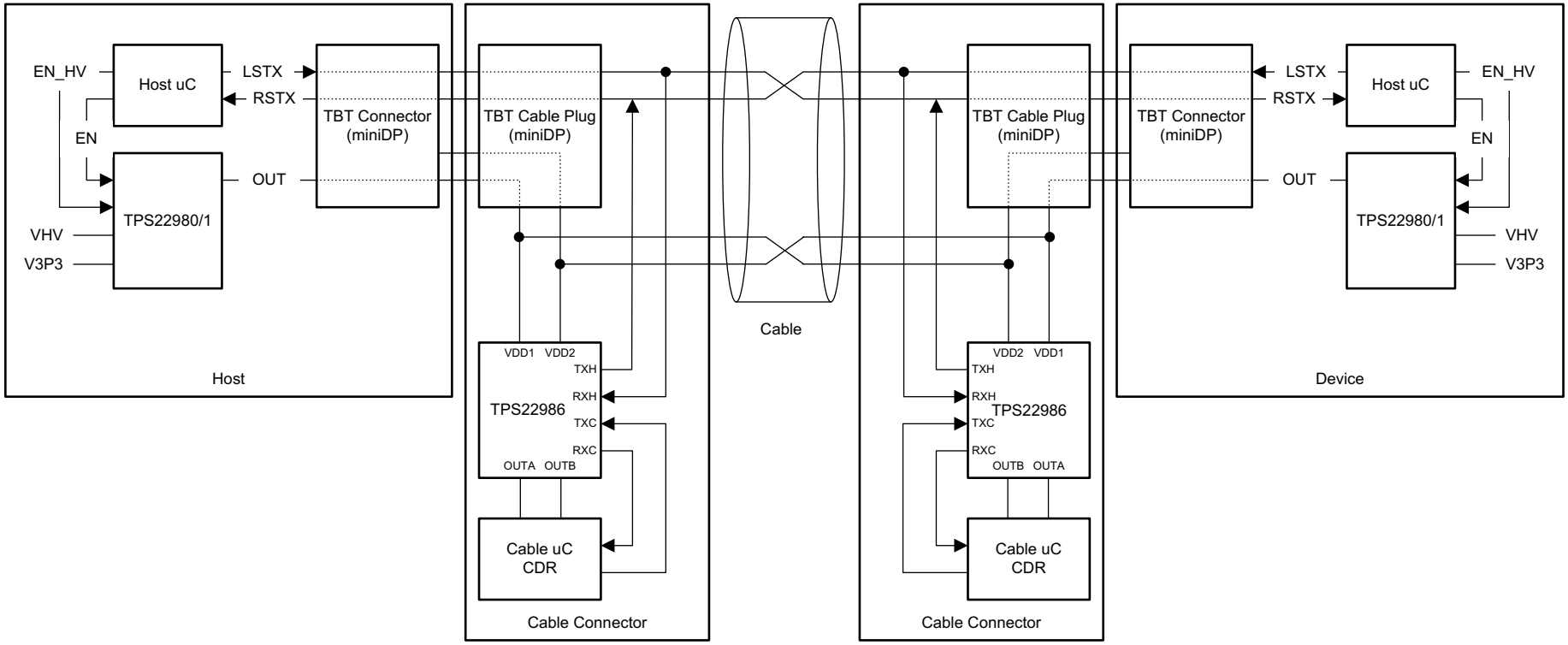


Figure 16. Thunderbolt System with TPS22981/TPS22986

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS22986YFPR	Active	Production	DSBGA (YFP) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DJ
TPS22986YFPR.A	Active	Production	DSBGA (YFP) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DJ
TPS22986YFPR.B	Active	Production	DSBGA (YFP) | 16	3000 | LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	DJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

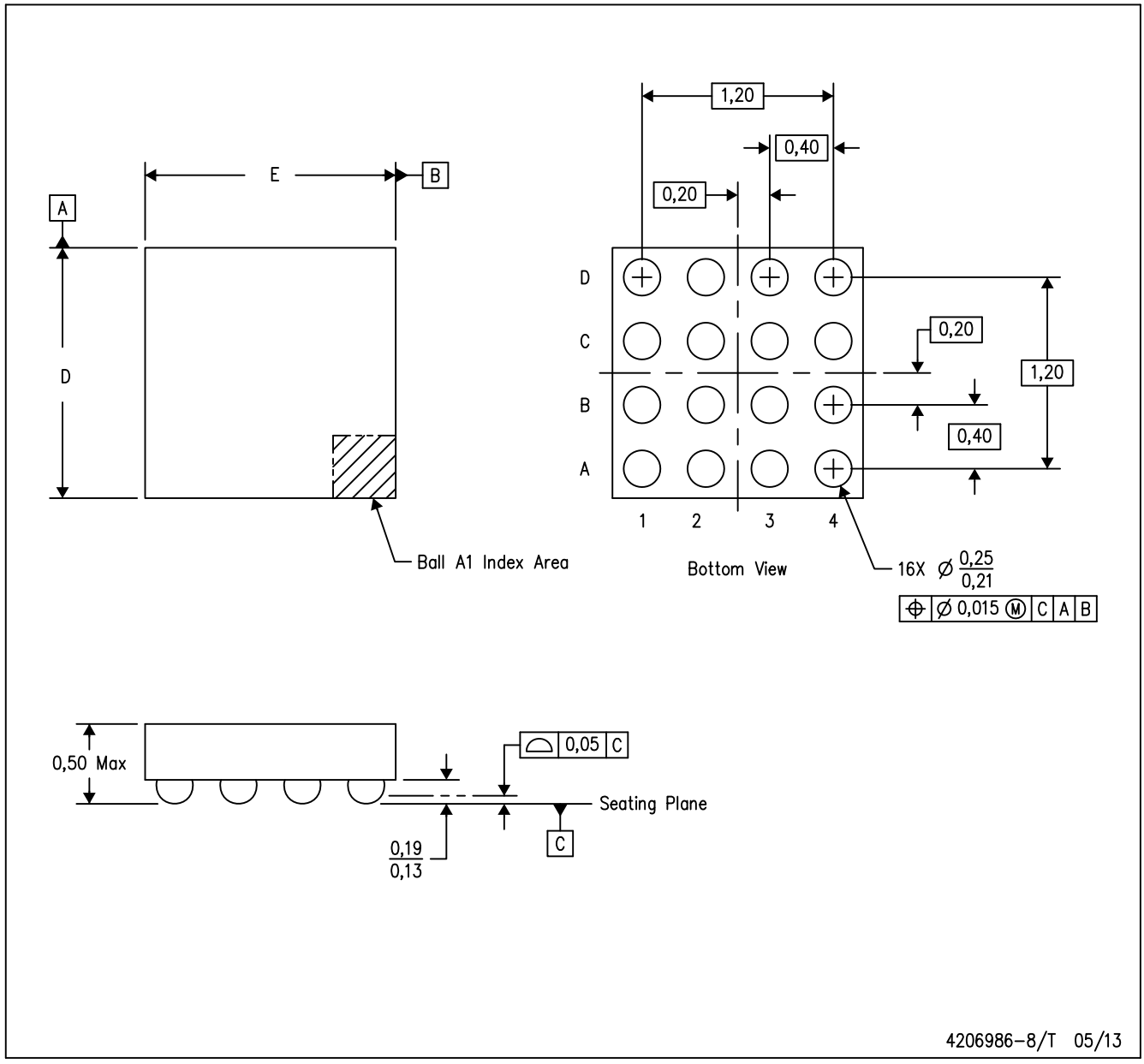
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

YFP (S–XBGA–N16) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments

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最后更新日期：2025 年 10 月