

TPS22968 双通道、超低电阻负载开关

1 特性

- 集成式双通道负载开关
- 输入电压范围：0.8V 至 5.5V
- VBIAS 电压范围：2.5V 至 5.5V
 - 非常适合 1S 电池配置
- 超低 R_{ON} 电阻
 - V_{IN} = 5V (V_{BIAS} = 5V) 时, R_{ON} = 27mΩ
 - V_{IN} = 3.3V (V_{BIAS} = 5V) 时, R_{ON} = 25mΩ
 - V_{IN} = 1.8V (V_{BIAS} = 5V) 时, R_{ON} = 25mΩ
- 每通道最大 4A 持续开关电流
- 低静态电流
 - V_{BIAS} = 5V 时为 55μA (两个通道)
 - V_{BIAS} = 5V 时为 55μA (单通道)
- 低控制输入阈值支持使用 1.2V、1.8V、2.5V、3.3V 逻辑
- 可配置上升时间⁽¹⁾
- 快速输出放电 (QOD)⁽²⁾ (可选)
- 带有散热垫的 SON 14 引脚封装
- ESD 性能经测试符合 JEDEC 标准
 - 2kV 人体放电模式 (HBM) 和 1kV 器件充电模型 (CDM)
- 闩锁性能超出 100mA, 符合 JESD 78 II 类规范的要求
- 通用输入输出 (GPIO) 使能 - 高电平有效
- TPS22968N: 仅限产品预览

(1) 有关 CT 值与上升时间之间的关系, 请参阅 [申请资料](#) 部分

(2) 此特性通过一个 270Ω 电阻器将开关的输出放电至接地 (GND), 从而防止输出悬空。

2 应用

- Ultrabook™
- 笔记本电脑和上网本
- 平板电脑
- 消费类电子产品
- 机顶盒
- 电信系统

3 说明

TPS22968x 是一款具有受控接通功能的小型、超低 R_{ON} 双通道负载开关。此器件包含两个可在 0.8 至 5.5V 输入电压范围内运行的 N 沟道 MOSFET, 并且每个沟道可支持最大

4A 的持续电流。每个开关由一个导通/关断输入 (ON1 和 ON2) 单独控制, 此输入可与低电压控制信号直接连接。为了能够在开关关闭时快速进行输出放电, TPS22968 中添加了一个 270Ω 的片上负载电阻器。

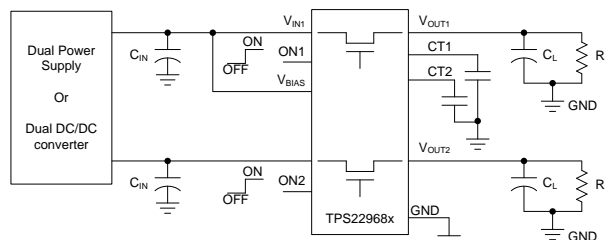
TPS22968x 采用小型、节省空间的封装 (DPU), 该封装具有集成式散热垫, 从而支持高功率耗散。该器件在自然通风环境下的额定运行温度范围为 -40 至 +105°C。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS22968 TPS22968N	WSON (14)	3.00mm x 2.00mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

典型应用电路原理图



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4 修订历史记录

Changes from Revision D (March 2016) to Revision E	Page
• 将 QOD 说明从 (仅限 TPS22968) 更改成了 (可选) (在特性部分中)	1

Changes from Revision E (July 2016) to Revision F	Page
• 已更改 Functional Block Diagram	1

Changes from Revision C (October 2015) to Revision D	Page
• Made Changes to Thermal Considerations	22

Changes from Revision B (June 2015) to Revision C	Page
• 更新了 TPS22968N 发行版的信息。	1
• Updated “TEST CONDITIONS” for RON.	6
• Updated “TEST CONDITIONS” for RON.	7

Changes from Revision A (July 2014) to Revision B	Page
• Updated Typical Characteristics graphs.	8

Changes from Original (January 2014) to Revision A	Page
• 已添加 添加了处理额定值表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	1

5 Device Comparison

DEVICE	Ron (typ) at VIN = 3.3 V, VBIAS = 5 V	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22968	25 mΩ	Yes	4 A	Active High
TPS22968N	25 mΩ	No	4 A	Active High

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN1	I	Switch 1 input. Bypass this input with a ceramic capacitor to GND
2			
3	ON1	I	Active-high switch 1 control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.5 V. See the VIN and VBIAS Voltage Range section
5	ON2	I	Active-high switch 2 control input. Do not leave floating
6	VIN2	I	Switch 2 input. Bypass this input with a ceramic capacitor to GND
7			
8	VOUT2	O	Switch 2 output
9			
10	CT2	O	Switch 2 slew rate control. Can be left floating
11	GND	—	Ground
12	CT1	O	Switch 1 slew rate control. Can be left floating
13	VOUT1	O	Switch 2 output
14			
15	Thermal Pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the Application Information section for layout guidelines

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT ⁽²⁾
V _{IN1,2}	Input voltage	-0.3	6	V
V _{BIAS}	Bias voltage	-0.3	6	V
V _{OUT1,2}	Output voltage	-0.3	6	V
V _{ON1,2}	ON voltage	-0.3	6	V
I _{MAX}	Maximum continuous switch current per channel, T _A = 30 °C		4	A
I _{PLS}	Maximum pulsed switch current, pulse < 300 μs, 2% duty cycle		6	A
T _J	Maximum junction temperature		125	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{IN1,2}	Input voltage		0.8	V _{BIAS}	V
V _{BIAS}	Bias voltage		2.5	5.5	V
V _{ON1,2}	ON voltage		0	5.5	V
V _{OUT1,2}	Output voltage			V _{IN}	V
V _{IH, ON1,2}	High-level input voltage, ON1,2	V _{BIAS} = 2.5 V to 5.5 V	1.2	5.5	V
V _{IL, ON1,2}	Low-level input voltage, ON1,2	V _{BIAS} = 2.5 V to 5.5 V	0	0.5	V
C _{IN1,2}	Input capacitor		1 ⁽¹⁾		μF
T _A	Operating free-air temperature ⁽²⁾		-40	105	°C

- (1) See the [Application Information](#) section.
- (2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T_{A(max)}] is dependent on the maximum operating junction temperature [T_{J(max)}], the maximum power dissipation of the device in the application [P_{D(max)}], and the junction-to-ambient thermal resistance of the part/package in the application (R_{θJA}), as given by the following equation: T_{A(max)} = T_{J(max)} - (R_{θJA} × P_{D(max)}).

7.4 Thermal Information

	THERMAL METRIC ⁽¹⁾ (2)	TPS22968	UNIT
		DPU (WSON)	
		14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	62.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	70.2	°C/W
R _{θJB}	Junction-to-board thermal resistance	23.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2.5	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) For thermal estimates of this device based on PCB copper area, see the [TI PCB Thermal Calculator](#).

Thermal Information (continued)

THERMAL METRIC ⁽¹⁾ ⁽²⁾		TPS22968	UNIT
		DPU (WSON)	
		14 PINS	
ψ_{JB}	Junction-to-board characterization parameter	23.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9	°C/W

7.5 Electrical Characteristics ($V_{BIAS} = 5\text{ V}$)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40^{\circ}\text{C} \leq T_A \leq +105^{\circ}\text{C}$ (full) and $V_{BIAS} = 5\text{ V}$. Typical values are for $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT			
POWER SUPPLIES AND CURRENTS										
I_Q, V_{BIAS}	V_{BIAS} quiescent current (both channels)	$I_{OUT1} = I_{OUT2} = 0, V_{IN1,2} = V_{ON1,2} = V_{BIAS} = 5\text{ V}$	-40°C to $+105^{\circ}\text{C}$	55	70		μA			
	V_{BIAS} quiescent current (single channel)	$I_{OUT1} = I_{OUT2} = 0, V_{ON2} = 0\text{ V}, V_{IN1,2} = V_{ON1} = V_{BIAS} = 5\text{ V}$	-40°C to $+105^{\circ}\text{C}$	55	68		μA			
I_{SD}, V_{BIAS}	V_{BIAS} shutdown current	$V_{ON1,2} = 0\text{ V}, V_{OUT1,2} = 0\text{ V}$	-40°C to $+105^{\circ}\text{C}$	1	2		μA			
$I_{SD}, V_{IN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2} = 0\text{ V}, V_{OUT1,2} = 0\text{ V}$	$V_{IN1,2} = 5\text{ V}$	-40°C to $+85^{\circ}\text{C}$	0.5	8	μA			
				-40°C to $+105^{\circ}\text{C}$		10				
			$V_{IN1,2} = 3.3\text{ V}$	-40°C to $+85^{\circ}\text{C}$	0.1	3				
				-40°C to $+105^{\circ}\text{C}$		4				
			$V_{IN1,2} = 1.8\text{ V}$	-40°C to $+85^{\circ}\text{C}$	0.07	2				
				-40°C to $+105^{\circ}\text{C}$		3				
			$V_{IN1,2} = 1.2\text{ V}$	-40°C to $+85^{\circ}\text{C}$	0.05	1				
				-40°C to $+105^{\circ}\text{C}$		2				
$I_{ON1,2}$	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	-40°C to $+105^{\circ}\text{C}$		0.1		μA			
RESISTANCE CHARACTERISTICS										
R_{ON}	On-state resistance	$I_{OUT} = -200\text{ mA}, V_{BIAS} = 5\text{ V}, V_{ON1,2} = 5\text{ V}$	$V_{IN} = 5\text{ V}$	25°C	27	36	$\text{m}\Omega$			
				-40°C to $+85^{\circ}\text{C}$		40				
				-40°C to $+105^{\circ}\text{C}$		42				
			$V_{IN} = 3.3\text{ V}$	25°C	25	34	$\text{m}\Omega$			
				-40°C to $+85^{\circ}\text{C}$		38				
				-40°C to $+105^{\circ}\text{C}$		40				
			$V_{IN} = 1.8\text{ V}$	25°C	25	34	$\text{m}\Omega$			
				-40°C to $+85^{\circ}\text{C}$		38				
				-40°C to $+105^{\circ}\text{C}$		40				
			$V_{IN} = 1.5\text{ V}$	25°C	25	34	$\text{m}\Omega$			
				-40°C to $+85^{\circ}\text{C}$		38				
				-40°C to $+105^{\circ}\text{C}$		40				
			$V_{IN} = 1.2\text{ V}$	25°C	25	34	$\text{m}\Omega$			
				-40°C to $+85^{\circ}\text{C}$		38				
				-40°C to $+105^{\circ}\text{C}$		40				
			$V_{IN} = 0.8\text{ V}$	25°C	25	34	$\text{m}\Omega$			
				-40°C to $+85^{\circ}\text{C}$		38				
				-40°C to $+105^{\circ}\text{C}$		40				
			$R_{PD}^{(1)}$	Output pulldown resistance	$V_{IN} = 5\text{ V}, V_{ON} = 0\text{ V}, I_{OUT} = 10\text{ mA}$	-40°C to $+105^{\circ}\text{C}$	270	320		Ω

(1) TPS22968 only.

7.6 Electrical Characteristics ($V_{BIAS} = 2.5\text{ V}$)

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature $-40\text{ }^{\circ}\text{C} \leq T_A \leq +105\text{ }^{\circ}\text{C}$ (full) and $V_{BIAS} = 2.5\text{ V}$. Typical values are for $T_A = 25\text{ }^{\circ}\text{C}$ (unless otherwise noted).

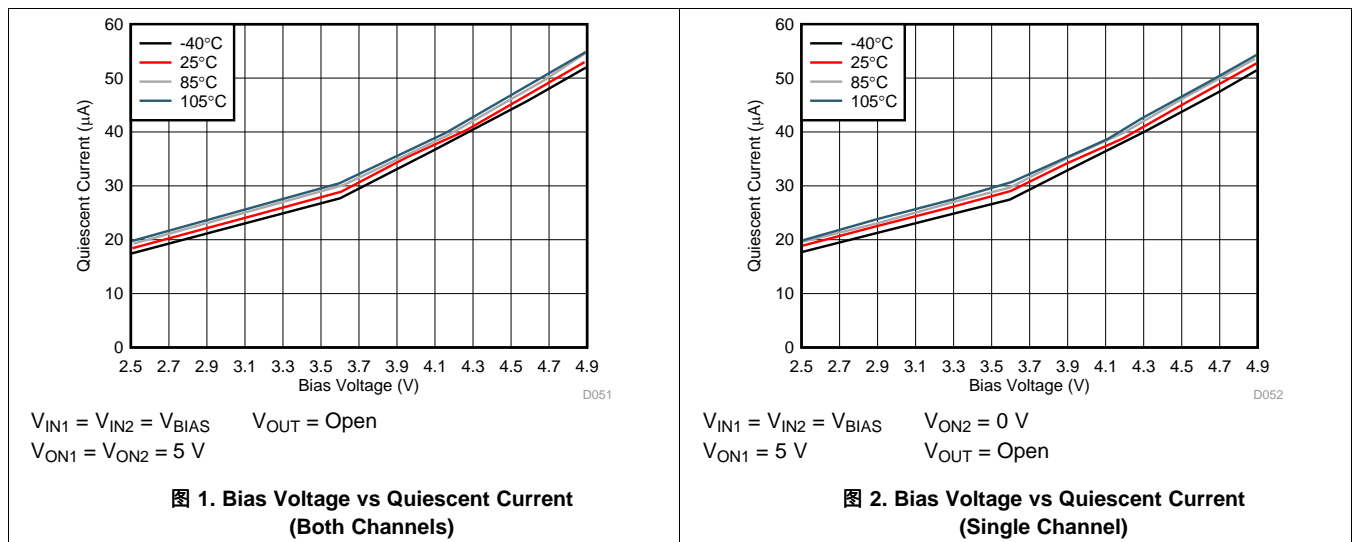
PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS							
I_Q, V_{BIAS}	V_{BIAS} quiescent current (both channels)	$I_{OUT1} = I_{OUT2} = 0, V_{IN1,2} = V_{ON1,2} = V_{BIAS} = 2.5\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$	18	27		μA
	V_{BIAS} quiescent current (single channel)	$I_{OUT1} = I_{OUT2} = 0, V_{ON2} = 0\text{ V}, V_{IN1,2} = V_{ON1} = V_{BIAS} = 2.5\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$	18	27		μA
I_{SD}, V_{BIAS}	V_{BIAS} shutdown current	$V_{ON1,2} = 0\text{ V}, V_{OUT1,2} = 0\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$	0.5	2		μA
$I_{SD}, V_{IN1,2}$	$V_{IN1,2}$ shutdown current (per channel)	$V_{ON1,2} = 0\text{ V}, V_{OUT1,2} = 0\text{ V}$	$V_{IN1,2} = 2.5\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	0.1	2	μA
				$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$		4	
			$V_{IN1,2} = 1.8\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	0.07	2	
				$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$		3	
			$V_{IN1,2} = 1.2\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$	0.05	1	
				$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$		2	
$I_{ON1,2}$	ON pin input leakage current	$V_{ON} = 5.5\text{ V}$	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$		0.1		μA
RESISTANCE CHARACTERISTICS							
R_{ON}	On-state resistance	$I_{OUT} = -200\text{ mA}, V_{BIAS} = 2.5\text{ V}, V_{ON1,2} = 5\text{ V}$	$V_{IN} = 2.5\text{ V}$	25 $^{\circ}\text{C}$	30	39	$\text{m}\Omega$
				$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$		44	
				$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$		46	
			$V_{IN} = 1.8\text{ V}$	25 $^{\circ}\text{C}$	28	36	$\text{m}\Omega$
				$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$		41	
				$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$		43	
			$V_{IN} = 1.5\text{ V}$	25 $^{\circ}\text{C}$	28	36	$\text{m}\Omega$
				$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$		41	
				$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$		43	
			$V_{IN} = 1.2\text{ V}$	25 $^{\circ}\text{C}$	27	36	$\text{m}\Omega$
				$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$		41	
				$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$		43	
$V_{IN} = 0.8\text{ V}$	25 $^{\circ}\text{C}$	26	35	$\text{m}\Omega$			
	$-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$		39				
	$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$		41				
$R_{PD}^{(1)}$	Output pulldown resistance	$V_{IN} = 2.5\text{ V}, V_{ON} = 0\text{ V}, I_{OUT} = 10\text{ mA}$	$-40\text{ }^{\circ}\text{C}$ to $+105\text{ }^{\circ}\text{C}$	270	320		Ω

(1) TPS22968 only.

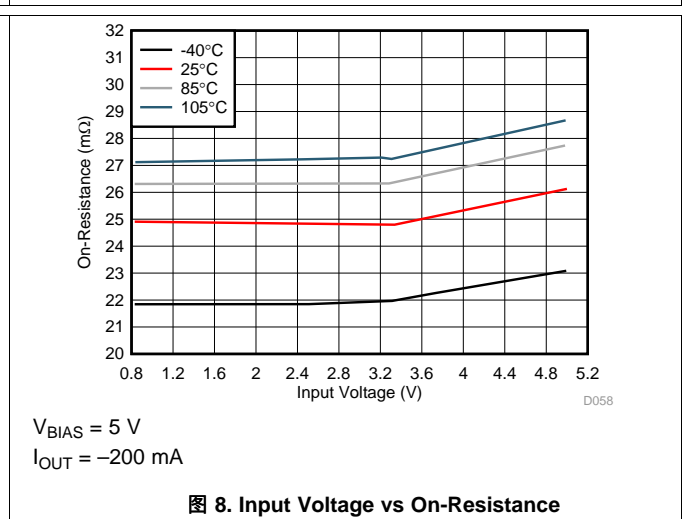
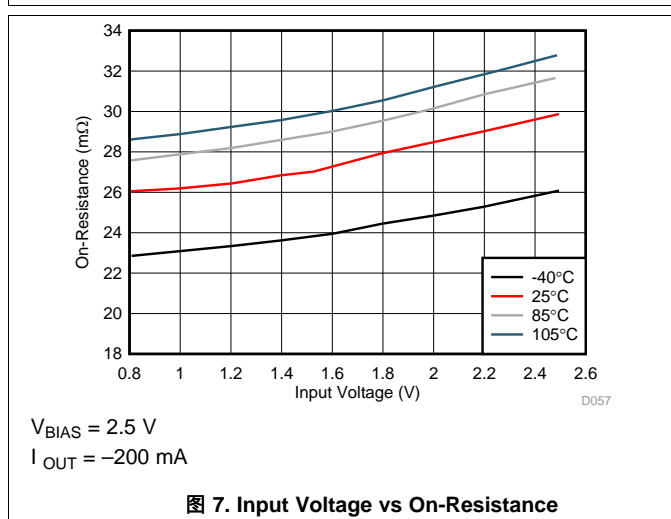
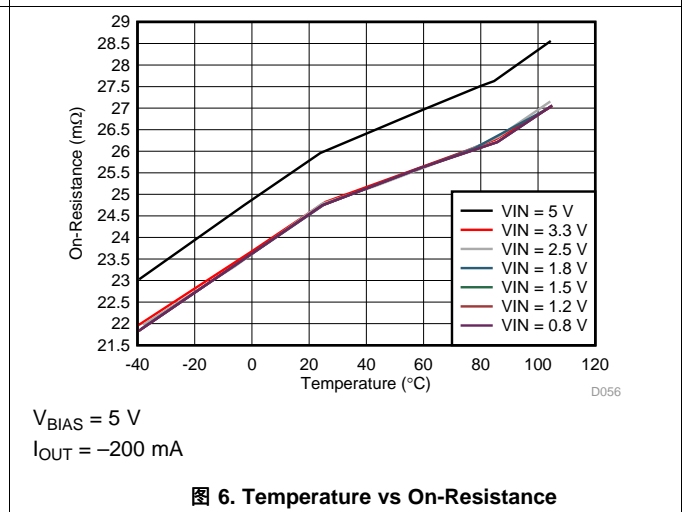
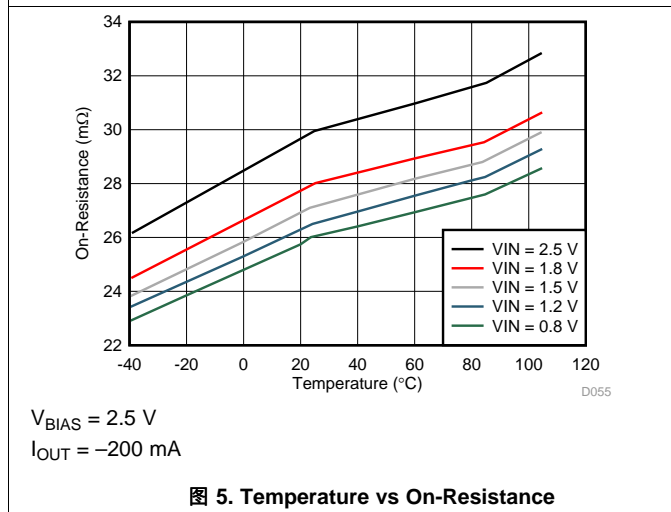
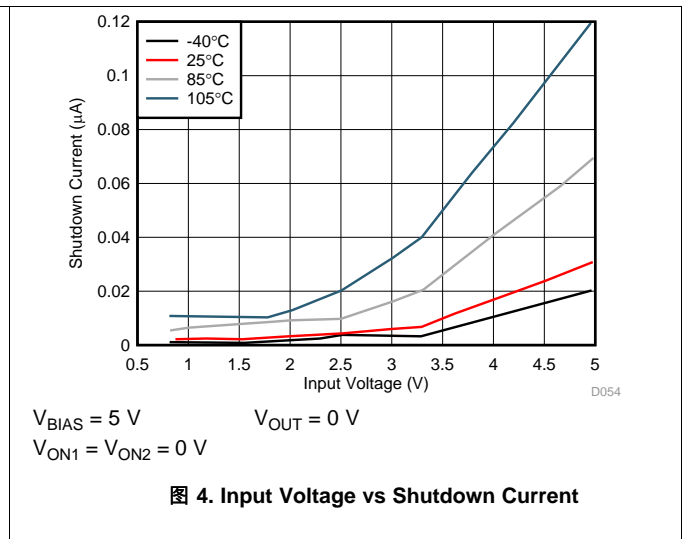
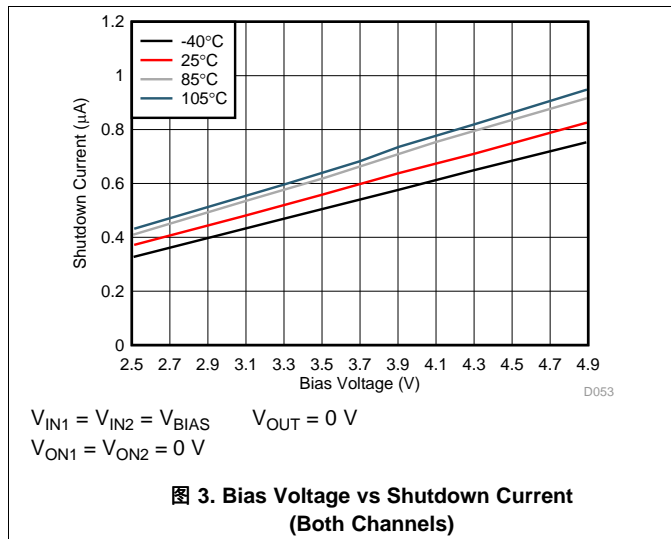
7.7 Switching Characteristics

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{IN} = V_{ON} = V_{BIAS} = 5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$ (unless otherwise noted)					
t_{ON} Turnon time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		1128		μs
t_{OFF} Turnoff time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		5		
t_R V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		1387		
t_F V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		2		
t_D ON delay time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		455		
$V_{IN} = 0.8\text{ V}$, $V_{ON} = V_{BIAS} = 5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$ (unless otherwise noted)					
t_{ON} Turnon time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		508		μs
t_{OFF} Turnoff time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		33		
t_R V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		273		
t_F V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		2		
t_D ON delay time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		377		
$V_{IN} = 2.5\text{ V}$, $V_{ON} = 5\text{ V}$, $V_{BIAS} = 2.5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$ (unless otherwise noted)					
t_{ON} Turnon time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		1718		μs
t_{OFF} Turnoff time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		7		
t_R V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		1701		
t_F V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		2		
t_D ON delay time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		859		
$V_{IN} = 0.8\text{ V}$, $V_{ON} = 5\text{ V}$, $V_{BIAS} = 2.5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$ (unless otherwise noted)					
t_{ON} Turnon time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		1117		μs
t_{OFF} Turnoff time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		30		
t_R V_{OUT} rise time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		651		
t_F V_{OUT} fall time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		2		
t_D ON delay time	$R_L = 10\ \Omega$, $C_L = 0.1\ \mu\text{F}$, $CT = 1000\ \text{pF}$		775		

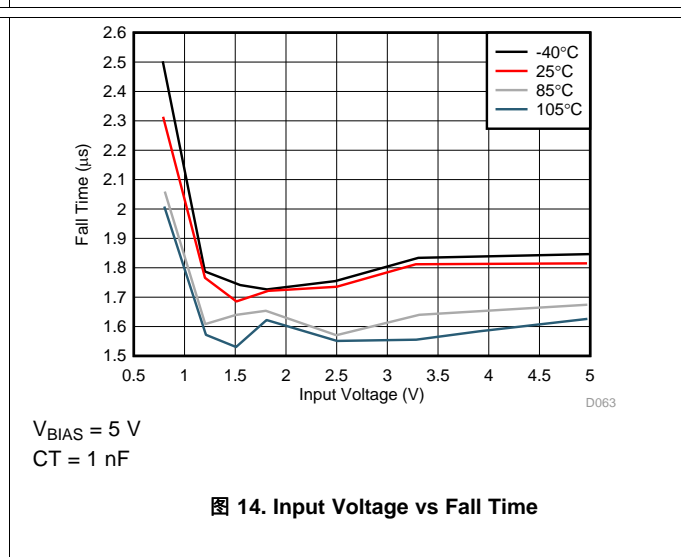
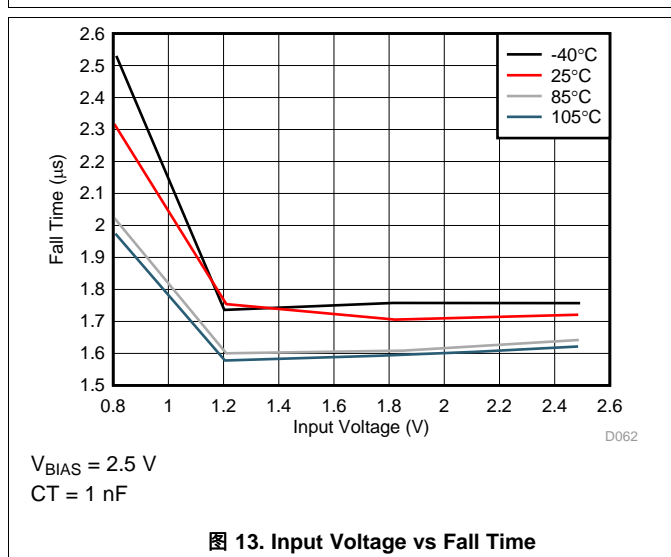
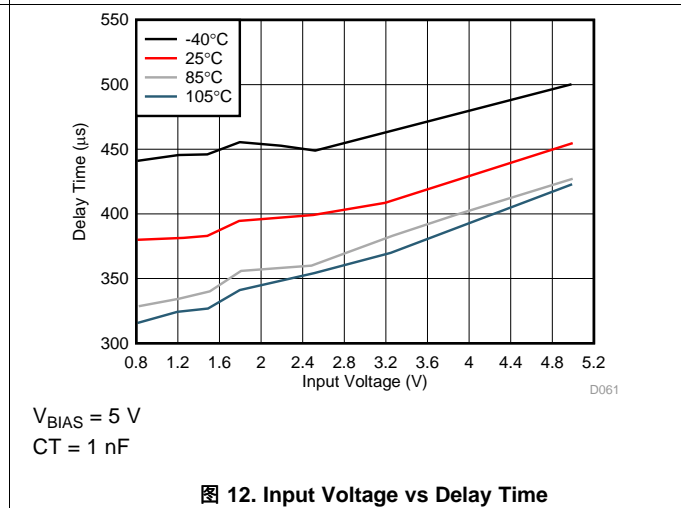
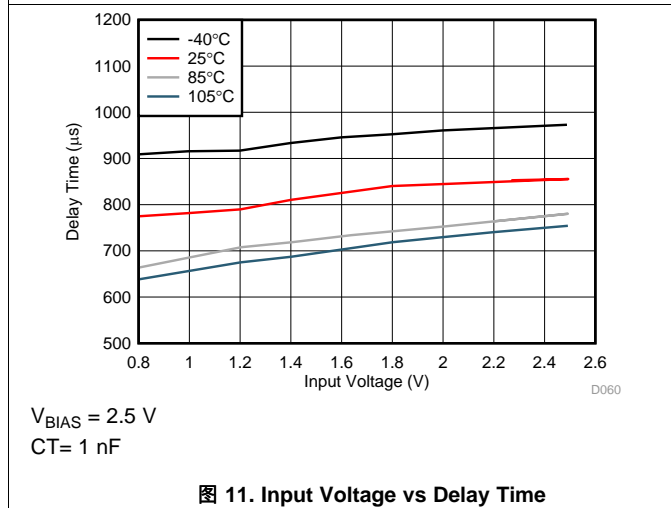
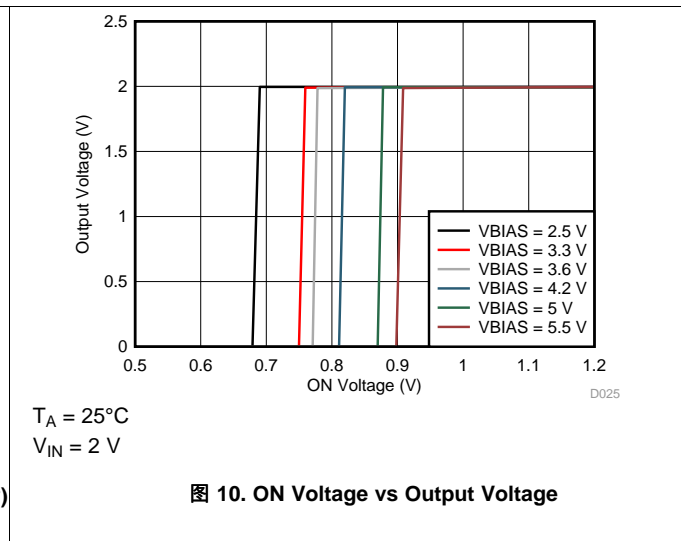
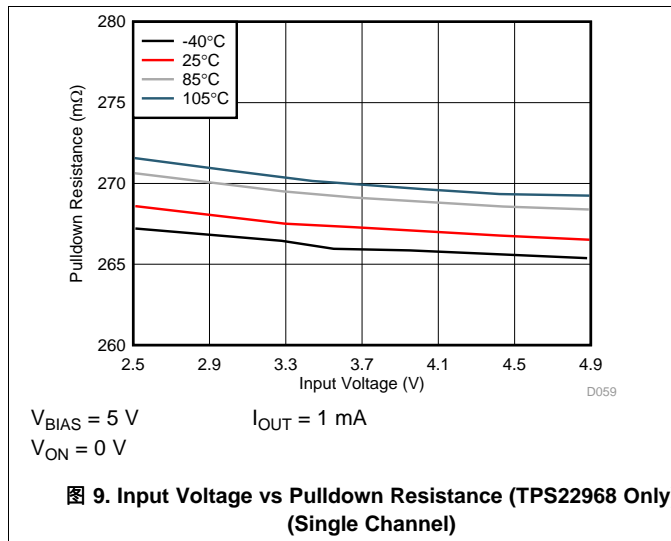
7.8 Typical DC Characteristics



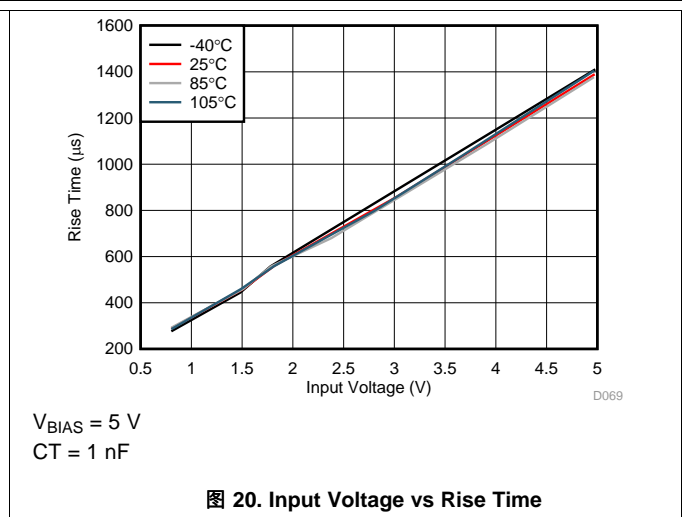
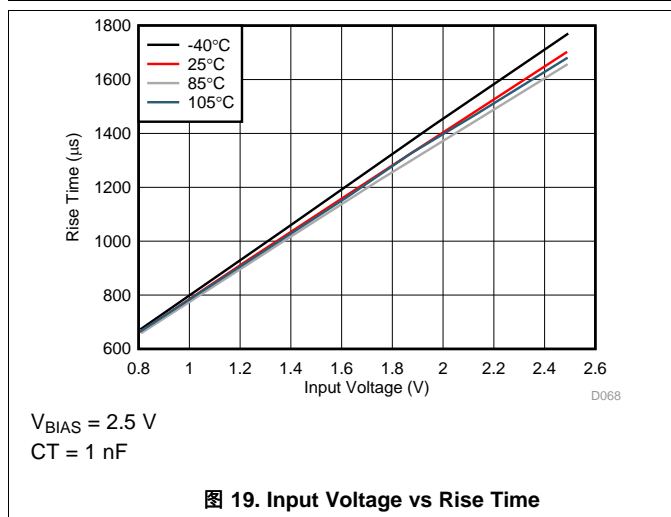
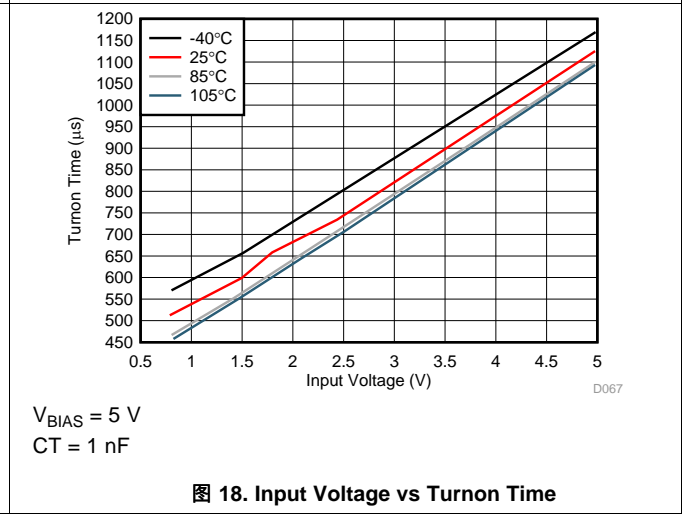
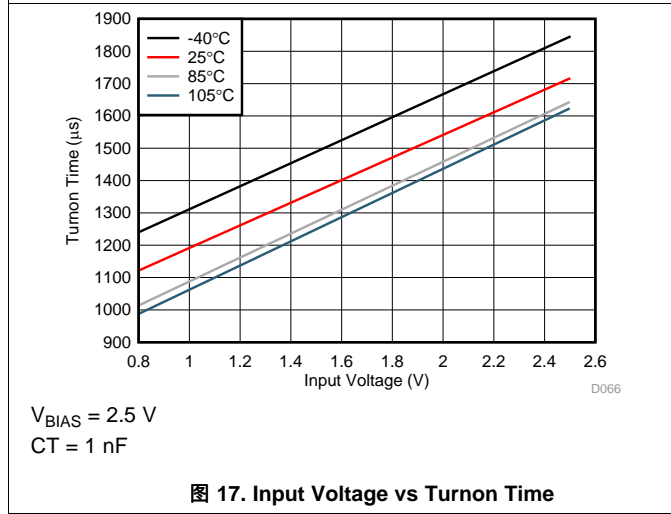
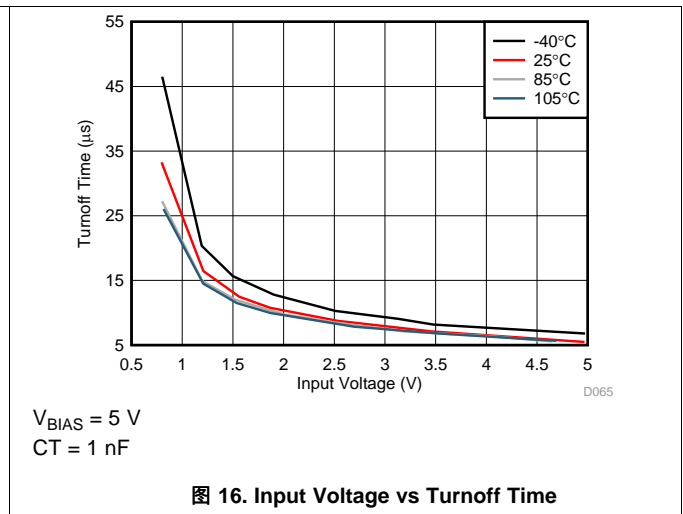
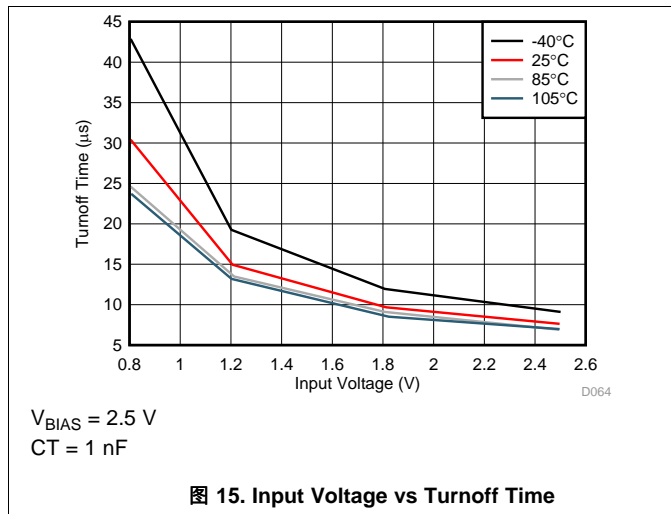
Typical DC Characteristics (接下页)



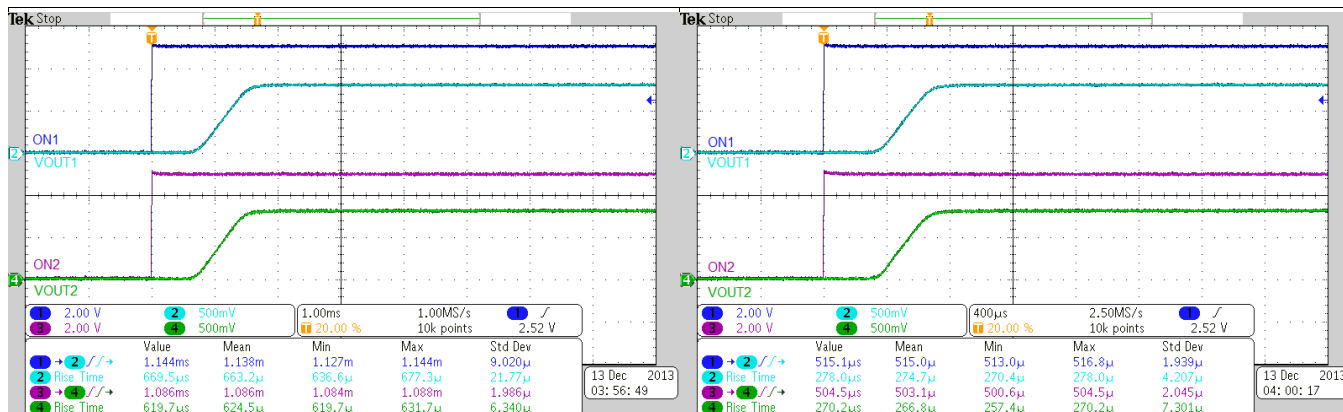
Typical DC Characteristics (接下页)



Typical DC Characteristics (接下页)



7.9 Typical AC Characteristics

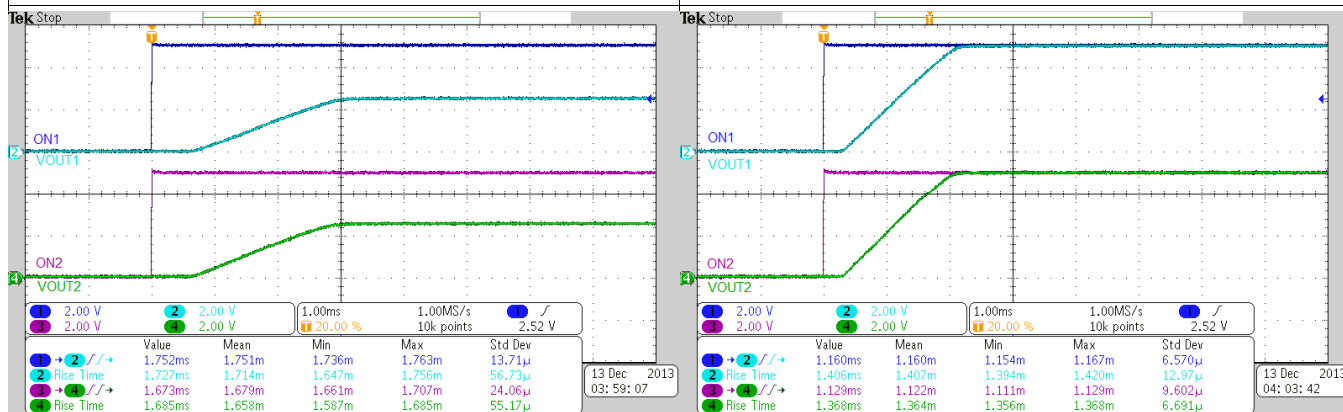


$V_{IN} = 0.8\text{ V}$ $V_{BIAS} = 2.5\text{ V}$ $C_{IN} = 1\text{ }\mu\text{F}$
 $R_L = 10\text{ }\Omega$ $C_L = 0.1\text{ }\mu\text{F}$

图 21. Turnon Response Time

$V_{IN} = 0.8\text{ V}$ $V_{BIAS} = 5\text{ V}$ $C_{IN} = 1\text{ }\mu\text{F}$
 $R_L = 10\text{ }\Omega$ $C_L = 0.1\text{ }\mu\text{F}$

图 22. Turnon Response Time

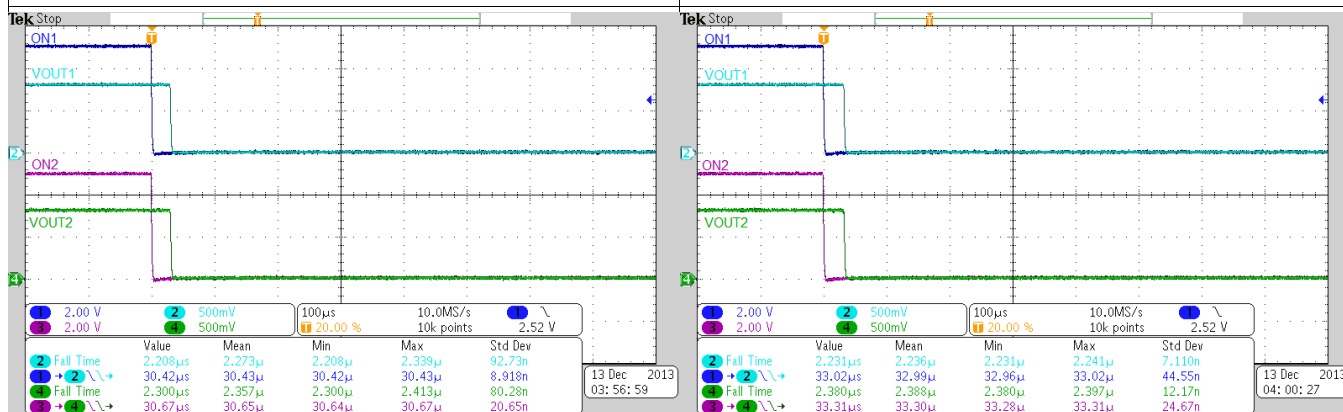


$V_{IN} = 2.5\text{ V}$ $V_{BIAS} = 2.5\text{ V}$ $C_{IN} = 1\text{ }\mu\text{F}$
 $R_L = 10\text{ }\Omega$ $C_L = 0.1\text{ }\mu\text{F}$

图 23. Turnon Response Time

$V_{IN} = 5\text{ V}$ $V_{BIAS} = 5\text{ V}$ $C_{IN} = 1\text{ }\mu\text{F}$
 $R_L = 10\text{ }\Omega$ $C_L = 0.1\text{ }\mu\text{F}$

图 24. Turnon Response Time



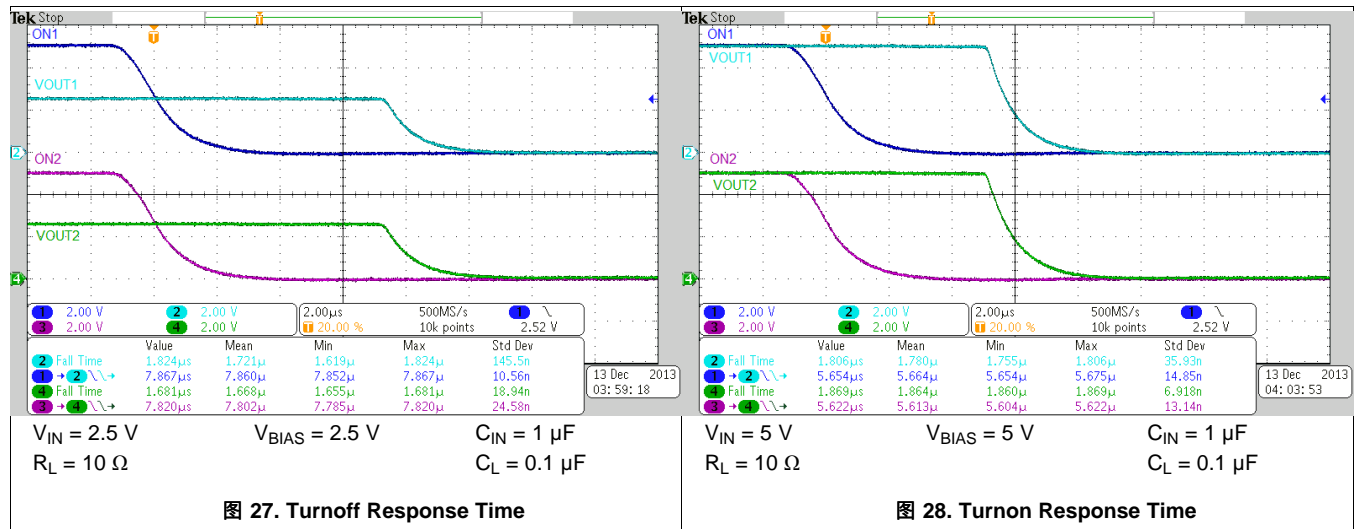
$V_{IN} = 0.8\text{ V}$ $V_{BIAS} = 2.5\text{ V}$ $C_{IN} = 1\text{ }\mu\text{F}$
 $R_L = 10\text{ }\Omega$ $C_L = 0.1\text{ }\mu\text{F}$

图 25. TurnOff Response Time

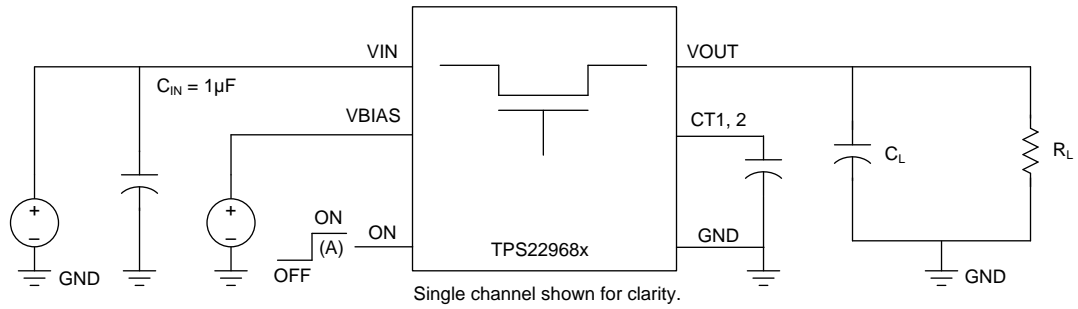
$V_{IN} = 0.8\text{ V}$ $V_{BIAS} = 5\text{ V}$ $C_{IN} = 1\text{ }\mu\text{F}$
 $R_L = 10\text{ }\Omega$ $C_L = 0.1\text{ }\mu\text{F}$

图 26. Turnoff Response Time

Typical AC Characteristics (接下页)

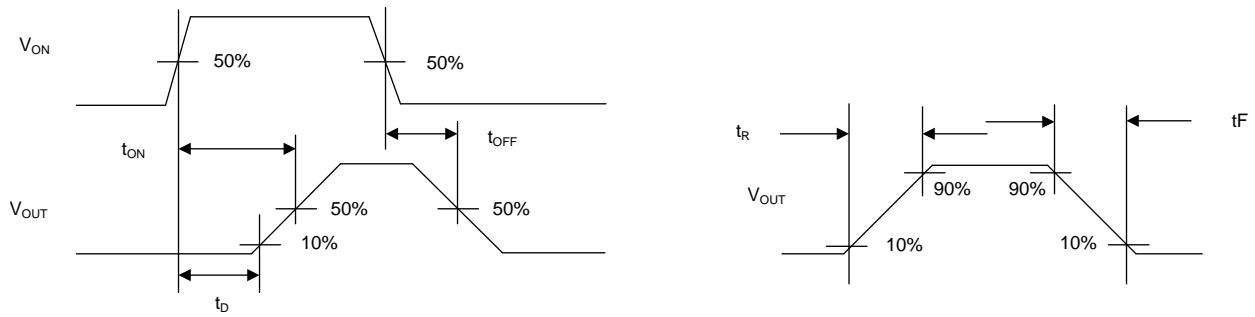


8 Parameter Measurement Information



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TEST CIRCUIT



TIMING DIAGRAMS

- A. Rise and fall times of the control signal is 100 ns.

图 29. Test Circuit and Timing Waveforms

9 Detailed Description

9.1 Overview

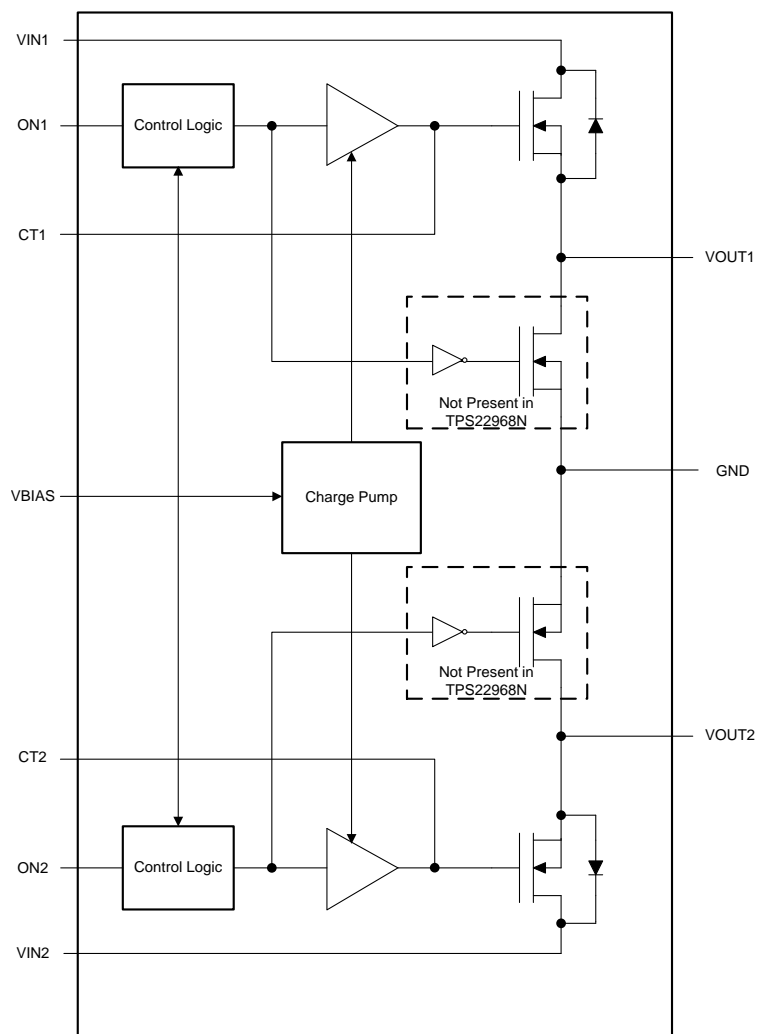
The TPS22968 is a 5.5-V, 4-A, dual-channel ultra-low R_{ON} load switch with controlled turnon. The device contains two N-channel MOSFETs. Each channel can support a maximum continuous current of 4 A and is controlled by an on and off GPIO-compatible input. The ON pin must be connected and cannot be left floating. The device is designed to control the turnon rate and therefore the inrush current. By controlling the inrush current, power supply sag can be reduced during turnon. The slew rate for each channel is set by connecting a capacitor to GND on the CT pins.

The slew rate is proportional to the capacitor on the CT pin. See the [Adjustable Rise Time](#) section to determine the correct CT value for a desired rise time.

The internal circuitry is powered by the VBIAS pin, which supports voltages from 2.5 V to 5.5 V. This circuitry includes the charge pump, QOD (optional), and control logic. For these internal blocks to function correctly, a voltage between 2.5 V and 5.5 V must be supplied to VBIAS.

When a voltage is supplied to VBIAS, the ON1 pin goes low, and the ON2 pins go low, the QOD turns on. This connects VOUT1 and VOUT2 to GND through an on-chip resistor. The typical pulldown resistance (R_{PD}) is 270 Ω .

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 ON and OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high and has a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

9.3.2 Input Capacitor (Optional)

When the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between VIN and GND to limit the voltage drop on the input supply caused by transient inrush currents. A 1- μ F ceramic capacitor (C_{IN}), placed close to the pins, is sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, TI recommends having an input capacitor 10x higher than the output capacitor to avoid excessive voltage drop.

9.3.3 Output Capacitor (Optional)

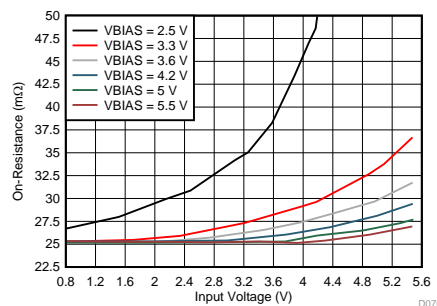
TI highly recommends a C_{IN} greater than C_L , because of the integrated body diode in the NMOS switch. A C_L greater than C_{IN} can cause the voltage on VOUT to exceed VIN when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. TI recommends a C_{IN} to C_L ratio of 10 to 1 for minimizing V_{IN} dip caused by inrush currents during startup.

9.3.4 QOD (Optional)

The TPS22968 includes a QOD feature. When the switch is disabled, a discharge resistor is connected between VOUT and GND. This resistor has a typical value of 270 Ω and prevents the output from floating while the switch is disabled.

9.3.5 VIN and VBIAS Voltage Range

For optimal R_{ON} performance, make sure $V_{IN} \leq V_{BIAS}$. The device is still functional if $V_{IN} > V_{BIAS}$, but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics ($V_{BIAS} = 5 V$)* and *Electrical Characteristics ($V_{BIAS} = 2.5 V$)* table. See [Figure 30](#) for an example of a typical device. Notice the increasing R_{ON} as V_{IN} exceeds V_{BIAS} voltage. Be sure to never exceed the maximum voltage rating for V_{IN} and V_{BIAS} .



Temperature = 25°C

$I_{OUT} = 200 \text{ mA}$

图 30. On-Resistance vs Input Voltage

Feature Description (接下页)

9.3.6 Adjustable Rise Time

A capacitor to GND on the CT pins sets the slew rate for each channel. The capacitor to GND on the CT pins must be rated for 25 V and above. An approximate formula for the relationship between CT and slew rate with $V_{BIAS} = 5\text{ V}$ is shown in [公式 1](#).

$$SR = 0.32 \times CT + 13.7$$

where

- SR is the slew rate (in $\mu\text{s/V}$)
- CT is the capacitance value on the CT pin (in pF)
- The units for the constant 13.7 is in $\mu\text{s/V}$.

(1)

Rise time can be calculated by multiplying the input voltage by the slew rate. [表 1](#) contains rise time values measured on a typical device.

表 1. Rise Time Table

CTx (pF)	Typical values at 25°C with a 25-V X7R 10% ceramic capacitor on CT ⁽¹⁾						
	VIN = 5 V	VIN = 3.3 V	VIN = 2.5 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2V	VIN = 0.8 V
0	65	48	41	35	31	29	24
220	378	253	197	152	131	111	83
470	704	474	363	272	234	192	140
1000	1387	931	717	544	449	372	273
2200	3062	2021	1536	1173	991	825	595
4700	7091	4643	3547	2643	2213	1828	1349
10000	14781	9856	7330	5507	4600	3841	2805

(1) RISE TIME (μs) 10% - 90%, $C_L = 0.1\ \mu\text{F}$, $C_{IN} = 1\ \mu\text{F}$, $R_L = 10\ \Omega$, $V_{BIAS} = 5\text{ V}$

9.4 Device Functional Modes

[表 2](#) lists the device function table.

表 2. Functional Table

ONx	VINx to VOUTx	VOUTx to GND
L	Off	On
H	On	Off

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

This section highlights some of the design considerations for implementing this device in various applications. A PSPICE model for this device is also available on the [product page](#) for additional information.

10.1.1 Parallel Configuration

To increase the current capabilities and lower the R_{ON} by approximately 50%, both channels can be placed in parallel as shown in [图 31](#) (parallel configuration). With this configuration, the CT1 and CT2 pins can be tied together to use one capacitor, CT, as shown in [图 31](#). With a single CT capacitor, the rise time is half of the typical rise-time value. Refer to the [表 1](#) for typical timing values.

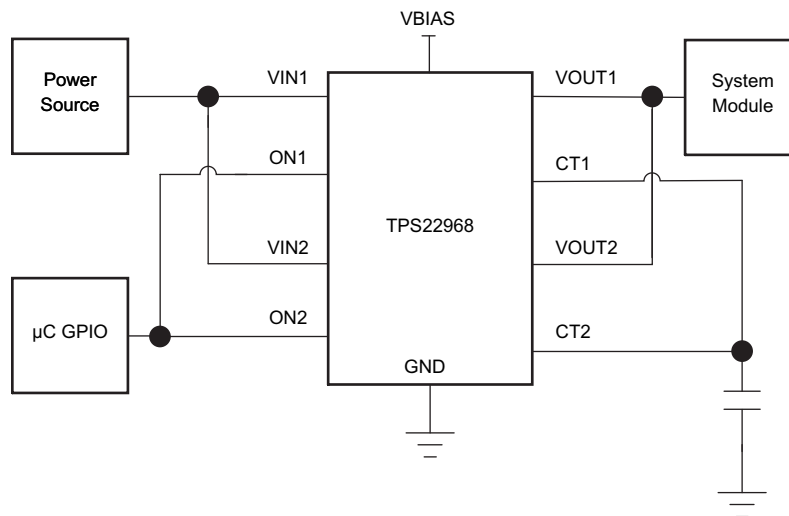


图 31. Parallel Configuration

Application Information (接下页)

10.1.2 Standby Power Reduction

Any end equipment that is powered from the battery has a need to reduce current consumption to keep the battery charged for a longer time. TPS22968 helps to accomplish this by turning off the supply to the modules that are in standby state, and therefore, significantly reduces the leakage current overhead of the standby modules. See [图 32](#).

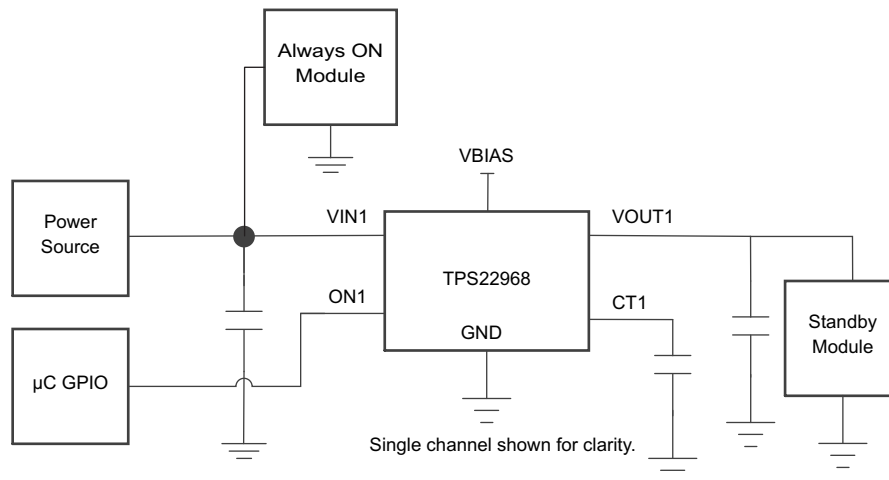
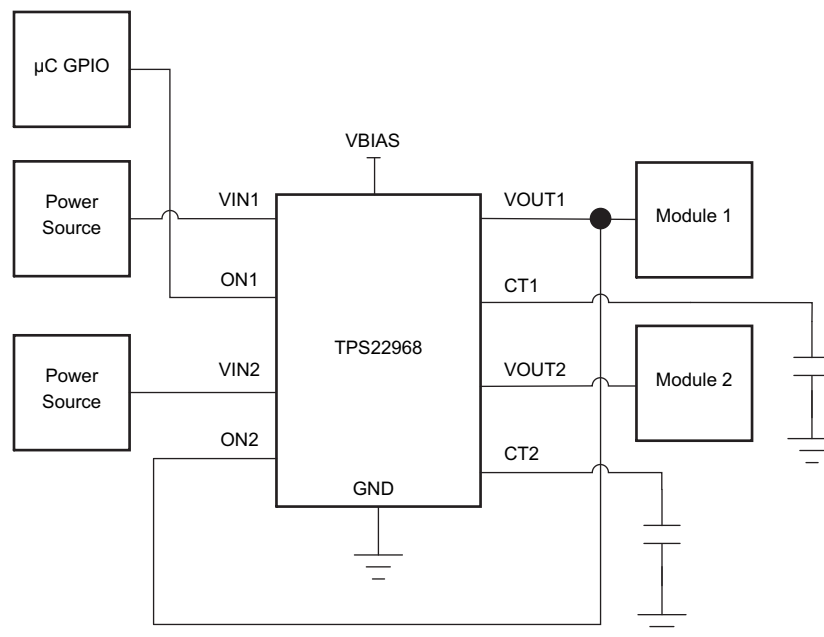


图 32. Standby Power Reduction

10.1.3 Power Supply Sequencing Without a GPIO Input

In many end equipments, there is a need to power up various modules in a predetermined manner. The TPS22968 can solve the problem of power sequencing without adding any complexity to the overall system. See [图 33](#).



VIN1 must be greater V_{IH} .

图 33. Power Sequencing Without a GPIO Input

Application Information (接下页)

10.1.4 Reverse Current Blocking

In certain applications, it may be desirable to have reverse current blocking. Reverse current blocking prevents current from flowing from the output to the input of the load switch when the device is disabled. With the following configuration, the TPS22968 can be converted into a single-channel switch with reverse current blocking. In this configuration, VIN1 or VIN2 can be used as the input and VIN2 or VIN1 is the output. See [图 34](#).

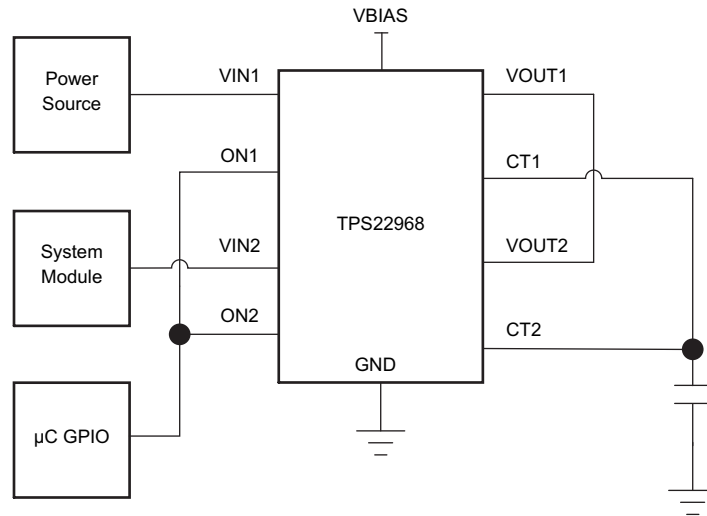


图 34. Reverse Current Blocking

10.2 Typical Application

This application demonstrates how the TPS22968 can be used to power downstream modules with large capacitances. The example in [图 35](#) TPS22968 is powering a 100- μF capacitive output load.

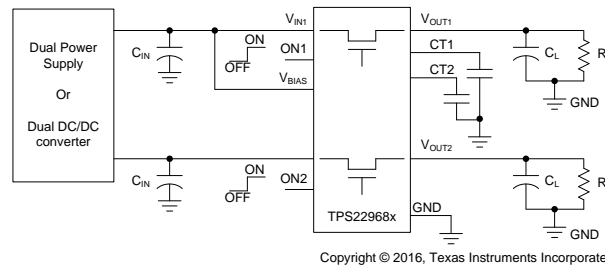


图 35. Typical Application Schematic for Powering a Downstream Module

10.2.1 Design Requirements

For this design example, use the following [表 3](#) as the input parameters.

表 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
Load current	4 A
Output capacitance (C_L)	22 μF
Allowable inrush current on VOUT	0.33 A

10.2.2 Detailed Design Procedure

To begin the design process, the designer must know the following:

- V_{IN} voltage
- V_{BIAS} voltage
- Load current
- Allowable inrush current on VOUT due to C_L capacitor

10.2.2.1 V_{IN} to V_{OUT} Voltage Drop

The V_{IN} to V_{OUT} voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the V_{IN} and V_{BIAS} conditions of the device. Refer to the R_{ON} specification of the device in the [Electrical Characteristics \(\$V_{BIAS} = 5\text{ V}\$ \)](#) and [Electrical Characteristics \(\$V_{BIAS} = 2.5\text{ V}\$ \)](#). After the R_{ON} of the device is determined based upon the V_{IN} and V_{BIAS} conditions, use [公式 2](#) to calculate the V_{IN} to V_{OUT} voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON}$$

where

- ΔV is the voltage drop from V_{IN} to V_{OUT}
 - I_{LOAD} is the load current
 - R_{ON} is the On-resistance of the device for a specific V_{IN} and V_{BIAS} combination
- (2)

An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

10.2.2.2 Inrush Current

To determine how much inrush current is caused by the C_L capacitor, use [公式 3](#).

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt}$$

where

- I_{INRUSH} is the amount of inrush caused by C_L
- C_L is the capacitance on VOUT
- dt is the time it takes for change in V_{OUT} during the ramp up of VOUT when the device is enabled
- dV_{OUT} is the change in V_{OUT} during the ramp up of VOUT when the device is enabled (3)

The device offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon through the CTx pins. The appropriate rise time can be calculated using the design requirements and the inrush current equation (公式 3). See 公式 4 and 公式 5.

$$330 \text{ mA} = 22 \text{ } \mu\text{F} \times 3.3 \text{ V} / \text{dt} \quad (4)$$

$$\text{dt} = 220 \text{ } \mu\text{s} \quad (5)$$

To ensure an inrush current of less than 330 mA, choose a CT based on 表 1 or 公式 1 value that yields a rise time of more than 220 μs . See the oscilloscope captures in the *Application Curves* for an example of how the CT capacitor can be used to reduce inrush current. See 表 1 for correlation between rise times and CT values.

An appropriate C_L value must be placed on VOUT such that the I_{MAX} and I_{PLS} specifications of the device are not violated.

10.2.2.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{\text{D(max)}}$ for a given output current and ambient temperature, use 公式 6.

$$P_{\text{D(MAX)}} = \frac{T_{\text{J(MAX)}} - T_{\text{A}}}{R_{\theta\text{JA}}}$$

where

- $P_{\text{D(max)}}$ is the maximum allowable power dissipation
- $T_{\text{J(max)}}$ is the maximum allowable junction temperature (125°C for the TPS22968)
- T_{A} is the ambient temperature of the device
- $R_{\theta\text{JA}}$ is the junction to air thermal impedance. See the *Thermal Information* table. This parameter is highly dependent upon board layout. (6)

公式 7 到 公式 10 和 公式 11 到 公式 13 show two examples to determine how to use this information correctly:

For $V_{\text{BIAS}} = 5 \text{ V}$, $V_{\text{IN}} = 5 \text{ V}$, the maximum ambient temperature with a 4-A load through each channel can be determined by using 公式 7 到 公式 10:

$$P_{\text{D}} = I^2 \times R \times 2 \text{ (multiplied by 2 because there are two channels)} \quad (7)$$

$$2 \times I^2 \times R = \frac{T_{\text{J(MAX)}} - T_{\text{A}}}{R_{\theta\text{JA}}} \quad (8)$$

$$T_{\text{A}} = T_{\text{J(MAX)}} - R_{\theta\text{JA}} \times 2 \times I^2 \times R \quad (9)$$

$$T_{\text{A}} = 125^\circ\text{C} - 62.5^\circ\text{C/W} \times 2 \times (4 \text{ A})^2 \times 27 \text{ m}\Omega = 71^\circ\text{C} \quad (10)$$

For $V_{\text{BIAS}} = 5 \text{ V}$, $V_{\text{IN}} = 5 \text{ V}$, the maximum continuous current for an ambient temperature of 85°C with the same current flowing through each channel can be determined by using 公式 11 到 公式 13:

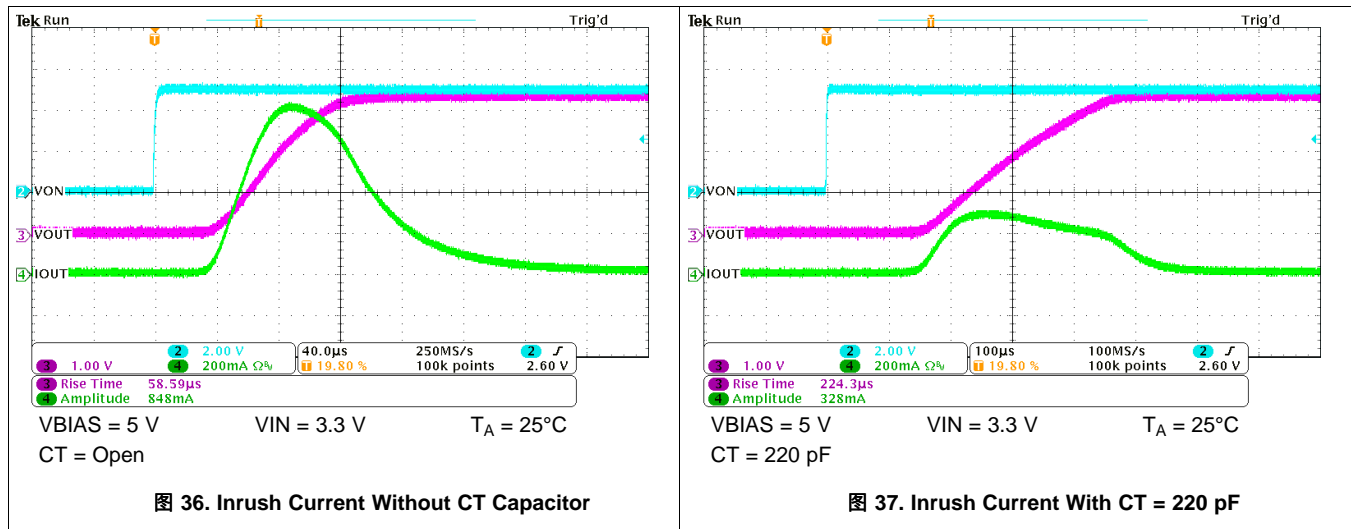
$$2 \times I^2 \times R = \frac{T_{\text{J(MAX)}} - T_{\text{A}}}{R_{\theta\text{JA}}} \quad (11)$$

$$I = \sqrt{\frac{T_{J(MAX)} - T_A}{2 \times R \times R_{\theta JA}}} \tag{12}$$

$$I = \sqrt{\frac{125^{\circ}\text{C} - 105^{\circ}\text{C}}{2 \times 27\text{m}\Omega \times 62.5^{\circ}\text{C/W}}} = 3.44 \text{ A per channel} \tag{13}$$

10.2.3 Application Curves

The twp scope captures show the usage of a CT capacitor in conjunction with the device. A higher CT value results in a slower rise and a lower inrush current.



11 Power Supply Recommendations

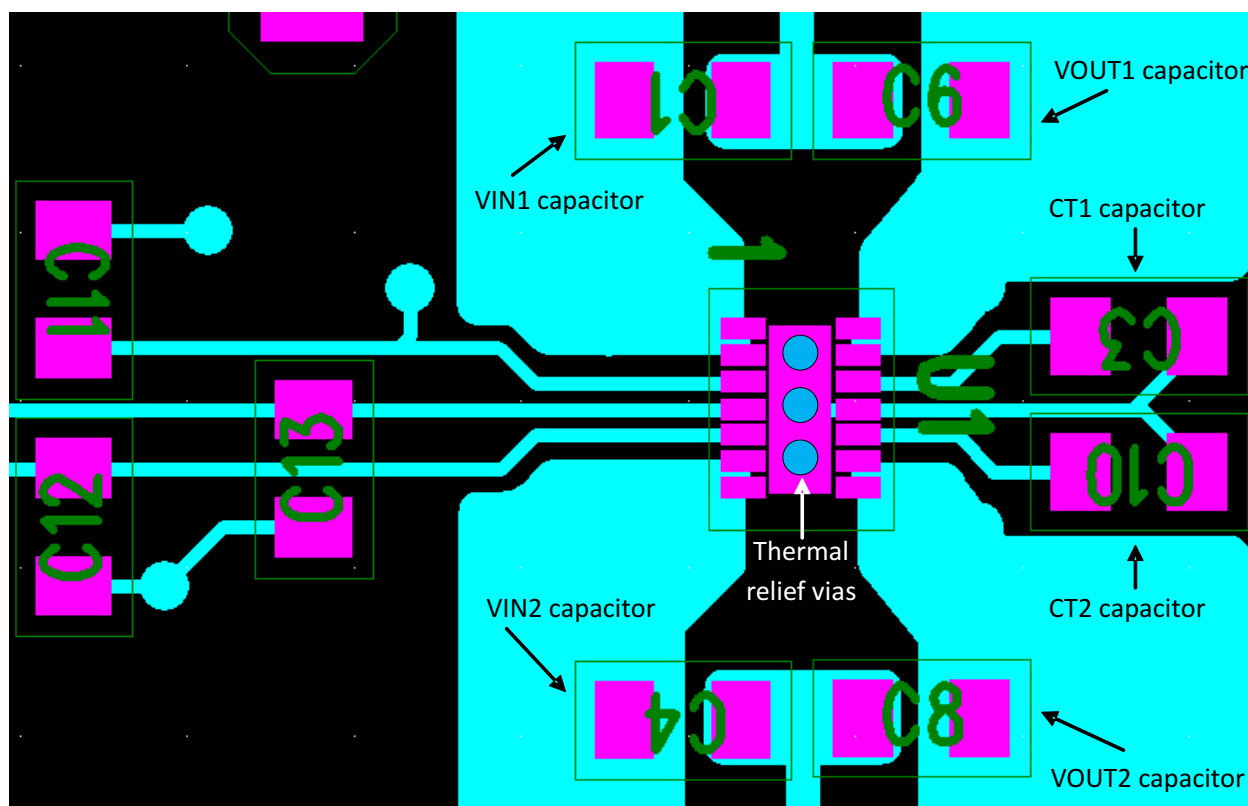
The device is designed to operate from a V_{BIAS} range of 2.5 V to 5.5 V and V_{IN} range of 0.8 V to 5.5 V. This supply must be well regulated and placed as close to the device pin as possible with the recommended 1- μ F bypass capacitor. If the supply is located more than a few inches from the device pins, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 μ F may be sufficient.

12 Layout

12.1 Layout Guidelines

- V_{IN} and V_{OUT} traces must be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- V_{INx} pins must be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 1- μ F ceramic with X5R or X7R dielectric. This capacitor must be placed as close to the device pins as possible.
- V_{OUTx} pins must be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is one-tenth of the V_{INx} bypass capacitor of X5R or X7R dielectric rating. This capacitor must be placed as close to the device pins as possible.
- The V_{BIAS} pin must be bypassed to ground with low-ESR ceramic bypass capacitors. The typical recommended bypass capacitance is 0.1- μ F ceramic with X5R or X7R dielectric.
- The CTx capacitors must be placed as close to the device pins as possible. The typical recommended CTx capacitance is a capacitor of X5R or X7R dielectric rating with a rating of 25 V or higher.

12.2 Layout Example



13 器件和文档支持

13.1 器件支持

13.1.1 开发支持

有关 TPS22968 和 TPS22968-Q1 PSpice 瞬态模型，请参阅 [SLVMA29](#)。

有关 TPS22968N 和 TPS22968N-Q1 PSpice 瞬态模型，请参阅 [SLVMBA9](#)。

13.2 文档支持

13.2.1 相关文档

请参阅如下相关文档：

- 《管理浪涌电流》，[SLVA670A](#)
- 《负载开关功耗之静态电流与关断电流》，[SLVA757](#)
- 《TPS22968EVM-007 双路 4A 负载开关》，[SLVUA30](#)
- 《负载开关热效应注意事项》，[SLVUA74](#)
- 《TPS22968/68N-Q1 双通道 5.5V 4A 27mΩ 负载开关 EVM 用户指南》，[SLVUAE2A](#)
- 《TPS22968NEVM 双路 4A 负载开关》，[SLVUAL0](#)

13.3 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 4. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
TPS22968	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS22968N	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.4 接收文档更新通知

如需接收文档更新通知，请访问 [ti.com](#) 上的器件产品文件夹。请单击右上角的通知我 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

13.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 [TI 的工程师对工程师 \(E2E\) 社区](#)。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](#) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

13.6 商标

E2E is a trademark of Texas Instruments.

Ultrabook is a trademark of Intel.

13.7 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.8 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22968DPUR	ACTIVE	WSON	DPU	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB968	Samples
TPS22968DPUT	ACTIVE	WSON	DPU	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB968	Samples
TPS22968NDPUR	ACTIVE	WSON	DPU	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	RB968N	Samples
TPS22968NDPUT	ACTIVE	WSON	DPU	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	RB968N	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS22968 :

- Automotive : [TPS22968-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22968DPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22968DPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22968NDPUR	WSON	DPU	14	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22968NDPUT	WSON	DPU	14	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

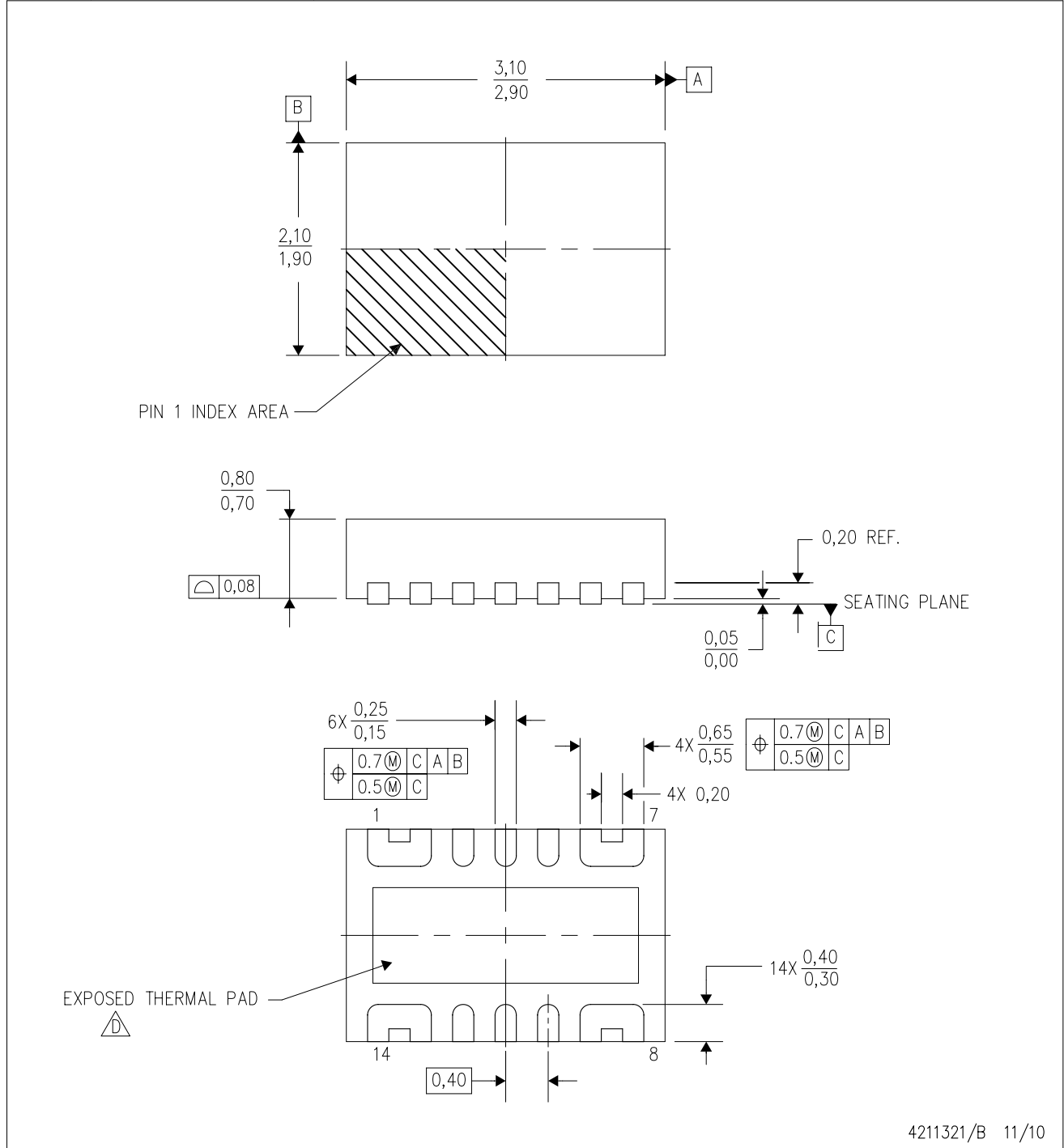
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22968DPUR	WSON	DPU	14	3000	210.0	185.0	35.0
TPS22968DPUT	WSON	DPU	14	250	210.0	185.0	35.0
TPS22968NDPUR	WSON	DPU	14	3000	182.0	182.0	20.0
TPS22968NDPUT	WSON	DPU	14	250	182.0	182.0	20.0

DPU (R-PWSON-N14)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - Small Outline No-Lead (SON) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - This package is Pb-free.

THERMAL PAD MECHANICAL DATA

DPU (R-PWSON-N14)

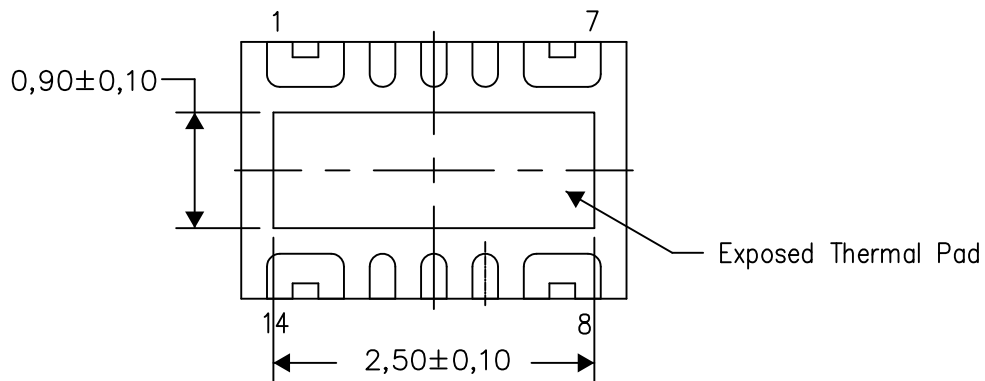
PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

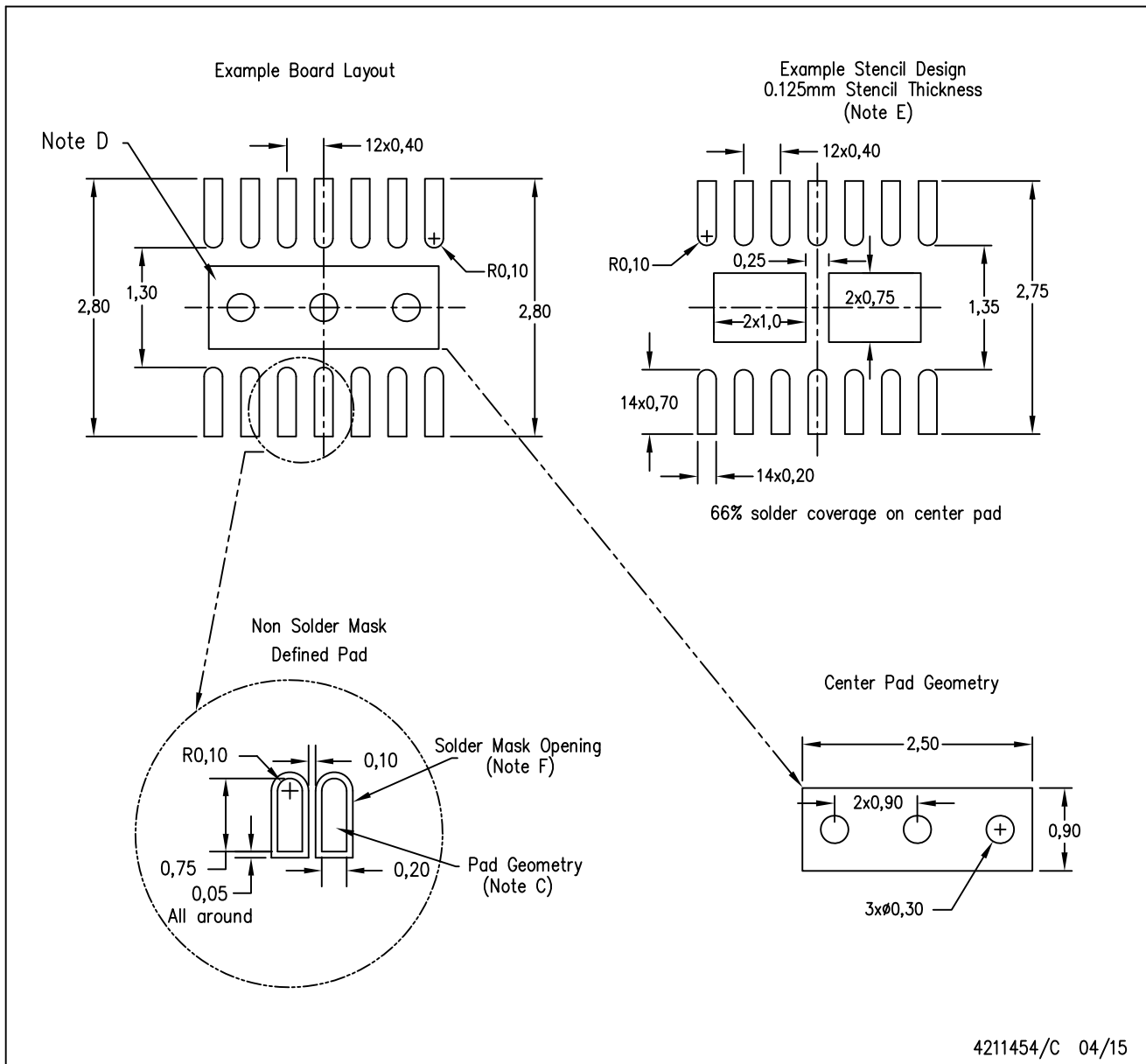
Exposed Thermal Pad Dimensions

4211395/C 04/15

NOTE: All linear dimensions are in millimeters

DPU (R-PWSON-N14)

PLASTIC SMALL OUTLINE NO-LEAD



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

重要声明和免责声明

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