

## TPS2295x 5.7V、5A、14mΩ 导通电阻负载开关

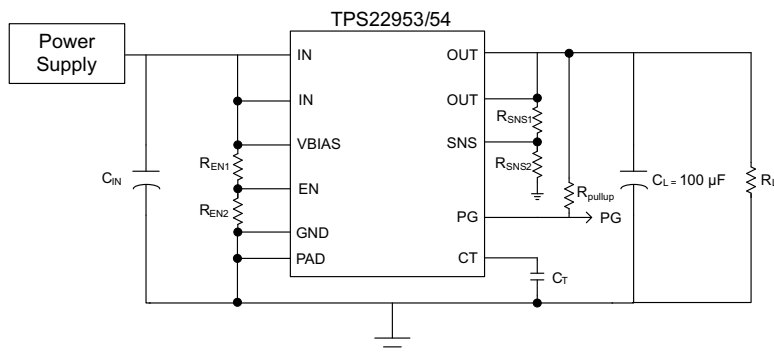
### 1 特性

- 集成单通道负载开关
- 输入电压范围：0.7V 至 5.7V
- $R_{ON}$  电阻
  - $V_{IN} = 5V$  ( $V_{BIAS} = 5V$ ) 时,  $R_{ON} = 14m\Omega$
- 5A 最大持续开关电流
- 可调欠压闭锁 (UVLO) 阈值
- 带有电源正常 (PG) 指示器的可调电压监控器
- 可调输出转换率控制
- 增强型快速输出放电功能, 在电源移除后仍能保持激活状态 (仅 TPS22954)
  - $15\Omega$  (典型值), 可使  $100\mu F$  电容在 10ms 内完全放电
- 禁用时提供反向电流保护 (仅 TPS22953)
- 可在监控器检测到故障后自动重启 (使能时)
- 热关断
- 低静态电流  $\leq 50\mu A$
- 带有散热焊盘的小外形尺寸无引线 (SON) 10 引脚封装
- 经测试, 静电放电 (ESD) 性能符合 JESD 22 规范
  - 2kV 人体模型 (HBM) 和 750V 充电器件模型 (CDM)

### 2 应用

- 固态硬盘
- 嵌入式/工业 PC
- Ultrabook™/笔记本电脑
- 台式机
- 服务器
- 电信系统

### 4 简化电路原理图



### 3 说明

TPS22953/54 是具有受控导通功能的小型单通道负载开关。该器件包含一个可在 0.7V 至 5.7V 输入电压范围内运行的 N 通道 MOSFET, 并且可支持最大 5A 的持续电流。

该器件具有可调欠压闭锁 (UVLO) 和可调电源正常 (PG) 阈值, 可提供电压监控和可靠的电源排序功能。器件的可调上升时间控制功能可大幅降低各类大容量负载电容的浪涌电流, 从而降低或消除电源压降。此开关可由一个导通/关断输入 (EN) 独立控制, 该输入可与低压控制信号直接对接。器件集成了一个  $15\Omega$  片上负载电阻, 可在开关被禁用时使输出快速放电。增强型快速输出放电 (QOD) 功能可在器件断电后的一小段时间内继续保持激活状态, 以便使输出完成放电。

TPS22953/54 采用小型、节省空间的 10 引脚小外形尺寸无引线 (SON) 封装, 此类封装具有集成散热焊盘, 支持较高功耗。器件在自然通风环境下的额定运行温度范围为  $-40^{\circ}C$  至  $105^{\circ}C$ 。

器件信息(1)

器件编号	封装 (引脚)	封装尺寸 (标称值)
TPS2295x	DSQ (10)	2.00mm x 2.00mm
	DQC (10)	2.00mm x 3.00mm

(1) 要了解所有可用封装, 请见数据表末尾的可订购产品附录。

## 目录

<b>1</b>	特性 .....	<b>1</b>	8.12	Typical Switching Characteristics .....	<b>15</b>
<b>2</b>	应用 .....	<b>1</b>	<b>9</b>	<b>Detailed Description</b> .....	<b>21</b>
<b>3</b>	说明 .....	<b>1</b>	9.1	Overview .....	<b>21</b>
<b>4</b>	简化电路原理图 .....	<b>1</b>	9.2	Functional Block Diagram .....	<b>21</b>
<b>5</b>	修订历史记录 .....	<b>2</b>	9.3	Feature Description .....	<b>22</b>
<b>6</b>	<b>Device Comparison Table</b> .....	<b>3</b>	9.4	Device Functional Modes .....	<b>27</b>
<b>7</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	<b>10</b>	<b>Application and Implementation</b> .....	<b>28</b>
<b>8</b>	<b>Specifications</b> .....	<b>4</b>	10.1	Application Information .....	<b>28</b>
8.1	Absolute Maximum Ratings .....	<b>4</b>	10.2	Typical Application .....	<b>31</b>
8.2	ESD Ratings .....	<b>4</b>	<b>11</b>	<b>Power Supply Recommendations</b> .....	<b>33</b>
8.3	Recommended Operating Conditions .....	<b>4</b>	<b>12</b>	<b>Layout</b> .....	<b>33</b>
8.4	Thermal Information .....	<b>5</b>	12.1	Layout Guidelines .....	<b>33</b>
8.5	Electrical Characteristics .....	<b>5</b>	12.2	Layout Example .....	<b>34</b>
8.6	Electrical Characteristics, $V_{BIAS} = 5\text{ V}$ .....	<b>6</b>	<b>13</b>	<b>器件和文档支持</b> .....	<b>35</b>
8.7	Electrical Characteristics, $V_{BIAS} = 3.3\text{ V}$ .....	<b>7</b>	13.1	相关链接 .....	<b>35</b>
8.8	Electrical Characteristics, $V_{BIAS} = 2.5\text{ V}$ .....	<b>8</b>	13.2	商标 .....	<b>35</b>
8.9	Switching Characteristics, $CT = 1000\text{ pF}$ .....	<b>9</b>	13.3	静电放电警告 .....	<b>35</b>
8.10	Switching Characteristics, $CT = 0\text{ pF}$ .....	<b>10</b>	13.4	术语表 .....	<b>35</b>
8.11	Typical DC Characteristics .....	<b>12</b>	<b>14</b>	<b>机械封装和可订购信息</b> .....	<b>35</b>

## 5 修订历史记录

### Changes from Original (March 2015) to Revision A

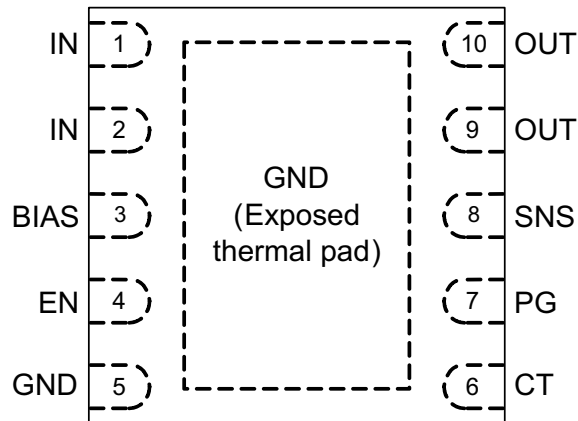
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• 完整版的最初发布版本。 .....	<b>1</b>
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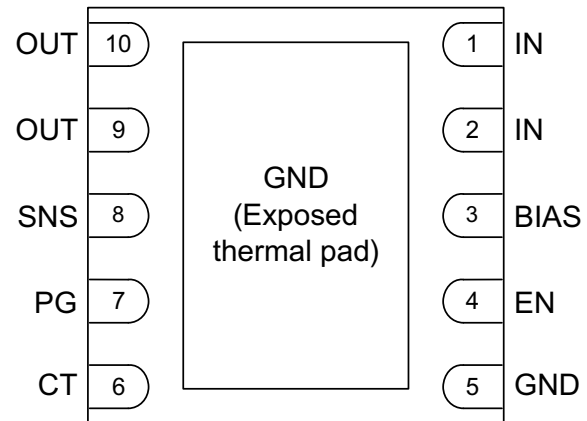
## 6 Device Comparison Table

Device	Quick Output Discharge	Reverse Current Blocking	Package (Pin)	Body Size	Pin Pitch
TPS22954	Yes	No	DSQ (10)	2.00 mm x 2.00 mm	0.4 mm
			DQC (10)	2.00 mm x 3.00 mm	0.5 mm
TPS22953	No	Yes	DSQ (10)	2.00 mm x 2.00 mm	0.4 mm
			DQC (10)	2.00 mm x 3.00 mm	0.5 mm

## 7 Pin Configuration and Functions



Top View



Bottom View

### Pin Functions

PIN <sup>(1)</sup>		I/O	DESCRIPTION
NAME	NO.		
IN	1, 2	I	Switch input. Bypass this input with a ceramic capacitor to GND.
BIAS	3	I	Bias pin and power supply to the device.
EN	4	I	Active high switch enable/disable input. Also acts as the input UVLO pin. Use external resistor divider to adjust the UVLO level. Do not leave floating.
GND	5	–	Device ground.
CT	6	O	$V_{OUT}$ slew rate control. Place ceramic cap from CT to GND to change the $V_{OUT}$ slew rate of the device and limit the inrush current. CT Capacitor should be rated to 25V or higher.
PG	7	O	Power good. This pin is open drain which will pull low when the voltage on EN and/or SNS is below their respective VIL level.
SNS	8	I	Sense pin. Use external resistor divider to adjust the power good level. Do not leave floating.
OUT	9, 10	O	Switch output.
Thermal Pad	–	–	Exposed thermal pad. Tie to GND.

(1) Pinout applies to all package versions.

## 8 Specifications

### 8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage range	-0.3	6	V
V <sub>BIAS</sub>	Bias voltage range	-0.3	6	V
V <sub>OUT</sub>	Output voltage range	-0.3	6	V
V <sub>EN</sub> , V <sub>SNS</sub> , V <sub>PG</sub>	EN, SNS, and PG voltage range	-0.3	6	V
I <sub>MAX</sub>	Maximum Continuous Switch Current, T <sub>A</sub> = 70°C		5	A
I <sub>PLS</sub>	Maximum Pulsed Switch Current, pulse <300µs, 2% duty cycle		7	A
T <sub>J,MAX</sub>	Maximum junction temperature	Internally limited <sup>(2)</sup>		
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) See TSD specification in *Electrical Characteristics* section and *Thermal Considerations* section.

### 8.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±750

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

### 8.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage range	0.7	V <sub>BIAS</sub>	V
V <sub>BIAS</sub>	Bias voltage range	2.5	5.7	V
V <sub>OUT</sub>	Output voltage range	0	5.7	V
V <sub>EN</sub> , V <sub>SNS</sub> , V <sub>PG</sub>	EN, SNS, and PG voltage range	0	5.7	V
T <sub>A</sub> <sup>(1)</sup>	Operating free-air temperature range	-40	105	°C
T <sub>J</sub>	Operating Junction Temperature	-40	125	°C

- (1) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature [T<sub>A(max)</sub>] is dependent on the maximum operating junction temperature [T<sub>J(max)</sub>], the maximum power dissipation of the device in the application [P<sub>D(max)</sub>], and the junction-to-ambient thermal resistance of the part/package in the application (θ<sub>JA</sub>), as given by the following equation: T<sub>A(max)</sub> = T<sub>J(max)</sub> - (θ<sub>JA</sub> × P<sub>D(max)</sub>)

## 8.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS22953/54		UNIT
		DQC-10	DSQ-10	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	65.2	63.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	73.9	81.6	
R <sub>θJB</sub>	Junction-to-board thermal resistance	25.5	34.1	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	2	1.9	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	25.4	34.5	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	8.5	7.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 8.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature  $-40\text{ °C} \leq T_A \leq 105\text{ °C}$  and the recommended  $V_{BIAS}$  voltage range of 2.5V to 5.7V. Typical values are for  $T_A = 25\text{ °C}$ .

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
<b>VOLTAGE THRESHOLDS</b>							
V <sub>EN</sub>	V <sub>IH</sub> , Rising threshold	V <sub>IN</sub> = 0.7V to V <sub>BIAS</sub>	-40°C to 105°C	650	700	750	mV
	V <sub>IL</sub> , Falling threshold	V <sub>IN</sub> = 0.7V to V <sub>BIAS</sub>	-40°C to 105°C	560	600	640	mV
V <sub>SNS</sub>	V <sub>IH</sub> , Rising threshold	V <sub>IN</sub> = 0.7V to V <sub>BIAS</sub>	-40°C to 105°C	465	515	565	mV
	V <sub>IL</sub> , Falling threshold	V <sub>IN</sub> = 0.7V to V <sub>BIAS</sub>	-40°C to 105°C	410	455	500	mV
<b>TIMINGS</b>							
t <sub>BLANK</sub>	Blanking time for EN and SNS	EN or SNS Rising	-40°C to 105°C	100			μs
t <sub>DEGLITCH</sub>	Deglitch time for EN and SNS	EN or SNS Falling	-40°C to 105°C	5			μs
t <sub>DIS</sub>	Output discharge time (TPS22954 Only)	C <sub>L</sub> = 100 μF	-40°C to 105°C			10	ms
t <sub>RESTART</sub>	Output Restart Time	SNS Falling	-40°C to 105°C	2			ms
<b>THERMAL CHARACTERISTICS</b>							
T <sub>SD</sub>	Thermal shutdown	Junction Temperature Rising	-	130	150	170	°C
TSD <sub>HYS</sub>	Thermal shutdown hysteresis	Junction Temperature Falling	-	20			°C

## 8.6 Electrical Characteristics, $V_{BIAS} = 5\text{ V}$

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature  $-40\text{ °C} \leq T_A \leq 105\text{ °C}$  and  $V_{BIAS} = 5\text{ V}$ . Typical values are for  $T_A = 25\text{ °C}$ .

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT	
<b>POWER SUPPLIES AND CURRENTS</b>								
$I_{Q, BIAS}$	BIAS quiescent current	$I_{OUT} = 0, V_{IN} = 0.7\text{ V to } V_{BIAS}, V_{EN} = 5\text{ V}$	-40°C to 85°C	34	45		$\mu\text{A}$	
			-40°C to 105°C			50		
$I_{SD, BIAS}$	BIAS shutdown current	$V_{OUT} = 0\text{ V}, V_{IN} = 0.7\text{ V to } V_{BIAS}, V_{EN} = 0\text{ V}$	-40°C to 85°C	5	7		$\mu\text{A}$	
			-40°C to 105°C			8	$\mu\text{A}$	
$I_{SD, IN}$	Input shutdown current	$V_{EN} = 0\text{ V}, V_{OUT} = 0\text{ V}$	$V_{IN} = 5.0\text{ V}$	-40°C to 85°C	0.02	4	$\mu\text{A}$	
				-40°C to 105°C				13
			$V_{IN} = 3.3\text{ V}$	-40°C to 85°C	0.01	3		
				-40°C to 105°C				10
			$V_{IN} = 1.8\text{ V}$	-40°C to 85°C	0.01	3		
				-40°C to 105°C				10
			$V_{IN} = 1.2\text{ V}$	-40°C to 85°C	0.01	2		
				-40°C to 105°C				8
$V_{IN} = 0.7\text{ V}$	-40°C to 85°C	0.01	2					
	-40°C to 105°C			8				
$I_{EN}$	EN pin input leakage current	$V_{EN} = 0\text{ V to } 5.7\text{ V}$	-40°C to 105°C			0.1	$\mu\text{A}$	
$I_{SNS}$	SNS pin input leakage current	$V_{SNS} \leq V_{BIAS}$	-40°C to 105°C			0.1	$\mu\text{A}$	
<b>RESISTANCE CHARACTERISTICS</b>								
$R_{ON}$	ON-state resistance	$I_{OUT} = -200\text{ mA}$	$V_{IN} = 5.0\text{ V}$	25°C	14	20	$\text{m}\Omega$	
				-40°C to 85°C				23
				-40°C to 105°C				24
			$V_{IN} = 3.3\text{ V}$	25°C	14	20	$\text{m}\Omega$	
				-40°C to 85°C				23
				-40°C to 105°C				24
			$V_{IN} = 1.8\text{ V}$	25°C	14	20	$\text{m}\Omega$	
				-40°C to 85°C				23
				-40°C to 105°C				24
			$V_{IN} = 1.5\text{ V}$	25°C	14	20	$\text{m}\Omega$	
				-40°C to 85°C				23
				-40°C to 105°C				24
			$V_{IN} = 1.2\text{ V}$	25°C	14	20	$\text{m}\Omega$	
				-40°C to 85°C				23
				-40°C to 105°C				24
			$V_{IN} = 0.7\text{ V}$	25°C	14	20	$\text{m}\Omega$	
				-40°C to 85°C				23
				-40°C to 105°C				24
$R_{PD}$	Output pulldown resistance (TPS22954 Only)	$V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0\text{ V}$	25°C	15	28	$\Omega$		
			-40°C to 105°C			30	$\Omega$	

## 8.7 Electrical Characteristics, $V_{BIAS} = 3.3\text{ V}$

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$  and  $V_{BIAS} = 3.3\text{ V}$ . Typical values are for  $T_A = 25\text{ }^{\circ}\text{C}$ .

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT	
<b>POWER SUPPLIES AND CURRENTS</b>								
$I_{Q, BIAS}$	BIAS quiescent current	$I_{OUT} = 0$ , $V_{IN} = 0.7\text{ V}$ to $V_{BIAS}$ , $V_{EN} = 5\text{ V}$	-40°C to 85°C	19	35		$\mu\text{A}$	
			-40°C to 105°C			37		
$I_{SD, BIAS}$	BIAS shutdown current	$V_{OUT} = 0\text{ V}$ , $V_{IN} = 0.7\text{ V}$ to $V_{BIAS}$ , $V_{EN} = 0\text{ V}$	-40°C to 85°C	4	6		$\mu\text{A}$	
			-40°C to 105°C			7	$\mu\text{A}$	
$I_{SD, IN}$	Input shutdown current	$V_{EN} = 0\text{ V}$ , $V_{OUT} = 0\text{ V}$	$V_{IN} = 3.3\text{ V}$	-40°C to 85°C	0.01	3	$\mu\text{A}$	
				-40°C to 105°C				10
			$V_{IN} = 1.8\text{ V}$	-40°C to 85°C	0.01	3		
				-40°C to 105°C				10
			$V_{IN} = 1.2\text{ V}$	-40°C to 85°C	0.01	2		
				-40°C to 105°C				8
			$V_{IN} = 0.7\text{ V}$	-40°C to 85°C	0.01	2		
				-40°C to 105°C				8
$I_{EN}$	EN pin input leakage current	$V_{EN} = 0\text{ V}$ to $5.7\text{ V}$	-40°C to 105°C			0.1	$\mu\text{A}$	
$I_{SNS}$	SNS pin input leakage current	$V_{SNS} = 0\text{ V}$ to $V_{BIAS}$	-40°C to 105°C			0.1	$\mu\text{A}$	
<b>RESISTANCE CHARACTERISTICS</b>								
$R_{ON}$	ON-state resistance	$I_{OUT} = -200\text{ mA}$	$V_{IN} = 3.3\text{ V}$	25°C	15	21	$\text{m}\Omega$	
				-40°C to 85°C				24
				-40°C to 105°C				25
			$V_{IN} = 1.8\text{ V}$	25°C	14	20	$\text{m}\Omega$	
				-40°C to 85°C				23
				-40°C to 105°C				24
			$V_{IN} = 1.5\text{ V}$	25°C	14	20	$\text{m}\Omega$	
				-40°C to 85°C				23
				-40°C to 105°C				24
			$V_{IN} = 1.2\text{ V}$	25°C	14	20	$\text{m}\Omega$	
				-40°C to 85°C				23
				-40°C to 105°C				24
$V_{IN} = 0.7\text{ V}$	25°C	14	20	$\text{m}\Omega$				
	-40°C to 85°C				23			
	-40°C to 105°C				24			
$R_{PD}$	Output pulldown resistance (TPS22954 Only)	$V_{IN} = V_{OUT} = V_{BIAS}$ , $V_{EN} = 0\text{ V}$	25°C	13	28	$\Omega$		
			-40°C to 105°C			30	$\Omega$	

## 8.8 Electrical Characteristics, $V_{BIAS} = 2.5\text{ V}$

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$  and  $V_{BIAS} = 2.5\text{ V}$ . Typical values are for  $T_A = 25\text{ }^{\circ}\text{C}$ .

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT	
<b>POWER SUPPLIES AND CURRENTS</b>								
$I_{Q, BIAS}$	BIAS quiescent current	$I_{OUT} = 0, V_{IN} = 0.7\text{ V to } V_{BIAS}, V_{EN} = 5\text{ V}$	-40°C to 85°C	16	25		$\mu\text{A}$	
			-40°C to 105°C			27		
$I_{SD, BIAS}$	BIAS shutdown current	$V_{OUT} = 0\text{ V}, V_{IN} = 0.7\text{ V to } V_{BIAS}, V_{EN} = 0\text{ V}$	-40°C to 85°C	4	5		$\mu\text{A}$	
			-40°C to 105°C			6	$\mu\text{A}$	
$I_{SD, IN}$	Input shutdown current	$V_{EN} = 0\text{ V}, V_{OUT} = 0\text{ V}$	$V_{IN} = 2.5\text{ V}$	-40°C to 85°C	0.01	3	$\mu\text{A}$	
				-40°C to 105°C				10
			$V_{IN} = 1.8\text{ V}$	-40°C to 85°C	0.01	3		
				-40°C to 105°C				10
			$V_{IN} = 1.2\text{ V}$	-40°C to 85°C	0.01	2		
				-40°C to 105°C				8
			$V_{IN} = 0.7\text{ V}$	-40°C to 85°C	0.01	2		
				-40°C to 105°C				8
$I_{EN}$	EN pin input leakage current	$V_{EN} = 0\text{ V to } 5.7\text{ V}$	-40°C to 105°C			0.1	$\mu\text{A}$	
$I_{SNS}$	SNS pin input leakage current	$V_{SNS} = 0\text{ V to } V_{BIAS}$	-40°C to 105°C			0.1	$\mu\text{A}$	
<b>RESISTANCE CHARACTERISTICS</b>								
$R_{ON}$	ON-state resistance	$I_{OUT} = -200\text{ mA}$	$V_{IN} = 2.5\text{ V}$	25°C	16	23	$\text{m}\Omega$	
				-40°C to 85°C				26
				-40°C to 105°C				27
			$V_{IN} = 1.8\text{ V}$	25°C	15	22	$\text{m}\Omega$	
				-40°C to 85°C				25
				-40°C to 105°C				26
			$V_{IN} = 1.5\text{ V}$	25°C	15	22	$\text{m}\Omega$	
				-40°C to 85°C				25
			$V_{IN} = 1.2\text{ V}$	-40°C to 105°C			26	
				25°C	15	22	$\text{m}\Omega$	
				-40°C to 85°C				24
			-40°C to 105°C			25		
$V_{IN} = 0.7\text{ V}$	25°C	14	21	$\text{m}\Omega$				
	-40°C to 85°C				24			
	-40°C to 105°C				25			
$R_{PD}$	Output pulldown resistance (TPS22954 Only)	$V_{IN} = V_{OUT} = V_{BIAS}, V_{EN} = 0\text{ V}$	25°C	12	28	$\Omega$		
			-40°C to 105°C			30	$\Omega$	

## 8.9 Switching Characteristics, CT = 1000 pF

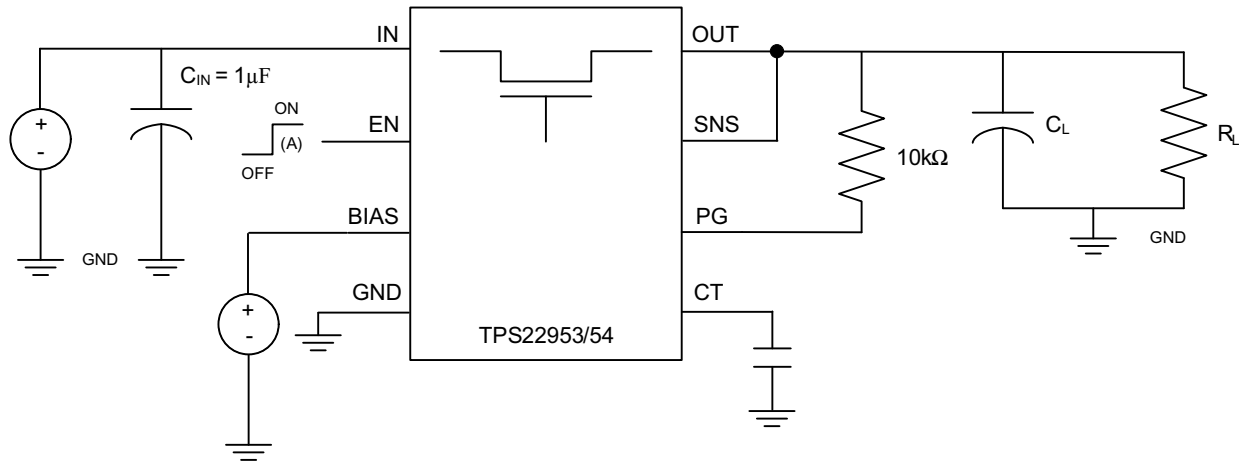
Refer to the timing test circuit in Figure 1 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where  $V_{IN}$  and  $V_{BIAS}$  are already in steady state condition before the EN terminal is asserted high.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b><math>V_{IN} = 5V, V_{EN} = V_{BIAS} = 5V, T_A = 25^\circ C</math></b>					
$t_{ON}$ Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 1000 pF$		1265		$\mu s$
$t_{OFF}$ Turn-off time			6.0		
$t_R$ $V_{OUT}$ rise time			1492		
$t_F$ $V_{OUT}$ fall time			2.2		
$t_D$ ON delay time			519		
<b><math>V_{IN} = 2.5V, V_{EN} = V_{BIAS} = 5V, T_A = 25^\circ C</math></b>					
$t_{ON}$ Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 1000 pF$		813		$\mu s$
$t_{OFF}$ Turn-off time			6.1		
$t_R$ $V_{OUT}$ rise time			765		
$t_F$ $V_{OUT}$ fall time			2.2		
$t_D$ ON delay time			430		
<b><math>V_{IN} = 0.7V, V_{EN} = V_{BIAS} = 5V, T_A = 25^\circ C</math></b>					
$t_{ON}$ Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 1000 pF$		476		$\mu s$
$t_{OFF}$ Turn-off time			6.2		
$t_R$ $V_{OUT}$ rise time			245		
$t_F$ $V_{OUT}$ fall time			2.1		
$t_D$ ON delay time			353		
<b><math>V_{IN} = 2.5V, V_{EN} = 5V, V_{BIAS} = 2.5V, T_A = 25^\circ C</math></b>					
$t_{ON}$ Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 1000 pF$		813		$\mu s$
$t_{OFF}$ Turn-off time			4.9		
$t_R$ $V_{OUT}$ rise time			765		
$t_F$ $V_{OUT}$ fall time			2.2		
$t_D$ ON delay time			430		
<b><math>V_{IN} = 0.7V, V_{EN} = 5V, V_{BIAS} = 2.5V, T_A = 25^\circ C</math></b>					
$t_{ON}$ Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 1000 pF$		476		$\mu s$
$t_{OFF}$ Turn-off time			6.1		
$t_R$ $V_{OUT}$ rise time			245		
$t_F$ $V_{OUT}$ fall time			2.1		
$t_D$ ON delay time			353		

## 8.10 Switching Characteristics, CT = 0 pF

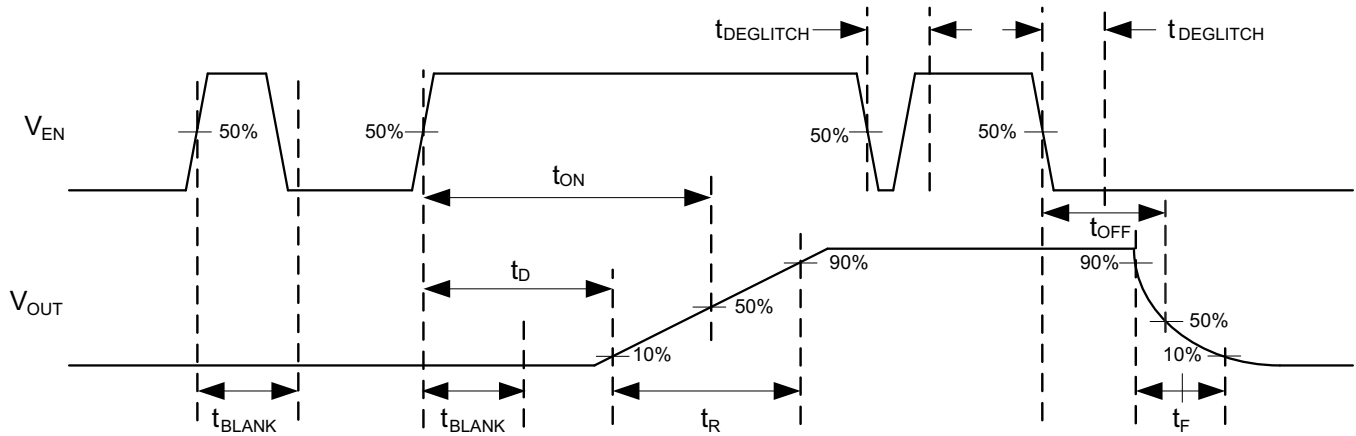
Refer to the timing test circuit in Figure 1 (unless otherwise noted) for references to external components used for the test condition in the switching characteristics table. Switching characteristics shown below are only valid for the power-up sequence where  $V_{IN}$  and  $V_{BIAS}$  are already in steady state condition before the EN terminal is asserted high.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
<b><math>V_{IN} = 5V, V_{EN} = V_{BIAS} = 5V, T_A = 25^\circ C</math></b>						
$t_{ON}$	Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 0 pF$		235		$\mu s$
$t_{OFF}$	Turn-off time			6.0		
$t_R$	$V_{OUT}$ rise time			140		
$t_F$	$V_{OUT}$ fall time			2.2		
$t_D$	ON delay time			165		
<b><math>V_{IN} = 2.5V, V_{EN} = V_{BIAS} = 5V, T_A = 25^\circ C</math></b>						
$t_{ON}$	Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 0 pF$		200		$\mu s$
$t_{OFF}$	Turn-off time			6		
$t_R$	$V_{OUT}$ rise time			79		
$t_F$	$V_{OUT}$ fall time			2.1		
$t_D$	ON delay time			160		
<b><math>V_{IN} = 0.7V, V_{EN} = V_{BIAS} = 5V, T_A = 25^\circ C</math></b>						
$t_{ON}$	Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 0 pF$		170		$\mu s$
$t_{OFF}$	Turn-off time			6		
$t_R$	$V_{OUT}$ rise time			32		
$t_F$	$V_{OUT}$ fall time			2		
$t_D$	ON delay time			154		
<b><math>V_{IN} = 2.5V, V_{EN} = 5V, V_{BIAS} = 2.5V, T_A = 25^\circ C</math></b>						
$t_{ON}$	Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 0 pF$		200		$\mu s$
$t_{OFF}$	Turn-off time			6		
$t_R$	$V_{OUT}$ rise time			79		
$t_F$	$V_{OUT}$ fall time			2.1		
$t_D$	ON delay time			160		
<b><math>V_{IN} = 0.7V, V_{EN} = 5V, V_{BIAS} = 2.5V, T_A = 25^\circ C</math></b>						
$t_{ON}$	Turn-on time	$R_L = 10 \Omega, C_L = 0.1 \mu F, CT = 0 pF$		170		$\mu s$
$t_{OFF}$	Turn-off time			6		
$t_R$	$V_{OUT}$ rise time			32		
$t_F$	$V_{OUT}$ fall time			2		
$t_D$	ON delay time			154		



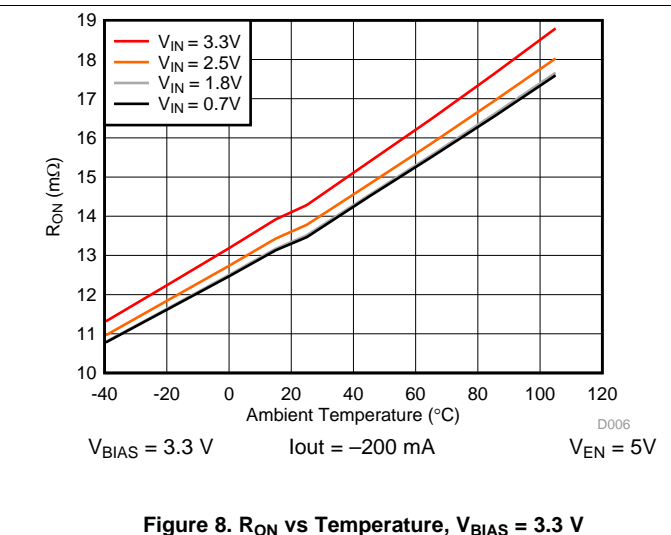
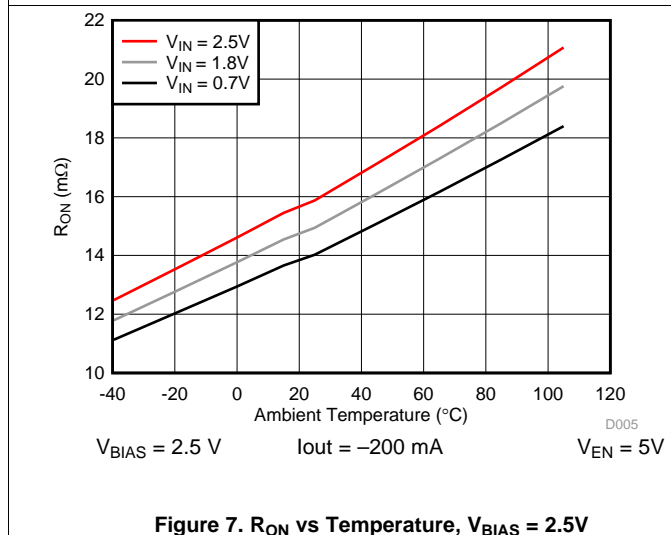
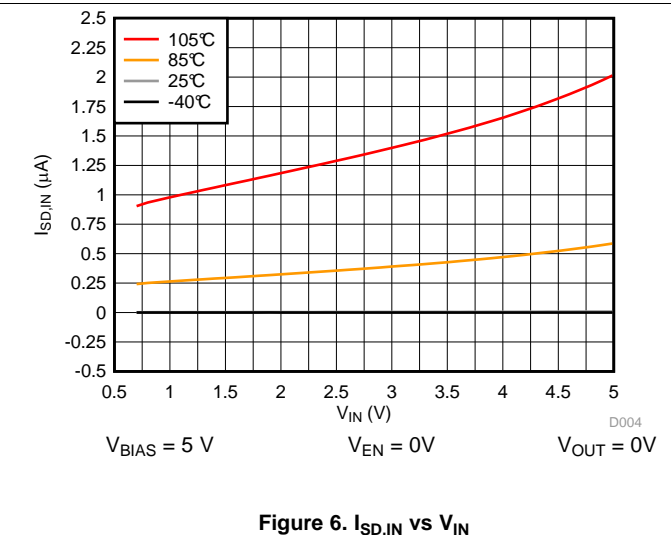
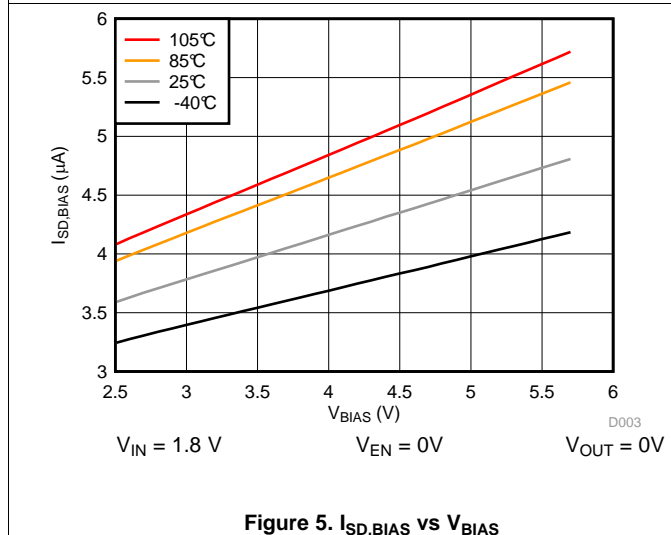
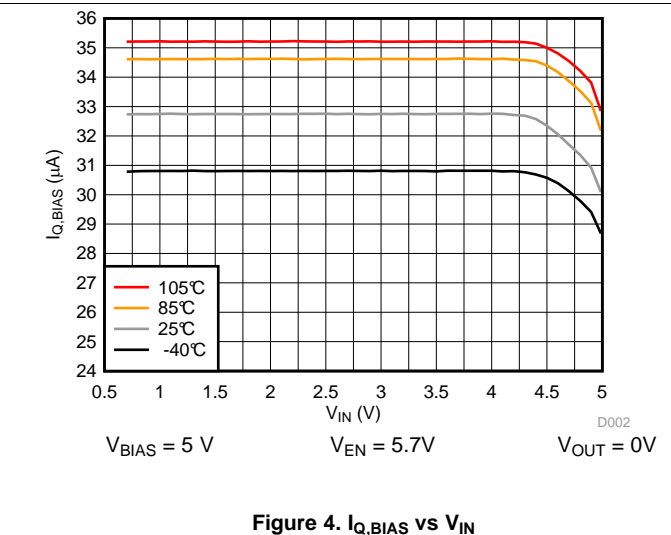
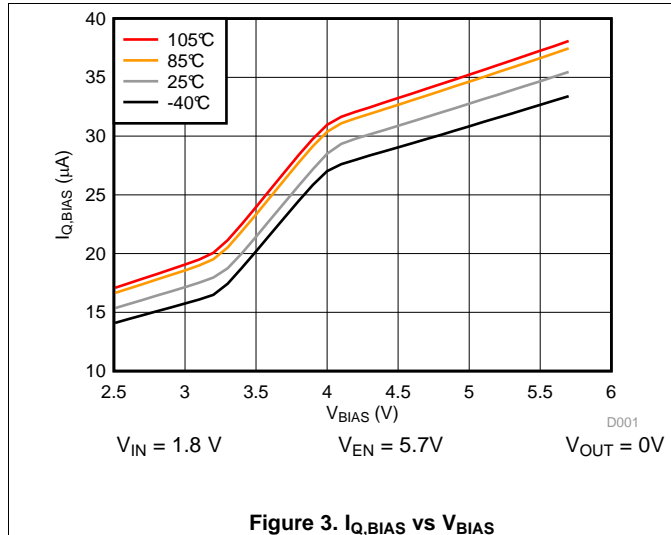
A. Rise and fall times of the control signal is 100 ns.

**Figure 1. Timing Test Circuit**



**Figure 2. Timing Waveforms**

### 8.11 Typical DC Characteristics



Typical DC Characteristics (continued)

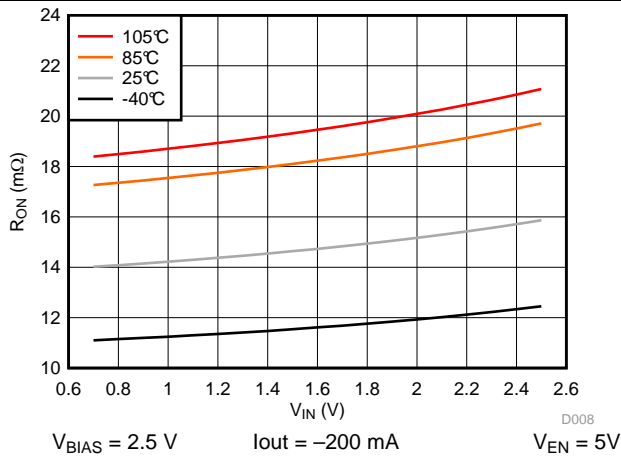


Figure 9.  $R_{ON}$  vs  $V_{IN}$ ,  $V_{BIAS} = 2.5\text{ V}$

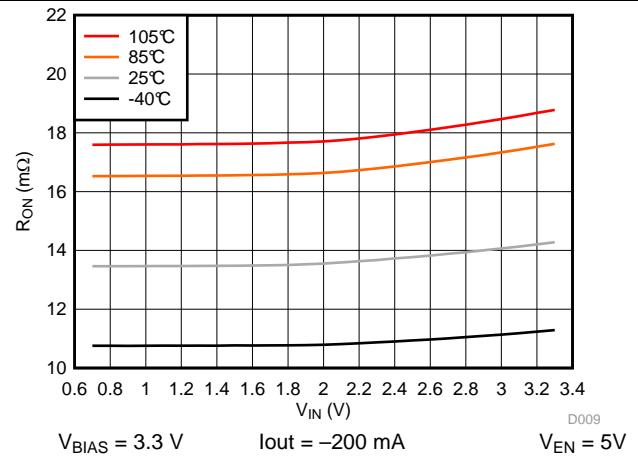


Figure 10.  $R_{ON}$  vs  $V_{IN}$ ,  $V_{BIAS} = 3.3\text{ V}$

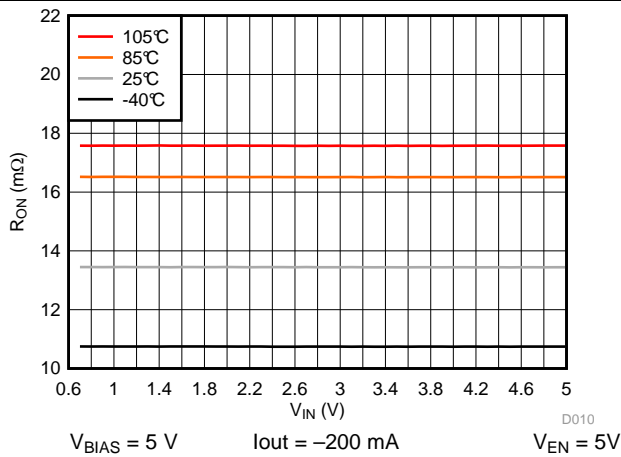


Figure 11.  $R_{ON}$  vs  $V_{IN}$ ,  $V_{BIAS} = 5\text{ V}$

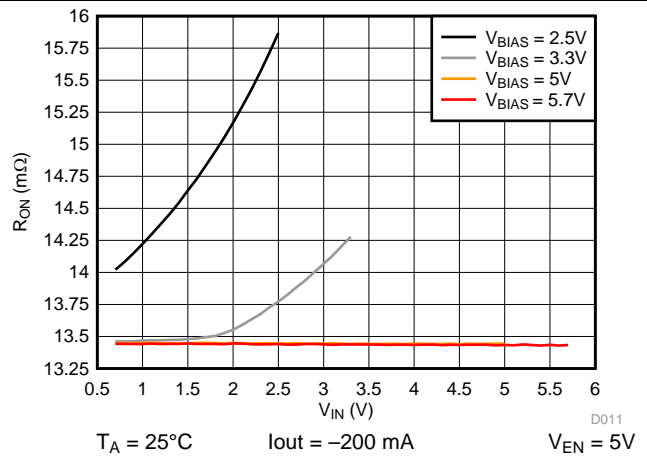


Figure 12.  $R_{ON}$  vs  $V_{IN}$

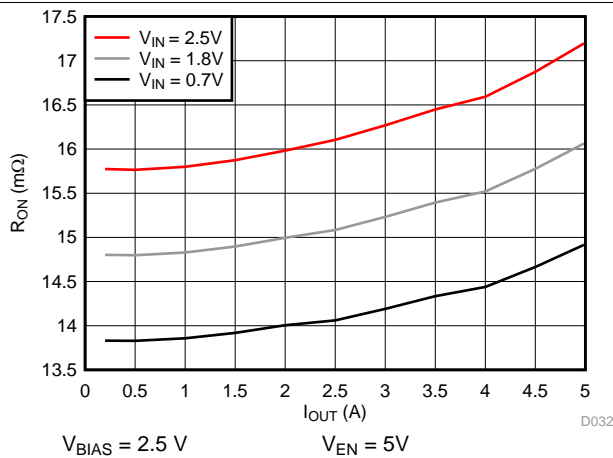


Figure 13.  $R_{ON}$  vs  $I_{OUT}$ ,  $V_{BIAS} = 2.5\text{ V}$

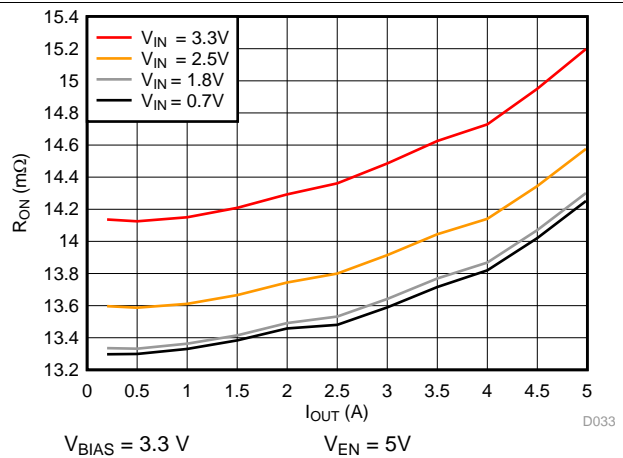


Figure 14.  $R_{ON}$  vs  $I_{OUT}$ ,  $V_{BIAS} = 3.3\text{ V}$

Typical DC Characteristics (continued)

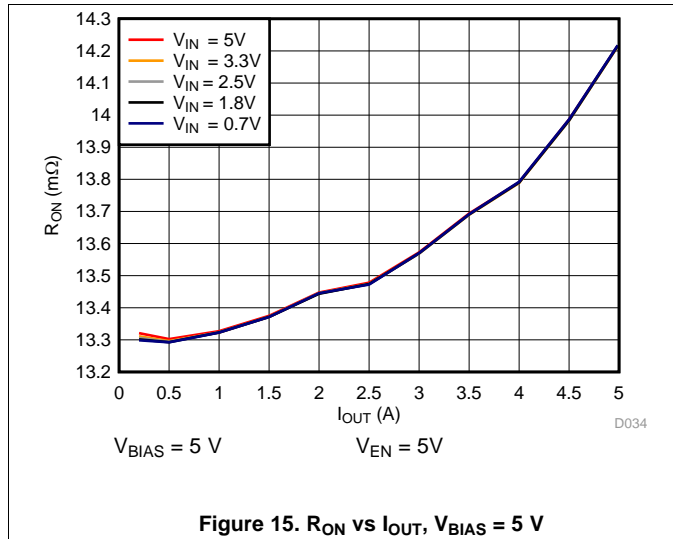


Figure 15.  $R_{ON}$  vs  $I_{OUT}$ ,  $V_{BIAS} = 5\text{ V}$

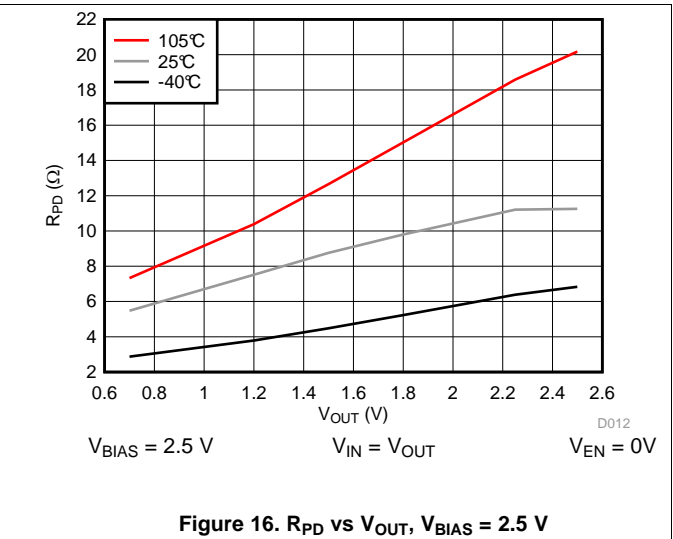


Figure 16.  $R_{PD}$  vs  $V_{OUT}$ ,  $V_{BIAS} = 2.5\text{ V}$

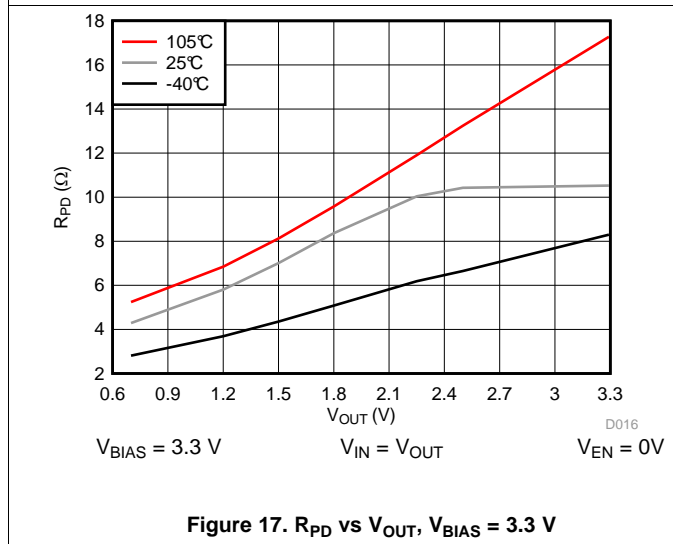


Figure 17.  $R_{PD}$  vs  $V_{OUT}$ ,  $V_{BIAS} = 3.3\text{ V}$

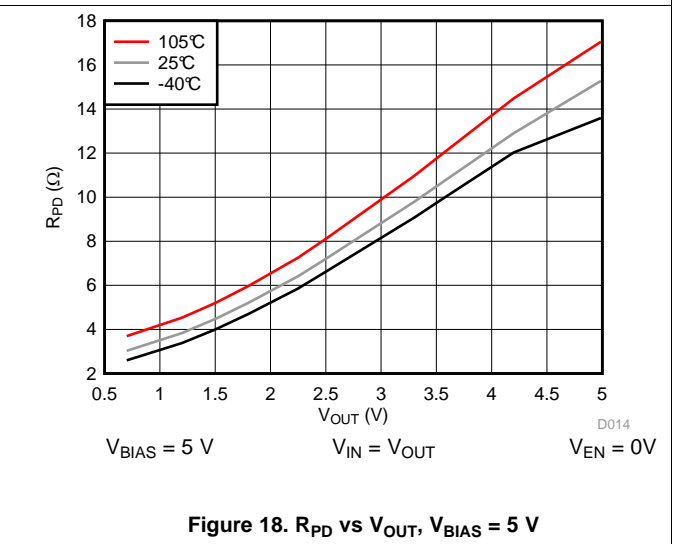


Figure 18.  $R_{PD}$  vs  $V_{OUT}$ ,  $V_{BIAS} = 5\text{ V}$

### 8.12 Typical Switching Characteristics

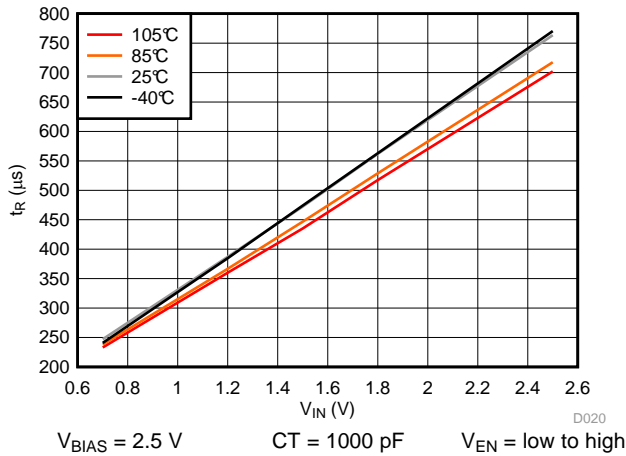


Figure 19.  $t_R$  vs  $V_{IN}$ ,  $V_{BIAS} = 2.5$  V

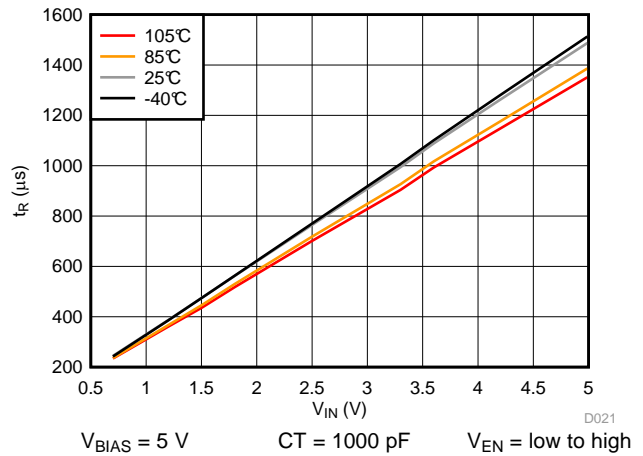


Figure 20.  $t_R$  vs  $V_{IN}$ ,  $V_{BIAS} = 5$  V

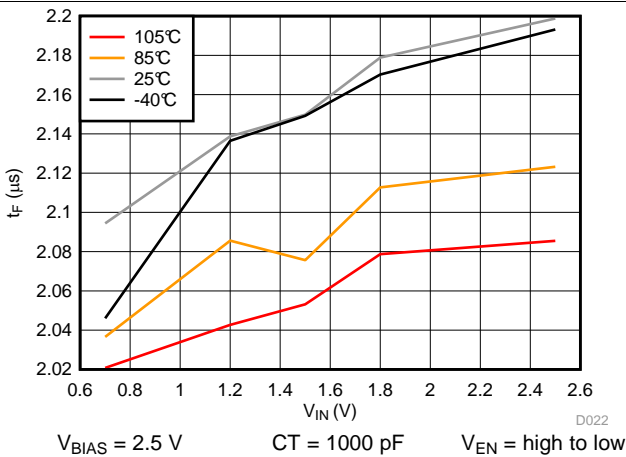


Figure 21.  $t_F$  vs  $V_{IN}$ ,  $V_{BIAS} = 2.5$  V

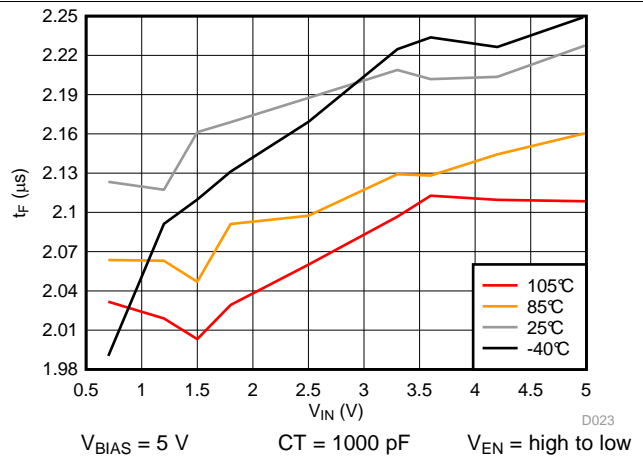


Figure 22.  $t_F$  vs  $V_{IN}$ ,  $V_{BIAS} = 5$  V

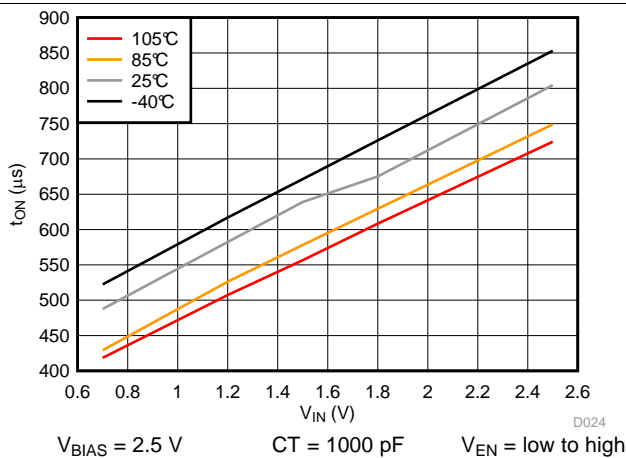


Figure 23.  $t_{ON}$  vs  $V_{IN}$ ,  $V_{BIAS} = 2.5$  V

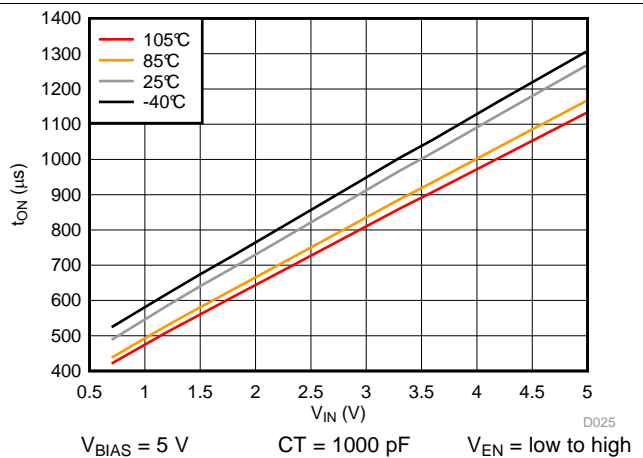
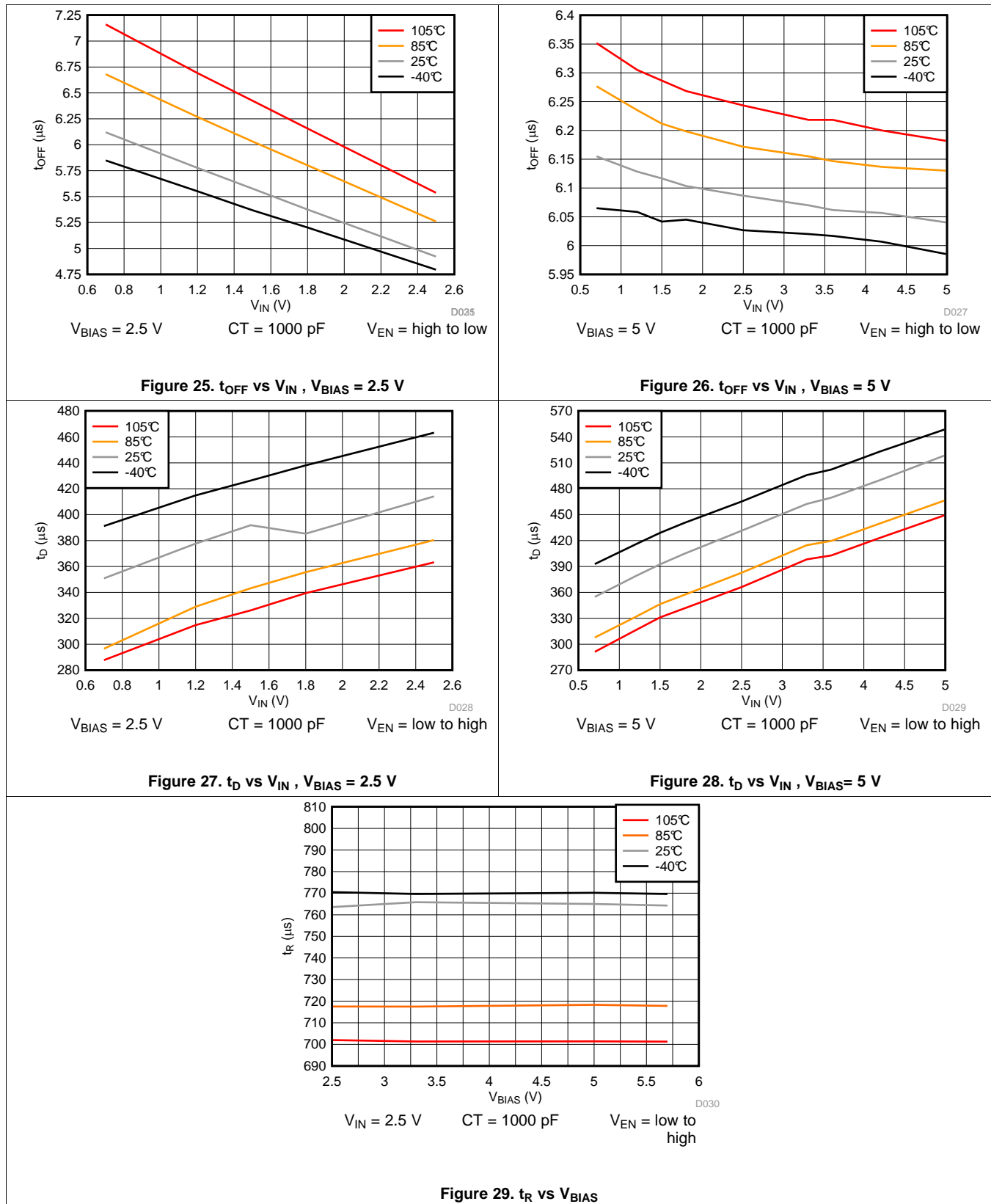


Figure 24.  $t_{ON}$  vs  $V_{IN}$ ,  $V_{BIAS} = 5$  V

Typical Switching Characteristics (continued)



Typical Switching Characteristics (continued)

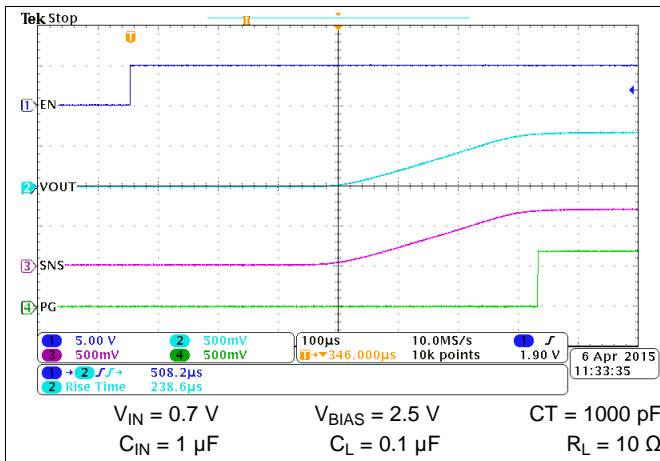


Figure 30. Turn On Waveform,  $V_{BIAS} = 2.5\text{ V}$

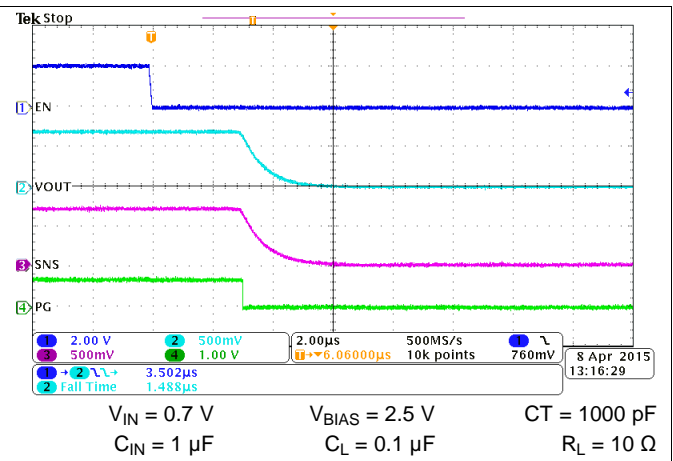


Figure 31. Turn Off Waveform,  $V_{BIAS} = 2.5\text{ V}$

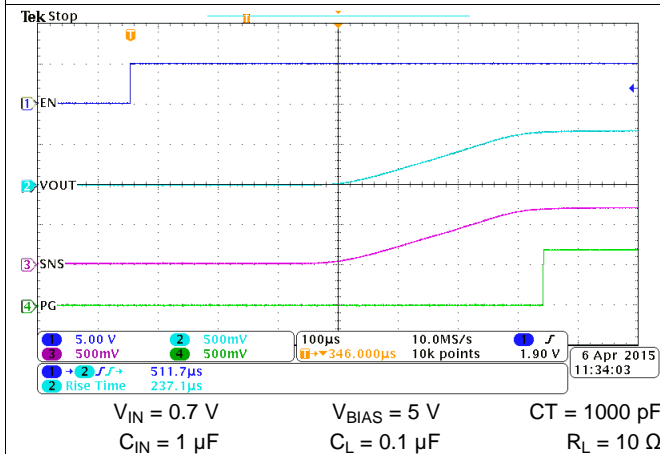


Figure 32. Turn On Waveform,  $V_{BIAS} = 5\text{ V}$

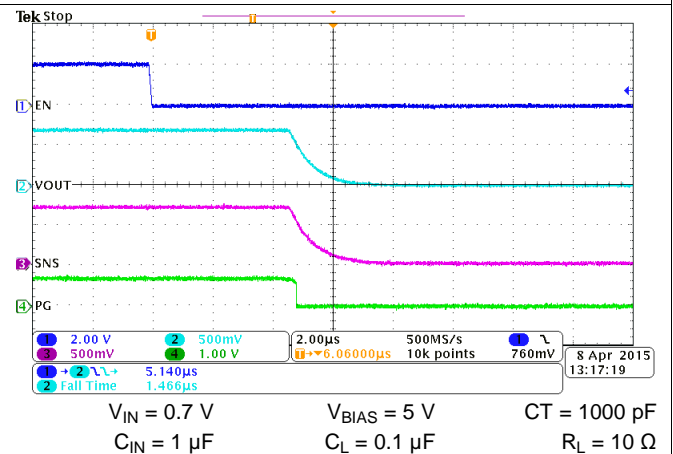


Figure 33. Turn Off Waveform,  $V_{BIAS} = 5\text{ V}$

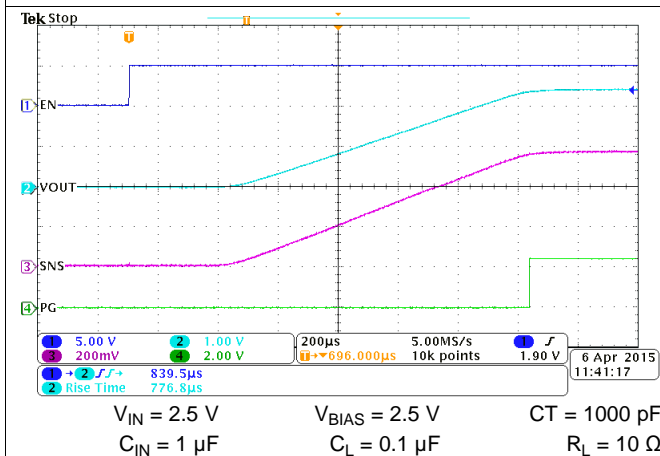


Figure 34. Turn On Waveform,  $V_{BIAS} = 2.5\text{ V}$

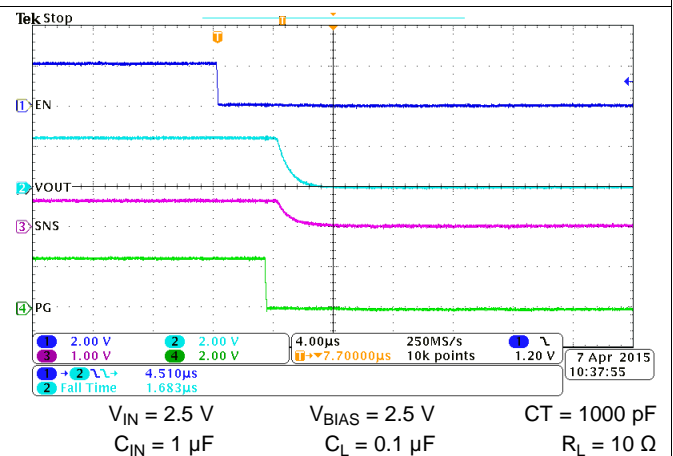


Figure 35. Turn Off Waveform,  $V_{BIAS} = 2.5\text{ V}$

Typical Switching Characteristics (continued)

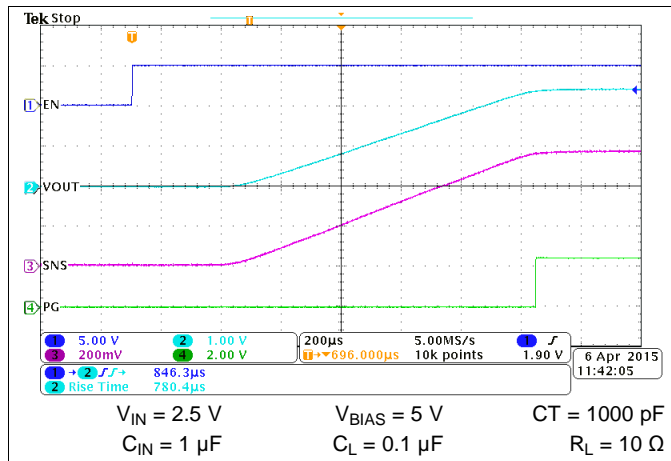


Figure 36. Turn On Waveform,  $V_{BIAS} = 5\text{ V}$

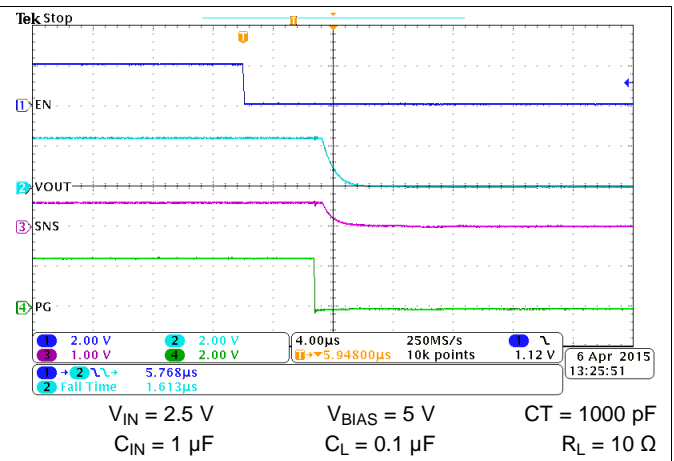


Figure 37. Turn Off Waveform,  $V_{BIAS} = 5\text{ V}$

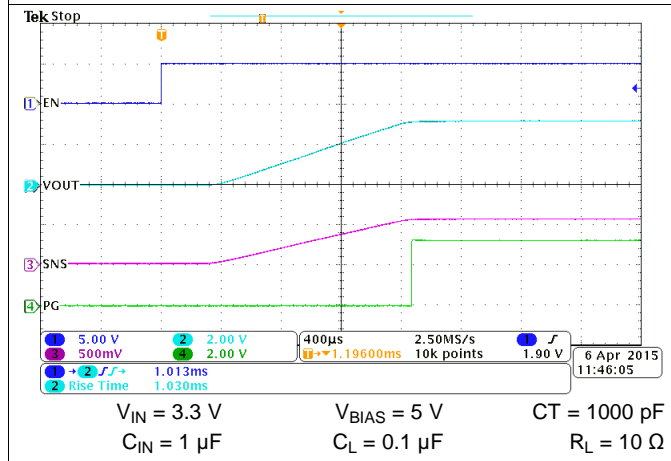


Figure 38. Turn On Waveform,  $V_{BIAS} = 5\text{ V}$

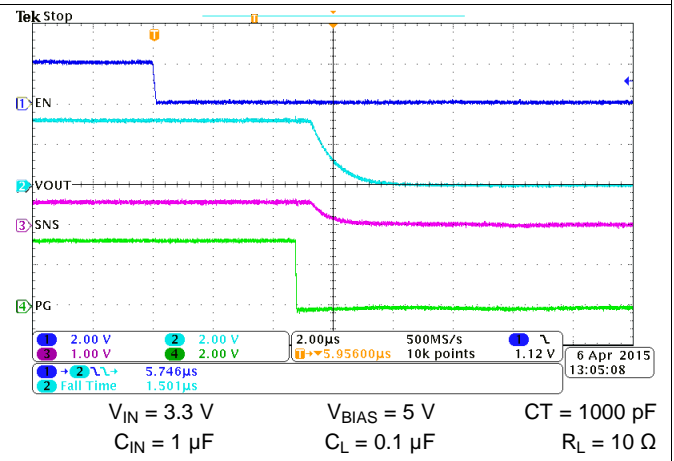


Figure 39. Turn Off Waveform,  $V_{BIAS} = 5\text{ V}$

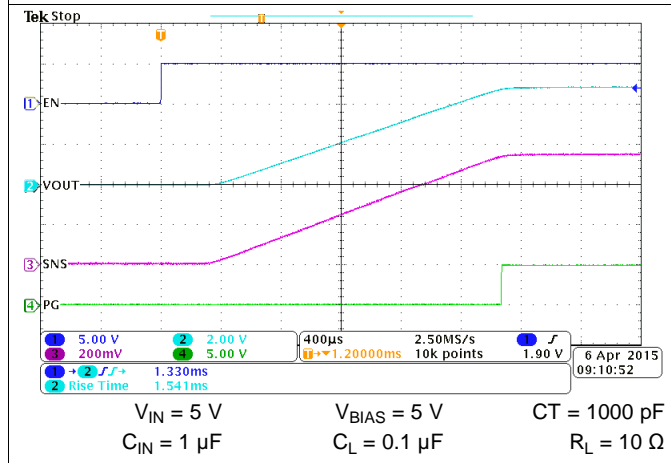


Figure 40. Turn On Waveform,  $V_{BIAS} = 5\text{ V}$

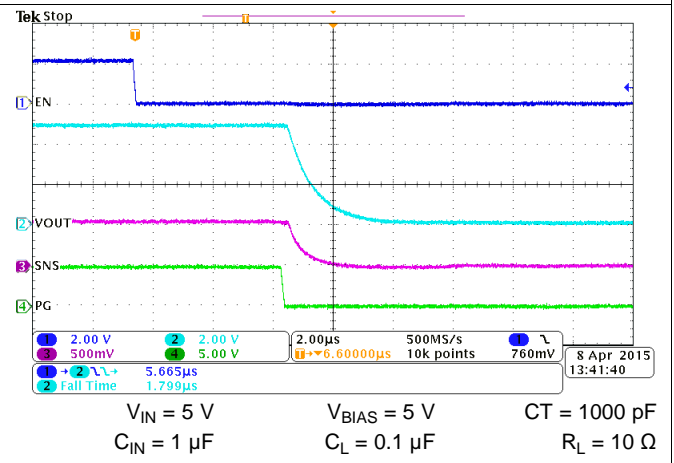


Figure 41. Turn Off Waveform,  $V_{BIAS} = 5\text{ V}$

Typical Switching Characteristics (continued)

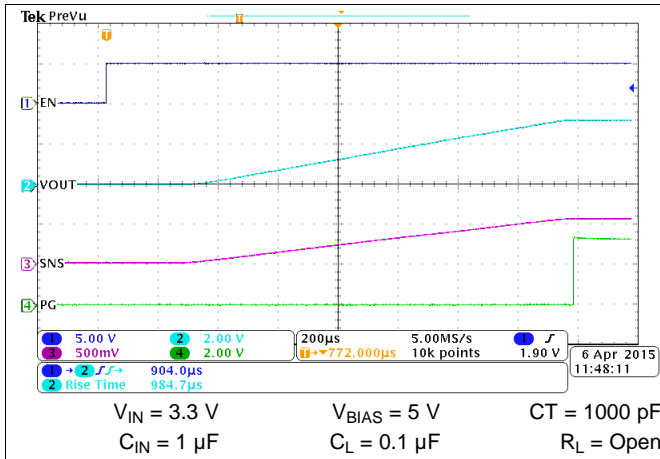


Figure 42. Turn On Waveform, No Load

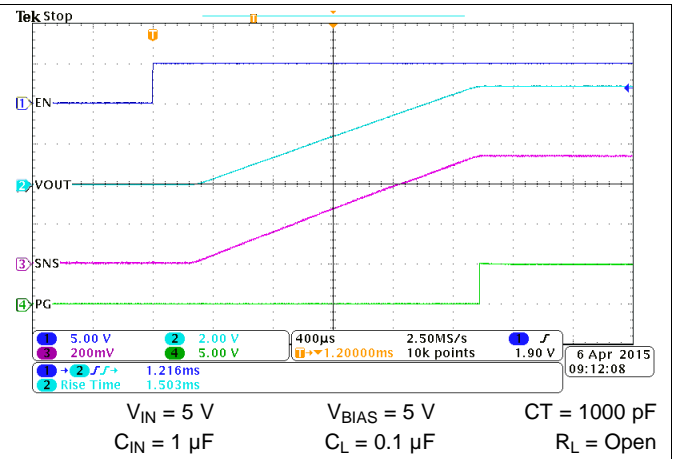


Figure 43. Turn On Waveform, No Load

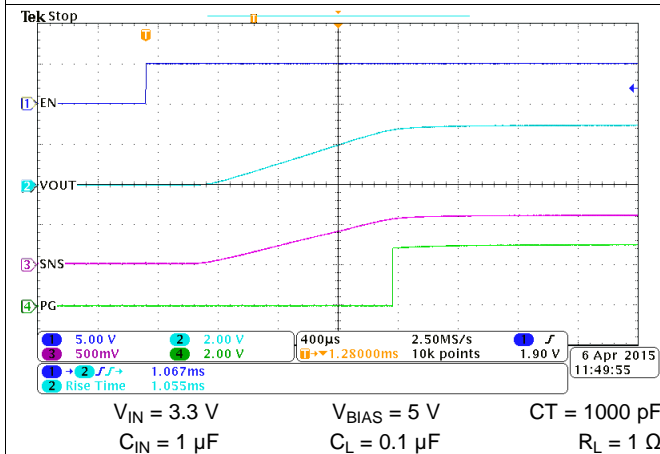


Figure 44. Turn On Waveform, Heavy Load

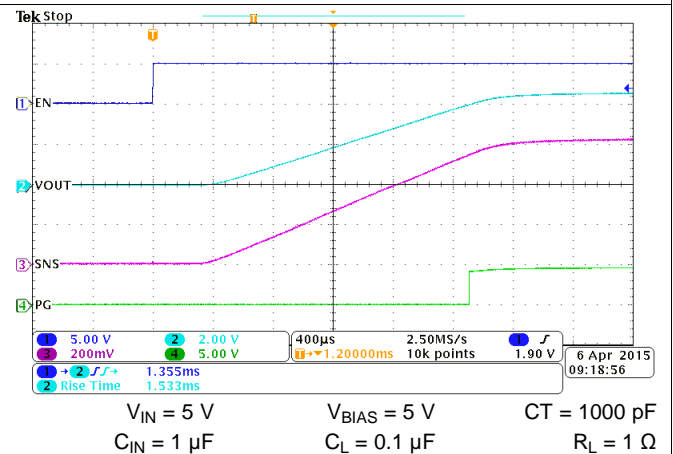


Figure 45. Turn On Waveform, Heavy Load

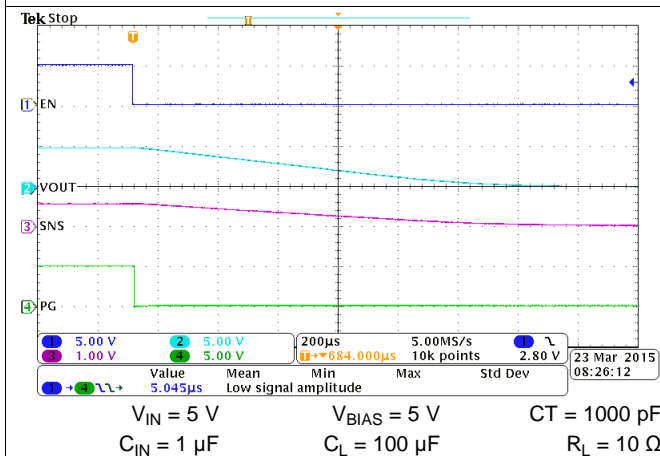


Figure 46. PG Response to EN Falling ( $t_{DEGLITCH}$ )

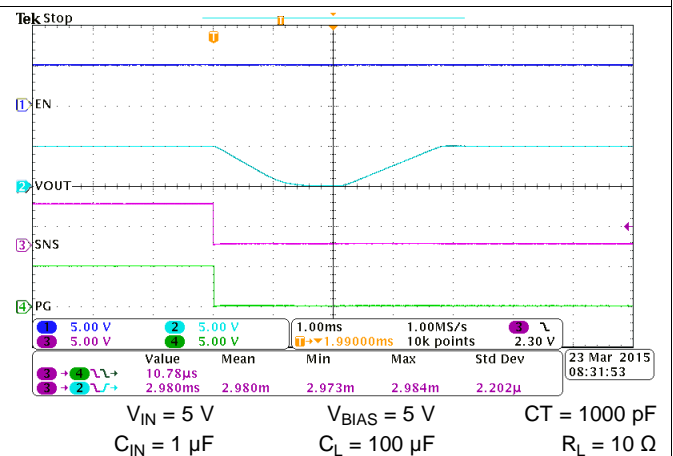
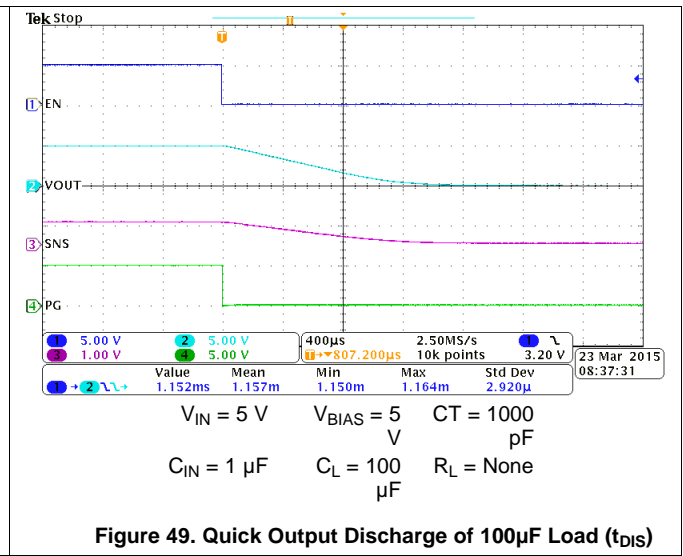
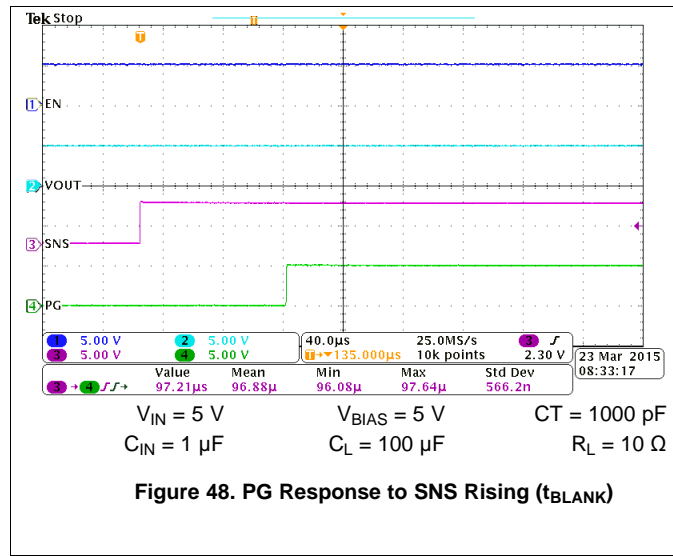


Figure 47. PG Response to SNS Falling with Auto-Restart ( $t_{DEGLITCH}$  and  $t_{RESTART}$ )

Typical Switching Characteristics (continued)



## 9 Detailed Description

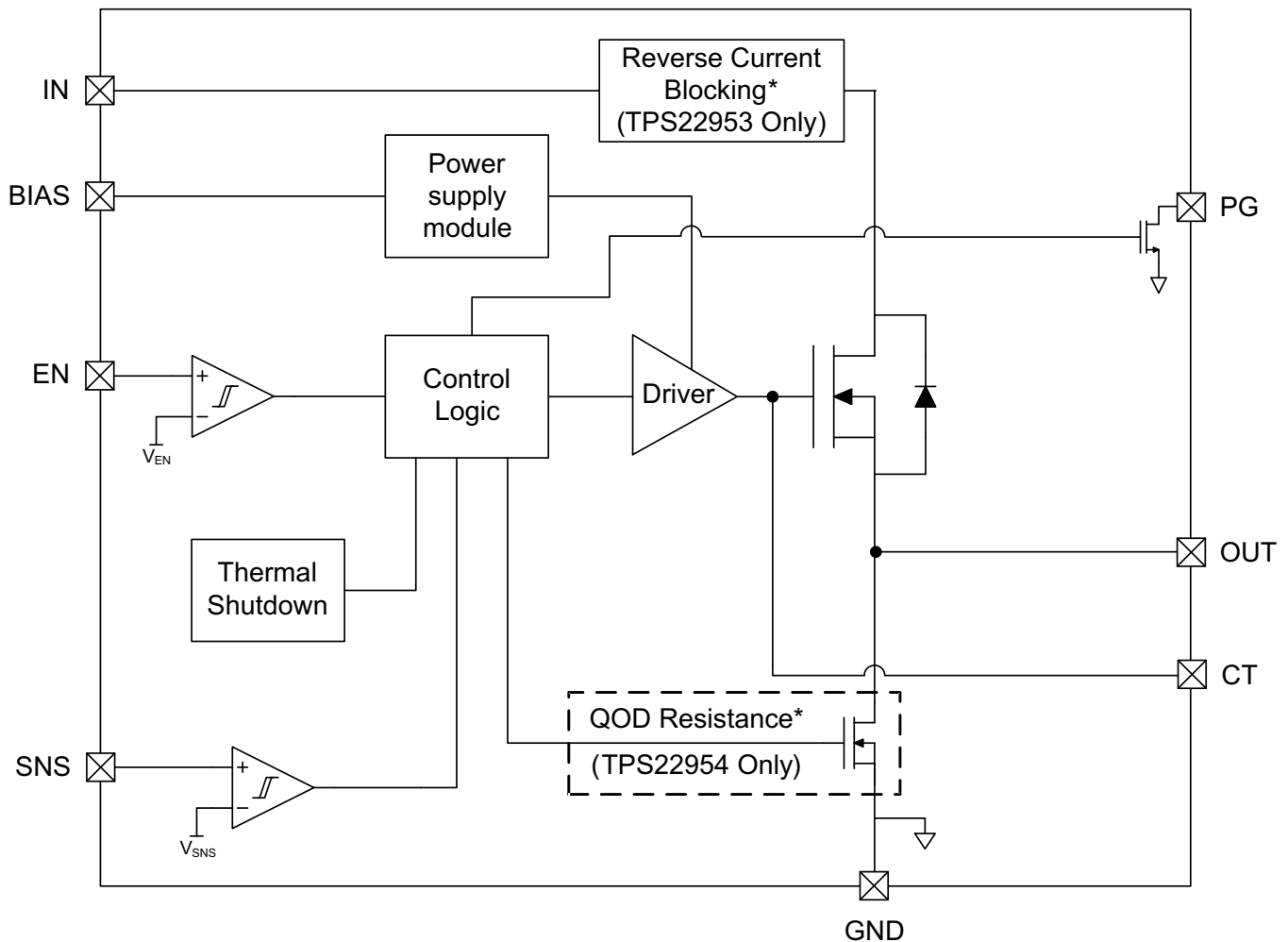
### 9.1 Overview

The TPS22953/4 are 5.7-V, 5-A load switches in 10-pin SON packages. To reduce voltage drop for low voltage, high current rails the device implements a low resistance N-channel MOSFET, which reduces the drop out voltage through the device at high currents. The integrated adjustable undervoltage lockout (UVLO) and adjustable power good (PG) threshold provides voltage monitoring as well as robust power sequencing.

The adjustable rise time control of the device greatly reduces inrush current for a wide variety of bulk load capacitances, thereby reducing or eliminating power supply droop. The switch is independently controlled by an on/off input (EN), which is capable of interfacing directly with low-voltage control signals. A 15  $\Omega$  on-chip load resistor is integrated into the device for output quick discharge when switch is turned off.

During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream modules during standby. Integrated power monitoring functionality, control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and BOM count.

### 9.2 Functional Block Diagram



(\*) Only active when the switch is disabled.

## 9.3 Feature Description

### 9.3.1 On/Off Control (EN pin)

The EN pin controls the state of the switch. When the voltage on EN has exceeded  $V_{IH,EN}$  the switch will be enabled. When EN goes below  $V_{IL,EN}$  the switch is disabled.

The EN pin has a blanking time of  $t_{BLANK}$  on the rising edge once the  $V_{IH,EN}$  threshold has been exceeded. It also has a deglitch time of  $t_{DEGLITCH}$  when the voltage has gone below  $V_{IL,EN}$ .

The EN pin can also be configured via an external resistor divider to monitor a voltage signal for input UVLO. Refer to the equation and diagram below on how to configure the EN pin for input UVLO.

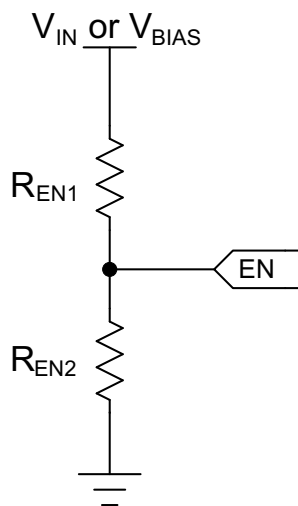
$$V_{IH,EN} = V_{IN} \times \frac{R_{EN2}}{R_{EN1} + R_{EN2}} \quad (1)$$

Where:

$V_{IH,EN}$  = the rising threshold of the EN pin (see [Electrical Characteristics](#) table)

$V_{IN}$  = the input voltage being monitored (this could be  $V_{IN}$ ,  $V_{BIAS}$ , or an external power supply)

$R_{EN1}$ ,  $R_{EN2}$  = resistor divider values



## Feature Description (continued)

### 9.3.2 Voltage Monitoring (SNS pin)

The SNS pin of the device can be used to monitor the output voltage of the device or another voltage rail. The pin can be configured with an external resistor divider to set the desired trip point for the voltage being monitored or be tied to OUT directly. If the voltage on the SNS pin exceeds  $V_{IH,SNS}$ , the voltage being monitored on the SNS pin is considered to be valid high. The voltage on the SNS pin must be greater than  $V_{IH,SNS}$  for at least  $t_{BLANK}$  before PG is asserted high. If the voltage on the SNS pin goes below  $V_{IL,SNS}$ , then the switch will power cycle (i.e., the switch will be disabled and re-enabled). For proper functionality of the device, this pin must not be left floating. If a resistor divider is not being used for voltage sensing, this pin can be tied directly to  $V_{OUT}$ .

The SNS pin has a blanking time of  $t_{BLANK}$  on the rising edge once the  $V_{IH,SNS}$  threshold has been exceeded. It has a deglitch time of  $t_{DEGLITCH}$  when the voltage has gone below  $V_{IL,SNS}$ .

Refer to the equation and diagram below on how to configure the SNS pin for voltage monitoring.

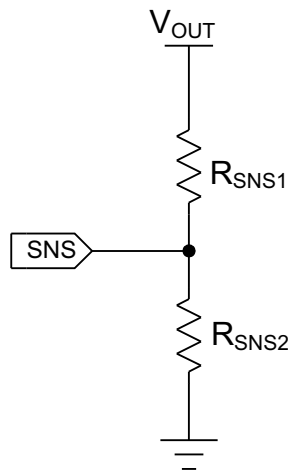
$$V_{IH,SNS} = V_{OUT} \times \frac{R_{SNS2}}{R_{SNS1} + R_{SNS2}} \quad (2)$$

Where:

$V_{IH,SNS}$  = the rising threshold of the SNS pin (see [Electrical Characteristics](#) table)

$V_{OUT}$  = voltage on the OUTpin

$R_{SNS1}$ ,  $R_{SNS2}$  = resistor divider values



## Feature Description (continued)

### 9.3.3 Power Good (PG Pin)

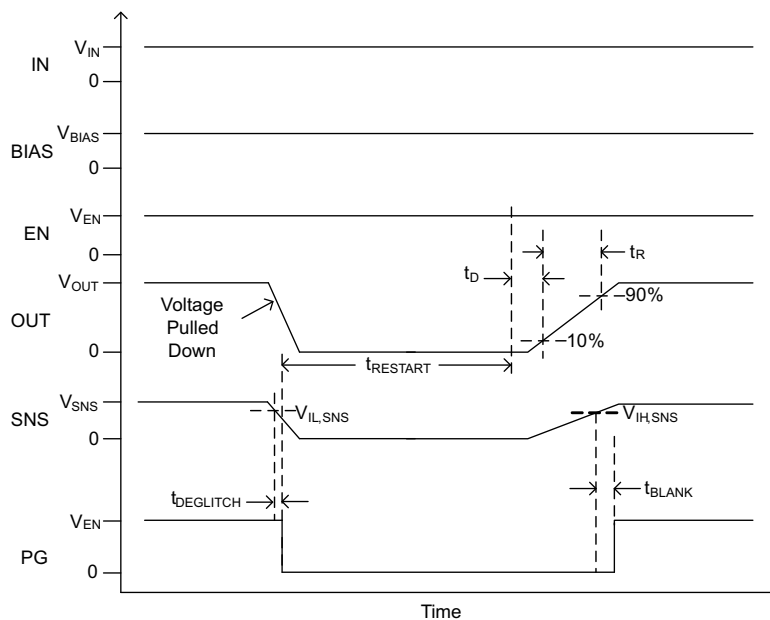
The PG pin is only asserted high when the voltage on EN has exceeded  $V_{IH,EN}$  and the voltage on SNS has exceeded  $V_{IH,SNS}$ . There is a  $t_{BLANK}$  time, typically  $100\mu s$ , between the SNS voltage exceeding  $V_{IH,SNS}$  and PG being asserted high. If the voltage on EN goes below  $V_{IL,EN}$  or the voltage on SNS goes below  $V_{IL,SNS}$ , PG will be de-asserted. There is a  $t_{DEGLITCH}$  time, typically  $5\mu s$ , between the EN voltage or SNS voltage going below their respective  $V_{IL}$  levels and PG being pulled low.

PG is an open drain pin and must be pulled up with a pull-up resistor. Be sure to never exceed the maximum operating voltage on this pin. If PG is not being used in the application, tie it to GND for proper device functionality.

For proper PG operation, the BIAS voltage should be within the recommended operating range. In systems that are very sensitive to noise or have long PG traces, it is recommended to add a small capacitance from PG to GND to for decoupling.

### 9.3.4 Supervisor Fault Detection and Automatic Restart

The falling edge of the SNS pin below  $V_{IL,SNS}$  is considered a fault case and will cause the load switch to be disabled for  $t_{RESTART}$  (typically 2ms). After the  $t_{RESTART}$  time, the switch will be automatically re-enabled as long as EN is still above  $V_{IH,EN}$ . In the case the SNS pin is being used to monitor  $V_{OUT}$  or a downstream voltage, the restart will help to protect against excessive over-current if there is a quick short to GND.



**Figure 50. Automatic Restart after Quick Short to GND**

## Feature Description (continued)

### 9.3.5 Manual Restart

The falling edge of the SNS pin below  $V_{IL,SNS}$  is considered a fault case and will cause the load switch to be disabled for  $t_{RESTART}$  (typically 2ms). The SNS pin can be driven by an MCU to manually reset the load switch. After the  $t_{RESTART}$  time, the switch will be automatically re-enabled as long as EN is still above  $V_{IH,EN}$ , even if SNS is held low. The PG pin will stay low until the switch is re-enabled and the SNS pin rises above  $V_{IH,SNS}$ .

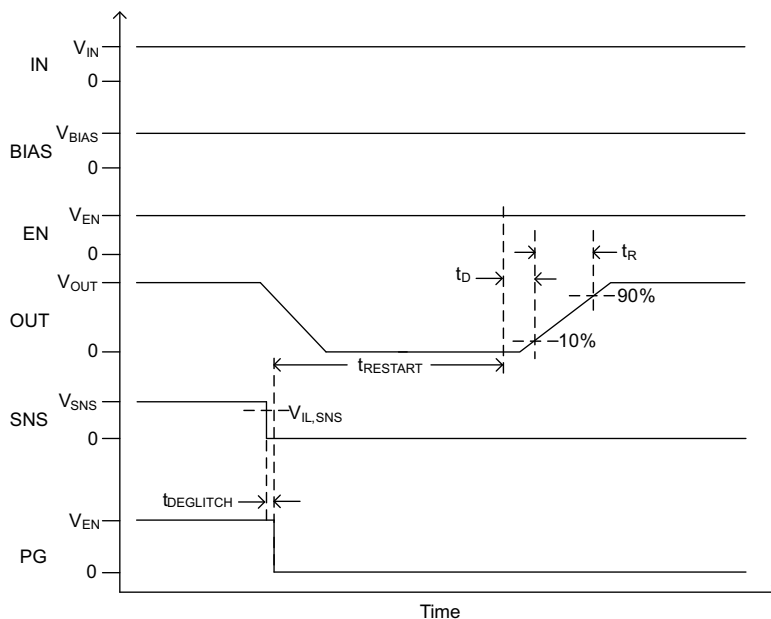


Figure 51. Manual Restart (SNS Held Low)

If the SNS pin is brought above  $V_{IH,SNS}$  within the  $t_{RESTART}$  time, the switch will still wait to re-enable. The PG pin will also stay low until  $t_{BLANK}$  after switch is re-enabled. In this case, PG will indicate when the switch is enabled and capable of being reset again.

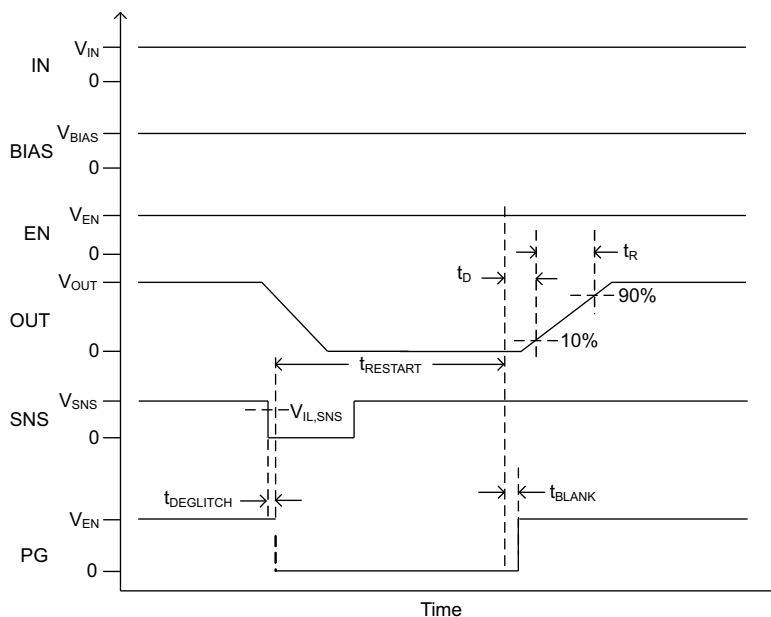


Figure 52. Manual Restart (SNS Toggled Low to High)

## Feature Description (continued)

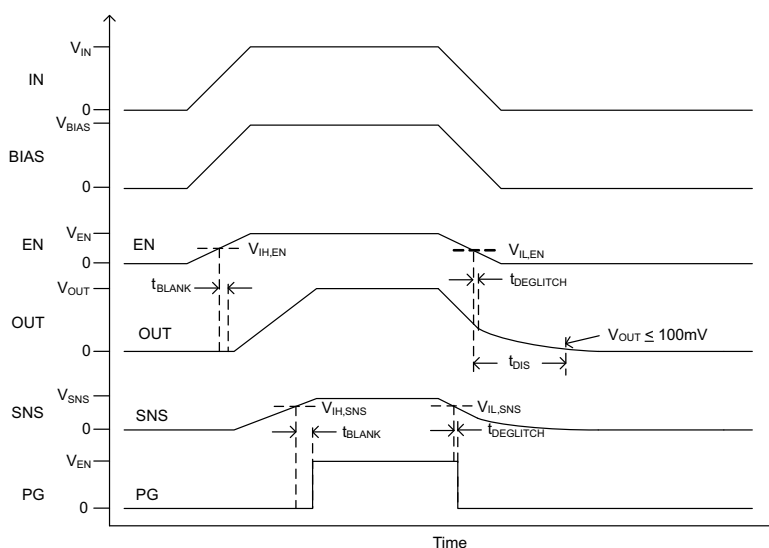
### 9.3.6 Thermal Shutdown

If the junction temperature of the device exceeds  $T_{SD}$ , the switch will be disabled. The device will be enabled once the junction temperature drops by  $TSD_{HYS}$  as long as  $EN$  is still greater than  $V_{IH,EN}$ .

### 9.3.7 Quick Output Discharge (QOD) (TPS22954 Only)

The quick output discharge (QOD) transistor is engaged indefinitely whenever the switch is disabled and the recommended  $V_{BIAS}$  voltage is met. During this state, the QOD resistance ( $R_{PD}$ ) will discharge  $V_{OUT}$  to GND. It is not recommended to apply a continuous DC voltage to OUT when the device is disabled.

The QOD transistor can remain active for a short period of time even after  $V_{BIAS}$  loses power. This brief period of time is defined as  $t_{DIS}$ . For best results, it is recommended the device get disabled before  $V_{BIAS}$  goes below the minimum recommended voltage. The waveform below shows the behaviour when power is applied and then removed in a typical application.



**Figure 53. Power Applied and then Removed in a Typical Application**

At the end of the  $t_{DIS}$  time, it is not guaranteed that  $V_{OUT}$  will be 0V since the final voltage will be dependent upon the initial voltage and the  $C_L$  capacitor. The final  $V_{OUT}$  can be calculated with the following formula for a given initial voltage and  $C_L$  capacitor.

$$V_f = V_o \times e^{\frac{-t}{RC}} \quad (3)$$

Where:

$V_f$  = final  $V_{OUT}$  voltage

$V_o$  = initial  $V_{OUT}$  voltage

$R$  = the value of the output discharge resistor,  $R_{PD}$  (see [Electrical Characteristics](#) table)

$C$  = the output bulk capacitance on OUT

### 9.3.8 $V_{IN}$ and $V_{BIAS}$ Voltage Range

For optimal  $R_{ON}$  performance, make sure  $V_{IN} \leq V_{BIAS}$ . The device will still be functional if  $V_{IN} > V_{BIAS}$  but it will exhibit  $R_{ON}$  greater than what is listed in the [Electrical Characteristics](#) table. See [Figure 50](#) for an example of a typical device. Notice the increasing  $R_{ON}$  as  $V_{IN}$  increases. Be sure to never exceed the maximum voltage rating for  $V_{IN}$  and  $V_{BIAS}$ .

## Feature Description (continued)

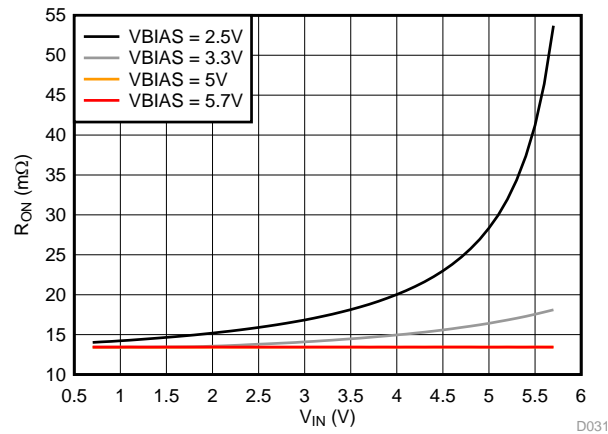


Figure 54.  $R_{ON}$  When  $V_{IN} > V_{BIAS}$

### 9.3.9 Adjustable Rise Time (CT pin)

A capacitor to GND on the CT pin sets the slew rate for  $V_{OUT}$ . An appropriate capacitance value should be placed on CT such that the  $I_{MAX}$  and  $I_{PLS}$  specifications of the device are not violated. The capacitor to GND on the CT pin should be rated for 25 V or higher. An approximate formula for the relationship between CT (except for CT = open) and the slew rate for any  $V_{BIAS}$  is:

$$SR = 0.35 \times CT + 20$$

where

- SR = slew rate (in  $\mu s/V$ )
  - CT = the capacitance value on the CT terminal (in pF)
  - The units for the constant 20 are  $\mu s/V$ .
  - The units for the constant 0.35 are  $\mu s/(V \cdot pF)$ .
- (4)

Rise time can be calculated by multiplying the input voltage (typically 10% to 90%) by the slew rate. The table below contains rise time values measured on a typical device.

CTx (pF)	RISE TIME ( $\mu s$ ) 10%–90%, $C_L = 0.1 \mu F$ , $V_{BIAS} = 2.5V$ to $5.7V$ , $R_L = 10\Omega$ LOAD. TYPICAL VALUES AT 25°C, 25V X7R 10% CERAMIC CAP					
	5V	3.3V	1.8V	1.5V	1.2V	0.7V
Open	140	98	62	54	46	32
220	444	301	175	150	124	81
470	767	518	299	255	210	133
1000	1492	994	562	474	387	245
2200	3105	2050	1151	961	787	490
4700	6420	4246	2365	1980	1612	998
10000	14059	9339	5183	4331	3533	2197

## 9.4 Device Functional Modes

The following Table describes what the OUT pin will be connected to for a particular device as determined by the EN pin.

EN	TPS22953	TPS22954
L	OPEN	$R_{PD}$ to GND
H	IN	IN

## 10 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

This section will highlight some of the design considerations when implementing this device in various applications. A PSPICE model for this device is also available on [www.ti.com](http://www.ti.com) for further aid.

#### 10.1.1 Input to Output Voltage Drop

The input to output voltage drop in the device is determined by the  $R_{ON}$  of the device and the load current. The  $R_{ON}$  of the device depends upon the  $V_{IN}$  and  $V_{BIAS}$  conditions of the device. Refer to the  $R_{ON}$  specification of the device in the [Electrical Characteristics](#) table of this datasheet. Once the  $R_{ON}$  of the device is determined based upon the  $V_{IN}$  and  $V_{BIAS}$  voltage conditions, use [Equation 5](#) to calculate the input to output voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (5)$$

Where:

$\Delta V$  = voltage drop from IN to OUT

$I_{LOAD}$  = load current

$R_{ON}$  = On-Resistance of the device for a specific  $V_{IN}$  and  $V_{BIAS}$

An appropriate  $I_{LOAD}$  must be chosen such that the  $I_{MAX}$  specification of the device is not violated.

#### 10.1.2 Thermal Considerations

The maximum IC junction temperature should be restricted to just under the thermal shutdown ( $T_{SD}$ ) limit of the device. To calculate the maximum allowable dissipation,  $P_{D(max)}$  for a given output current and ambient temperature, use [Equation 6](#).

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (6)$$

Where:

$P_{D(max)}$  = maximum allowable power dissipation

$T_{J(max)}$  = maximum allowable junction temperature before hitting thermal shutdown (see [Electrical Characteristics](#) table)

$T_A$  = ambient temperature of the device

$\theta_{JA}$  = junction to air thermal impedance. See [Thermal Information](#) section. This parameter is highly dependent upon board layout.

## Application Information (continued)

### 10.1.3 Automatic Power Sequencing

The PG pin of the TPS22953/54 allows for automatic sequencing of multiple system rails or loads. The accurate SNS voltage monitoring will ensure the first rail is up before the next starts to turn on. This approach provides robust system sequencing and reduces the total inrush current by preventing overlap. The example shows how two rails can be sequenced. There is no limit to the number of rails that can be sequenced in this way

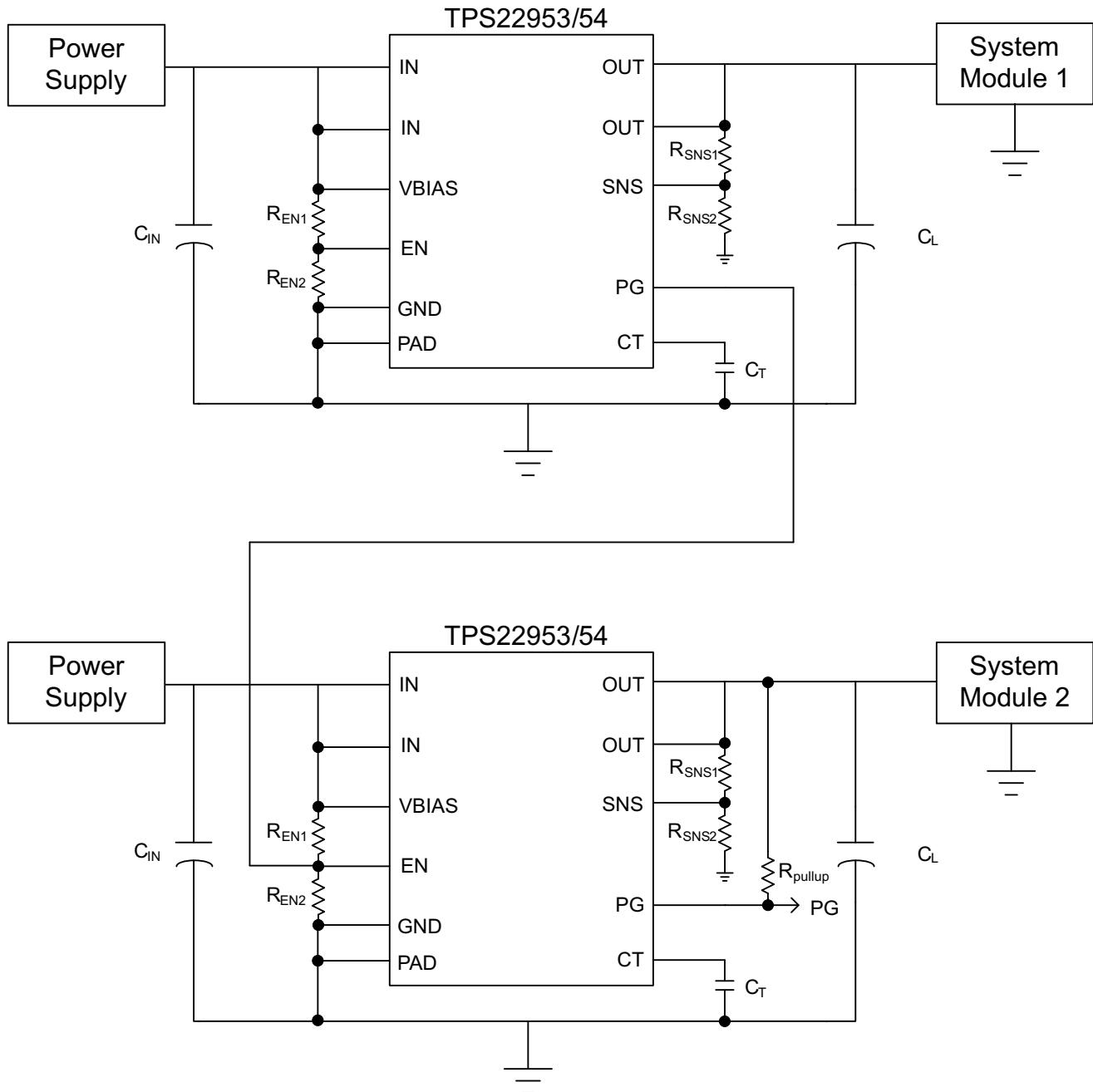
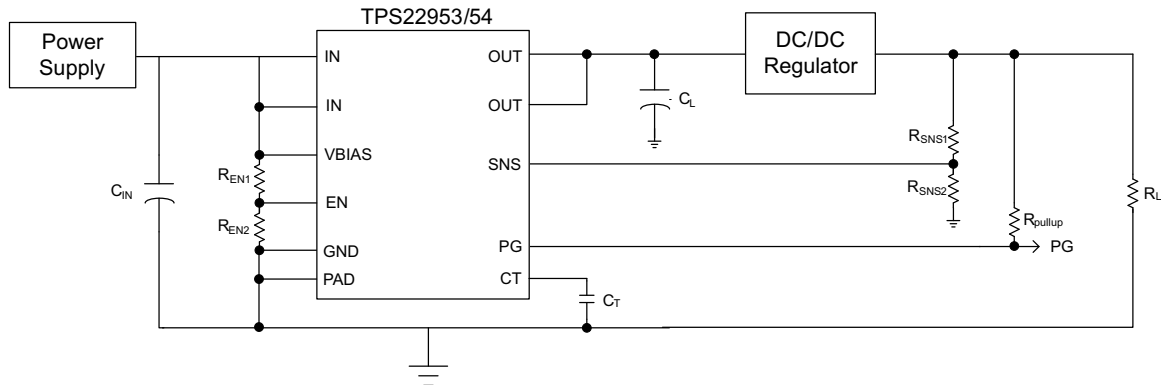


Figure 55. Power Sequencing with PG Control

## Application Information (continued)

### 10.1.4 Monitoring a Downstream Voltage

The SNS pin can be used to monitor other system voltages in addition to  $V_{OUT}$ . The status of the monitored voltage will be indicated by the PG pin which can be pulled up to  $V_{OUT}$  or another voltage. The figure below shows an example of the TPS22953/54 monitoring the output of a downstream DC/DC regulator. In this case, the switch will turn on when the power supply is above the UVLO, but the PG will not be asserted until the DC/DC regulator has started up.

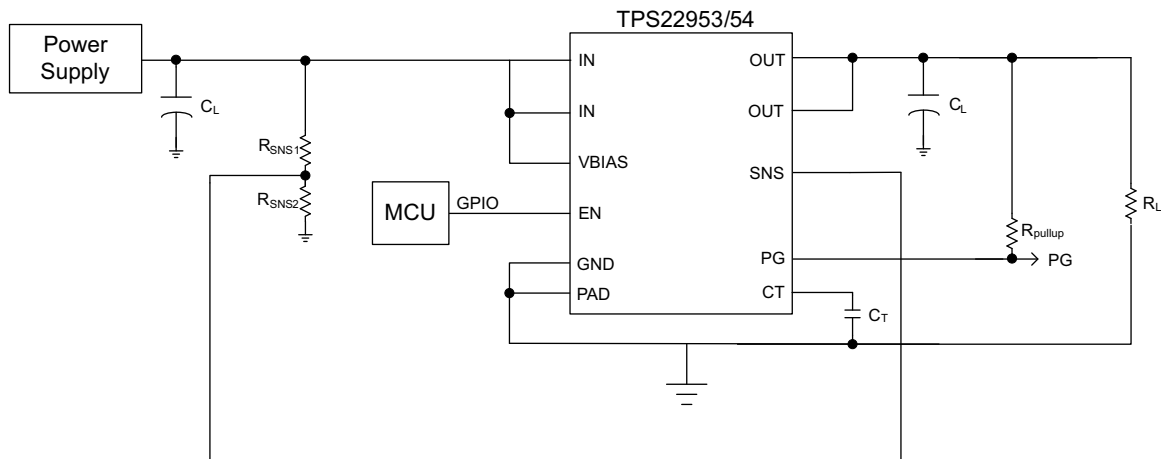


**Figure 56. Monitoring a Downstream Voltage**

In this application, if the DC/DC Regulator is shut down, the supervisor will register this as a fault case and reset the load switch.

#### 10.1.4.1 Monitoring the Input Voltage

The SNS pin can also be used to monitor  $V_{IN}$  in the case a MCU GPIO is being used to control the EN. This will allow PG to report on the status of the input voltage when the switch is enabled.



**Figure 57. Monitoring Input Voltage**

## 10.2 Typical Application

This application demonstrates how the TPS22953/54 can be used to limit inrush current to output capacitance.

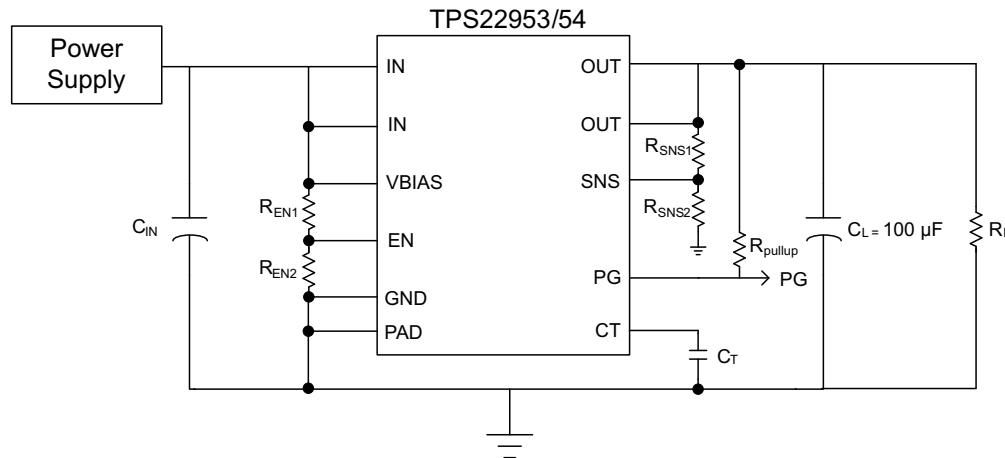


Figure 58. Typical Application Schematic for Powering a Downstream Module

### 10.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
$V_{IN}$	3.3 V
$V_{BIAS}$	5.0 V
$C_L$	47 $\mu$ F
Maximum Acceptable Inrush Current	150mA
$R_L$	None

### 10.2.2 Detailed Design Procedure

To begin the design process, the designer needs to know the following:

- Input voltage
- BIAS voltage
- Load current
- Load capacitance
- Maximum acceptable inrush current

#### 10.2.2.1 Inrush Current

To determine how much inrush current will be caused by the  $C_L$  capacitor, use Equation 7:

$$I_{INRUSH} = C_L \times \frac{dV_{OUT}}{dt} \quad (7)$$

Where:

$I_{INRUSH}$  = amount of inrush caused by  $C_L$

$C_L$  = capacitance on  $V_{OUT}$

$dt$  =  $V_{OUT}$  Rise Time (typically 10% to 90%)

$dV_{OUT}$  = Change in  $V_{OUT}$  Voltage (typically 10% to 90%)

In this case, a Slew Rate slower than 314 $\mu$ s/V will be required to meet the maximum acceptable inrush requirement. Equation 4 can be used to estimate the  $C_T$  capacitance required for this slew rate.

$$314 \mu\text{s/V} = 0.35 \times C_T + 20 \quad (8)$$

$$C_T = 840 \text{ pF} \quad (9)$$

### 10.2.3 Application Curves

The following Application Curves show the inrush with multiple different CT values. These curves show only a CT capacitance greater than 840pF results in the acceptable inrush current of 150mA.

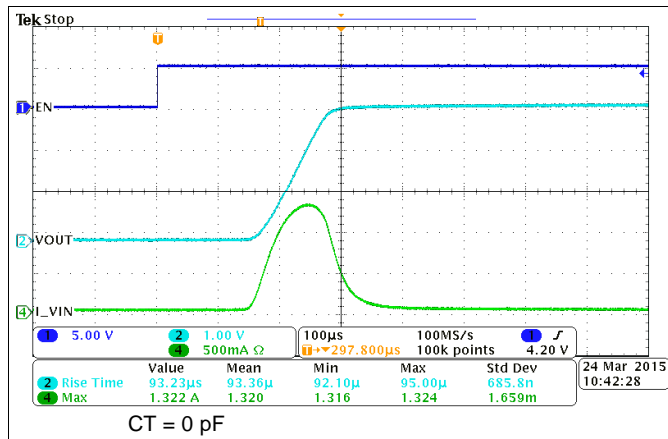


Figure 59. Inrush with CT = 0 pF

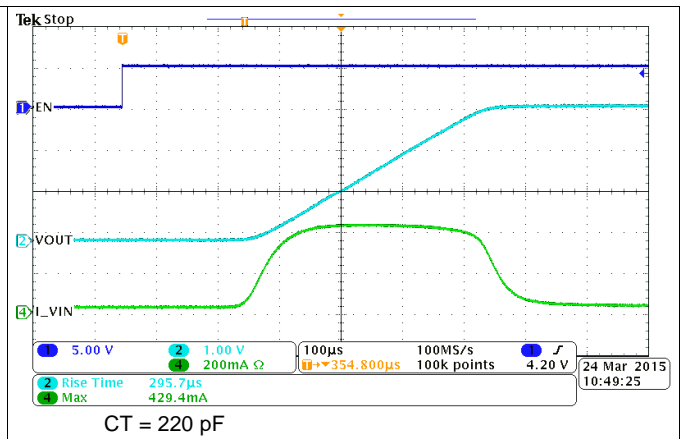


Figure 60. Inrush with CT = 220 pF

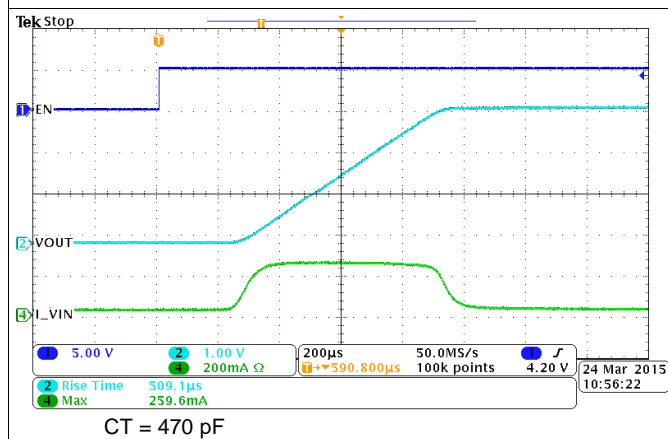


Figure 61. Inrush with CT = 470 pF

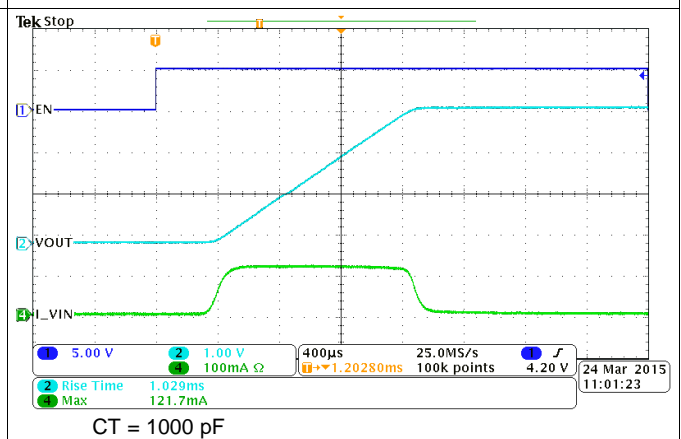


Figure 62. Inrush with CT = 1000 pF

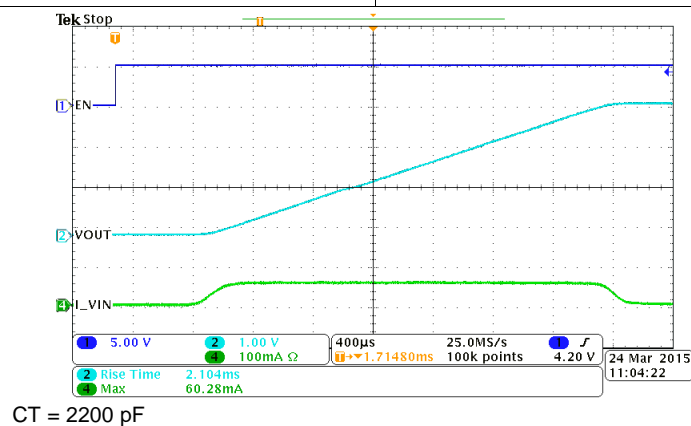


Figure 63. Inrush with CT = 2200 pF

## 11 Power Supply Recommendations

The device is designed to operate from a  $V_{BIAS}$  range of 2.5V to 5.7V and a  $V_{IN}$  range of 0.7 V to 5.7 V. The power supply should be well regulated and placed as close to the device terminals as possible. It must be able to withstand all transient and load current steps. In most situations, using an input capacitance of 1  $\mu$ F is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

The requirements for larger input capacitance can be mitigated by adding additional capacitance to the CT pin. This will cause the load switch to turn on more slowly. Not only will this reduce transient inrush current, but it will also give the power supply more time to respond to the load current step.

## 12 Layout

### 12.1 Layout Guidelines

- Input and Output traces should be as short and wide as possible to accommodate for high current.
- Use vias under the exposed thermal pad for thermal relief for high current operation.
- The CT Capacitor should be placed as close as possible to the device to minimize parasitic trace capacitance. It is also recommended to cutout copper on other layers directly below CT to minimize parasitic capacitance.
- The IN terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The OUT terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric. This capacitor should be placed as close to the device pins as possible.
- The BIAS terminal should be bypassed to ground with low ESR ceramic bypass capacitors. The typical recommended bypass capacitance is ceramic with X5R or X7R dielectric.

## 12.2 Layout Example

○ VIA to Power Ground Plane

○ VIA to PG pin

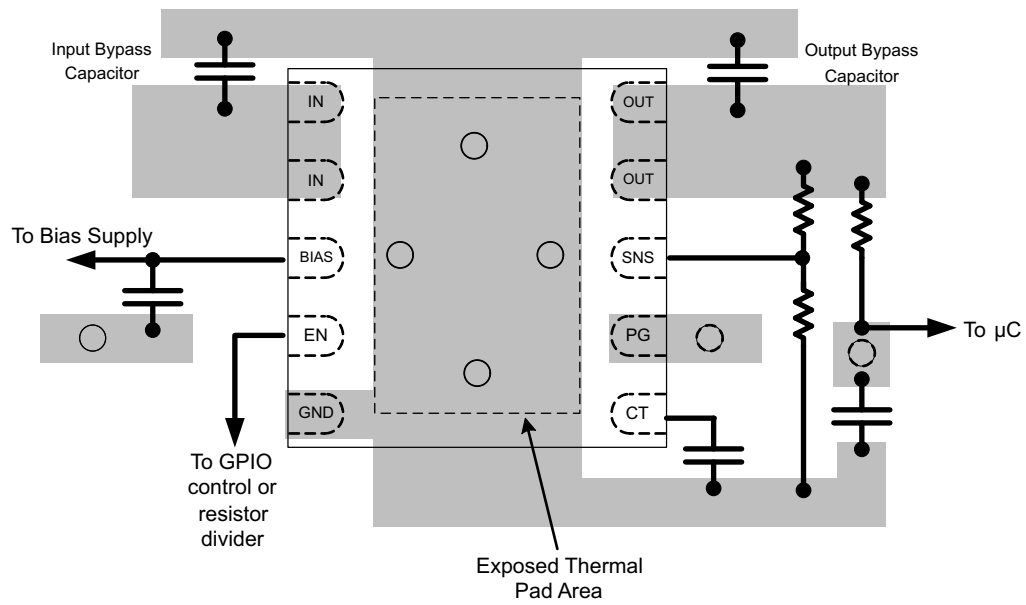


Figure 64. Recommended Board Layout

## 13 器件和文档支持

### 13.1 相关链接

以下表格列出了快速访问链接。范围包括技术文档、支持与社区资源、工具和软件，并且可以快速访问样片或购买链接。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS22953	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>
TPS22954	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>	<a href="#">请单击此处</a>

### 13.2 商标

All trademarks are the property of their respective owners.

### 13.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 13.4 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、首字母缩略词和定义。

## 14 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TPS22953DQCR</a>	Active	Production	WSON (DQC)   10	3000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 105	RB953
TPS22953DQCR.A	Active	Production	WSON (DQC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB953
TPS22953DQCRG4	Active	Production	WSON (DQC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB953
TPS22953DQCRG4.A	Active	Production	WSON (DQC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB953
<a href="#">TPS22953DSQR</a>	Active	Production	WSON (DSQ)   10	3000   LARGE T&R	Yes	NIPDAU   SN   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	ZFDI
TPS22953DSQR.A	Active	Production	WSON (DSQ)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZFDI
TPS22953DSQRG4	Active	Production	WSON (DSQ)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZFDI
TPS22953DSQRG4.A	Active	Production	WSON (DSQ)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	ZFDI
<a href="#">TPS22954DQCR</a>	Active	Production	WSON (DQC)   10	3000   LARGE T&R	Yes	NIPDAU   SN	Level-2-260C-1 YEAR	-40 to 105	RB954
TPS22954DQCR.A	Active	Production	WSON (DQC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB954
TPS22954DQCRG4	Active	Production	WSON (DQC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB954
TPS22954DQCRG4.A	Active	Production	WSON (DQC)   10	3000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	RB954
<a href="#">TPS22954DSQR</a>	Active	Production	WSON (DSQ)   10	3000   LARGE T&R	Yes	NIPDAU   SN   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	ZDKI
TPS22954DSQR.A	Active	Production	WSON (DSQ)   10	3000   LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	ZDKI
TPS22954DSQRG4	Active	Production	WSON (DSQ)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZDKI
TPS22954DSQRG4.A	Active	Production	WSON (DSQ)   10	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZDKI

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**OTHER QUALIFIED VERSIONS OF TPS22953, TPS22954 :**

- Automotive : [TPS22953-Q1](#), [TPS22954-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22953DQCR	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22953DQCRG4	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22953DSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22953DSQRG4	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22954DQCR	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22954DQCRG4	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
TPS22954DSQR	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22954DSQRG4	WSON	DSQ	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

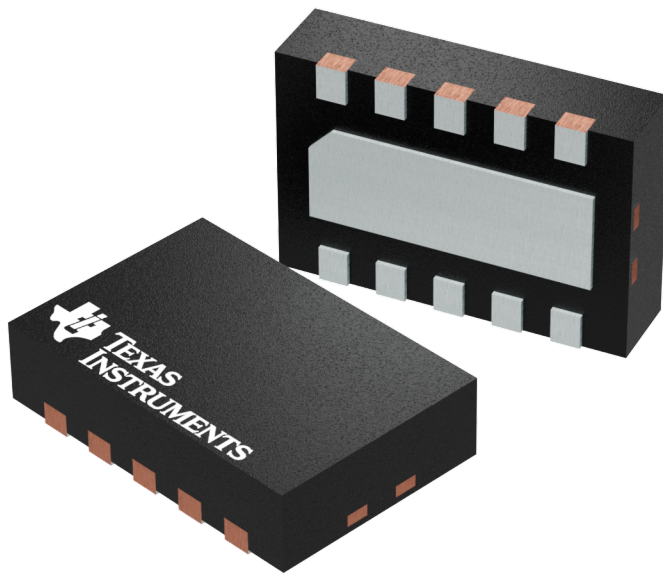
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22953DQCR	WSON	DQC	10	3000	210.0	185.0	35.0
TPS22953DQCRG4	WSON	DQC	10	3000	210.0	185.0	35.0
TPS22953DSQR	WSON	DSQ	10	3000	210.0	185.0	35.0
TPS22953DSQRG4	WSON	DSQ	10	3000	210.0	185.0	35.0
TPS22954DQCR	WSON	DQC	10	3000	210.0	185.0	35.0
TPS22954DQCRG4	WSON	DQC	10	3000	210.0	185.0	35.0
TPS22954DSQR	WSON	DSQ	10	3000	182.0	182.0	20.0
TPS22954DSQRG4	WSON	DSQ	10	3000	182.0	182.0	20.0

## GENERIC PACKAGE VIEW

DQC 10

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4209674/B

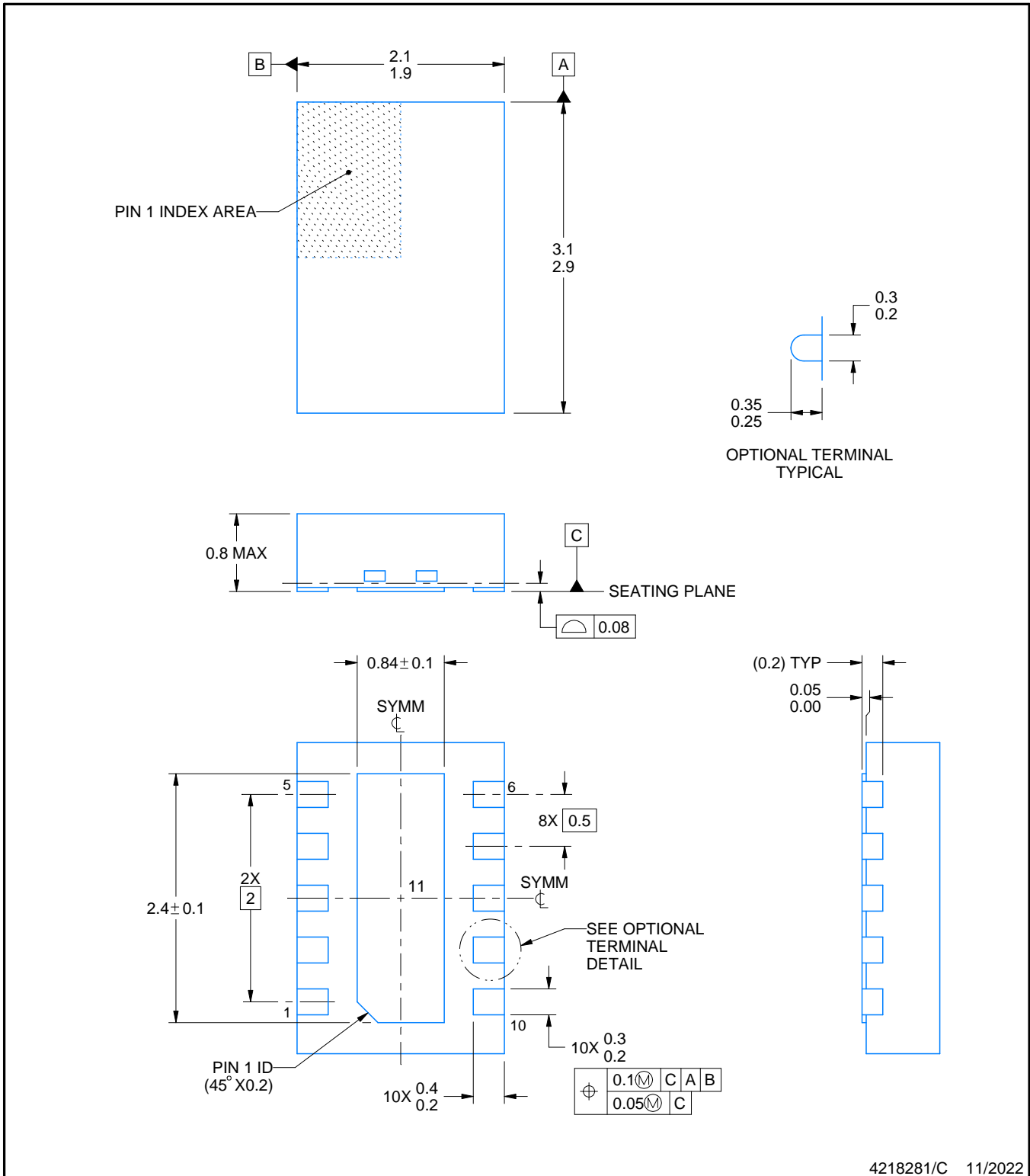
# DQC0010A



# PACKAGE OUTLINE

## WSO - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4218281/C 11/2022

**NOTES:**

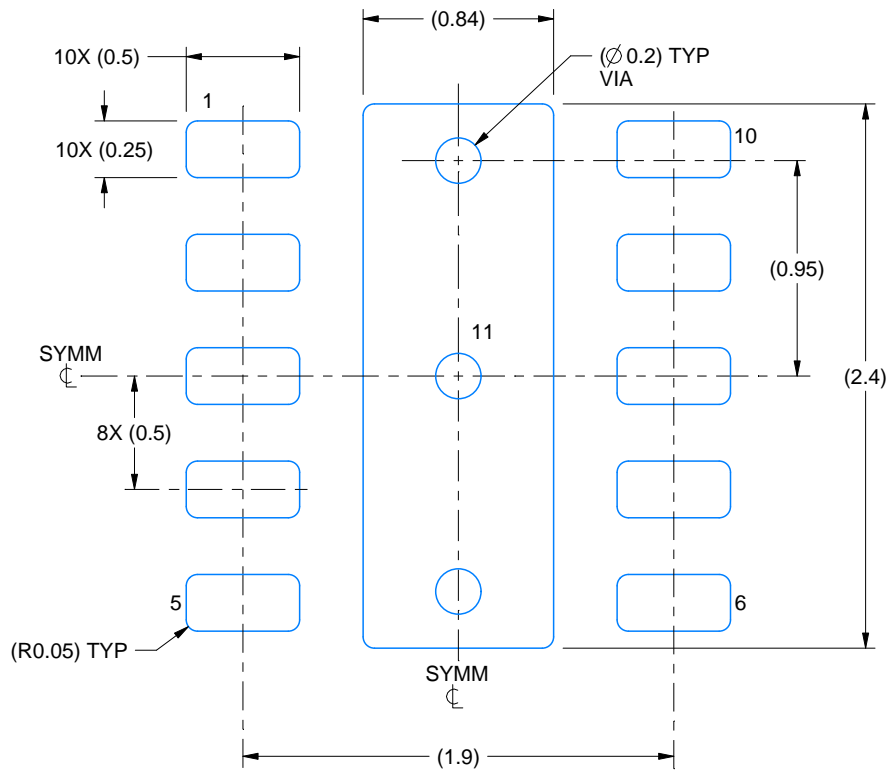
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

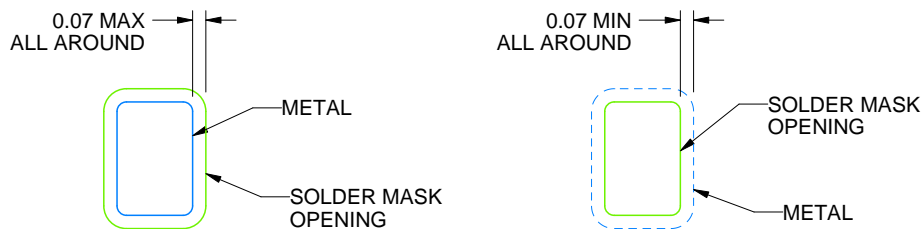
DQC0010A

WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE: 30X



NON SOLDER MASK  
DEFINED  
(PREFERRED)

SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4218281/C 11/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



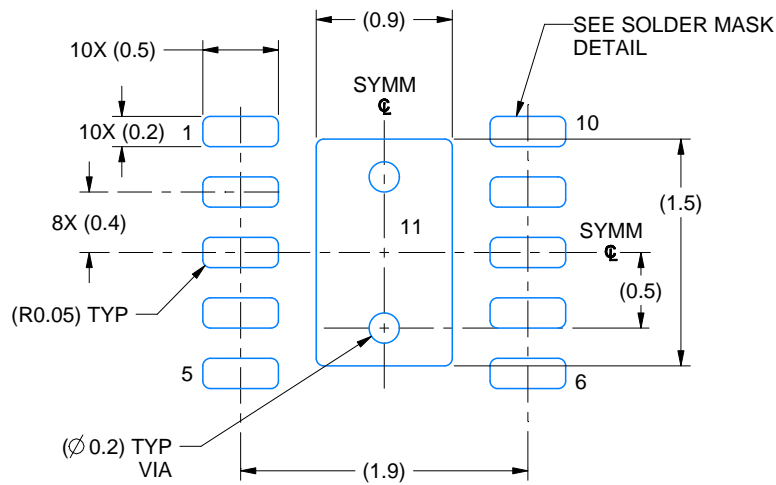


# EXAMPLE BOARD LAYOUT

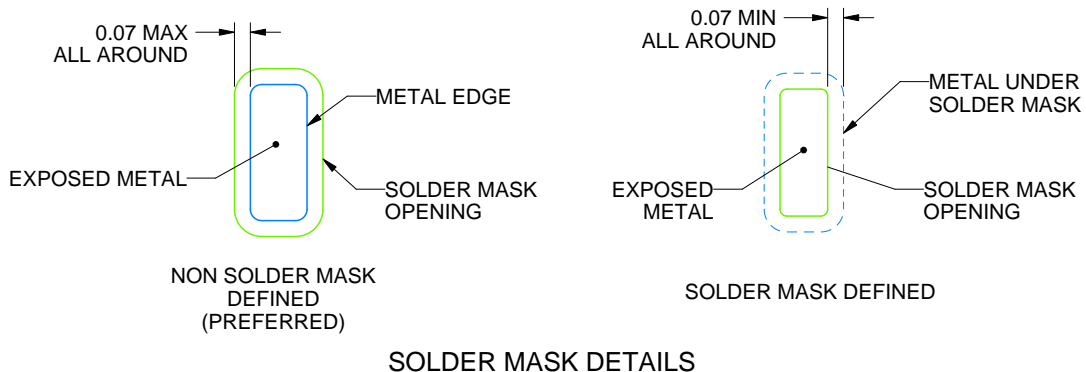
DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



SOLDER MASK DETAILS

4218906/A 04/2019

NOTES: (continued)

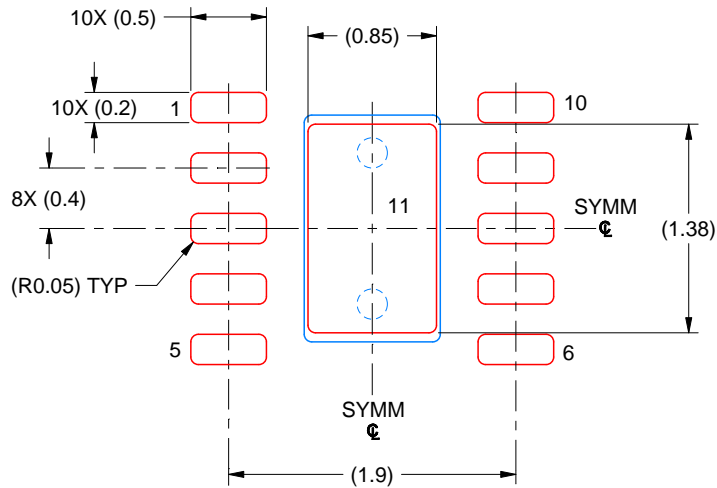
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSQ0010A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 11  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218906/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月