限流配电开关

查询样品: **TPS2066-Q1**

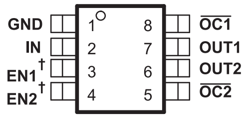
特性

- 符合汽车应用要求
- **70 mΩ** 高侧 **MOSFET**
- **1-A** 持续电流
- 过热和短路保护
- 准确电流限制
  (最小 **1.1 A,** 最大 **1.9 A)**
- 工作电压范围：**2.7 V** 至 **5.5 V**
- **0.6-ms** 典型上升时间
- 欠压锁定
- 抗尖刺脉冲错误报告 **($\overline{\text{OC}}$)**
- 加电期间无 **$\overline{\text{OC}}$**尖刺脉冲
- **1-μA** 最大待机电源电流
- 双向开关
- 工作环境温度范围**: -40°C** 至 **105°C**
- 内置软启动
- **UL** 列示：文件编号 **E169910**

应用范围

- 高电容负载
- 短路保护功能

DGN 封装
（顶视图）



†All enable inputs are active high

说明

TPS2066-Q1 配电开关适合于可能会发生重电容负载和短路的应用。 此设备包含一个用于配电系统的 70-mΩ N-通道 MOSFET 电源开关，此配电系统要求在一个封装内具有多重开关。 每个开关由一个逻辑使能引脚控制。 内部充电泵提供栅极驱动，此充电泵设计用来控制电源开关的上升和下落次数以将开关时的电流冲击降到最低。 充电泵不需要外部组件并在供电电压低至 2.7 V时仍可正常工作。

当输出负载超出电流限制阈值或出现短路时，通过切换到恒定电流模式，上拉过载(OC) 逻辑输出低电平，器件将输出电流限制在安全水平上。 当开关中的持续高过载和短路使功率耗散增加进而引起结点温度上升时，一个过热保护电路会关闭此开关以避免电路损坏。 一旦设备充分冷却，将自动从热关断中恢复。 内部电路确保开关保持关闭状态直到合格输入电压出现。 此配电开关设计用于将电流限制在 1.5 A (典型值)。

English Data Sheet: SLVSB37

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 105°C	8-Pin VSSOP - DGN	Reel of 2500	TPS2066TDGNRQ1	2066Q

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

		UNIT
Input voltage range, $V_{I(IN)}$ [2]		-0.3 V to 6 V
Output voltage range, $V_{O(OUT)}$ [2], $V_{O(OUTx)}$		-0.3 V to 6 V
Input voltage range, $V_{I(EN)}$, $V_{I(EN)}$, $V_{I(ENx)}$, $V_{I(EN)}$		-0.3 V to 6 V
Voltage range, $V_{I(\overline{OC})}$, $V_{I(\overline{OCx})}$		-0.3 V to 6 V
Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$		Internally limited
Continuous total power dissipation		See Dissipation Rating Table
Operating junction temperature range, T_J		-40°C to 150°C
Electrostatic discharge (ESD) protection	Human body model (HBM)	2 kV
	Charge device model (CDM)	1000 V
	Machine model (MM)	100V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND.

DISSIPATING RATING TABLE

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 105°C POWER RATING
DGN-8[1]	1712.3 mW	17.123 mW/°C	941.78 mW	684.33 mW	341 mW

(1) Power ratings are based on the high-k board (2 signal, 2 plane) with PowerPAD™ vias to the internal ground plane.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Input voltage, $V_{I(IN)}$	2.7	5.5	V
Input voltage, $V_{I(EN)}$, $V_{I(EN)}$, $V_{I(ENx)}$, $V_{I(EN)}$	0	5.5	V
Continuous output current, $I_{O(OUT)}$, $I_{O(OUTx)}$	0	1	A
Operating ambient temperature, T_A	-40	105	°C

ELECTRICAL CHARACTERISTICS

over recommended operating ambient temperature range T_A = -40°C to 105°C (unless otherwise noted), $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
POWER SWITCH							
$r_{DS(on)}$	Static drain-source on-state resistance, 5-V operation and 3.3-V operation	$V_{I(IN)}$ = 5 V or 3.3 V, I_O = 1 A, -40°C ≤ T_A ≤ 105°C			70	135	mΩ
	Static drain-source on-state resistance, 2.7-V operation	$V_{I(IN)}$ = 2.7 V, I_O = 1 A, -40°C ≤ T_A ≤ 105°C			75	150	mΩ
t_r	Rise time, output	$V_{I(IN)}$ = 5.5 V	C_L = 1 μF, R_L = 5 Ω, T_A = 25°C		0.6	1.5	ms
		$V_{I(IN)}$ = 2.7 V			0.4	1	
t_f	Fall time, output	$V_{I(IN)}$ = 5.5 V		0.05		0.5	
		$V_{I(IN)}$ = 2.7 V		0.05		0.5	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating ambient temperature range T_A = -40°C to 105°C (unless otherwise noted), $V_{I(IN)}$ = 5.5 V, I_O = 1 A, $V_{I(ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V

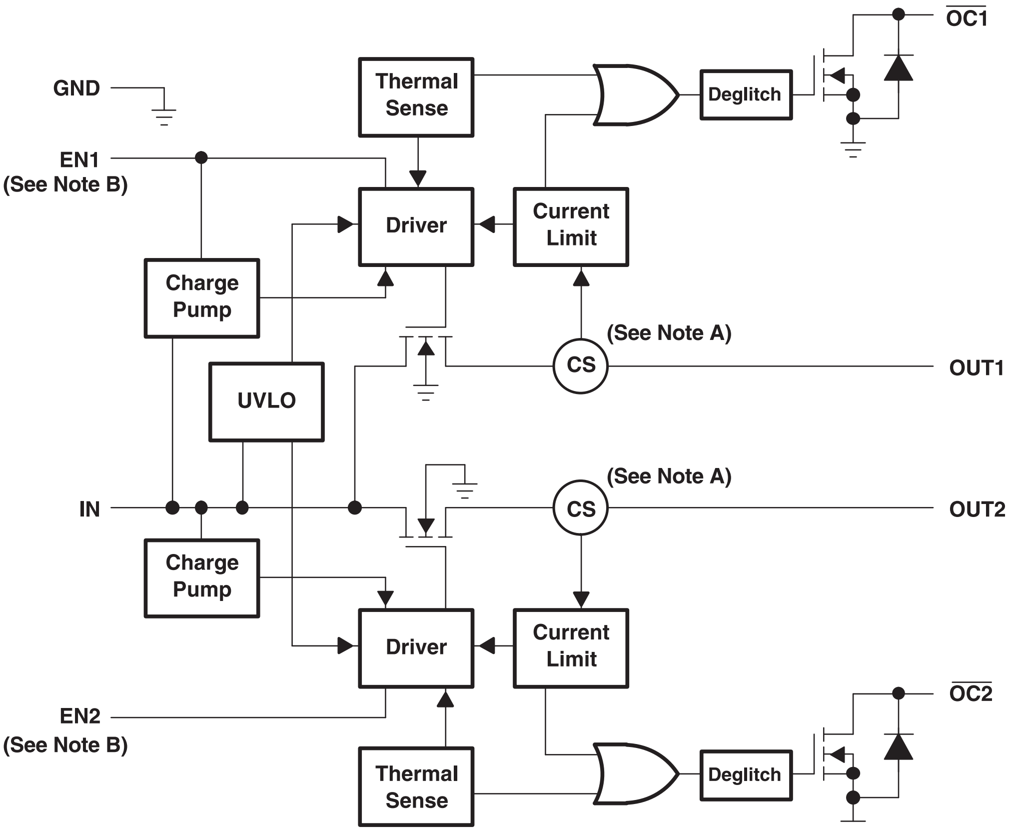
PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
ENABLE INPUT $\overline{\text{EN}}$ OR EN							
V_{IH}	High-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V		2			V
V_{IL}	Low-level input voltage	2.7 V ≤ $V_{I(IN)}$ ≤ 5.5 V				0.8	
I_I	Input current	$V_{I(ENx)}$ = 0 V or 5.5 V, $V_{I(ENx)}$ = 0 V or 5.5 V		-0.5		0.5	μA
t_{on}	Turnon time	C_L = 100 μF, R_L = 5 Ω				3	ms
t_{off}	Turnoff time	C_L = 100 μF, R_L = 5 Ω				10	
CURRENT LIMIT							
I_{OS}	Short-circuit output current	$V_{I(IN)}$ = 5 V, OUT connected to GND, device enabled into short-circuit	T_A = 25°C	1.1	1.5	1.9	A
			-40°C ≤ T_A ≤ 105°C	1.1	1.5	2.1	
I_{OC_TRIP}	Overcurrent trip threshold	$V_{I(IN)}$ = 5 V, current ramp (≤ 100 A/s) on OUT		1.6	2.3	2.9	A
SUPPLY CURRENT							
Supply current, low-level output		No load on OUT, $V_{I(ENx)}$ = 0 V	T_A = 25°C		0.5	1	μA
			-40°C ≤ T_A ≤ 105°C		0.5	5	
Supply current, high-level output		No load on OUT, $V_{I(ENx)}$ = 5.5 V	T_A = 25°C		50	70	μA
			-40°C ≤ T_A ≤ 105°C		50	90	
Leakage current		OUT connected to ground, $V_{I(ENx)}$ = 0 V	-40°C ≤ T_A ≤ 105°C		1		μA
Reverse leakage current		$V_{I(OUTx)}$ = 5.5 V, IN = ground	T_A = 25°C		0.2		μA
UNDERVOLTAGE LOCKOUT							
Low-level input voltage, IN				2		2.5	V
Hysteresis, IN		T_A = 25°C			75		mV
OVERCURRENT $\overline{\text{OC1}}$ and $\overline{\text{OC2}}$							
Output low voltage, $V_{OL(OCx)}$		$I_{O(\overline{OCx})}$ = 5 mA				0.4	V
Off-state current		$V_{O(\overline{OCx})}$ = 5 V or 3.3 V				1	μA
$\overline{\text{OC}}$ deglitch		$\overline{\text{OCx}}$ assertion or deassertion		4	8	15	ms
THERMAL SHUTDOWN[2]							
Thermal shutdown threshold				135			°C
Recovery from thermal shutdown				125			°C
Hysteresis					10		°C

(2) The thermal shutdown only reacts under overcurrent conditions.

PIN FUNCTIONS

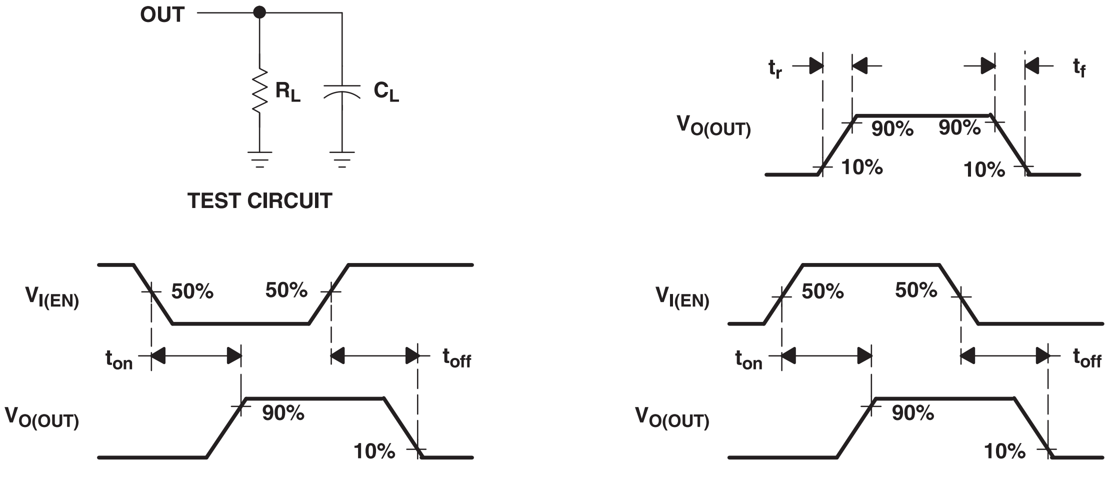
PINS		I/O	DESCRIPTION
NAME	NO.		
EN1	3	I	Enable input, logic high turns on power switch IN-OUT1
EN2	4	I	Enable input, logic high turns on power switch IN-OUT2
GND	1		Ground
IN	2	I	Input voltage
$\overline{\text{OC1}}$	8	O	Overcurrent, open-drain output, active low, IN-OUT1
$\overline{\text{OC2}}$	5	O	Overcurrent, open-drain output, active low, IN-OUT2
OUT1	7	O	Power-switch output, IN-OUT1
OUT2	6	O	Power-switch output, IN-OUT2
PowerPAD™	-		Internally connected to GND; used to heat-sink the part to the circuit board traces. Should be connected to GND pin.

Functional Block Diagram



Note A: Current sense
Note B: Active high (ENx)

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

Figure 1. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)

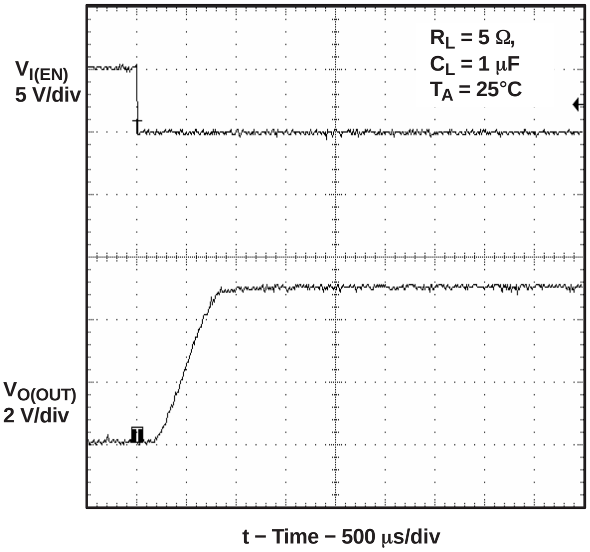


Figure 2. Turnon Delay and Rise Time With 1-µF Load

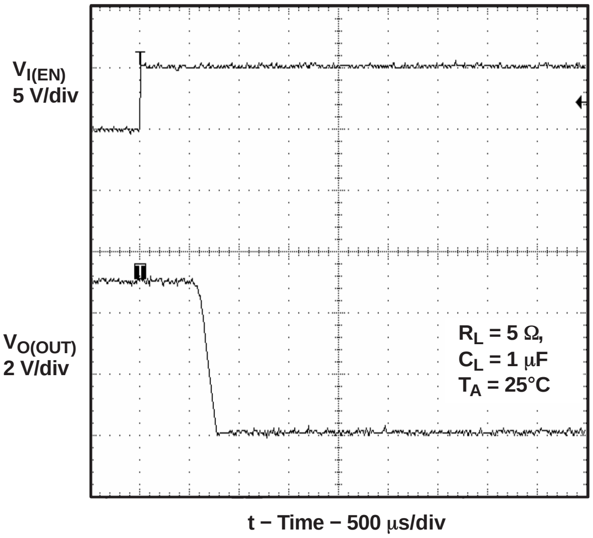


Figure 3. Turnoff Delay and Fall Time With 1-µF Load

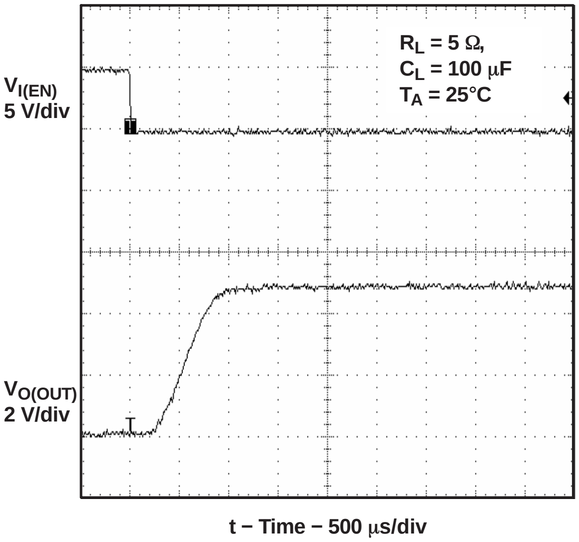


Figure 4. Turnon Delay and Rise Time With 100-µF Load

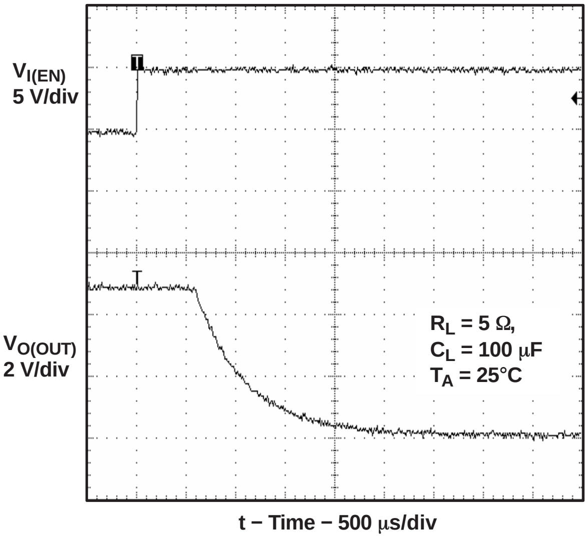


Figure 5. Turnoff Delay and Fall Time With 100-µF Load

PARAMETER MEASUREMENT INFORMATION (continued)

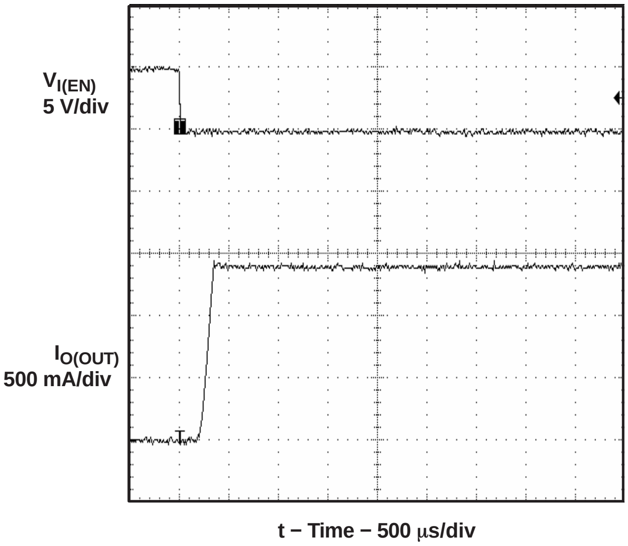


Figure 6. Short-Circuit Current, Device Enabled Into Short

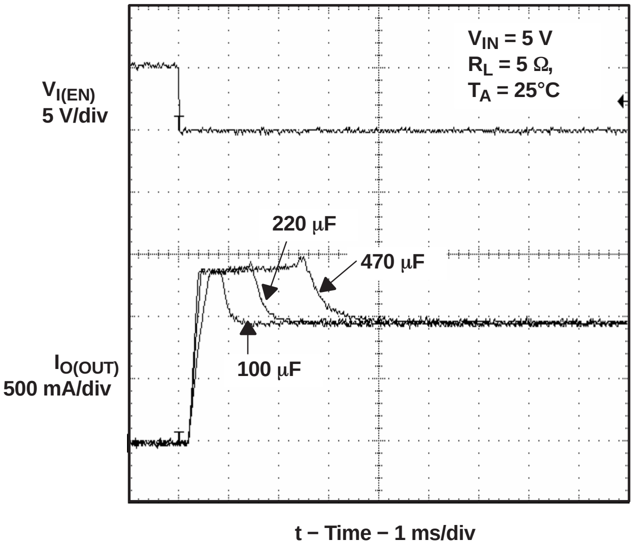


Figure 7. Inrush Current With Different Load Capacitance

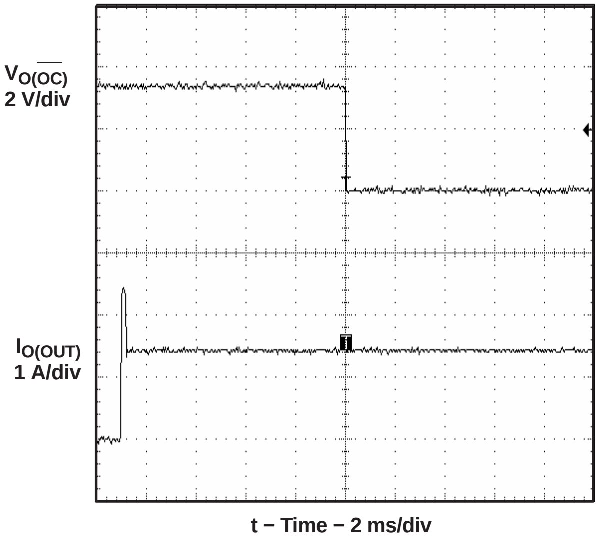


Figure 8. 2-Ω Load Connected to Enabled Device

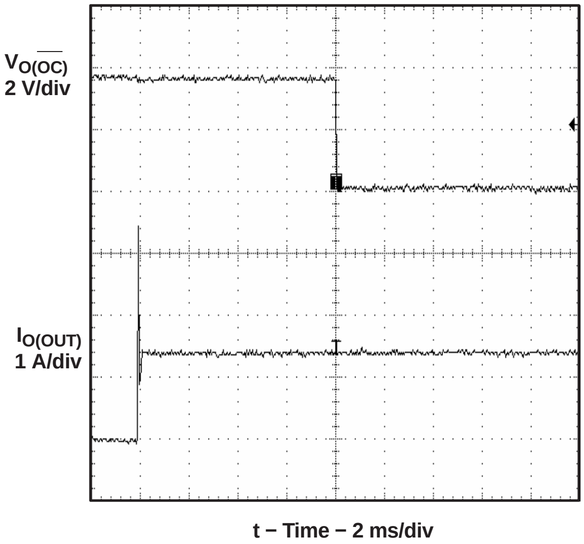


Figure 9. 1-Ω Load Connected to Enabled Device

TYPICAL CHARACTERISTICS

TURN-ON TIME vs INPUT VOLTAGE

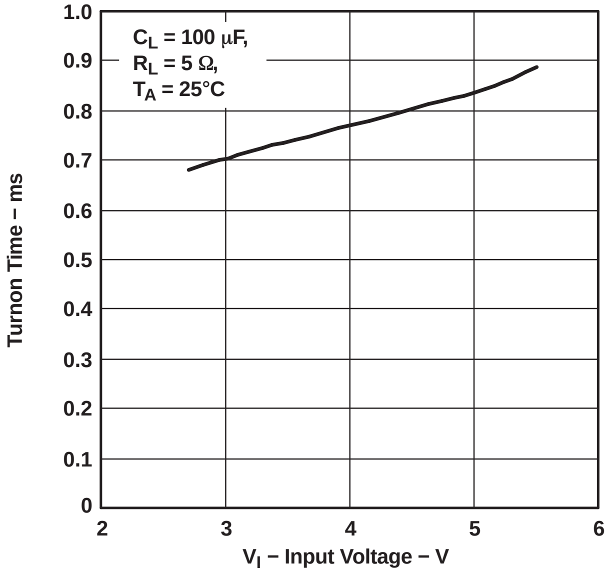


Figure 10.

TURN-OFF TIME vs INPUT VOLTAGE

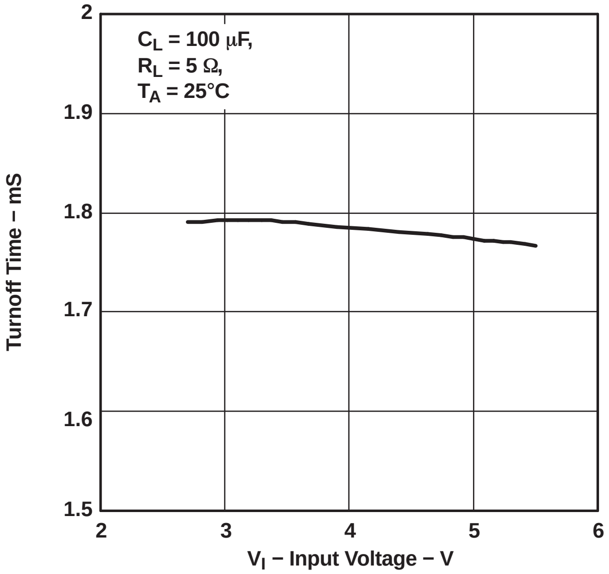


Figure 11.

RISE TIME vs INPUT VOLTAGE

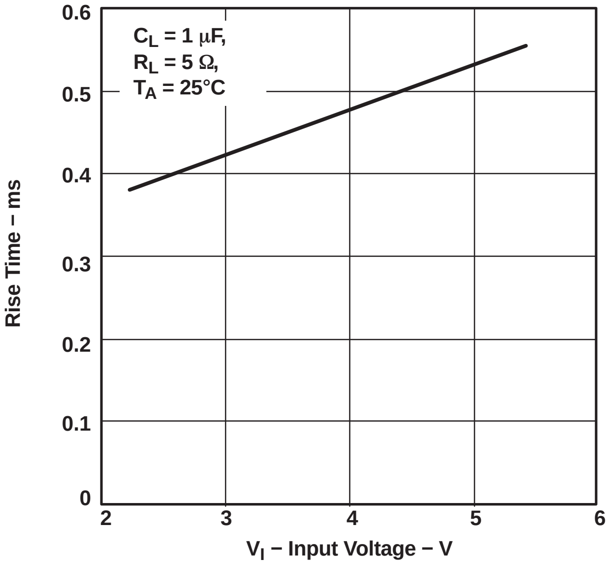


Figure 12.

FALL TIME vs INPUT VOLTAGE

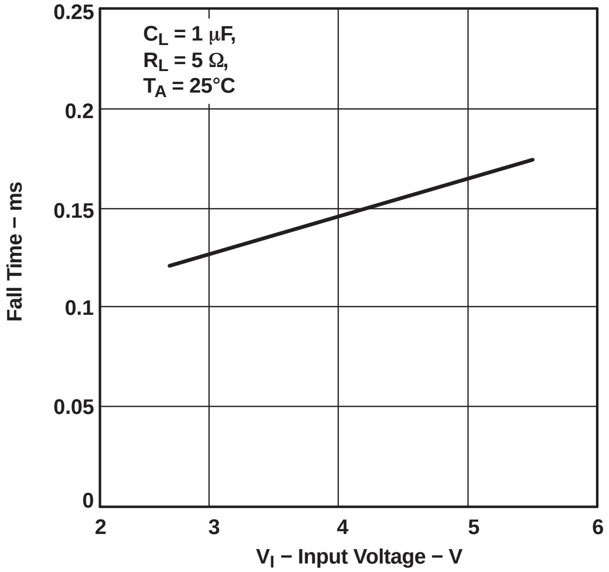


Figure 13.

TYPICAL CHARACTERISTICS (continued)

SUPPLY CURRENT, OUTPUT ENABLED vs JUNCTION TEMPERATURE

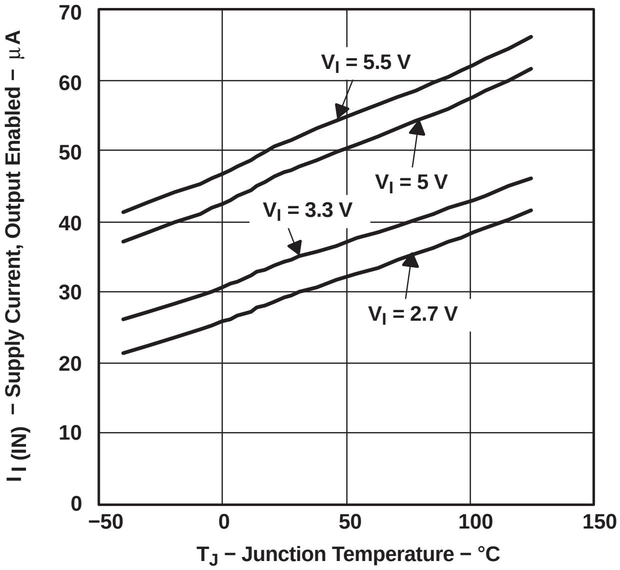


Figure 14.

SUPPLY CURRENT, OUTPUT DISABLED vs JUNCTION TEMPERATURE

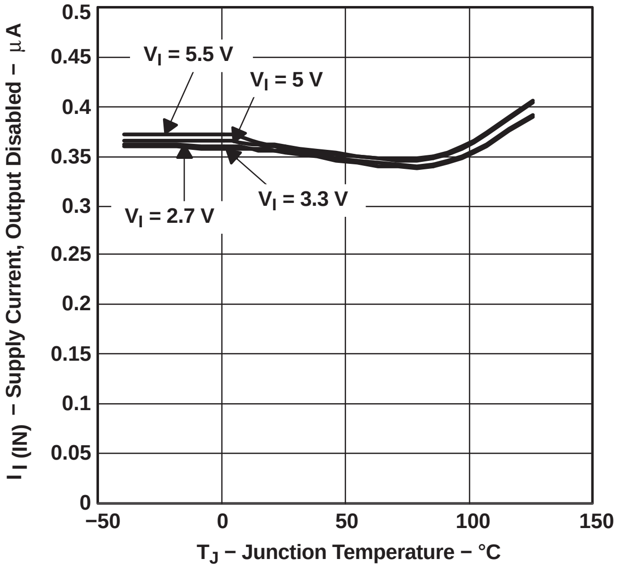


Figure 15.

STATIC DRAIN-SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURE

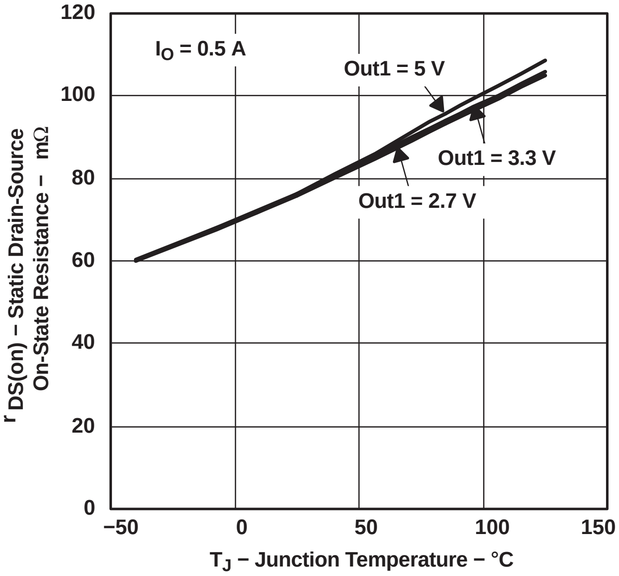


Figure 16.

SHORT-CIRCUIT OUTPUT CURRENT vs JUNCTION TEMPERATURE

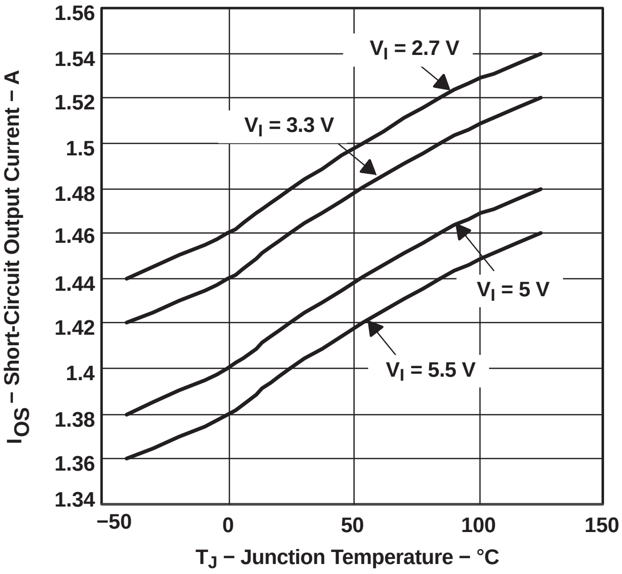


Figure 17.

TYPICAL CHARACTERISTICS (continued)

THRESHOLD TRIP CURRENT
vs
INPUT VOLTAGE

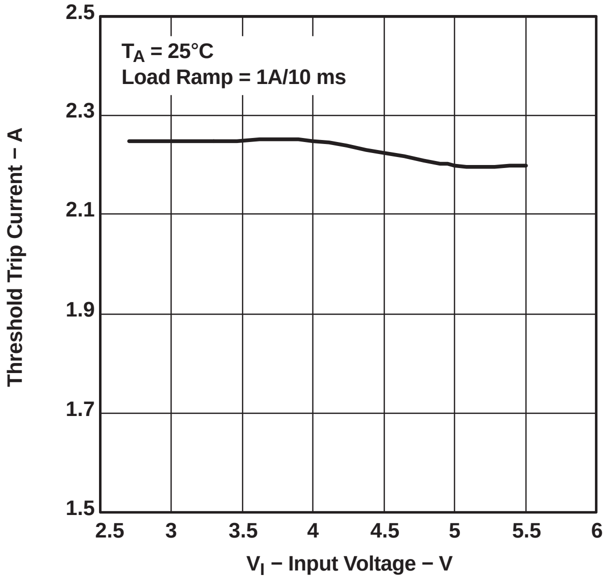


Figure 18.

UNDERVOLTAGE LOCKOUT
vs
JUNCTION TEMPERATURE

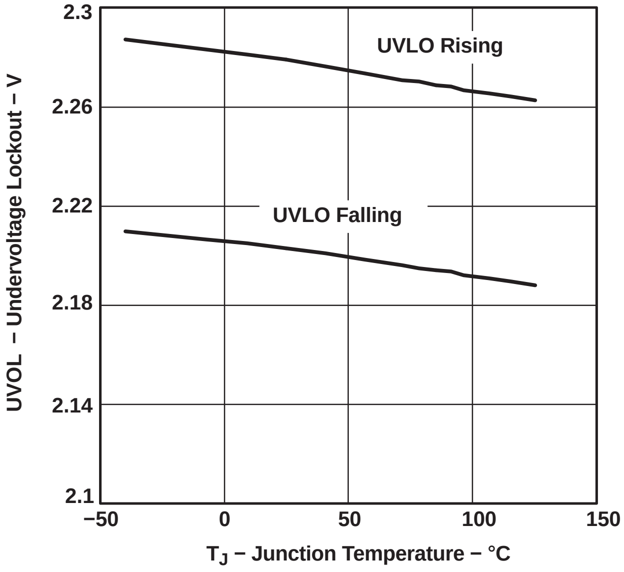


Figure 19.

CURRENT-LIMIT RESPONSE
vs
PEAK CURRENT

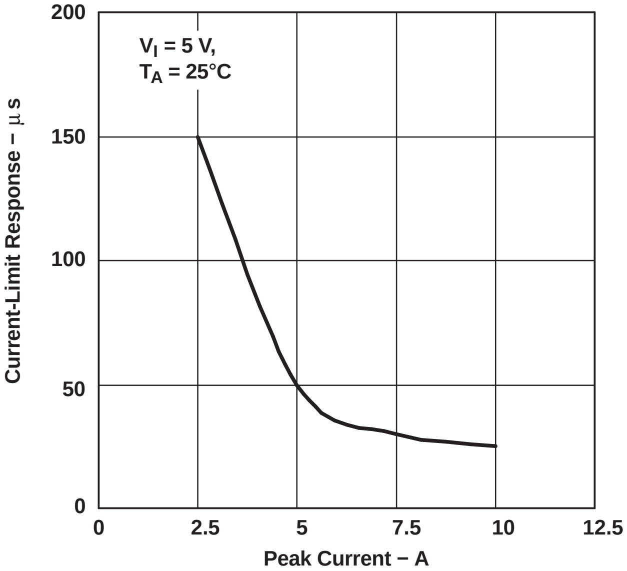


Figure 20.

APPLICATION INFORMATION

POWER-SUPPLY CONSIDERATIONS

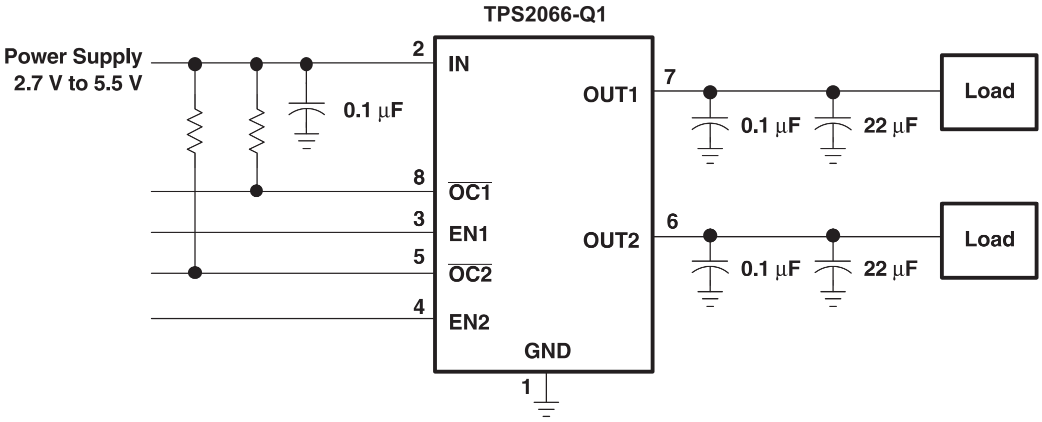


Figure 21. Typical Application

A 0.01-µF to 0.1-µF ceramic bypass capacitor between IN and GND, close to the device, is recommended. Placing a high-value electrolytic capacitor on the output pin(s) is recommended when the output load is heavy. This precaution reduces power-supply transients that may cause ringing on the input. Additionally, bypassing the output with a 0.01-µF to 0.1-µF ceramic capacitor improves the immunity of the device to short-circuit transients.

OVERCURRENT

A sense FET is employed to check for overcurrent conditions. Unlike current-sense resistors, sense FETs do not increase the series resistance of the current path. When an overcurrent condition is detected, the device maintains a constant output current and reduces the output voltage accordingly. Complete shutdown occurs only if the fault is present long enough to activate thermal limiting.

Three possible overload conditions can occur. In the first condition, the output has been shorted before the device is enabled or before $V_{I(IN)}$ has been applied (see Figure 14). The TPS2066-Q1 senses the short and immediately switches into a constant-current output.

In the second condition, a short or an overload occurs while the device is enabled. At the instant the overload occurs, high currents may flow for a short period of time before the current-limit circuit can react. After the current-limit circuit has tripped (reached the overcurrent trip threshold), the device switches into constant-current mode.

In the third condition, the load has been gradually increased beyond the recommended operating current. The current is permitted to rise until the current-limit threshold is reached or until the thermal limit of the device is exceeded (see Figure 15). The TPS2066-Q1 is capable of delivering current up to the current-limit threshold without damaging the device. Once the threshold has been reached, the device switches into its constant-current mode.

$\overline{\text{OC}}$ RESPONSE

The $\overline{\text{OC}}$x open-drain output is asserted (active low) when an overcurrent or overtemperature shutdown condition is encountered after a 10-ms deglitch timeout. The output remains asserted until the overcurrent or overtemperature condition is removed. Connecting a heavy capacitive load to an enabled device can cause a momentary overcurrent condition; however, no false reporting on $\overline{\text{OC}}$x occurs due to the 10-ms deglitch circuit. The TPS2066-Q1 is designed to eliminate false overcurrent reporting. The internal overcurrent deglitch eliminates the need for external components to remove unwanted pulses. $\overline{\text{OC}}$x is not deglitched when the switch is turned off due to an overtemperature shutdown.

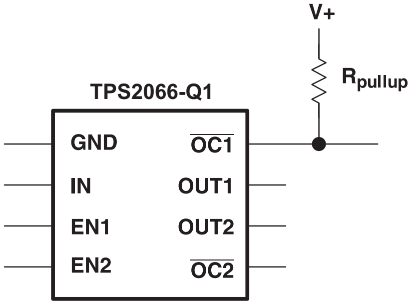


Figure 22. Typical Circuit for the $\overline{OC}$ Pin

POWER DISSIPATION AND JUNCTION TEMPERATURE

The low on-resistance on the N-channel MOSFET allows the small surface-mount packages to pass large currents. The thermal resistances of these packages are high compared to those of power packages; it is good design practice to check power dissipation and junction temperature. Begin by determining the $r_{DS(on)}$ of the N-channel MOSFET relative to the input voltage and operating temperature. As an initial estimate, use the highest operating ambient temperature of interest and read $r_{DS(on)}$ from Figure 16. Using this value, the power dissipation per switch can be calculated by:

- $P_D = r_{DS(on)} \times I^2$

Multiply this number by the number of switches being used. This step renders the total power dissipation from the N-channel MOSFETs.

The thermal resistance, $R_{\theta JA}$ = 1 / (DERATING FACTOR), where DERATING FACTOR is obtained from the Dissipation Ratings Table. Thermal resistance is a strong function of the printed circuit board construction , and the copper trace area connecting the integrated circuit.

Finally, calculate the junction temperature:

- $T_J = P_D \times R_{\theta JA} + T_A$

Where:

- T_A= Ambient temperature °C
- $R_{\theta JA}$ = Thermal resistance
- P_D = Total power dissipation based on number of switches being used.

Compare the calculated junction temperature with the initial estimate. If they do not agree within a few degrees, repeat the calculation, using the calculated value as the new estimate. Two or three iterations are generally sufficient to get a reasonable answer.

THERMAL PROTECTION

Thermal protection prevents damage to the IC when heavy-overload or short-circuit faults are present for extended periods of time. The TPS2066-Q1 implements a thermal sensing to monitor the operating junction temperature of the power distribution switch. In an overcurrent or short-circuit condition, the junction temperature rises due to excessive power dissipation. Once the die temperature rises above a minimum of 135°C due to overcurrent conditions, the internal thermal sense circuitry turns the power switch off, thus preventing the power switch from damage. Hysteresis is built into the thermal sense circuit, and after the device has cooled approximately 10°C, the switch turns back on. The switch continues to cycle in this manner until the load fault or input power is removed. The $\overline{OC}$x open-drain output is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

UNDERVOLTAGE LOCKOUT (UVLO)

An undervoltage lockout ensures that the power switch is in the off state at power up. Whenever the input voltage falls below approximately 2 V, the power switch is quickly turned off. This facilitates the design of hot-insertion systems where it is not possible to turn off the power switch before input power is removed. The UVLO also keeps the switch from being turned on until the power supply has reached at least 2 V, even if the switch is enabled. On reinsertion, the power switch is turned on, with a controlled rise time to reduce EMI and voltage overshoots.

UNIVERSAL SERIAL BUS (USB) APPLICATIONS

The universal serial bus (USB) interface is a 12-Mb/s, or 1.5-Mb/s, multiplexed serial bus designed for low-to-medium bandwidth PC peripherals (e.g., keyboards, printers, scanners, and mice). The four-wire USB interface is conceived for dynamic attach-detach (hot plug-unplug) of peripherals. Two lines are provided for differential data, and two lines are provided for 5-V power distribution.

USB data is a 3.3-V level signal, but power is distributed at 5 V to allow for voltage drops in cases where power is distributed through more than one hub across long cables. Each function must provide its own regulated 3.3 V from the 5-V input or its own internal power supply.

The USB specification defines the following five classes of devices, each differentiated by power-consumption requirements:

- Hosts/self-powered hubs (SPH)
- Bus-powered hubs (BPH)
- Low-power, bus-powered functions
- High-power, bus-powered functions
- Self-powered functions

SPHs and BPHs distribute data and power to downstream functions. The TPS2066-Q1 has higher current capability than required by one USB port; so, it can be used on the host side and supplies power to multiple downstream ports or functions.

HOST/SELF-POWERED AND BUS-POWERED HUBS

Hosts and SPHs have a local power supply that powers the embedded functions and the downstream ports (see Figure 23). This power supply must provide from 5.25 V to 4.75 V to the board side of the downstream connection under full-load and no-load conditions. Hosts and SPHs are required to have current-limit protection and must report overcurrent conditions to the USB controller. Typical SPHs are desktop PCs, monitors, printers, and stand-alone hubs.

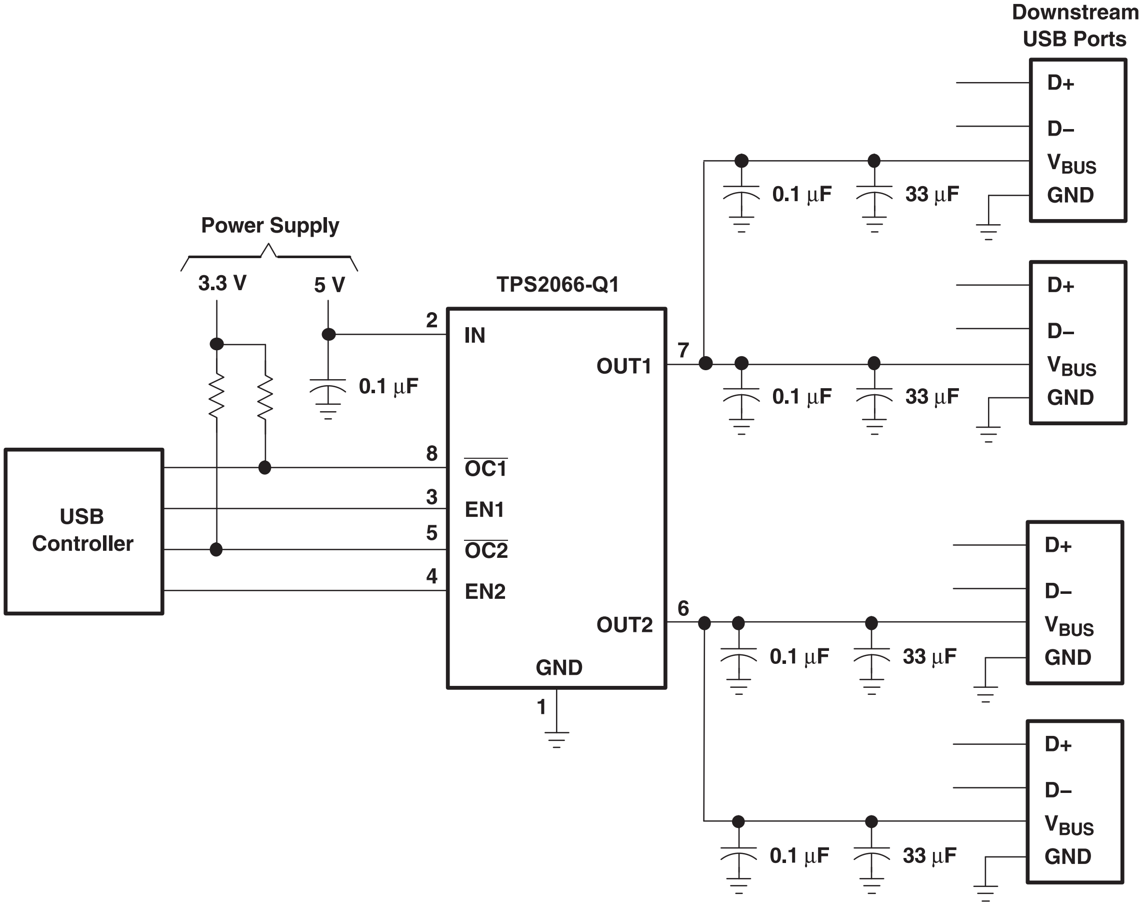


Figure 23. Typical Four-Port USB Host / Self-Powered Hub

BPHs obtain all power from upstream ports and often contain an embedded function. The hubs are required to power up with less than one unit load. The BPH usually has one embedded function, and power is always available to the controller of the hub. If the embedded function and hub require more than 100 mA on power up, the power to the embedded function may need to be kept off until enumeration is completed. This can be accomplished by removing power or by shutting off the clock to the embedded function. Power switching the embedded function is not necessary if the aggregate power draw for the function and controller is less than one unit load. The total current drawn by the bus-powered device is the sum of the current to the controller, the embedded function, and the downstream ports, and it is limited to 500 mA from an upstream port.

LOW-POWER BUS-POWERED AND HIGH-POWER BUS-POWERED FUNCTIONS

Both low-power and high-power bus-powered functions obtain all power from upstream ports; low-power functions always draw less than 100 mA; high-power functions must draw less than 100 mA at power up and can draw up to 500 mA after enumeration. If the load of the function is more than the parallel combination of 44 Ω and 10 µF at power up, the device must implement inrush current limiting (see Figure 24). With TPS2066-Q1, the internal functions could draw more than 500 mA, which fits the needs of some applications such as motor driving circuits.

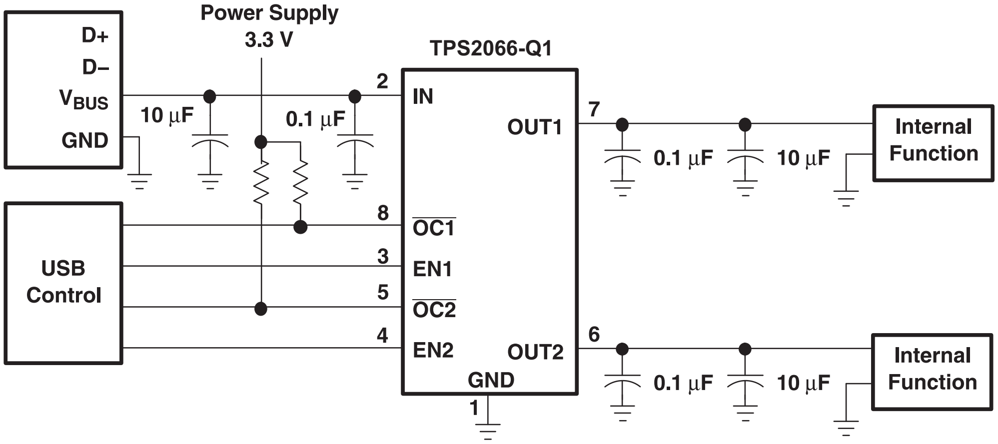


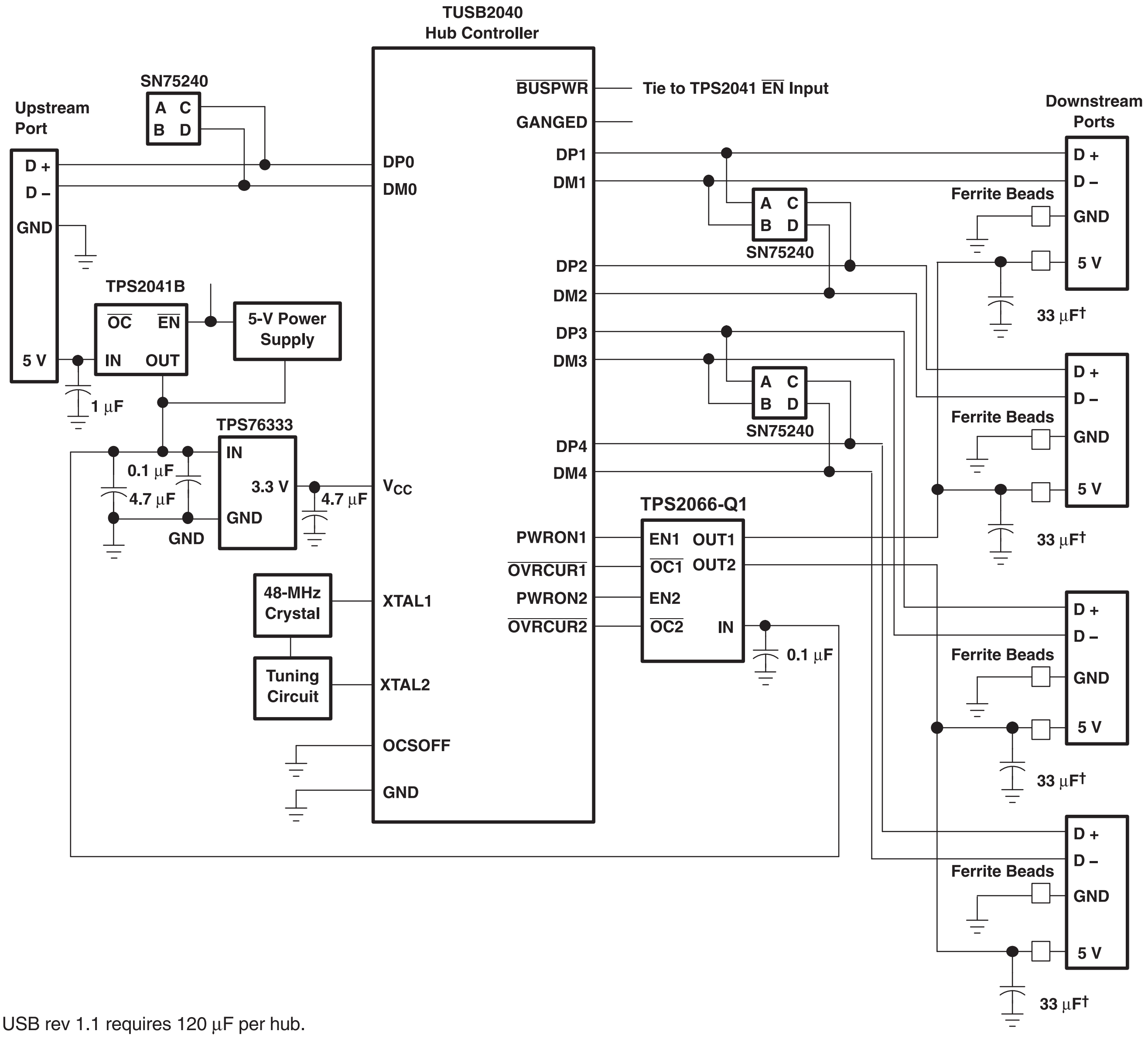
Figure 24. High-Power Bus-Powered Function

USB POWER-DISTRIBUTION REQUIREMENTS

USB can be implemented in several ways, and, regardless of the type of USB device being developed, several power-distribution features must be implemented.

- Hosts/SPHs must:
  - Current-limit downstream ports
  - Report overcurrent conditions on USB V_{BUS}
- BPHs must:
  - Enable/disable power to downstream ports
  - Power up at <100 mA
  - Limit inrush current (<44 Ω and 10 µF)
- Functions must:
  - Limit inrush currents
  - Power up at <100 mA

The feature set of the TPS2066-Q1 allows them to meet each of these requirements. The integrated current-limiting and overcurrent reporting is required by hosts and self-powered hubs. The logic-level enable and controlled rise times meet the need of both input and output ports on bus-powered hubs, as well as the input ports for bus-powered functions (see Figure 25).



† USB rev 1.1 requires 120 µF per hub.

Figure 25. Hybrid Self / Bus-Powered Hub Implementation

GENERIC HOT-PLUG APPLICATIONS

In many applications it may be necessary to remove modules or pc boards while the main unit is still operating. These are considered hot-plug applications. Such implementations require the control of current surges seen by the main power supply and the card being inserted. The most effective way to control these surges is to limit and slowly ramp the current and voltage being applied to the card, similar to the way in which a power supply normally turns on. Due to the controlled rise times and fall times of the TPS2066-Q1, these devices can be used to provide a softer start-up to devices being hot-plugged into a powered system. The UVLO feature of the TPS2066-Q1 also ensures that the switch is off after the card has been removed, and that the switch is off during the next insertion. The UVLO feature insures a soft start with a controlled rise time for every insertion of the card or module.

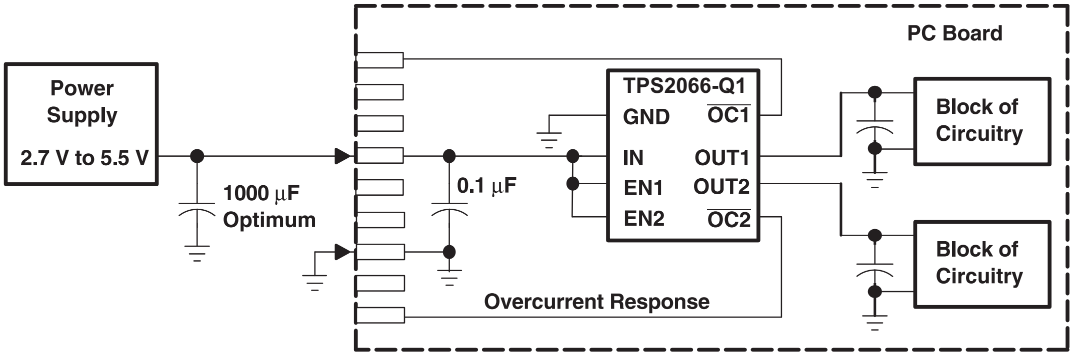


Figure 26. Typical Hot-Plug Implementation

By placing the TPS2066-Q1 between the V_{CC} input and the rest of the circuitry, the input power reaches these devices first after insertion. The typical rise time of the switch is approximately 1 ms, providing a slow voltage ramp at the output of the device. This implementation controls system surge currents and provides a hot-plugging mechanism for any device.

DETAILED DESCRIPTION

Power Switch

The power switch is an N-channel MOSFET with a low on-state resistance. Configured as a high-side switch, the power switch prevents current flow from OUT to IN and IN to OUT when disabled. The power switch supplies a minimum current of 1 A.

Charge Pump

An internal charge pump supplies power to the driver circuit and provides the necessary voltage to pull the gate of the MOSFET above the source. The charge pump operates from input voltages as low as 2.7 V and requires little supply current.

Driver

The driver controls the gate voltage of the power switch. To limit large current surges and reduce the associated electromagnetic interference (EMI) produced, the driver incorporates circuitry that controls the rise times and fall times of the output voltage.

Enable ($\overline{\text{ENx}}$ or ENx)

The logic enable disables the power switch and the bias for the charge pump, driver, and other circuitry to reduce the supply current. The supply current is reduced to less than 1 µA when a logic high is present on $\overline{\text{ENx}}$, or when a logic low is present on ENx. A logic zero input on $\overline{\text{ENx}}$, or a logic high input on ENx restores bias to the drive and control circuits and turns the switch on. The enable input is compatible with both TTL and CMOS logic levels.

Overcurrent ($\overline{\text{OCx}}$)

The $\overline{\text{OCx}}$ open-drain output is asserted (active low) when an overcurrent or overtemperature condition is encountered. The output remains asserted until the overcurrent or overtemperature condition is removed. A 10-ms deglitch circuit prevents the $\overline{\text{OCx}}$ signal from oscillation or false triggering. If an overtemperature shutdown occurs, the $\overline{\text{OCx}}$ is asserted instantaneously.

Current Sense

A sense FET monitors the current supplied to the load. The sense FET measures current more efficiently than conventional resistance methods. When an overload or short circuit is encountered, the current-sense circuitry sends a control signal to the driver. The driver in turn reduces the gate voltage and drives the power FET into its saturation region, which switches the output into a constant-current mode and holds the current constant while varying the voltage on the load.

Thermal Sense

The TPS2066-Q1 implements a thermal sensing to monitor the operating temperature of the power distribution switch. In an overcurrent or short-circuit condition the junction temperature rises. When the die temperature rises to approximately 140°C due to overcurrent conditions, the internal thermal sense circuitry turns off the switch, thus preventing the device from damage. Hysteresis is built into the thermal sense, and after the device has cooled approximately 10 degrees, the switch turns back on. The switch continues to cycle off and on until the fault is removed. The open-drain false reporting output ($\overline{\text{OCx}}$) is asserted (active low) when an overtemperature shutdown or overcurrent occurs.

Undervoltage Lockout

A voltage sense circuit monitors the input voltage. When the input voltage is below approximately 2 V, a control signal turns off the power switch.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2066TDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2066Q
TPS2066TDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2066Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TPS2066-Q1 :

- Catalog : TPS2066

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

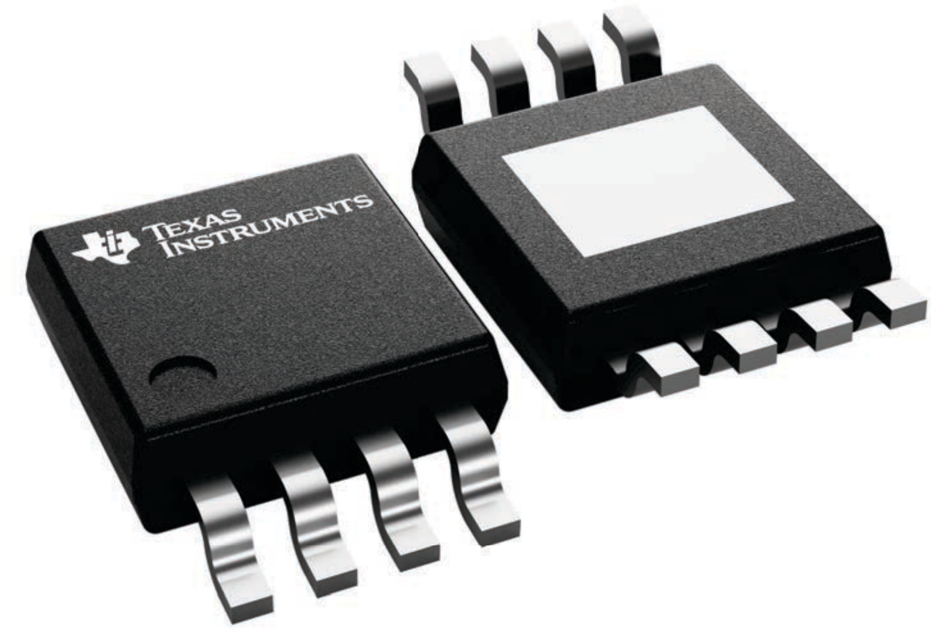
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

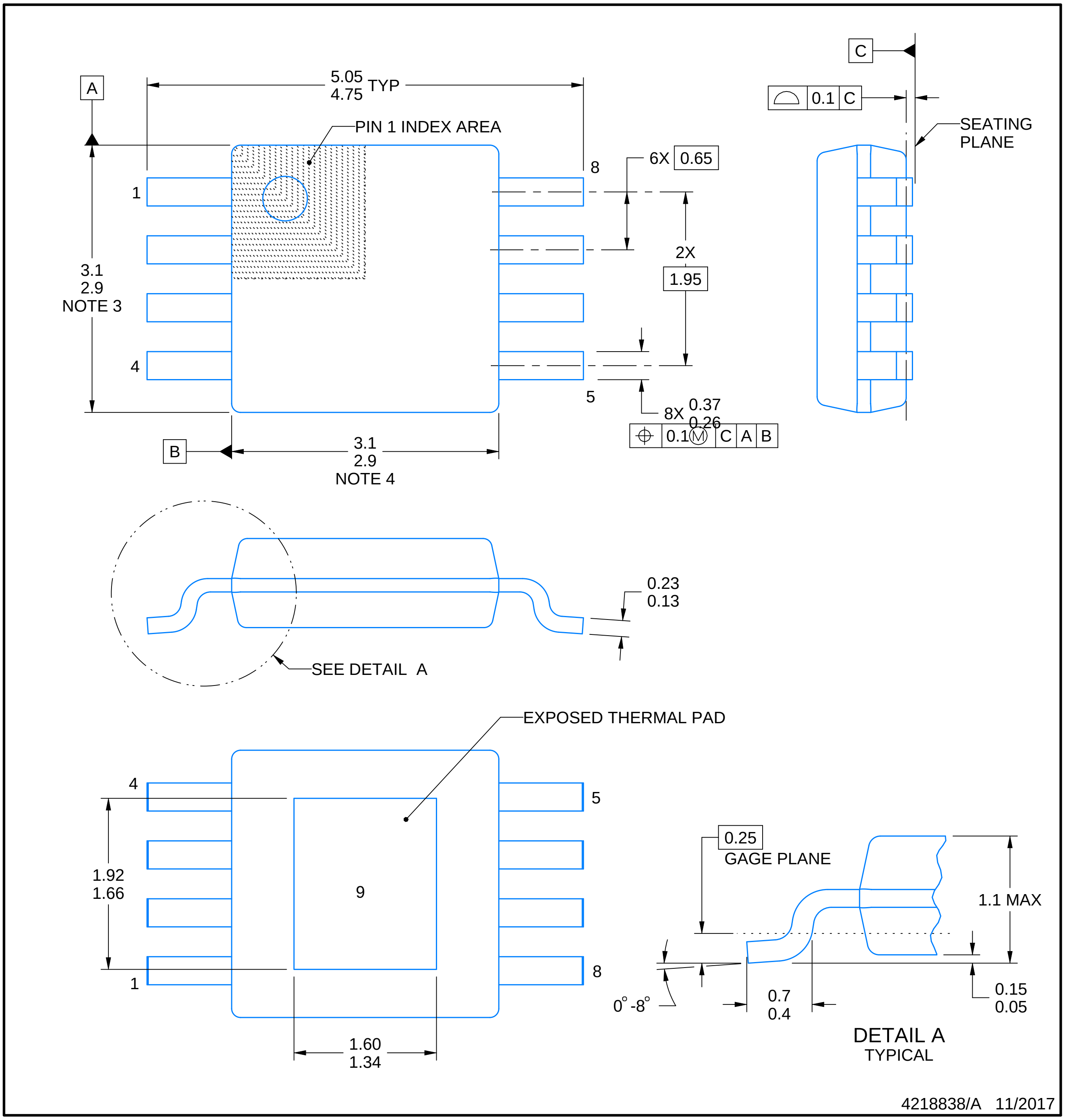
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

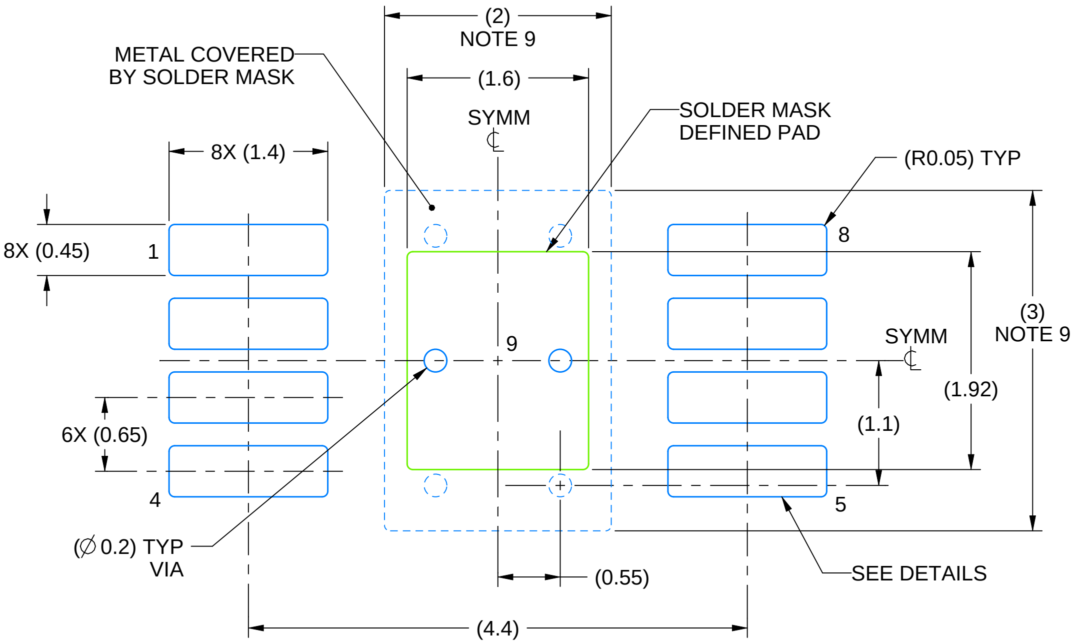
HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

NON-SOLDER MASK
DEFINED
(PREFERRED)

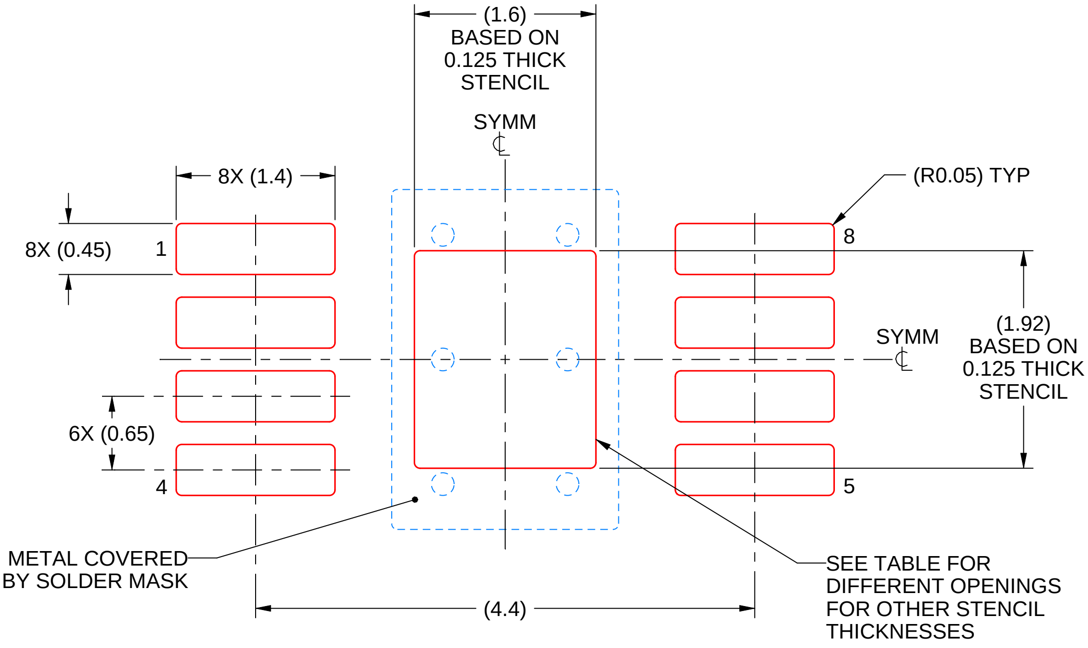
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4218838/A 11/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明