用于电源门控的毫微级功耗系统计时器 TPL5110-Q1 AEC-Q100

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C5
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 电压为 2.5V 时，电流消耗为 35nA（典型值）
- 电源电压范围为 1.8V 至 5.5V
- 可选计时间隔：100ms 至 7200s
- 计时器精度：1%（典型值）
- 可通过电阻选择时间间隔
- 手动为 MOSFET 上电
- 单次触发功能
- TPL5x10Q 系列 AEC-Q100 毫微级功耗系统计时器：
  - **TPL5010-Q1**：具备可编程延迟范围的看门狗功能
  - **TPL5110-Q1**：具有可编程延迟范围和单次触发特性的 MOS 驱动器

2 应用

- 电动汽车
- 电池供电型系统
- 离合器执行器电路
- 车门把手电路
- 智能钥匙
- 远程电流传感器
- 入侵者检测

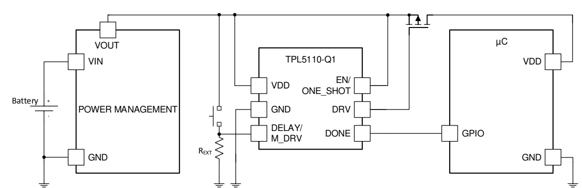
3 说明

TPL5110-Q1 毫微级计时器是一种集成了 MOSFET 驱动器且通过 AEC-Q100 认证的低功耗计时器，非常适合占空比或电池供电型应用中的电源门控。TPL5110-Q1 的电流消耗仅为 35nA，可用于支持电源线路，并大幅降低系统睡眠期间的总待机电流。利用这一节能特性可以明显缩小电池尺寸，使得 TPL5111 成为能量采集或无线传感器应用的理想选择。TPL5110-Q1 可提供 100ms 至 7200s 的可选计时间隔，适用于电源门控应用。此外，TPL5110-Q1 还具有独特的单次触发功能，计时器可仅在一个周期内为 MOSFET 供电。TPL5110-Q1 采用 6 引脚 SOT23 封装。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TPL5110-Q1	SOT23 (6)	3.00mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用原理图

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4 Revision History

Changes from Revision * (February 2017) to Revision A (September 2021)	Page
• 向*特性* 部分添加了功能安全要点	1

Device Comparison Table

表 5-1. TPL5x10Q Family of AEC-Q100 Nano- Power System Timers

PART NUMBER	SUPPLY CURRENT (Typ)	SPECIAL FEATURES
TPL5010-Q1	35 nA	Low Power Timer
		Watchdog Function
		Programmable Delay Range
		Manual Reset
TPL5110-Q1	35 nA	Low Power Timer
		MOS-Driver
		Programmable Delay Range
		Manual Reset
		One-Shot Feature

5 Pin Configuration and Functions

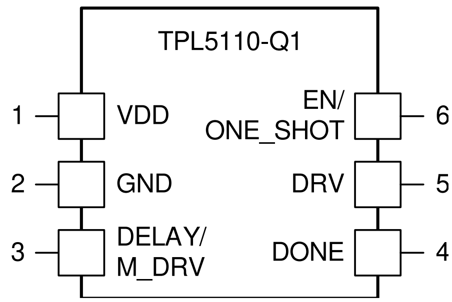


图 **5-1. SOT-23 6-Lead DDC Top View**

表 **5-1. Pin Functions**

PIN		TYPE[(1)]	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VDD	P	Supply voltage	
2	GND	G	Ground	
3	DELAY/ M_DRV	I	Time interval set and manual MOSFET Power ON	Resistance between this pin and GND is used to select the time interval. The manual MOSFET power ON switch is also connected to this pin.
4	DONE	I	Logic Input for watchdog functionality	Digital signal driven by the µC to indicate successful processing.
5	DRV	O	Power Gating output signal generated every t_{IP}	The Gate of the MOSFET is connected to this pin. When DRV = LOW, the MOSFET is ON.
6	EN/ ONE_SHOT	I	Selector of mode of operation	When EN/ONE_SHOT = HIGH, the TPL5110-Q1 works as a TIMER. When EN/ONE_SHOT = LOW, the TPL5110-Q1 turns on the MOSFET one time for the programmed time interval. The next power on of the MOSFET is enabled by the manual power ON.

(1) G= Ground, P= Power, O= Output, I= Input.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

	MIN	MAX	UNIT
Supply voltage (VDD-GND)	-0.3	6.0	V
Input voltage at any pin[(3)]	-0.3	VDD + 0.3	V
Input Current on any pin	-5	+5	mA
Storage temperature, T_{stg}	-65	150	°C
Junction temperature, TJ[(2)]		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation is a function of T_J(MAX), θ JA, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is PDMAX = (T_J(MAX) - T_A)/ θ JA. All numbers apply for packages soldered directly onto a PC board.
(3) The voltage between any two pins should not exceed 6V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human Body Model, per AEC Q100-002[(1)]	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JADEC JS-001 specification.

6.3 Recommended Operating Ratings

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.5	V
Temperature Range	−40	125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TPL5110-Q1 SOT-23 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	57	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Specifications are for T_A= 25°C, VDD-GND=2.5 V, unless otherwise stated.(1)

	PARAMETER	TEST CONDITIONS		MIN(2)	TYP(3)	MAX(2)	UNIT
POWER SUPPLY							
IDD	Supply current(4)	Operation mode			35	50	nA
		Digital conversion of external resistance (Rext)			200	400	µA
TIMER							
t_{IP}	Time interval Period(5)	1650 selectable Time intervals	Min time interval		100		ms
			Max time interval		7200		s
	Time interval Setting Accuracy(7)	Excluding the precision of Rext			±0.6%		
	Time interval Setting Accuracy over supply voltage	1.8V ≤ VDD ≤ 5.5V			±25		ppm/V
t_{OSC}	Oscillator Accuracy			–0.5%		0.5%	
	Oscillator Accuracy over temperature(5)	–40°C ≤ T_A ≤ 125°C			150		ppm/°C
	Oscillator Accuracy over supply voltage(5)	1.8V ≤ VDD ≤ 5.5V			±0.4		%/V
	Oscillator Accuracy over life time(6)				±0.24%		
t_{DONE}	Minimum DONE Pulse width (5)				100		ns
t_{DRV}	DRV Pulse width	DONE signal not received			t_{IP} – 50ms		
t_Rext	Time to convert Rext (5)				100		ms
DIGITAL LOGIC LEVELS							
VIH	Minimum Logic High Threshold DONE pin				0.7xVDD		V
VIL	Maximum Logic Low Threshold DONE pin				0.3xVDD		V
VOH	Logic output High Level DRV pin	Iout = 100 µA		VDD – 0.3			V
		Iout = 1 mA		VDD – 0.7			V
VOL	Logic output Low Level DRV pin	Iout = –100 µA				0.3	V
		Iout = –1 mA				0.7	V
VIH_{M_DRV}	Minimum Logic High Threshold DELAY/M_DRV pin (5)				1.5		V

(1) Electrical Characteristics Table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J = T_A. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where T_J > T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
(2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
(4) The supply current excludes load and pull-up resistor current. Input pins are at GND or VDD.
(5) This parameter is specified by design and/or characterization and is not tested in production.
(6) Operational life time test procedure equivalent to10 years.
(7) The accuracy for time interval settings below 1second is ±100ms.

6.6 Timing Requirements

			MIN[3]	NOM[4]	MAX[3]	UNIT
tr_{DRV}	Rise Time DRV[2]	Capacitive load 50 pF		50		ns
tf_{DRV}	Fall Time DRV[2]	Capacitive load 50 pF		50		ns
tD_{DONE}	DONE to DRV delay	Min delay[1]		100		ns
		Max delay [1]		t_{DRV}		
t_{M_DRV}	Minimum Valid manual MOSFET Power ON	Observation time 30ms		20		ms
t_{DB}	De-bounce manual MOSFET Power ON			20		ms

(1) from DRV falling edge.
(2) This parameter is specified by design and/or characterization and is not tested in production.
(3) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

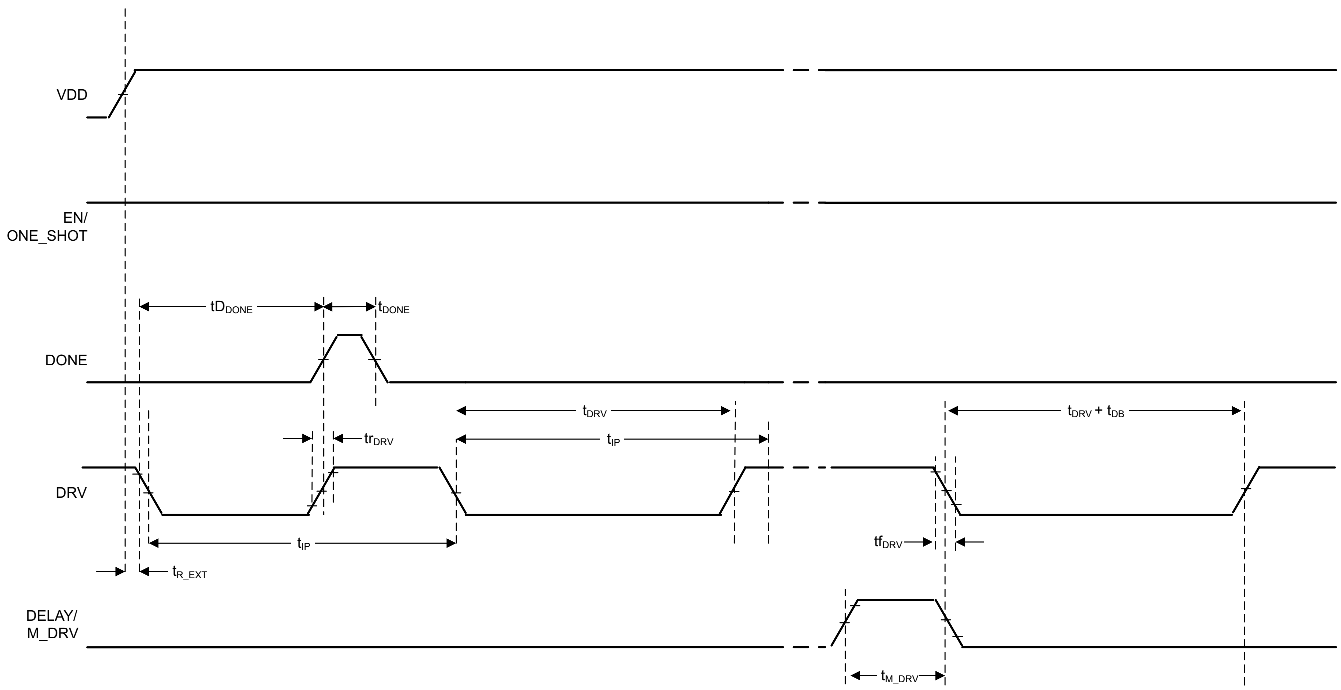


图 6-1. TPL5110-Q1 Timing

6.7 Typical Characteristics

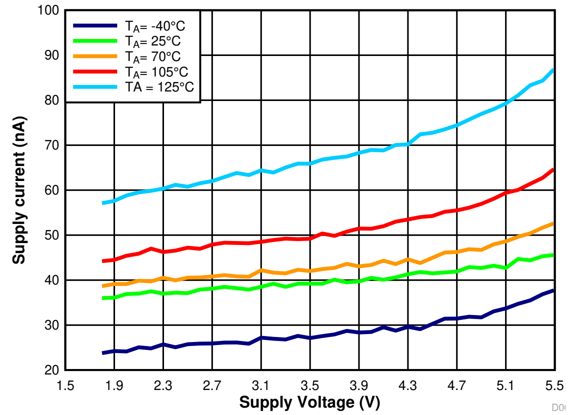


图 6-2. I_{DD} vs. V_{DD}

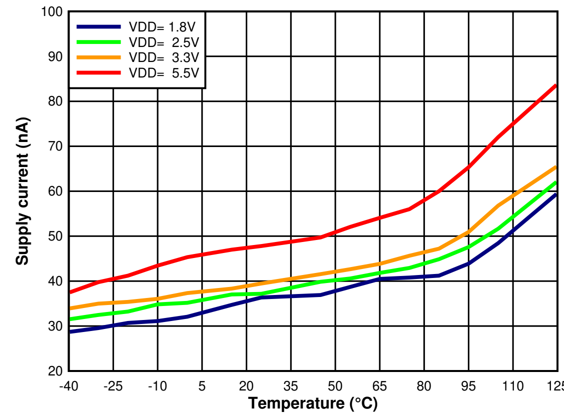
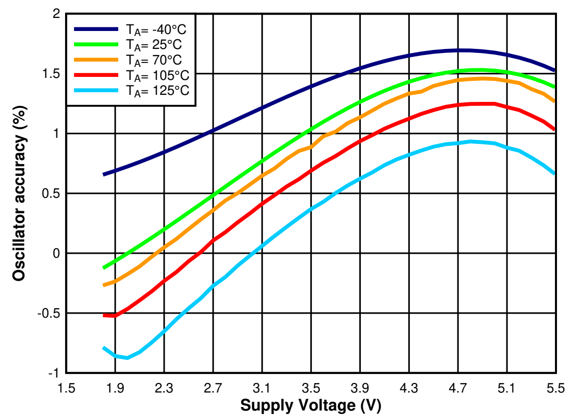


图 6-3. I_{DD} vs. Temperature



A.

图 6-4. Oscillator Accuracy vs. V_{DD}

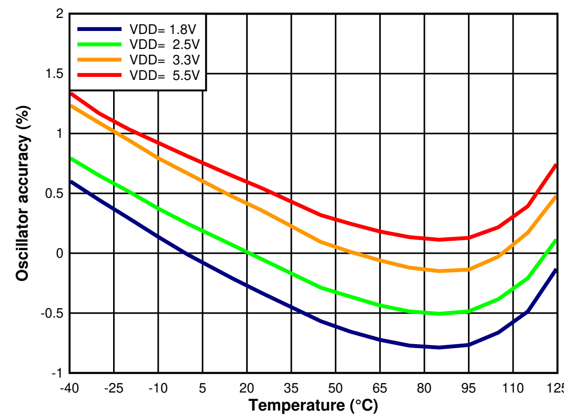


图 6-5. Oscillator Accuracy vs. Temperature

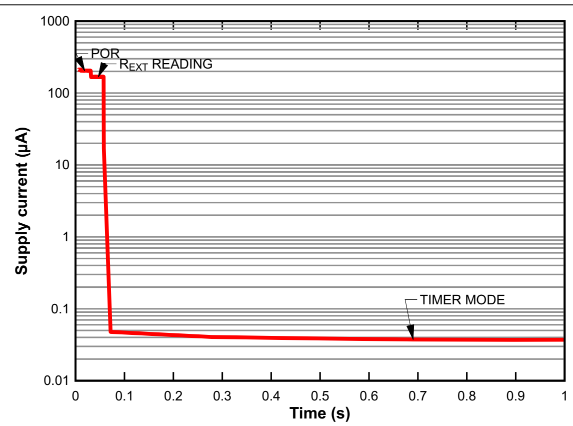
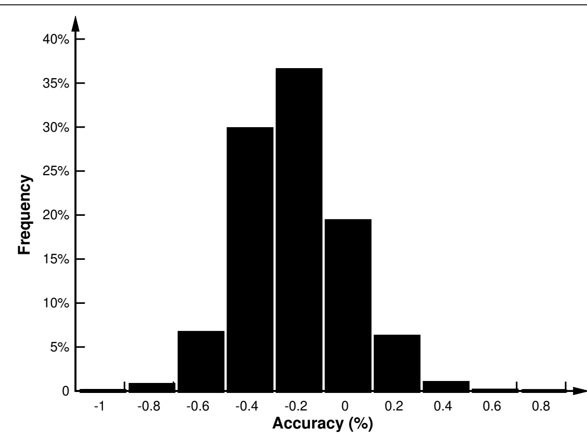


图 6-6. I_{DD} vs. Time



number of observations >20000 1s < t_{IP} ⩽ 7200s

图 6-7. Time Interval Setting Accuracy

7 Detailed Description

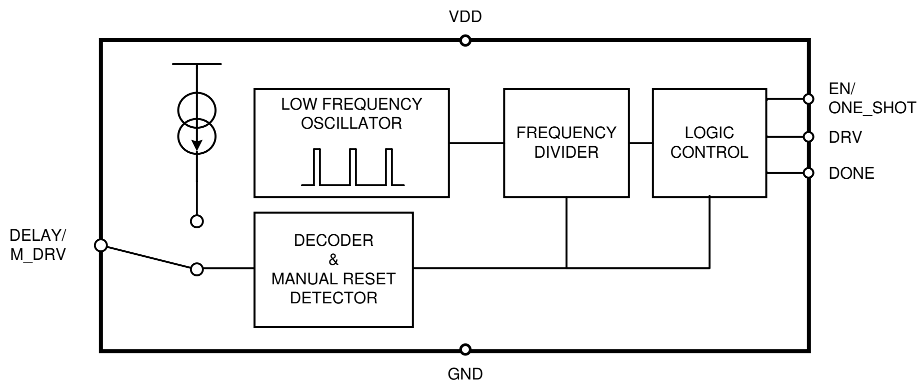
7.1 Overview

The TPL5110-Q1 is a timer with power gating feature. It is ideal for use in power-cycled applications and provides selectable timing from 100ms to 7200s.

Once configured in timer mode (EN/ONE_SHOT= HIGH) the TPL5110-Q1 periodically sends out a DRV signal to a MOSFET to turn on the µC. If the µC replies with a DONE signal within the programmed time interval (t_{DRV}) the TPL5110-Q1 turns off the µC, otherwise the TPL5110-Q1 keeps the µC in the on state for a time equal to t_{DRV}.

The TPL5110-Q1 can work also in a one-shot mode (EN/ONE_SHOT= LOW). In this mode the DRV signal is sent out just one time at the power on of the TPL5110-Q1 to turn on the µC. If the µC replies with a DONE signal within the programmed time interval (t_{DRV}) the TPL5110-Q1 turns off the µC, otherwise the TPL5110-Q1 keeps the µC in the on state for a time equal to t_{DRV}.

7.2 Functional Block Diagram



7.3 Feature Description

The TPL5110-Q1 implements a periodical power gating feature or one shot power gating according to the EN/ONE_SHOT voltage. A manual MOSFET Power ON function is realized by momentarily pulling the DELAY/M_DRV pin to VDD.

7.3.1 DRV

The gate of the MOSFET is connected to the DRV pin. When DRV= LOW, the MOSFET is turned ON. The pulse generated at DRV is equal to the selected time interval period, minus 50ms. It is shorter in the case of a DONE signal received from the µC. If the DONE signal is not received within the programmed time interval (minus 50ms), the DRV signal will be high for the last 50ms of the time interval in order to turn off the MOSFET before the next cycle starts.

The default value (after resistance reading) is HIGH. The signal is sent out from the TPL5110-Q1 when the programmed time interval starts. When the DRV is LOW, the manual power ON signal is ignored.

7.3.2 DONE

The DONE pin is driven by a µC to signal that the µC is working properly. The TPL5110-Q1 recognizes a valid DONE signal as a low to high transition; if two or more DONE signals are received within the time interval, only the first DONE signal is processed. The minimum DONE signal pulse length is 100ns. When the TPL5110-Q1 receives the DONE signal it asserts DRV logic HIGH.

7.4 Device Functional Modes

7.4.1 Start-Up

During start-up, after POR, the TPL5110-Q1 executes a one-time measurement of the resistance attached to the DELAY/M_DRV pin in order to determine the desired time interval for DRV. This measurement interval is t_{R_EXT}. During this measurement a constant current is temporarily flowing into R_{EXT}.

Once the reading of the external resistance is completed the TPL5110-Q1 enters automatically in one of the 2 modes according to the EN/ONE_SHOT value. The EN/ONE_SHOT pin must be hard wired to GND or VDD according to the required mode of operation.

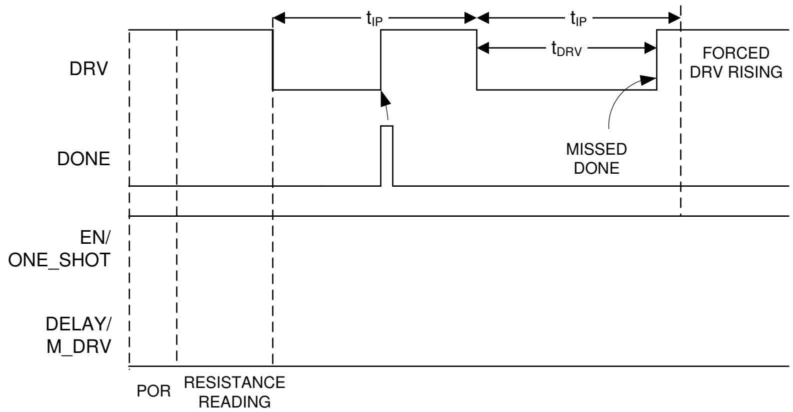


图 7-1. Start-Up - Timer Mode

7.4.2 Timer Mode

During timer mode (EN/ONE_SHOT = HIGH), the TPL5110-Q1 asserts periodic DRV pulses according to the programmed time interval. The length of the DRV pulses is set by the receiving of a DONE pulse from the uC. See 图 7-1.

7.4.3 One-Shot Mode

During one-shot mode (EN/ONE_SHOT = LOW), the TPL5110-Q1 generates just one pulse at the DRV pin which lasts according to the programmed time interval. In one-shot mode, other DRV pulses can be triggered using the DELAY/M_DRV pin. If a valid manual power ON occurs when EN/ONE_SHOT is LOW, the TPL5110-Q1 generates just one pulse at the DRV pin. The duration of the pulse is set by the programmed time interval. Also in this case, if a DONE signal is received within the programmed time interval (minus 50ms), the MOSFET connected to the DRV pin is turned off. See 图 7-2 and 图 7-3.

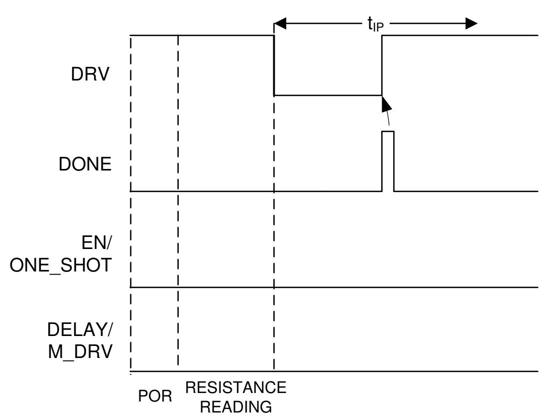


图 7-2. Start-Up One-Shot Mode, (DONE Received Within t_{IP})

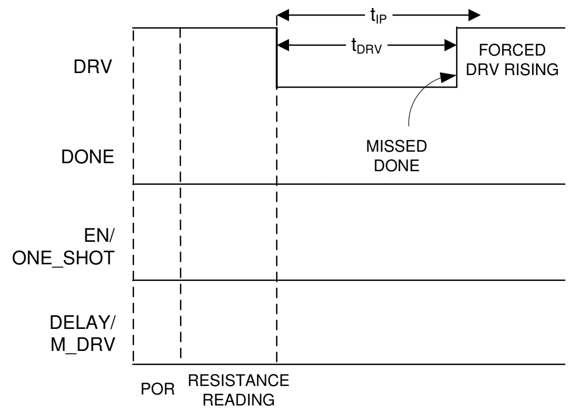


图 7-3. Start-Up One-Shot Mode, (No DONE Received Within t_{IP})

7.5 Programming

7.5.1 Configuring the Time Interval with the DELAY/M_DRV Pin

The time interval between 2 adjacent DRV pulses (falling edges, in timer mode) is selectable through an external resistance (R_{EXT}) between the DELAY/M_DRV pin and ground. The resistance (R_{EXT}) must be in the range between 500 Ω and 170k Ω. At least a 1% precision resistance is recommended. See section 节 7.5.3 on how to set the time interval using R_{EXT}.

7.5.2 Manual MOSFET Power ON Applied to the DELAY/M_DRV Pin

If VDD is connected to the DELAY/M_DRV pin, the TPL5110-Q1 recognizes this as a manual MOSFET Power ON condition. In this case the time interval is not set. If the manual MOSFET Power ON is asserted during the POR or during the reading procedure, the reading procedure is aborted and is re-started as soon as the manual MOSFET Power ON switch is released. A pulse on the DELAY/M_DRV pin is recognized as a valid manual MOSFET Power ON only if it lasts at least 20ms (observation time is 30ms). The manual MOSFET Power ON may be implemented using a switch (momentary mechanical action).

If the DRV is already LOW (MOSFET ON) the manual MOSFET Power ON is ignored.

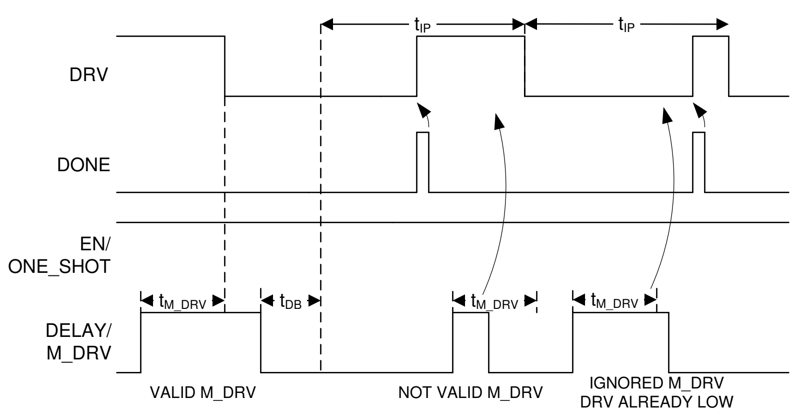


图 7-4. Manual MOSFET Power ON in Timer Mode

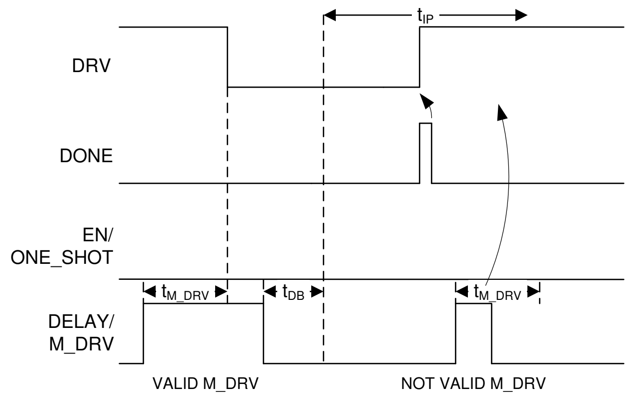


图 7-5. Manual MOSFET Power ON in One-Shot Mode

7.5.2.1 DELAY/M_DRV

A resistance in the range between 500 Ω and 170k Ω must to be connected to the DELAY/M_DRV pin in order to select a valid time interval. At the POR and during the reading of the resistance, the DELAY/M_DRV is connected to an analog signal chain through a mux. After the reading of the resistance, the analog circuit is switched off and the DELAY/M_DRV is connected to a digital circuit.

In this state, a logic HIGH applied to the DELAY/M_DRV pin is interpreted by the TPL5110-Q1 as a manual power ON. The manual power ON detection is provided with a de-bounce feature (on both edges) which makes the TPL5110-Q1 insensitive to the glitches on the DELAY/M_DRV.

The M_DRV must stay high for at least 20ms to be valid. Once a valid signal at DELAY/M_DRV is understood as a manual power on, the DRV signal will be asserted in the next 10ms. Its duration will be according to the programmed time interval (minus 50ms), or less if the DONE is received.

A manual power ON signal resets all the counters. The counters will restart as soon as a valid manual power ON signal is recognized and the signal at DELAY/M_DRV pin is asserted LOW. Due to the asynchronous nature of the manual power ON signal and its arbitrary duration, the LOW status of the DRV signal may be affected by an uncertainty of about ±5ms.

An extended assertion of a logic HIGH at the DELAY/M_DRV pin will turn on the MOSFET for a time longer than the programmed time interval. DONE signals received while the DELAY/M_DRV is HIGH are ignored. If the DRV is already LOW (MOSFET ON) the manual power ON is ignored.

7.5.2.2 Circuitry

The manual Power ON may be implemented using a switch (momentary mechanical action). The TPL5110-Q1 offers 2 possible approaches according to the power consumption constraints of the application.

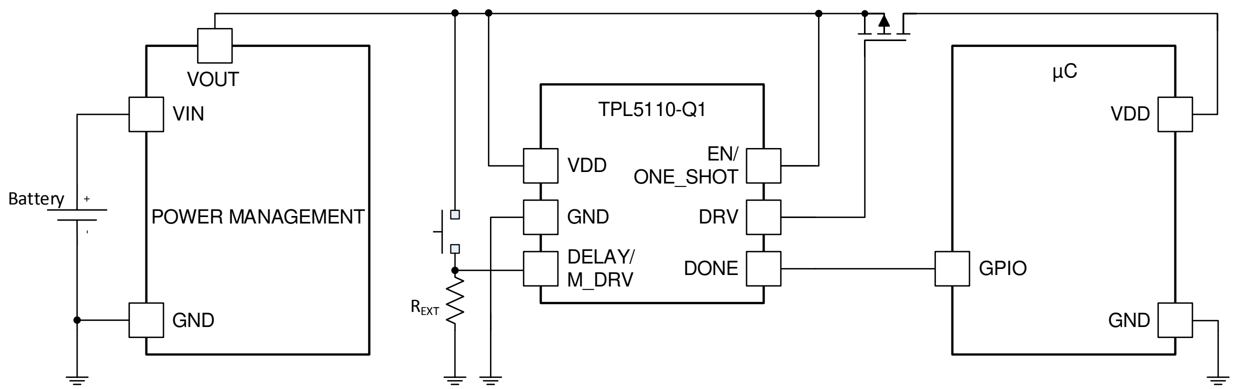


图 7-6. Manual MOSFET Power ON with SPST Switch

For use cases that do not require the lowest power consumption, using a single pole single throw switch may offer a lower cost solution. The DELAY/M_DRV pin may be directly connected to VDD with R_{EXT} in the circuit. The current drawn from the supply voltage during the manual power ON is given by VDD/R_{EXT}.

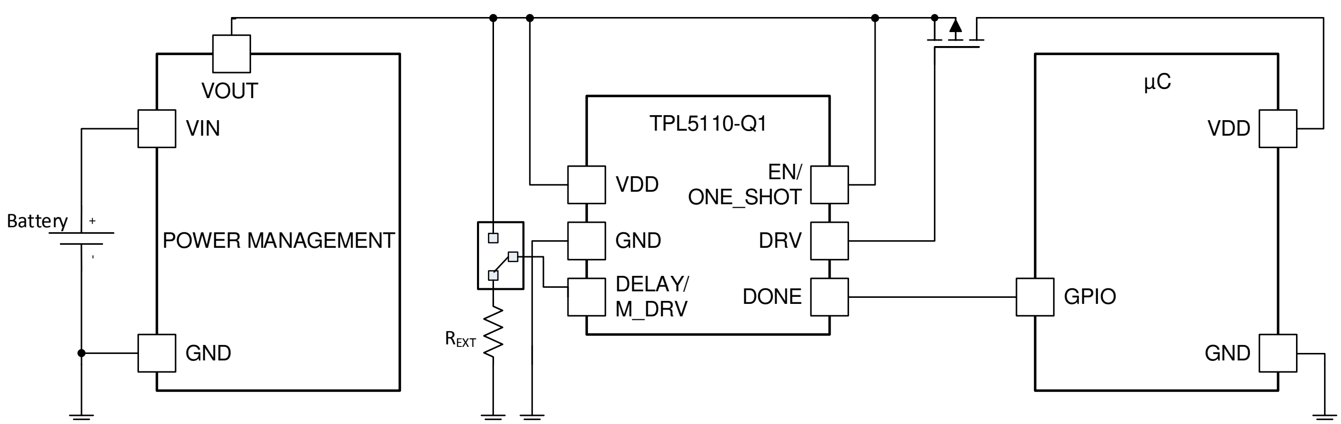


图 7-7. Manual MOSFET Power ON with SPDT Switch

The manual MOSFET Power ON function may also be asserted by switching DELAY/M_DRV from R_{EXT} to VDD using a single pole double throw switch, which will provide a lower power solution for the manual power ON, because no current flows.

7.5.3 Selection of the External Resistance

In order to set the time interval, the external resistance R_{EXT} is selected according the following formula:

$$R_{EXT} = 100\left(\frac{-b+\sqrt{b^2-4a(c-100T)}}{2a}\right) \tag{1}$$

Where:

- **T** is the desired time interval in seconds.
- **R_{EXT}** is the resistance value to use in Ω.
- **a**,**b**,**c** are coefficients depending on the range of the time interval.

表 7-1. Coefficients for 方程式 1

SET	Time Interval Range (s)	a	b	c
1	1 <T⩽ 5	0.2253	-20.7654	570.5679
2	5 <T⩽ 10	-0.1284	46.9861	-2651.8889
3	10 <T⩽ 100	0.1972	-19.3450	692.1201
4	100 <T⩽ 1000	0.2617	-56.2407	5957.7934
5	T> 1000	0.3177	-136.2571	34522.4680

EXAMPLE

Required time interval: 8s

The coefficient set to be selected is the number 2. The formula becomes

$$R_{EXT} = 100\left(\frac{46.9861 - \sqrt{46.9861^2 + 4*0.1284(-2561.8889 - 100*8)}}{2*0.1284}\right) \tag{2}$$

The resistance value is 10.18 kΩ.

The following Look-Up-Tables contain example values of t_{IP} and their corresponding value of R_{EXT}.

表 7-2. First 9 Time Intervals

t_{IP} (ms)	Resistance (Ω)	Closest real value (Ω)	Parallel of two 1% tolerance resistors, (kΩ)
100	500	500	1.0 // 1.0
200	1000	1000	-
300	1500	1500	2.43 // 3.92
400	2000	2000	-
500	2500	2500	4.42 // 5.76
600	3000	3000	5.36 // 6.81
700	3500	3500	4.75 // 13.5
800	4000	4000	6.19 // 11.3
900	4500	4501	6.19 // 16.5

表 7-3. Most Common Time Intervals Between 1s to 2h

t_{IP}	Calculated Resistance (kΩ)	Closest Real Value (kΩ)	Parallel of Two 1% Tolerance Resistors, (kΩ)
1s	5.20	5.202	7.15 // 19.1
2s	6.79	6.788	12.4 // 15.0
3s	7.64	7.628	12.7// 19.1
4s	8.30	8.306	14.7 // 19.1
5s	8.85	8.852	16.5 // 19.1
6s	9.27	9.223	18.2 // 18.7
7s	9.71	9.673	19.1 // 19.6
8s	10.18	10.180	11.5 // 8.87
9s	10.68	10.68	17.8 // 26.7
10s	11.20	11.199	15.0 // 44.2
20s	14.41	14.405	16.9 // 97.6
30s	16.78	16.778	32.4 // 34.8
40s	18.75	18.748	22.6 // 110.0

表 7-3. Most Common Time Intervals Between 1s to 2h (continued)

t_{IP}	Calculated Resistance (kΩ)	Closest Real Value (kΩ)	Parallel of Two 1% Tolerance Resistors, (kΩ)
50s	20.047	20.047	28.7 // 66.5
1min	22.02	22.021	40.2 // 48.7
2min	29.35	29.349	35.7 // 165.0
3min	34.73	34.729	63.4 // 76.8
4min	39.11	39.097	63.4 // 102.0
5min	42.90	42.887	54.9 // 196.0
6min	46.29	46.301	75.0 // 121.0
7min	49.38	49.392	97.6 // 100.0
8min	52.24	52.224	88.7 // 127.0
9min	54.92	54.902	86.6 // 150.0
10min	57.44	57.437	107.0 // 124.0
20min	77.57	77.579	140.0 // 174.0
30min	92.43	92.233	182.0 // 187.0
40min	104.67	104.625	130.0 // 536.00
50min	115.33	115.331	150.0 // 499.00
1h	124.91	124.856	221.0 // 287.00
1h30min	149.39	149.398	165.0 // 1580.0
2h	170.00	170.00	340.0 // 340.0

7.5.4 Quantization Error

The TPL5110-Q1 can generate 1650 discrete timer intervals in the range of 100ms to 7200s. The first 9 intervals are multiples of 100ms. The remaining 1641 intervals cover the range between 1s to 7200s. Because they are discrete intervals, there is a quantization error associated with each value.

The quantization error can be evaluated according to the following formula:

$$Err = 100\frac{(T_{DESIRED} - T_{ADC})}{T_{DESIRED}} \quad (3)$$

Where:

$$T_{ADC} = INT\left[\frac{1}{100}\left(a\frac{R_D^2}{100^2} + b\frac{R_D}{100} + c\right)\right] \quad (4)$$

$$R_D = INT\left[\frac{R_{EXT}}{100}\right] \quad (5)$$

R_{EXT} is the resistance calculated with 方程式 1 and a,b,c are the coefficients of the equation listed in 表 7-1.

7.5.5 Error Due to Real External Resistance

R_{EXT} is a theoretical value and may not be available in standard commercial resistor values. It is possible to closely approach the theoretical R_{EXT} using two or more standard values in parallel. However, standard values are characterized by a certain tolerance. This tolerance will affect the accuracy of the time interval.

The accuracy can be evaluated using the following procedure:

1. Evaluate the min and max values of R_{EXT} (R_{EXT_MIN}, R_{EXT_MAX} with 方程式 1 using the selected commercial resistance values and their tolerances.
2. Evaluate the time intervals ($T_{ADC\_MIN}[R_{EXT\_MIN}]$, $T_{ADC\_MAX}[R_{EXT\_MAX}]$) with 方程式 4.

3. Find the errors using 方程式 3 with T_{ADC_MIN}, T_{ADC_MAX}.

The results of the formula indicate the accuracy of the time interval.

The example below illustrates the procedure.

- Desired time interval , T_desired = 600s,
- Required R_{EXT}, from 方程式 1, R_{EXT}= 57.44kΩ.

From 表 7-3, R_{EXT} can be built with a parallel combination of two commercial values with 1% tolerance: R1=107kΩ, R2=124kΩ. The uncertainty of the equivalent parallel resistance can be found using:

$$uR_{//} = R_{//}\sqrt{\left(\frac{u_{R1}}{R1}\right)^2 + \left(\frac{u_{R2}}{R2}\right)^2} \quad (6)$$

Where uRn (n=1,2) represent the uncertainty of a resistance,

$$u_{Rn} = Rn\frac{Tolerance}{\sqrt{3}} \quad (7)$$

The uncertainty of the parallel resistance is 0.82%, meaning the value of R_{EXT} may range between R_{EXT_MIN} = 56.96 kΩ and R_{EXT_MAX} = 57.90 kΩ.

Using these value of R_{EXT}, the digitized timer intervals calculated with 方程式 4 are respectively T_{ADC_MIN} = 586.85 s and T_{ADC_MAX} = 611.3 s, giving an error range of -1.88% / +2.19%. The asymmetry of the error range is due to the quadratic transfer function of the resistance digitizer.

8 Application and Implementation

Note

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

In battery powered applications one design constraint is the need for low current consumption. The TPL5110-Q1 is suitable in applications where there is a need to monitor environmental conditions at a fixed time interval. Often in these applications a watchdog or other internal timer in a µC is used to implement a wakeup function. Typically, the power consumption of these functions is not optimized. Using the TPL5110-Q1 to implement a periodical power gating of the µC or of the entire system the current consumption will be only tens of nA.

8.2 Typical Application

The TPL5110-Q1 can be used in environment sensor nodes such as humidity and temperature sensor node. The sensor node has to measure the humidity and the temperature and transmit the data through a low power RF micro such as the CC2531. Since the temperature and the humidity in home application do not change so fast, the measurement and the transmission of the data can be done at very low rate, such as every 30 seconds. The RF micro should spend most of the time in counting the elapsed time, but using the TPL5110-Q1 it is possible to complete turn off the RF micro and extend the battery life. The TPL5110-Q1 will turn on the RF micro when the programmed time interval elapses or for debug purpose with the manual MOSFET Power ON switch.

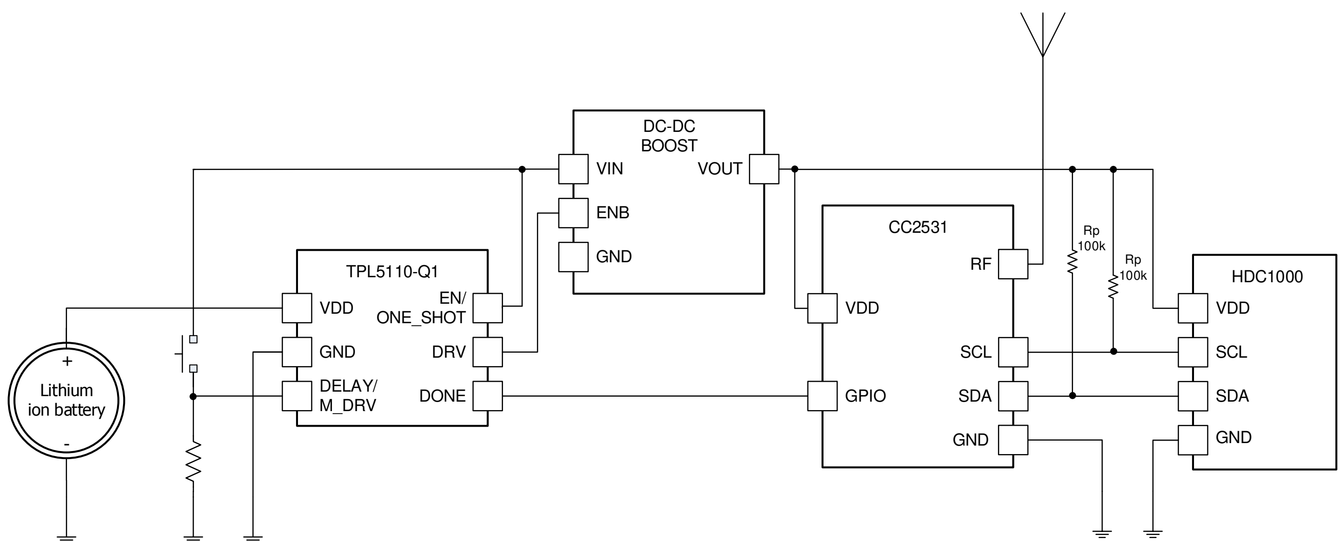


图 8-1. Sensor Node

8.2.1 Design Requirements

The Design is driven by the low current consumption constraint. The data are usually acquired on a rate which is in the range between 30s and 60s. The highest necessity is the maximization of the battery life. The TPL5110-Q1 helps achieve this goal because it allows turning off the RF micro.

8.2.2 Detailed Design Procedure

When the focal constraint is the battery life, the selection of a low power voltage regulator and low leakage MOSFET to power gate the µC is mandatory. The first step in the design is the calculation of the power consumption of each device in the different mode of operations. An example is the HDC1000, in measurement mode the RF micro is in normal operation and transmission. The different modes offer the possibility to select the appropriate time interval which respect the application constraint and maximize the life of the battery.

8.2.3 Application Curve

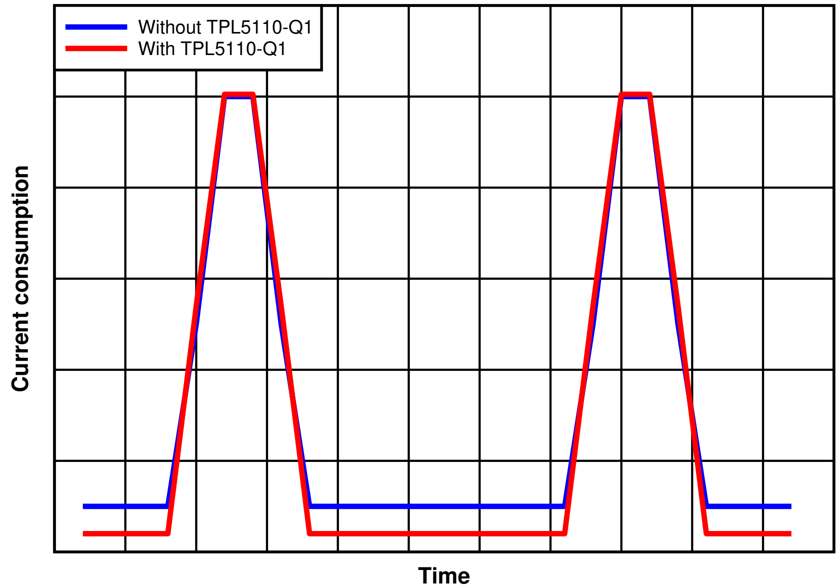


图 8-2. Effect of TPL5110-Q1 on Current Consumption

9 Power Supply Recommendations

The TPL5110-Q1 requires a voltage supply within 1.8 V and 5.5 V. A multilayer ceramic bypass X7R capacitor of 0.1 µF between VDD and GND pin is recommended.

10 Layout

10.1 Layout Guidelines

The DELAY/M_DRV pin is sensitive to parasitic capacitance. It is suggested that the traces connecting the resistance on this pin to GROUND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the DRV pin is also improved by keeping the trace length between the TPL5110-Q1 and the gate of the MOSFET short to reduce the parasitic capacitance. The EN/ONE_SHOT needs to be tied to GND or VDD with short traces.

10.2 Layout Example

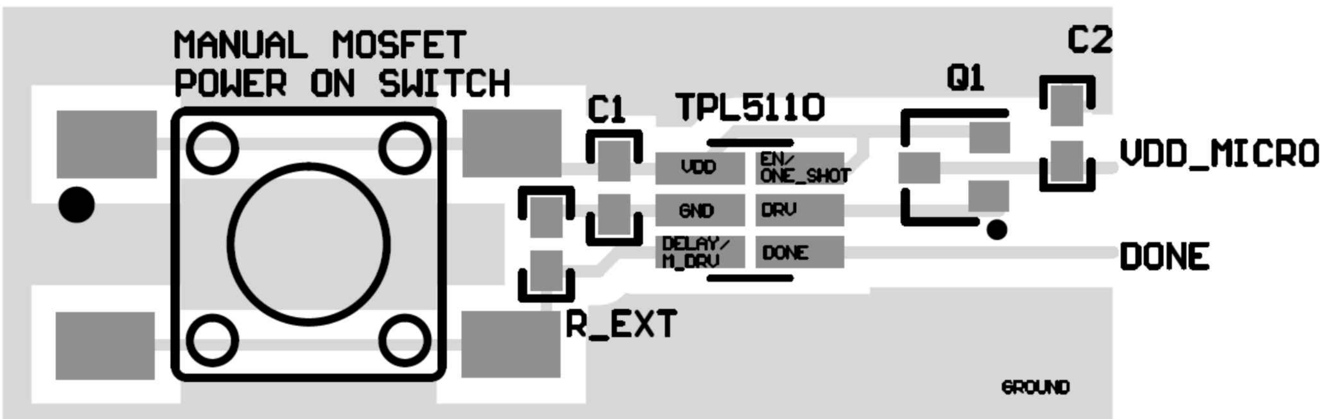


图 10-1. Layout

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPL5110QDDCRQ1	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	13ZX
TPL5110QDDCRQ1.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	13ZX
TPL5110QDDCTQ1	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	13ZX
TPL5110QDDCTQ1.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	13ZX

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPL5110-Q1 :

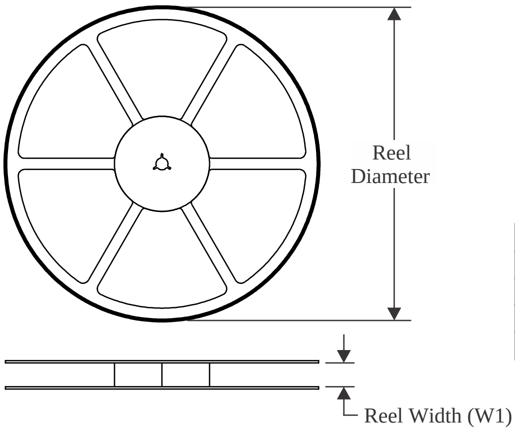
- Catalog : TPL5110

NOTE: Qualified Version Definitions:

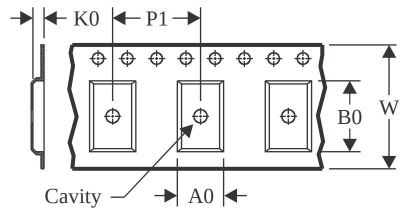
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

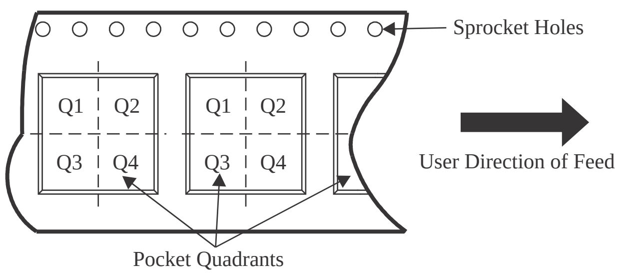


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

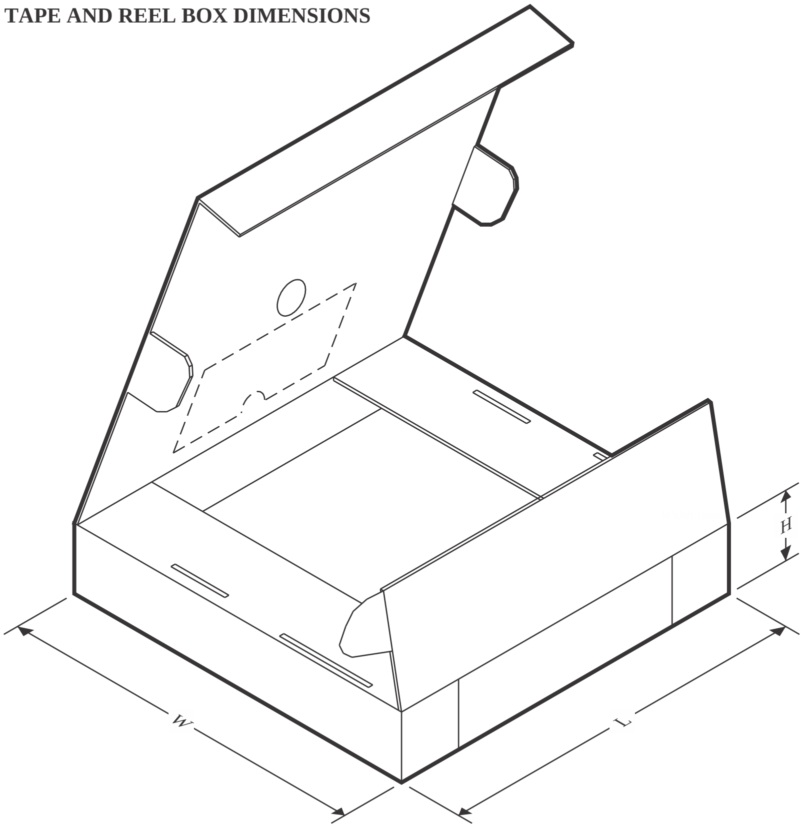
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

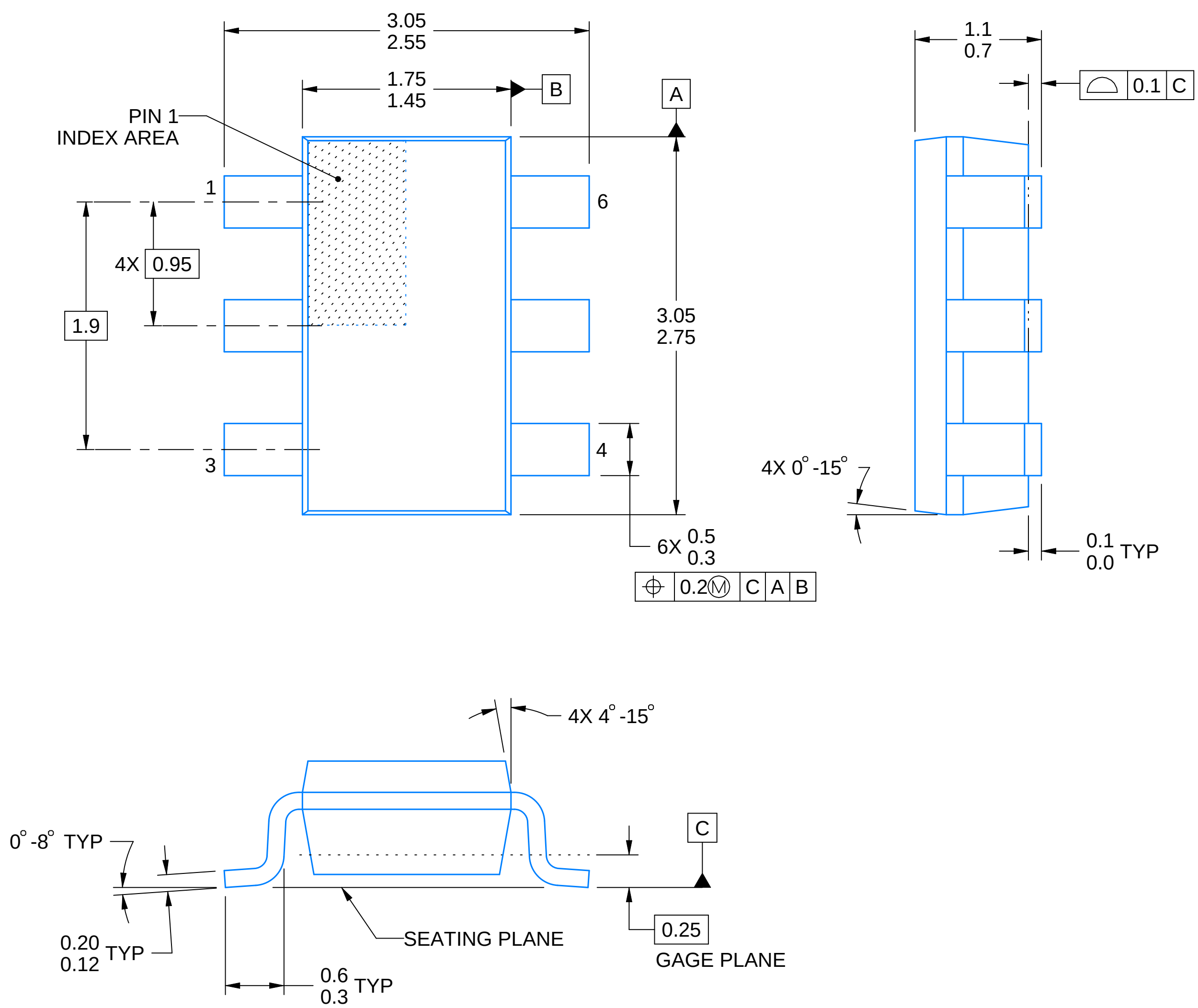
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL5110QDDCRQ1	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPL5110QDDCTQ1	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL5110QDDCRQ1	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
TPL5110QDDCTQ1	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0



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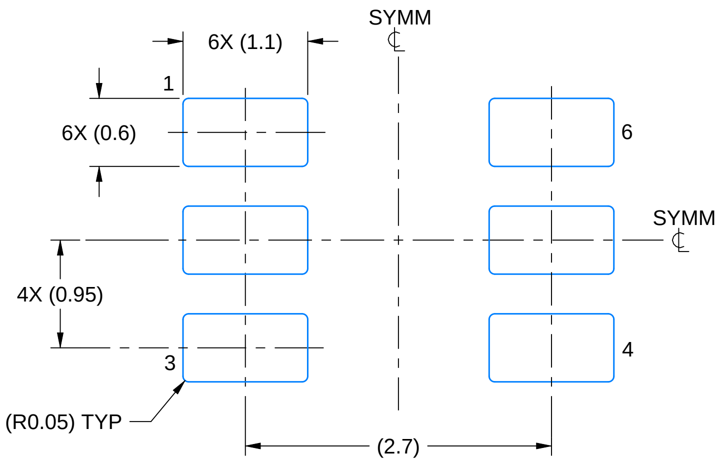
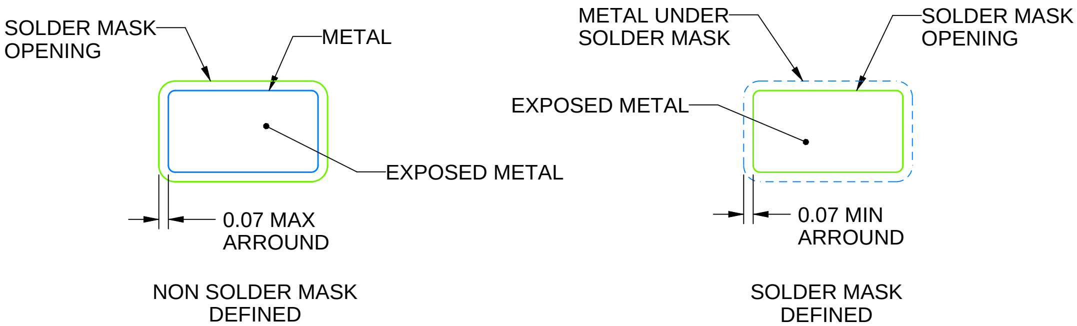
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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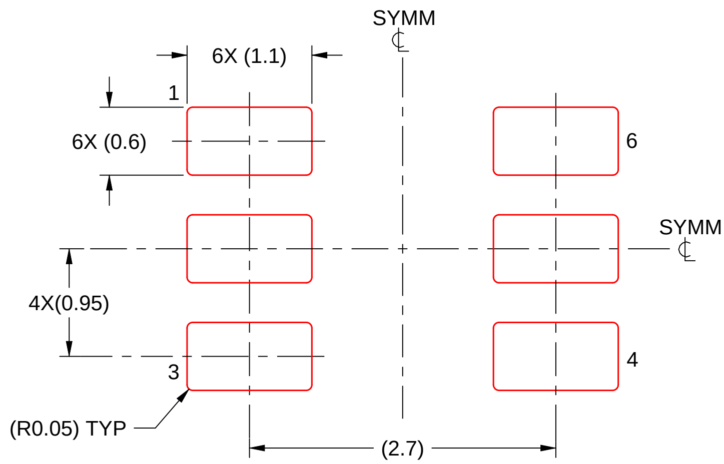
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.