TPIC6596 电源逻辑 8 位移位寄存器

1 特性

- 低 $r_{DS(on)}$：1.3Ω（典型值）
- 雪崩能量：75mJ
- 250mA 连续电流的八个功率 DMOS 晶体管输出
- 每个输出 1.5A 脉冲电流
- 45V 时的输出钳位电压
- 增强了多级级联，只需一次输入即可清零所有寄存器
- 低功耗

2 应用

- 仪表组
- 信号灯
- LED 照明和控制
- 汽车继电器或螺线管驱动器

3 说明

TPIC6596 是一款单片、高压、高电流功率 8 位移位寄存器，专为负载功率要求相对较高的系统而设计。该器件包含内置的输出钳位电压，用于提供电感瞬态保护。电源驱动器应用包括继电器、螺线管和其他中等电流或高电压负载。

该器件包含一个可对 8 位 D 类存储寄存器进行馈送的 8 位串行输入、并行输出移位寄存器。移位和存储寄存器之间的数据传输分别在移位寄存器时钟 (SRCK) 和寄存器时钟 (RCK) 的上升沿上发生。当移位寄存器清零 ($\overline{SRCLR}$) 为高电平时，存储寄存器将数据传输到输出缓冲器。只有当 RCK 为低电平时，写入数据和读取数据才有效。当 $\overline{SRCLR}$ 为低电平时，器件中的所有寄存器都将清零。当输出使能 ($\overline{G}$) 保持高电平时，输出缓冲器中的所有数据将保持低电平，并且所有漏极输出将关闭。当 $\overline{G}$ 保持低电平时，来自存储寄存器中的数据对输出缓冲器透明。串行输出 (SER OUT) 在 SRCK 下降沿时从器件时钟输出，为级联应用提供额外的保持时间。这可为时钟信号有可能偏移、器件相距较远或系统必须容许电磁干扰的应用提供更佳的性能。

输出为低侧、漏极开路 DMOS 晶体管，额定输出功率为 45V，连续灌电流能力为 250mA。当输出缓冲器中的数据较低时，DMOS 晶体管的输出被关闭。当数据较高时，DMOS 晶体管输出具有灌电流能力。

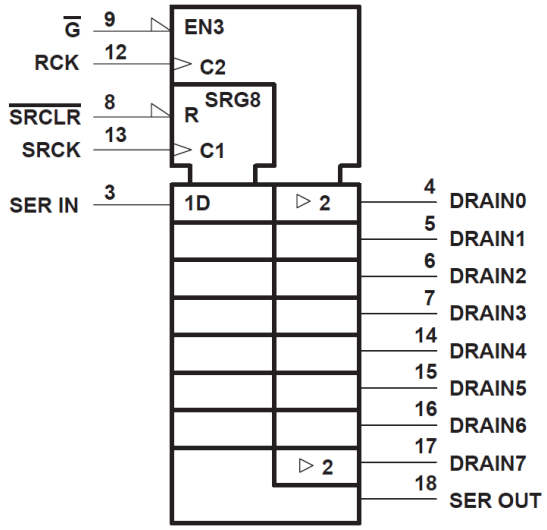
提供单独的电源和逻辑电平接地引脚，有助于尽可能提高系统灵活性。引脚 1、10、11 和 20 在内部连接，每个引脚必须从外部连接到电源系统接地，以尽可能减小寄生电感。引脚 19 逻辑接地 (LGND) 以及引脚 1、10、11 和 20 电源接地 (PGND) 之间的单点连接必须在外部进行，以减少逻辑和负载电路之间的串扰。TPIC6596 具有 -40°C 至 125°C 的额定管壳工作温度范围。

器件信息

器件型号(1)	封装	本体尺寸（标称值）
TPIC6596	SOIC (20)	12.80mm × 7.50mm
	PDIP (20)	25.40mm × 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

典型应用

Table of Contents

4 Pin Configuration and Functions

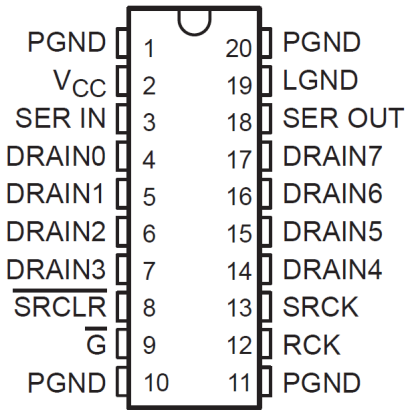


图 4-1. DW or N Package, 20-pin SOIC (Top- View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
DRAIN0	4	O	Open-drain output
DRAIN1	5		
DRAIN2	6		
DRAIN3	7		
DRAIN4	14		
DRAIN5	15		
DRAIN6	16		
DRAIN7	17		
$\overline{G}$	9	I	Output enable, active-low
LGND	19	-	Logic ground
PGND	1, 10, 11, 20	-	Power ground
RCK	12	I	Register clock
SER IN	3	I	Serial data input
SER OUT	18	O	Serial data output
SRCK	13	I	Shift register clock
$\overline{SRCLR}$	8	I	Shift register clear, active-low
V_{CC}	2	I	Power supply

(1) P: Power Pin; I: Input Pin; I/O: Input/Output Pin; O: Output Pin.

5 Specifications

over operating free-air temperature range (unless otherwise noted)(1) (2)

5.1 Absolute Maximum Ratings

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage		7	V
V_I	Logic input voltage range	-0.3	7	V
V_{DS}	Power DMOS drain-to-source voltage		45	V
	Continuous source-drain diode anode current		1	A
	Pulsed source-drain diode anode current		2	A
	Pulsed drain current, each output, all outputs on, see also (3)		750	mA
I_{Dn}	Continuous drain current, each output, all outputs on, T_A = 25°		250	mA
$I_{DM,}$	Peak drain current single output, T_A = 25°C (See (3))		2	A
E_{AS}	Single-pulse avalanche energy (See (4))		75	mJ
I_{AS}	Avalanche current (See (4))		1	A
	Continuous total power dissipation	see 节 5.2		(5)
T_J	Operating virtual junction temperature range	-40	150	°C
T_{stg}	Storage temperature	−65	150	°C
	Lead temperature 1, 6mm (1/16 inch) from case for 10 seconds		260	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal GND.
(3) Pulse duration ⩽ 100µs, duty cycle ⩽ 2 %
(4) DRAIN supply voltage = 15V, starting junction temperature (TJS) = 25°C, L = 100mH, IAS = 1A (see 图 5-1).
(5) See Dissipation Table

5.2 Dissipation Rating Table

PACKAGE	T_C ⩽ 25°C POWER RATING	DERATING FACTOR ABOVE T_C = 25°C	T_C = 125°C POWER RATING
DW	1125mW	9.0mW/°C	225mW
N	1150mW	9.2mW/°C	230mW

over operating free-air temperature range (unless otherwise noted)

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Logic supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	0.85V_{CC}		V
V_{IL}	Low-level input voltage		0.15V_{CC}	V
	Pulsed drain output current, T_C = 25°C, V_{CC} = 5V See ((1), (2))	-1.8	1.5	A
t_{su}	Setup time, SER IN high before SRCK ↑ , see 图 6-2	10		ns
t_h	Hold time, SER IN high after SRCK ↑ , see 图 6-2	10		ns
t_w	Pulse duration, see 图 6-2	20		ns
T_C	Operating case temperature	-40	125	°C

(1) Pulse duration ⩽ 100µs, duty cycle ⩽ 2%.

(2) Technique must limit $T_J - T_C$ to 10°C maximum.

over operating free-air temperature range (V_{CC} = 5V, T_C = 25°C, unless otherwise noted)

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(BR)DSX}$	Drain-source breakdown voltage	I_D = 1mA		45			V
V_{SD}	Source-drain diode forward voltage	I_F = 250mA, see (1)			0.85	1	V
V_{OH}	High-level output voltage,High-level output voltage, SER OUT	I_{OH} = −20mA, V_{CC} = 4.5V		4.4	4.49		V
		I_{OH} = −4mA, V_{CC} = 4.5V		4.1	4.3		
V_{OL}	Low-level output voltage, SER OUT	I_{OH} = 20mA, V_{CC} = 4.5V			0.002	0.1	V
		I_{OH} = 4mA, V_{CC} = 4.5V			0.2	0.4	
$V_{(hys)}$	Input hysteresis	V_{DS} = 15V			1.3		V
I_{IH}	High-level input current	V_{CC} = 5.5V, V_I = V_{CC}				1	µA
I_{IL}	Low-level input current	V_{CC} = 5.5V, V_I = 0				-1	µA
I_{CCL}	Logic supply current	IO = 0, All inputs low			15	100	µA
$I_{CC(FRQ)}$	Logic supply current frequency	f_{SRCK} = 5MHz, IO = 0, CL = 30pF	See 图 6-1, 图 6-2, and 图 5-2		0.6	5	mA
I_N	Nominal current	$V_{DS(on)}$ = 0.5V, I_N = I_D, T_C = 85°C.	See (2), (3), and (4)		250		mA
I_{DSX}	Off-state drain current	V_{DS} = 40V			0.05	1	µA
		V_{DS} = 40V; T_C = 125°C			0.15	5	
$r_{DS(on)}$	Static drain-source on-state resistance	I_D = 250mA, V_{CC} = 4.5V	See (2), (3), 图 5-5 and 图 5-6		1.3	2	Ω
		I_D = 250mA, V_{CC} = 4.5V, T_C = 125°C.			2	3.2	
		I_D = 500mA, V_{CC} = 4.5V			1.3	2	

(1) Pulse duration ⩽ 100µs, duty cycle ⩽ 2%.
(2) Technique must limit $T_J - T_C$ to 10°C maximum.
(3) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.
(4) Nominal current is defined for a consistent comparison between devices from different sources. The current produces a voltage drop of 0.5V at T_C = 85°C.

over operating free-air temperature range (unless otherwise noted)

5.5 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from $\overline{G}$	C_{LL} = 30pF = 30pF, I_{DD} = 250mA, See 图 6-1, 图 6-2, and 图 5-7		650		ns
t_{PHL}	Propagation delay time, high-to-low-level output from $\overline{G}$			200		ns
t_r	Rise time, drain output			230		ns
t_f	Fall time, drain output			170		ns
t_{PD}	Propagation delay time, SRCK ↓ to SER OUT	C_L= 30pF, I_D= 250mA, See (3)		50		ns
f_{SRCK}	Serial clock frequency	C_L= 30pF, I_D= 250mA, See 图 6-2			5	MHz
t_a	Reverse-recovery-current rise time	I_{FF} = 250mA, di/dt = 20A/µs. See (1), (2), and 图 6-3		100		ns
t_{rr}	Reverse-recovery time			300		

(1) Technique must limit $T_J - T_C$ to 10°C maximum.
(2) These parameters are measured with voltage-sensing contacts separate from the current-carrying contacts.

(3) This is the maximum serial clock frequency assuming cascaded operation where serial data is passed from one stage to a second stage. The clock period allows SRCK → SER OUT propagation delay and setup time plus some timing margin

5.6 Thermal Resistance Characteristics

PARAMETER			TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Thermal resistance, junction-to-ambient	DW	All eight outputs with equal power		111	℃/W
		N			108	

5.7 Typical Characteristics

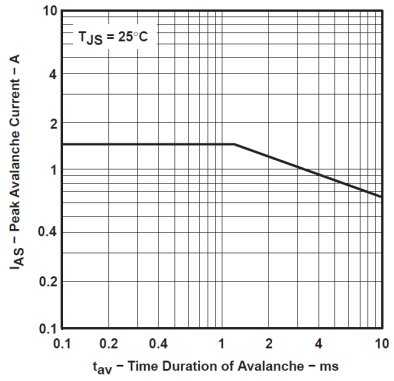


图 5-1. Peak Avalanche Current vs. Time Duration of Avalanche

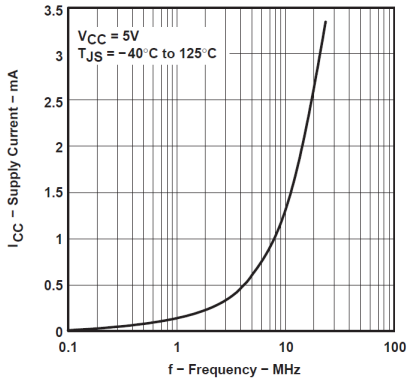


图 5-2. Supply Current vs. Frequency

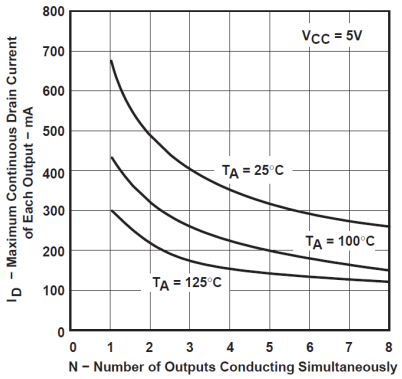


图 5-3. Maximum Continuous Drain Current of Each Output vs. Number Of Outputs Conducting Simultaneously

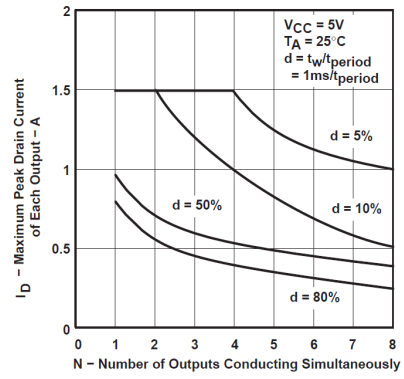


图 5-4. Maximum Peak Drain Current of Each Output vs. Number of Outputs Conducting Simultaneously

5.7 Typical Characteristics (continued)

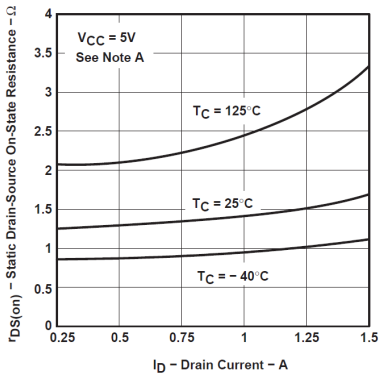


图 5-5. Static Drain-source On-state Resistance vs. Drain Current

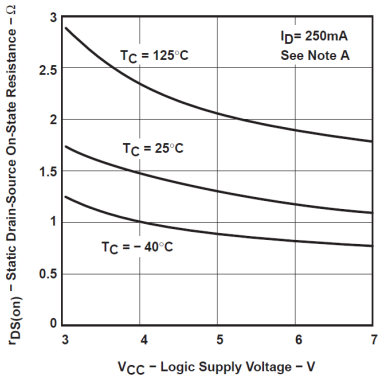


图 5-6. Static Drain-source On-state Resistance vs. Logic Supply Voltage

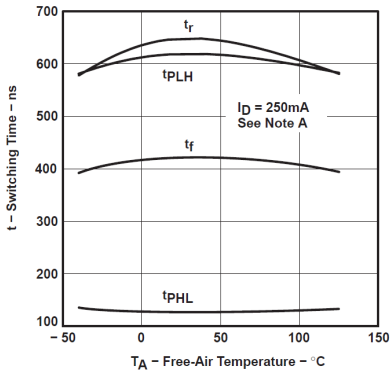
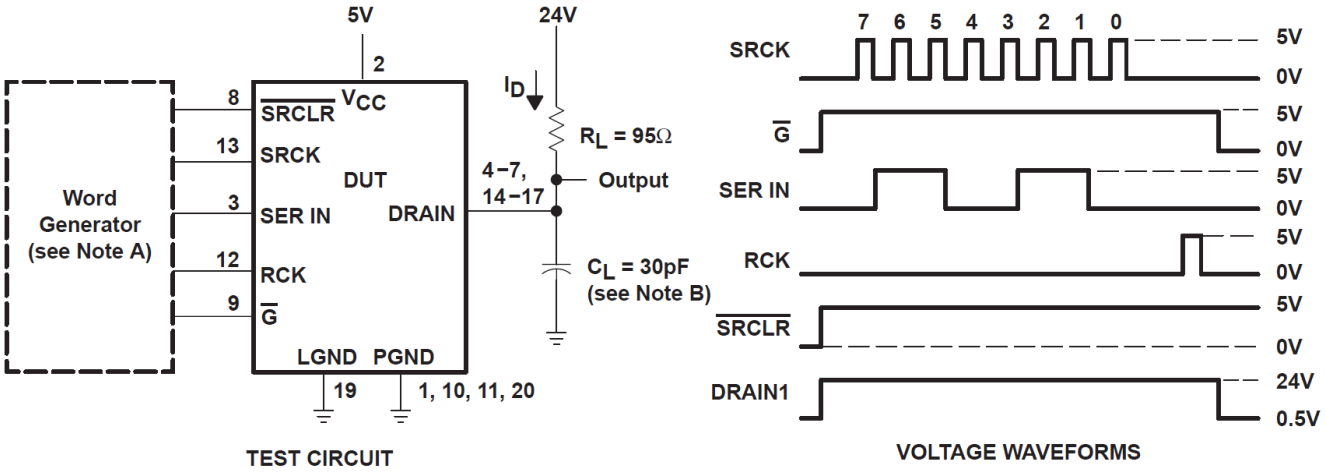


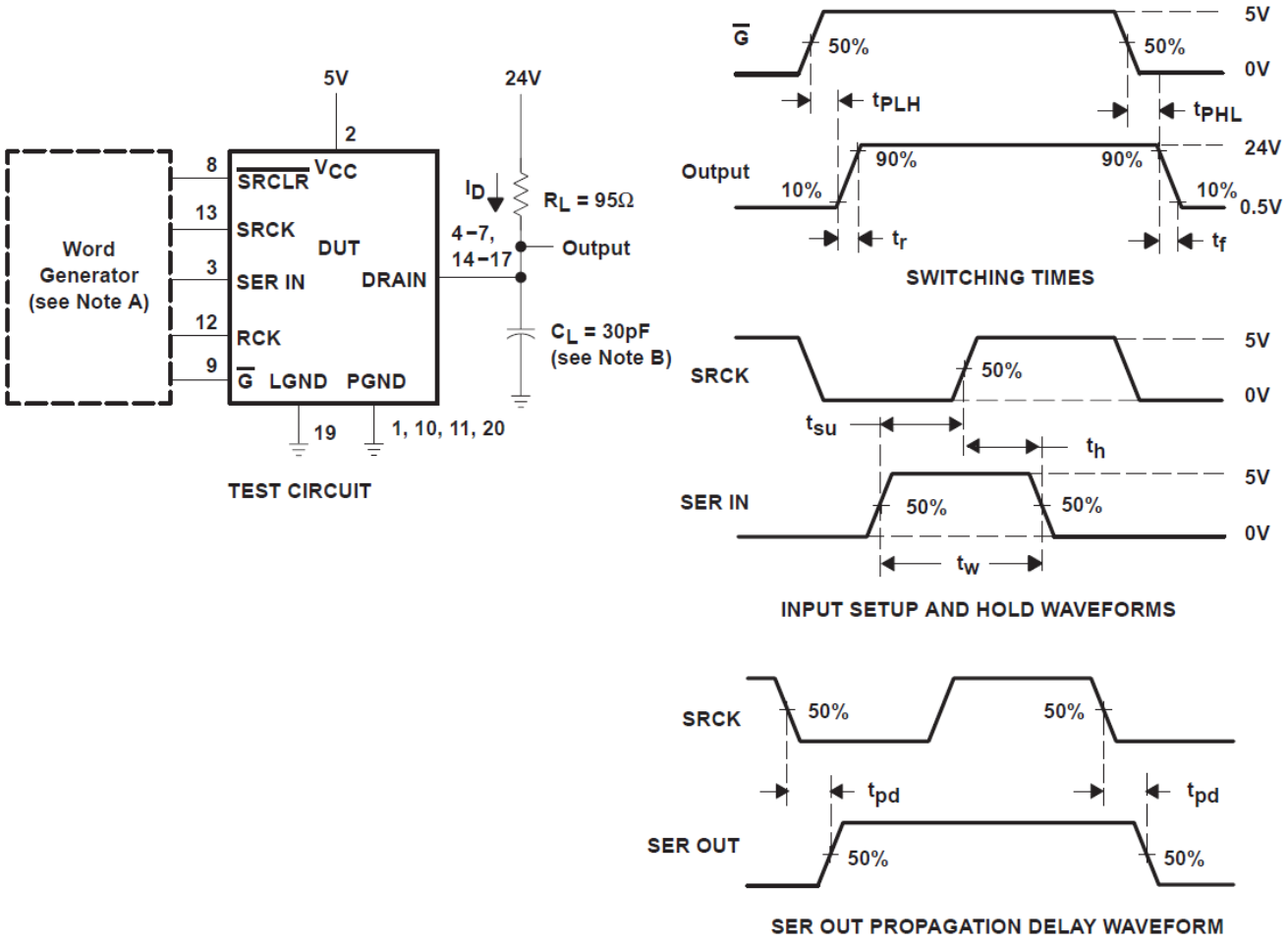
图 5-7. Switching Time vs. Free-air Temperature

6 Parameter Measurement Information



A. Write data and read data are valid only when RCK is low

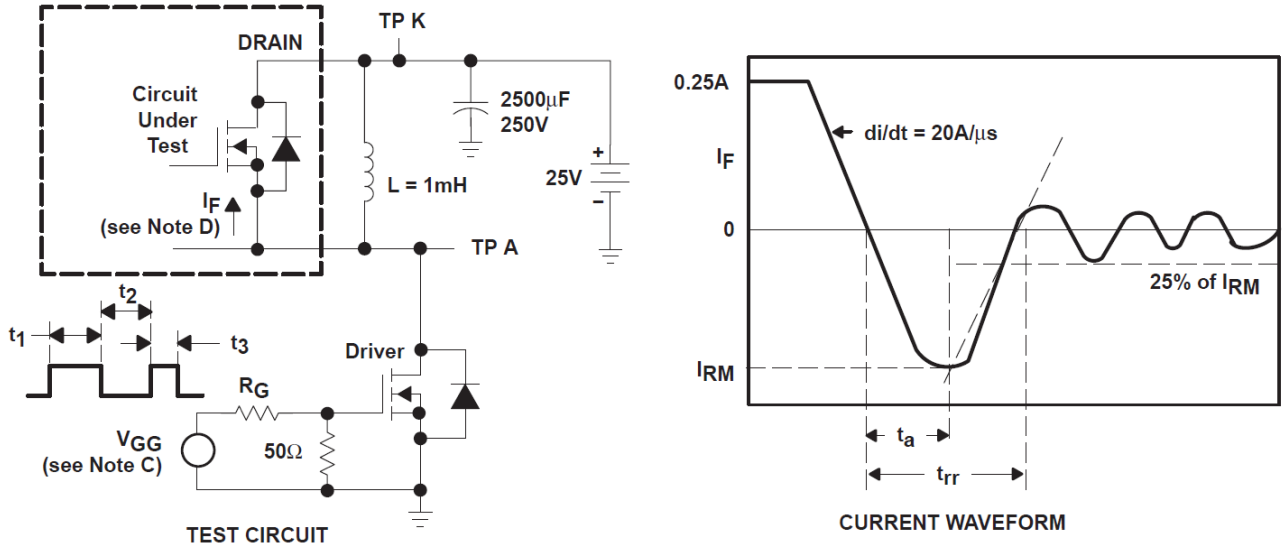
图 6-1. Resistive Load Operation



A. C_L includes probe and jig capacitance.

B. Outputs DRAIN 1, 2, 5, and 6 low (PGND), all other DRAIN outputs are at 24V. The word generator has the following characteristics: t_r ⩽ 10ns, t_f ⩽ 10ns, t_w = 300ns, pulsed repetition rate (PRR) = 5kHz, ZO = 50Ω.

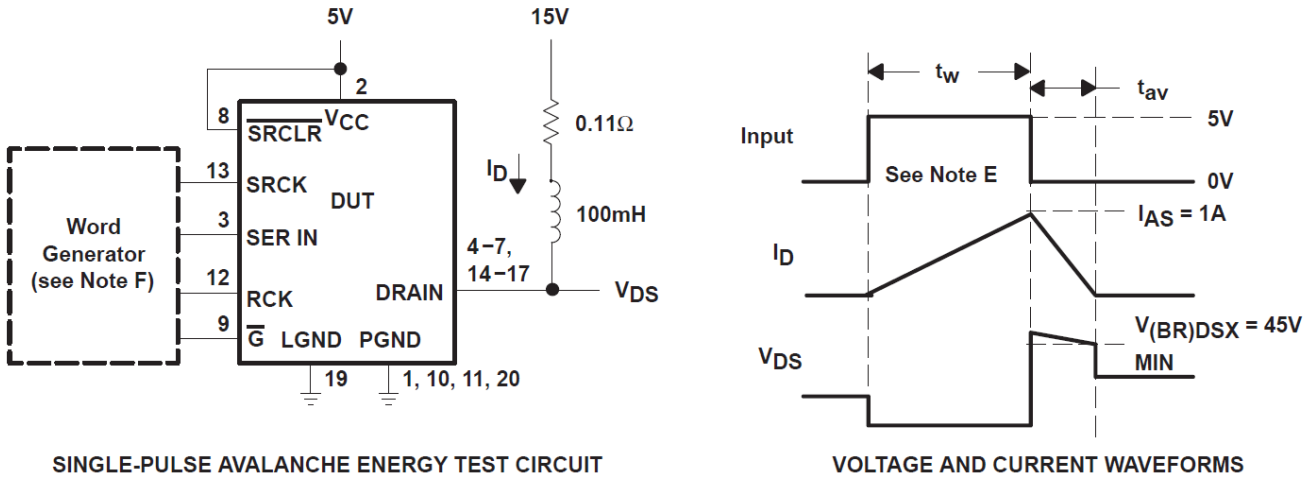
图 6-2. Test Circuit, Switching Times, and Voltage Waveforms



A. The V_{GG} amplitude and R_G are adjusted for di/dt = 20A/µs. A V_{GG} double-pulse train is used to set I_F = 0.25A, where t_1 = 10µs, t_2 = 7µs, and t_3 = 3µs.

B. The DRAIN terminal under test is connected to the TP K test point. All other terminals are connected together and connected to the TP A test point.

图 6-3. Reverse-Recovery-Current Test Circuit and Waveforms of Source-Drain Diode



A. The word generator has the following characteristics: t_r ⩽ 10ns, t_f ⩽ 10ns, Z_O = 50Ω.

B. Input pulse duration, t_w, is increased until peak current I_{AS} = 1A. Energy test level is defined as $E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{av}/2$ = 75mJ, where t_{av} = avalanche time.

图 6-4. Single-Pulse Avalanche Energy Test Circuit and Waveforms

7 Detailed Description

7.1 Overview

The TPIC6596 is a monolithic, high-voltage, highcurrent power 8-bit shift register designed for use in systems that require relatively high load power. The device contains a built-in voltage clamp on the outputs for inductive transient protection. Power driver applications include relays, solenoids, and other medium-current or high-voltage loads.

7.2 Functional Block Diagram

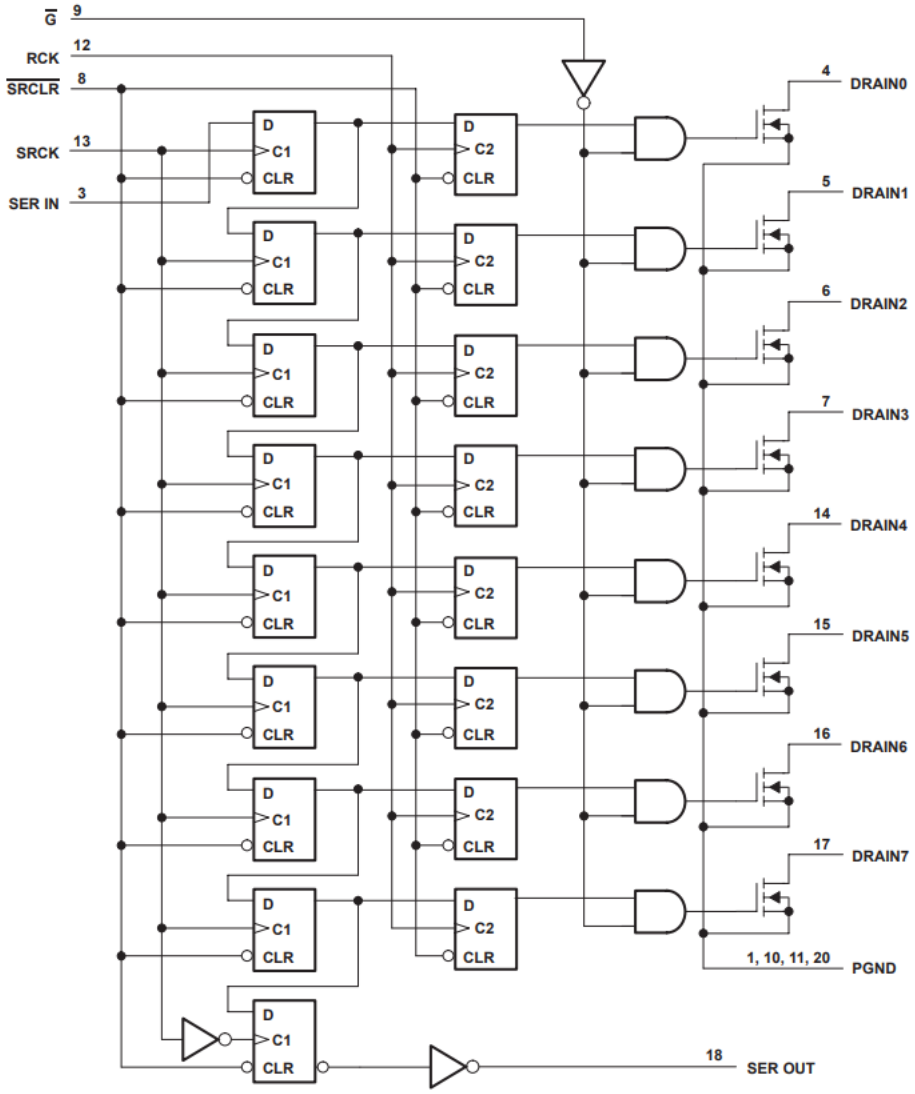
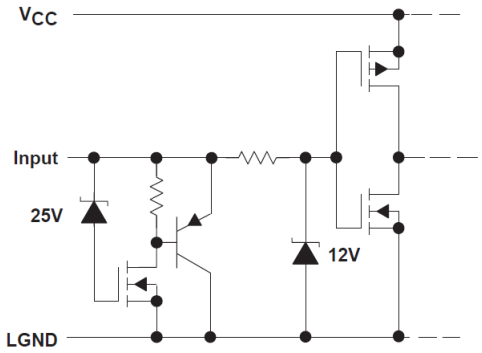
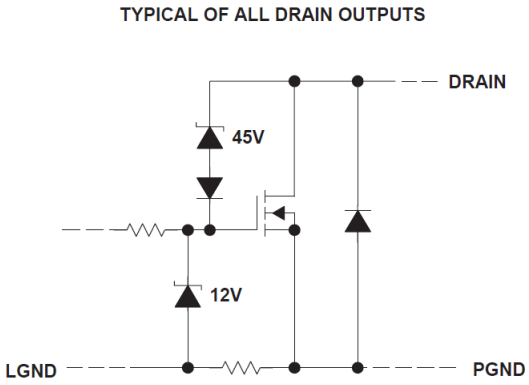


图 7-1. Functional Block Diagram



Equivalent of Each Input Schematic



Typical of All Drain Outputs Schematic

7.3 Feature Description

7.3.1 Serial-In Interface

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Data transfers through both the shift and storage registers on the rising edge of the shift-register clock (SRCK) and the register clock (RCK) respectively. Write data and read data are valid only when RCK is low. The storage register transfers data to the output buffer when shift register clear ($\overline{\text{SRCLR}}$) is high.

7.3.2 Clear Register

A logical low on ($\overline{\text{SRCLR}}$) clears all registers in the device. TI suggests clearing the device during power up or initialization.

7.3.3 Output Control

When output enable (G) is held high, all data in the output buffers is held low and all drain outputs are off. Holding ($\overline{\text{G}}$) low makes data from the storage register transparent to the output buffers. When data in the output buffers is low, the DMOS transistor outputs are OFF. When data is high, the DMOS transistor outputs have sink-current capability. This pin can also be used for global PWM dimming.

7.3.4 Cascaded Application

The serial output (SER OUT) is clocked out of the device on the falling edge of SRCK to provide additional hold time for cascaded applications. This will provide improved performance for applications where clock signals may be skewed, devices are not located near one another, or the system must tolerate electromagnetic interference. Connect the device (SER OUT) pin to the next device (SER IN) for daisy Chain.

7.3.5 Current Limit Function

Outputs are low-side, open-drain DMOS transistors with output ratings of 45V and 250mA continuous sink current capability

7.4 Device Functional Modes

7.4.1 Operating with V_{cc} < 4.5V

This device works normally during 4.5V ⩽ V_{cc} ⩽ 5.5V, when operation voltage is lower than 4.5V, correct behavior of the device, including communication interface and current capability, is not assured.

7.4.2 Operating with 5.5V < V_{cc} ⩽ 7V

The device works normally in this voltage range, but reliability issues can occur if the device works for a long time in this voltage range.

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (April 2000) to Revision B (March 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Changed $\overline{\text{SRCLR}}$ timing diagram	8

Changes from Revision * (May 2005) to Revision A (April 2000)	Page
• 更改了 $\overline{\text{SRCLR}}$ 时序图	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPIC6596DWG4	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-	TPIC6596
TPIC6596DWRG4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-	TPIC6596
TPIC6596DWRG4.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TPIC6596
TPIC6596N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPIC6596N
TPIC6596N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TPIC6596N

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

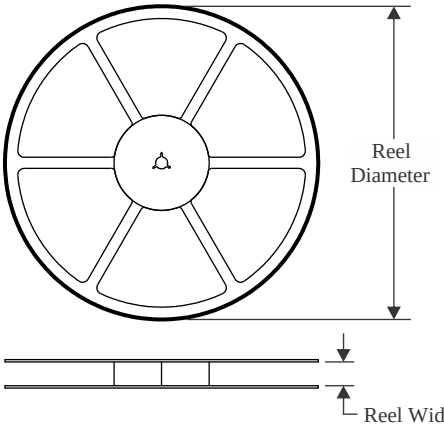
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

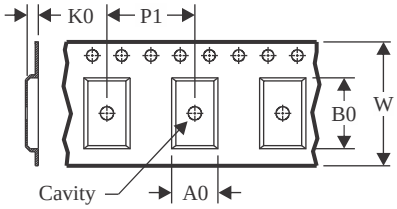
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

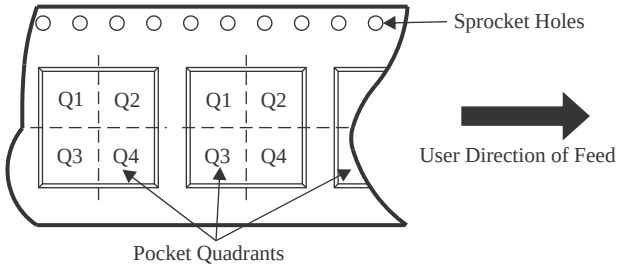


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

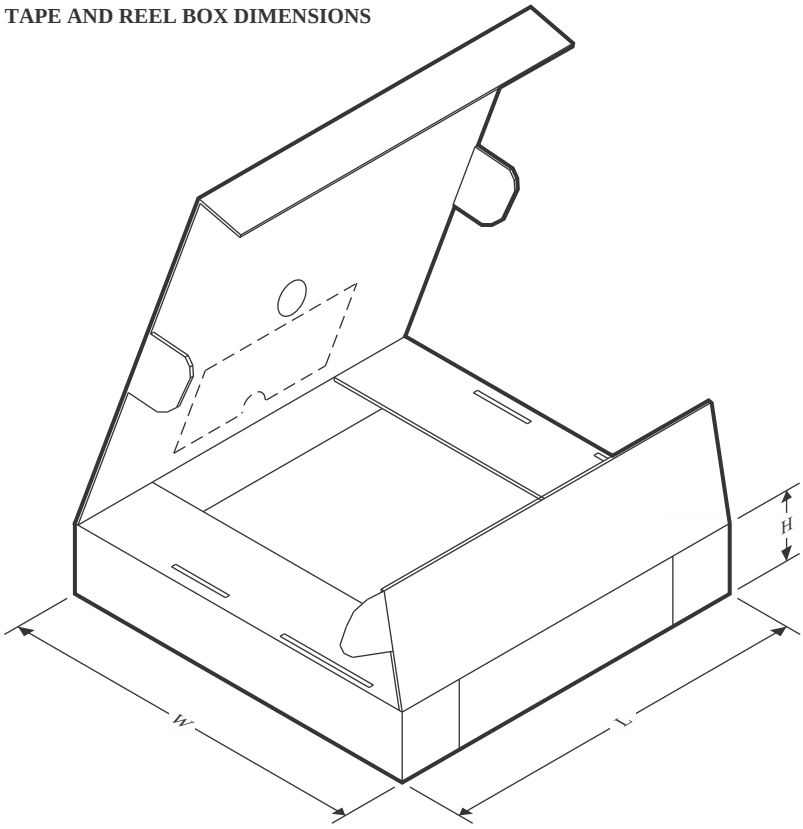
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPIC6596DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
TPIC6596DWRG4	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

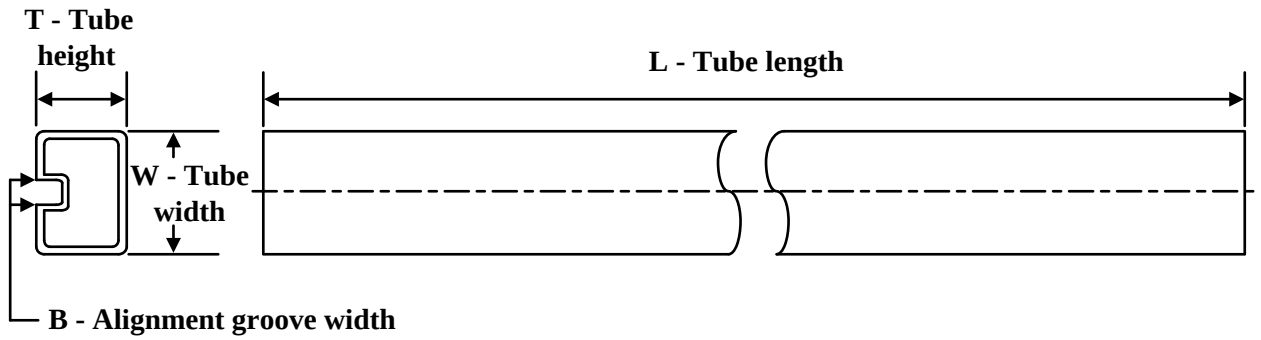
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPIC6596DWRG4	SOIC	DW	20	2000	350.0	350.0	43.0
TPIC6596DWRG4	SOIC	DW	20	2000	350.0	350.0	43.0

TUBE



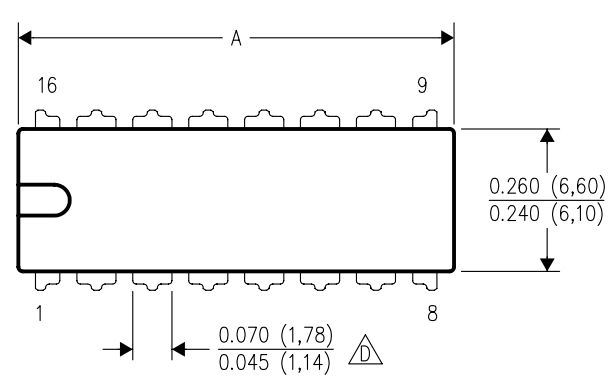
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPIC6596N	N	PDIP	20	20	506	13.97	11230	4.32
TPIC6596N.A	N	PDIP	20	20	506	13.97	11230	4.32

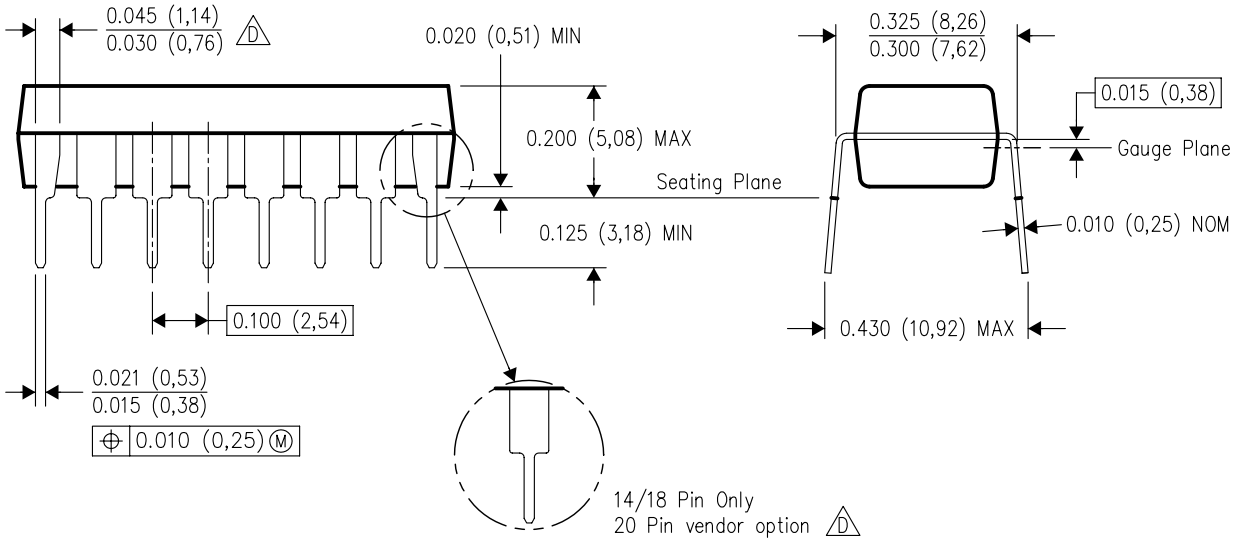
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

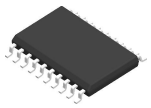


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

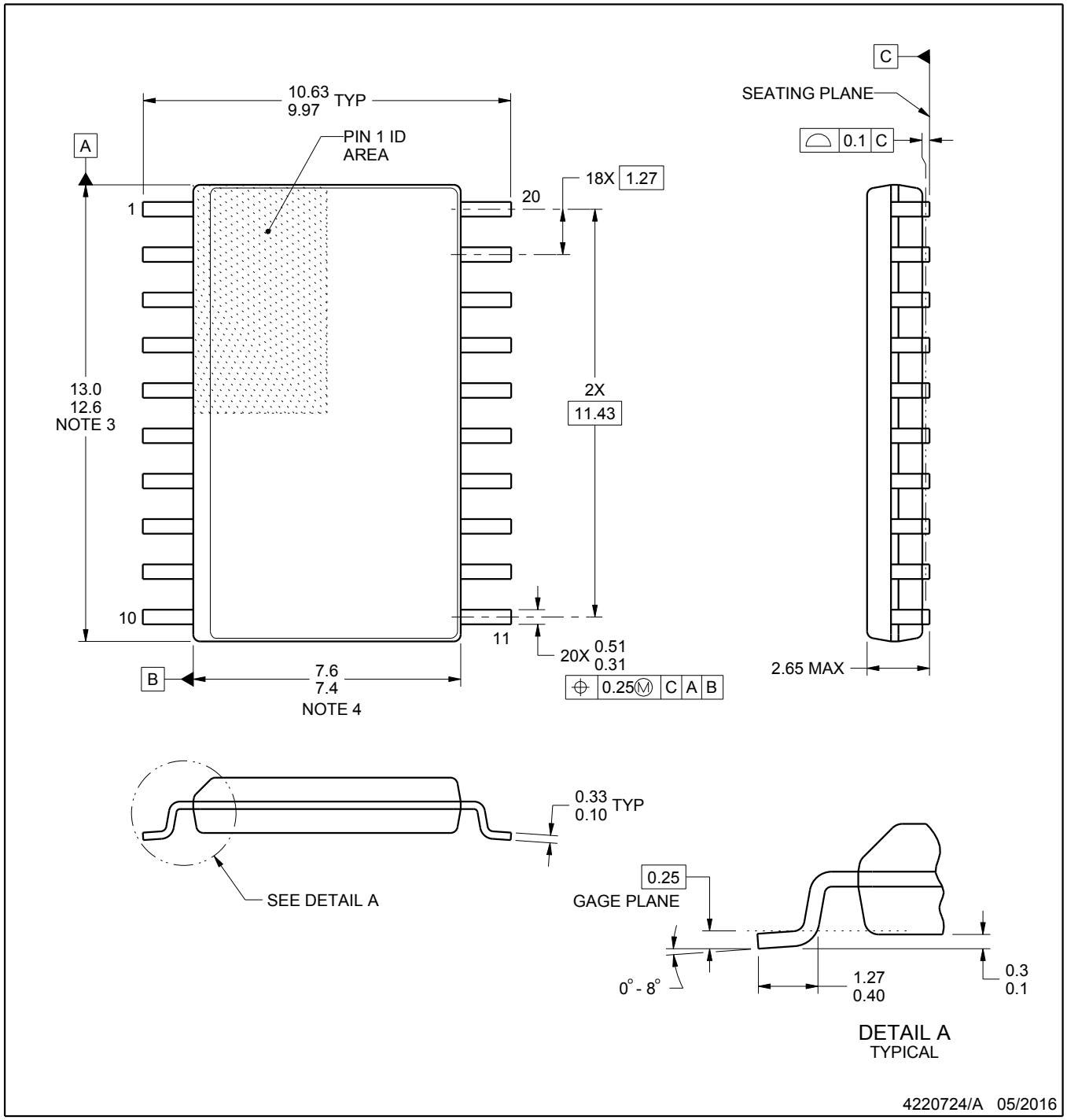


PACKAGE OUTLINE

DW0020A

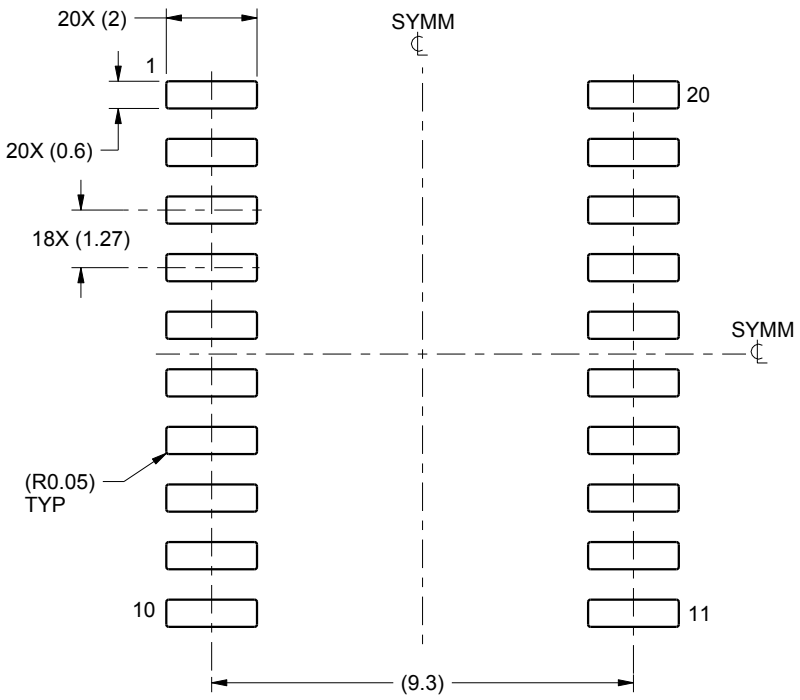
SOIC - 2.65 mm max height

SOIC

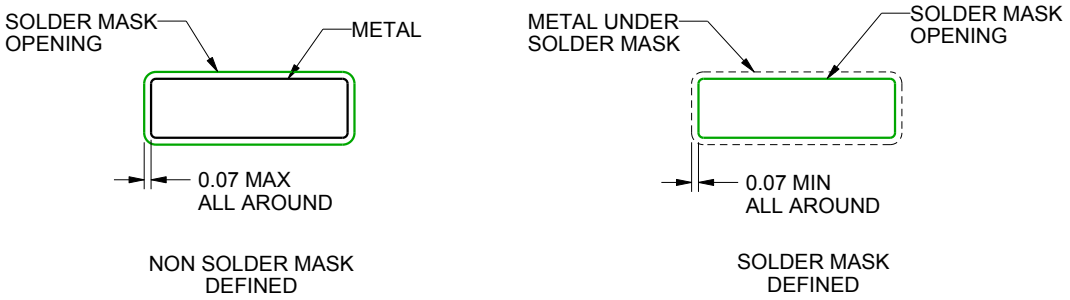


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

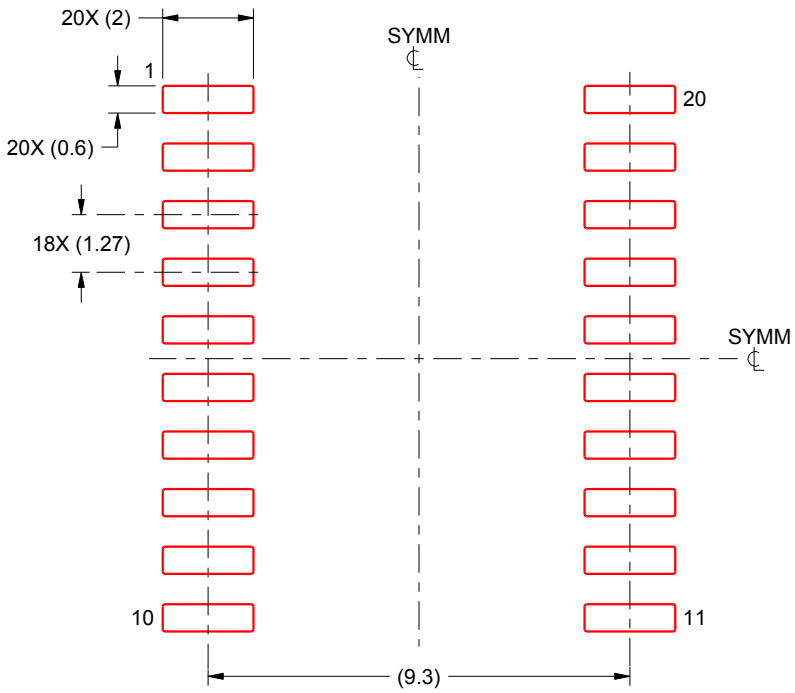


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月