用于 LCD 显示屏的具有 ESD 保护的 TPDxF202 4 通道或 6 通道 EMI 滤波器

1 特性

- 适用于数据线路的四通道或六通道 EMI 滤波和 ESD 保护
- 出色的滤波性能
  - 1GHz 至 3GHz 时衰减大于 40dB
  - 108MHz 时带宽为 -3dB
  - 100MHz 频率下的串扰衰减为 70dB
- 超过 IEC 61000-4-2（4 级）ESD 保护要求
  - ±25kV IEC 61000-4-2 接触放电
  - ±25kV IEC 61000-4-2 空气间隙放电
  - ±15kV 人体放电模型 (HBM)
- Pi 型 C-R-C 滤波器配置提供对称滤波心梗（R = 100 Ω，C_{TOTAL} = 30pF）
- 10nA 低泄漏电流
- 节省空间的 DSBGA 封装和直通式引脚映射可在便携式应用中提供出色的性能

2 应用

- 终端设备：
  - LCD 显示屏
  - 存储器接口
  - 键盘
  - 便携式设备
- 接口：
  - DVI
  - VGA、SVGA
  - SIM 卡
  - 数据线路

3 说明

TPDxF202 器件是四通道或六通道 EMI 滤波器，专为抑制手机及其他便携式应用中的 EMI 噪声而设计。这些滤波器还配有瞬态电压抑制 (TVS) 二极管电路以提供静电放电 (ESD) 保护，从而保证应用在承受远远超过 IEC 61000-4-2（4 级）ESD 应力的情况下完好无损。该 π 型 C-R-C 滤波器可在其两侧的输入和输出数据线路上提供对称的滤波性能。

由于 DSBGA 封装的寄生效应小，TPDxF202 滤波器能够在典型的手机载波频率范围内提供出色的信号衰减性能（1GHz 时为 –40dB）。

TPDxF202 器件采用节省空间的超薄型（板载安装时封装高度为 0.3mm）YFU 封装，因此能够安装在高度为关键约束因素的印刷电路板上。

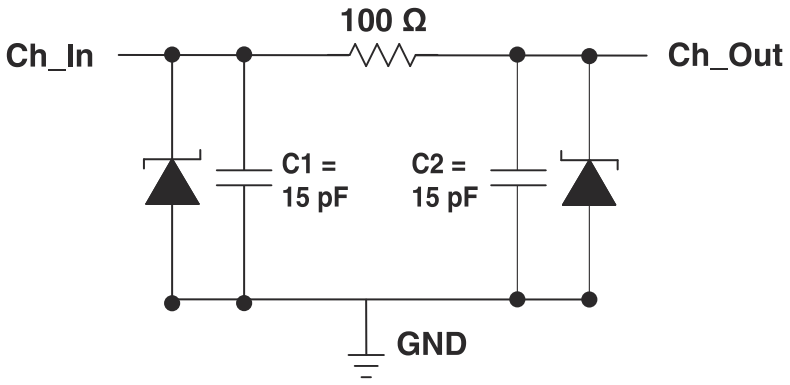
TPDxF202 器件的额定工作温度范围为 –40°C 至 85°C。

TPDxF202 器件的典型应用为具有 DVI、VGA、SVGA、SIM 卡及其他数据接口的便携式设备。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPD4F202	DSBGA (10)	1.06mm × 1.57mm
TPD6F202	DSBGA (15)	1.06mm × 2.36mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



功能方框图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (November 2015) to Revision B (May 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 将*器件信息*表中 DSBGA (15) 封装的尺寸从 *1.06mm × 2.63mm* 更改为 *1.06mm × 2.36mm*	1

Changes from Revision * (June 2010) to Revision A (November 2015)	Page
• 添加了*引脚配置和功能*部分、*ESD 等级*表、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分	1
• 删除了*订购信息*部分	1

5 Pin Configuration and Functions

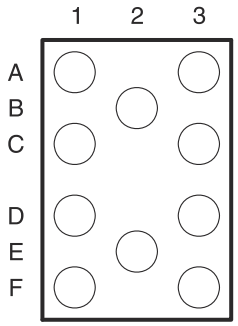


图 5-1. YFU Package 10-Pin DSBGA Top View

表 5-1. Pin Functions — TPD4F202

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	Ch1_In	I/O	ESD-protected channel, route to connector. Corresponds with CH1_Out.
A3	Ch1_Out	I/O	ESD-protected channel, route to system. Corresponds with CH1_In.
B2	GND	G	Ground
C1	Ch2_In	I/O	ESD-protected channel, route to connector. Corresponds with CH2_Out.
C3	Ch2_Out	I/O	ESD-protected channel, route to system. Corresponds with CH2_In.
D1	Ch3_In	I/O	ESD-protected channel, route to connector. Corresponds with CH3_Out.
D3	Ch3_Out	I/O	ESD-protected channel, route to system. Corresponds with CH3_In.
E2	GND	G	Ground
F1	Ch4_In	I/O	ESD-protected channel, route to connector. Corresponds with CH4_Out.
F3	Ch4_Out	I/O	ESD-protected channel, route to system. Corresponds with CH4_In.

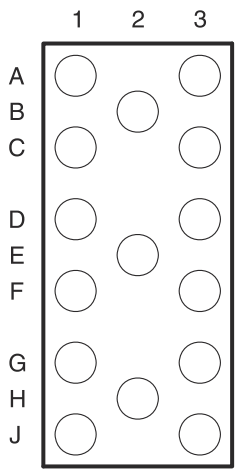


图 5-2. YFU Package 15-Pin DSBGA Top View

表 5-2. Pin Functions — TPD6F202

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	Ch1_In	I/O	ESD-protected channel, route to connector. Corresponds with CH1_Out.
A3	Ch1_Out	I/O	ESD-protected channel, route to system. Corresponds with CH1_In.
B2	GND	G	Ground
C1	Ch2_In	I/O	ESD-protected channel, route to connector. Corresponds with CH2_Out.
C3	Ch2_Out	I/O	ESD-protected channel, route to system. Corresponds with CH2_In.
D1	Ch3_In	I/O	ESD-protected channel, route to connector. Corresponds with CH3_Out.
D3	Ch3_Out	I/O	ESD-protected channel, route to system. Corresponds with CH3_In.
E2	GND	G	Ground
F1	Ch4_In	I/O	ESD-protected channel, route to connector. Corresponds with CH4_Out.
F3	Ch4_Out	I/O	ESD-protected channel, route to system. Corresponds with CH4_In.
G1	Ch5_In	I/O	ESD-protected channel, route to connector. Corresponds with CH5_Out.
G3	Ch5_Out	I/O	ESD-protected channel, route to system. Corresponds with CH5_In.
H2	GND	G	Ground
J1	Ch6_In	I/O	ESD-protected channel, route to connector. Corresponds with CH6_Out.
J3	Ch6_Out	I/O	ESD-protected channel, route to system. Corresponds with CH6_In.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IO}	IO to GND	–0.3	6	V
	Continuous power dissipation (T_A = 70°C)		100	mW
T_J	Junction temperature		150	°C
	Lead temperature (soldering, 10 s)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings — JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±15000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings — IEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±25000	V
		IEC 61000-4-2 air-gap discharge	±25000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	I/O to GND	0	5.5	V
T_A	Ambient temperature	–40	85	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD4F202 YFU (DSBGA) 10 PINS	TPD6F202 YFU (DSBGA) 15 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	91.8	72	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1	0.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.7	14.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	19.7	14.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics

T_A = –40°C to 85°C (Unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{BR}	DC breakdown voltage	I_{IO} = 10 μA	6			V
R	Resistance		85	100	115	Ω
C	Capacitance (C1 or C2)	V_{IO} = 3.3 V, f = 1 MHz		15		pF
I_{IO}	Channel leakage current	V_{IO} = 3.3 V		10		nA
f_C	Cut-off frequency	Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω		108		MHz

(1) Typical values are at T_A = 25°C.

6.7 Typical Characteristics

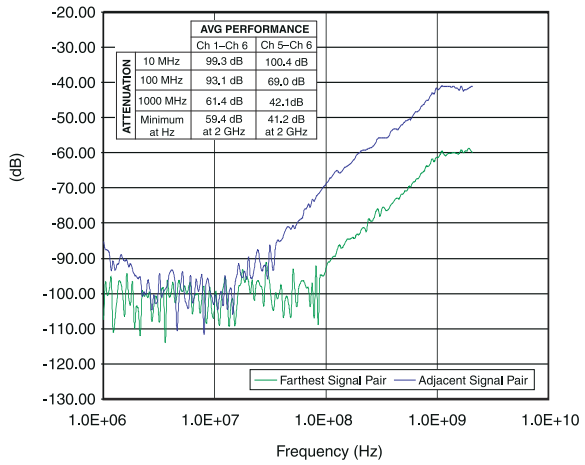


图 6-1. Channel-to-Channel Crosstalk

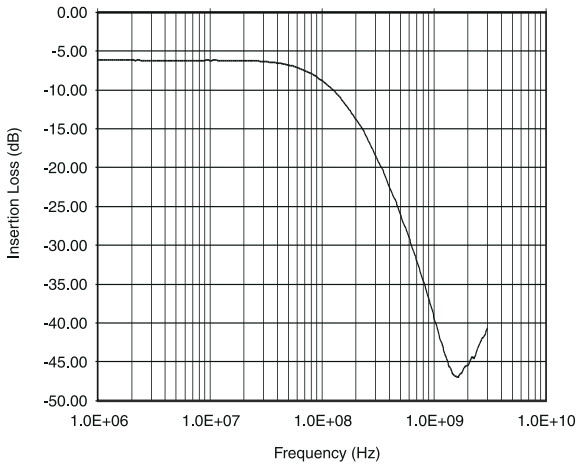


图 6-2. Frequency Response Data (0-V Bias)

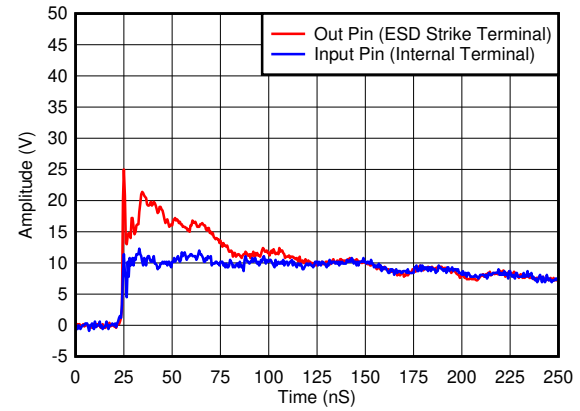


图 6-3. IEC Clamping Waveforms +8-kV Contact

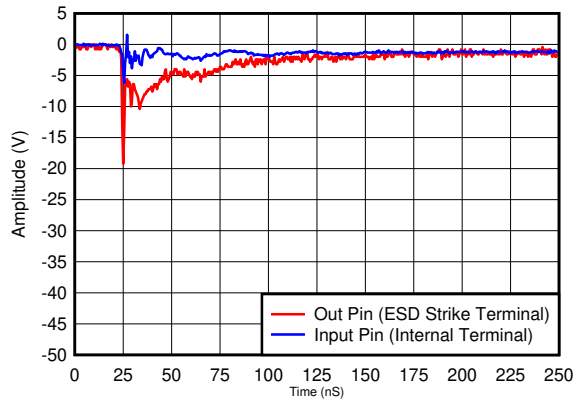


图 6-4. IEC Clamping Waveforms –8-kV Contact

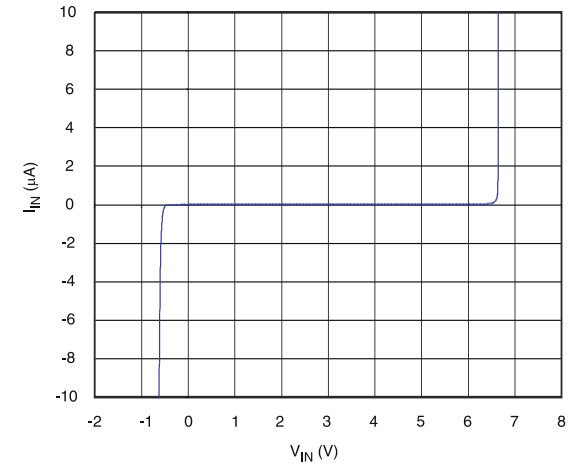


图 6-5. DC Characteristics (I_{IN} vs V_{IN}), T_A = 25°C

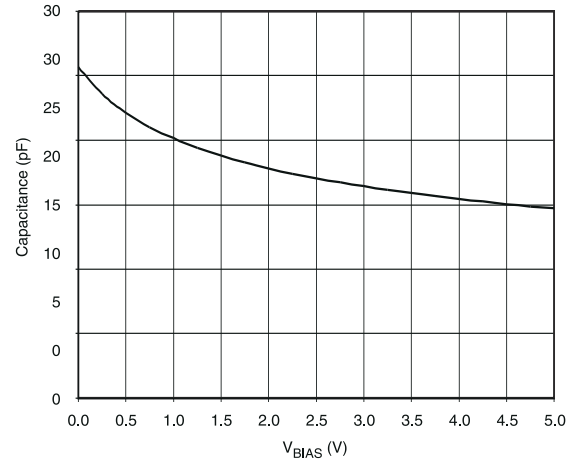


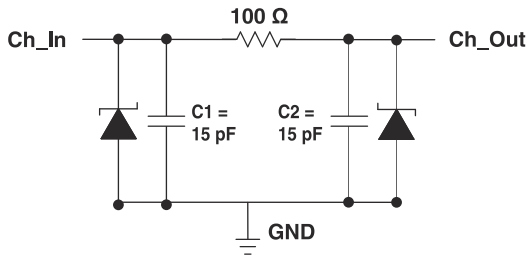
图 6-6. C1 or C2 Capacitance vs V_{BIAS}

7 Detailed Description

7.1 Overview

The TPDxF202 family is a series of highly integrated devices designed to provide EMI filtering in all systems subjected to electromagnetic interference. These filters also provide a Transient Voltage Suppressor (TVS) diode circuit for ESD protection which prevents damage to the application when subjected to ESD stress far exceeding IEC 61000-4-2 (Level 4).

7.2 Functional Block Diagram



7.3 Feature Description

The TPDxF202 family is a line of ESD and EMI filtering devices designed to reduce EMI emissions and provide system level ESD protection. Each device can dissipate ESD strikes above the maximum level specified by IEC 61000-4-2 international standard. Additionally, the EMI filtering structure reduces EMI emissions by providing high frequency roll-off.

7.3.1 Exceeds IEC61000-4-2 (Level 4) ESD Protection Requirements

The ESD protection on all pins exceeds the IEC 61000-4-2 level 4 standard. Contact and Air-Gap ESD are rated at ±25 kV.

7.3.2 Pi-Style C-R-C Filter Configuration

This family of devices has a pi-style filtering configuration composed of a series resistor and two capacitors in parallel with the I/O pins. The typical resistor value is 100 Ω and the typical capacitor values are 15 pF each. Signal attenuation is above 40 dB at 1 GHz to 3 GHz, which provides significant reduction in spurious emissions, with a bandwidth (3-dB loss) of 108 MHz. Crosstalk is attenuated 70 dB at 100 MHz.

7.3.3 Low 10-nA Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (typical) with a bias of 3.3 V.

7.3.4 Space-Saving DSBGA Package

The DSBGA package is characterized by a minimal footprint for savings in board space, fitting the design philosophy of portable devices.

7.3.4.1 Flow-Through Pin Mapping

The pinout of this device makes it easy to add protection to existing board layouts. The packages offer flow-through routing which requires minimal changes to existing board layout for addition of these devices.

7.4 Device Functional Modes

The TPDxF202 family of devices are passive-integrated circuits that passively filter EMI and trigger when voltages are above V_{BR} or below the lower diode voltage (– 0.6 V). During IEC 61000-4-2 ESD events, transient voltages as high as ±25 kV can be directed to ground through the internal diode network. Once the voltages on the protected line falls below the trigger levels, the device reverts to passive.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPDxF202 family are diode-type TVSs integrated with series resistors and parallel capacitors for filtering emitted EMI. As a signal passes through the device, higher frequency components are filtered out. This device also provides a path to ground during ESD events and isolates the protected IC. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. In particular, these filters are ideal for EMI filtering and protecting data lines from ESD at display, keypad, and memory interfaces.

8.2 Typical Application

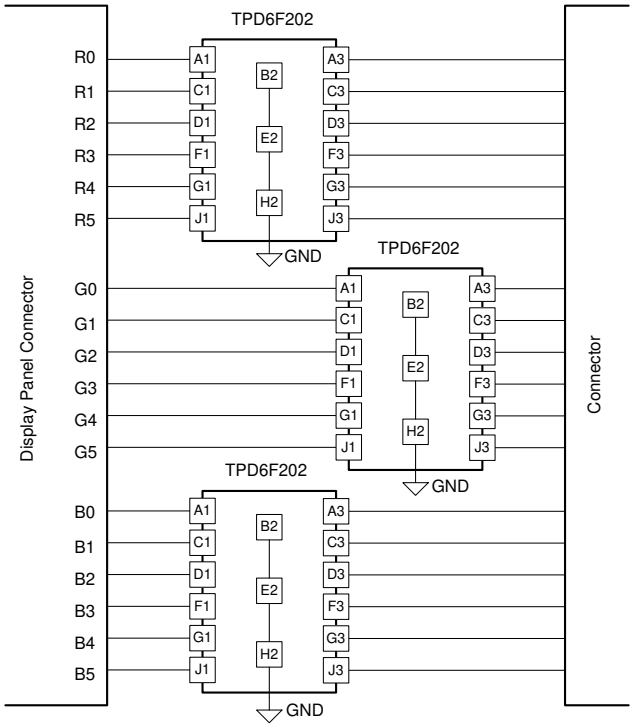


图 8-1. Display Panel Schematic

8.2.1 Design Requirements

For this design example, three TPD6F202 devices are used in an 18-bit display panel application. This application provides a complete ESD and EMI protection solution for the display connector. For the display panel application, the following parameters are in shown 表 8-1.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on all pins except GND	0 V to 5 V
Data Rate	200 Mbps
ESD Protection Level	IEC 61000-4-2 Level 4

8.2.2 Detailed Design Procedure

To begin the design process, some design parameters must be decided; the designer needs to know the operating frequency and the signal range on all the protected lines.

8.2.2.1 Signal Range on All Protected Lines

The TPD6F202 has 6 identical protection channels for signal lines. All I/O pins will support a signal range from 0 to 5.5 V.

8.2.2.2 Data Rate

The TPD6F202 has a 108-MHz, –3-dB bandwidth, which supports the data rate for this display.

8.2.2.3 ESD Protection Level

The contact and air-gap ratings of ± 25 kV for TPD6F202 exceeds the IEC 61000-4-2 Level 4 rating of ± 8-kV contact and ± 15-kV air-gap ratings.

8.2.3 Application Curve

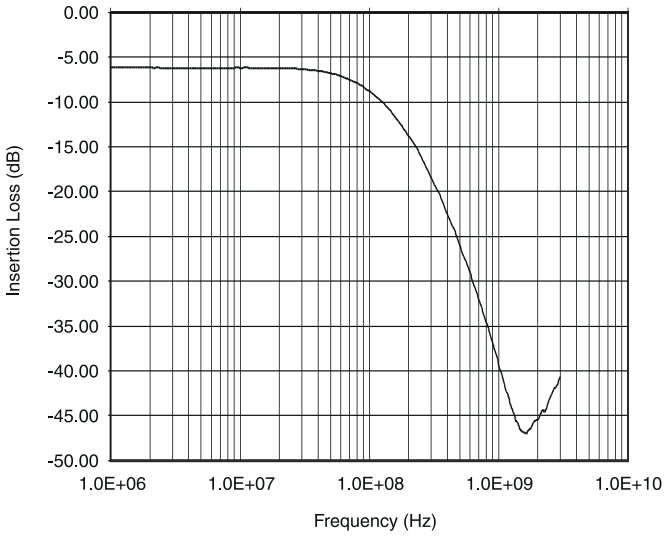


图 8-2. Frequency Response Data (0-V Bias)

9 Power Supply Recommendations

The TPDxF202 device is a passive ESD-protection device, and therefore, does not require a power supply. Take care to avoid violating the maximum-voltage specification to ensure that the device functions properly. The IO lines can tolerate up to 6-V DC.

10 Layout

10.1 Layout Guidelines

Typically, there are multiple EMI filters being used in portable applications to suppress the EMI interference. This means the total board area consumed by EMI filters are relatively large. One example of space-saving innovation is to place the EMI filters right under the connectors so that the main PCB space is not used. The YFU packages of the TPDxF202 series offer ultra low-profile package height which enables such innovative component placement in portable applications. Package under-fill is recommended while using the YFU packages in flex boards.

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

For maximum efficiency of filtering and ESD protection, while doing the board layout, take care to reduce board parasitic series inductances from package GND pins to board GND plane. The TPDxF202 devices must be connected to a ground plane with a micro via adjacent to the device GND pad. If this is not possible, the connection to the ground plane must be as direct as possible to minimize the inductance. Due to flow-through pin mapping, the signal pins routing is easily achieved in a single layer.

10.2 Layout Example

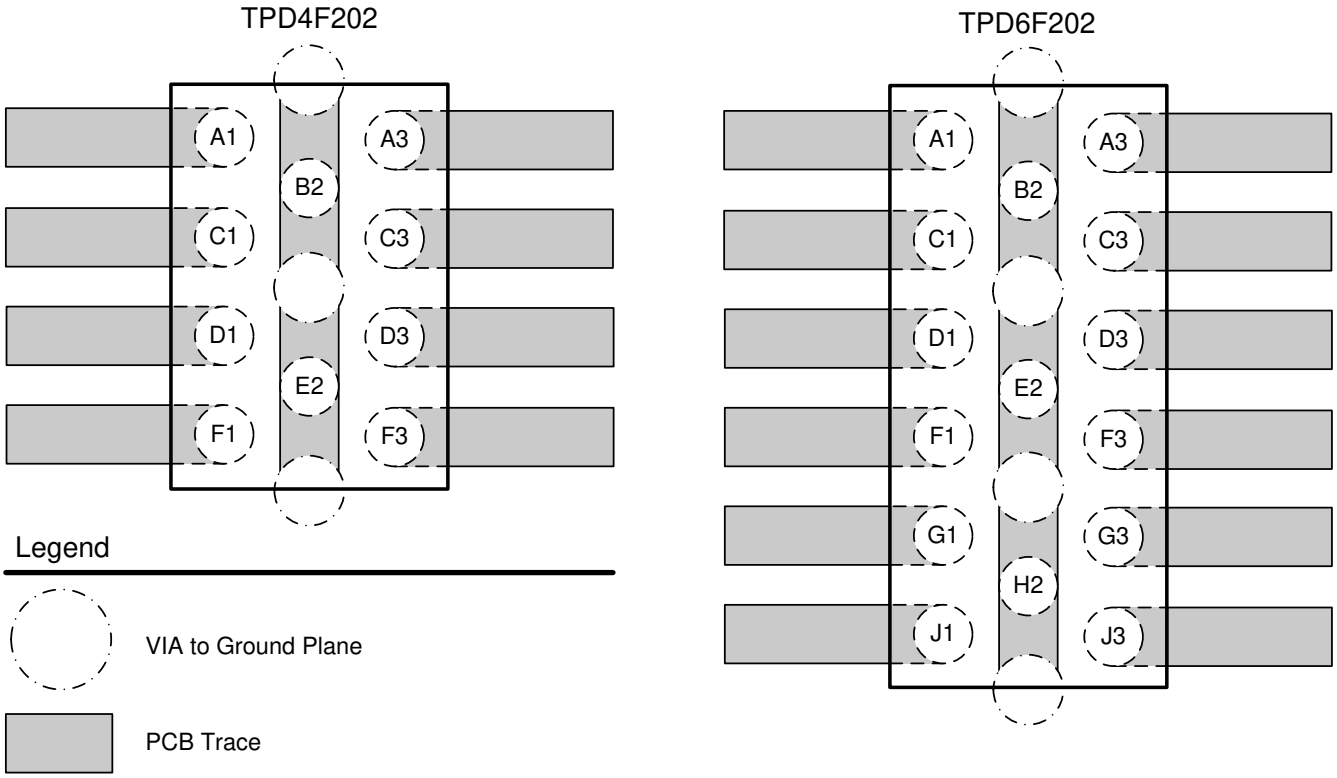


图 10-1. Board Layout With TPDxF202

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

The following documents contain additional information related to the use of the TPDxF202 device:

- Texas Instruments, *ESD Protection Layout Guide* application report
- Texas Intruments, *Reading and Understanding an ESD Protection Data Sheet* application report

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPD4F202	Click here	Click here	Click here	Click here	Click here
TPD6F202	Click here	Click here	Click here	Click here	Click here

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4F202YFUR	Obsolete	Production	DSBGA (YFU) | 10	-	-	Call TI	Call TI	-40 to 85	
TPD6F202YFUR	Obsolete	Production	DSBGA (YFU) | 15	-	-	Call TI	Call TI	-40 to 85	

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

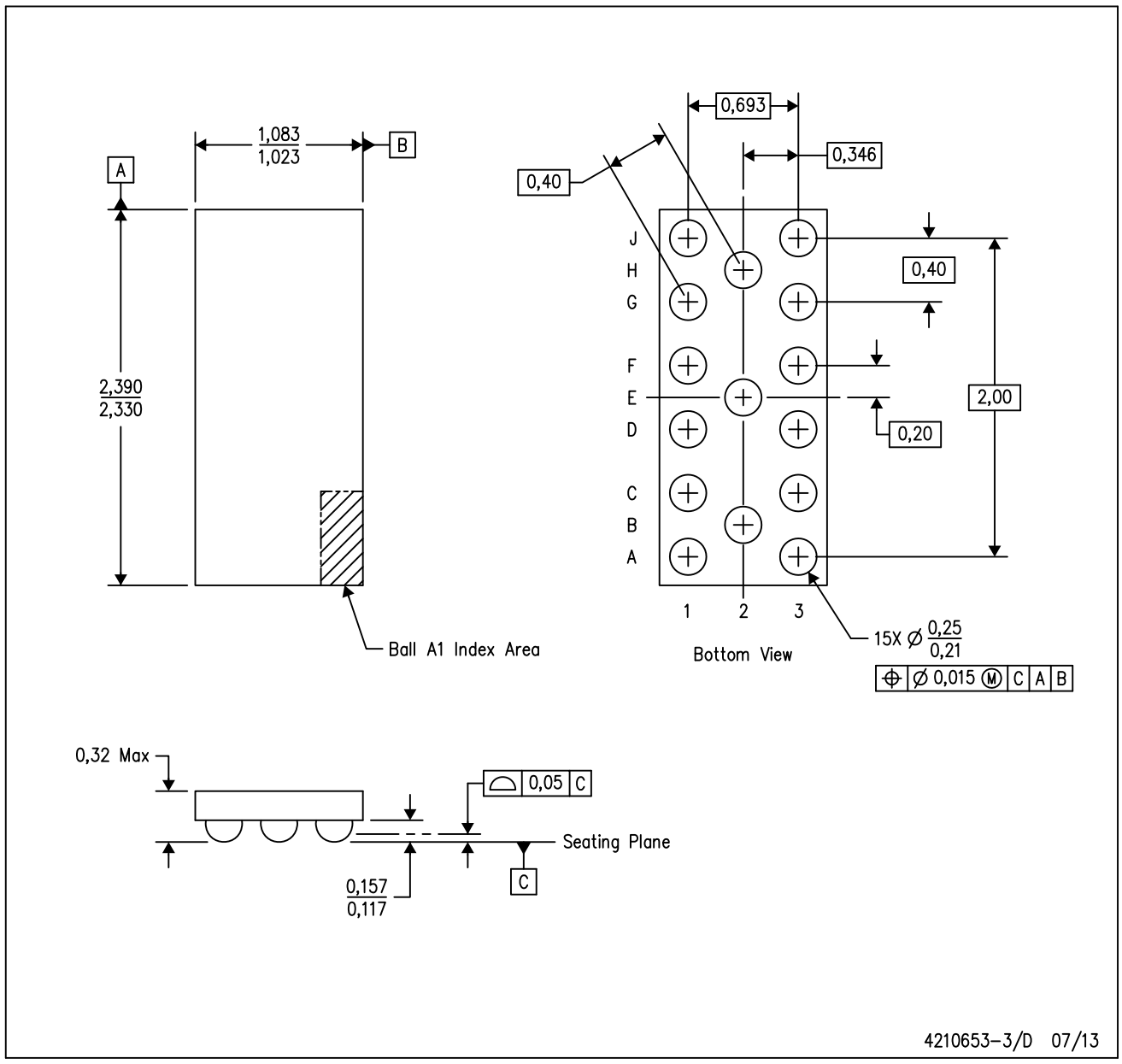
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

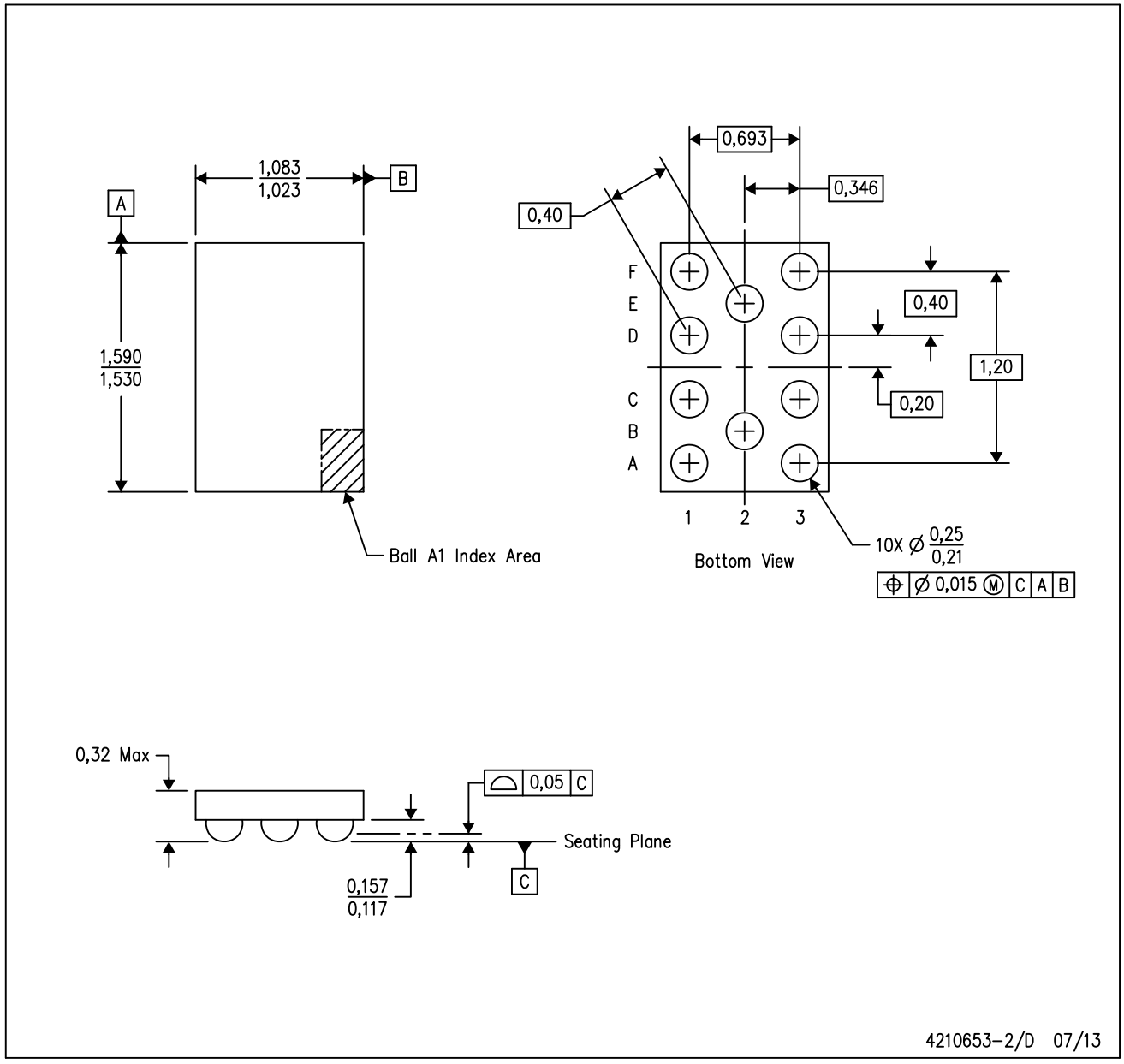
YFU (R–XBGA–N15) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

YFU (R–XBGA–N10) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
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