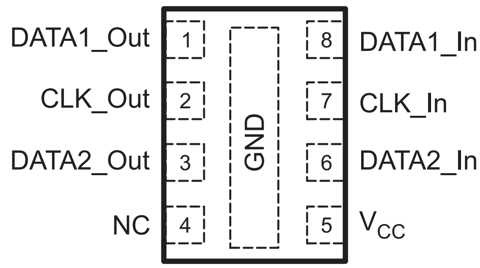
用于 SIM 卡接口并具有集成型 V_{CC}箝位的 EMI 滤波器

查询样品: **TPD3F303**

特性

- 双向 **EMI/RFI** 滤波和具有集成 **ESD** 保护功能的线路终端
- 牢固可靠的 **ESD** 保护超过了 **IEC 61000-4-2 (Level 4)** 规格的要求
  - **±15-kV** 人体模型**(HBM)**
  - **±15-kV IEC 61000-4-2** （接触放电）
  - **±15-kV IEC 61000-4-2** （空气间隙放电）
- 击穿电压： **6V**
- 低噪声 **C-R-C** 滤波器拓扑结构
- 集成型 V_{CC} 箝位免除了增设外部 **ESD** 保护的需要
- 采用节省空间的 **DPV** 封装 （**0.5mm** 间距）、**DQD** 封装 （**0.4mm** 间距）

TPD3F303 封装
(顶视图**)**



2.1-mm x 1.6-mm DPV (0.5-mm Pitch)
1.7-mm x 1.35-mm DQD (0.4-mm Pitch)

应用

- 移动手机
- **PDA**
- 视频控制台
- 便携式计算机

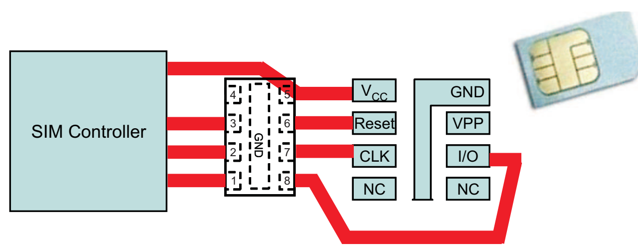


图 **1.** 在 **SIM** 卡接口上使用 **TPD3F303** 的电路板布局

说明/订购信息

TPD3F303 是一款用于 SIM 卡接口的三通道集成型 EMI 滤波器。 该器件集成了一个 V_{CC} 箝位，用于在 V_{CC} 线路上提供系统级的 ESD 保护。 在 CLK 线路上设有阻值为 47Ω 的终端电阻器，并在 DATA 和 RST 线路上采用了一个 100Ω 终端。

低通滤波器阵列降低了 EMI 辐射并提供了系统级的 ESD 保护。 凭借其小外形封装及易用型引脚配置，TPD3F303 滤波器可适合广泛的应用，例如：移动手机、 PDA、视频控制台、笔记本电脑等等。

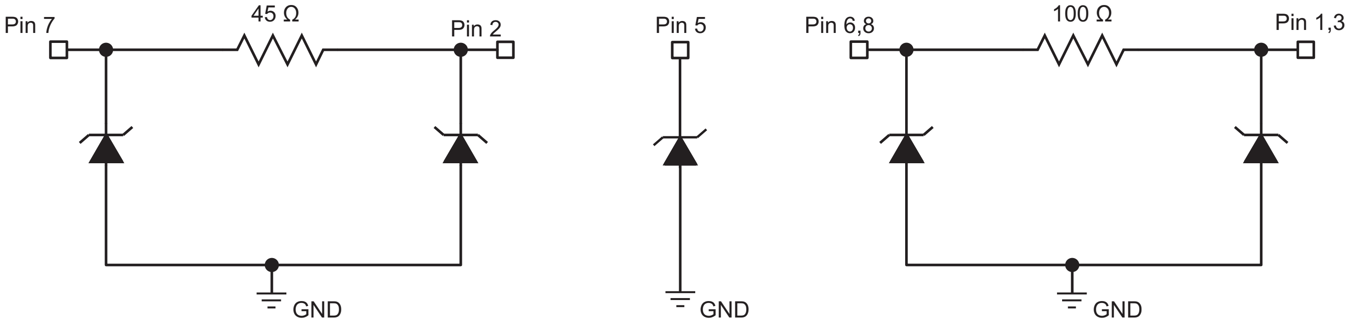
TPD3F303 专为抑制那些容易遭受电磁干扰的系统中的 EMI/RFI 噪声而设计。 该滤波器系列内置一个 ESD 保护电路，用于防止应用在遭受远远超过 IEC 61000-4-2 (Level 4) 规格值的 ESD 应力时受损。 TPD3F303 的规定工作温度范围为－40°C 至 85°C。

订购信息

T_A	封装(1) (2)		可订购的器件型号	顶端标记
－40°C 至 85°C	8 引脚 DPV 封装	卷带包装	TPD3F303DPVR	6SS
	8 引脚 DQD 封装	卷带包装	TPD3F303DQDR	6SS

(1) 封装图样、热数据和符号可登录 www.ti.com/package 获取。
(2) 如需了解最新的封装及订购信息，请参见本文件结尾处的 “Package Option Addendum （封装选项附录）”，或登录 TI 的网站 www.ti.com.cn 进行查询。

CIRCUIT DIAGRAMS



Schematic for CLK Line **Schematic for V_{CC}** **Schematic for DATA1, DATA2 Lines**

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	DPV/DQD PIN NO.		
DATAx_IN, DATAx_OUT	1, 3, 6, 8	Input, Output Pins	Data and Rest signals Input, Output pins. The DATA1 and DATA2 are symmetric circuits. They can be used interchangeably for either DATA or RESET pins based off board layout scheme.
CLK_OUT, CLK_IN V	2, 7	Input, Output Pins	Clock Input and Output signals.
V_{CC}	5	Power Clamp	ESD Clamp circuit for the V_{CC} pin.
NC	4	No Connect	Not connected to any internal circuit. Leave this pin floating.
GND	Central ground Pad	Ground	Ground connection for the EMI filter. It is very important to connect the device GND to the printed circuit board ground plane through Vias directly under the package.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	IO voltage tolerance	IO pins		5.5	V
T_A	Operating free-air temperature range		–40	85	°C
T_{stg}	Storage temperature range		–55	155	°C
	IEC 61000-4-2 Contact Discharge	IO pins		±15	KV
	IEC 61000-4-2 Air-gap Discharge	IO pins		±15	KV
	Human Body Model ESD	IO pins		±15	KV

(1) Stresses beyond those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{clamp}	Clamp voltage	I_{IO} = ±2 A	IO pin to ground			±10	V
I_I	Leakage current	R_{PU} = Open	IO pin to ground			0.1	μA
R_{CLK}	CLK series resistors			40	47	55	Ω
R_{DAT_RST}	Data/RST series resistors			85	100	115	Ω
C_{Total}	IO Capacitance	V_{IO} = 0 V	IO Pins to GND	16	20	24	pF
V_{BR}	Break-down Voltage	I_{IO} = 1 mA		6			V
$F_{–3dB}$	–3 dB BW for DATA/RESET line	Z_{SOURCE} = 50 Ω Z_{LOAD} = 50 Ω			294		MHz

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{-3dB}	–3 dB BW for CLK line	Z_{SOURCE} = 50 Ω Z_{LOAD} = 50 Ω		308		MHz

TYPICAL OPERATING CHARACTERISTICS

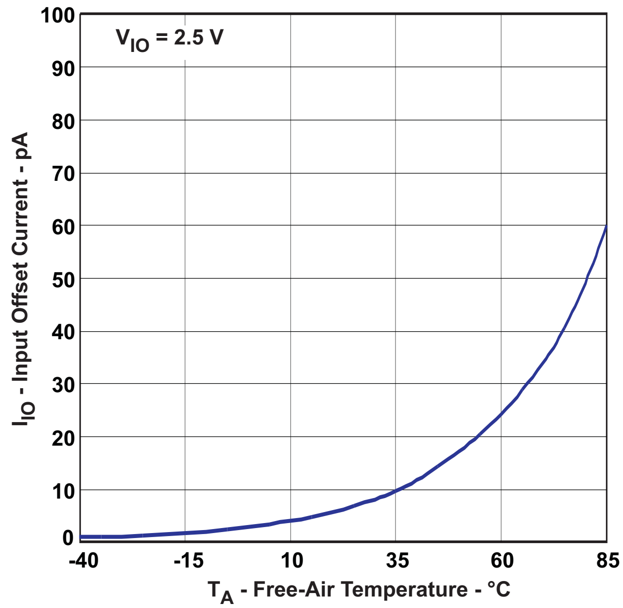


Figure 2. I_{IO} vs Temperature, VIO = 2.5V

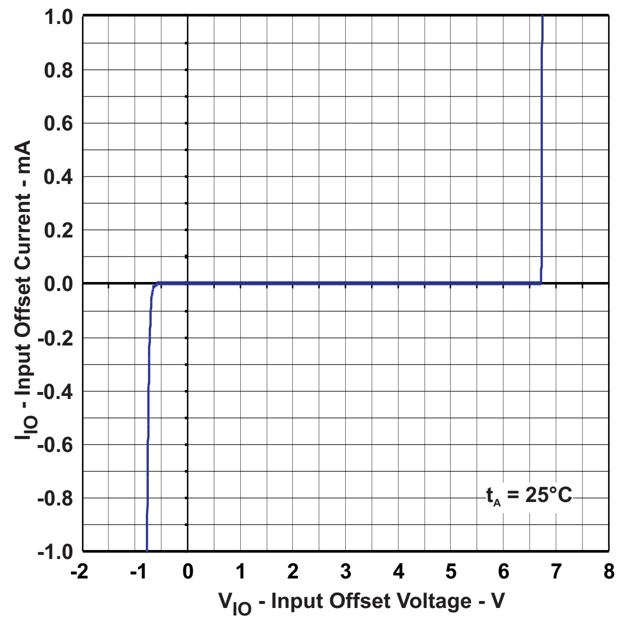


Figure 3. I_{IO} vs V_{IO}

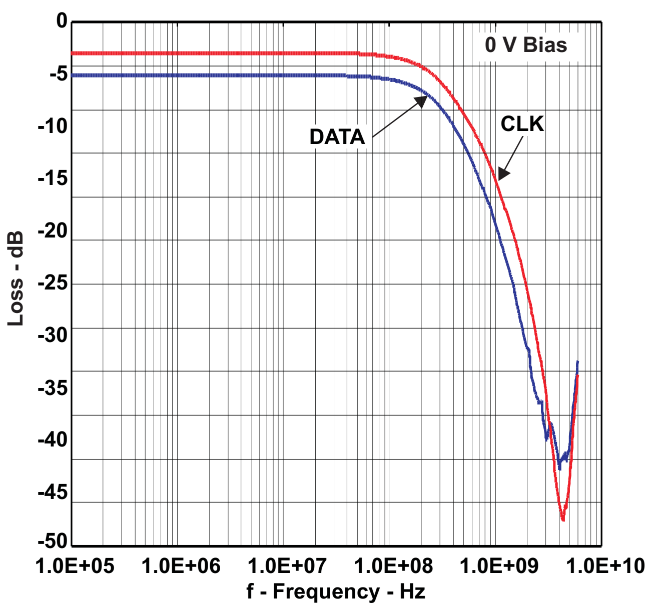


Figure 4. Frequency Response Data (0 V Bias)

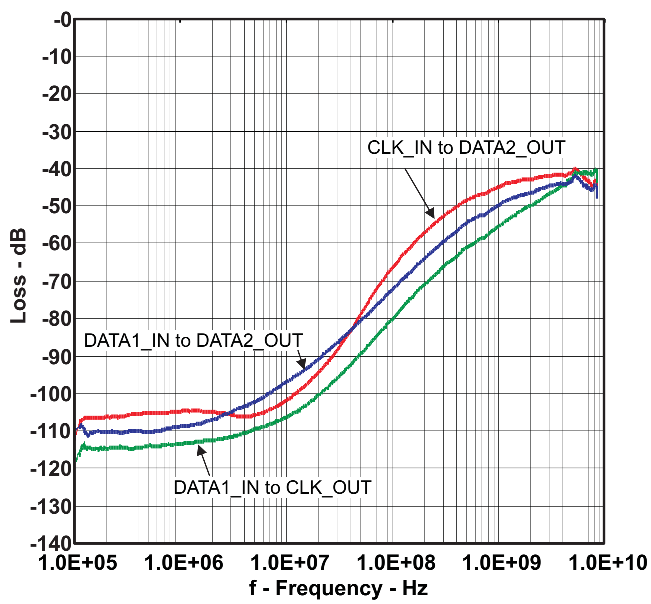


Figure 5. Channel-to-Channel Crosstalk

TYPICAL OPERATING CHARACTERISTICS (continued)

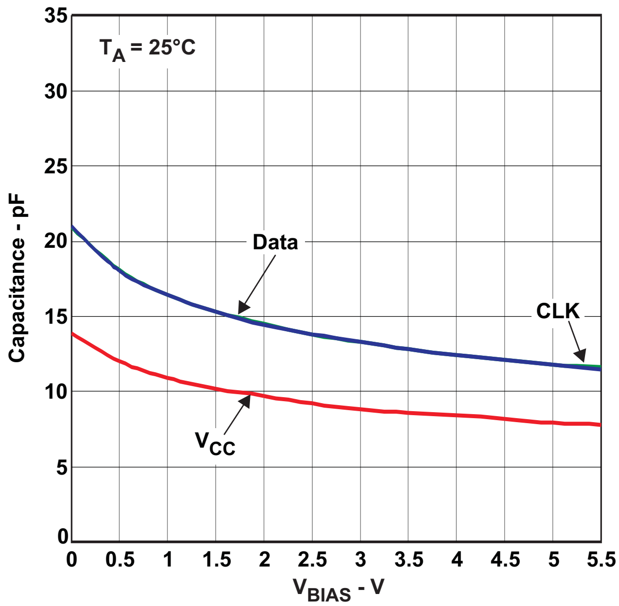


Figure 6. Capacitance vs V_{BIAS}, t_A = 25°C

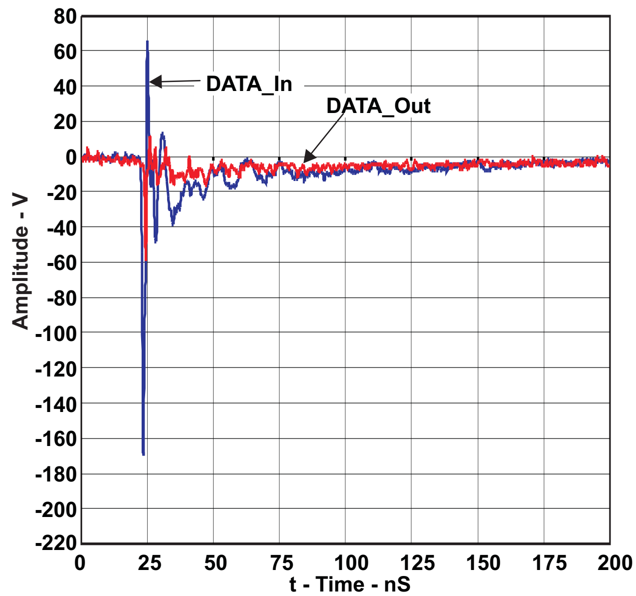


Figure 7. IEC Clamping Waveforms
–15 kV Contact, DATA1_In Stressed

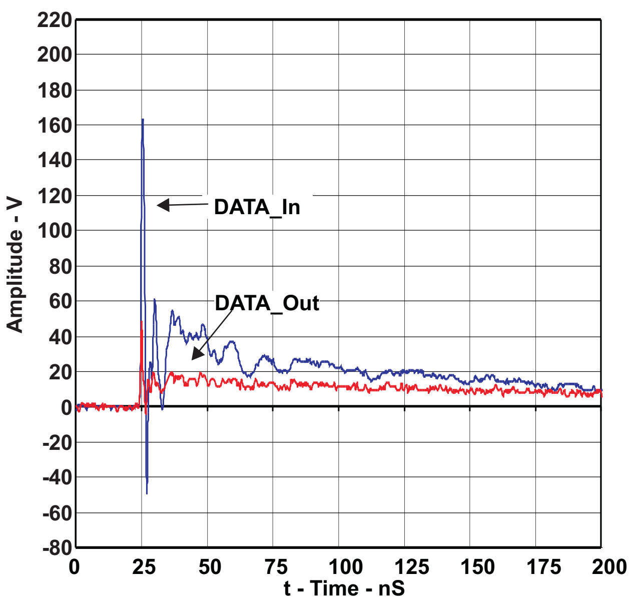


Figure 8. IEC Clamping Waveforms
+15 kV Contact, DATA1_In Stressed

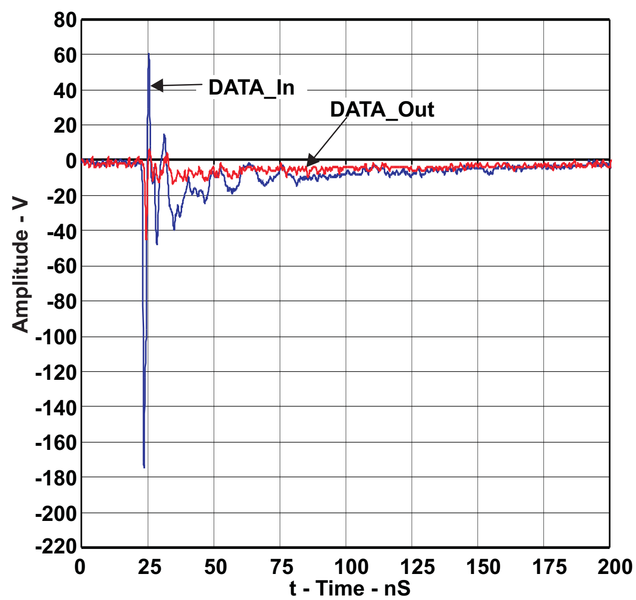


Figure 9. IEC Clamping Waveforms
–15 kV Contact, CLK_In Stressed

TYPICAL OPERATING CHARACTERISTICS (continued)

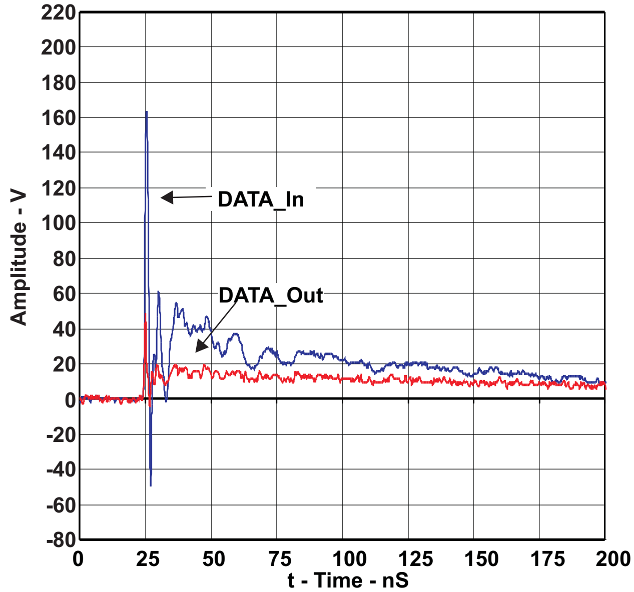


Figure 10. IEC Clamping Waveforms
+15 kV Contact, CLK_In Stressed

重要声明

可访问以下 URL 地址以获取有关其它 TI 产品和应用解决方案的信息：

产品	
放大器	http://www.ti.com.cn/amplifiers
数据转换器	http://www.ti.com.cn/dataconverters
DSP	http://www.ti.com.cn/dsp
接口	http://www.ti.com.cn/interface
逻辑	http://www.ti.com.cn/logic
电源管理	http://www.ti.com.cn/power
微控制器	http://www.ti.com.cn/microcontrollers
应用	
音频	http://www.ti.com.cn/audio
汽车	http://www.ti.com.cn/automotive
宽带	http://www.ti.com.cn/broadband
数字控制	http://www.ti.com.cn/control
光纤网络	http://www.ti.com.cn/opticalnetwork
安全	http://www.ti.com.cn/security
电话	http://www.ti.com.cn/telecom
视频与成像	http://www.ti.com.cn/video
无线	http://www.ti.com.cn/wireless

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD3F303DPVR	Active	Production	USON (DPV) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	6SS
TPD3F303DPVR.A	Active	Production	USON (DPV) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	6SS
TPD3F303DQDR	Active	Production	WSON (DQD) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	6SS
TPD3F303DQDR.A	Active	Production	WSON (DQD) | 8	3000 | LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	6SS

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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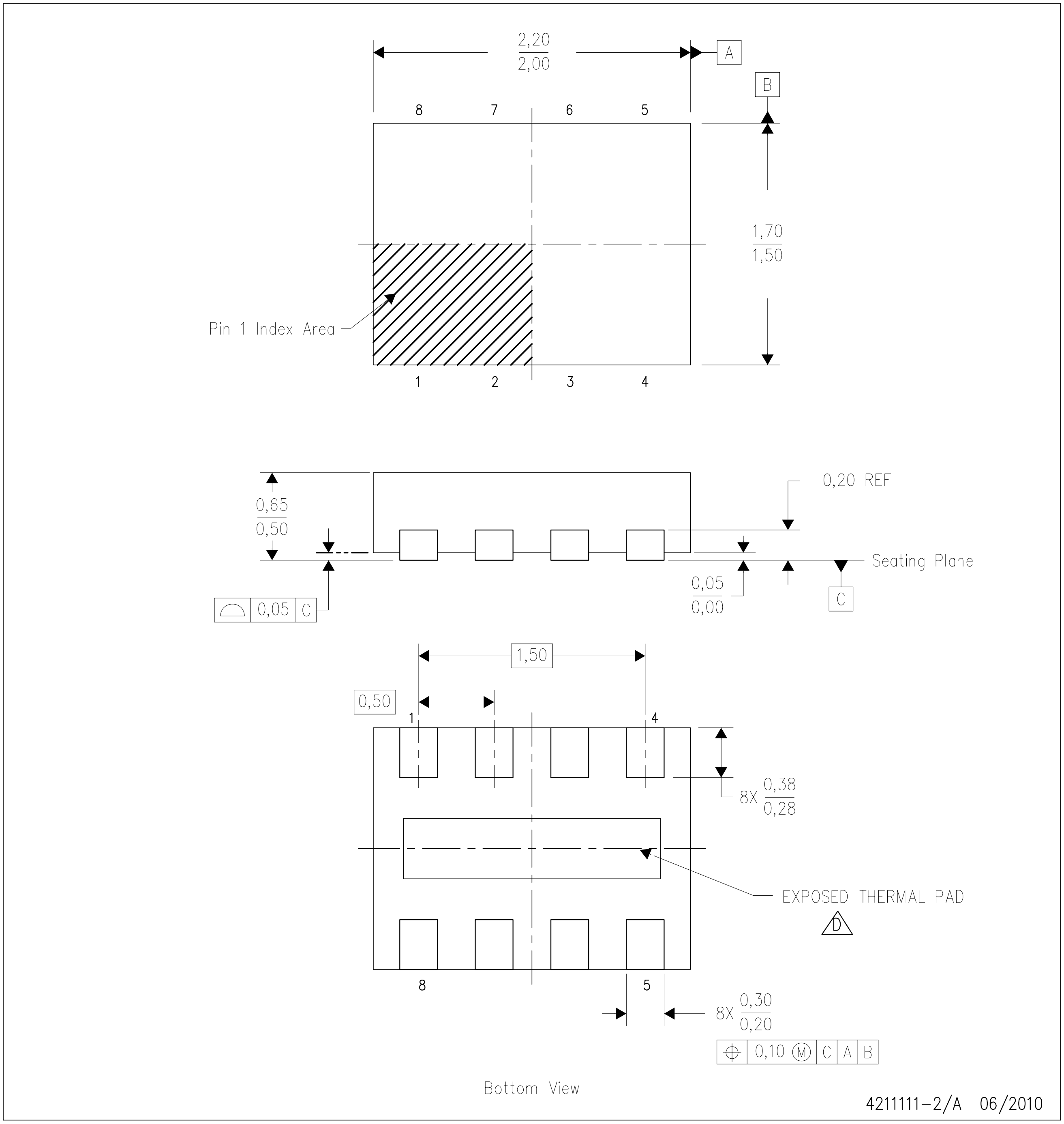
DPV (R–PUSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

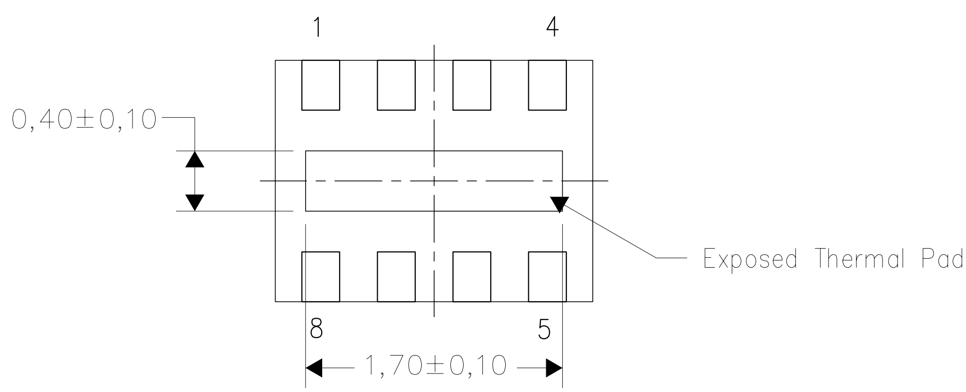
DPV (R-PUSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



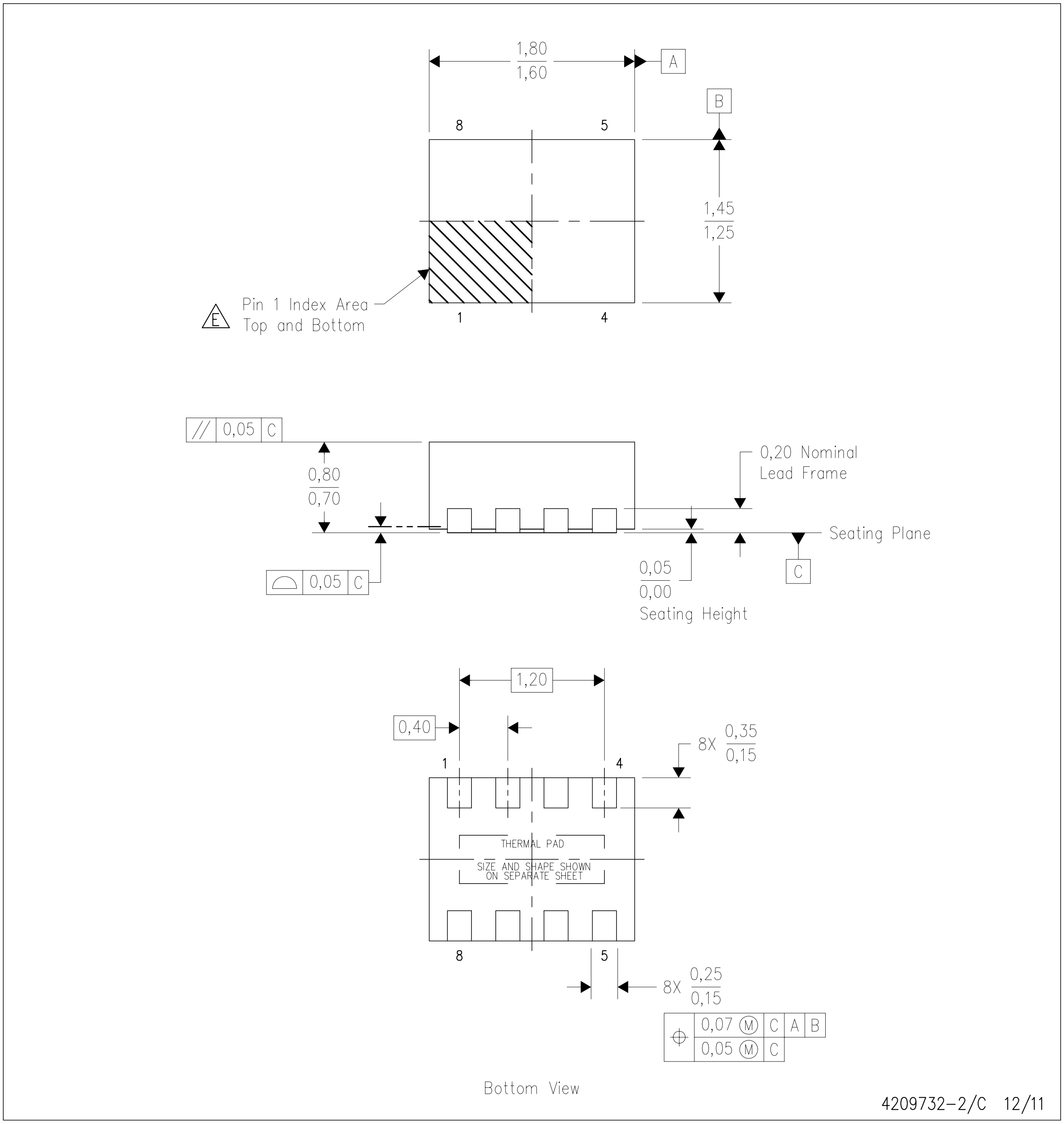
Bottom View

Exposed Thermal Pad Dimensions

4211680/A 04/11

NOTE: A. All linear dimensions are in millimeters

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.

DQD (R–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

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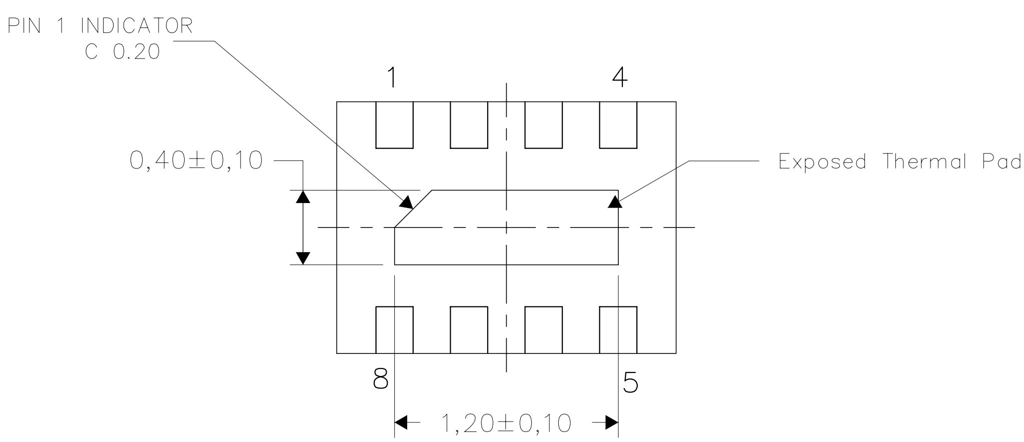


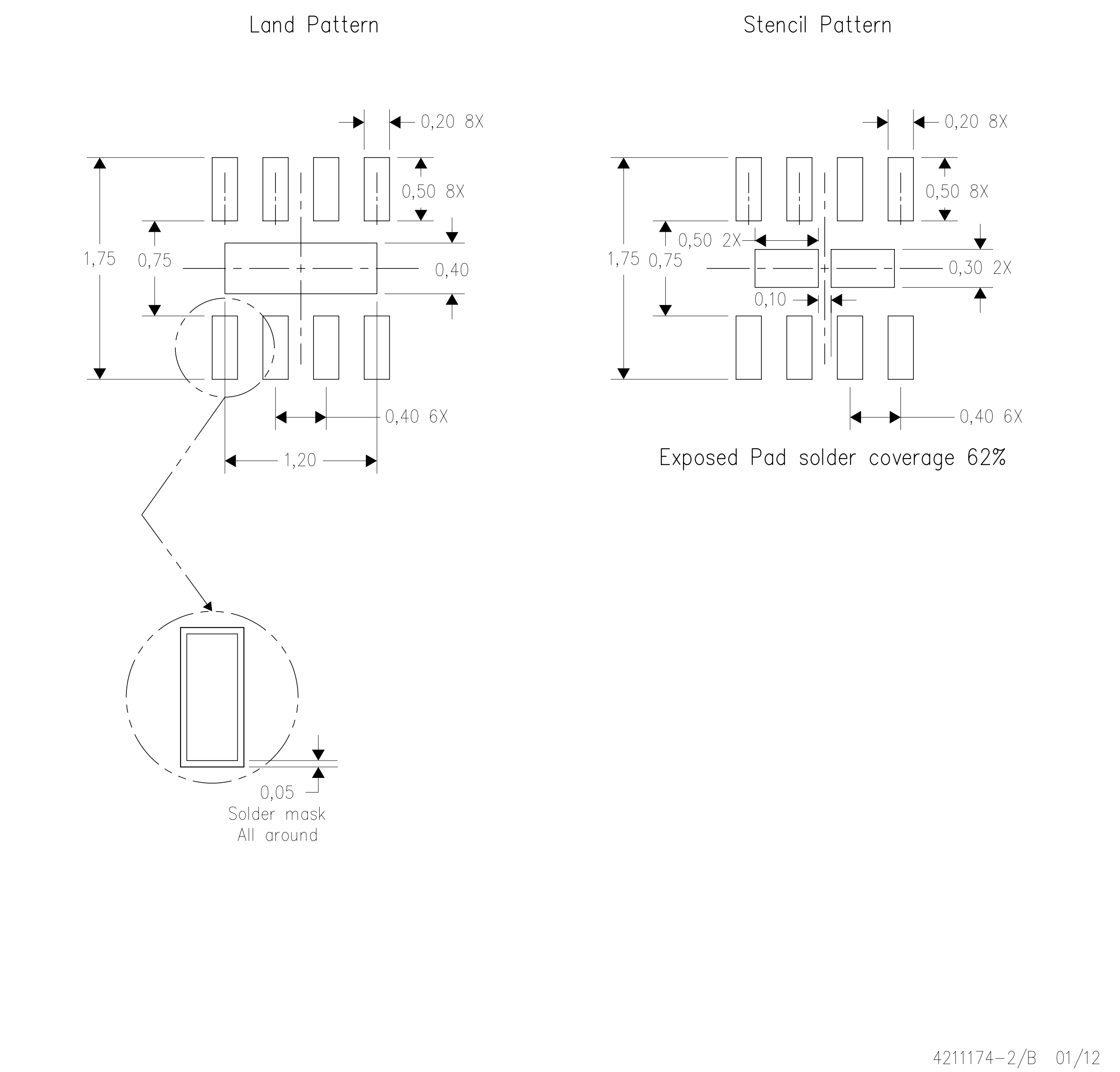
Bottom View

Exposed Thermal Pad Dimensions

4209733–2/C 12/11

NOTE: All linear dimensions are in millimeters

DQD (R-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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