双通道高速静电放电 (ESD) 保护器件

查询样品: TPD2E1B06

特性

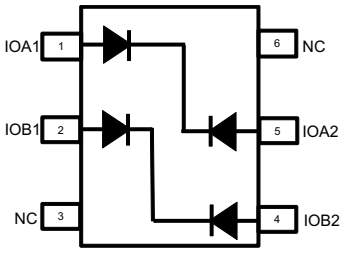
- 为低压输入输出 **(IO)** 接口提供系统级的静电放电 **(ESD)** 保护
- **IEC 61000-4-2 4** 级接触 **ESD** 额定值
- **IO** 电容值 **1pF**（典型值）
- 直流 **(DC)** 击穿电压 **7V**（最小值）
- 超低泄漏电流 **10nA**（最大值）
- 低 **ESD** 钳位电压
- 车用温度范围：**–40°C** 至 **125°C**
- 小型易于走线的 **DRL** 封装

应用范围

- 游戏机
- 电子书
- 便携式媒体播放器
- 数码摄像机

说明

TPD2E1B06 是一款双通道超低电容 ESD 保护器件。它提供 ±10KV IEC 接触 ESD 保护。 其 1pF 线路电容值使得这款器件适合于广泛应用。 典型应用接口为 USB 2.0，低压差分信令 (LVDS) 和 I2C。 有两个针对 TPD2E1B06 的常见布局布线方法并且都在应用信息部分中突出显示。



DRL
1.6 mm x 1.2 mm x 0.55mm
(0.5-mm pitch)

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM

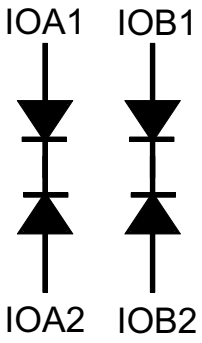


Figure 1. CIRCUIT SCHEMATIC DIAGRAM

TERMINAL FUNCTIONS

PIN		PIN TYPE	DESCRIPTION	USAGE
NAME	NO.			
IOA1	1	I/O	ESD protected channel	Please refer to the Application Information Section.
IOA2	5	I/O		
IOB1	2	I/O		
IOB2	4	I/O		
NC	3, 6	NC	No connect	Can be left floating, grounded, or connected to VCC

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
	Operating temperature range	–40 to 125	°C
	Storage temperature	–65 to 155	°C
	IEC 61000-4-2 contact ESD(1)	±10	kV
I_{PP}	Peak pulse current (tp = 8/20μs)(1)	2.5	A
P_{PP}	Peak pulse power (tp = 8/20μs)(1)	35	W

(1) Using Routing Option 1 or 2 as shown in Figure 2 or Figure 3.

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		TPD2E1B06 DRL (6) PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	349.7	ºC/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	120.5	
θ_{JB}	Junction-to-board thermal resistance	171.4	
ψ_{JT}	Junction-to-top characterization parameter	10.8	
ψ_{JB}	Junction-to-board characterization parameter	169.4	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage				5.5	V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, TLP, I/O to GND (1)(2)		11		V
		I_{PP} = 5 A, TLP, I/O to GND (1)(2)		15		V
V_{CLAMP}	Clamp voltage with ESD strike	I_{PP} = 1 A, TLP, GND to I/O (1)(2)		11		V
		I_{PP} = 5 A, TLP, GND to I/O (1)(2)		15		V
R_{DYN}	Dynamic resistance			0.9		Ω
C_{L1}	Pin 2 and 5 capacitance	Pin 1 and 4 = GND, f = 1MHz, V_{BIAS} = +2.5V (2)(3)		0.85		pF
C_{L2}	Pin 1 and 4 capacitance	Pin 2 and 5 = GND, f = 1MHz, V_{BIAS} = +2.5V (2)(4)		1.05		pF
V_{BR}	Break-down voltage	I_{IO} = 1 mA	7		9.5	V
I_{LEAK}	Leakage current	V_{BIAS} = +2.5 V		1	10	nA

(1) Transmission line pulse with rise time 10ns and pulse width 100ns.
(2) T_A = 25°C
(3) Using Routing Option 1, Figure 2.
(4) Using Routing Option 2, Figure 3.

APPLICATION INFORMATION

There are 2 channels of back-to-back diodes in TPD2E1B06DRL. The device should be routed in one of the two ways shown below. Routing option 1 is recommended because TPD2E1B06 is designed to maximize signal integrity in this configuration while still comply with IEC 61000-4-2 level 4 contact ESD rating.

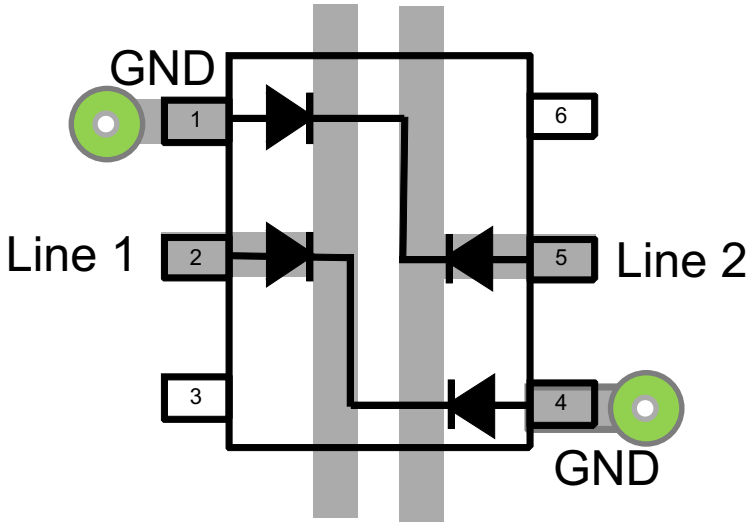


Figure 2. Routing Option 1

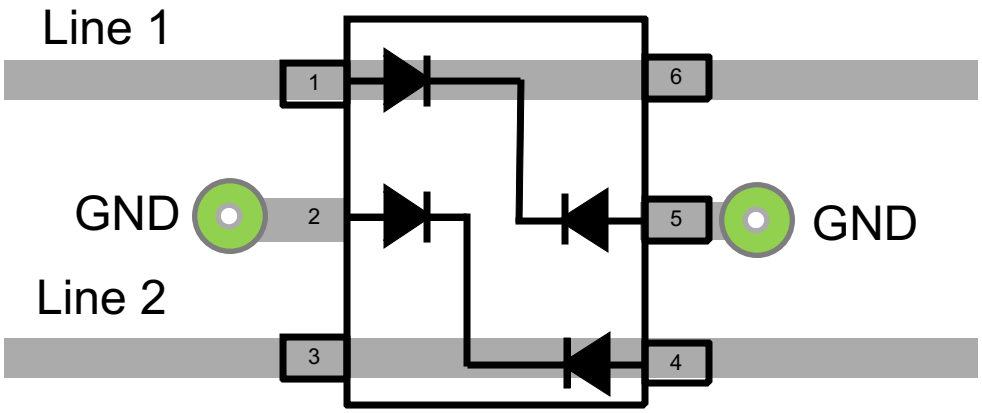


Figure 3. Routing Option 2

REVISION HISTORY

Changes from Original (July 2013) to Revision A	Page
• 将文档从预览改为生产数据。	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E1B06DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(DUH, DUL) DUG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

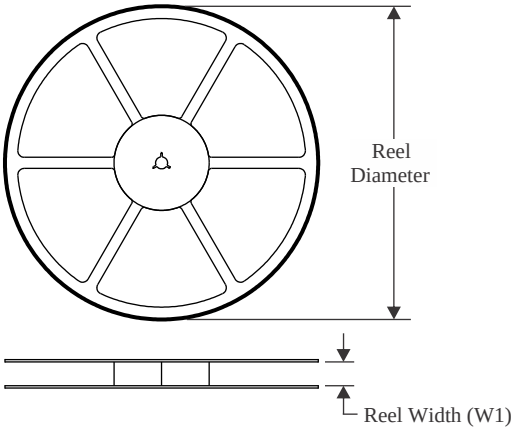
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

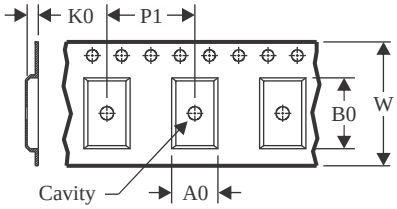
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

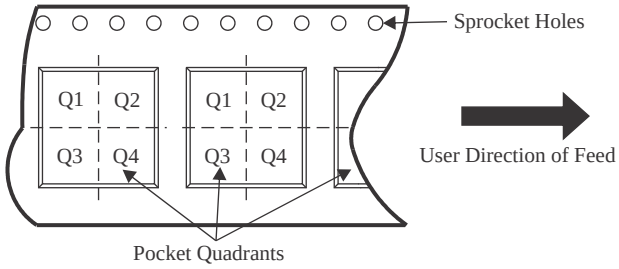


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

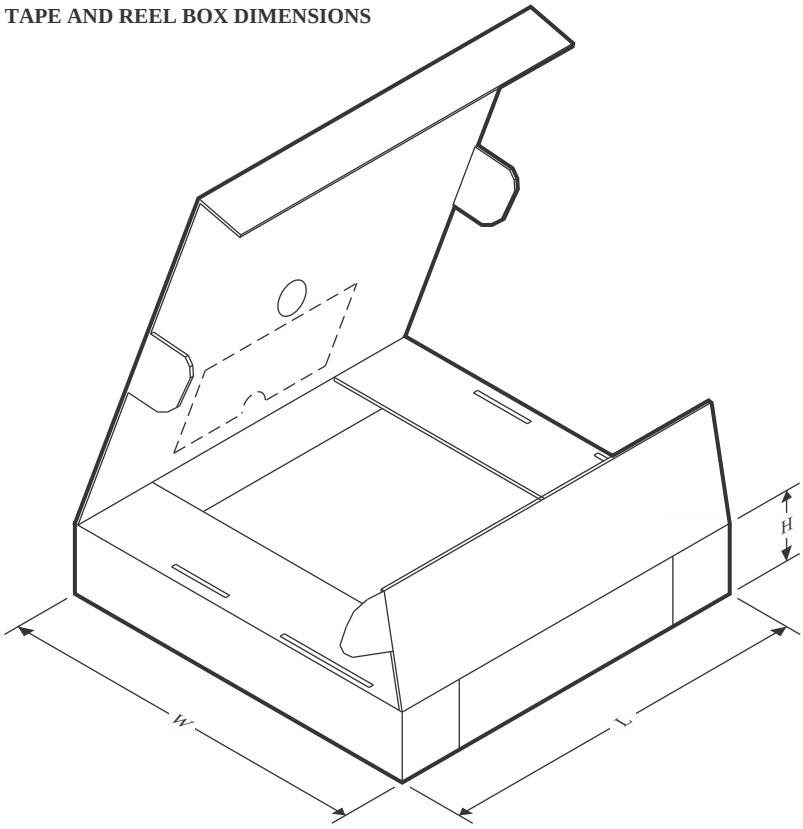
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

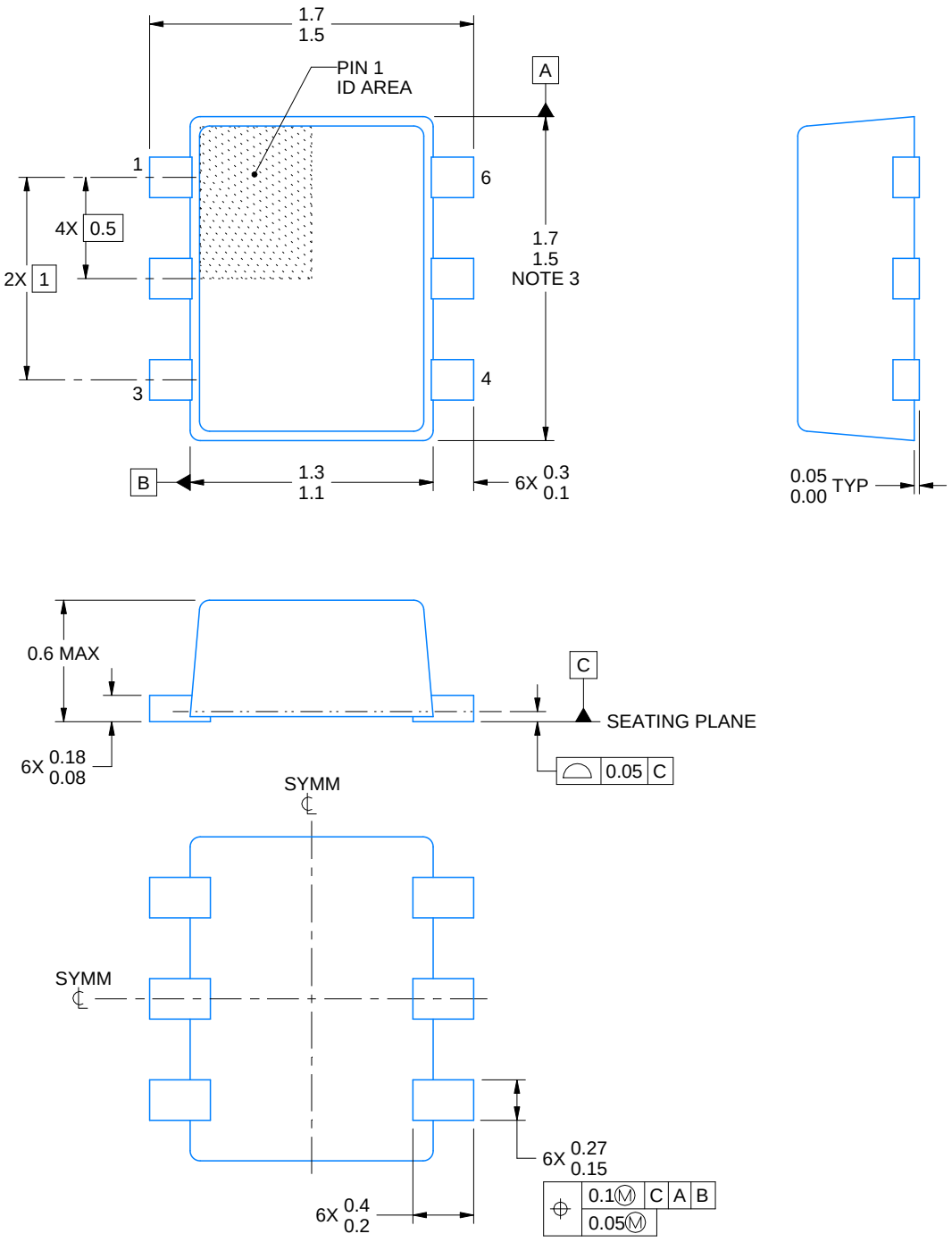
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	183.0	183.0	20.0
TPD2E1B06DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

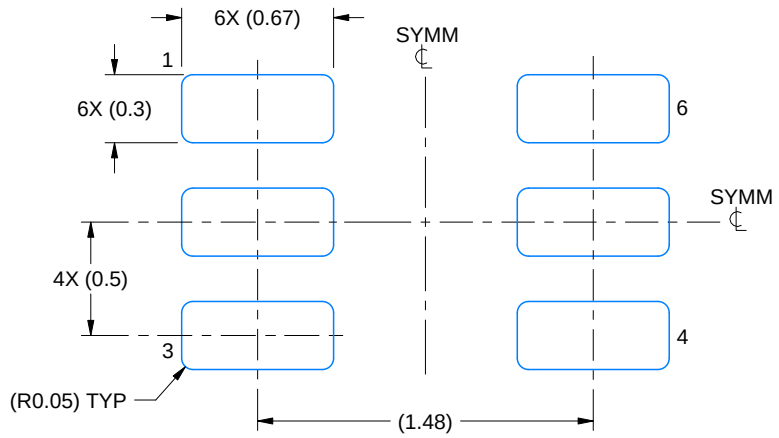
SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

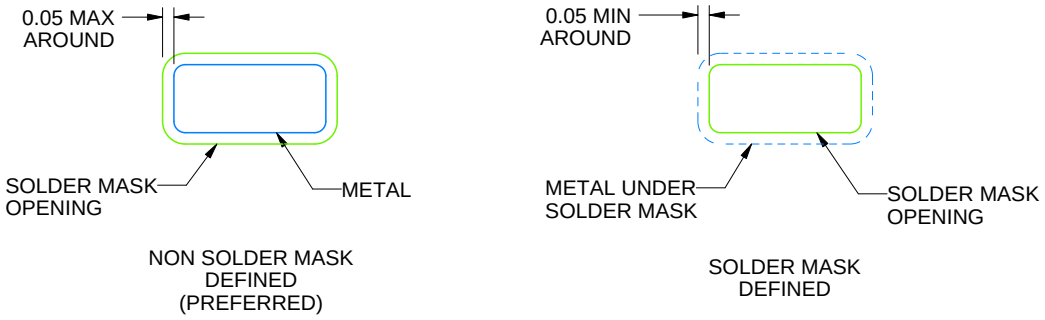


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/C 12/2021

NOTES: (continued)

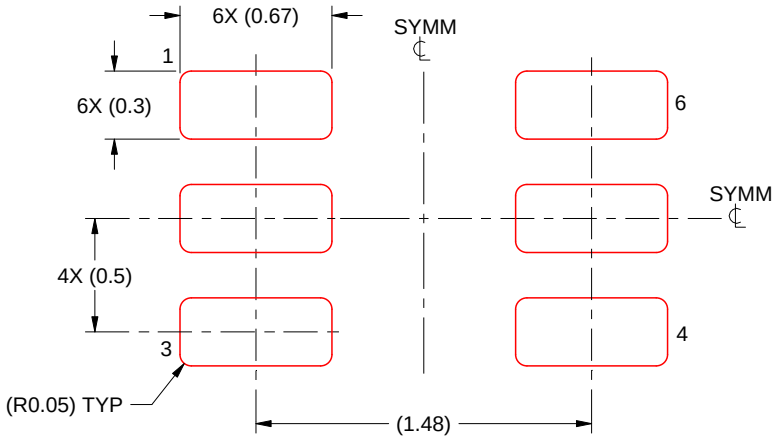
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/C 12/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265