具有可编程固定增益的 DirectPath™ 25-mW 头戴式耳机放大器

查询样品: TPA6139A2

特性

- **DirectPath™**
  - 消除噼啪/喀哒声
  - 免除输出隔直流电容器
  - 采用 **3 V** 至 **3.6 V** 电源电压
- 低噪声及 **THD**
  - **SNR > 105 dB** （在 **−1x** 增益条件下）
  - 典型 **Vn < 15 μVms** （在 **20 Hz**～**20 kHz** 及 **−1x** 增益条件下）
  - **THD+N < 0.003%** （在 **10 kΩ** 负载及 **−1x** 增益条件下）
- 可向 **600 Ω** 负载输送 **25 mW** 功率
- 可向 **5 kΩ** 负载提供 **2 Vrms** 输出电压
- 单端输入和输出
- 可编程增益选择功能减少了元件数量
  - **13x** 增益值
- 具有 **>80 dB** 衰减的有源静音
- 具有短路保护及热保护功能
- 对输出提供了 **±8 kV HBM ESD** 保护

应用

- **PDP / LCD TV**
- **Blu-ray Disc™, DVD Players**
- 迷你型/微型组合音响系统
- 声卡

说明

TPA6139A2PW 是一款 25-mW 无噼啪声立体声头戴式耳机驱动器，专为缩减组件数量、板级空间和成本而设计。 对于那些将尺寸和成本作为关键设计参数的单电源电子产品而言，该器件是理想的选择。

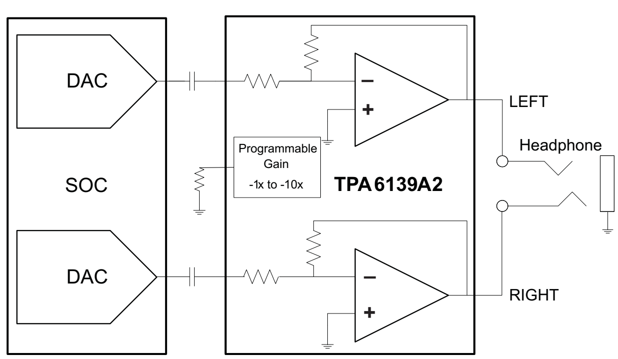
TPA6139A2 既不需要采用一个高于 3.3 V 的电源来产生其 25 mW 输出功率，也不需要一个分离轨电源。

TPA6139A2 的设计运用了 TI 的 DirectPath™ 专利技术，它集成了充电泵以产生一个负电源轨，可提供一个干净、无噼啪声的接地偏置输出。 TPA6139A2 能够向 32 Ω 负载输送 25 mW 驱动功率，以及向一个 600 Ω 负载提供 2 Vrms 电压。 另外，DirectPath 技术还允许去除昂贵的输出隔直流电容器。

该器件具有固定增益单端输入和一个增益选择引脚。 通过在该引脚上使用单个电阻器，设计人员就能够从 13 种内部可编程增益设定值中进行选择，以使线路驱动器与编解码器输出电平相匹配。 此外，这款器件还削减了组件数量和板级空间。

头戴式耳机输出具有 ±8kV HBM ESD 保护等级，因而实现了一种简单的 ESD 保护电路。 TPA6139A2 内置了具有 >80 dB 衰减的有源静音控制功能电路，旨在实现无噼啪声的静音接通/关断控制。

TPA6139A2 采用 14-引脚 TSSOP 封装和 16-引脚 QFN 封装。 如需一款引脚兼容的 2 Vrms 线路驱动器，请参见 DRV612。



English Data Sheet: SLOS700

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

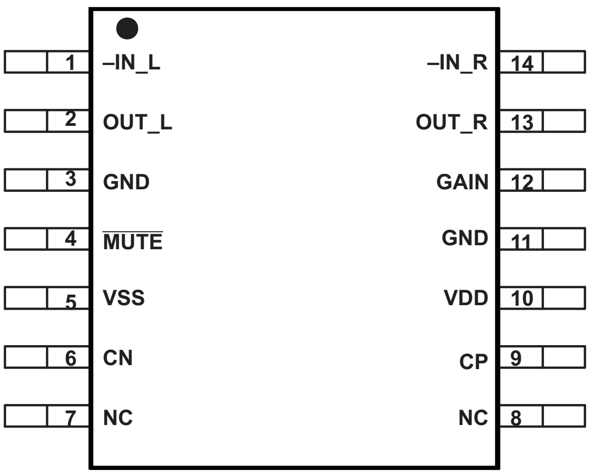
GENERAL INFORMATION

PIN ASSIGNMENT

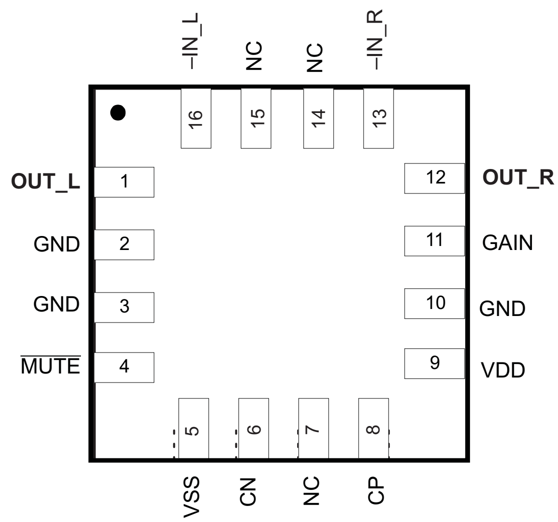
The TPA6139A2 is available in the:

- 14-pin TSSOP package (PW) or
- 16-pin QFN package (RGT)

PW PACKAGE
TSSOP
(TOP VIEW)



RGT PACKAGE
QFN
(TOP VIEW)

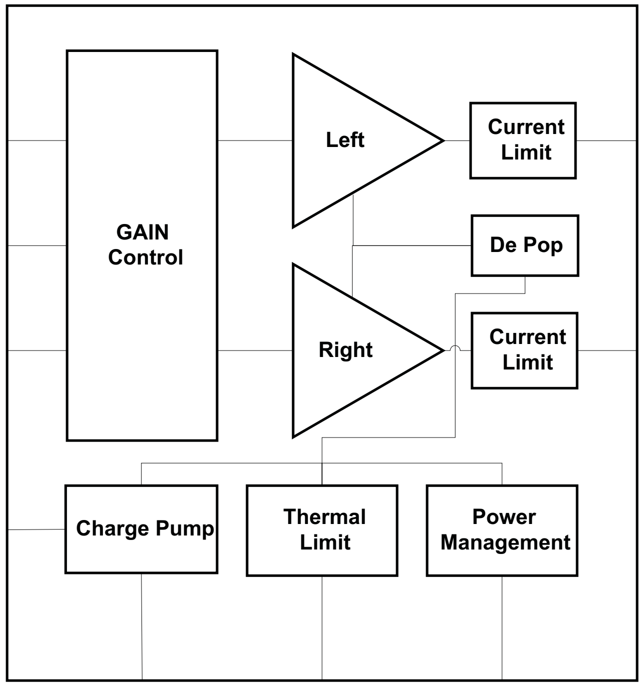


PIN FUNCTIONS

PIN			FUNCTION(1)	DESCRIPTION
NAME	PW NO.	RGT NO.		
-IN_L	1	16	I	Negative input, left channel
OUT_L	2	1	O	Output, left channel
GND	3, 11	2, 3, 10	P	Ground
MUTE	4	4	I	MUTE, active low
VSS	5	5	O	Change Pump negative supply voltage
CN	6	6	I/O	Charge Pump flying capacitor negative connection
NC	7, 8	7. 14, 15		No internal connection
CP	9	8	I/O	Charge Pump flying capacitor positive connection
VDD	10	9	P	Supply voltage, connect to positive supply
GAIN	12	11	I	Gain set programming pin; connect a resistor to ground. See Table 1 for recommended resistor values
OUT_R	13	12	O	Output, right channel
-IN_R	14	13	I	Negative input, right channel

(1) I = input, O = output, P = power

SYSTEM BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE	DESCRIPTION
–40°C to 85°C	TPA6139A2PW	14-pin TSSOP
–40°C to 85°C	TPA6139A2RGT	16-pin QFN

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC(1)		TPA6139A2 PW (14-Pin)	TPA6139A2 RGT (16-Pin)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	130	52	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	49	71	
θ_{JB}	Junction-to-board thermal resistance	63	26	
ψ_{JT}	Junction-to-top characterization parameter	3.6	3.0	
ψ_{JB}	Junction-to-board characterization parameter	62	26	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	9.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
VDD to GND		–0.3 to 4	V
Input voltage, V_I		VSS–0.3 to VDD+0.3	V
$\overline{\text{MUTE}}$ to GND		–0.3 to VDD+0.3	V
Maximum operating junction temperature range, T_J		–40 to 150	°C
Storage temperature		–40 to 150	°C
Lead temperature		260	°C
ESD Protection – HBM	OUT_L, OUT_R	8	kV
	All other pins	2	kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
VDD	Supply voltage	DC supply voltage	3.0	3.3	3.6	V
R_L				5		kΩ
V_{IL}	Low-level input voltage	$\overline{\text{MUTE}}$	38	40	43	%PVDD
V_{IH}	High-level input voltage	$\overline{\text{MUTE}}$	57	60	66	%PVDD
T_A	Free-air temperature		–40	25	85	°C

ELECTRICAL CHARACTERISTICS

VDD = 3.3V, R_{Load} = 32Ω, T_A = 25°C, Charge pump: C_{CP} = 1.0 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\lvert V_{OS}\rvert$	Output offset voltage	VDD = 3.3 V, input ac-coupled		0.5	1	mV
PSRR	Power-supply rejection ratio		70	80		dB
V_{OH}	High-level output voltage	VDD = 3.3 V	3.1			V
V_{OL}	Low-level output voltage	VDD = 3.3 V			–3.05	V
Vuvp_on	PVDD, under voltage detection				2.8	V
Vuvp_hysteresis	PVDD, under voltage detection, hysteresis			200		mV
Fcp	Charge pump switching frequency			350		kHz
$\lvert I_{IH}\rvert$	High-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V_{IH} = VDD			1	μA
$\lvert I_{IL}\rvert$	Low-level input current, $\overline{\text{MUTE}}$	VDD = 3.3 V, V_{IL} = 0 V			1	μA
I (VDD)	Supply current, no load	VDD, $\overline{\text{MUTE}}$ = 3.3 V		25		mA
	Supply current, MUTED	VDD = 3.3 V, $\overline{\text{MUTE}}$ = GND		25		mA
Tsd	Thermal shutdown			150		°C
	Thermal shutdown hysteresis			15		°C
P_O	Output Power, outputs in phase	THD+N = 1%, f = 1kHz, 32Ω load		25		mW
V_O	Output Voltage, outputs in phase	THD+N = 1%, f = 1kHz, 32Ω load		0.9		V_{rms}
		THD+N = 1%, f = 1kHz, 600Ω load		2.0		
THD+N	Total Harmonic distortion plus noise	f = 1kHz, 32Ω load, Po= 25mW, -1x gain		0.03%		
THD+N	Total Harmonic distortion plus noise	f = 1kHz, 10kΩload, Vo=2 Vrms, -1x gain		0.005%		
ΔA_V	Gain matching	Between left and right channels		0.25		dB
Z_O	Output impedance when muted	$\overline{\text{MUTE}}$ = GND			1	Ω
	Input to output attenuation when muted	$\overline{\text{MUTE}}$ = GND		80		dB
SNR	Signal to noise ratio	A-weighted, AES17 filter, 1Vrms ref 32Ω load, -1x gain		99		dB
	Signal to noise ratio	A-weighted, AES17 filter, 2Vrms ref 600Ω load, -1x gain		105		dB
V_n	Noise voltage	A-weighted, AES17 filter, Gain=-2x		12		μV
	Slew rate			4.5		V/μs
Gbw	Unity Gain bandwidth			8		MHz
Crosstalk	Channel to channel	f = 1kHz, Rload = 32Ω, Po= 25mW		–85		dB
Vincm_pos	Positive Common mode input voltage			+2.0		V
Vincm_neg	Negative Common mode input voltage			–2.0		V
I_{lim}	Output current limit			60		mA

PROGRAMMABLE GAIN SETTINGS

V_{DD} = 3.3 V, R_{load} = 32 kΩ, T_A = 25°C, Charge pump:= C_{CP} 1 µF, C_{IN} = 1.0 µF, 1 x gain select (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	TPA6139A2			UNIT
			MIN	TYP	MAX	
R_Tol	Gain programming resistor tolerance				2%	
ΔA_V	Gain matching	Between left and right channels		0.25		dB
	Gain step tolerance			0.10		dB
	Gain steps	Gain resistor 2% tolerance				V/V
		249k or higher		–2.0		
		82k0		–1.0		
		49k2		–1.5		
		35k1		–2.3		
		27k3		–2.5		
		20k5		–3.0		
		15k4		–3.5		
		11k5		–4.0		
		9k09		–5.0		
		7k50		–5.6		
		6k19		–6.4		
		5k11		–8.3		
		3k90		–10.0		
	Input impedance	Gain resistor 2% tolerance				kΩ
		249k or higher		37		
		82k0		55		
		49k2		44		
		35k1		33		
		27k3		31		
		20k5		28		
		15k4		24		
		11k5		22		
		9k09		18		
		7k50		17		
		6k19		15		
		5k11		12		
		3k90		10.0		

(1) If pin 12, GAIN, is left floating an internal pull-up sets the gain to –2.0x
Gain setting is latched during power-up

TYPICAL CHARACTERISTICS, LINE DRIVER

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{PUMP} = $C_{(VSS)}$ = 10 µF, Gain Step = –2V/V (unless otherwise noted)

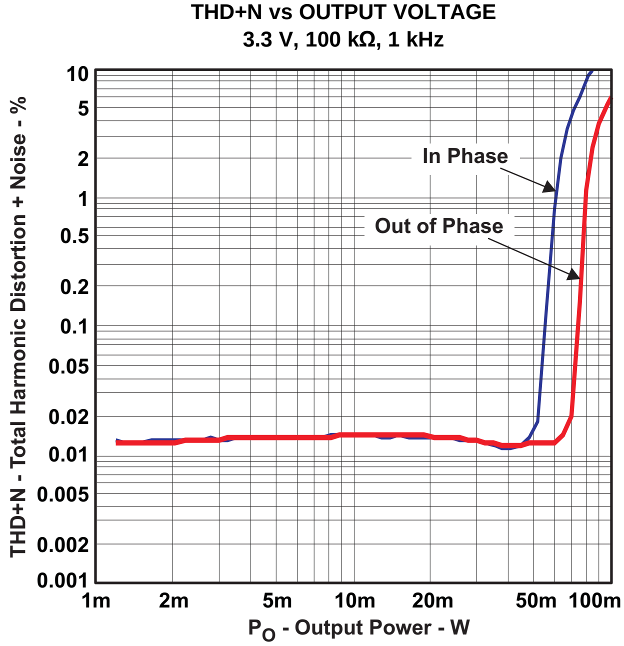


Figure 1.

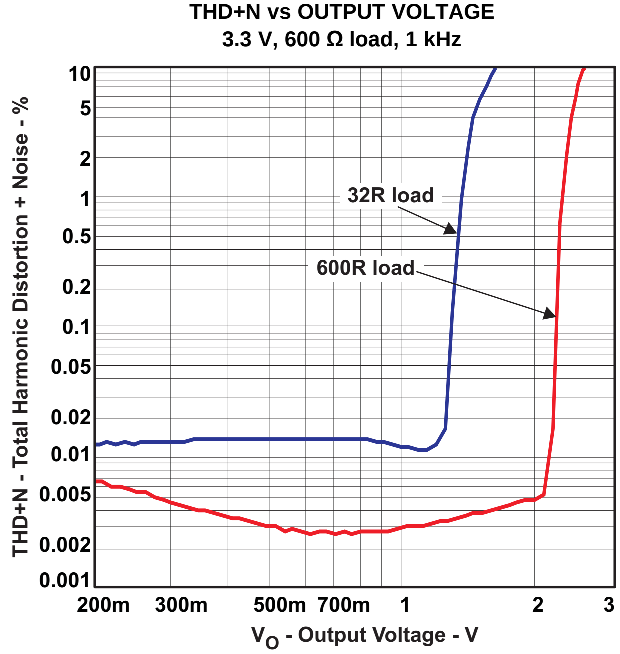


Figure 2.

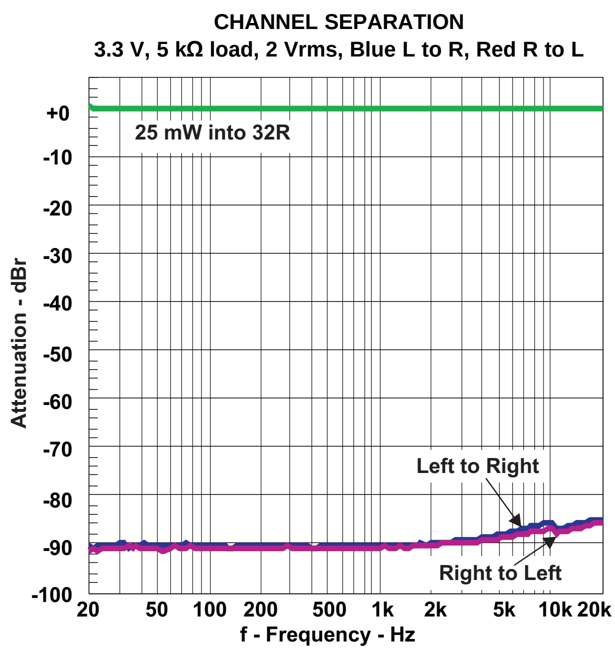


Figure 3.

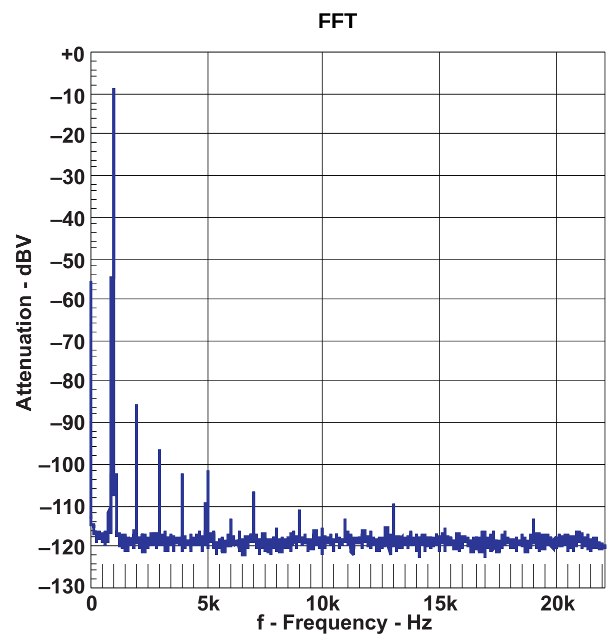


Figure 4.

TYPICAL CHARACTERISTICS, LINE DRIVER (continued)

V_{DD} = 3.3 V, T_A = 25°C, R_L = 2.5 kΩ, C_{PUMP} = $C_{(VSS)}$ = 10 µF, Gain Step = –2V/V (unless otherwise noted)

Gain vs FREQUENCY

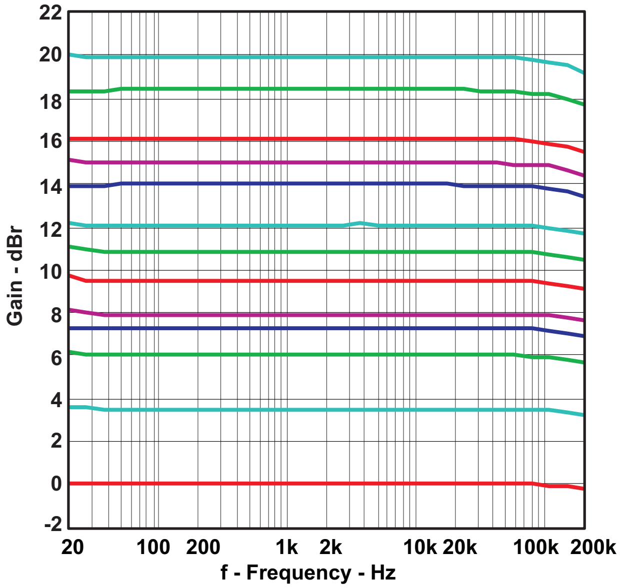


Figure 5.

TOTAL HARMONIC DISTORTION vs FREQUENCY

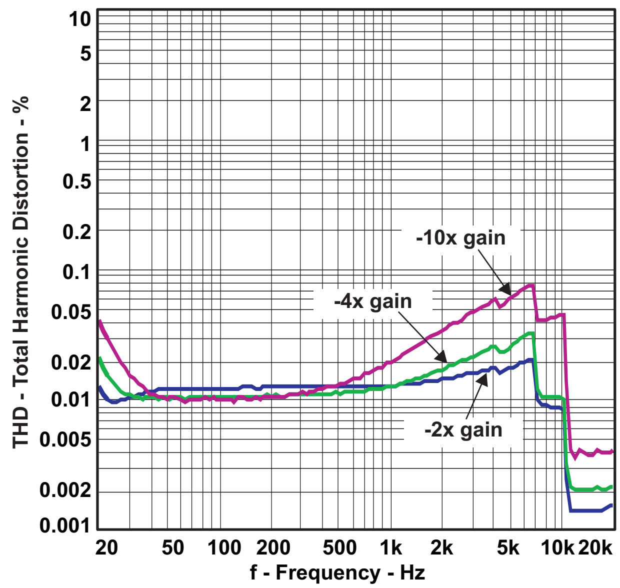


Figure 6.

MUTE TO UN-MUTE

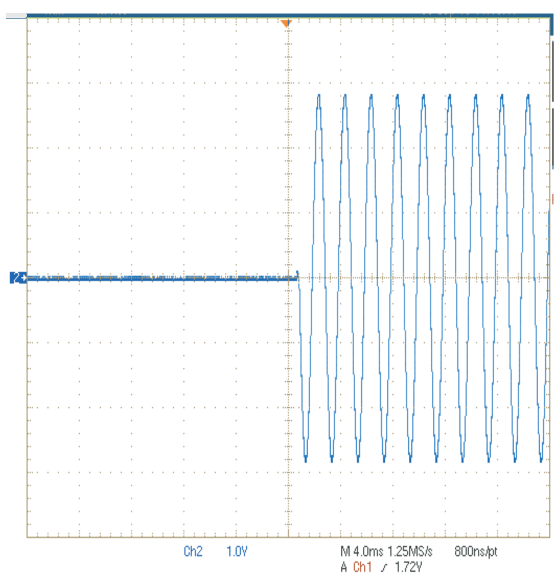


Figure 7.

UN-MUTE TO MUTE

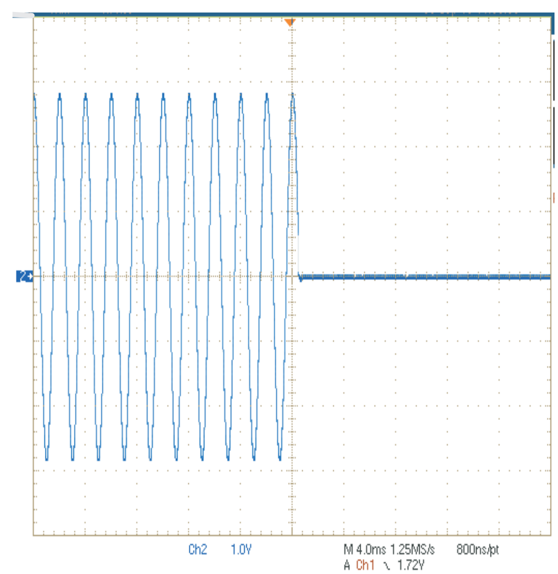


Figure 8.

APPLICATION INFORMATION

LINE DRIVER AMPLIFIERS

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 9 illustrates the conventional line-driver amplifier connection to the load and output signal.

DC blocking capacitors are often large in value, and a mute circuit is needed during power up to minimize click and pop. The output capacitor and mute circuit consume PCB area and increase cost of assembly, and can reduce the fidelity of the audio output signal.

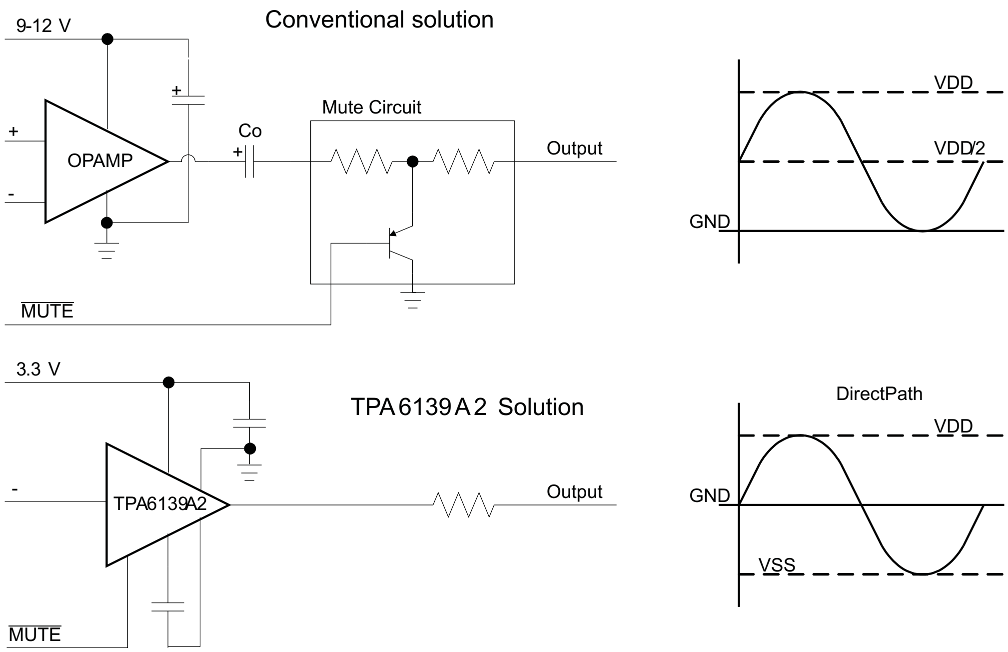


Figure 9. Conventional and DirectPath Line Driver

The DirectPath™ amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail.

Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split supply mode.

The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. Combining this with the built-in click and pop reduction circuit, the DirectPath™ amplifier requires no output dc blocking capacitors.

The bottom block diagram and waveform of Figure 9 illustrate the ground-referenced line-driver architecture. This is the architecture of the TPA6139A2.

COMPONENT SELECTION

Charge Pump

The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR capacitors are an ideal selection, and a value of 1μF is typical. Capacitor values that are smaller than 1μF cannot be recommended as it limits the negative voltage swing in low impedance loads.

Decoupling Capacitors

The TPA6139A2 is a DirectPath™ amplifier that requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, placed as close as possible to the device VDD leads works best. Placing this decoupling capacitor close to the TPA6139A2 is important for the performance of the amplifier. For filtering lower frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier also helps, but it is not required in most applications because of the high PSRR of this device.

Gain-Setting

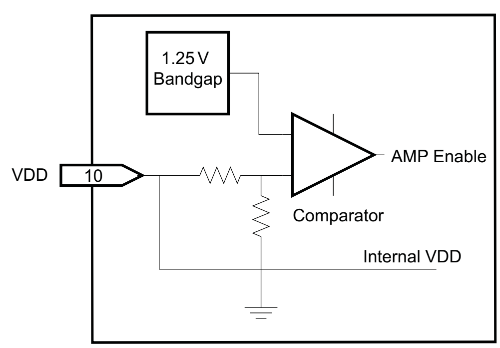
The gain setting is programmed with the GAIN pin individually for line driver and headphone section. Gain setting is latched when the $\overline{\text{MUTE}}$ pin is set high. Table 1 lists the gain settings. The default gain with the gain-set pin left open is –2x.

Table 1. Gain Settings

Gain_set RESISTOR	GAIN	GAIN (dB)	INPUT RESISTANCE
No connect	–2.0x	6.0	37k
82k0	–1.0x	0.0	55k
49k2	–1.5x	3.5	44k
35k1	–2.3x	7.2	33k
27k3	–2.5x	8.0	31k
20k5	–3.0x	9.5	28k
15k4	–3.5x	10.9	24k
11k5	–4.0x	12.0	22k
9k09	–5.0x	14.0	18k
7k50	–5.6x	15.0	17k
6k19	–6.4x	16.1	15k
5k11	–8.3x	18.4	12k
3k90	–10x	20.0	10k

Internal Under Voltage Detection

The TPA6139A2 contains an internal precision band gap reference voltage and a comparator used to monitor the supply voltage, VDD. The internal VDD monitor is set at 2.8V with 200mV hysteresis.



Input-Blocking Capacitors

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the TPA6139A2. These capacitors block the dc portion of the audio source and allow the TPA6139A2 inputs to be properly biased to provide maximum performance. The input blocking capacitors also limit the DC gain to 1, limiting the DC-offset voltage at the output.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 1. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1. Then the frequency and/or capacitance can be determined when one of the two values is given.

$$fc_{IN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad \text{or} \quad C_{IN} = \frac{1}{2\pi fc_{IN} R_{IN}} \tag{1}$$

For a fixed cutoff frequency of 2Hz the size of the input capacitance is shown in the table below with the capacitors rounded up to nearest E6 values. For 20Hz cutoff simply divide the capacitor values with 10; e.g., for 1x gain, 150nF is needed.

Table 2. Input Capacitor for Different Gain and Cutoff

Gain_set RESISTOR	GAIN	Gain (dB)	INPUT RESISTANCE	2 Hz Cutoff
249k	–2.0x	6.0	37k	2.2 µF
82k0	–1.0x	0.0	55k	1.5 µF
49k2	–1.5x	3.5	44k	2.2 µF
35k1	–2.3x	7.2	33k	3.3 µF
27k3	–2.5x	8.0	31k	3.3 µF
20k5	–3.0x	9.5	28k	3.3 µF
15k4	–3.5x	10.9	24k	3.3 µF
11k5	–4.0x	12.0	22k	4.7 µF
9k09	–5.0x	14.0	18k	4.7 µF
7k50	–5.6x	15.0	17k	4.7 µF
6k19	–6.4x	16.1	15k	6.8 µF
5k11	–8.3x	18.4	12k	6.8 µF
3k90	–10x	20.0	10k	10 µF

Pop-Free Power Up

Pop-free power up is ensured by keeping the $\overline{\text{MUTE}}$ low during power supply ramp up and down. The pin should be kept low until the input AC-coupling capacitors are fully charged before asserting the $\overline{\text{MUTE}}$ pin high to pre-charge the ac-coupling; and, pop-less power-up is achieved. Figure 10 illustrates the preferred sequence.

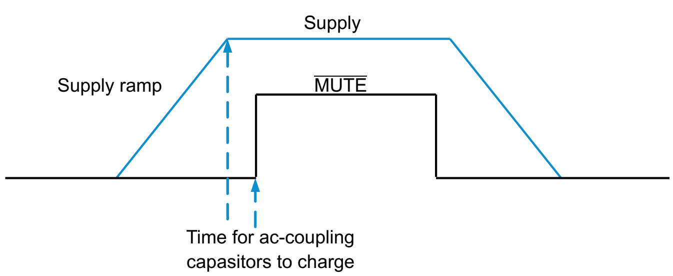


Figure 10. Power-Up Sequence

CAPACITIVE LOAD

The TPA6139A2 has the ability to drive a high capacitive load up to 220 pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47 Ω or larger for the line driver output.

LAYOUT RECOMMENDATIONS

A proposed layout for the TPA6139A2 can be seen in the TPA6139A2EVM User's Guide (SLOU248), and the Gerber files can be downloaded from http://focus.ti.com/docs/toolsw/folders/print/TPA6139A2evm.html. To access this information, open the TPA6139A2 product folder and look in the Tools and Software folder.

Ground traces are recommended to be routed as a star ground to minimize hum interference. VDD, VSS decoupling capacitors and the charge pump capacitors should be connected with short traces.

PIN COMPATIBLE WITH THE DRV612

The TPA6139A2 stereo Headphone amplifier is pin compatible with the DRV612 . A single PCB layout can therefore be used with stuffing options for different board configurations.

APPLICATION CIRCUIT

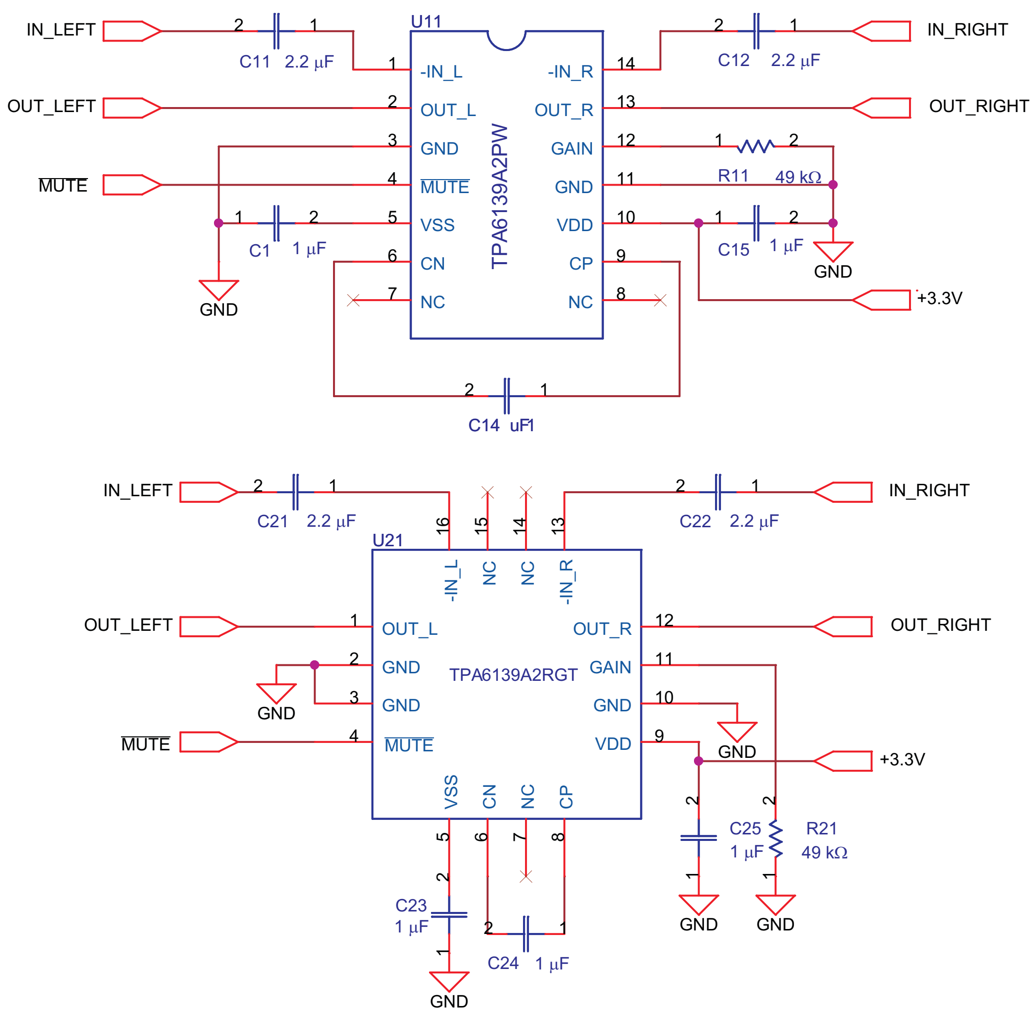


Figure 11. Single Ended Input and Output, Gain Set to –1.5x

REVISION HISTORY

NOTE: Page numbers in current version may differ from previous versions.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6139A2PW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6139
TPA6139A2PW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6139
TPA6139A2PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6139
TPA6139A2PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6139
TPA6139A2RGTR	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T6139
TPA6139A2RGTR.A	Active	Production	VQFN (RGT) | 16	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T6139
TPA6139A2RGTT	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T6139
TPA6139A2RGTT.A	Active	Production	VQFN (RGT) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T6139

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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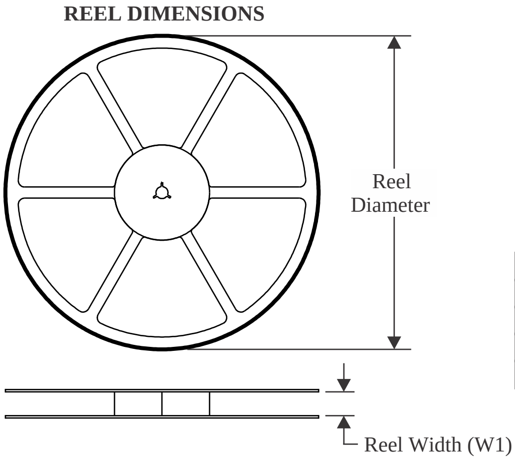
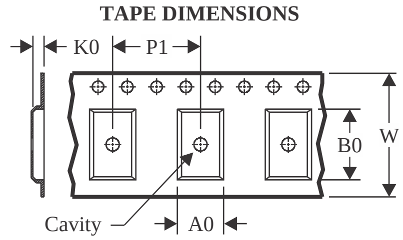
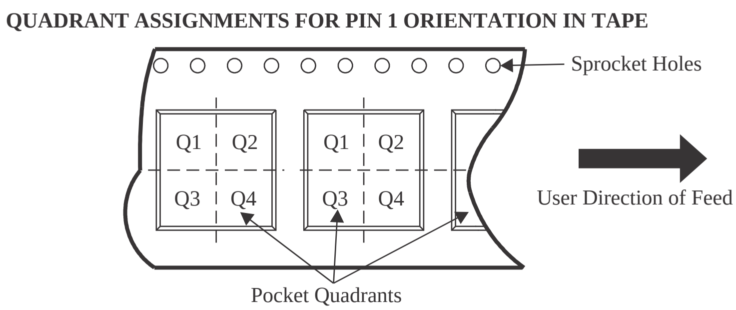
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





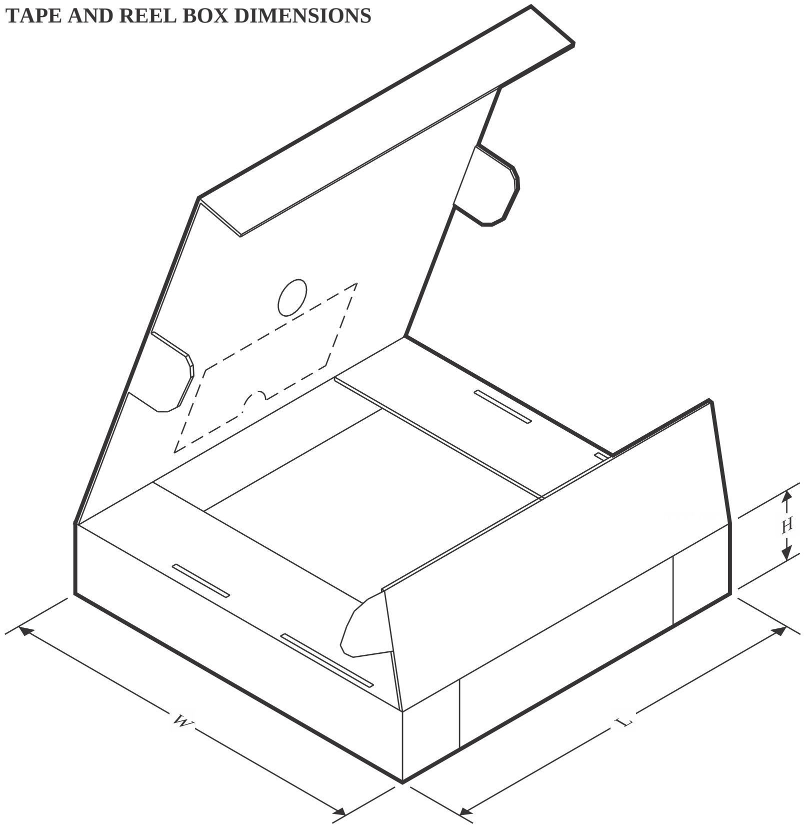
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6139A2PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

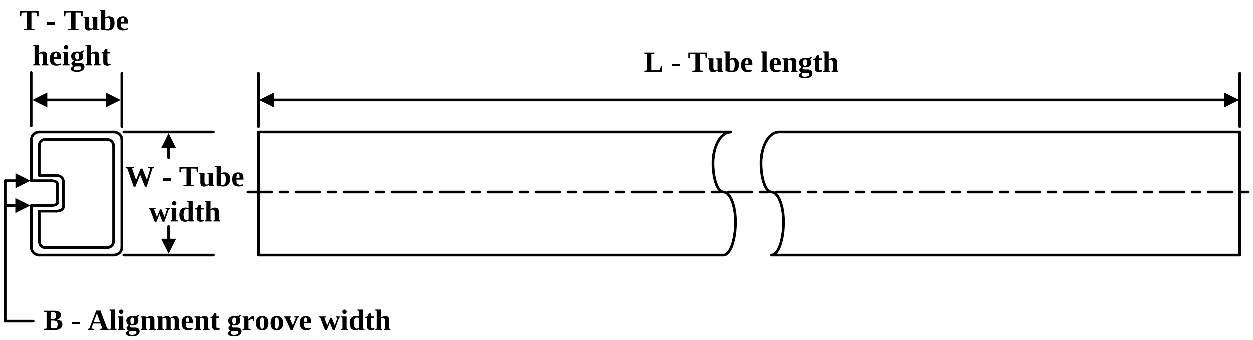
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6139A2PWR	TSSOP	PW	14	2000	350.0	350.0	43.0

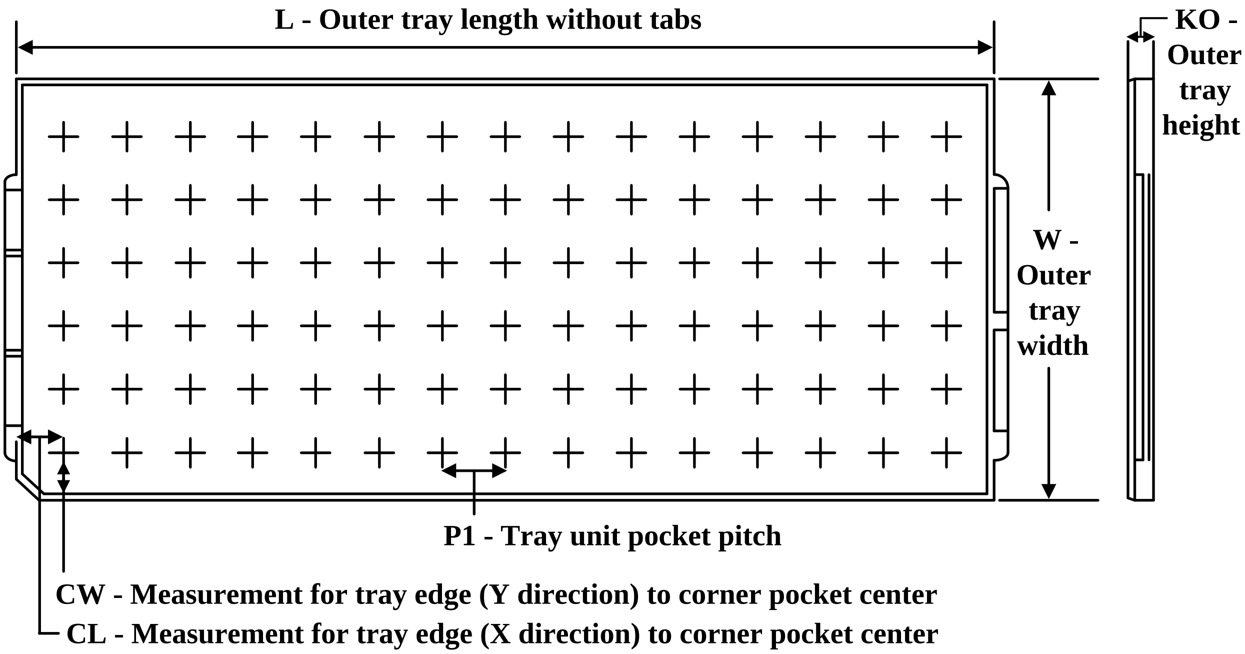
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA6139A2PW	PW	TSSOP	14	90	530	10.2	3600	3.5
TPA6139A2PW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

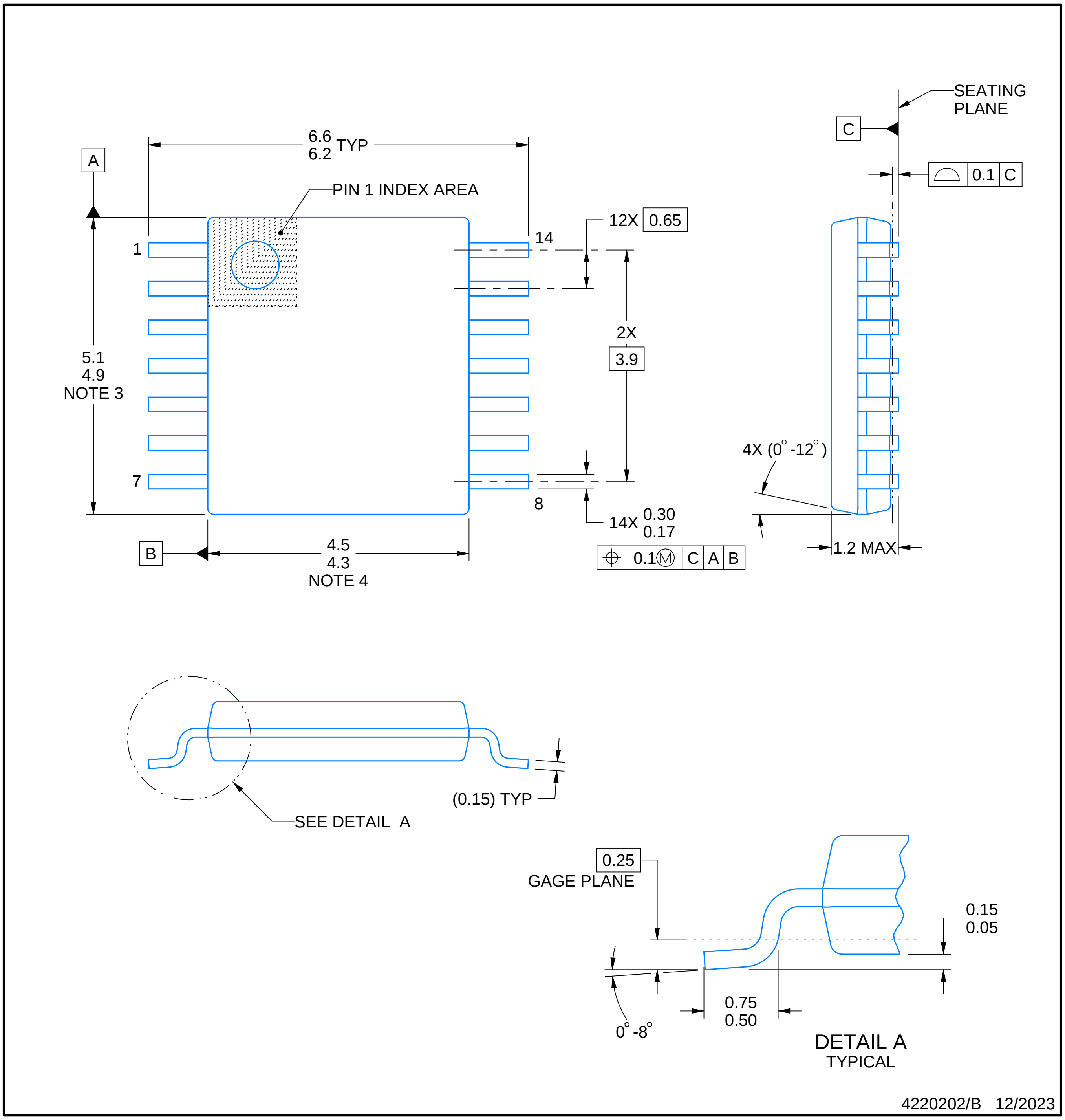
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

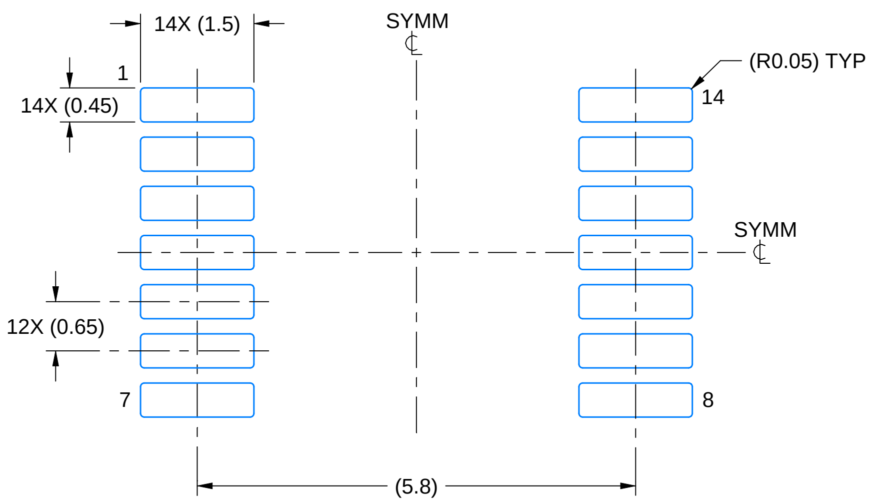
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPA6139A2RGTR	RGT	VQFN	16	3000	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
TPA6139A2RGTR.A	RGT	VQFN	16	3000	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
TPA6139A2RGTT	RGT	VQFN	16	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15
TPA6139A2RGTT.A	RGT	VQFN	16	250	35 X 14	150	315	135.9	7620	8.8	7.9	8.15

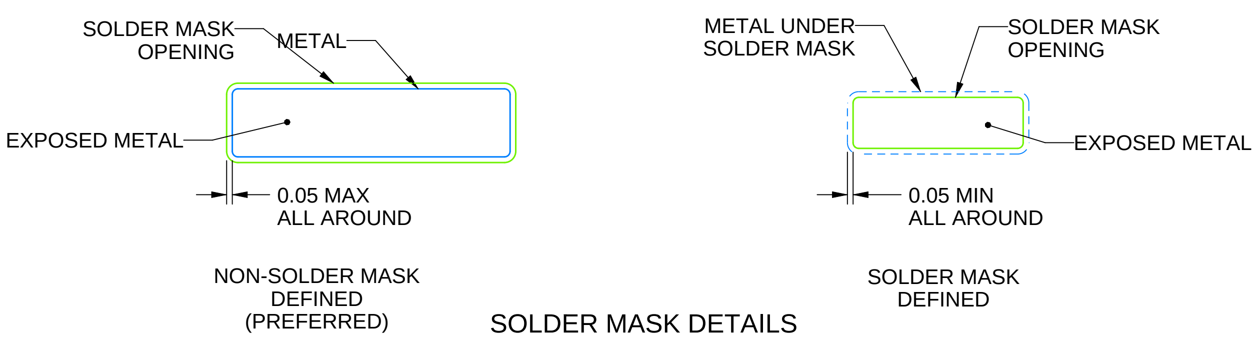


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

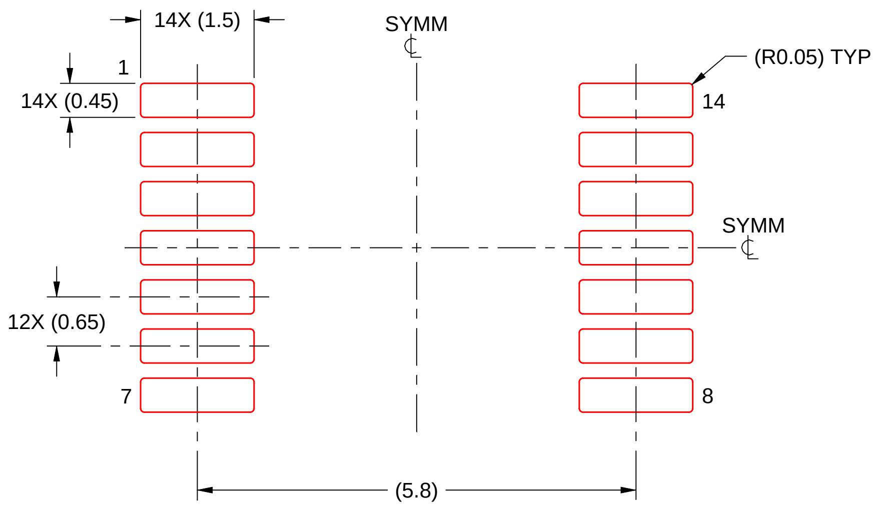


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

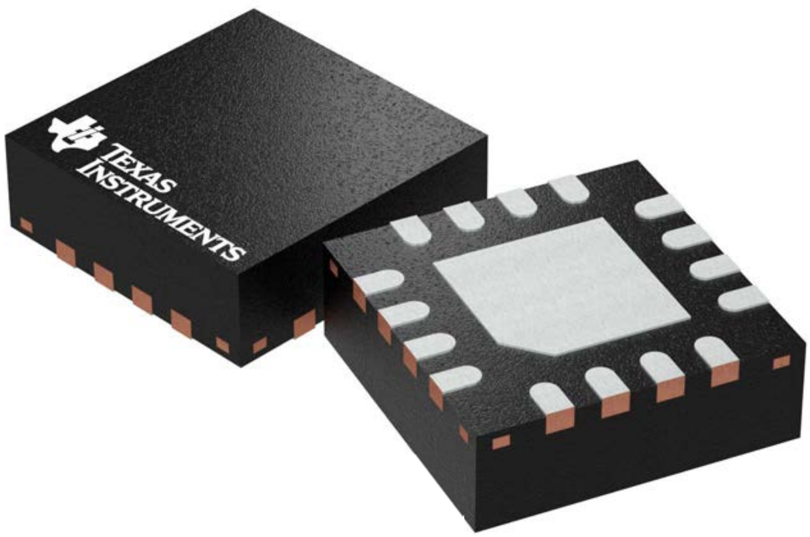


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

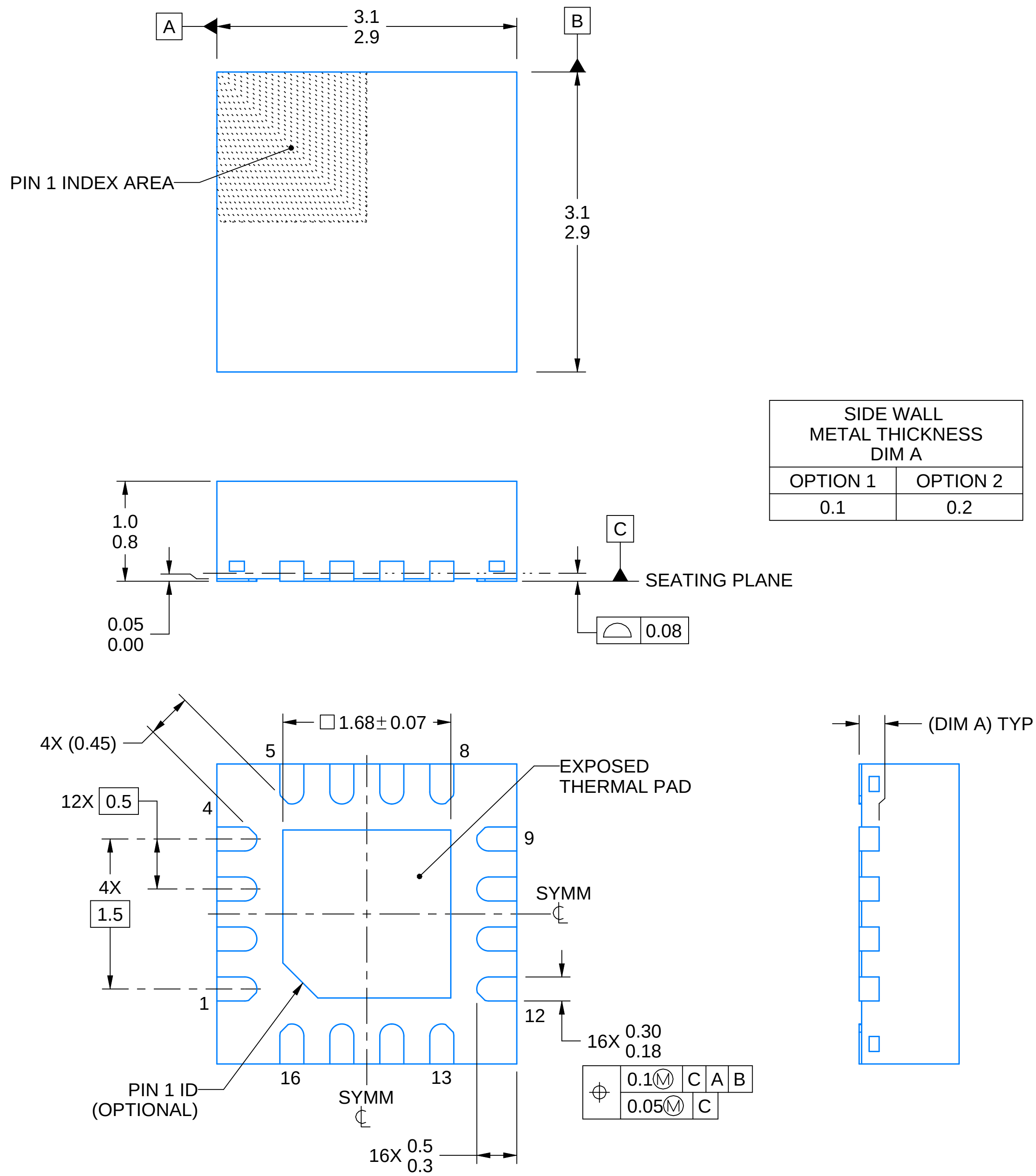
4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

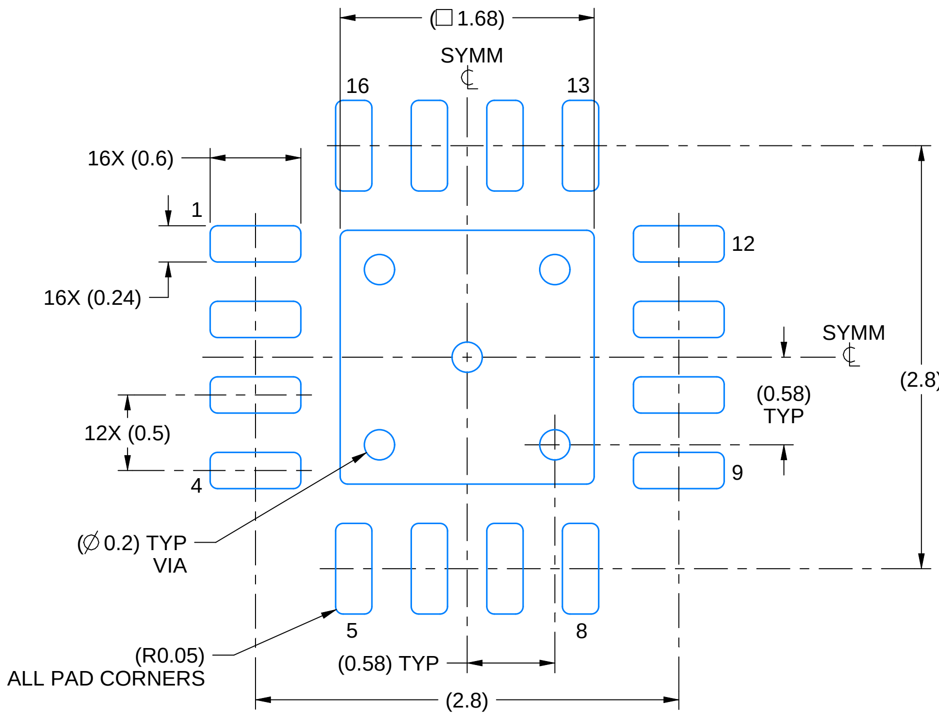


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

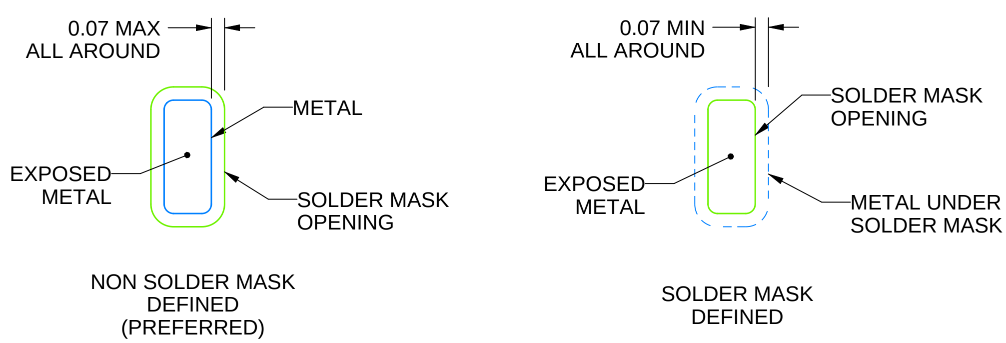
4222419/E 07/2025

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

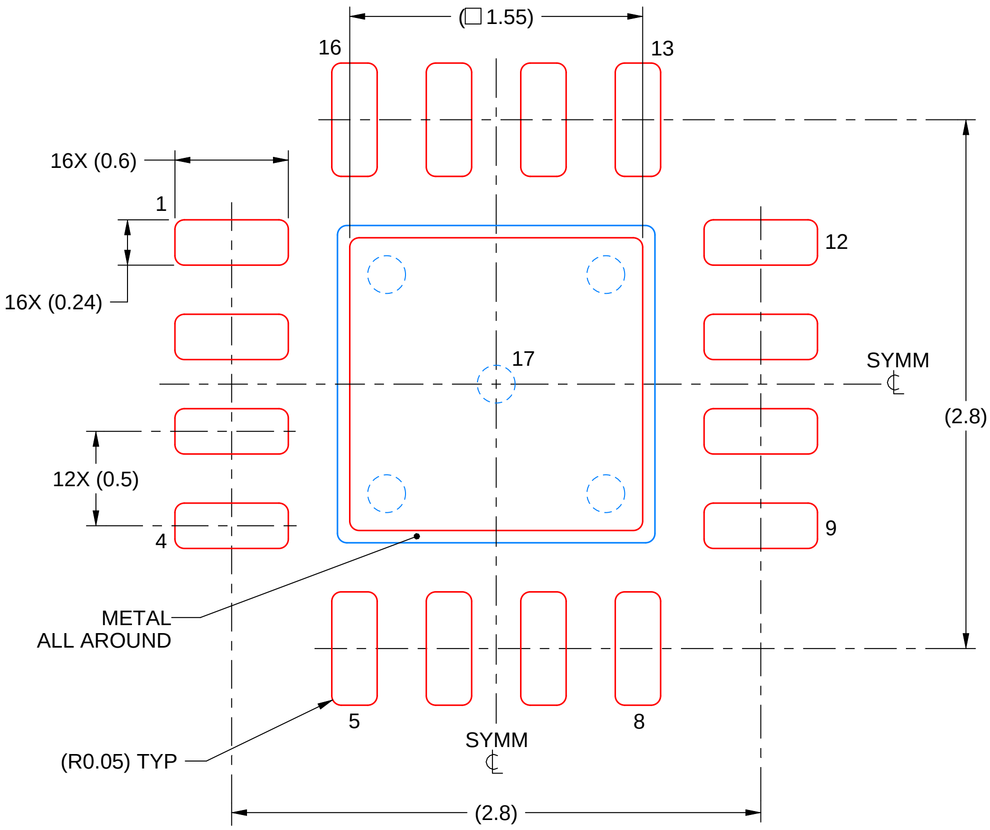


SOLDER MASK DETAILS

4222419/E 07/2025

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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