具有可调节增益的 DirectPath™ 头戴式耳机驱动器

查询样品：TPA6138A2

特性

- 立体声 **DirectPath™**头戴式耳机放大器
  - 采用 **3.3V** 电源时，可向 **32Ω** 负载输送 **40mW** 功率
- 低 **THD+N**：**< 0.01%**（在向 **32Ω** 负载输送 **10mW** 功率时）
- 高**SNR**，**>90dB**
- 差分输入和单端输出
- 可利用外部增益设定电阻器来调节增益
- 可配置成一个二阶低通滤波器
  - 非常适合于 **PWM** 音源
- 低 **DC** 失调，**<1mV**
- 接地参考输出免除了隔直流电容器
  - 缩减了板级空间
  - 降低了组件成本
  - 改善了**THD+N** 性能
  - 未出现因输出电容器所导致的低频响应性能下降
- 具短路保护功能
- 喀哒声和噼啪声抑制电路
- 外部欠压静音
- 用于实现无噼啪声音频接通**/**关断控制的有源静音控制功能
- 节省空间的 **TSSOP** 封装

应用

- **LCD** 及 **PDP TV**
- **Blu-ray Disc™DVD** 播放机
- 机顶盒
- 迷你型**/**微型组合音响系统
- 声卡
- 笔记本电脑

说明

TPA6138A2 是一款无噼啪声立体声头戴式耳机放大器，专为允许去除输出隔直流电容器以达到减少组件数量及成本之目的而设计。 对于那些将尺寸和成本作为关键设计参数的单电源电子产品而言，该器件是理想的选择。

TPA6138A2 的设计运用了 TI 的 DirectPath™ 专利技术，能够在采用 3.3V 电源电压的条件下向一个 32Ω 负载输送 25mW 的驱动功率。 这款器件具有差分输入并采用外部增益设定电阻器，可支持 ±1 V/V 至 ±10 V/V 的增益范围。可为每个通道个别地配置增益。 另外，此器件也可以配置成一个二阶低通滤波器，且非常适合与 PWM 音源相连。 音频输出符合 ±8kV IEC ESD 保护规格，因而只需要使用一个简单的电阻器－电容器 ESD 保护电路即可。 TPA6138A2 具有内置的有源静音控制功能电路，用于实现无噼啪声的音频接通/关断控制。 TPA6138A2 具有一个外部欠压检测器，该欠压检测器在电源被拿掉时使输出静音，从而确保了无噼啪声的关断操作。

与传统的头戴式耳机放大器相比，在音频产品中使用 TPA6138A2 能够大幅度地减少组件数量。 TPA6138A2 不需要分离轨电源或隔直流电容器。 TPA6138A2 集成了其自己的充电泵以产生一个负电源轨，可提供一个干净、无噼啪声的接地偏置音频信号。

TPA6138A2 采用 14 引脚 TSSOP 封装。

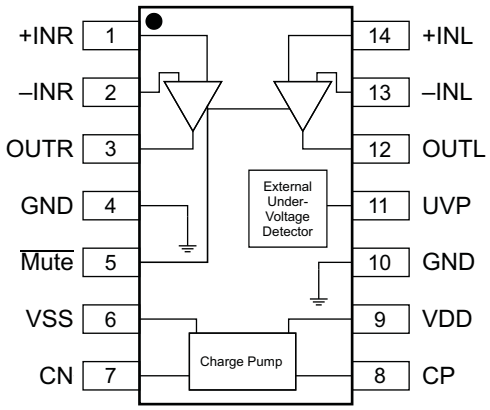
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TERMINAL ASSIGNMENT

The TPA6138A2 is available in the TSSOP package:

- 14-pin TSSOP package (PW)

PW PACKAGE
(TOP VIEW)

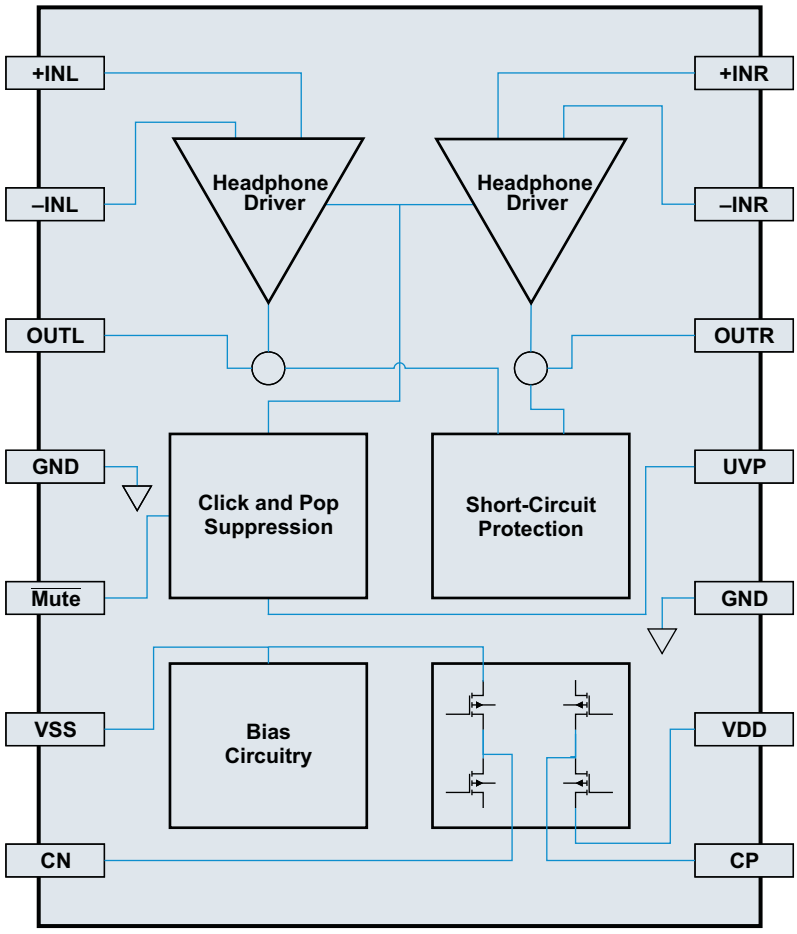


PIN FUNCTIONS

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
CN	7	I/O	Charge-pump flying capacitor negative connection
CP	8	I/O	Charge-pump flying capacitor positive connection
GND	4, 10	P	Ground
–INL	13	I	Left-channel OPAMP negative input
+INL	14	I	Left-channel OPAMP positive input
–INR	2	I	Right-channel OPAMP negative input
+INR	1	I	Right-channel OPAMP positive input
$\overline{\text{Mute}}$	5	I	Mute, active-low
OUTL	12	O	Left-channel OPAMP output
OUTR	3	O	Right-channel OPAMP output
UVP	11	I	Undervoltage protection; internal pull-up, unconnected if UVP function is unused.
VDD	9	P	Positive supply
VSS	6	P	Supply voltage

(1) I = input, O = output, P = power

SYSTEM BLOCK DIAGRAM



ORDERING INFORMATION(1)

T_A	PACKAGE	DESCRIPTION
–40°C to 85°C	TPA6138A2PW	14-Pin

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	VALUE	UNIT
V_{DD} to GND	–0.3 to 4	V
Input voltage, V_I	V_{SS} – 0.3 to V_{DD} + 0.3	V
Minimum load impedance – line outputs – OUTL, OUTR	12.8	Ω
$\overline{\text{Mute}}$ to GND, UVP to GND	–0.3 to V_{DD} +0.3	V
Maximum operating junction temperature range, T_J	–40 to 150	°C
Storage temperature range, T_{stg}	–40 to 150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC(1)		TPA6138A2 PW 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	130	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	49	
θ_{JB}	Junction-to-board thermal resistance	63	
ψ_{JT}	Junction-to-top characterization parameter	3.6	
ψ_{JB}	Junction-to-board characterization parameter	62	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{DD}	Power supply	DC supply voltage	3	3.3	3.6	V
R_L	Load impedance		16	32		Ω
V_{IL}	Low-level input voltage	$\overline{\text{Mute}}$		40		%VDD
V_{IH}	High-level input voltage	$\overline{\text{Mute}}$		60		%VDD
T_A	Ambient temperature		–40	25	85	°C

ELECTRICAL CHARACTERISTICS

V_{DD} = 3.3 V, R_{DL} = 32 Ω, R_{fb} = 30 kΩ, R_{IN} = 15 kΩ, T_A = 25°C, Charge pump: C_P = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage	V_{DD} = 3.3 V		0.5	1	mV
PSRR	Power-supply rejection ratio			80		dB
V_{OH}	High-level output voltage	V_{DD} = 3.3 V	3.1			V
V_{OL}	Low-level output voltage	V_{DD} = 3.3 V			–3.05	V
V_{UVP_EX}	External UVP detect voltage			1.25		V
$V_{UVP\_EX\_HYSTERESIS}$	External UVP detect hysteresis current			5		µA
f_{CP}	Charge-pump switching frequency		200	300	400	kHz
$\|I_{IH}\|$	High-level input current, $\overline{\text{Mute}}$	V_{DD} = 3.3 V, V_{IH} = V_{DD}			1	µA
$\|I_{IL}\|$	Low-level input current, $\overline{\text{Mute}}$	V_{DD} = 3.3 V, V_{IL} = 0 V			1	µA
I_{DD}	Supply current	V_{DD} = 3.3 V, no load, $\overline{\text{Mute}}$ = V_{DD}, no load	5	14	25	mA
		V_{DD} = 3.3 V, no load, $\overline{\text{Mute}}$ = GND, disabled		14		

OPERATING CHARACTERISTICS

V_{DD} = 3.3 V, R_{DL} = 32 Ω, R_{fb} = 30 kΩ, R_{IN} = 15 kΩ, T_A = 25°C, Charge pump: C_P = 1 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Output power, outputs in phase	THD+N = 1%, V_{DD} = 3.3 V, f = 1 kHz, R_L = 32 Ω		40		mW
THD+N	Total harmonic distortion plus noise	V_{DD} = 3.3V, f = 1kHz, R_{LD} = 32Ω, Po = 10mW		0.01%		
SNR	Signal-to-noise ratio (1)	A-weighted	90	96		dB
DNR	Dynamic range (2)	A-weighted	90	100		dB
V_N	Noise voltage	A-weighted		13		µV
Z_O	Output Impedance when muted	$\overline{\text{Mute}}$ = GND		110		mΩ
	Input-to-output attenuation when muted	$\overline{\text{Mute}}$ = GND		80		dB
	Crosstalk—L to R, R to L	Po = 20 mW		–75		dB
I_{LIMIT}	Current limit	PVDD = 3.3 V		50		mA

(1) SNR is calculated relative to 25-mW output.
(2) DNR is calculated relative to output at 1% THD+N.

TYPICAL CHARACTERISTICS

VDD = 3.3 V , T_A = 25°C, C(PUMP) = C(VSS) = 1 µF , C_{IN} = 2.2 µF, R_{IN} = 15 kΩ, R_{fb} = 30 kΩ, R_{OUT} = 10 Ω, C_{OUT} = 1 nF (unless otherwise noted)

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER
V_{DD} = 3.3 V, R_L = 32 Ω

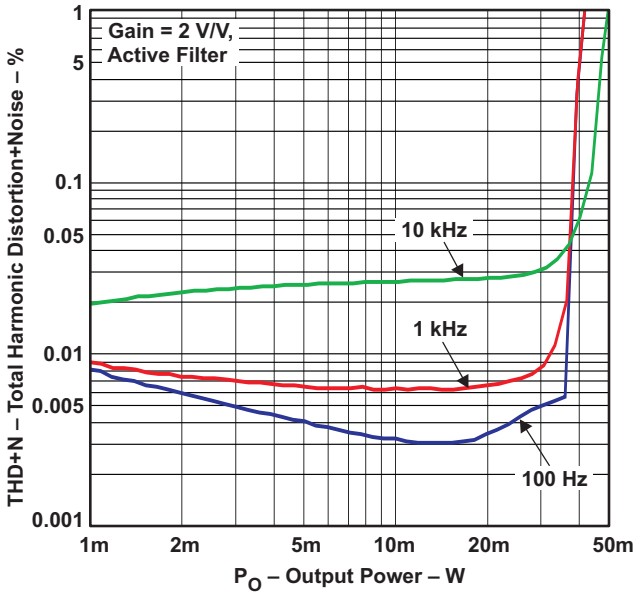


Figure 1.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT VOLTAGE
V_{DD} = 3.3 V, R_L = 16 Ω

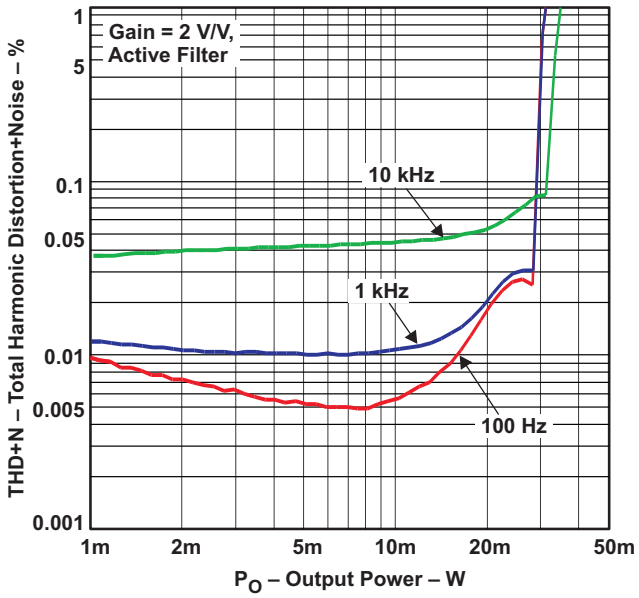


Figure 2.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY
V_{DD} = 3.3 V, R_L = 32 Ω

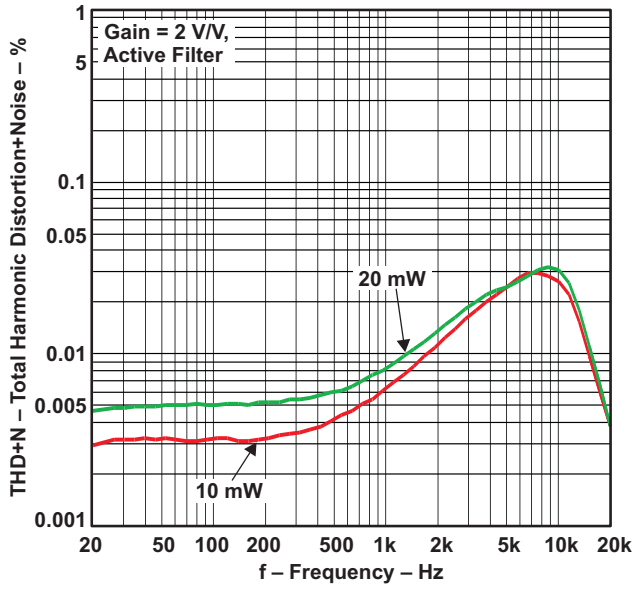


Figure 3.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY
V_{DD} = 3.3 V, R_L = 16 Ω

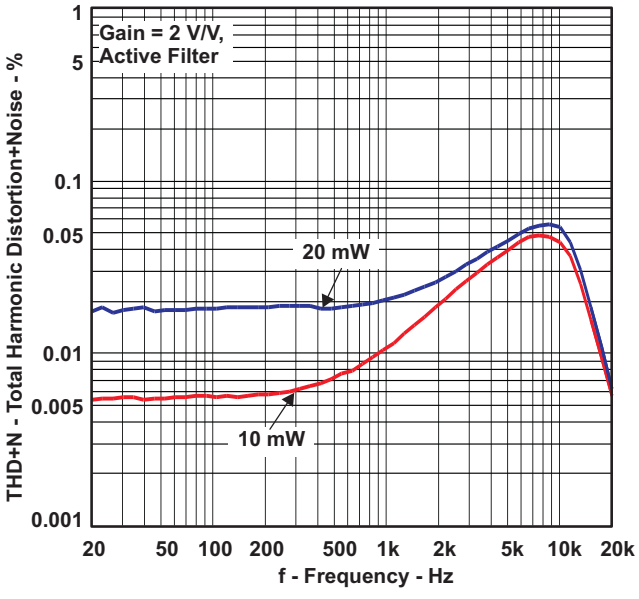


Figure 4.

TYPICAL CHARACTERISTICS (continued)

VDD = 3.3 V , T_A = 25°C, C(PUMP) = C(VSS) = 1 µF , C_{IN} = 2.2 µF, R_{IN} = 15 kΩ, R_{fb} = 30 kΩ, R_{OUT} = 10 Ω, C_{OUT} = 1 nF (unless otherwise noted)

CROSSTALK vs FREQUENCY

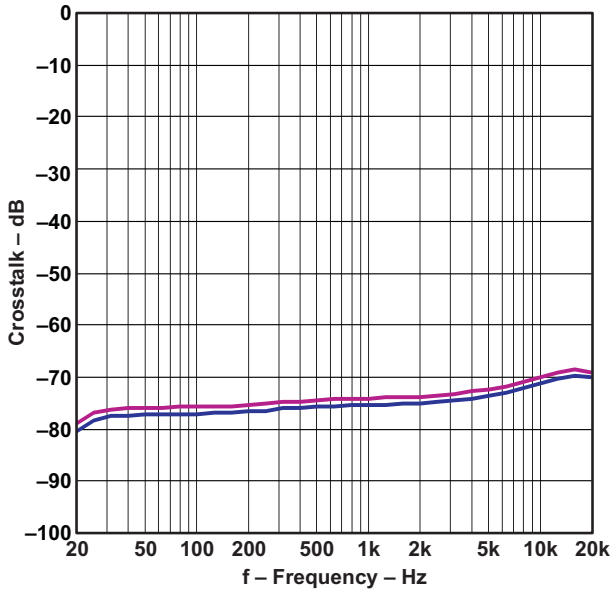


Figure 5.

SUPPLY REJECTION RATIO vs FREQUENCY Gain = 6dB, V_{ripple} = 200 mVpp

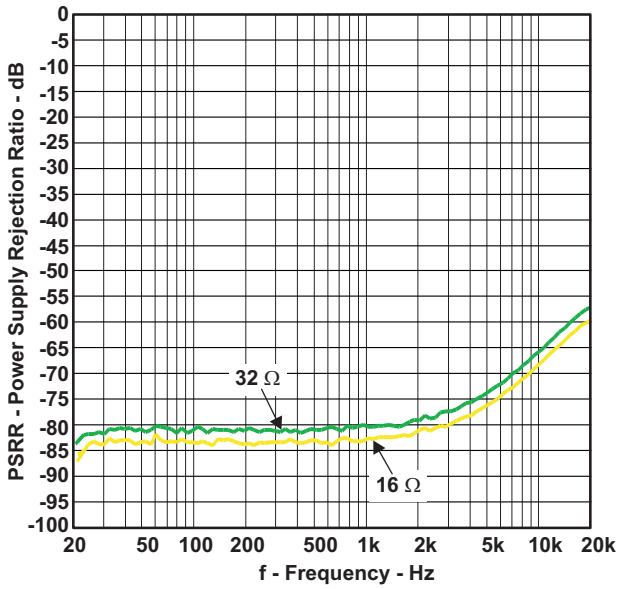


Figure 6.

APPLICATION INFORMATION

Single-supply line-driver amplifiers typically require dc-blocking capacitors. The top drawing in Figure 7 illustrates the conventional line-driver-amplifier connection to the load and output signal. DC blocking capacitors are often large in value. The headphone load (typical resistive values of 16 Ω to 32 Ω) combine with the dc blocking capacitors to form a high-pass filter. Equation 1 shows the relationship between the load impedance (R_L), the capacitor (C_O), and the cutoff frequency (f_C).

$$f_c = \frac{1}{2\pi R_L C_O} \tag{1}$$

C_O can be determined using Equation 2, where the load impedance and the cutoff frequency are known.

$$C_O = \frac{1}{2\pi R_L f_c} \tag{2}$$

If f_C is low, the capacitor must then have a large value because the load resistance is small. Large capacitance values require large package sizes. Large package sizes consume PCB area, stand high above the PCB, increase cost of assembly, and can reduce the fidelity of the audio output signal.

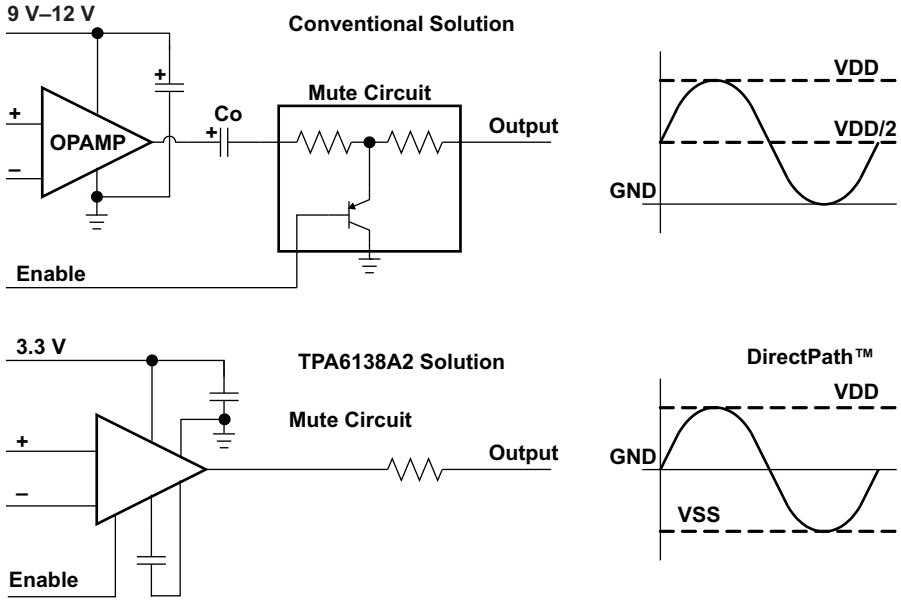


Figure 7. Conventional and DirectPath Line Driver

The DirectPath amplifier architecture operates from a single supply but makes use of an internal charge pump to provide a negative voltage rail. Combining the user-provided positive rail and the negative rail generated by the IC, the device operates in what is effectively a split-supply mode. The output voltages are now centered at zero volts with the capability to swing to the positive rail or negative rail. The DirectPath amplifier requires no output dc-blocking capacitors. The bottom block diagram and waveform of Figure 7 illustrate the ground-referenced line-driver architecture. This is the architecture of the TPA6138A2.

CHARGE-PUMP FLYING CAPACITOR AND VSS CAPACITOR

The charge-pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The VSS capacitor must be at least equal to the charge-pump capacitor in order to allow maximum charge transfer. Low-ESR capacitors are an ideal selection, and a value of 1 µF is typical. Capacitor values that are smaller than 1 µF can be used, but the maximum output voltage may be reduced, and the device may not operate to specifications. If the TPA6138A2 is used in highly noise-sensitive circuits, it is recommended to add a small LC filter on the V_{DD} connection.

DECOUPLING CAPACITORS

The TPA6138A2 is a DirectPath headphone amplifier that requires adequate power-supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF, placed as close as possible to the device V_{DD} lead works best. Placing this decoupling capacitor close to the TPA6138A2 is important for the performance of the amplifier. For filtering lower-frequency noise signals, a 10-µF or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

GAIN-SETTING RESISTOR RANGES

The gain-setting resistors, R_{IN} and R_{fb}, must be chosen so that noise, stability, and input capacitor size of the TPA6138A2 are kept within acceptable limits. Voltage gain is defined as R_{fb} divided by R_{IN}.

Selecting values that are too low demands a large input ac-coupling capacitor, C_{IN}. Selecting values that are too high increases the noise of the amplifier. Table 1 lists the recommended resistor values for different inverting-input gain settings.

Table 1. Recommended Resistor Values

GAIN	INPUT RESISTOR VALUE, R_{IN}	FEEDBACK RESISTOR VALUE, R_{fb}
–1 V/V	10 kΩ	10 kΩ
–1.5 V/V	8.2 kΩ	12 kΩ
–2 V/V	15 kΩ	30 kΩ
–10 V/V	4.7 kΩ	47 kΩ

USING THE TPA6138A2 AS A SECOND-ORDER FILTER

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the TPA6138A2, as it can be used like a standard OPAMP. Several filter topologies can be implemented, both single-ended and differential. In Figure 8, a multi-feedback (MFB) topology with differential input and single-ended input is shown.

An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc gain to 1, helping to reduce the output dc offset to a minimum.

The component values can be calculated with the help of the TI FilterPro™ program available on the TI Web site at:

http://focus.ti.com/docs/toolsw/folders/print/filterpro.html.

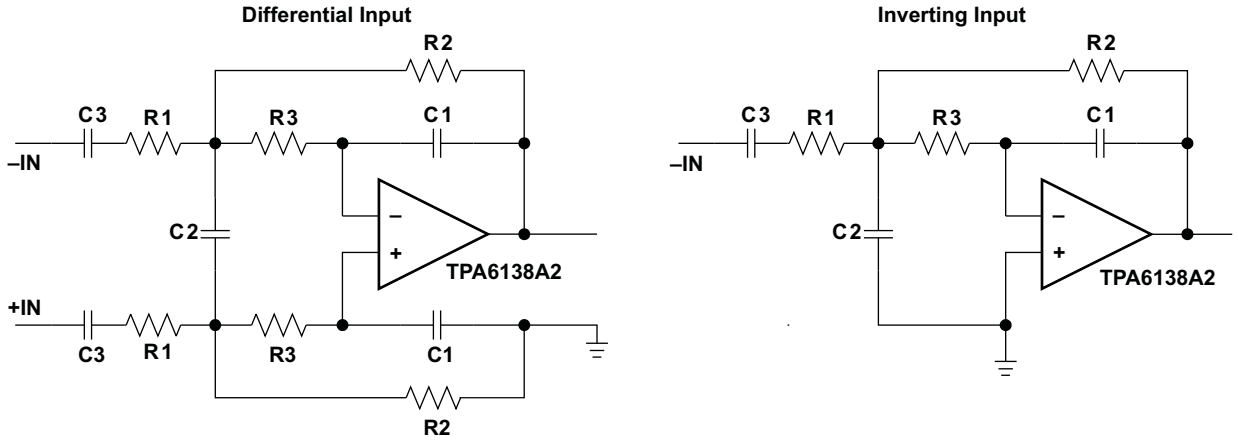


Figure 8. Second-Order Active Low-Pass Filter

The resistor values should have a low value for obtaining low noise, but should also have a high enough value to allow use of a small-size ac-coupling capacitor. With the proposed values of 15 kΩ, 30 kΩ, and 43 kΩ, a dynamic range (DYR) of 106 dB can be achieved with a 1-µF input ac-coupling capacitor.

INPUT-BLOCKING CAPACITORS

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of the TPA6138A2. These capacitors block the dc portion of the audio source and allow the TPA6138A2 inputs to be properly biased to provide maximum performance.

These capacitors form a high-pass filter with the input resistor, R_{IN}. The cutoff frequency is calculated using Equation 3. For this calculation, the capacitance used is the input-blocking capacitor and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.

It is recommended to use electrolytic capacitors or high-voltage-rated capacitors as input blocking capacitors to ensure minimal variation in capacitance with input voltages. Such variation in capacitance with input voltages is commonly seen in ceramic capacitors and can increase low-frequency audio distortion.

$$f_{cIN} = \frac{1}{2\pi R_{IN} C_{IN}} \quad or \quad C_{IN} = \frac{1}{2\pi f_{cIN} R_{IN}} \tag{3}$$

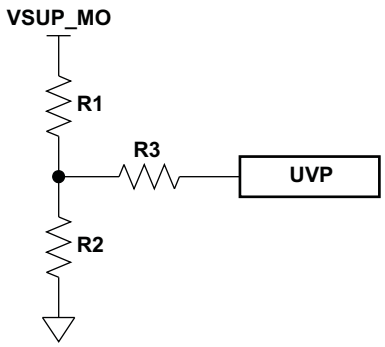
TPA6138A2 UVP OPERATION

The shutdown threshold at the UVP pin is 1.25 V. The customer must use a resistor divider to obtain the shutdown threshold and hysteresis desired for a particular application. The customer-selected thresholds can be determined as follows:

V_{UVP} = (1.25 – 6 µA × R3) × (R1 + R2) / R2

Hysteresis = 5 µA × R3 × (R1 + R2) / R2

For example, to obtain V_{UVP} = 3.8 V and 1-V hysteresis, we can use R1 = 3 kΩ, R2 = 1 kΩ and R3 = 50 kΩ.



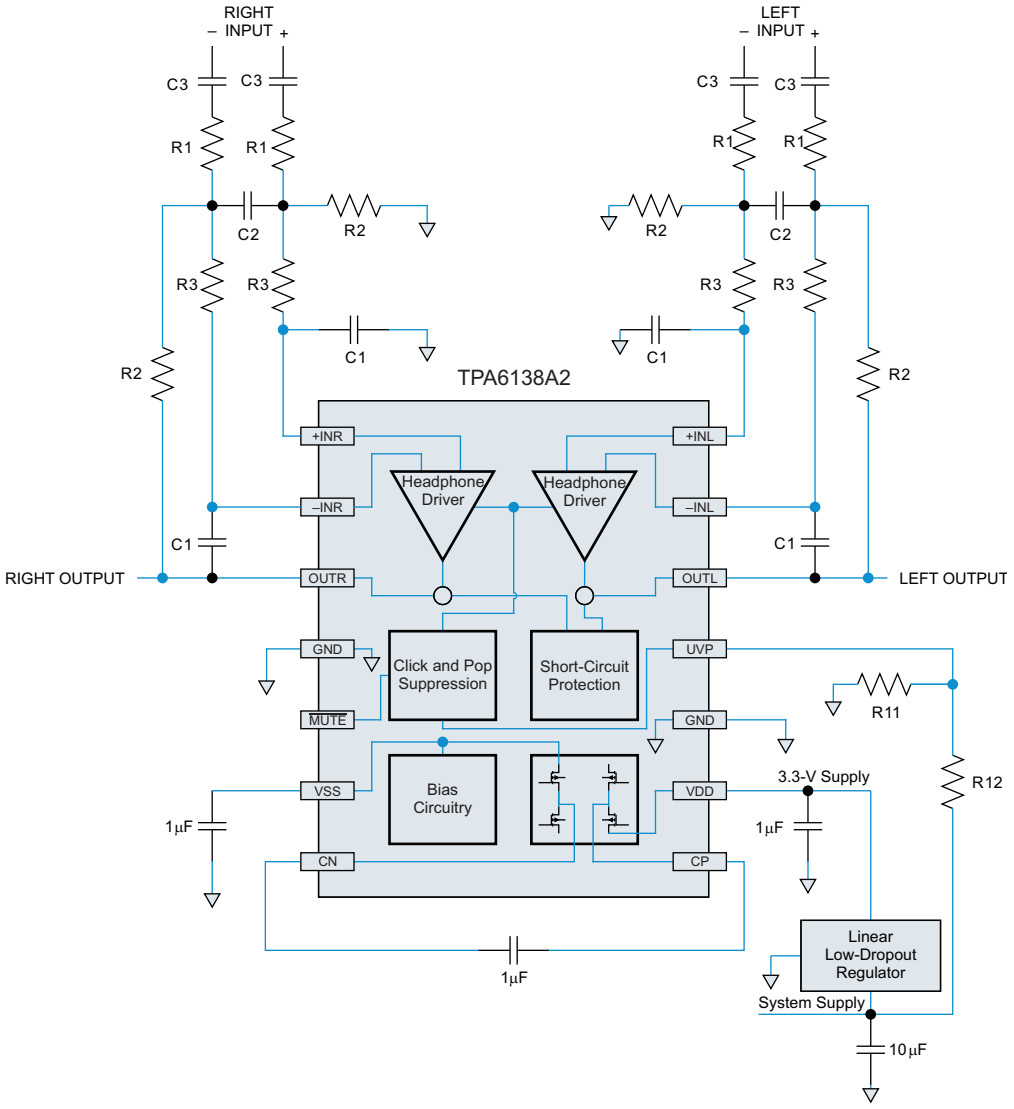
LAYOUT RECOMMENDATIONS

A proposed layout for the TPA6138A2 can be seen in the TPA6138A2EVM User's Guide, and the Gerber files can be downloaded from http://www.ti.com. To access this information, open the TPA6138A2 product folder and look in the Tools and Software folder.

GAIN-SETTING RESISTORS

The gain-setting resistors, R_{IN} and R_{fb}, must be placed close to pins 13 and 17, respectively, to minimize capacitive loading on these input pins and to ensure maximum stability of the TPA6138A2. For the recommended PCB layout, see the TPA6138A2EVM User's Guide.

APPLICATION CIRCUIT



R1 = 15 kΩ, R2 = 30 kΩ, R3 = 43 kΩ, C1 = 47 pF, C2 = 180 pF

REVISION HISTORY

Changes from Original (January 2011) to Revision A **Page**

- Added Rev A and May 2011 to Header, No other changes to page 1 1
- Changed Pin Functions Description for UVP pin from "connect to PVDD with a 10-kΩ resistor if function is unused" to "internal pull-up, unconnected if UVP function is unused". 2

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA6138A2PW	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6138
TPA6138A2PW.A	Active	Production	TSSOP (PW) | 14	90 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6138
TPA6138A2PWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6138
TPA6138A2PWR.A	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA6138

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

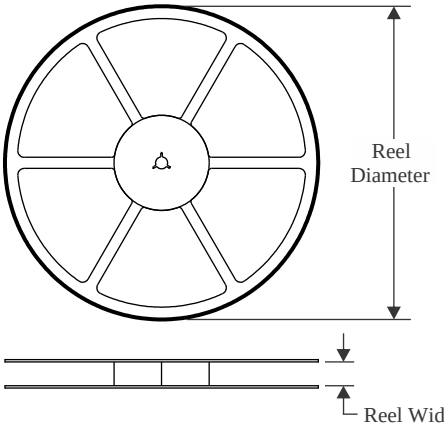
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

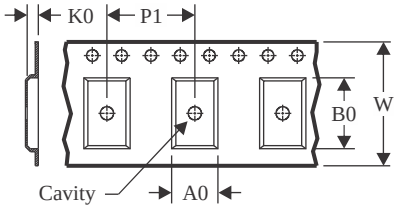
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

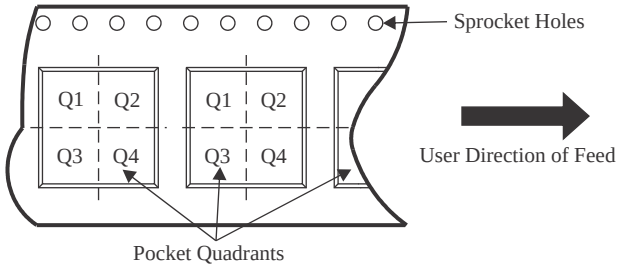


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

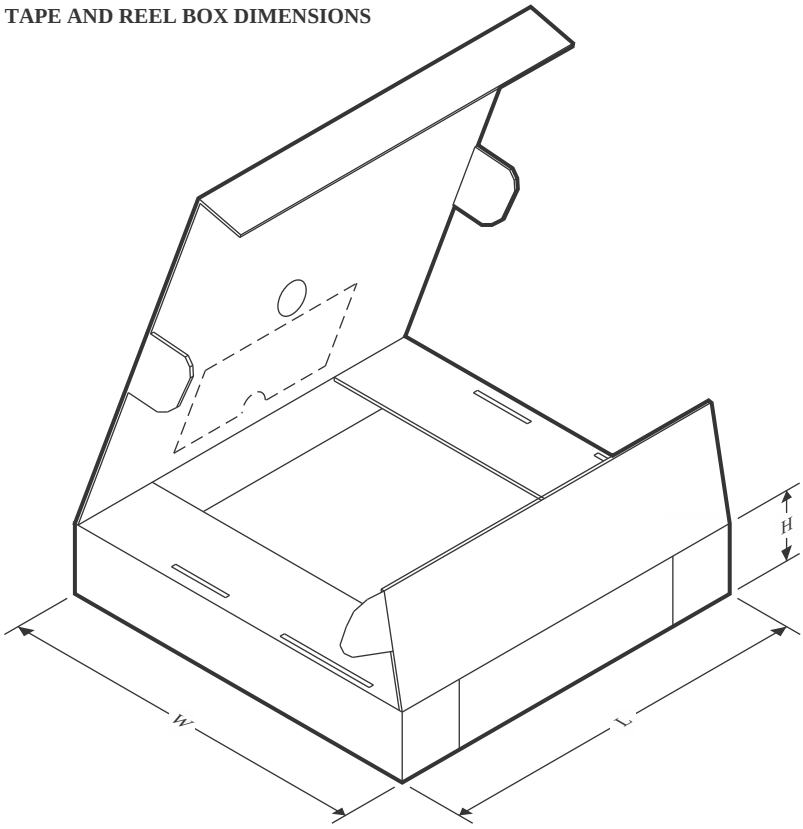
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6138A2PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

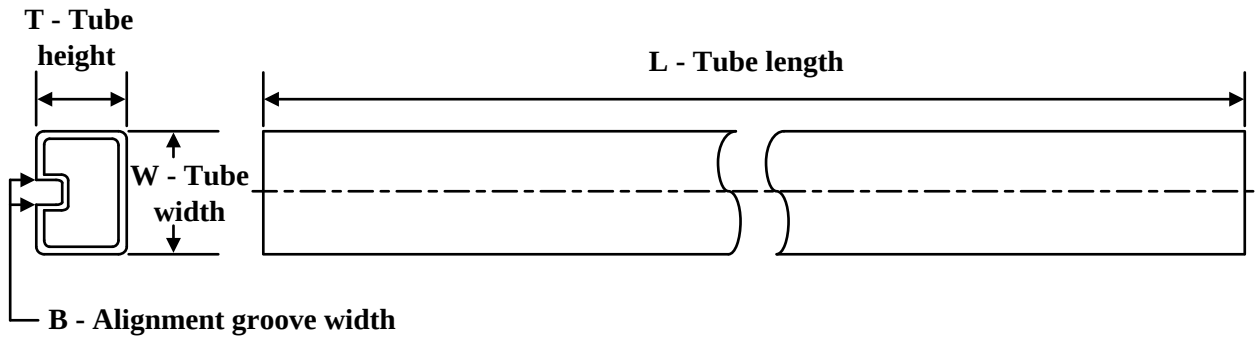
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6138A2PWR	TSSOP	PW	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

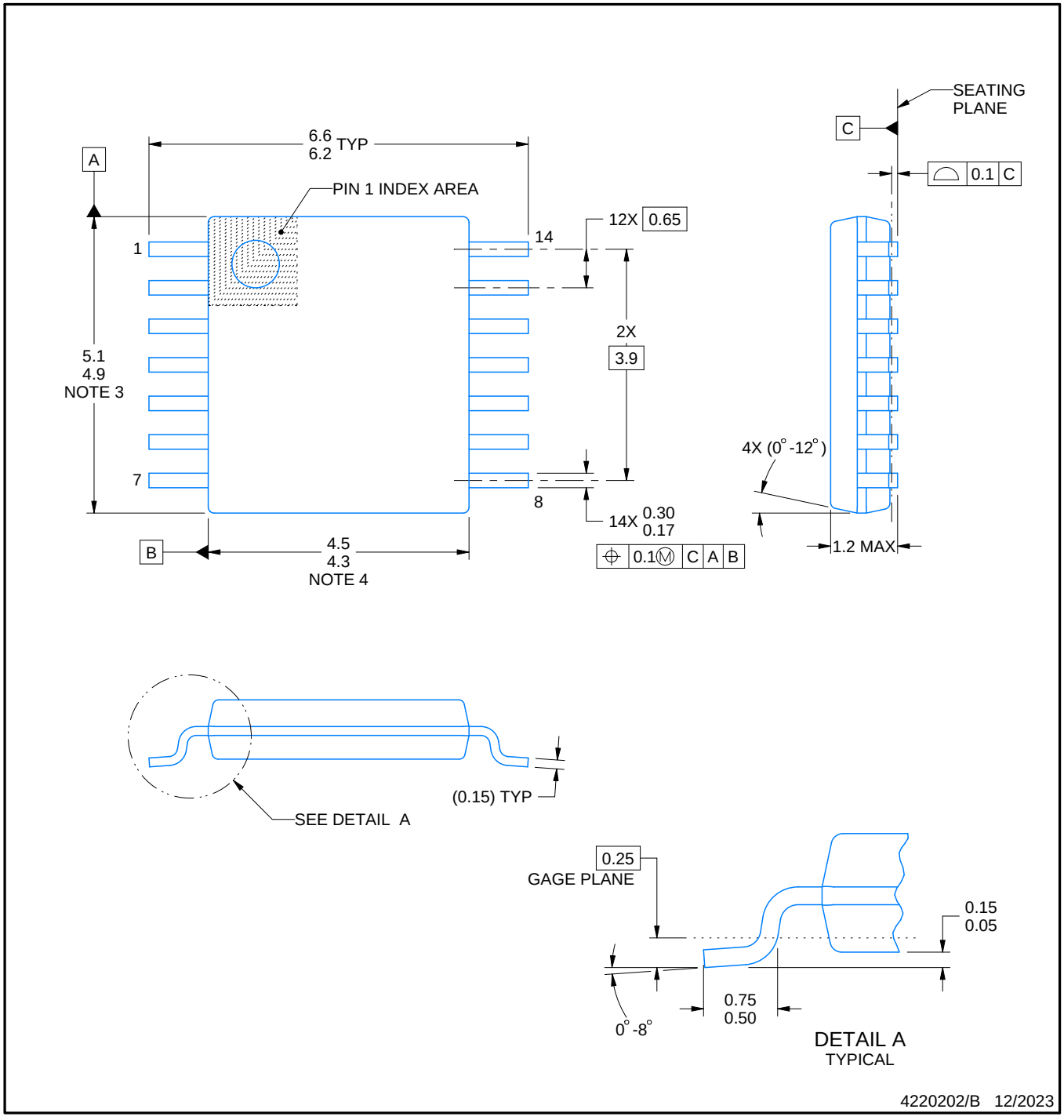
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA6138A2PW	PW	TSSOP	14	90	530	10.2	3600	3.5
TPA6138A2PW.A	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0014A

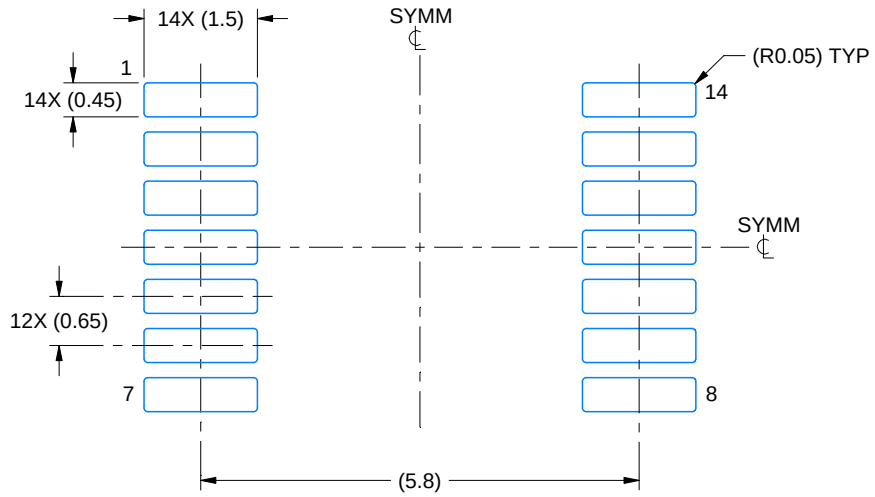
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

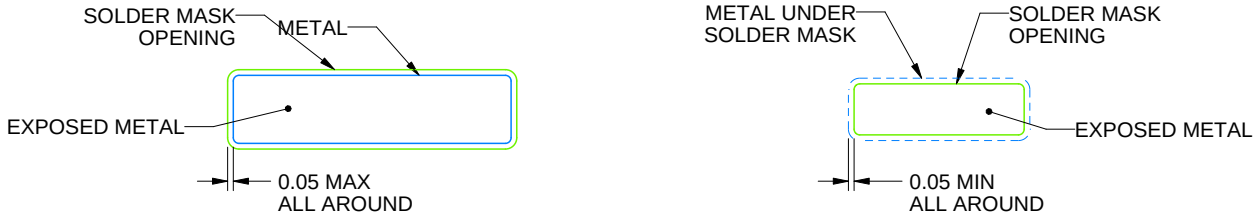


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

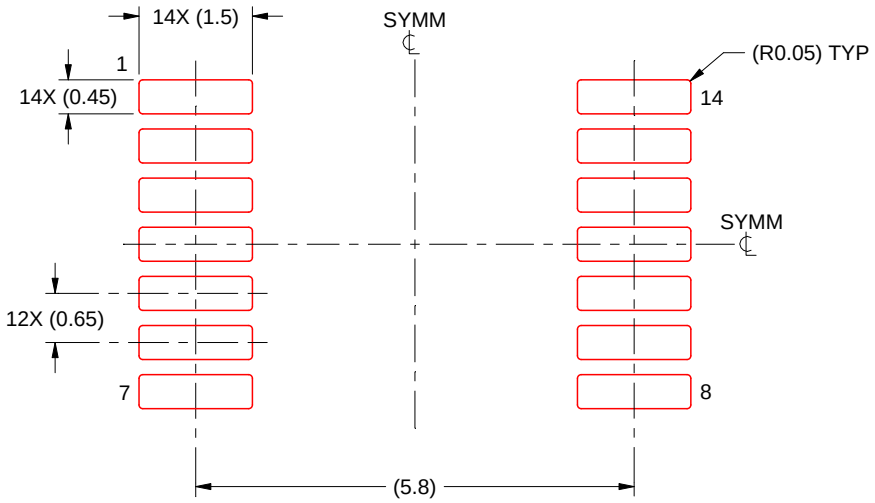


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

最后更新日期：2025 年 10 月