TPA3223 200W 立体声、400W 单声道 HD 模拟输入 D 类放大器

1 特性

- 10V 至 42V 宽电源电压范围
- 立体声 (2 x BTL) 和单声道 (1 x PBTL) 配置
- THD+N 为 10% 时的输出功率
  - 200W/4Ω，BTL 立体声配置
  - 300W/3Ω，PBTL 单声道配置
  - 425W/2Ω，PBTL 单声道配置
- THD+N 为 1% 时的输出功率
  - 170W/4Ω，BTL 立体声配置
  - 325W/2Ω，PBTL 单声道配置
- 闭环反馈设计
  - 1W/4Ω 时的 THD+N 小于 0.02%
  - 60dB PSRR（BTL，无输入信号）
  - 输出噪声（A 加权）< 100μV
  - SNR（A 加权）> 110dB
- 低功耗运行模式
  - 待机模式：静音和关断
  - 单通道 BTL 运行
- 多输入选项，可简化前置放大器设计
  - 差分或单端模拟输入
  - 可选增益：20dB、23.5dB、32dB、36dB
- 集成式保护：欠压、过压、过流、逐周期电流限制、短路、削波检测、过热警告和关断以及直流扬声器保护
- 轻松同步多个器件
- 90% 高效 D 类运行 (4Ω)

2 应用

- 蓝牙和 Wi-Fi™ 扬声器
- 条形音箱
- 低音炮
- 专业和公共广播 (PA) 扬声器

3 说明

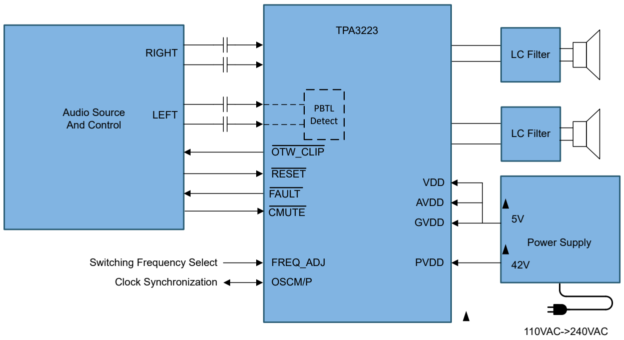
TPA3223 是一款可在全功率、空闲和待机状态下实现高效运行的高功率 D 类放大器。该器件具有闭环反馈，从而在整个音频频带内实现低失真并提供出色的音质。该器件以 AD 调制运行，最多可为 4Ω 负载提供 2 x 200W 的功率，或为 2Ω 负载提供 1 x 400W 的功率。

TPA3223 具有单端或差分模拟输入接口，最高支持 2V_{RMS}，具有四种可选增益：20dB、23.5dB、32dB 和 36dB。TPA3223 还实现了大于 90% 的效率、低空闲功率和超低待机功耗 (< 0.1W)。这是通过采用 60mΩ MOSFET、经优化的栅极驱动方案和低功耗运行模式实现的。为进一步简化设计，该器件集成了重要的保护功能，包括欠压、过压、逐周期电流限制、短路、削波检测、过热警告和关断以及直流扬声器保护。

器件信息(1)

器件型号	封装	封装尺寸（NOM）
TPA3223	HTSSOP (44)	6.10mm x 14.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 Revision History

DATE	REVISION	NOTES
November 2022	*	Initial release

5 Device Comparison

表 5-1. Device Comparison Table

DEVICE NAME	DESCRIPTION	SUPPLY VOLTAGE	THERMAL PAD LOCATION
TPA3220	60-W Stereo, 110-W Peak HD Analog-Input, Pad-Down Class-D Amplifier	32 V	Bottom
TPA3221	100 W Stereo, 200 W Mono HD, Analog-Input, Class-D Amplifier	32 V	Top
TPA3244	60-W Stereo, 110-W peak PurePath™ Ultra-HD Pad Down Class-D Amplifier	31.5 V	Bottom
TPA3245	115-W Stereo, 230-W Mono PurePath™ Ultra-HD Analog-Input Class-D Amplifier	31.5 V	Top
TPA3250	70 W Stereo, 130 W Peak Ultra-HD, Analog-Input, Pad-Down Class-D Amplifier	38 V	Bottom
TPA3251	175 W Stereo, 350 W Mono Ultra-HD, Analog-Input Class-D Amplifier	38 V	Top
TPA3255	315 W Stereo, 600 W Mono Ultra-HD, Analog-Input Class-D Amplifier	53.5 V	Top

6 Pin Configuration and Functions

The TPA3223 is available in a thermally enhanced TSSOP package.

The package type contains a thermal pad that is located on the top side of the device for convenient thermal coupling to the heat sink.

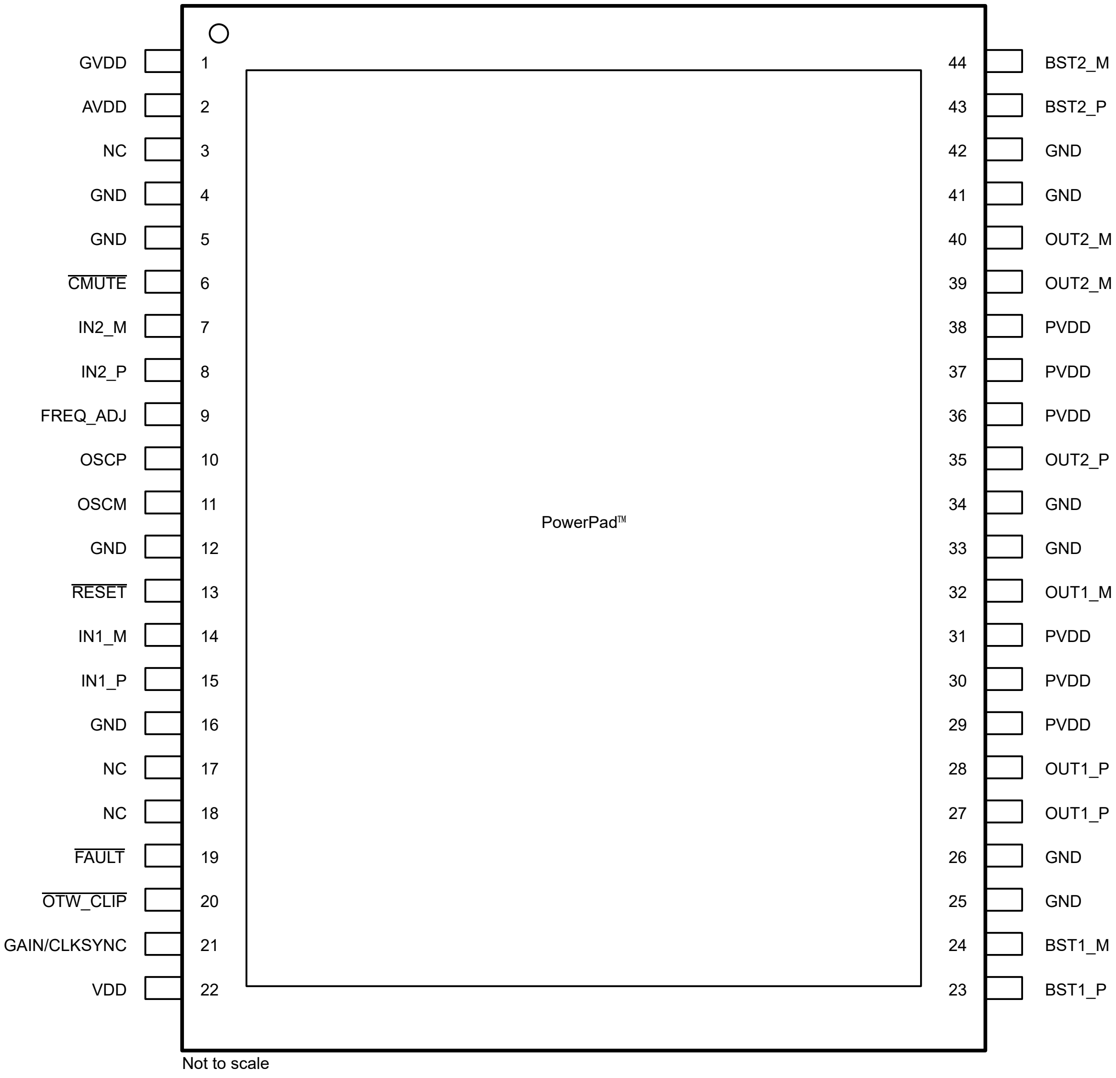


图 6-1. DDV Package, HTSSOP 44-Pin, Top View

6.1 Pin Functions

表 6-1. Pin Functions Table

NAME	NO.	I/O(1)	DESCRIPTION
AVDD	2	P	AVDD voltage supply. Refer to: 节 10.3.1.2
BST1_M	24	P	OUT1_M HS bootstrap supply (BST), 0.033 μF capacitor to OUT1_M required. Refer to: 节 10.2.1.2.3
BST1_P	23	P	OUT1_P HS bootstrap supply (BST), 0.033 μF capacitor to OUT1_P required. Refer to: 节 10.2.1.2.3
BST2_M	44	P	OUT2_M HS bootstrap supply (BST), 0.033 μF capacitor to OUT2_M required. Refer to: 节 10.2.1.2.3
BST2_P	43	P	OUT2_P HS bootstrap supply (BST), 0.033 μF capacitor to OUT2_P required. Refer to: 节 10.2.1.2.3
CMUTE	6	P	Mute and Startup Timing Capacitor. Connect a 33 nF capacitor to GND. Refer to: 节 9.4.3
FAULT	19	O	Shutdown signal, open drain; active low. Refer to: 节 9.3.6
FREQ_ADJ	9	O	Oscillator frequency programming pin. Refer to: 节 9.3.4
GAIN/CLKSYNC	21	I	Closed loop gain and clock synchronization configuration pin. Refer to: 节 9.3.1
GND	4,5,12,16,25, 26,42,33,34, 41	P	Ground
GVDD	1	P	Gate drive supply. Refer to: 节 10.3.1.2
IN1_M	14	I	Negative audio input for channel 1
IN1_P	15	I	Positive audio input for channel 1
IN2_M	7	I	Negative audio input for channel 2
IN2_P	8	I	Positive audio input for channel 2
NC	3,17,18		Not connected or pulled to ground
OSCM	11	I/O	Oscillator synchronization interface. Refer to: 节 9.3.1
OSCP	10	I/O	Oscillator synchronization interface. Refer to: 节 9.3.1
OTW_CLIP	20	O	Clipping warning and Over-temperature warning; open drain; active low. Refer to: 节 9.3.6
OUT1_M	32	O	Negative output for channel 1
OUT1_P	27,28	O	Positive output for channel 1
OUT2_M	39,40	O	Negative output for channel 2
OUT2_P	35	O	Positive output for channel 2
PVDD	29,30,31,36, 37,38	P	PVDD supply. Refer to: 节 10.2.1.2.2 and 节 10.3.1.3
RESET	13	I	Device reset input; active low. Refer to: 节 9.4.5.7, 节 9.4.1, 节 9.4.2
VDD	22	P	Input power supply. Refer to: 节 10.3.1.1
PowerPad™		P	Ground, connect to grounded heatsink. Placed on top side of device.

(1) I=Input, O=Output, I/O= Input/Output, P=Power

表 6-2. Mode Selection Pins

MODE PINS(2)		INPUT MODE(1)	OUTPUT CONFIGURATION	DESCRIPTION
IN2_M	IN2_P			
X	X	1N/2N + 1	2 × BTL	Stereo, BTL output configuration, AD mode modulation
0	0	1N/2N + 1	1 x PBTL	Mono, Paralleled BTL configuration. Connect OUT1_P to OUT2_P and OUT1_M to OUT2_M, AD mode modulation
1	1	1N/2N + 1	1 x BTL	Mono, BTL configuration. OUT1_M and OUT1_P active, AD mode modulation

(1) 2N refers to differential input signal, 1N refers to single ended input signal. +1 refers to number of logic control (RESET) input pins.
(2) X refers to inputs connected through AC coupling capacitor, 0 refers to logic low (GND), 1 refers to logic high (AVDD).

7 Specifications

7.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

		最小值	最大值	单位
电源电压	PVDD 至 GND	–0.3	50	V
	PVDD 至 GND（瞬态小于 8ns）(2)	–0.3	57	V
	BST_X 至 GVDD	–0.3	50	V
	VDD 至 GND	–0.3	50	V
	GVDD 至 GND(2)	–0.3	5.5	V
	AVDD 至 GND	–0.3	5.5	V
输出引脚	OUT1_M、OUT1_P、OUT2_M、OUT2_P 至 GND	–0.3	50	V
	OUT1_M、OUT1_P、OUT2_M、OUT2_P 至 GND（瞬态小于 8ns）(2)	–0.3	57	V
接口引脚	IN1_M、IN1_P、IN2_M、IN2_P 至 GND	–0.3	5.5	V
	FREQ_ADJ、GAIN/CLKSYNC、$\overline{\text{CMUTE}}$、$\overline{\text{RESET}}$、OSCP、OSCM 至 GND	–0.3	5.5	V
	$\overline{\text{FAULT}}$、$\overline{\text{OTW\_CLIP}}$ 至 GND	–0.3	5.5	V
	持续灌电流、$\overline{\text{FAULT}}$、$\overline{\text{OTW\_CLIP}}$ 至 GND		9	mA
T_J	工作结温范围	0	150	°C
T_{stg}	贮存温度范围	-40	150	°C

(1) 应力超出*绝对最大额定值*下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是应力额定值，这并不表示器件在这些条件下以及在*建议运行条件*以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 这些电压表示在各种条件下测得的器件端子直流电压 + 峰值交流波形。

7.2 ESD 等级

			值	单位
V_{ESD}	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001，所有引脚 (1)	±3000	V
		充电器件模型（CDM），符合 JEDEC 规范 JESD22-C101，所有引脚(2)	±1500	V

(1) JEDEC 文档 JEP155 指出：500V HBM 可实现在标准 ESD 控制流程下安全生产。
(2) JEDEC 文件 JEP157 指出：250V CDM 可实现在标准 ESD 控制流程下安全生产。

7.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）

			最小值	典型值	最大值	单位
PVDD	功率级电源	直流电源电压	10	42	45	V
VDD(1)	VDD、GVDD 和 AVDD 的外部电源	直流电源电压	4.5	5	5.5	V
AVDD	模拟电路的电源电压	直流电源电压	4.5	5	5.5	V
GVDD	栅极驱动电路的电源电压	直流电源电压	4.5	5	5.5	V
V_{IN}	最大输入电压摆幅（INx_P、INx_M）				±2.8	V
R_L(BTL)	负载阻抗 BTL	PVDD = 42V，输出滤波器电感在推荐范围内	3.5	4		Ω
		PVDD =< 42V，输出滤波器电感在推荐范围内	PVDD/（I_{OC}，BTL）			
R_L(PBTL)	负载阻抗 PBTL	PVDD = 42V，输出滤波器电感在推荐范围内	1.6	3		Ω
L_{OUT}(BTL)	输出滤波器电感	I_{OC} 处的最小输出电感	5	10		μH
L_{OUT}(PBTL)	输出滤波器电感，LC 滤波器后的 PBTL	每个电感器在一半 I_{OC} 处的最小输出电感	5	10		μH
F_{PWM}	为避免 AM 干扰，PWM 帧速率可供选择；1% 电阻容差	标称值	460	480	500	kHz
		AM1	510	533	555	
		AM2	575	600	625	
$f_{OSC(IO)}$	OSCM/OSCP 上的 CLK 输入（外设模式）		2.3		3.78	MHz
$R_{(FREQ\_ADJ)}$	PWM 帧速率编程电阻	标称值；主模式	9.9	10	10.1	kΩ
		AM1；主模式	29.7	30	30.3	
		AM2；主模式	49.5	50	50.5	
C_{PVDD}	PVDD 闭合去耦电容器			1.0		μF
$V_{(FREQ\_ADJ)}$	用于外设模式运行的 FREQ_ADJ 引脚上的电压	外设模式（连接至 AVDD）		5		V
T_J	结温		0		125	°C

(1) VDD 必须连接至 5V 电源

7.4 热性能信息

热指标(1)		TPA3223	单位
		DDV 44 引脚 HTSSOP	
		JEDEC 标准 4 层 PCB	
$R_{\theta JA}$	结至环境热阻	42.6	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	0.9	°C/W
$R_{\theta JB}$	结至电路板热阻	13.8	°C/W
ψ_{JT}	结至顶部特征参数	0.4	°C/W
ψ_{JB}	结至电路板特征参数	13.5	°C/W
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	不适用	°C/W

(1) 有关新旧热指标的更多信息，请参阅*半导体和 IC 封装热指标*应用报告。

7.5 电气特性

PVDD = 42V，VDD = 5V，GVDD = 5V，AVDD = 5V，T_C（外壳温度）= 75°C，f_S = 480kHz，除非另有说明。

参数		测试条件	最小值	典型值	最大值	单位
电源电压和电流消耗						
I_{VDD}	VDD 电源电流	运行，无音频信号，VDD = 5V		150		μA
I_{VDD}		复位模式，VDD = 5V		5		μA
I_{GVDD}	栅极电源电流。AD 模式调制	50% 占空比，VDD = 5V		23		mA
I_{GVDD}		复位模式，VDD = 5V		5		μA
I_{PVDD}	总 PVDD 空闲电流，AD 模式调制，BTL	使用推荐输出滤波器，占空比为 50%		45		mA
I_{PVDD}	总 PVDD 空闲电流，AD 模式调制，BTL	使用推荐输出滤波器，占空比为 50%，T_C = 25ºC		35		mA
I_{PVDD}	总 PVDD 空闲电流，AD 模式调制，BTL	复位模式，无开关		1		mA
模拟输入						
G	反相电压增益，V_{OUT}/V_{IN}（主时钟同步器件配置）	R_1 = 5.6kΩ，R_2 = 断开		20		dB
		R_1 = 20kΩ，R_2 = 100kΩ		23.5		
		R_1 = 39kΩ，R_2 = 100kΩ		32		
		R_1 = 47kΩ，R_2 = 75kΩ		36		
	反相电压增益，V_{OUT}/V_{IN}（外设时钟同步器件配置）	R_1 = 51kΩ，R_2 = 51kΩ		20		
		R_1 = 75kΩ，R_2 = 47kΩ		23.5		
		R_1 = 100kΩ，R_2 = 39kΩ		32		
		R_1 = 100kΩ，R_2 = 16kΩ		36		
R_{IN}	输入电阻	G = 20dB		48		kΩ
		G = 23.5dB		24		
		G = 32dB		12		
		G = 36dB		7.3		
振荡器						
$f_{OSC(IO)}$ (1)	标称值，主模式	F_{PWM} × 6	2.76	2.88	3	MHz
	AM1，主模式		3.06	3.198	3.33	
	AM2，主模式		3.45	3.6	3.75	
V_{IH}	高电平输入电压		2.7			V
V_{IL}	低电平输入电压				0.7	V
外部振荡器（外设模式）						
输出级 MOSFET						
$R_{DS(on)}$	漏源电阻，低侧 (LS)	T_J = 25°C，不包括金属化电阻，GVDD = 5V		60		mΩ
	漏源电阻，高侧 (HS)			60		mΩ
I/O 保护						
$V_{uvp,AVDD}$	欠压保护限制，AVDD			4		V
$V_{uvp,AVDD,hyst}$	欠压保护迟滞，AVDD			0.2		V
$V_{uvp,PVDD}$	欠压保护限制，PVDD_x			9.1		V
$V_{uvp,PVDD,hyst}$	欠压保护迟滞，PVDD_x			0.6		V
$V_{ovp,PVDD}$	过压保护限制，PVDD_x			46		V
$V_{ovp,PVDD,hyst}$	过压保护迟滞，PVDD_x			0.85		V
OTW	过热警告，$\overline{\mathrm{OTW\_CLIP}}$			125		°C
OTW_{hyst}	需将温度降至 OTW 温度以下，才能在 OTW 事件后停用 $\overline{\mathrm{OTW\_CLIP}}$。			20		°C
OTE	过热错误			155		°C
OTE_{hyst}	需复位才能在 OTE 事件后释放 $\overline{\mathrm{FAULT}}$			20		°C
$OTE\text{-}OTW_{(differential)}$	OTE-OTW 差分			25		°C
OLPC	过载保护计数器	f_{PWM} = 480kHz（1024 个 PWM 周期）		2.2		ms
$I_{OC,\ BTL}$	过流限制保护，扬声器负载电流	1Ω 负载时的标称峰值电流		10		A

7.5 电气特性 (continued)

PVDD = 42V，VDD = 5V，GVDD = 5V，AVDD = 5V，T_C（外壳温度）= 75°C，f_S = 480kHz，除非另有说明。

参数		测试条件	最小值	典型值	最大值	单位
$I_{OC, PBTL}$	过流限制保护，扬声器输出电流	1Ω 负载时的标称峰值电流		20		A
I_{OCT}	过流响应时间	由过流引起的从开关转换到翻转状态的时间。		150		ns
静态数字规格						
V_{IH}	高电平输入电压	$\overline{\text{RESET}}$	2.3			V
V_{IL}	低电平输入电压				0.7	V
I_{lkg}	输入漏电流	OSCM、OSCP、$\overline{\text{RESET}}$			100	μA
OTW/关断（故障）						
R_{INT_PU}	内部上拉电阻，$\overline{\text{OTW\_CLIP}}$ 至 AVDD，$\overline{\text{FAULT}}$ 至 AVDD			26		kΩ
V_{OH}	高电平输出电压	内部上拉电阻	4.5	5	5.5	V
V_{OL}	低电平输出电压	I_O = 4 mA		200	500	mV

(1) 标称值，AM1 和 AM2 使用相同的内部振荡器，其固定比率为 4 : 4.5 : 5

7.6 音频特性 (BTL)

PCB 和系统配置符合推荐指南。音频频率 = 1kHz，PVDD_X = 42V，VDD = 5V，GVDD = 5V，R_L = 4 Ω、f_S = 480kHz，T_C = 75°C，输出滤波器：L_{DEM} = 10 µ H，C_{DEM} = 1µF，AD 调制，AES17 + AUX-0025 测量滤波器，除非另有说明。

参数		测试条件	最小值	典型值	最大值	单位
P_O	每通道功率输出	R_L = 4Ω，10% THD+N		200		W
P_O	每通道功率输出	R_L = 4Ω，1% THD+N		170		W
THD+N	总谐波失真 + 噪声	1W		0.02		%
V_n	输出积分噪声	A 加权，AES17 滤波器，输入电容器接地，增益 = 20dB		100		µ V
$\|V_{OS}\|$	输出失调电压	输入交流耦合至 GND		5	20	mV
SNR	信噪比(1)	A 加权，增益 = 20dB		108		dB
DNR	动态范围	A 加权，增益 = 20dB		109		dB
P_{idle}	空闲损耗引起的功率耗散 (I_{PVDD_X})	P_O = 0，所有输出开关，AD 调制，T_C = 25°C(2)		1.5		W

(1) SNR 根据 1% THD+N 输出电平计算得出。
(2) 实际系统空闲损耗也受输出电感器磁芯损耗的影响。

7.7 音频特性 (PBTL)

PCB 和系统配置符合推荐指南。音频频率 = 1kHz，PVDD_X = 42V，VDD = 5V，GVDD = 5V，R_L = 3Ω，f_S = 480kHz，T_C = 75°C，输出滤波器：L_{DEM} = 10 µ H，C_{DEM} = 1µF，后置滤波器 PBTL，AD 调制，AES17 + AUX-0025 测量滤波器，除非另有说明。

参数		测试条件	最小值	典型值	最大值	单位
P_O	每通道功率输出	R_L = 2Ω，10% THD+N		425		W
		R_L = 3Ω，10% THD+N		300		W
		R_L = 4Ω，10% THD+N		250		
		R_L = 2Ω，1% THD+N		325		
		R_L = 3Ω，1% THD+N		245		
		R_L = 4Ω，1% THD+N		195		
THD+N	总谐波失真 + 噪声	1W		0.017		%
V_n	输出积分噪声	A 加权，AES17 滤波器，输入电容器接地，增益 = 20dB		100		µ V
$\|V_{OS}\|$	输出失调电压	输入交流耦合至 GND		10		mV
SNR	信噪比(1)	A 加权，增益 = 20dB		109		dB
DNR	动态范围	A 加权，增益 = 20dB		110		dB
P_{idle}	空闲损耗引起的功率耗散 (IPVDD_X)	P_O = 0，所有输出开关，AD 调制，T_C = 25°C(2)		1.5		W

(1) SNR 根据 1% THD+N 输出电平计算得出。
(2) 实际系统空闲损耗受输出电感器磁芯损耗的影响。

7.8 Typical Characteristics, BTL Configuration, AD-mode

All Measurements taken at audio frequency = 1 kHz, PVDD = 42 V, VDD = 5 V, GVDD = 5 V, R_L = 4 Ω, f_S = 480 kHz, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µFAES17 + AUX-0025 measurement filters, unless otherwise noted.

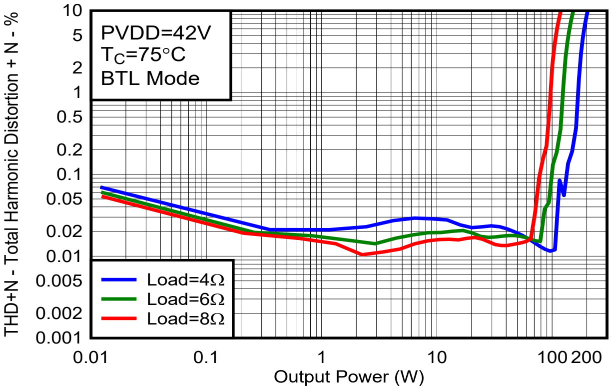


图 7-1. Total Harmonic Distortion + Noise vs Output Power

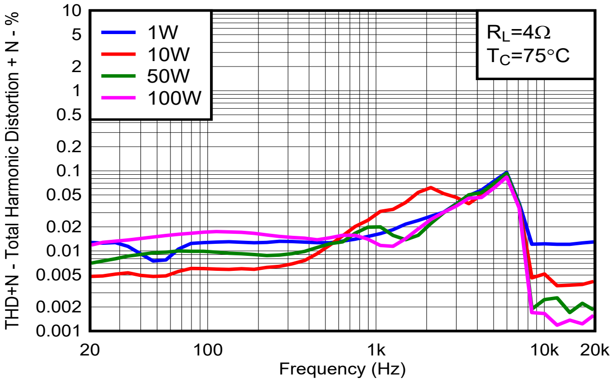


图 7-2. Total Harmonic Distortion+Noise vs Frequency

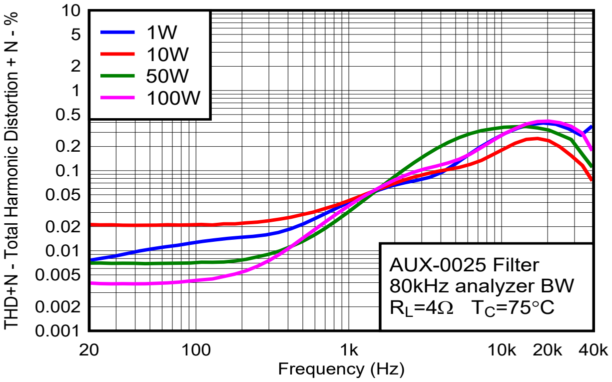


图 7-3. Total Harmonic Distortion+Noise vs Frequency

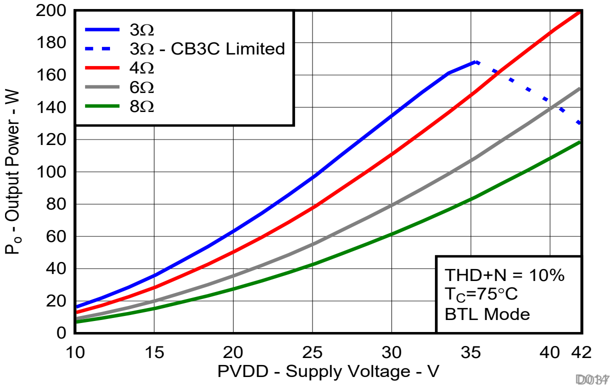


图 7-4. Output Power vs Supply Voltage, AD-mode

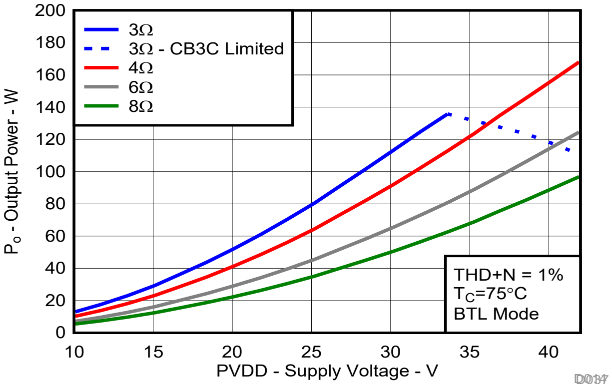


图 7-5. Output Power vs Supply Voltage, AD-mode

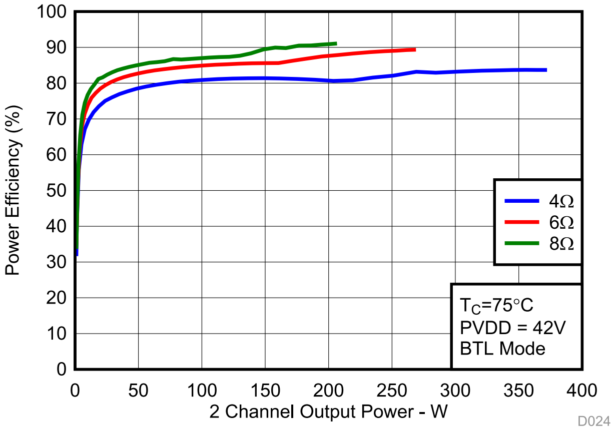


图 7-6. System Efficiency vs Output Power

7.8 Typical Characteristics, BTL Configuration, AD-mode (continued)

All Measurements taken at audio frequency = 1 kHz, PVDD = 42 V, VDD = 5 V, GVDD = 5 V, R_L = 4 Ω, f_S = 480 kHz, T_C = 75°C, Output Filter: L_{DEM} = 10 μH, C_{DEM} = 1 μF AES17 + AUX-0025 measurement filters, unless otherwise noted.

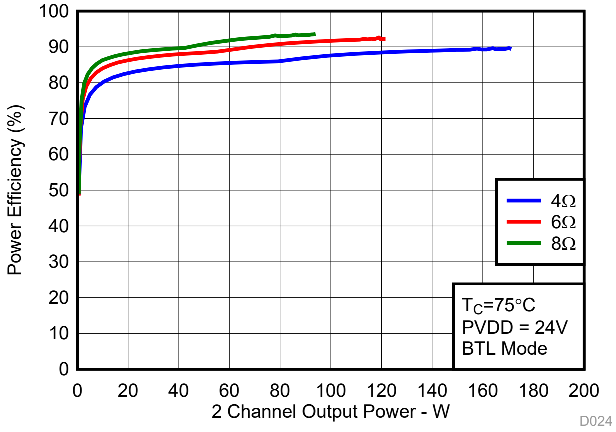


图 7-7. System Efficiency vs Output Power

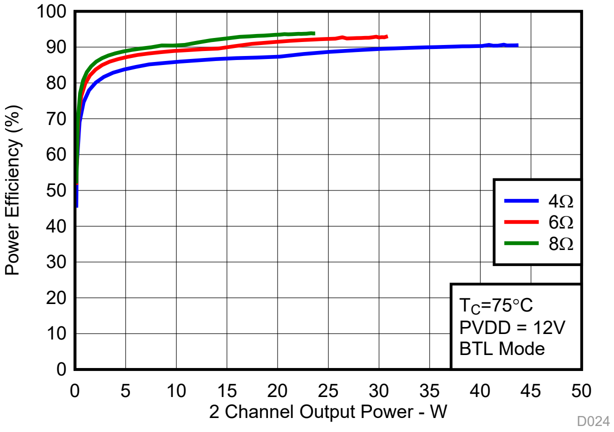


图 7-8. System Efficiency vs Output Power

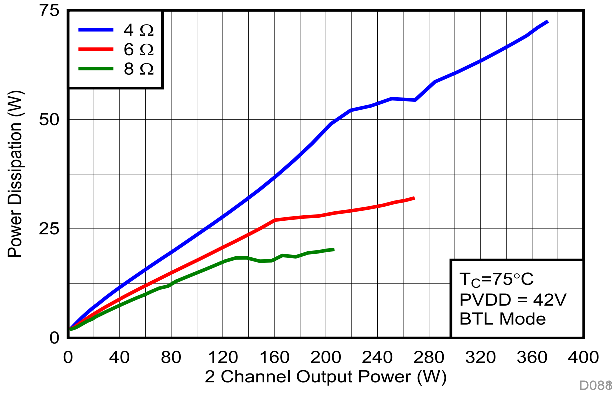


图 7-9. Power Dissipation vs Output Power

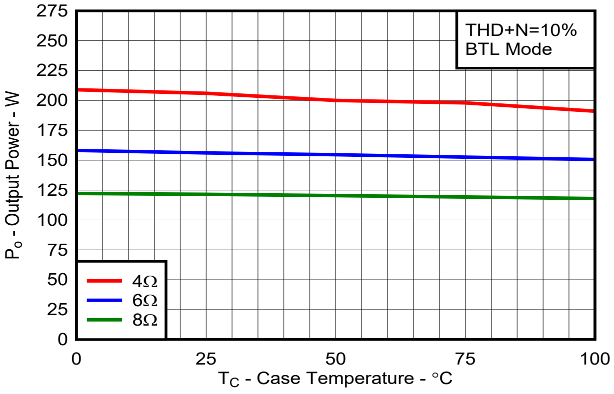


图 7-10. Output Power vs Case Temperature

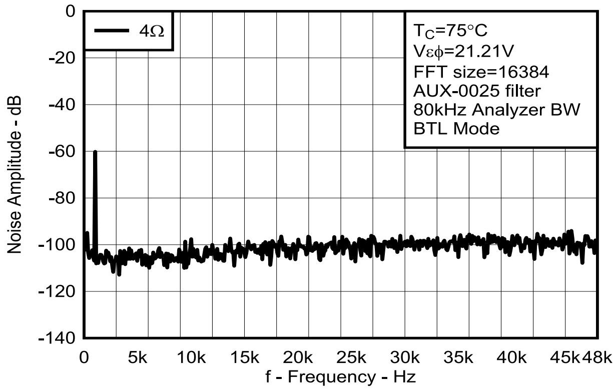
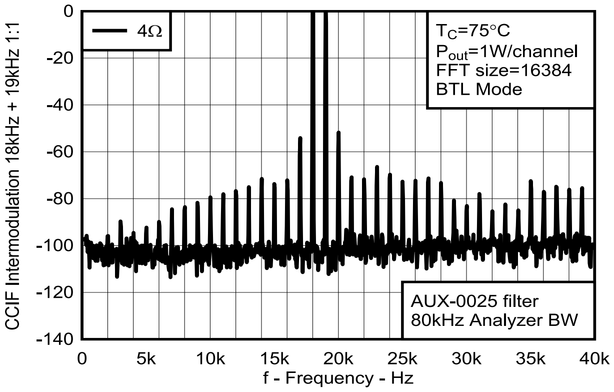


图 7-11. Noise Amplitude vs Frequency

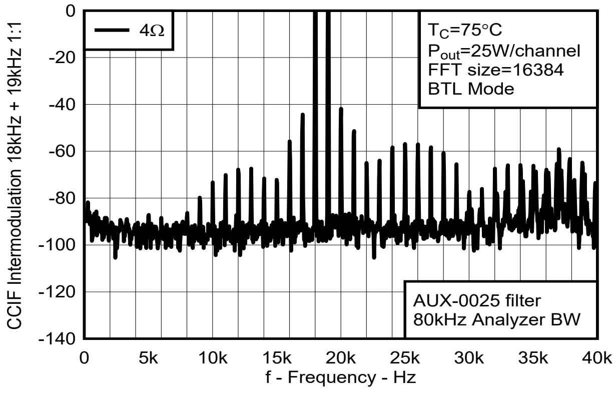


18 kHz + 19 kHz Ratio 1 : 1

图 7-12. CCIF Intermodulation

7.8 Typical Characteristics, BTL Configuration, AD-mode (continued)

All Measurements taken at audio frequency = 1 kHz, PVDD = 42 V, VDD = 5 V, GVDD = 5 V, R_L = 4 Ω, f_S = 480 kHz, T_C = 75°C, Output Filter: L_{DEM} = 10 µ H, C_{DEM} = 1 µ FAES17 + AUX-0025 measurement filters, unless otherwise noted.



18 kHz + 19 kHz Ratio 1 : 1

图 7-13. CCIF Intermodulation

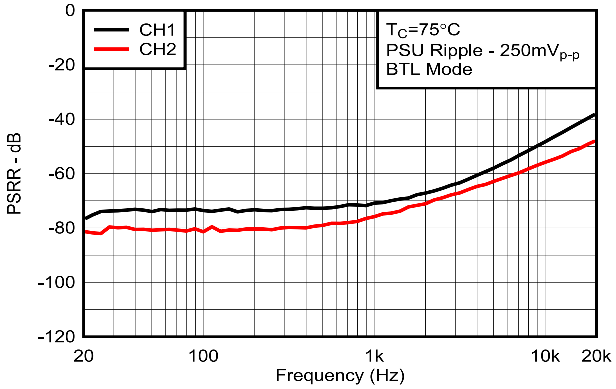


图 7-14. Power Supply Rejection Ratio vs Frequency

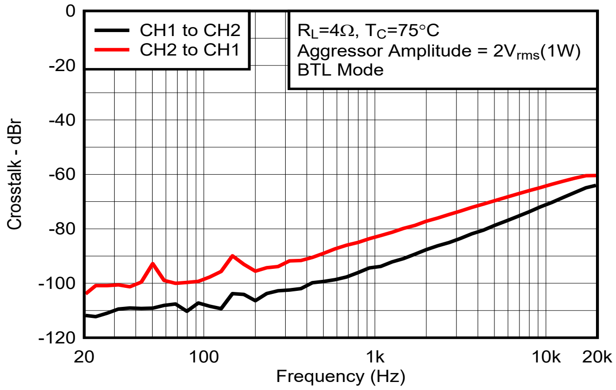


图 7-15. Channel to Channel Crosstalk vs Frequency

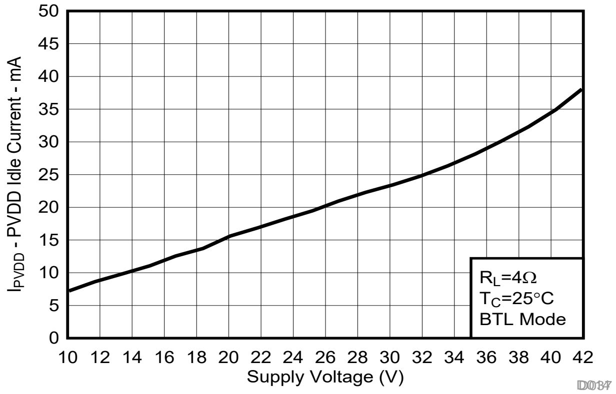


图 7-16. PVDD Idle Current vs Supply Voltage

7.9 Typical Characteristics, PBTL Configuration, AD-mode

All Measurements taken at audio frequency = 1 kHz, PVDD = 42 V, VDD = 5 V, GVDD = 5 V, R_L = 2 Ω, f_S = 480 kHz, T_A = 75°C, Output Filter: L_{DEM} = 10 μ H, C_{DEM} = 1 μF, Post-Filter PBTL, AES17 + AUX-0025 measurement filters, unless otherwise noted.

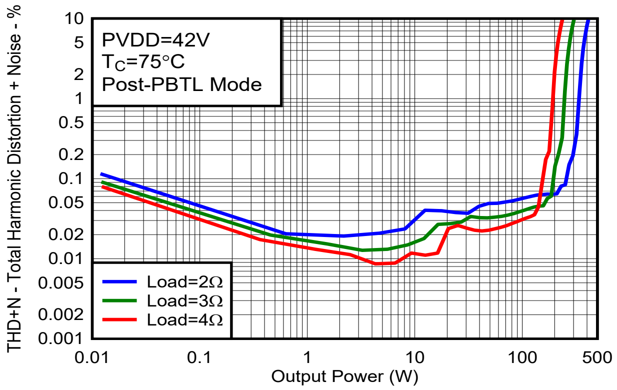


图 7-17. Total Harmonic Distortion+Noise vs Output

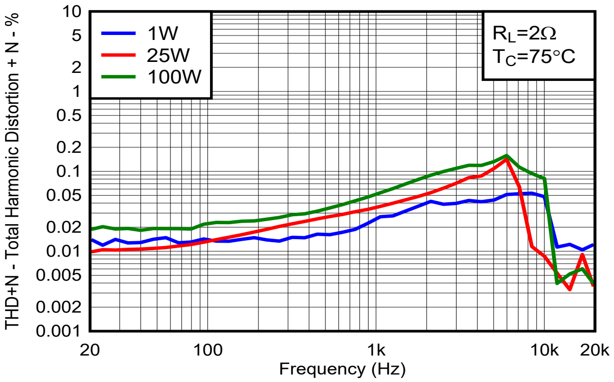


图 7-18. Total Harmonic Distortion+Noise vs Frequency

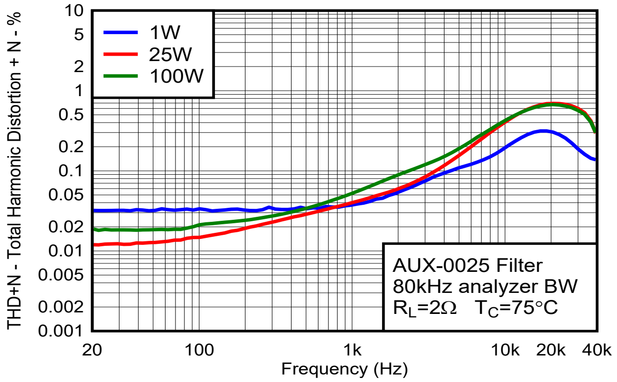


图 7-19. Total Harmonic Distortion+Noise vs Frequency

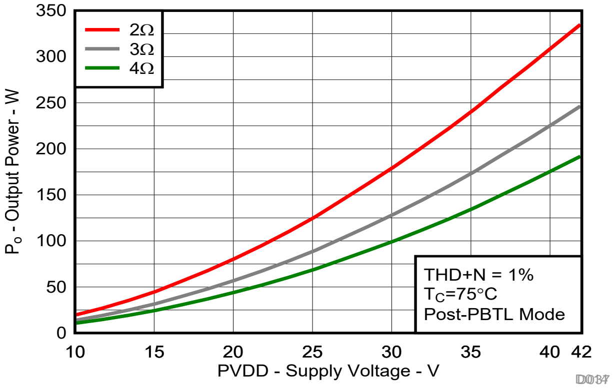


图 7-20. Output Power vs Supply Voltage

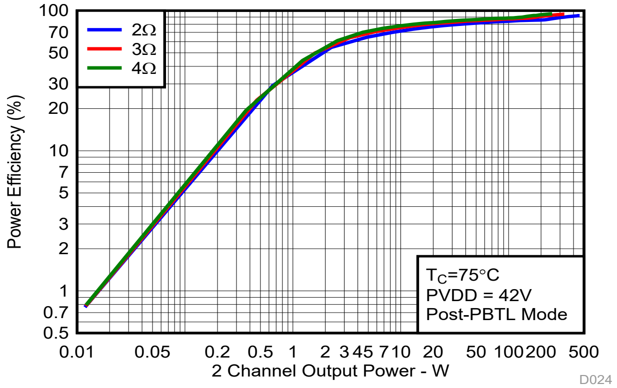


图 7-21. System Efficiency vs Output Power

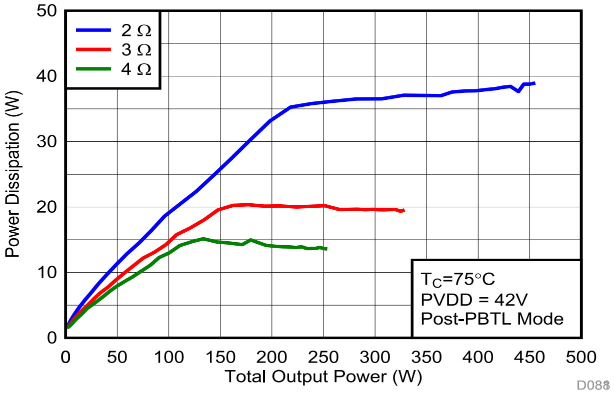


图 7-22. Power Dissipation vs Output Power

7.9 Typical Characteristics, PBTL Configuration, AD-mode (continued)

All Measurements taken at audio frequency = 1 kHz, PVDD = 42 V, VDD = 5 V, GVDD = 5 V, R_L = 2 Ω, f_S = 480 kHz, T_A = 75°C, Output Filter: L_{DEM} = 10 μH, C_{DEM} = 1 μF, Post-Filter PBTL, AES17 + AUX-0025 measurement filters, unless otherwise noted.

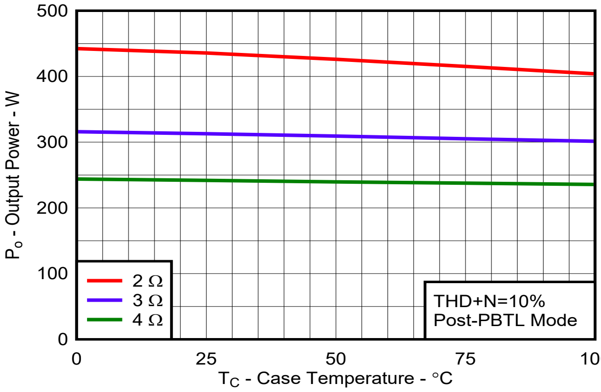


图 7-23. Output Power vs Case Temperature

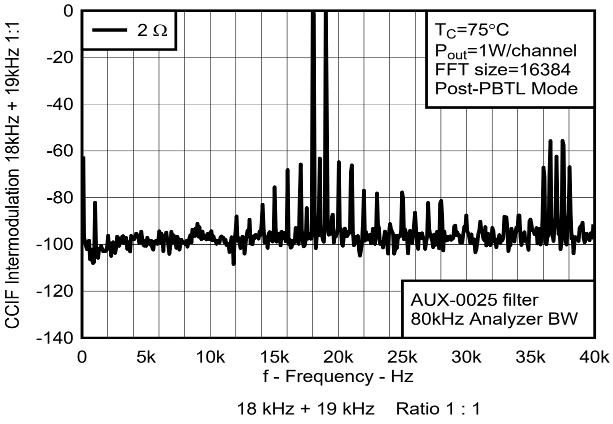


图 7-24. CCIF Intermodulation vs Frequency

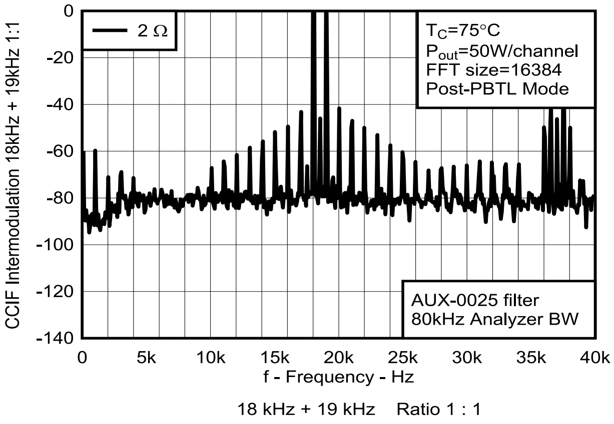


图 7-25. CCIF Intermodulation vs Frequency

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the 节 7.3 .

Most audio analyzers will not give correct readings of Class-D amplifiers' performance due to their sensitivity to out of band noise present at the amplifier output. AES-17 + AUX-0025 pre-analyzer filters are recommended to use for Class-D amplifier measurements. In absence of such filters, a 30-kHz low-pass filter (10 Ω + 47 nF) can be used to reduce the out of band noise remaining on the amplifier outputs.

9 Detailed Description

9.1 Overview

TPA3223 is designed as a feature-enhanced cost efficient high power Class-D audio amplifier. The device has built-in advanced protection circuitry to provide for maximum product robustness as well as a flexible feature set including selectable gain settings, switching frequency, clock synchronization of multiple devices, mute function, temperature and clipping status signals. TPA3223 has a bandwidth up to 100 kHz and low output noise designed for high resolution audio applications and accepts both differential and single ended analog audio inputs at levels from 1 V_{RMS} to 2 V_{RMS}. With the closed loop operation TPA3223 is designed for high audio performance with a system power supply between 10 V and 42 V.

An external 5 V supply is used for the AVDD and VDD supply pins. Although supplied from the same 5 V source, separating AVDD and VDD on the printed-circuit board (PCB) by RC filters (see 节 10.2 for details) is recommended. These RC filters provide the recommended high-frequency isolation. Special attention needs to be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the physical loop with the power supply pins, decoupling capacitors and GND return path to the device pins must be kept as short as possible and with as little area as possible to minimize induction (see *节 10.4.2* for additional information).

The floating supplies for the output stage high side gate drives are supplied by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides an acceptable voltage supply for the high-side gate driver. TI recommends to use 33 nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33 nF capacitors maintain sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention needs to be paid to the power stage power supply; this includes component selection, PCB placement, and routing.

For good electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X node is decoupled with 1 μF ceramic capacitors placed as close as possible to the PVDD supply pins. TI recommends to follow the PCB layout of the TPA3223 reference design. For additional information on recommended power supply and required components, see 节 10.2.

The external power supply for the AVDD and VDD supplies must be from a low-noise, low-output-impedance voltage regulator. Likewise, the 42V power stage supply is assumed to have low output impedance throughout the entire audio band, and low noise. The power supply sequence is not critical as facilitated by the internal power-on-reset circuit, but TI recommends to release $\overline{\text{RESET}}$ after the power supply is settled for minimum turn on audible artifacts. Moreover, the TPA3223 is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are noncritical within the specified range (see the *节 7.3* table of this data sheet).

9.2 Functional Block Diagrams

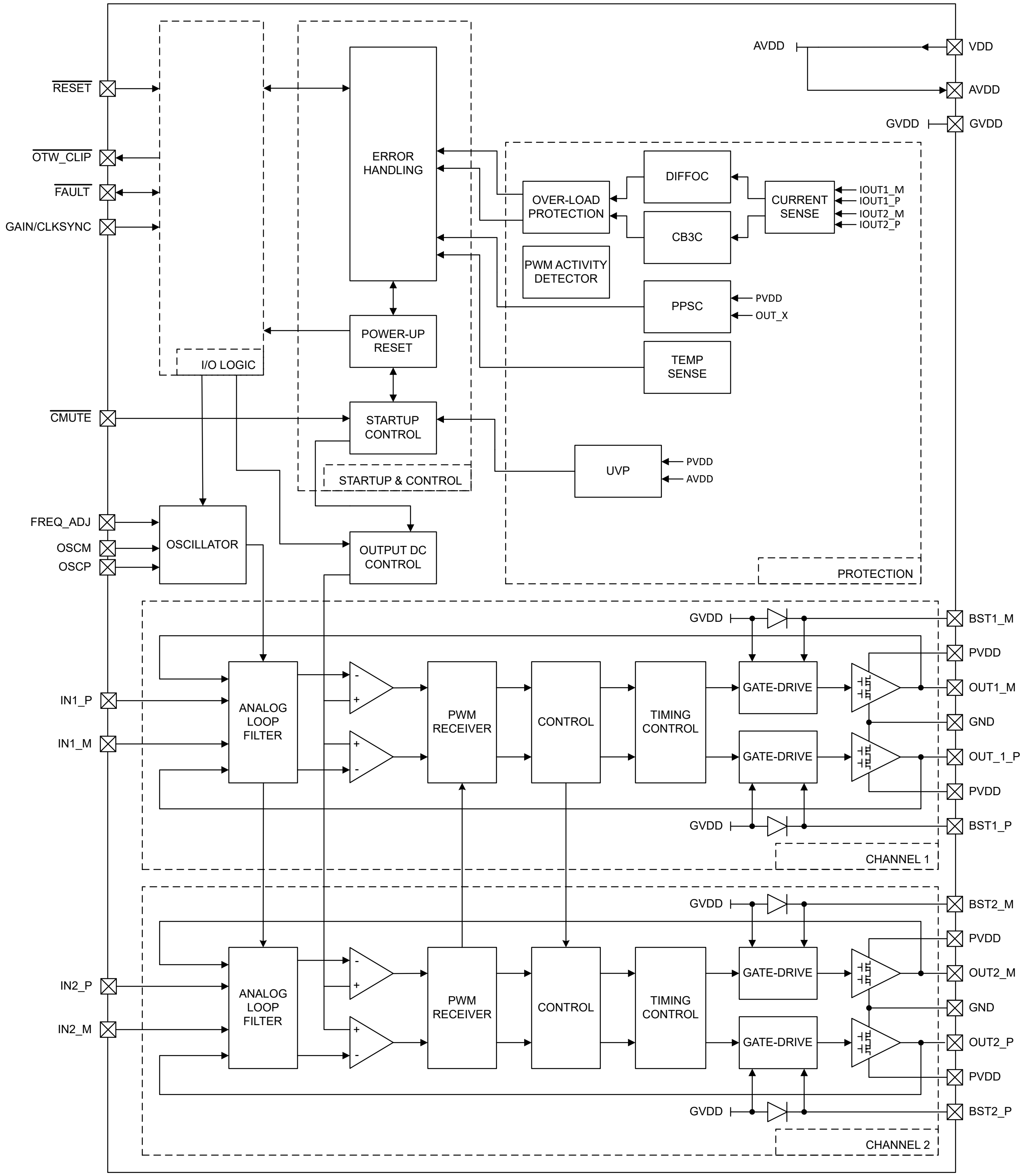
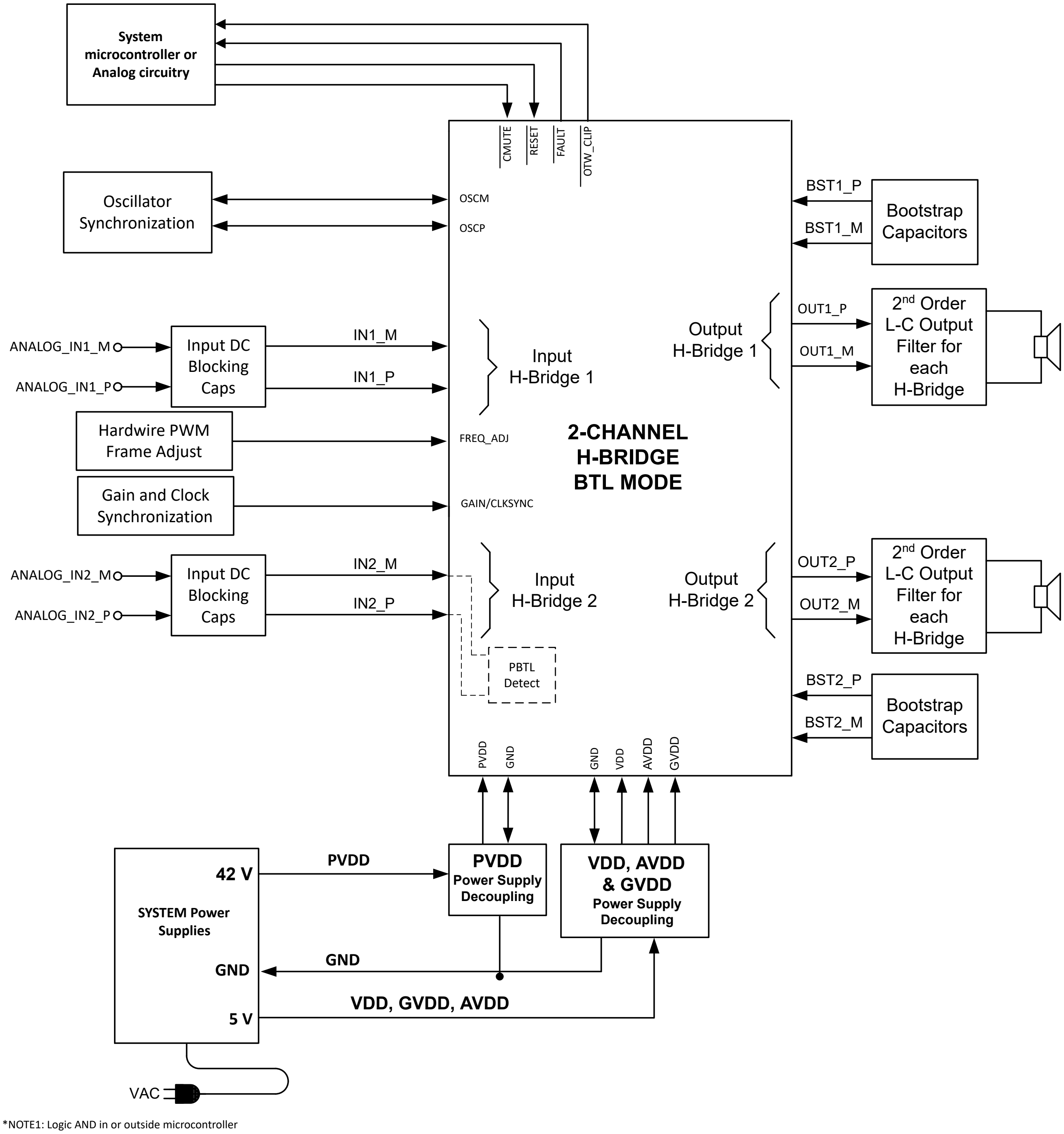


图 9-1. Functional Block Diagram



*NOTE1: Logic AND in or outside microcontroller

图 9-2. System Block Diagram

9.3 Feature Description

9.3.1 Input Configuration, Gain Setting And Primary / Peripheral Operation

TPA3223 is designed to accept either a differential or a single-ended audio input signal. To accept a wide range of system front ends TPA3223 has selectable input gain that allows full scale output with a wide range of input signal levels.

Best system noise performance is obtained with balanced audio interface. However, in systems with only a single ended audio input signal available, one input terminal can be connected to AC ground to accept single ended audio input signals.

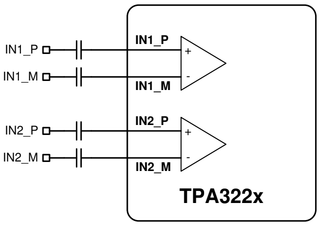


图 9-3. Balanced Audio Input Configuration

In systems with single ended audio inputs, set the device gain higher than for systems with balanced audio input signals.

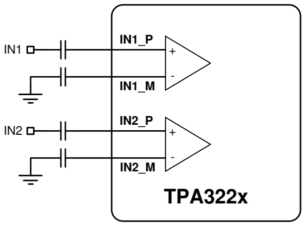


图 9-4. Single Ended Audio Input Configuration

9.3.2 Gain Setting And Clock Synchronization

The gain of TPA3223 is set by the voltage divider connected to the GAIN/CLKSYNC control pin. Clock synchronization configuration is also controlled by the same pin. An internal ADC is used to detect the 8 input states. The first four stages sets the GAIN in Primary mode in gains of 20, 23.5, 32 and 36 dB respectively, while the next four stages sets the GAIN in peripheral mode in gains of 20, 23.5, 32 and 36 dB respectively. The gain setting is latched when $\overline{\text{RESET}}$ goes high and cannot be changed while $\overline{\text{RESET}}$ is high. 表 9-1 shows the recommended resistor values, the state and gain:

表 9-1. Clock Synchronization Configuration

Primary / Peripheral Mode	Gain	R1 (to GND)	R2 (to AVDD)	Differential Input Signal Level (each input pin)	Single Ended Input Signal Level
Primary	20 dB	5.6 kΩ	OPEN	2 VRMS	2 VRMS
Primary	23.5 dB	20 kΩ	100 kΩ	1 VRMS	2 VRMS
Primary	32 dB	39 kΩ	100 kΩ	0.5 VRMS	1 VRMS
Primary	36 dB	47 kΩ	75 kΩ	0.32 VRMS	0.63 VRMS
Peripheral	20 dB	51 kΩ	51 kΩ	2 VRMS	2 VRMS
Peripheral	23.5 dB	75 kΩ	47 kΩ	1 VRMS	2 VRMS
Peripheral	32 dB	100 kΩ	39 kΩ	0.5 VRMS	1 VRMS
Peripheral	36 dB	100 kΩ	16 kΩ	0.32 VRMS	0.63 VRMS

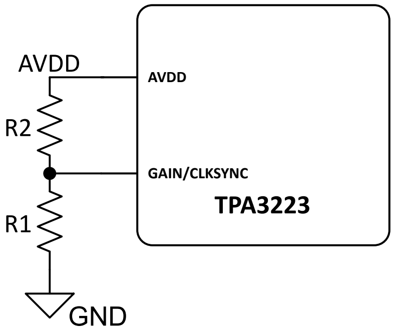


图 9-5. Clock Synchronization Setup

For easy multi-channel system design TPA3223 has a Clock Synchronization feature that allows automatic synchronization of multiple peripheral devices operated at the PWM switching frequency of a Primary device. Using clock synchronization benefits system noise performance by eliminating spurious crosstalk sum and difference tones due to unsynchronized channel-to-channel switching frequencies. Furthermore, the Clock Synchronization scheme is designed to interleave switching of the individual channels in a multi-channel system such that the power supply current ripple frequency is moved to a higher frequency, which reduces the RMS ripple current in the power supply bulk capacitors.

The Clock Synchronization scheme and the interleaving of the output stage switching are automatically configured by connecting the OSCx pins between a Primary and multiple peripheral devices. There are two different configurations of peripheral devices (secondary or tertiary) depending on how the OSCx pins are connected. Connect the OSCM of the Primary device to the OSCM of a peripheral device and the OSCP of the Primary device to the OSCP pin of a peripheral device to configure as a secondary. Connect the OSCM of the Primary device to the OSCP of a peripheral device and the OSCP of the Primary device to the OSCM pin of a peripheral device to configure as a tertiary. The Primary, secondary and tertiary PWM switching is 30 degrees out of phase with each other. All switching channels are automatically synchronized by releasing $\overline{\text{RESET}}$ on all devices at the same time.

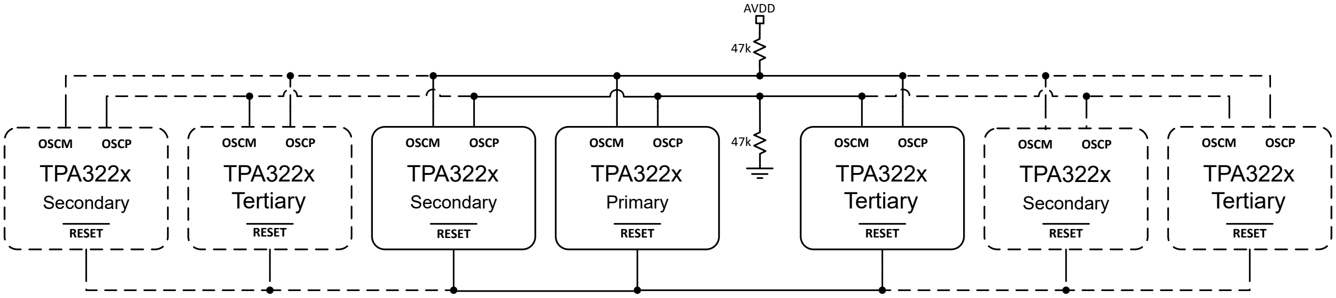


图 9-6. Gain and Primary PCB Implementation

Placement on the PCB and connection of multiple TPA3223 devices in a multi channel system is illustrated in 图 9-6. Peripheral devices must be placed on either side of the Primary device, with a secondary device on one side of the Primary device, and a tertiary device on the other. In systems with more than 3 TPA3223 devices, the Primary must be in the middle, and every second peripheral device must be a secondary or tertiary as illustrated in 图 9-6. A 47 kΩ pull up resistor to AVDD must be connected to the Primary device OSCM output and a 47 kΩ pull down resistor to GND must be connected to the Primary OSCP CLK outputs.

9.3.3 PWM Modulation

The TPA3223 uses the AD-Mode PWM modulation scheme which continuous switches the two half bridge outputs in each BTL output channel.

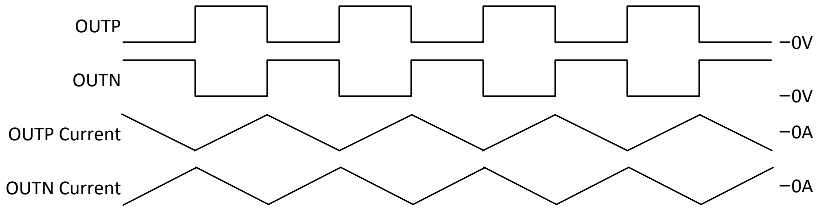


图 9-7. AD Mode Output Waveforms, Idle

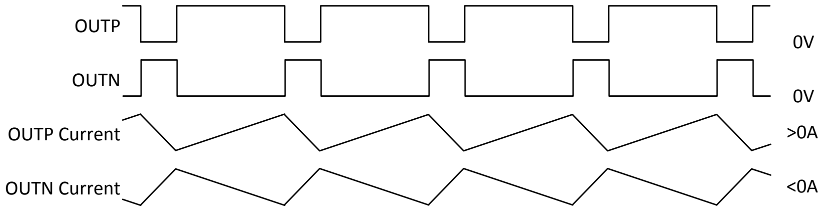


图 9-8. AD Mode Output Waveforms, High Level Output

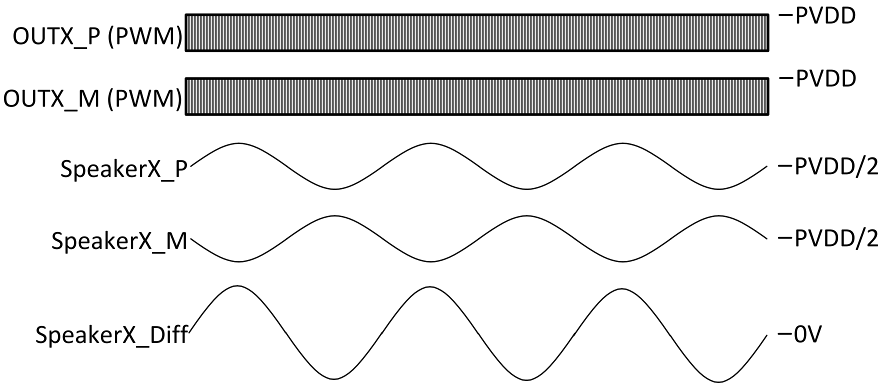


图 9-9. AD Mode Speaker Output Signals, Low or and High Level Output

9.3.4 Oscillator

The oscillator frequency can be trimmed by external control of the FREQ_ADJ pin.

To reduce interference problems while using radio receiver tuned within the AM band, change the switching frequency from nominal to higher values. Choose these values so that the nominal and the higher value switching frequencies together results in the fewest cases of interference throughout the AM band. Select the oscillator frequency by changing the FREQ_ADJ resistor value connected to GND in Primary mode, according to the description in the *节 7.3*.

For peripheral mode operation, turn off the oscillator by pulling the FREQ_ADJ pin to AVDD. Doing so configures the OSC_I/O pins as inputs to be controlled from an external differential clock. In a multiple device system, inter-channel delay is automatically set up between the switching of the audio channels, which can be illustrated by no idle channels switching at the same time. Doing so will not influence the audio output, but only the switch timing to minimize noise coupling between audio channels through the power supply to optimize audio performance and to get better operating conditions for the power supply. The inter-channel delay will be set up for a peripheral device depending on the polarity of the OSC_I/O connection such that a secondary is selected by connecting the primary device OSC_I/O to the secondary device OSC_I/O with same polarity (+ to + and - to -), and tertiary is selected with the inverse polarity (+ to - and - to +).

9.3.5 Input Impedance

The TPA3223 input stage is a fully differential input stage and the input impedance changes with the gain setting from 7.3 kΩ at 36 dB gain to 48 kΩ at 20 dB gain. 表 9-2 lists the values from min to max gain. The tolerance of the input resistor value is ±20 % so the minimum value is higher than 5.8 kΩ. The inputs need to be AC-coupled to minimize the output DC-offset and ensure correct ramping of the output voltages during power-ON and power-OFF. The input ac-coupling capacitor together with the input impedance forms a high-pass filter with the following cut-off frequency:

If a flat bass response is required down to 20 Hz, then the recommended cut-off frequency is a tenth of that, which is 2 Hz. 表 9-2 lists the recommended ac-couplings capacitors for each gain step. If a -3 dB in frequency response is accepted at 20 Hz, then 10 times lower capacitors can be used – for example, a 1 µF can be used.

表 9-2. Recommended Input AC-Coupling Capacitors

Gain	Input Impedance	Input AC-Coupling Capacitance	Input High Pass Filter
20 dB	48 kΩ	4.7 µF	0.7 Hz
23.5 dB	24 kΩ	10 µF	0.7 Hz
32 dB	12 kΩ	10 µF	1.3 Hz
36 dB	7.3 kΩ	10 µF	2.2 Hz

Use an input capacitors with low leakage, like quality electrolytic, tantalum, film or ceramic. If a polarized type of input capacitor is used, then place the positive connection such that the capacitor has a positive DC bias.

9.3.6 Error Reporting

The $\overline{\text{FAULT}}$, and $\overline{\text{OTW\_CLIP}}$, pins are active-low, open-drain outputs. The $\overline{\text{FAULT}}$ function is for protection-mode signaling to a system-control device. Any fault resulting in device shutdown is signaled by the $\overline{\text{FAULT}}$ pin going low. Also, $\overline{\text{OTW\_CLIP}}$ goes low when the device junction temperature exceeds 125°C (see 表 9-3).

表 9-3. Error Reporting

FAULT	OTW_CLIP [1]	DESCRIPTION
0	0	Overtemperature (OTE), overload (OLP), undervoltage (UVP) or overvoltage (OVP). Junction temperature higher than 125°C (overtemperature warning).
0	1	Overload (OLP), undervoltage (UVP), overvoltage (OVP). Junction temperature lower than 125°C
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

(1) Static value. OTW_CLIP is static low when OTW is asserted, and toggling when output signal is CLIP

备注

Asserting RESET low forces the FAULT signal high, independent of faults being present. TI recommends monitoring the OTW_CLIP signal using the system microcontroller and responding to an overtemperature warning signal by turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both FAULT and OTW_CLIP outputs.

9.4 Device Functional Modes

TPA3223 can be configured in either a stereo BTL (Bridge Tied Load) mode, mono BTL mode (only one output BTL channel active), or in a mono PBTL (Parallel Bridge Tied Load) mode. In PBTL mode the two output BTL channels are paralleled with double output current available. The paralleling of the two BTL outputs must be made after the output LC filter.

See 表 6-2 for mode configuration setup.

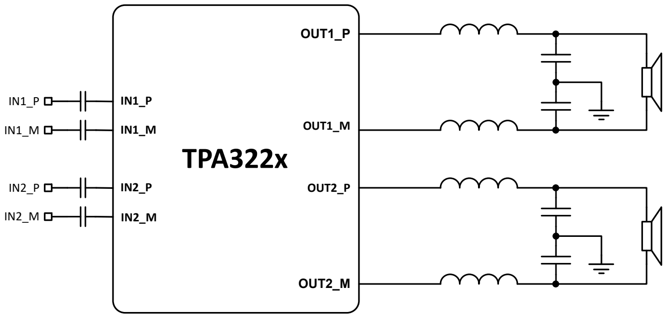


图 9-10. Stereo BTL

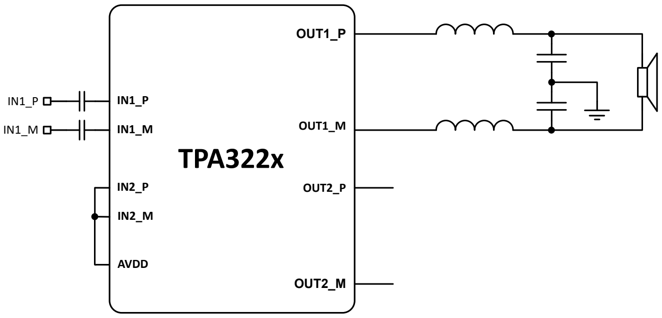


图 9-11. Mono BTL

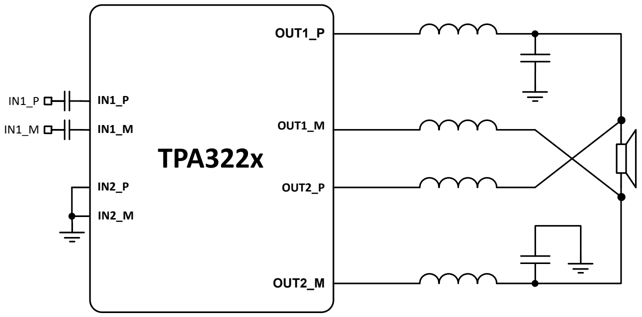


图 9-12. Mono PBTL, Post LC Filter

9.4.1 Powering Up

The TPA3223 does not require a power-up sequence because of the integrated undervoltage protection (UVP), but TI recommends to hold RESET low until PVDD supply voltage is stable to avoid audio artifacts. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply (GVDD) and AVDD voltages are above their UVP voltage thresholds (see the 节 7.5 table of this data sheet). Doing so allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pull-down of the half-bridge output as well as initiating a controlled ramp up sequence of the output voltage.

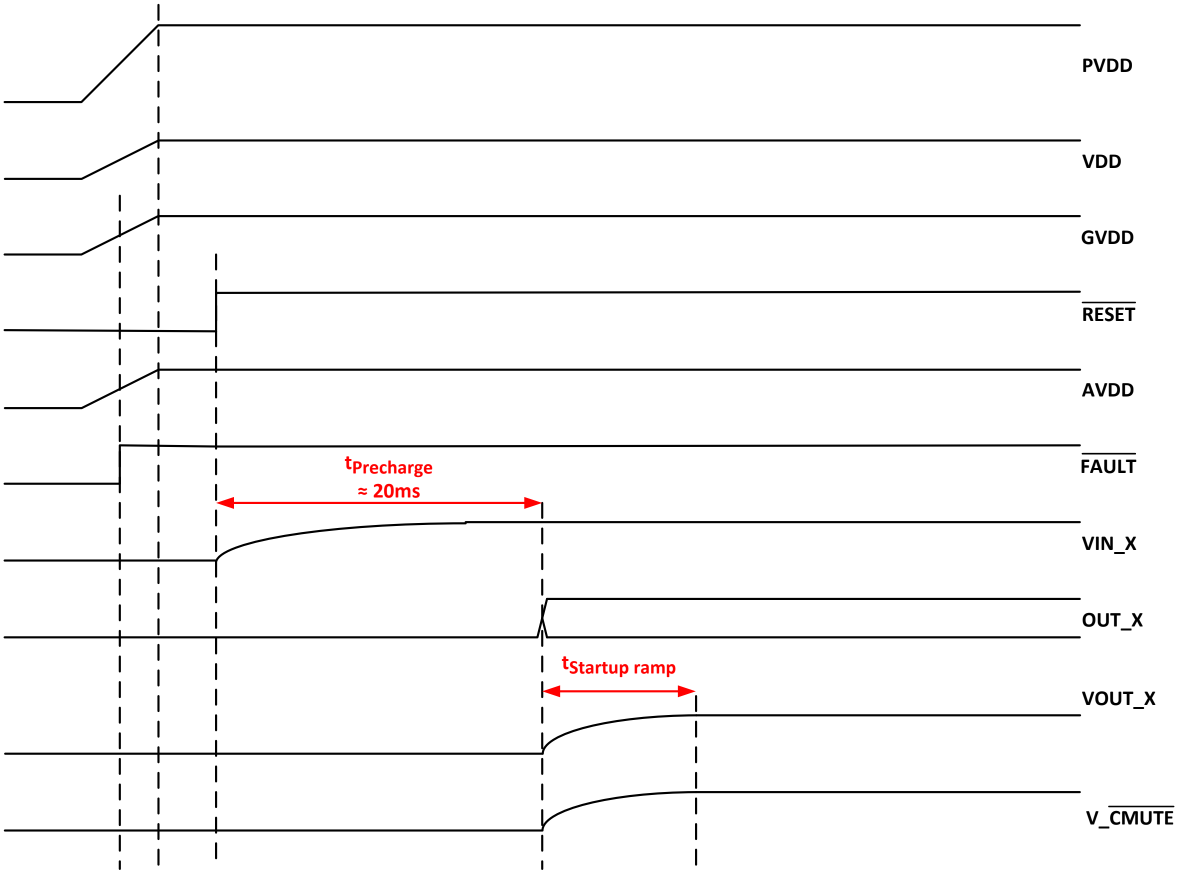


图 9-13. Startup Timing

When RESET is released to turn on TPA3223, FAULT signal turns low. FAULT stays low until AVDD reaches the undervoltage protection (UVP) voltage threshold (see the 节 7.5 table of this data sheet). After a pre-charge time to stabilize the DC voltage across the input AC coupling capacitors, the ramp up sequence starts and completes once the CMUTE node is charged to the final value.

9.4.1.1 Startup Ramp Time

During the startup ramp the CMUTE capacitor is charged by an internal current generator. With use of the recommended 33 nF CMUTE capacitor value, the startup ramp time is approximately 20 ms. Higher CMUTE capacitor value will increase the ramp time, and a lower value will decrease the ramp time. The recommended CMUTE capacitor value is selected for minimum audible artifacts during startup and shutdown ramp.

9.4.2 Powering Down

The TPA3223 does not require a power-down sequence. The device remains fully operational as long as the VDD, AVDD and PVDD voltages are above their undervoltage protection (UVP) voltage thresholds (see 节 7.5). Although not specifically required, TI recommends to hold RESET low during power down, thus preventing audible artifacts including pops or clicks by initiating a controlled ramp down sequence of the output voltage. The ramp down sequence will complete once the CMUTE node is discharged.

9.4.2.1 Power Down Ramp Time

During the power down ramp the $\overline{\text{CMUTE}}$ capacitor is discharged by internal circuitry. With use of the recommended 33 nF $\overline{\text{CMUTE}}$ capacitor value, the power-down ramp time is approximately 20 ms.

9.4.3 Device Reset

Asserting $\overline{\text{RESET}}$ low initiates the device ramp down. The output FETs go into a Hi-Z state after the ramp down is complete. Output pull downs are active in both BTL mode and PBTL mode with $\overline{\text{RESET}}$ low.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the $\overline{\text{RESET}}$ input low enables weak pull-down of the half-bridge outputs.

Asserting $\overline{\text{RESET}}$ low removes any fault information to be signaled on the $\overline{\text{FAULT}}$ output, that is, $\overline{\text{FAULT}}$ is forced high. A rising-edge transition on $\overline{\text{RESET}}$ allows the device to resume operation after a fault. To make sure of thermal reliability, the rising edge of $\overline{\text{RESET}}$ must occur no sooner than 4 ms after the falling edge of $\overline{\text{FAULT}}$.

The TPA3223 will enter a low power state once the ramp down sequence is complete.

9.4.4 Device Soft Mute

Asserting $\overline{\text{CMUTE}}$ low initiates the device soft mute function. The soft mute function initiates a ramp down sequence of the outputs, and the output FETs go into a Hi-Z state after the ramp down is complete. All internal circuits are powered while in soft mute state. External control of the soft mute function must provide high impedance output when not engaged (open drain output) to allow the $\overline{\text{CMUTE}}$ node to charge/discharge during device ramp up and ramp down when de-asserting and asserting $\overline{\text{RESET}}$.

9.4.5 Device Protection System

The TPA3223 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, overvoltage, and undervoltage. The TPA3223 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased. The device will handle errors, as shown in 表 9-4.

表 9-4. Device Protection

BTL MODE		PBTL MODE	
LOCAL ERROR IN	**TURNS OFF**	**LOCAL ERROR IN**	**TURNS OFF**
A	A+B	A	A+B+C+D
B		B	
C	C+D	C	
D		D	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective half-bridge (non-latching, does not assert $\overline{\text{FAULT}}$).

9.4.5.1 Overload and Short Circuit Current Protection

TPA3223 has fast reacting current sensors on all high-side and low-side FETs. To prevent output current from increasing beyond the overcurrent threshold, TPA3223 uses current limiting of the output current for each switching cycle (Cycle By Cycle Current Control, CB3C) in case of excess output current. CB3C prevents premature shutdown due to high output current transients caused by high level music transients and a drop of the real load impedance of the speaker, and allows the output current to be limited to a maximum programmed level. If the maximum output current persists, for example the power stage being overloaded with too low load impedance, then the device will shut down the affected output channel and the affected output is put in a high-impedance (Hi-Z) state until a $\overline{\text{RESET}}$ cycle is initiated. CB3C works individually for each full-bridge output. If an over current event is triggered, then the CB3C performs a state flip of the full-bridged output that is cleared upon beginning of next PWM frame.

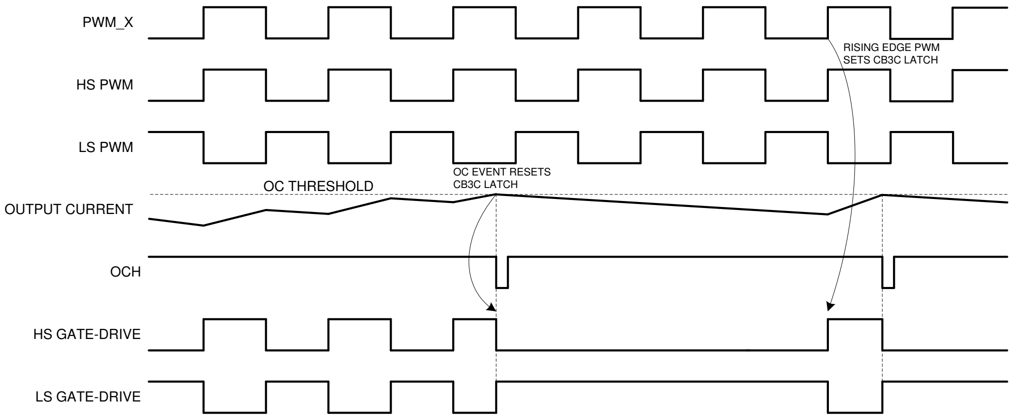


图 9-14. **CB3C Timing Example**

9.4.5.2 Signal Clipping and Pulse Injector

A built-in activity detector monitors the PWM activity of the OUT_X pins. TPA3223 is designed to drive unclipped output signals all the way to PVDD and GND rails. In case of audio signal clipping when applying excessive input signal voltage, or in case of CB3C current protection being active, the amplifier feedback loop of the audio channel will respond to this condition with a saturated state, and the output PWM signals will stop unless special circuitry is implemented to handle this situation. To prevent the output PWM signals from stopping in a clipping or CB3C situation, narrow pulses are injected to the gate drive to maintain output activity. The injected narrow pulses are injected at every 4th PWM frame, and thus the effective switching frequency during this state is reduced to 1/4 of the normal switching frequency.

Signal clipping is signaled on the $\overline{\text{OTW\_CLIP}}$ pin and is self clearing when signal level reduces and the device reverts to normal operation. The $\overline{\text{OTW\_CLIP}}$ pulses start at the onset to output clipping, typically at a THD level around 0.01%, resulting in narrow $\overline{\text{OTW\_CLIP}}$ pulses starting with a pulse width of approximately 500 ns.

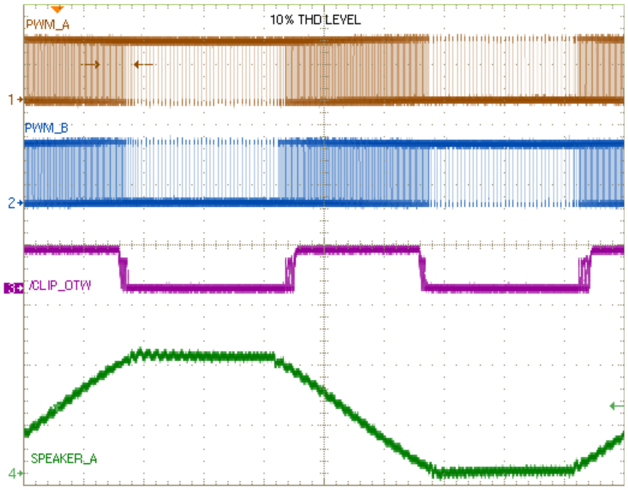


图 9-15. **Signal Clipping PWM and Speaker Output Signals**

9.4.5.3 DC Speaker Protection

The output DC protection scheme protects a speaker from excess DC current in case one terminal of the speaker is connected to the amplifier while the other is accidentally shorted to the chassis ground. Such a short circuit results in a DC voltage of PVDD/2 across the speaker, which potentially can result in destructive current levels. The output DC protection detects any unbalance of the output and input current of a BTL or PBTL output configuration (current into/out of one half-bridge equals current out of/into the other half-bridge), and in the event of the imbalance exceeding a programmed threshold, the overload counter increments until the maximum value and the affected output channel is shut down. DC Speaker Protection is enabled in both BTL and PBTL mode operation.

9.4.5.4 Pin-to-Pin Short Circuit Protection (PPSC)

The PPSC detection system protects the device from permanent damage in the case that a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup after $\overline{\text{RESET}}$ is pulled high. When PPSC detection is activated by a short on the output, all half-bridges are kept in a Hi-Z state until the short is removed; the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is < 15 ms/μF. While the PPSC detection is in progress, $\overline{\text{FAULT}}$ is kept low. If no shorts are present, then the PPSC detection passes, and $\overline{\text{FAULT}}$ is released. A device reset will start a new PPSC detection. PPSC detection is enabled in both BTL and PBTL output configurations. To ensure not to trip the PPSC detection system, TI recommends not to insert a resistive load to GND_X or PVDD_X.

9.4.5.5 Overtemperature Protection OTW and OTE

TPA3223 has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{\text{OTW\_CLIP}}$) when the device junction temperature exceeds 125°C (typical). If the device junction temperature exceeds 155°C (typical), then the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{\text{RESET}}$ must be asserted. Thereafter, the device resumes normal operation.

9.4.5.6 Undervoltage Protection (UVP), Overvoltage Protection (OVP), and Power-on Reset (POR)

The UVP, OVP and POR circuits of the TPA3223 fully protect the device in any power-up/down and brownout situation, and also in overvoltage situation with PVDD not exceeding the values stated in 节 7.1. While powering up, the POR circuit ensures that all circuits are fully operational when the AVDD supply voltage reaches the value stated in *节 7.5*. Although AVDD is independently monitored, a supply voltage drop below the UVP threshold on AVDD pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state. The device automatically resumes operation when all supply voltages have increased above their UVP threshold. In case of an OVP event, all half-bridge outputs are immediately set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ is asserted low until PVDD is below the OVP threshold.

9.4.5.7 Fault Handling

If a fault situation occurs while in operation, then the device acts accordingly to the fault being a global or a channel fault. A global fault is a chip-wide fault situation and causes all PWM activity of the device to be shut down, and asserts FAULT low. A global fault is a latching fault and clearing FAULT and restarting operation requires resetting the device by toggling RESET. De-asserting RESET is never allowed with excessive system temperature, so TI recommends to monitor RESET with a system microcontroller and only release RESET (RESET high) if the OTW_CLIP signal is cleared (high). A channel fault results in shutdown of the PWM activity of the affected channels.

备注

Asserting RESET low forces the FAULT signal high, independent of faults being present.

表 9-5. Error Reporting

Fault/Event	Fault/Event Description	Global or Channel	Reporting Method	Latched/Self Clearing	Action needed to Clear	Output FETs
PVDD_X UVP	Voltage Fault	Global	FAULT pin	Self Clearing	Increase affected supply voltage	HI-Z
PVDD_X OVP					Decrease affected supply voltage	
AVDD UVP					Increase affected supply voltage	
POR (AVDD UVP)	Power On Reset	Global	FAULT pin	Self Clearing	Allow AVDD to rise	HI-Z
OTW	Thermal Warning	Global	OTW_CLIP pin	Self Clearing	Cool below OTW threshold	Normal operation
OTE	Thermal Shutdown	Global	FAULT pin	Latched	Toggle RESET	HI-Z
OLP (CB3C>2.1 ms)	OC Shutdown	Channel	FAULT pin	Latched	Toggle RESET	HI-Z
CB3C	OC Limiting	Channel	None	Self Clearing	Reduce signal level or remove short	Flip state, cycle by cycle at fs/3
Stuck at Fault(1)	No OSC_IO activity in Peripheral Mode	Global	None	Self Clearing	Resume OSC_IO activity	HI-Z

(1) Stuck at Fault occurs when input OSC_IO input signal frequency drops below minimum frequency given in the *Electrical Characteristics* table of this data sheet.

10 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

10.1 Application Information

TPA3223 can be configured either in stereo BTL, mono BTL or mono PBTL mode depending on output power conditions and system design.

10.2 Typical Applications

10.2.1 Stereo BTL Application

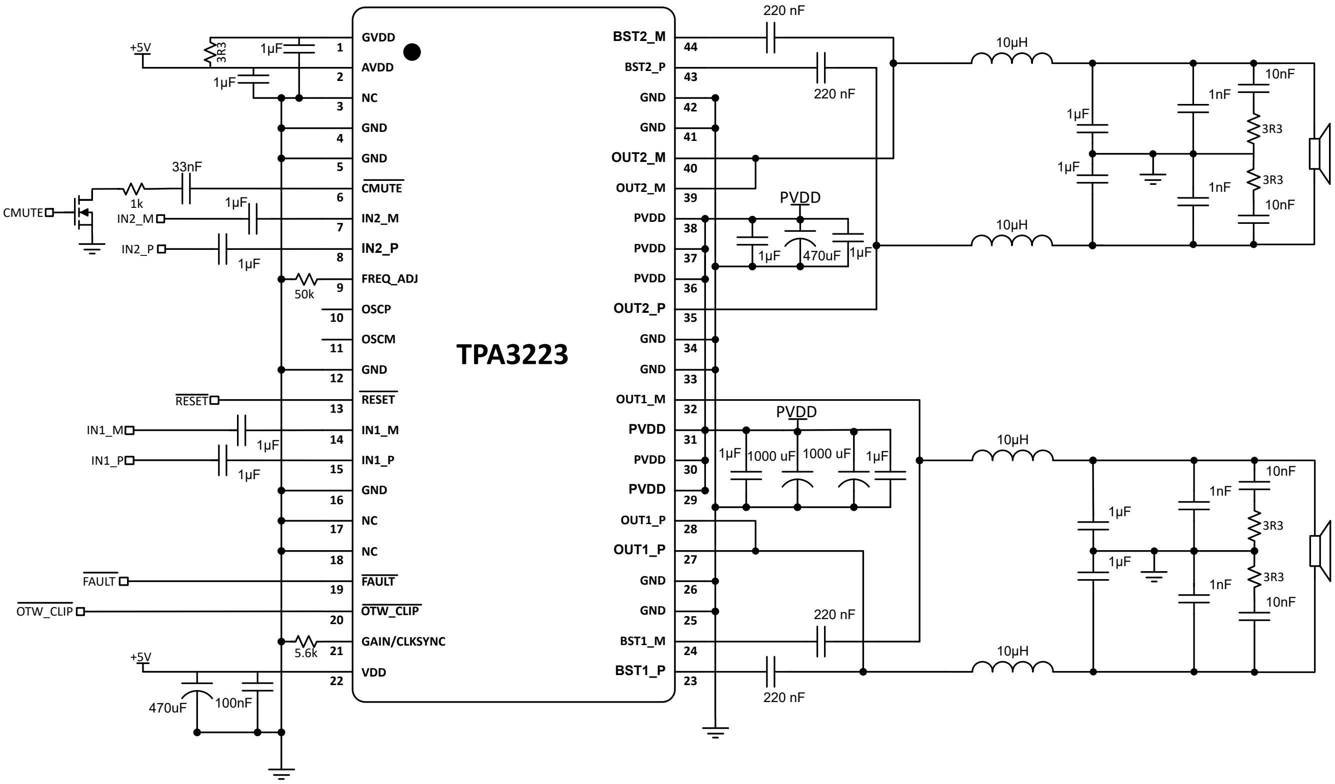


图 10-1. Typical Differential (2N) AD-Mode BTL Application

10.2.1.1 Design Requirements

For this design example, use the parameters in 表 10-1.

表 10-1. Design Requirements, BTL Application

DESIGN PARAMETER	EXAMPLE
Low Power Supply	5 V
High Power Supply	10 - 42 V
Analog Inputs	IN1_M = ±2.8V (peak, max)
	IN1_P = ±2.8V (peak, max)
	IN2_M = ±2.8V (peak, max)
	IN2_P = ±2.8V (peak, max)
Output Filters	Inductor-Capacitor Low Pass Filter (10 µH + 1 µF)
Speaker Impedance	3.5 - 8 Ω

10.2.1.2 Detailed Design Procedures

A rising-edge transition on $\overline{\text{RESET}}$ input allows the device to execute the startup sequence and start switching.

A toggling $\overline{\text{OTW\_CLIP}}$ signal is indicating that the output is approaching clipping. The signal can be used either to decrease audio volume or to control an intelligent power supply nominally operating at a low rail adjusting to a higher supply rail.

The device inverts the audio signal from input to output.

10.2.1.2.1 Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, use X7R in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This is particularly true in the selection of the 1 µF capacitor that is placed on the power supply to each full-bridge. The capacitor must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 75 V is required for use with a 42 V power supply.

10.2.1.2.2 PVDD Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. Select these capacitors for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, two 1000 µF capacitors, 75 V supports most applications. Use PVDD capacitors with low ESR type because they are used in a circuit associated with high-speed switching.

10.2.1.2.3 BST capacitors

To make sure of a large enough bootstrap energy storage for the high side gate drive to work correctly with all audio source signals, 33 nF / 50 V X7R BST capacitors are recommended.

10.2.1.2.4 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper is recommended for use with the TPA3223. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin due to lower PCB trace inductance.

10.2.2 Application Curves

Relevant performance plots for TPA3223 in BTL configuration are shown in *节 7.8*

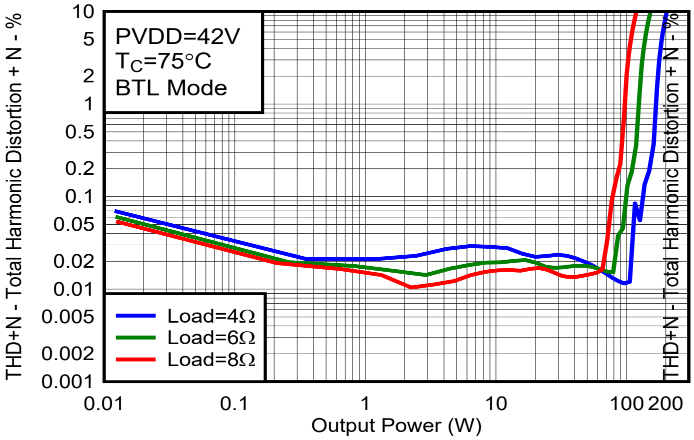


图 10-2. Total Harmonic Distortion + Noise vs Output Power

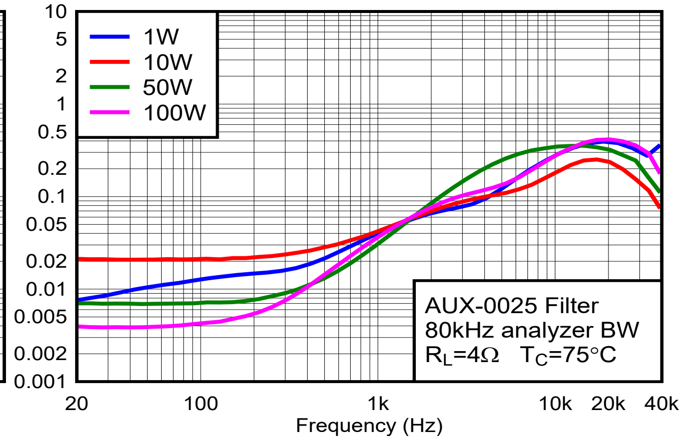


图 10-3. Total Harmonic Distortion+Noise vs Frequency

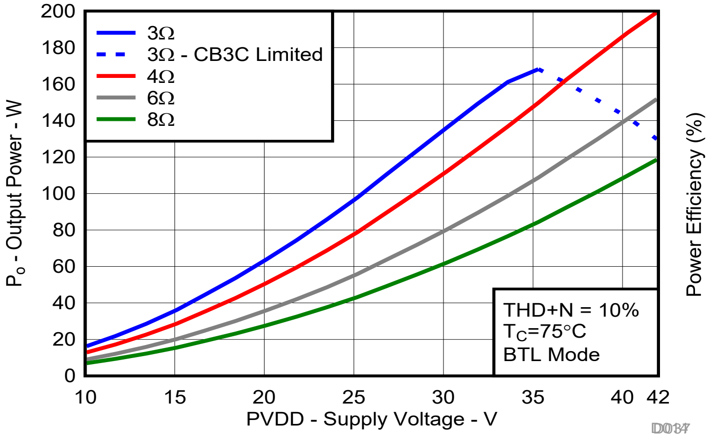


图 10-4. Output Power vs Supply Voltage, AD-mode

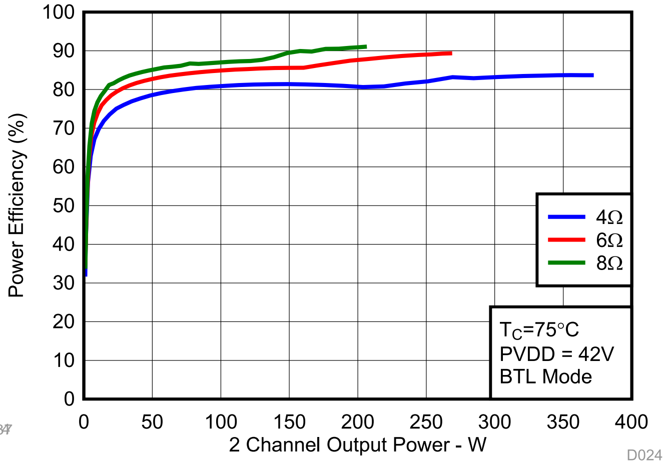


图 10-5. System Efficiency vs Output Power

10.2.3 Typical Application, Differential (2N), AD-Mode PBTL (Outputs Paralleled after LC filter)

TPA3223 can be configured in mono PBTL mode by paralleling the outputs before the LC filter (see) or after the LC filter. Paralleled outputs after the LC filter can be preferred if a single board design must support both PBTL and BTL, or in the case multiple, smaller paralleled inductors are preferred due to size or cost. Paralleling after the LC filter requires four inductors, one for each OUT_x. This section shows an example of paralleled outputs after the LC filter.

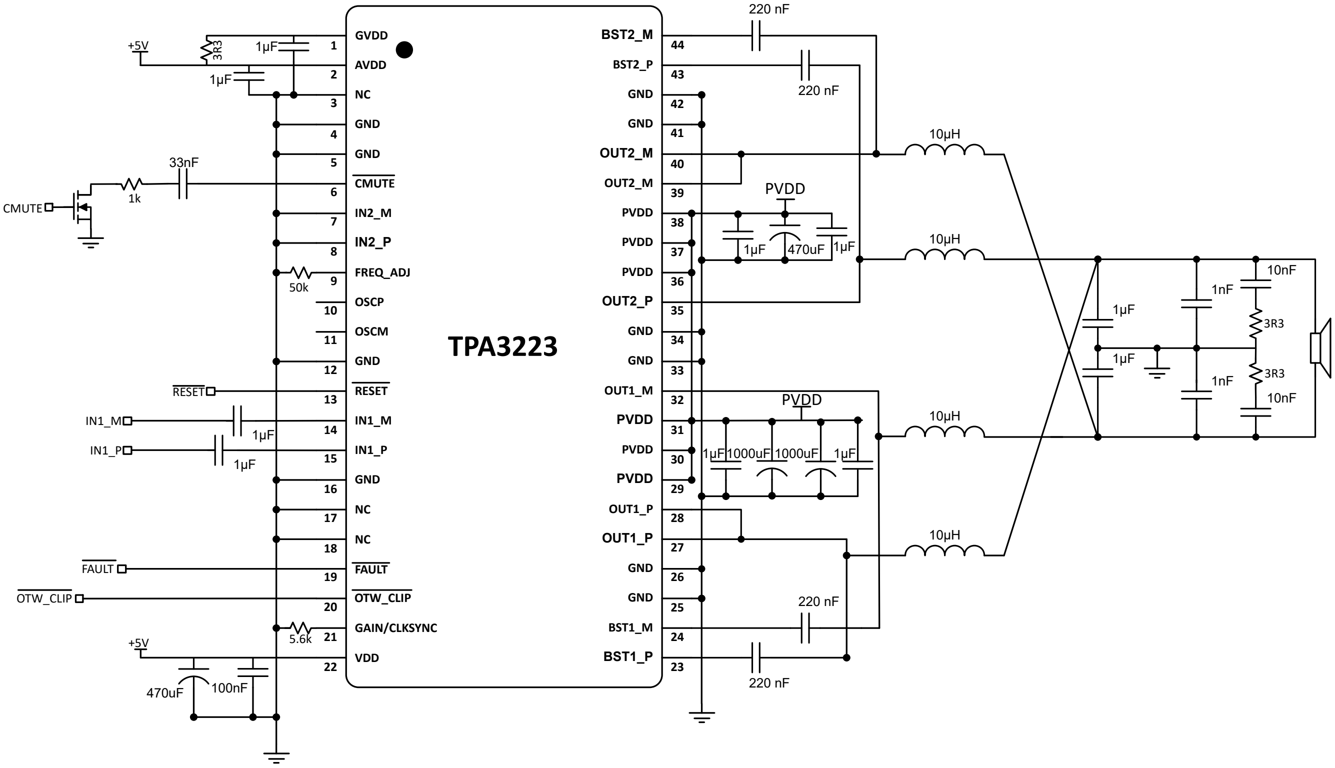


图 10-6. Typical Differential (2N) AD-Mode PBTL Application

10.2.3.1 Design Requirements

Refer to 节 10.2.1 for the Design Requirements.

表 10-2. Design Requirements, PBTL Application

DESIGN PARAMETER	EXAMPLE
Low Power Supply	5 V
High Power Supply	10 - 42 V
Analog Inputs	IN1_M = ±2.8 V (peak, max)
	IN1_P = ±2.8 V (peak, max)
	IN2_M = Grounded
	IN2_P = Grounded
Output Filters	Inductor-Capacitor Low Pass Filter (10 µH + 1 µF)
Speaker Impedance	2 - 4 Ω

10.3 Power Supply Recommendations

10.3.1 Power Supplies

The TPA3223 device requires an external power supply for PVDD to power the output stage of the speaker amplifier and the associated circuitry.

An external power supply must be connected to GVDD, AVDD and VDD to power the gate-drive and other internal digital and analog circuit blocks in the device.

The allowable voltage range for both the PVDD and GVDD/AVDD/VDD supplies are listed in *节 7.3*. Ensure both the PVDD and the GVDD/AVDD/VDD supplies can deliver more current than listed in *节 7.3*.

10.3.1.1 VDD Supply

An external 5 V power supply needs to be connected to VDD, AVDD and GVDD.

Proper connection, routing, and decoupling techniques are highlighted in the TPA3223 EVM User's Guide (as well as *节 10.1* and *节 10.4.2*) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3223 device EVM User's Guide, which followed the same techniques as those shown in *节 10.1*, may result in reduced performance, errant functionality, or even damage to the TPA3223 device.

10.3.1.2 AVDD and GVDD Supplies

AVDD and GVDD can be supplied through an external 5 V power supply to power internal analog and digital circuits and the gate-drivers for the output H-bridges. Proper connection, routing, and decoupling techniques are highlighted in the TPA3223 device EVM User's Guide (as well as *节 10.1* and *节 10.4.2*) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3223 device EVM User's Guide, which followed the same techniques as those shown in *节 10.1* may result in reduced performance, errant functionality, or even damage to the TPA3223 device.

10.3.1.3 PVDD Supply

The output stage of the speaker amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TPA3223 device EVM User's Guide (as well as *节 10.1* and *节 10.4.2*) and must be followed as closely as possible for proper operation and performance. Due to the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TPA3223 device EVM User's Guide. The lack of proper decoupling, like that shown in the EVM User's Guide, can result in voltage spikes which can damage the device, or cause poor audio performance and device shutdown faults.

10.3.1.4 BST Supply

TPA3223 has built-in bootstrap supply for each half bridge gate drive to supply the high side MOSFETs, only requiring a single capacitor per half bridge. The capacitors are connected to each half bridge output, and are charged by the GVDD supply via an internal diode while the PWM outputs are in low state. The high side gate drive is supplied by the voltage across the BST capacitor while the output PWM is high. It is recommended to place the BST capacitors close to the TPA3223 device, and to keep PCB routing traces at minimum length.

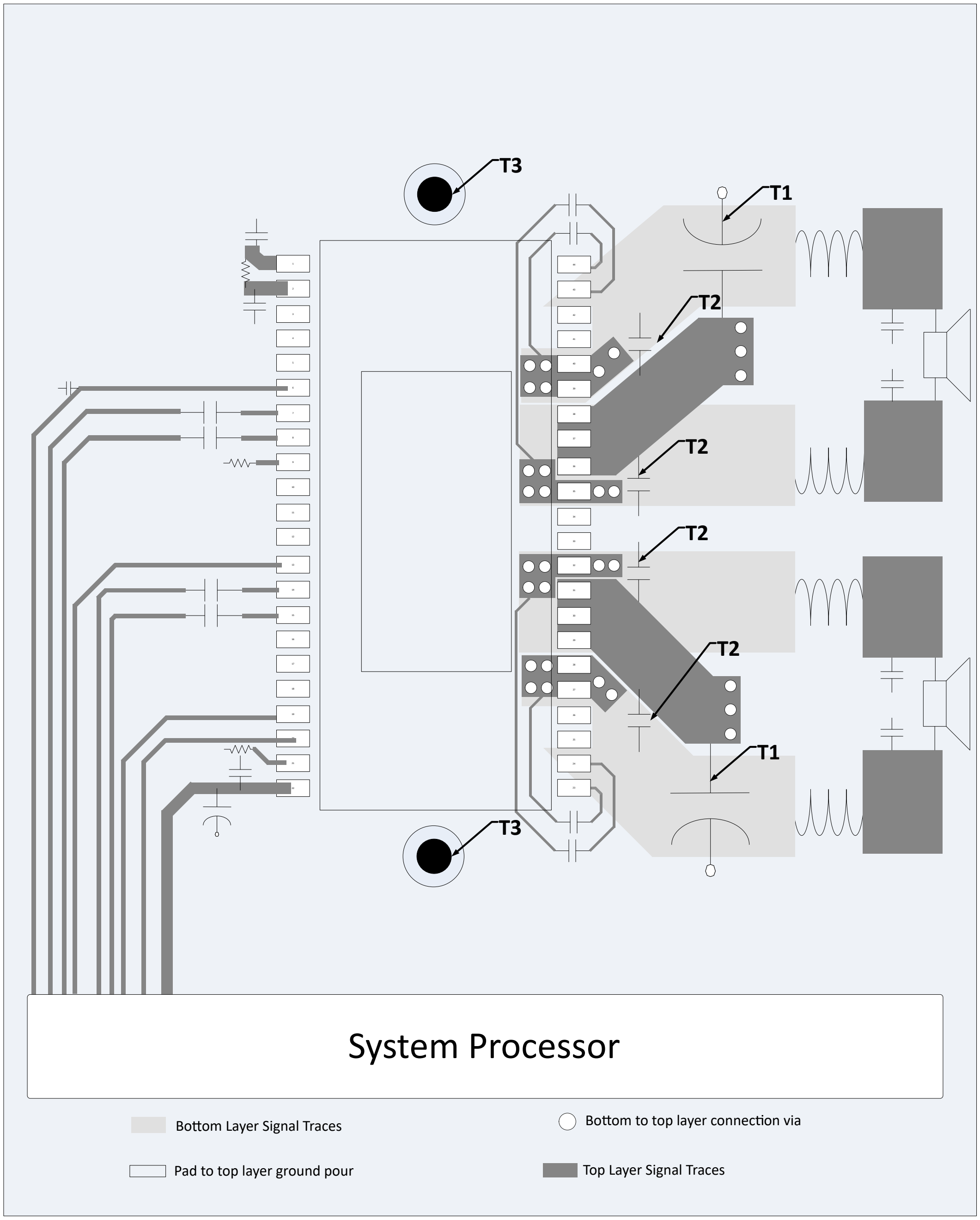
10.4 Layout

10.4.1 Layout Guidelines

- Use an unbroken ground plane to have good low impedance and inductance return path to the power supply for power and audio signals.
- Maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible, since the ground pins are the best conductors of heat in the package.
- PCB layout, audio performance and EMI are linked closely together.
- Routing the audio input should be kept short and together with the accompanied audio source ground.
- The small bypass capacitors on the PVDD lines should be placed as close to the PVDD pins as possible.
- A solid local ground area underneath the device is important to minimize ground bounce.
- Orient the passive component so that the narrow end of the passive component is facing the TPA3223 device, unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads.
- Avoid placing other heat producing components or structures near the TPA3223 device.
- Avoid cutting off the flow of heat from the TPA3223 device to the surrounding ground areas with traces or via strings, especially on output side of device.

10.4.2 Layout Examples

10.4.2.1 BTL Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces must be GND copper pour (transparent on example image)

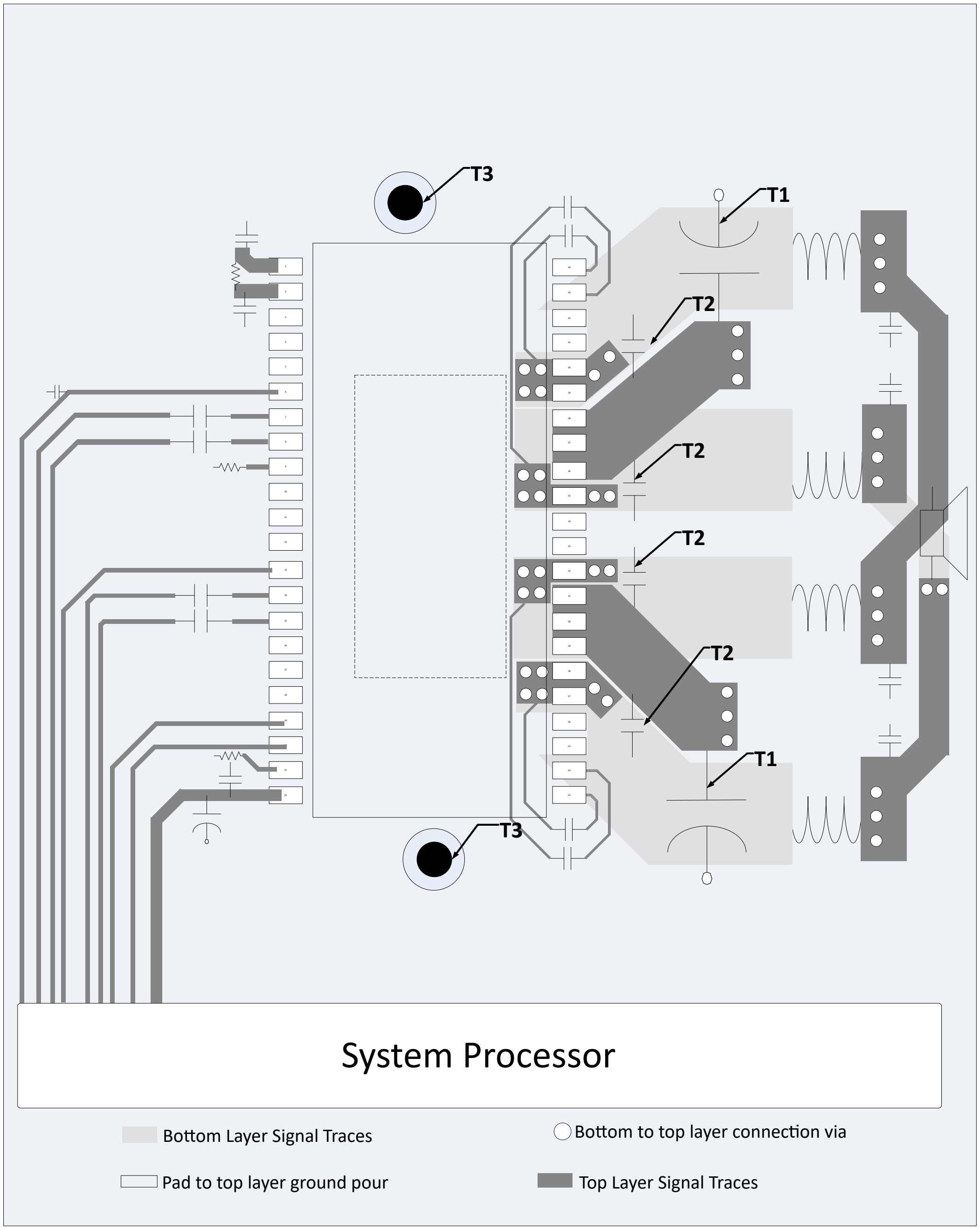
B. **Note T1**: PVDD decoupling bulk capacitors must be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces must be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces must be blocking the current path.

C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **Note T3**: Heat sink needs to have a good connection to PCB ground.

图 10-7. BTL Application Printed Circuit Board - Composite

10.4.2.2 PBTL (Outputs Paralleled after LC filter) Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces must be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces must be blocking the current path.

C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **Note T3**: Heat sink needs to have a good connection to PCB ground.

图 10-8. PBTL (Outputs Paralleled after LC filter) Application Printed Circuit Board - Composite

11 Device and Documentation Support

11.1 Documentation Support

- TPA3223 Evaluation Module User's Guide
- Multi-Device Configuration for TPA32xx Amplifiers

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document

11.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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Wi-Fi™ is a trademark of Wi-Fi Alliance.
TI E2E™ is a trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3223DDVR	ACTIVE	HTSSOP	DDV	44	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	3223	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

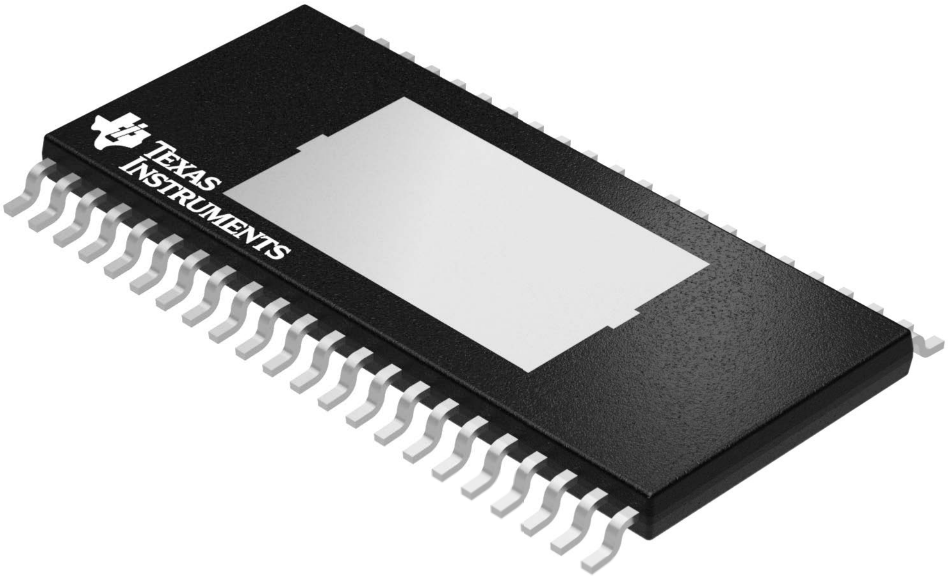
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

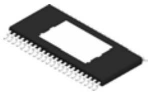
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

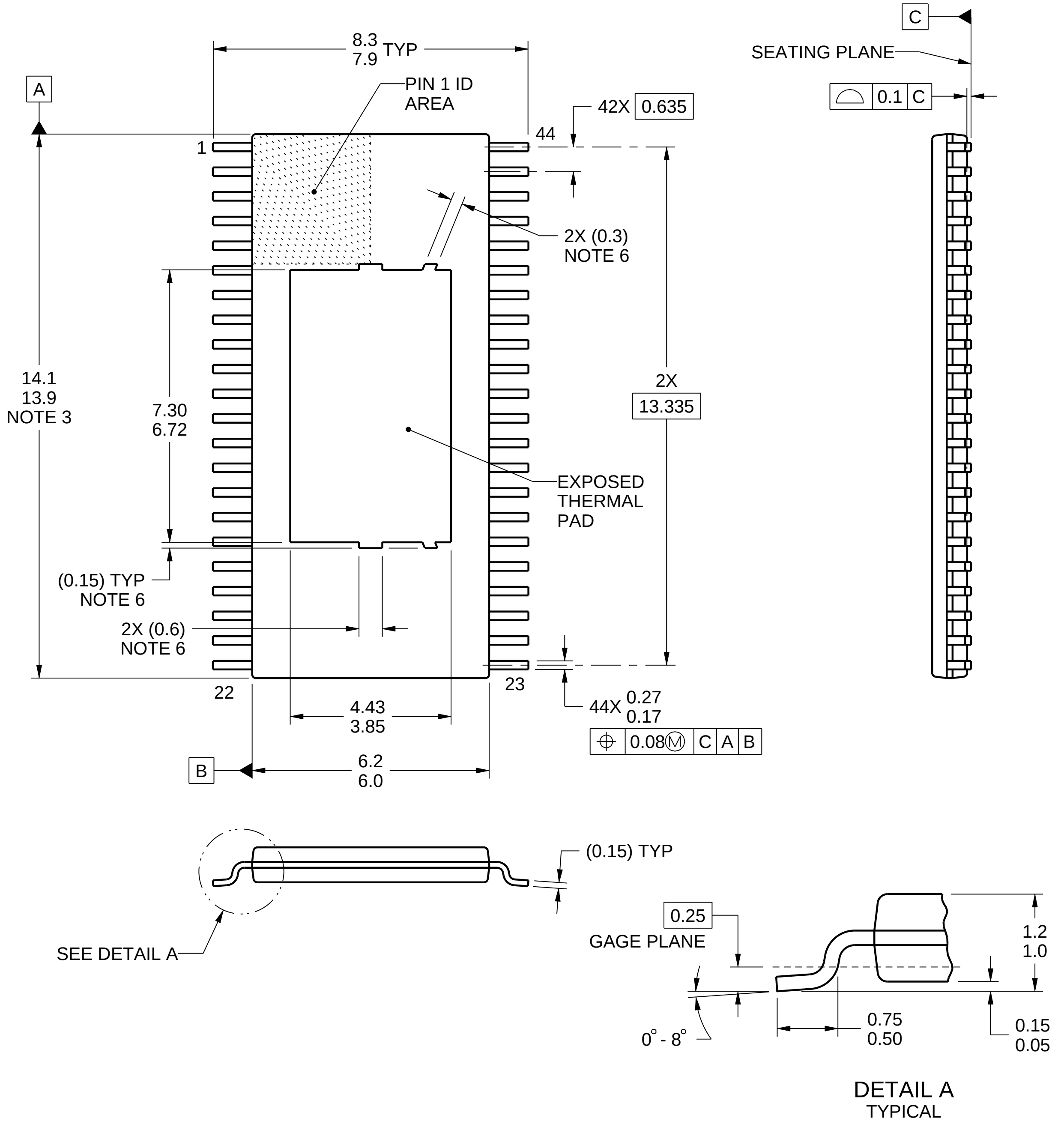


PACKAGE OUTLINE

DDV0044D

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



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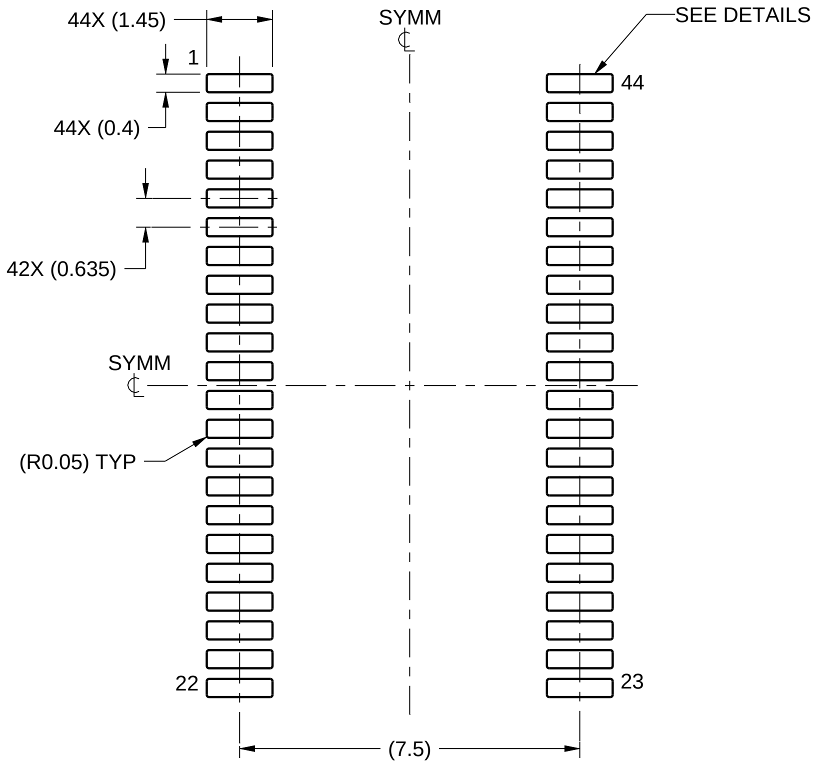
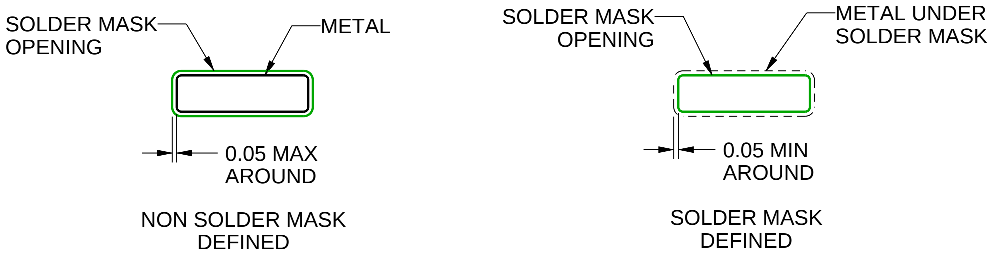
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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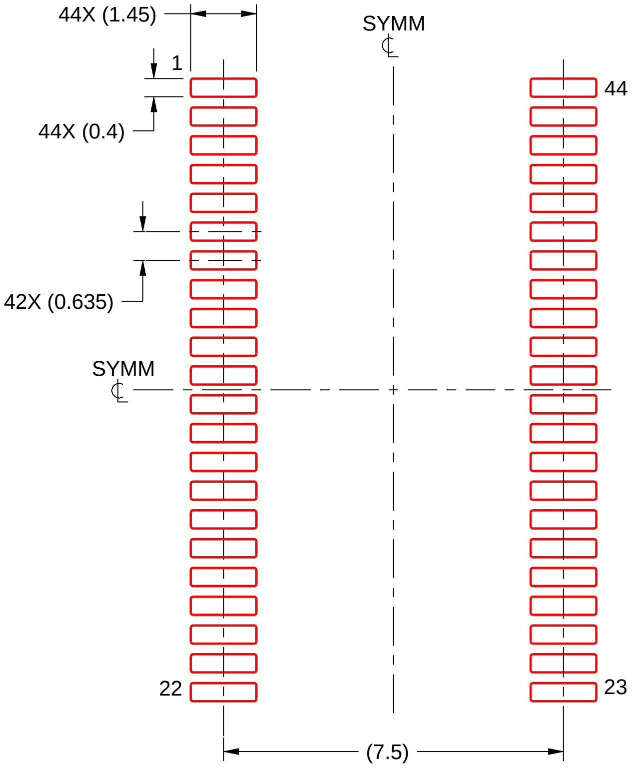
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE :6X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265