

# TMUX7236 具有闩锁效应抑制和 1.8V 逻辑电平的双通道精密开关

## 1 特性

- 闩锁效应抑制
- 双电源电压范围：±4.5 V 至 ±22 V
- 单电源电压范围：4.5 V 至 44 V
- 低导通电阻：2 Ω
- 高电流支持：330 mA (最大值) (WQFN)
- -40°C 至 +125°C 工作温度
- 兼容 1.8 V 逻辑电平
- 逻辑引脚上具有集成的下拉电阻器
- 失效防护逻辑
- 轨至轨运行
- 双向运行

## 2 应用

- 燃气表
- 流量变送器
- 工厂自动化和工业控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- 半导体测试
- 数据采集系统
- 超声波扫描仪
- 光纤网络
- 光学测试设备
- 远程无线电单元
- 有线网络
- 患者监护和诊断

## 3 说明

TMUX7236 是一款具有闩锁效应抑制特性的互补金属氧化物半导体 (CMOS) 开关，采用双通道 2:1 配置。该器件在双电源 (±5V 至 ±22V)、单电源 (5V 至 44V) 或非对称电源 (例如  $V_{DD} = 12V$ ,  $V_{SS} = -5V$ ) 供电时均能正常运行。TMUX7236 可在源极 (Sx) 和漏极 (D) 引脚上支持从  $V_{SS}$  到  $V_{DD}$  范围的双向模拟和数字信号。

所有逻辑控制输入均支持 1.8V 到  $V_{DD}$  的逻辑电平，当器件在有效电源电压范围内运行时，可实现 TTL 和 CMOS 逻辑兼容性。失效防护逻辑电路允许先在控制引脚上施加电压，然后在电源引脚上施加电压，从而保护器件免受潜在的损害。

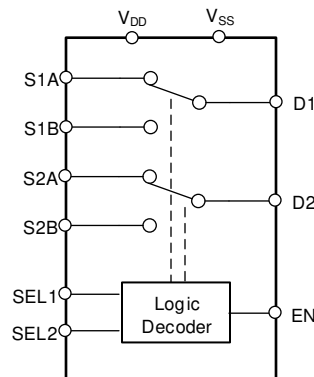
TMUX72xx 系列具有闩锁效应抑制特性，可防止器件内寄生结构之间通常由过压事件引起的大电流不良事件。闩锁状态通常会一直持续到电源轨关闭为止，并可能导致器件故障。闩锁效应抑制特性使得 TMUX72xx 系列开关和多路复用器能够在恶劣的环境中使用。

### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>
TMUX7236	RUM (WQFN, 16)	4mm × 4mm
	PW (TSSOP, 16)	5mm × 6.4mm

(1) 有关详细信息，请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



方框图



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## 4 Pin Configuration and Functions

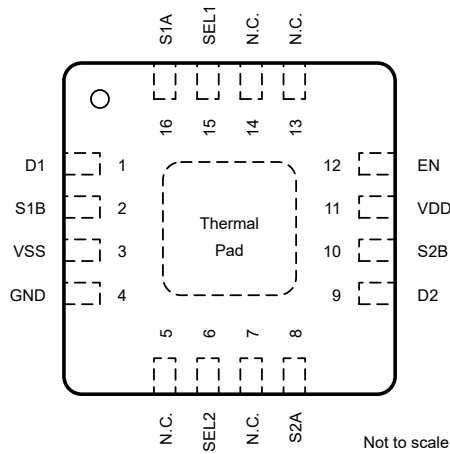


图 4-1. RUM Package, 16-Pin WQFN (Top View)

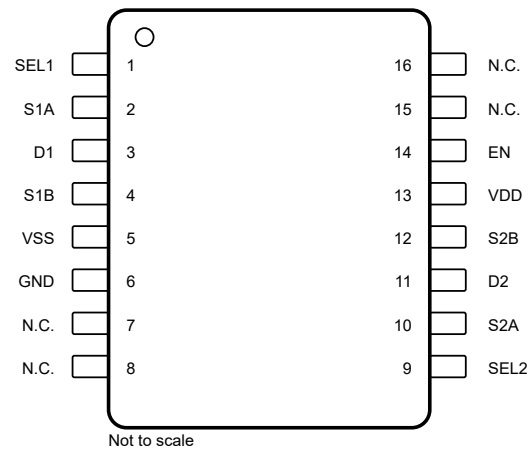


图 4-2. PW Package, 16-Pin TSSOP (Top View)

表 4-1. Pin Functions

PIN			TYPE <sup>(1)</sup>	DESCRIPTION
NAME	TSSOP	WQFN		
D1	3	1	I/O	Drain pin. Can be an input or output.
D2	11	9	I/O	Drain pin. Can be an input or output.
GND	6	4	P	Ground (0 V) reference
NC	7, 8, 15, 16	5, 7, 13, 14	—	No internal connection. Can be shorted to GND or left floating.
S1A	2	16	I/O	Source pin 1A. Can be an input or output.
S1B	4	2	I/O	Source pin 1B. Can be an input or output.
S2A	10	8	I/O	Source pin 2A. Can be an input or output.
S2B	12	10	I/O	Source pin 2B. Can be an input or output.
EN	14	12	I	Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on.
SEL1	1	15	I	Logic control input, has internal pull-down resistor. Controls the switch connection as shown in 节 7.4.
SEL2	9	6	I	Logic control input, has internal pull-down resistor. Controls the switch connection as shown in 节 7.4.
V <sub>DD</sub>	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 $\mu$ F to 10 $\mu$ F between V <sub>DD</sub> and GND.
V <sub>SS</sub>	5	3	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 $\mu$ F to 10 $\mu$ F between V <sub>SS</sub> and GND.
Thermal Pad			—	The thermal pad is not connected internally. There is no requirement to electrically connect this pad. If connected, however, it is recommended that the pad be left floating or tied to GND.

(1) I = input, O = output, P = power

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		48	V
$V_{DD}$		- 0.5	48	V
$V_{SS}$		- 48	0.5	V
$V_{SEL}$ or $V_{EN}$	Logic control input pin voltage (SELx)	- 0.5	48	V
$I_{SEL}$ or $I_{EN}$	Logic control input pin current (SELx)	- 30	30	mA
$V_S$ or $V_D$	Source or drain voltage (Sx, Dx)	$V_{SS} - 0.5$	$V_{DD} + 0.5$	V
$I_{IK}$	Diode clamp current <sup>(3)</sup>	- 30	30	mA
$I_S$ or $I_D$ (CONT)	Source or drain continuous current (Sx, Dx)		$I_{DC} + 10\%$ <sup>(4)</sup>	mA
$T_A$	Ambient temperature	- 55	150	°C
$T_{stg}$	Storage temperature	- 65	150	°C
$T_J$	Junction temperature		150	°C
$P_{tot}$	Total power dissipation (QFN) <sup>(5)</sup>		1650	mW
$P_{tot}$	Total power dissipation (TSSOP) <sup>(5)</sup>		720	mW

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (4) Refer to *Source or Drain Continuous Current* table for  $I_{DC}$  specifications.
- (5) For QFN package:  $P_{tot}$  derates linearly above  $T_A = 70^\circ\text{C}$  by  $24.2\text{mW}/^\circ\text{C}$ .

### 5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TMUX7236		UNIT
		RUM (WQFN)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.5	97.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	25.1	25.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.5	44.1	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.3	1.1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	16.4	43.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.9	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ <sup>(1)</sup>	Power supply voltage differential	4.5		44	V
$V_{DD}$	Positive power supply voltage	4.5		44	V
$V_S$ or $V_D$	Signal path input/output voltage (source or drain pin) (Sx, D)	$V_{SS}$		$V_{DD}$	V
$V_{SEL}$ or $V_{EN}$	Address or enable pin voltage	0		44	V
$I_S$ or $I_D (CONT)$	Source or drain continuous current (Sx, D)			$I_{DC}$ <sup>(2)</sup>	mA
$T_A$	Ambient temperature	- 40		125	°C

(1)  $V_{DD}$  and  $V_{SS}$  can be any value as long as  $4.5\text{ V} \leq (V_{DD} - V_{SS}) \leq 44\text{ V}$ , and the minimum  $V_{DD}$  is met.

(2) Refer to *Source or Drain Continuous Current* table for  $I_{DC}$  specifications.

## 5.5 Source or Drain Continuous Current

at supply voltage of  $V_{DD} \pm 10\%$ ,  $V_{SS} \pm 10\%$  (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL ( $I_{DC}$ ) <sup>(2)</sup>		$T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$	$T_A = 125^\circ\text{C}$	UNIT
PACKAGE	TEST CONDITIONS				
PW (TSSOP)	+44 V Dual Supply <sup>(1)</sup>	470	300	165	mA
	±15 V Dual Supply	455	300	165	mA
	+12 V Single Supply	355	240	145	mA
	±5 V Dual Supply	335	225	140	mA
RUM (WQFN)	+44 V Single Supply <sup>(1)</sup>	650	400	180	mA
	±15 V Dual Supply	650	400	180	mA
	+12 V Single Supply	500	310	170	mA
	±5 V Dual Supply	450	290	160	mA

(1) Specified for nominal supply voltage only.

(2) Refer to Total power dissipation ( $P_{tot}$ ) limits in *Absolute Maximum Ratings* table that must be followed with max continuous current specification.

## 5.6 ±15 V Dual Supply: Electrical Characteristics

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ , GND = 0 V (unless otherwise noted)

Typical at  $V_{DD} = +15\text{ V}$ ,  $V_{SS} = -15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = - 10 V to +10 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		2	2.7	Ω
			- 40°C to +85°C			3.4	Ω
			- 40°C to +125°C			4	Ω
Δ R <sub>ON</sub>	On-resistance mismatch between channels	V <sub>S</sub> = - 10 V to +10 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		0.1	0.18	Ω
			- 40°C to +85°C			0.19	Ω
			- 40°C to +125°C			0.21	Ω
R <sub>ON FLAT</sub>	On-resistance flatness	V <sub>S</sub> = - 10 V to +10 V I <sub>S</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		0.2	0.46	Ω
			- 40°C to +85°C			0.65	Ω
			- 40°C to +125°C			0.7	Ω
R <sub>ON DRIFT</sub>	On-resistance drift	V <sub>S</sub> = 0 V, I <sub>S</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	- 40°C to +125°C		0.008		Ω/°C
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = - 16.5 V Switch state is off V <sub>S</sub> = +10 V / - 10 V V <sub>D</sub> = - 10 V / + 10 V Refer to <a href="#">Off-Leakage Current</a>	25°C	- 0.25	0.05	0.25	nA
			- 40°C to +85°C	- 3		3	nA
			- 40°C to +125°C	- 20		20	nA
I <sub>D(OFF)</sub>	Drain off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = - 16.5 V Switch state is off V <sub>S</sub> = +10 V / - 10 V V <sub>D</sub> = - 10 V / + 10 V Refer to <a href="#">Off-Leakage Current</a>	25°C	- 0.6	0.1	0.6	nA
			- 40°C to +85°C	- 7		7	nA
			- 40°C to +125°C	- 45		45	nA
I <sub>S(ON)</sub> I <sub>D(ON)</sub>	Channel on leakage current <sup>(2)</sup>	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = - 16.5 V Switch state is on V <sub>S</sub> = V <sub>D</sub> = ±10 V Refer to <a href="#">On-Leakage Current</a>	25°C	- 0.25	0.05	0.25	nA
			- 40°C to +85°C	- 3		3	nA
			- 40°C to +125°C	- 20		20	nA
LOGIC INPUTS (SEL / EN pins)							
V <sub>IH</sub>	Logic voltage high		- 40°C to +125°C	1.3		44	V
V <sub>IL</sub>	Logic voltage low		- 40°C to +125°C	0		0.8	V
I <sub>IH</sub>	Input leakage current		- 40°C to +125°C		0.4	2	μA
I <sub>IL</sub>	Input leakage current		- 40°C to +125°C	- 1.5	- 0.005		μA
C <sub>IN</sub>	Logic input capacitance		- 40°C to +125°C		3.5		pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = - 16.5 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		35	56	μA
			- 40°C to +85°C			65	μA
			- 40°C to +125°C			80	μA
I <sub>SS</sub>	V <sub>SS</sub> supply current	V <sub>DD</sub> = 16.5 V, V <sub>SS</sub> = - 16.5 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		5	20	μA
			- 40°C to +85°C			24	μA
			- 40°C to +125°C			35	μA

(1) When  $V_S$  is positive,  $V_D$  is negative, or when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating, or when  $V_D$  is at a voltage potential,  $V_S$  is floating.

## 5.7 ±15 V Dual Supply: Switching Characteristics

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +15\text{ V}$ ,  $V_{SS} = -15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{\text{TRAN}}$	Transition time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Transition Time</a>	$25^\circ\text{C}$		110	125	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			140	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			155	ns
$t_{\text{ON}}$	Turn-on time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on and Turn-off Time</a>	$25^\circ\text{C}$		95	120	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			135	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			145	ns
$t_{\text{OFF}}$	Turn-off time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on and Turn-off Time</a>	$25^\circ\text{C}$		125	160	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			175	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			190	ns
$t_{\text{BBM}}$	Break-before-make time delay	$V_S = 10\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Break-before-make Time</a>	$25^\circ\text{C}$		27		ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$	5			ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$	5			ns
$t_{\text{ON}}(V_{DD})$	Device turn on time ( $V_{DD}$ to output)	$V_{DD}$ rise time = $1\ \mu\text{s}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on (VDD) Time</a>	$25^\circ\text{C}$		0.17		ms
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$		0.18		ms
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$		0.18		ms
$t_{\text{PD}}$	Propagation delay	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ Refer to <a href="#">Propagation Delay</a>	$25^\circ\text{C}$		720		ps
$Q_{\text{INJ}}$	Charge injection	$V_S = 0\text{ V}$ , $C_L = 100\text{ pF}$ Refer to <a href="#">Charge Injection</a>	$25^\circ\text{C}$		30		pC
$O_{\text{ISO}}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 100\text{ kHz}$ Refer to <a href="#">Off Isolation</a>	$25^\circ\text{C}$		-70		dB
$O_{\text{ISO}}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$ Refer to <a href="#">Off Isolation</a>	$25^\circ\text{C}$		-50		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 100\text{ kHz}$ Refer to <a href="#">Crosstalk</a>	$25^\circ\text{C}$		-107		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$ Refer to <a href="#">Crosstalk</a>	$25^\circ\text{C}$		-93		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ Refer to <a href="#">Bandwidth</a>	$25^\circ\text{C}$		40		MHz
$I_L$	Insertion loss	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-0.15		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on $V_{DD}$ and $V_{SS}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ Refer to <a href="#">ACPSRR</a>	$25^\circ\text{C}$		-68		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 15\text{ V}$ , $V_{\text{BIAS}} = 0\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 5\text{ pF}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ Refer to <a href="#">THD + Noise</a>	$25^\circ\text{C}$		0.0006		%
$C_{S(\text{OFF})}$	Source off capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		45		pF
$C_{D(\text{OFF})}$	Drain off capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		55		pF
$C_{S(\text{ON})}$ , $C_{D(\text{ON})}$	On capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		165		pF

## 5.8 ±20 V Dual Supply: Electrical Characteristics

$V_{DD} = +20\text{ V} \pm 10\%$ ,  $V_{SS} = -20\text{ V} \pm 10\%$ , GND = 0 V (unless otherwise noted)

Typical at  $V_{DD} = +20\text{ V}$ ,  $V_{SS} = -20\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = - 15 V to +15 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		1.7	2.5	Ω
			- 40°C to +85°C			3.2	Ω
			- 40°C to +125°C			3.8	Ω
Δ R <sub>ON</sub>	On-resistance mismatch between channels	V <sub>S</sub> = - 15 V to +15 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		0.1	0.18	Ω
			- 40°C to +85°C			0.19	Ω
			- 40°C to +125°C			0.21	Ω
R <sub>ON FLAT</sub>	On-resistance flatness	V <sub>S</sub> = - 15 V to +15 V I <sub>S</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		0.3	0.6	Ω
			- 40°C to +85°C			0.8	Ω
			- 40°C to +125°C			0.95	Ω
R <sub>ON DRIFT</sub>	On-resistance drift	V <sub>S</sub> = 0 V, I <sub>S</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	- 40°C to +125°C		0.008		Ω/°C
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = - 22 V Switch state is off V <sub>S</sub> = +15 V / - 15 V V <sub>D</sub> = - 15 V / + 15 V Refer to <a href="#">Off-Leakage Current</a>	25°C	- 1	0.05	1	nA
			- 40°C to +85°C	- 4.5		4.5	nA
			- 40°C to +125°C	- 33		33	nA
I <sub>D(OFF)</sub>	Drain off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = - 22 V Switch state is off V <sub>S</sub> = +15 V / - 15 V V <sub>D</sub> = - 15 V / + 15 V Refer to <a href="#">Off-Leakage Current</a>	25°C	- 2.2	0.22	2.2	nA
			- 40°C to +85°C	- 10		10	nA
			- 40°C to +125°C	- 70		70	nA
I <sub>S(ON)</sub> I <sub>D(ON)</sub>	Channel on leakage current <sup>(2)</sup>	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = - 22 V Switch state is on V <sub>S</sub> = V <sub>D</sub> = ±15 V Refer to <a href="#">On-Leakage Current</a>	25°C	- 1	0.05	1	nA
			- 40°C to +85°C	- 4.5		4.5	nA
			- 40°C to +125°C	- 33		33	nA
LOGIC INPUTS (SEL / EN pins)							
V <sub>IH</sub>	Logic voltage high		- 40°C to +125°C	1.3		44	V
V <sub>IL</sub>	Logic voltage low		- 40°C to +125°C	0		0.8	V
I <sub>IH</sub>	Input leakage current		- 40°C to +125°C		0.4	2	μA
I <sub>IL</sub>	Input leakage current		- 40°C to +125°C	- 1.2	- 0.005		μA
C <sub>IN</sub>	Logic input capacitance		- 40°C to +125°C		3.5		pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = - 22 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		33	65	μA
			- 40°C to +85°C			74	μA
			- 40°C to +125°C			90	μA
I <sub>SS</sub>	V <sub>SS</sub> supply current	V <sub>DD</sub> = 22 V, V <sub>SS</sub> = - 22 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		7	26	μA
			- 40°C to +85°C			30	μA
			- 40°C to +125°C			45	μA

(1) When  $V_S$  is positive,  $V_D$  is negative, or when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating, or when  $V_D$  is at a voltage potential,  $V_S$  is floating.



## 5.9 ±20 V Dual Supply: Switching Characteristics

$V_{DD} = +20\text{ V} \pm 10\%$ ,  $V_{SS} = -20\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +20\text{ V}$ ,  $V_{SS} = -20\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{\text{TRAN}}$	Transition time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Transition Time</a>	$25^\circ\text{C}$		100	160	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			170	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			180	ns
$t_{\text{ON}}$	Turn-on time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on and Turn-off Time</a>	$25^\circ\text{C}$		95	140	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			160	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			180	ns
$t_{\text{OFF}}$	Turn-off time from control input	$V_S = 10\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on and Turn-off Time</a>	$25^\circ\text{C}$		125	150	ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$			165	ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$			190	ns
$t_{\text{BBM}}$	Break-before-make time delay	$V_S = 10\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Break-before-make Time</a>	$25^\circ\text{C}$		28		ns
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$	5			ns
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$	5			ns
$t_{\text{ON}}(V_{DD})$	Device turn on time ( $V_{DD}$ to output)	$V_{DD}$ rise time = $1\ \mu\text{s}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on (VDD) Time</a>	$25^\circ\text{C}$		0.17		ms
			$-40^\circ\text{C}$ to $+85^\circ\text{C}$		0.18		ms
			$-40^\circ\text{C}$ to $+125^\circ\text{C}$		0.18		ms
$t_{\text{PD}}$	Propagation delay	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ Refer to <a href="#">Propagation Delay</a>	$25^\circ\text{C}$		740		ps
$Q_{\text{INJ}}$	Charge injection	$V_S = 0\text{ V}$ , $C_L = 100\text{ pF}$ Refer to <a href="#">Charge Injection</a>	$25^\circ\text{C}$		45		pC
$O_{\text{ISO}}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 100\text{ kHz}$ Refer to <a href="#">Off Isolation</a>	$25^\circ\text{C}$		-70		dB
$O_{\text{ISO}}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$ Refer to <a href="#">Off Isolation</a>	$25^\circ\text{C}$		-50		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 100\text{ kHz}$ Refer to <a href="#">Crosstalk</a>	$25^\circ\text{C}$		-107		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$ Refer to <a href="#">Crosstalk</a>	$25^\circ\text{C}$		-93		dB
BW	-3dB Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ Refer to <a href="#">Bandwidth</a>	$25^\circ\text{C}$		35		MHz
$I_L$	Insertion loss	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		-0.14		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on $V_{DD}$ and $V_{SS}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ Refer to <a href="#">ACPSRR</a>	$25^\circ\text{C}$		-68		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 20\text{ V}$ , $V_{\text{BIAS}} = 0\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 5\text{ pF}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ Refer to <a href="#">THD + Noise</a>	$25^\circ\text{C}$		0.0006		%
$C_{S(\text{OFF})}$	Source off capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		45		pF
$C_{D(\text{OFF})}$	Drain off capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		55		pF
$C_{S(\text{ON})}$ , $C_{D(\text{ON})}$	On capacitance	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$	$25^\circ\text{C}$		165		pF

## 5.10 44 V Single Supply: Electrical Characteristics

$V_{DD} = +44\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +44\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = 0 V to 40 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		2	2.4	Ω
			- 40°C to +85°C			3.2	Ω
			- 40°C to +125°C			3.8	Ω
Δ R <sub>ON</sub>	On-resistance mismatch between channels	V <sub>S</sub> = 0 V to 40 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		0.1	0.18	Ω
			- 40°C to +85°C			0.19	Ω
			- 40°C to +125°C			0.21	Ω
R <sub>ON FLAT</sub>	On-resistance flatness	V <sub>S</sub> = 0 V to 40 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		0.65	0.8	Ω
			- 40°C to +85°C			1.1	Ω
			- 40°C to +125°C			1.2	Ω
R <sub>ON DRIFT</sub>	On-resistance drift	V <sub>S</sub> = 22 V, I <sub>S</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	- 40°C to +125°C		0.007		Ω/°C
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 44 V, V <sub>SS</sub> = 0 V Switch state is off V <sub>S</sub> = 40 V / 1 V V <sub>D</sub> = 1 V / 40 V Refer to <a href="#">Off-Leakage Current</a>	25°C	- 1	0.05	1	nA
			- 40°C to +85°C	- 7		7	nA
			- 40°C to +125°C	- 50		50	nA
I <sub>D(OFF)</sub>	Drain off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 44 V, V <sub>SS</sub> = 0 V Switch state is off V <sub>S</sub> = 40 V / 1 V V <sub>D</sub> = 1 V / 40 V Refer to <a href="#">Off-Leakage Current</a>	25°C	- 2.2	0.12	2.2	nA
			- 40°C to +85°C	- 15		15	nA
			- 40°C to +125°C	- 115		115	nA
I <sub>S(ON)</sub> I <sub>D(ON)</sub>	Channel on leakage current <sup>(2)</sup>	V <sub>DD</sub> = 44 V, V <sub>SS</sub> = 0 V Switch state is on V <sub>S</sub> = V <sub>D</sub> = 40 V or 1 V Refer to <a href="#">On-Leakage Current</a>	25°C	- 1	0.05	1	nA
			- 40°C to +85°C	- 7		7	nA
			- 40°C to +125°C	- 50		50	nA
LOGIC INPUTS (SEL / EN pins)							
V <sub>IH</sub>	Logic voltage high		- 40°C to +125°C	1.3		44	V
V <sub>IL</sub>	Logic voltage low		- 40°C to +125°C	0		0.8	V
I <sub>IH</sub>	Input leakage current		- 40°C to +125°C		1	2.75	μA
I <sub>IL</sub>	Input leakage current		- 40°C to +125°C	- 1.2	- 0.005		μA
C <sub>IN</sub>	Logic input capacitance		- 40°C to +125°C		3.5		pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 44 V, V <sub>SS</sub> = 0 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		44	79	μA
			- 40°C to +85°C			88	μA
			- 40°C to +125°C			105	μA

(1) When  $V_S$  is positive,  $V_D$  is negative, or when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating, or when  $V_D$  is at a voltage potential,  $V_S$  is floating.

## 5.11 44 V Single Supply: Switching Characteristics

$V_{DD} = +44\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +44\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{\text{TRAN}}$	Transition time from control input	$V_S = 18\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Transition Time</a>	25°C		85	145	ns
			– 40°C to +85°C			155	ns
			– 40°C to +125°C			185	ns
$t_{\text{ON}}$	Turn-on time from control input	$V_S = 18\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on and Turn-off Time</a>	25°C		90	130	ns
			– 40°C to +85°C			140	ns
			– 40°C to +125°C			160	ns
$t_{\text{OFF}}$	Turn-off time from control input	$V_S = 18\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on and Turn-off Time</a>	25°C		125	160	ns
			– 40°C to +85°C			170	ns
			– 40°C to +125°C			180	ns
$t_{\text{BBM}}$	Break-before-make time delay	$V_S = 18\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Break-before-make Time</a>	25°C		27		ns
			– 40°C to +85°C	10			ns
			– 40°C to +125°C	10			ns
$t_{\text{ON}}(V_{DD})$	Device turn on time ( $V_{DD}$ to output)	$V_{DD}$ rise time = 1 $\mu\text{s}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on (VDD) Time</a>	25°C		0.14		ms
			– 40°C to +85°C		0.15		ms
			– 40°C to +125°C		0.15		ms
$t_{\text{PD}}$	Propagation delay	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ Refer to <a href="#">Propagation Delay</a>	25°C		900		ps
$Q_{\text{INJ}}$	Charge injection	$V_S = 22\text{ V}$ , $C_L = 100\text{ pF}$ Refer to <a href="#">Charge Injection</a>	25°C		104		pC
$O_{\text{ISO}}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 100\text{ kHz}$ Refer to <a href="#">Off Isolation</a>	25°C		– 70		dB
$O_{\text{ISO}}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$ Refer to <a href="#">Off Isolation</a>	25°C		– 50		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 100\text{ kHz}$ Refer to <a href="#">Crosstalk</a>	25°C		– 112		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$ Refer to <a href="#">Crosstalk</a>	25°C		– 93		dB
BW	– 3dB Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ Refer to <a href="#">Bandwidth</a>	25°C		35		MHz
$I_L$	Insertion loss	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	25°C		– 0.15		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on $V_{DD}$ and $V_{SS}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ Refer to <a href="#">ACPSRR</a>	25°C		– 66		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 22\text{ V}$ , $V_{\text{BIAS}} = 22\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 5\text{ pF}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ Refer to <a href="#">THD + Noise</a>	25°C		0.0006		%
$C_{S(\text{OFF})}$	Source off capacitance	$V_S = 22\text{ V}$ , $f = 1\text{ MHz}$	25°C		45		pF
$C_{D(\text{OFF})}$	Drain off capacitance	$V_S = 22\text{ V}$ , $f = 1\text{ MHz}$	25°C		55		pF
$C_{S(\text{ON})}$ , $C_{D(\text{ON})}$	On capacitance	$V_S = 22\text{ V}$ , $f = 1\text{ MHz}$	25°C		165		pF

## 5.12 12 V Single Supply: Electrical Characteristics

$V_{DD} = +12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +12\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T <sub>A</sub>	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R <sub>ON</sub>	On-resistance	V <sub>S</sub> = 0 V to 10 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		2.8	5.4	Ω
			- 40°C to +85°C			6.8	Ω
			- 40°C to +125°C			7.4	Ω
Δ R <sub>ON</sub>	On-resistance mismatch between channels	V <sub>S</sub> = 0 V to 10 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		0.13	0.21	Ω
			- 40°C to +85°C			0.23	Ω
			- 40°C to +125°C			0.25	Ω
R <sub>ON FLAT</sub>	On-resistance flatness	V <sub>S</sub> = 0 V to 10 V I <sub>D</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	25°C		0.8	1.7	Ω
			- 40°C to +85°C			1.9	Ω
			- 40°C to +125°C			2	Ω
R <sub>ON DRIFT</sub>	On-resistance drift	V <sub>S</sub> = 6 V, I <sub>S</sub> = - 10 mA Refer to <a href="#">On-Resistance</a>	- 40°C to +125°C		0.015		Ω/°C
I <sub>S(OFF)</sub>	Source off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V Switch state is off V <sub>S</sub> = 10 V / 1 V V <sub>D</sub> = 1 V / 10 V Refer to <a href="#">Off-Leakage Current</a>	25°C	- 0.25	0.01	0.25	nA
			- 40°C to +85°C	- 2		2	nA
			- 40°C to +125°C	- 16		16	nA
I <sub>D(OFF)</sub>	Drain off leakage current <sup>(1)</sup>	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V Switch state is off V <sub>S</sub> = 10 V / 1 V V <sub>D</sub> = 1 V / 10 V Refer to <a href="#">Off-Leakage Current</a>	25°C	- 0.6	0.12	0.6	nA
			- 40°C to +85°C	- 5		5	nA
			- 40°C to +125°C	- 34		34	nA
I <sub>S(ON)</sub> I <sub>D(ON)</sub>	Channel on leakage current <sup>(2)</sup>	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V Switch state is on V <sub>S</sub> = V <sub>D</sub> = 10 V or 1 V Refer to <a href="#">On-Leakage Current</a>	25°C	- 0.25	0.01	0.25	nA
			- 40°C to +85°C	- 2		2	nA
			- 40°C to +125°C	- 16		16	nA
LOGIC INPUTS (SEL / EN pins)							
V <sub>IH</sub>	Logic voltage high		- 40°C to +125°C	1.3		44	V
V <sub>IL</sub>	Logic voltage low		- 40°C to +125°C	0		0.8	V
I <sub>IH</sub>	Input leakage current		- 40°C to +125°C		0.4	2.25	μA
I <sub>IL</sub>	Input leakage current		- 40°C to +125°C	- 1.25	- 0.005		μA
C <sub>IN</sub>	Logic input capacitance		- 40°C to +125°C		3.5		pF
POWER SUPPLY							
I <sub>DD</sub>	V <sub>DD</sub> supply current	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V Logic inputs = 0 V, 5 V, or V <sub>DD</sub>	25°C		30	44	μA
			- 40°C to +85°C			52	μA
			- 40°C to +125°C			62	μA

(1) When  $V_S$  is positive,  $V_D$  is negative, or when  $V_S$  is negative,  $V_D$  is positive.

(2) When  $V_S$  is at a voltage potential,  $V_D$  is floating, or when  $V_D$  is at a voltage potential,  $V_S$  is floating.

### 5.13 12 V Single Supply: Switching Characteristics

$V_{DD} = +12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +12\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$t_{\text{TRAN}}$	Transition time from control input	$V_S = 8\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Transition Time</a>	25°C		90	160	ns
			– 40°C to +85°C			190	ns
			– 40°C to +125°C			225	ns
$t_{\text{ON}}$	Turn-on time from control input	$V_S = 8\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on and Turn-off Time</a>	25°C		190	235	ns
			– 40°C to +85°C			260	ns
			– 40°C to +125°C			280	ns
$t_{\text{OFF}}$	Turn-off time from control input	$V_S = 8\text{ V}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on and Turn-off Time</a>	25°C		160	200	ns
			– 40°C to +85°C			220	ns
			– 40°C to +125°C			245	ns
$t_{\text{BBM}}$	Break-before-make time delay	$V_S = 8\text{ V}$ , $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Break-before-make Time</a>	25°C		30		ns
			– 40°C to +85°C	9			ns
			– 40°C to +125°C	9			ns
$t_{\text{ON (VDD)}}$	Device turn on time ( $V_{DD}$ to output)	$V_{DD}$ rise time = 1 $\mu\text{s}$ $R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ Refer to <a href="#">Turn-on (VDD) Time</a>	25°C		0.17		ms
			– 40°C to +85°C		0.18		ms
			– 40°C to +125°C		0.18		ms
$t_{\text{PD}}$	Propagation delay	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ Refer to <a href="#">Propagation Delay</a>	25°C		770		ps
$Q_{\text{INJ}}$	Charge injection	$V_S = 6\text{ V}$ , $C_L = 100\text{ pF}$ Refer to <a href="#">Charge Injection</a>	25°C		12		pC
$O_{\text{ISO}}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 100\text{ kHz}$ Refer to <a href="#">Off Isolation</a>	25°C		– 70		dB
$O_{\text{ISO}}$	Off-isolation	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$ Refer to <a href="#">Off Isolation</a>	25°C		– 50		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 100\text{ kHz}$ Refer to <a href="#">Crosstalk</a>	25°C		– 112		dB
$X_{\text{TALK}}$	Crosstalk	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$ Refer to <a href="#">Crosstalk</a>	25°C		– 93		dB
BW	– 3dB Bandwidth	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ Refer to <a href="#">Bandwidth</a>	25°C		50		MHz
$I_L$	Insertion loss	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ $V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	25°C		– 0.25		dB
ACPSRR	AC Power Supply Rejection Ratio	$V_{PP} = 0.62\text{ V}$ on $V_{DD}$ and $V_{SS}$ $R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ Refer to <a href="#">ACPSRR</a>	25°C		– 70		dB
THD+N	Total Harmonic Distortion + Noise	$V_{PP} = 6\text{ V}$ , $V_{\text{BIAS}} = 6\text{ V}$ $R_L = 10\text{ k}\Omega$ , $C_L = 5\text{ pF}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ Refer to <a href="#">THD + Noise</a>	25°C		0.001		%
$C_{S(\text{OFF})}$	Source off capacitance	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	25°C		52		pF
$C_{D(\text{OFF})}$	Drain off capacitance	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	25°C		68		pF
$C_{S(\text{ON})}$ , $C_{D(\text{ON})}$	On capacitance	$V_S = 6\text{ V}$ , $f = 1\text{ MHz}$	25°C		170		pF

## 5.14 Typical Characteristics

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

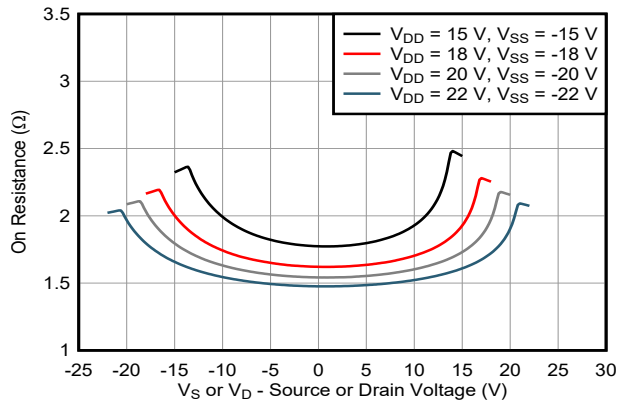


图 5-1. On-Resistance vs Source or Drain Voltage - Dual Supply

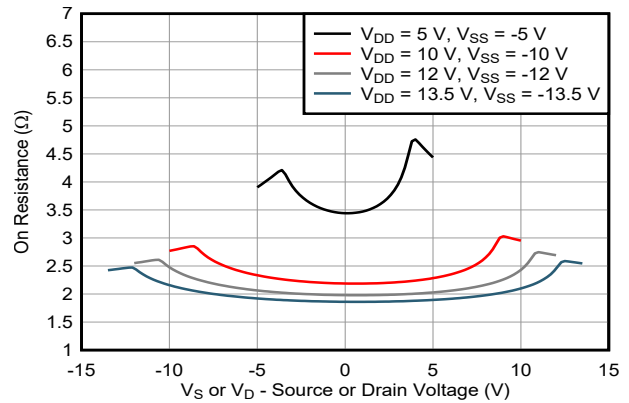


图 5-2. On-Resistance vs Source or Drain Voltage - Dual Supply

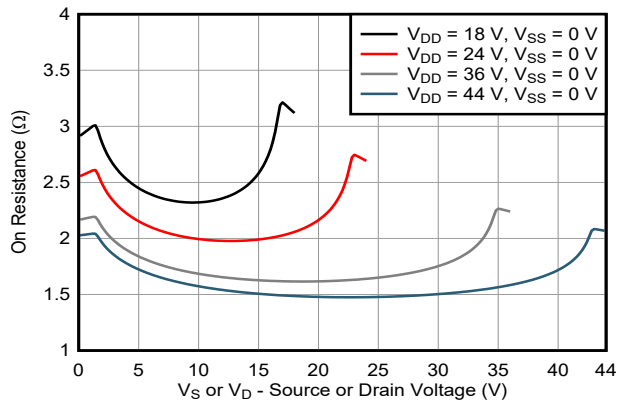


图 5-3. On-Resistance vs Source or Drain Voltage - Single Supply

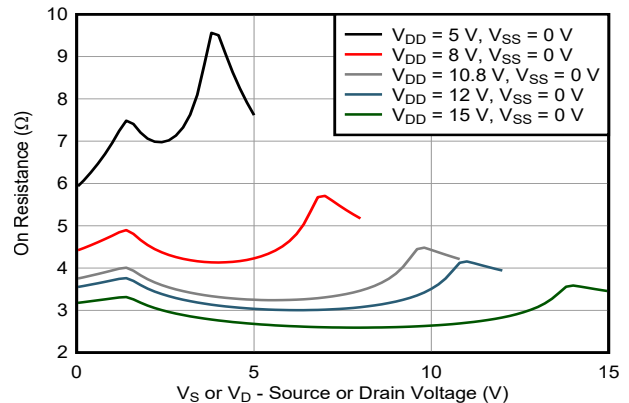


图 5-4. On-Resistance vs Source or Drain Voltage - Single Supply

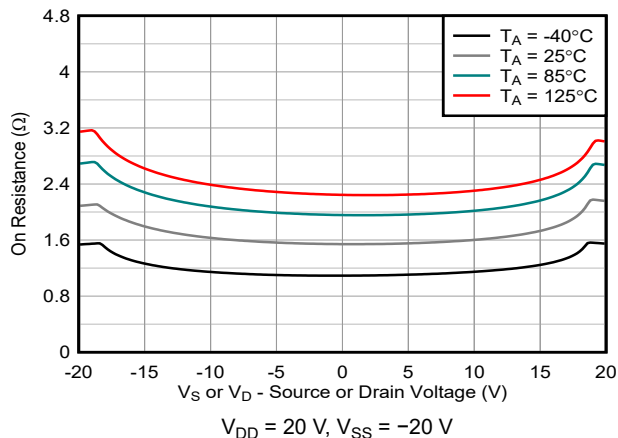


图 5-5. On-Resistance vs Temperature

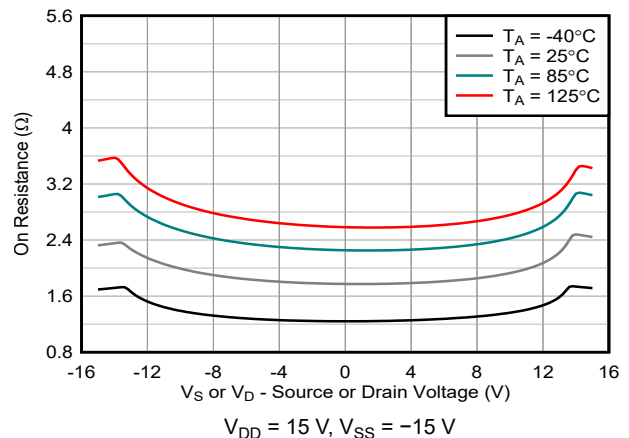


图 5-6. On-Resistance vs Temperature

## 5.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

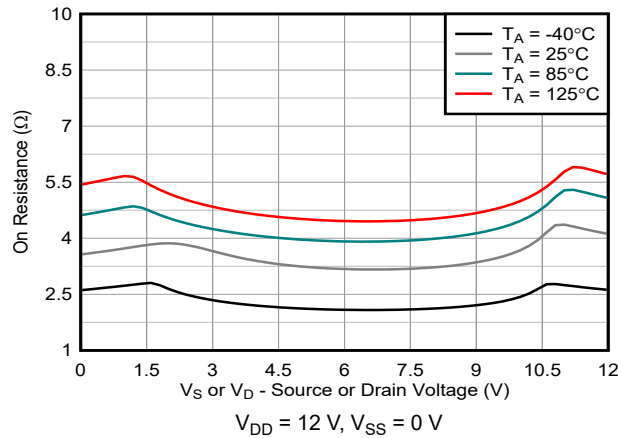


图 5-7. On-Resistance vs Temperature

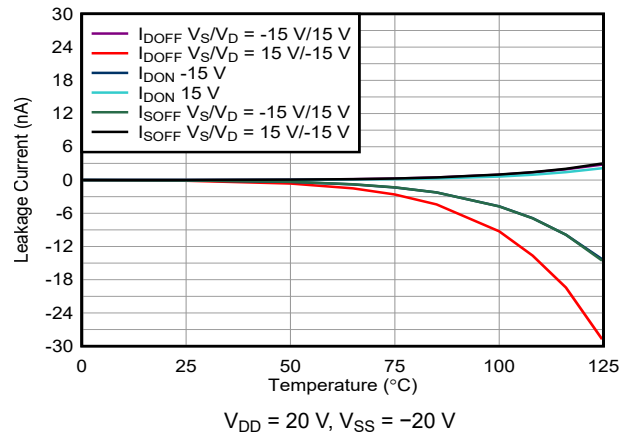


图 5-8. On-Leakage vs Temperature

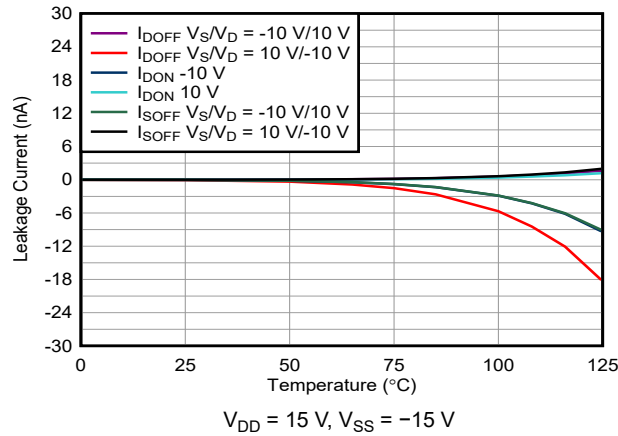


图 5-9. On-Leakage vs Temperature

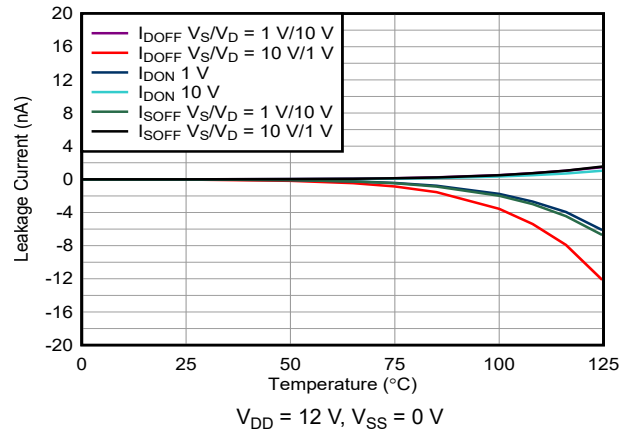


图 5-10. On-Leakage vs Temperature

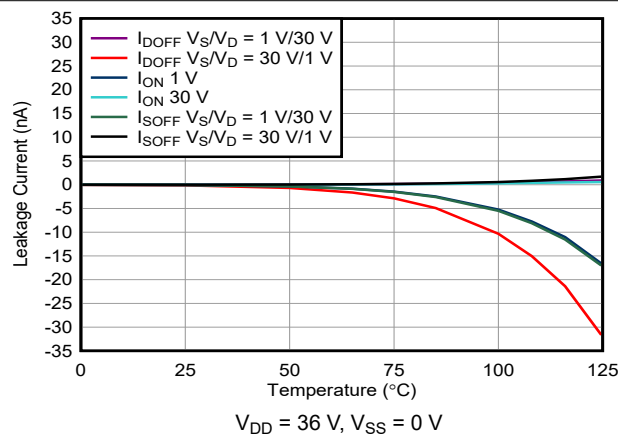


图 5-11. On-Leakage vs Temperature

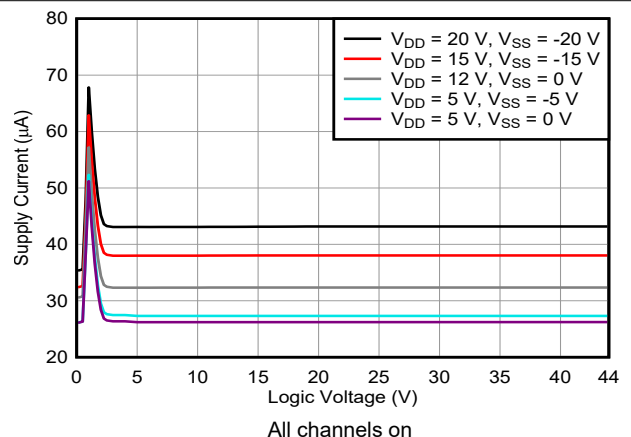


图 5-12. Supply Current vs Logic Voltage

## 5.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

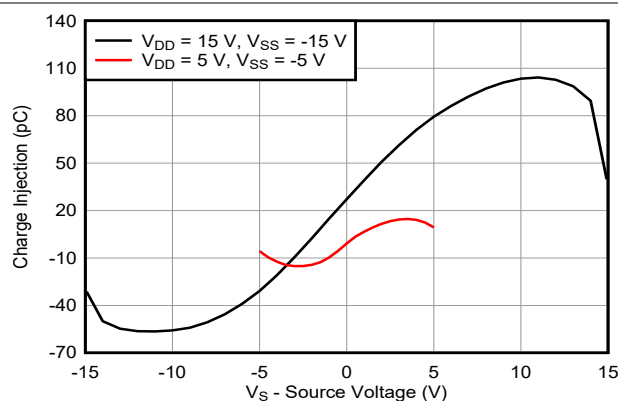


图 5-13. Charge Injection vs Source Voltage - Dual Supply

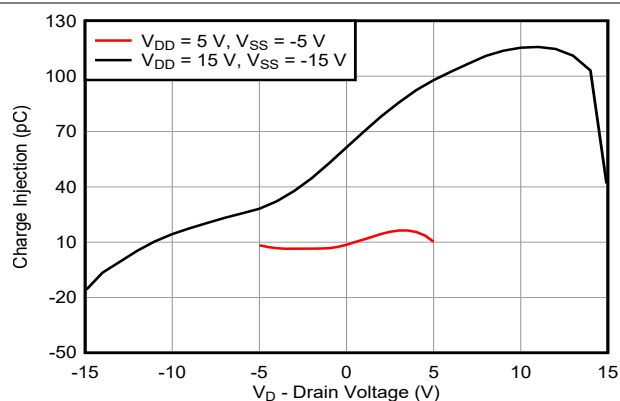


图 5-14. Charge Injection vs Drain Voltage - Dual Supply

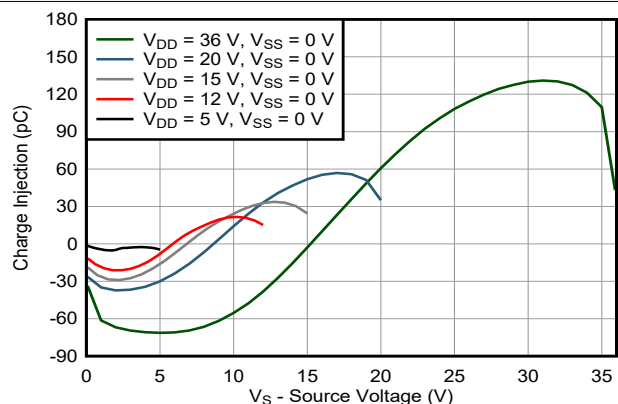


图 5-15. Charge Injection vs Source Voltage - Single Supply

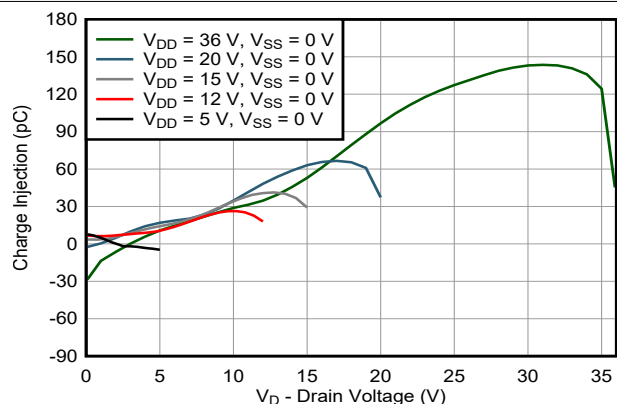


图 5-16. Charge Injection vs Drain Voltage - Single Supply

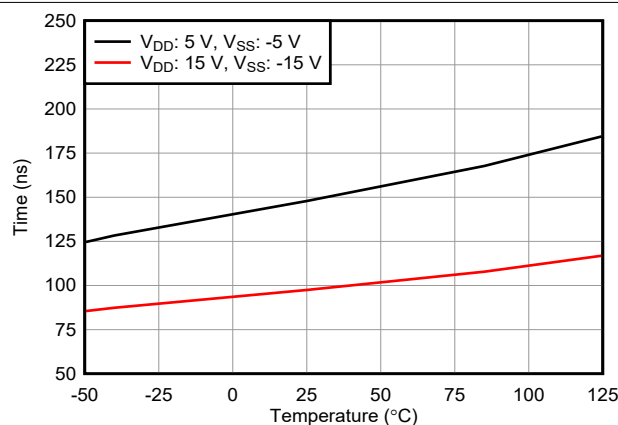


图 5-17.  $T_{\text{TRANSITION}}$  vs Temperature

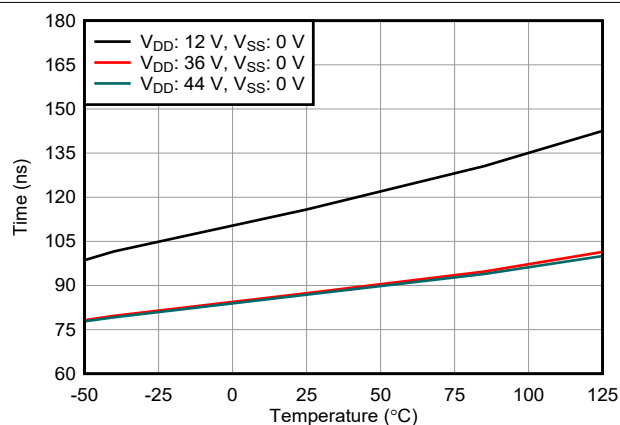


图 5-18.  $T_{\text{TRANSITION}}$  vs Temperature



## 5.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

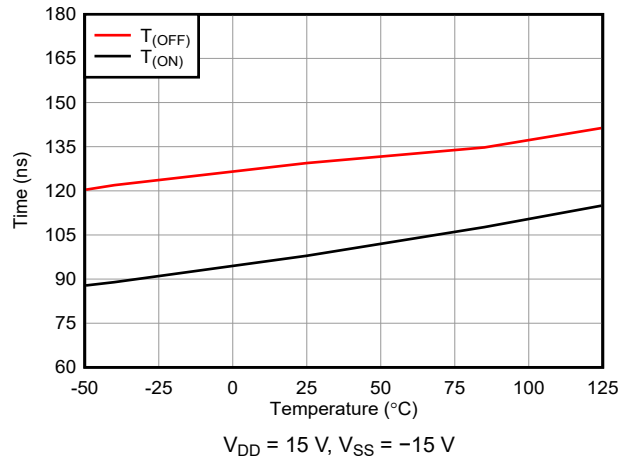


图 5-19.  $T_{ON}$  (EN) and  $T_{OFF}$  (EN) vs Temperature

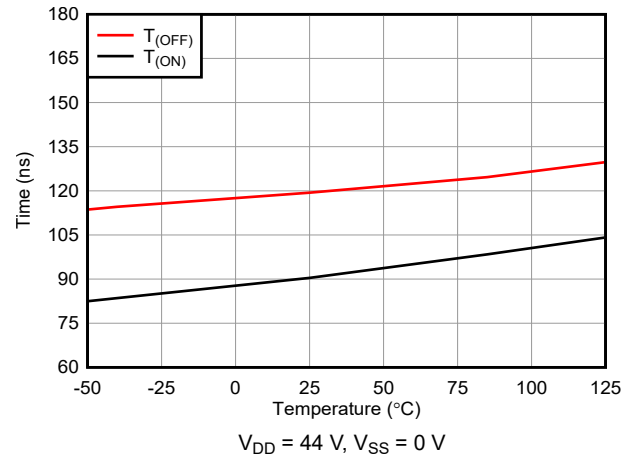


图 5-20.  $T_{ON}$  (EN) and  $T_{OFF}$  (EN) vs Temperature

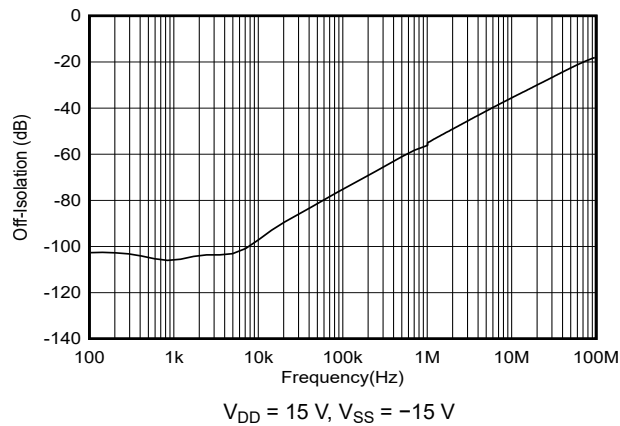


图 5-21. Off-Isolation vs Frequency

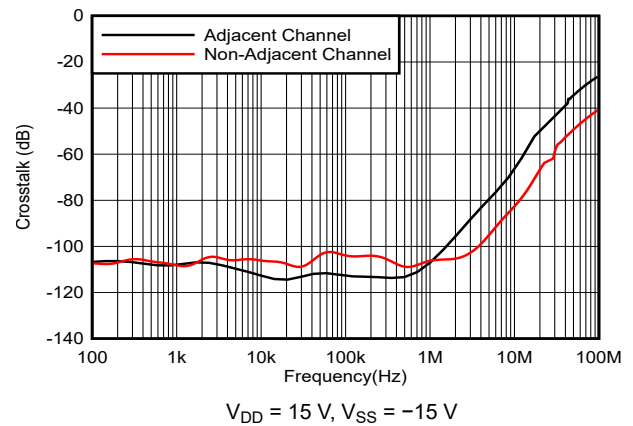


图 5-22. Crosstalk vs Frequency

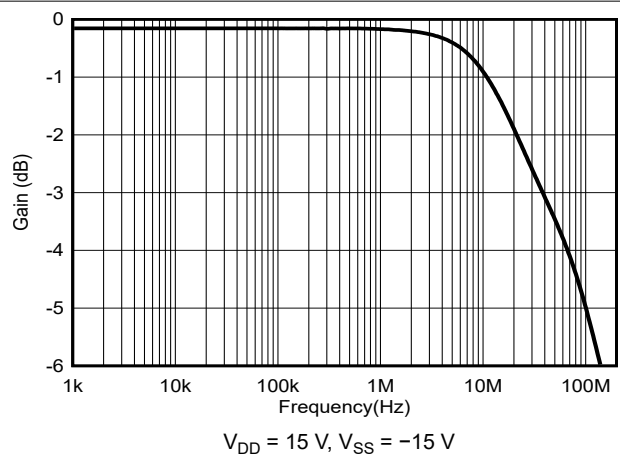


图 5-23. On Response vs Frequency

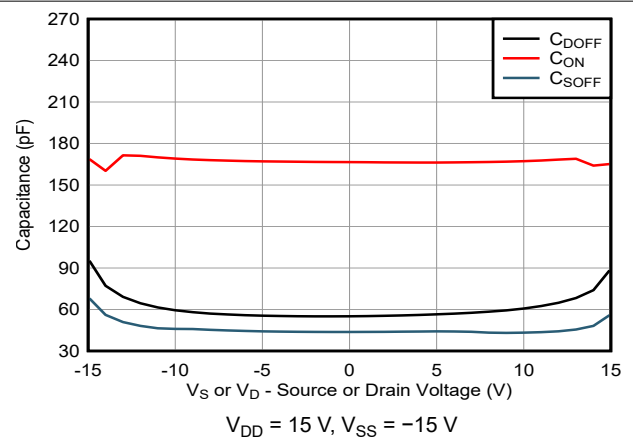


图 5-24. Capacitance vs Source or Drain Voltage

## 5.14 Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

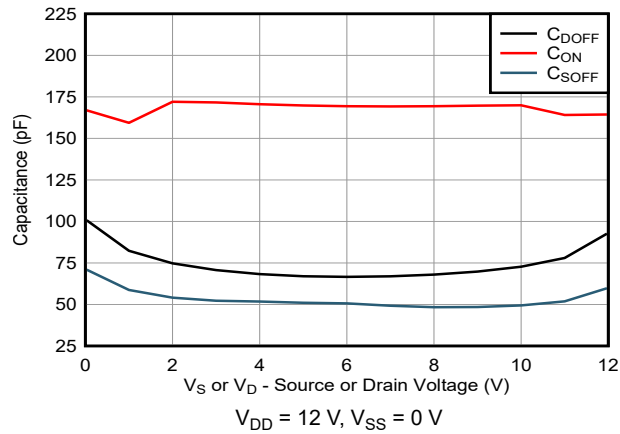


图 5-25. Capacitance vs Source or Drain Voltage

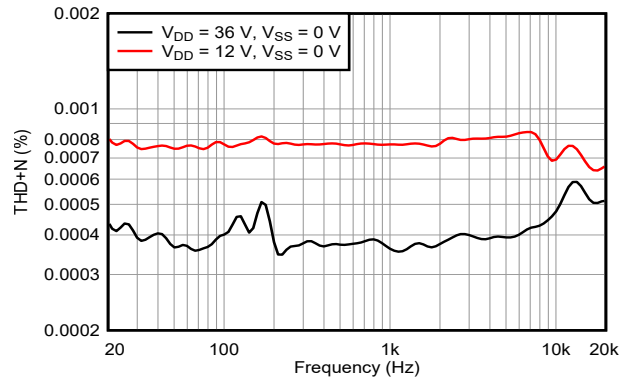


图 5-26. THD+N vs Frequency - Single Supply

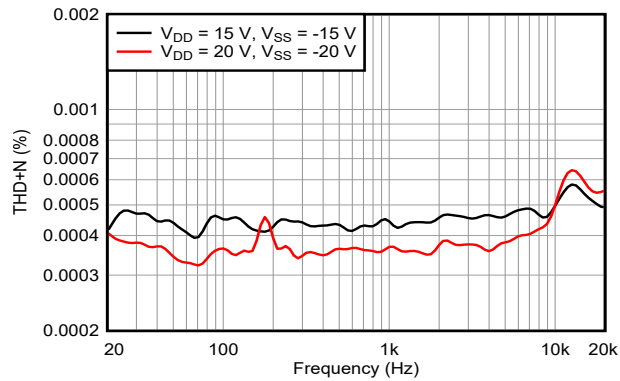


图 5-27. THD+N vs Frequency - Dual Supply

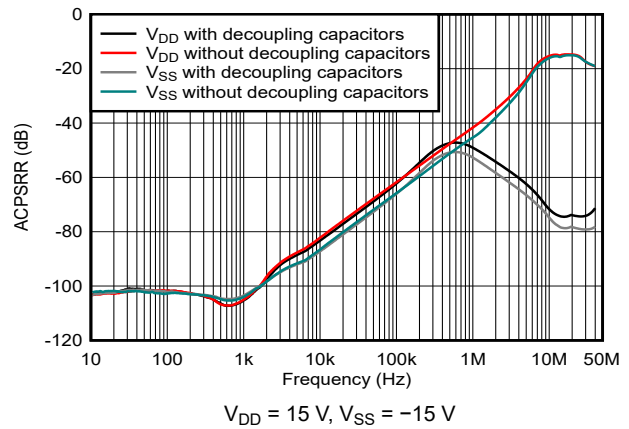


图 5-28. ACPSRR vs Frequency

## 6 Parameter Measurement Information

### 6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol  $R_{ON}$  is used to denote on-resistance. 图 6-1 shows the measurement setup used to measure  $R_{ON}$ . Voltage (V) and current ( $I_{SD}$ ) are measured using this setup, and  $R_{ON}$  is computed with  $R_{ON} = V / I_{SD}$ .

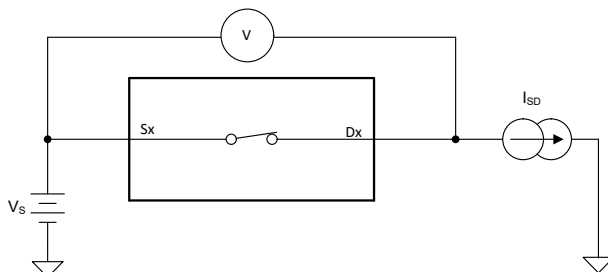


图 6-1. On-Resistance Measurement Setup

### 6.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

- Source off-leakage current
- Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol  $I_{S(OFF)}$ .

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol  $I_{D(OFF)}$ .

图 6-2 shows the setup used to measure both off-leakage currents.

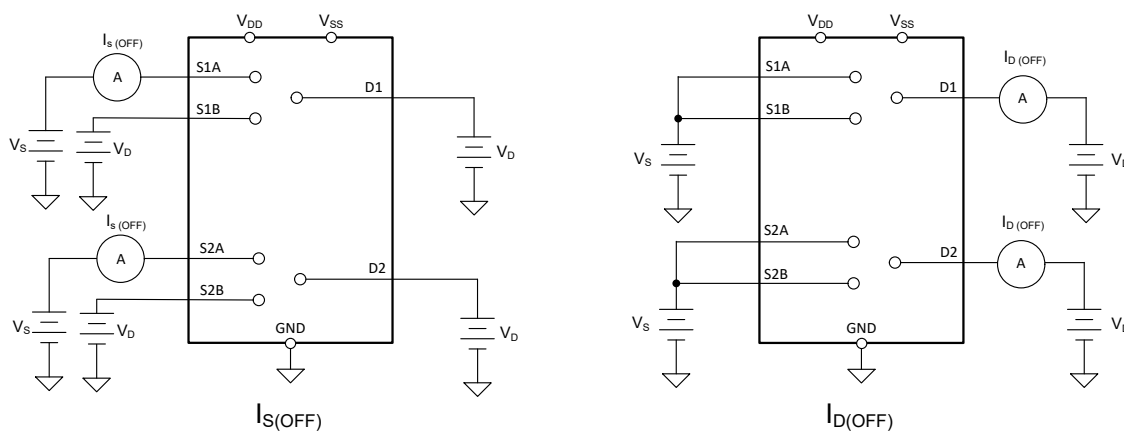


图 6-2. Off-Leakage Measurement Setup

### 6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol  $I_{S(ON)}$ .

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol  $I_{D(ON)}$ .

Either the source pin or drain pin is left floating during the measurement. 图 6-3 shows the circuit used for measuring the on-leakage current, denoted by  $I_{S(ON)}$  or  $I_{D(ON)}$ .

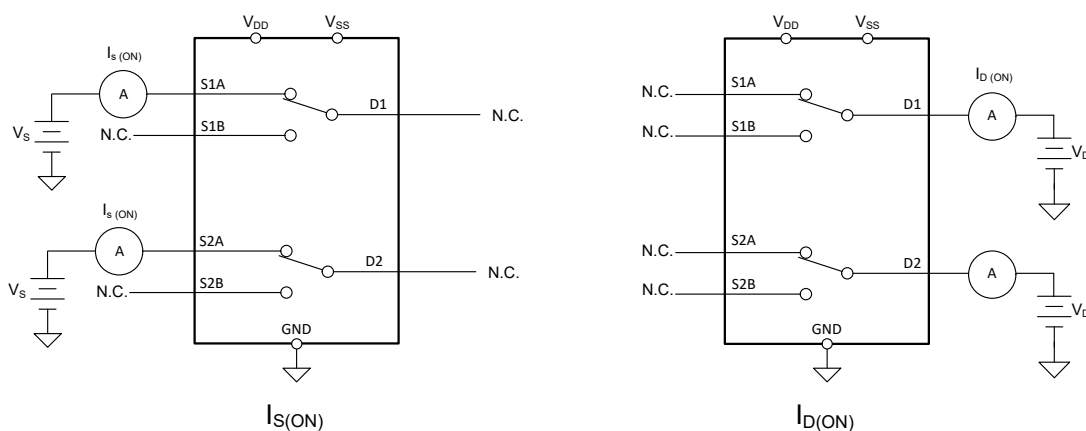


图 6-3. On-Leakage Measurement Setup

### 6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 6-4 shows the setup used to measure transition time, denoted by the symbol  $t_{\text{TRANSITION}}$ .

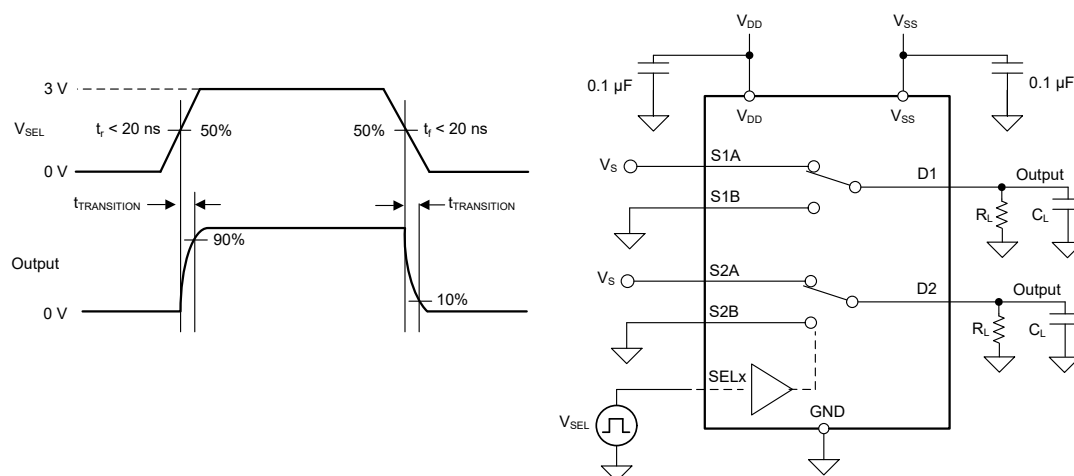


图 6-4. Transition-Time Measurement Setup

## 6.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 6-5 shows the setup used to measure turn-on time, denoted by the symbol  $t_{ON(EN)}$ .

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 6-5 shows the setup used to measure turn-off time, denoted by the symbol  $t_{OFF(EN)}$ .

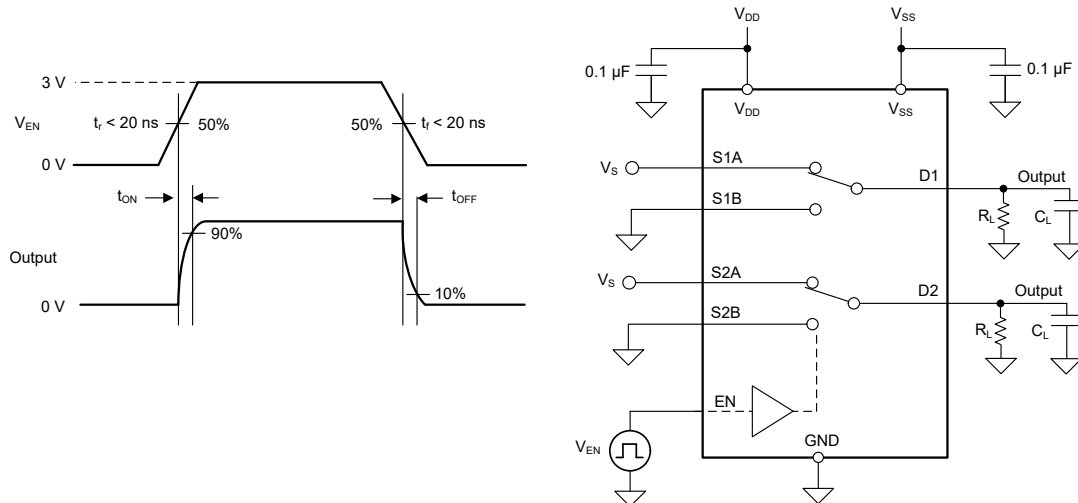


图 6-5. Turn-On and Turn-Off Time Measurement Setup

## 6.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 6-6 shows the setup used to measure break-before-make delay, denoted by the symbol  $t_{OPEN(BBM)}$ .

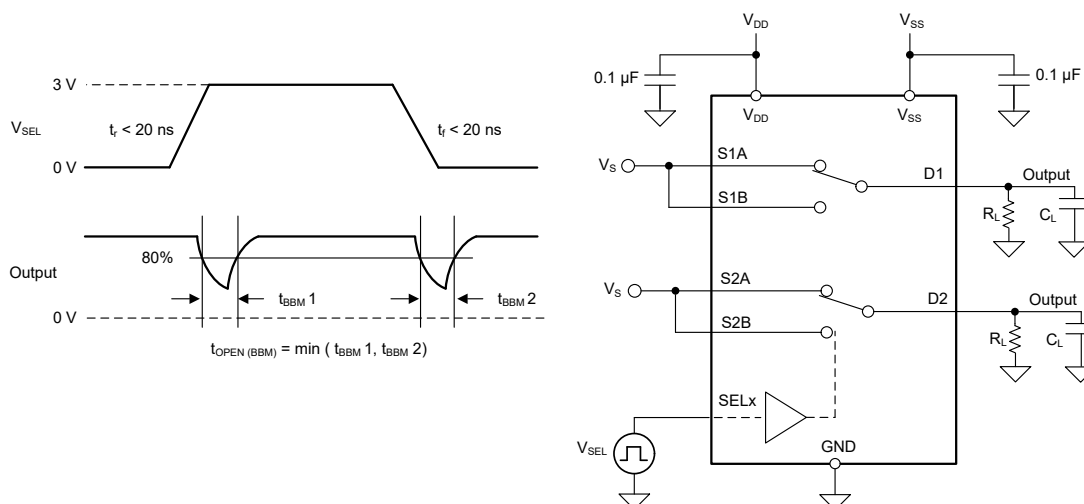


图 6-6. Break-Before-Make Delay Measurement Setup

## 6.7 $t_{ON}(V_{DD})$ Time

The  $t_{ON}(V_{DD})$  time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. 图 6-7 shows the setup used to measure turn on time, denoted by the symbol  $t_{ON}(V_{DD})$ .

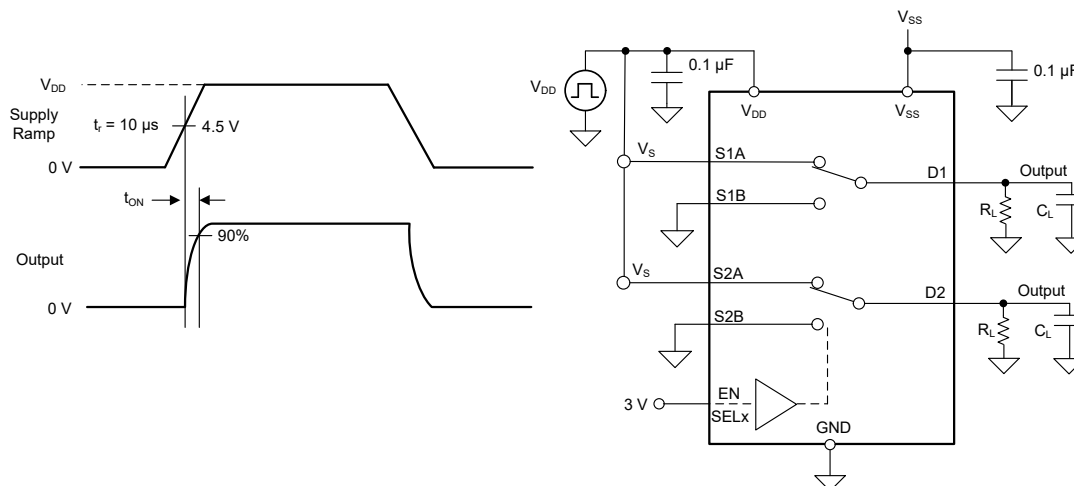


图 6-7.  $t_{ON}(V_{DD})$  Time Measurement Setup

## 6.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. 图 6-8 shows the setup used to measure propagation delay, denoted by the symbol  $t_{PD}$ .

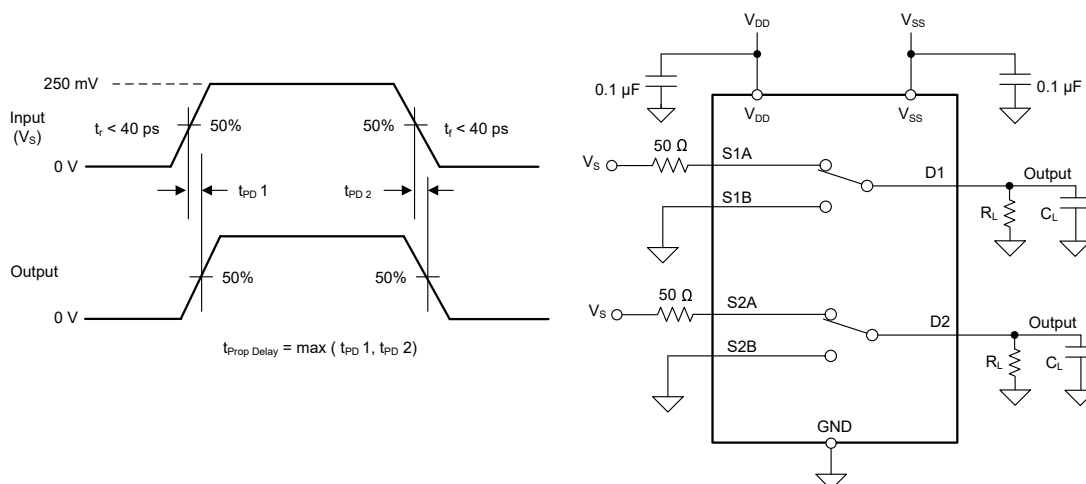


图 6-8. Propagation Delay Measurement Setup

## 6.9 Charge Injection

The TMUX7236 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol  $Q_{INJ}$ . 图 6-9 shows the setup used to measure charge injection from source ( $S_x$ ) to drain ( $D$ ).

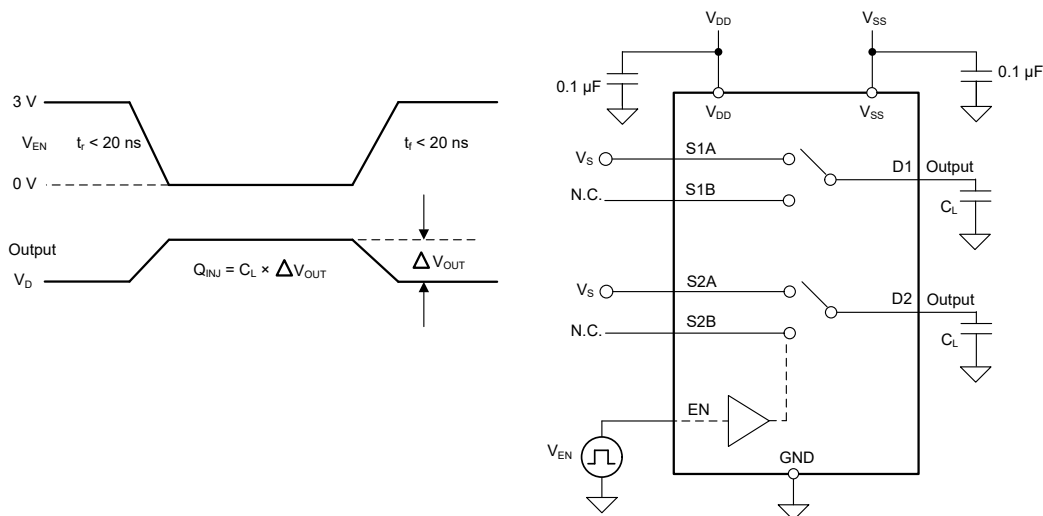


图 6-9. Charge-Injection Measurement Setup

## 6.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin ( $D$ ) of the device when a signal is applied to the source pin ( $S_x$ ) of an off-channel. 图 6-10 shows the setup used to measure, and the equation used to calculate off isolation.

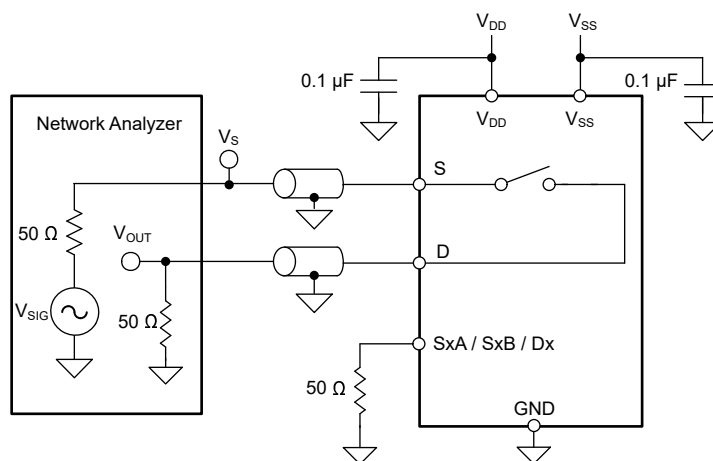


图 6-10. Off Isolation Measurement Setup

## 6.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 6-11 shows the setup used to measure and the equation used to calculate crosstalk.

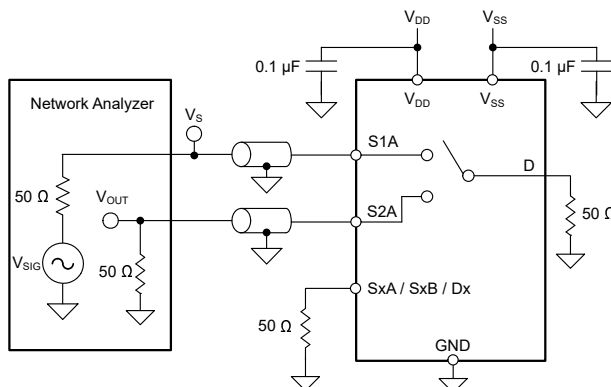


图 6-11. Crosstalk Measurement Setup

## 6.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 6-12 shows the setup used to measure bandwidth.

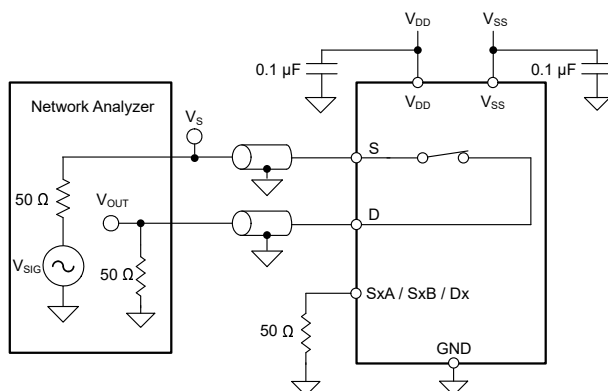


图 6-12. Bandwidth Measurement Setup



## 6.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD.

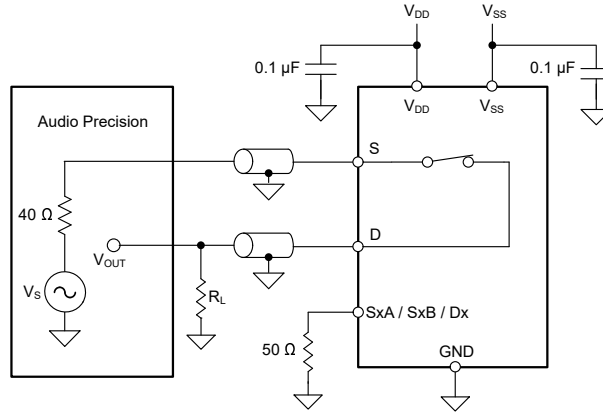


图 6-13. THD Measurement Setup

## 6.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

图 6-14 shows how the decoupling capacitors reduce high frequency noise on the supply pins. This helps stabilize the supply and immediately filter as much of the supply noise as possible.

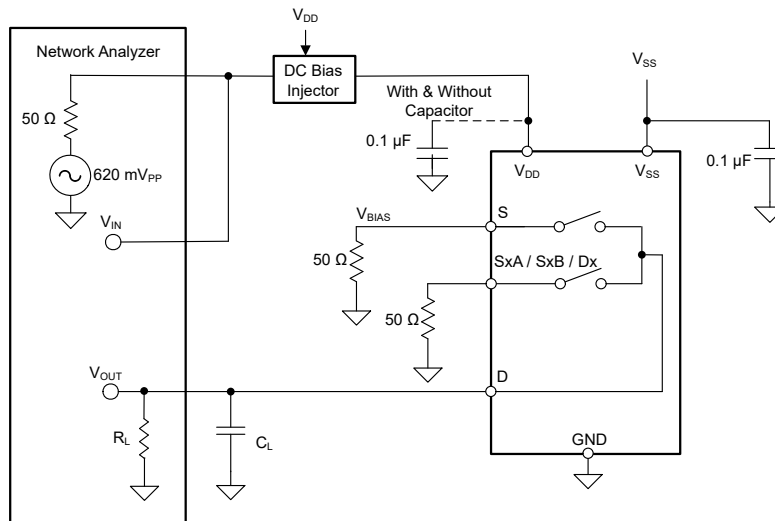
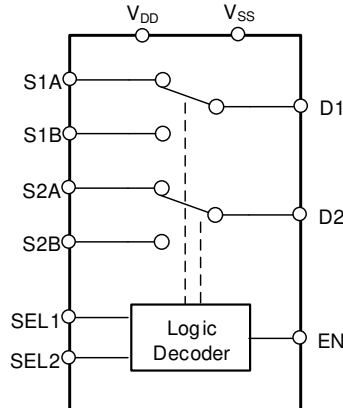


图 6-14. ACPSRR Measurement Setup

## 7 Detailed Description

### 7.1 Functional Block Diagram

The TMUX7236 is a 2:1, 2-channel multiplexer or demultiplexer. Each input is turned on or turned off based on the state of the select lines and enable pin.



### 7.2 Feature Description

#### 7.2.1 Bidirectional Operation

The TMUX7236 conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

#### 7.2.2 Rail to Rail Operation

The valid signal path input or output voltage for TMUX7236 ranges from  $V_{SS}$  to  $V_{DD}$ .

#### 7.2.3 1.8 V Logic Compatible Inputs

The TMUX7236 has 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the TMUX7236 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and bill of materials (BOM) cost. For more information on 1.8 V logic implementations, refer to [Simplifying Design with 1.8 V logic Muxes and Switches](#).

#### 7.2.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX7236 has internal weak pull-down resistors to GND so that the logic pins are not left floating. The value of this pull-down resistor is approximately  $4\text{ M}\Omega$ , but is clamped to about  $1\text{ }\mu\text{A}$  at higher voltages. This feature integrates up to three external components and reduces system size and cost.

#### 7.2.5 Fail-Safe Logic

The TMUX7236 supports Fail-Safe Logic on the control input pins (EN and SEL) allowing the device to operate up to 44 V above  $V_{SS}$ , regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX7236 to be ramped to +44 V while  $V_{DD}$  and  $V_{SS} = 0\text{ V}$ . The logic control inputs are protected against positive faults of up to +44 V in the powered-off condition, but does not offer protection against negative overvoltage conditions.

## 7.2.6 Latch-Up Immune

Latch-up is a condition where a low impedance path is created between a supply pin and ground. The latch-up condition is caused by a trigger (current injection or overvoltage); but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX7236 is constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX7236 to be used in harsh environments. For more information on latch-up immunity, refer to [Using Latch Up Immune Multiplexers to Help Improve System Reliability](#).

## 7.2.7 Ultra-Low Charge Injection

图 7-1 shows how the TMUX7236 device has a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

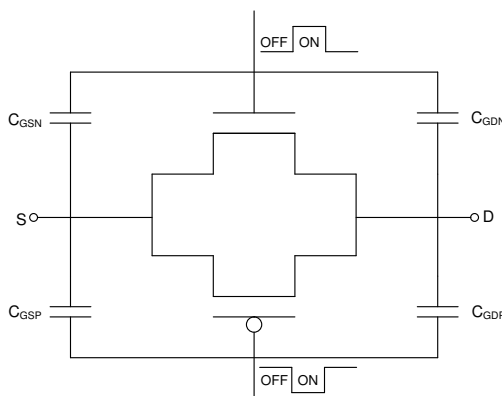


图 7-1. Transmission Gate Topology

The TMUX7236 contains specialized architecture to reduce charge injection on the Drain (Dx). To further reduce charge injection in a sensitive application, a compensation capacitor ( $C_p$ ) can be added on the Source (Sx). This will push excess charge from the switch transition into the compensation capacitor on the Source (Sx) instead of the Drain (Dx). As a general rule,  $C_p$  should be 20x larger than the equivalent load capacitance on the Drain (Dx). 图 7-2 shows charge injection variation with different compensation capacitors on the Source side. 图 7-2 was captured on the TMUX7219 as part of the TMUX72xx family with a 100 pF load capacitance.

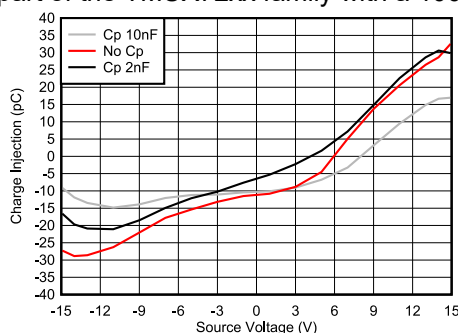


图 7-2. Charge Injection Compensation

## 7.3 Device Functional Modes

When the EN pin of the TMUX7236 is pulled high, one of the switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both of the switches are in an open state regardless of the state of the SEL pin. The control pins can be as high as 44 V.

## 7.4 Truth Tables

表 7-1 show the truth tables for the TMUX7236.

表 7-1. TMUX7236 Truth Table

EN	SELx	Selected Input Connected To Drain (D) Pin
0	X <sup>(1)</sup>	All channels are off (Hi-Z)
1	0	SxB
1	1	SxA

(1) X denotes *do not care*.

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

### 8.1 Application Information

The TMUX7236 is part of the precision switches and multiplexers family of devices. This device operates with dual supplies ( $\pm 4.5$  V to  $\pm 22$  V), a single supply (4.5 V and 44 V), or asymmetric supplies (such as,  $V_{DD} = 12$  V and  $V_{SS} = -5$  V), and offers rail-to-rail input and output. The TMUX7236 offers low  $R_{ON}$ , low on and off leakage currents and ultra-low charge injection performance. These features makes the TMUX7236 a precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

### 8.2 Typical Application

One application for the TMUX7236 is in data acquisition systems. For these types of input modules, accuracy and precision is key. To help account for drift over time and temperature, a calibration path is often added to calibrate the input in real time before a measurement. An SPDT switch can be used to switch in this calibration path, which the TMUX7236 is an excellent choice for. This device offers a very low on-resistance, leakage, and charge injection, which allows for a high measurement fidelity and reduces error. The break-before-make feature allows switching from the calibration path without shorting the inputs together. This device also offers on-resistance mismatch, which makes this device suitable for high precision systems. As 图 8-1 shows, the TMUX7236 can be used in both voltage and current acquisition.

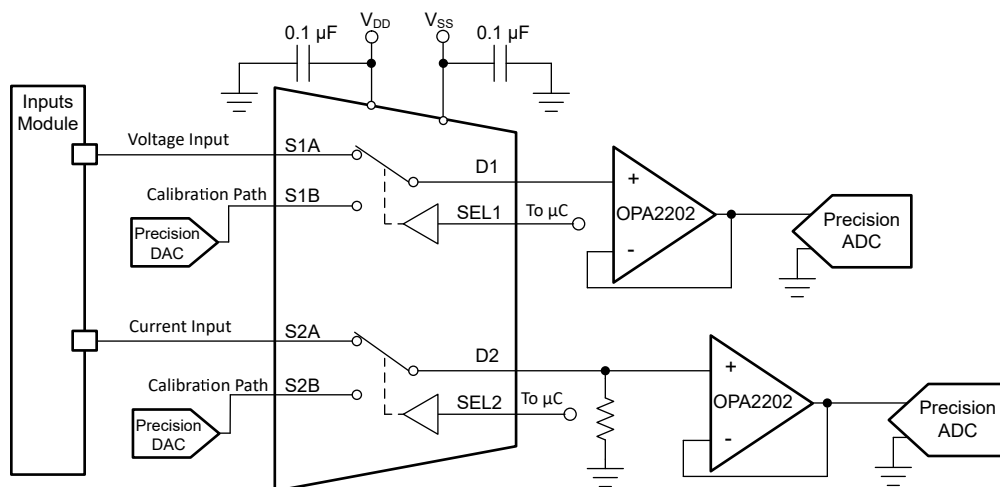


图 8-1. Data Acquisition Systems (DAQ) Calibration

## 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

表 8-1. Design Parameters

PARAMETERS	VALUES
Supply ( $V_{DD}$ )	15 V
Supply ( $V_{SS}$ )	-15 V
MUX I/O signal range	-15 V to 15 V (Rail-to-Rail)
Control logic thresholds	1.8 V compatible (up to $V_{DD}$ )
EN	EN pulled high to enable the switch

## 8.2.2 Detailed Design Procedure

The TMUX7236 can operate without any external components except for the supply decoupling capacitors. All inputs passing through the switch must fall within the recommended operating conditions of the TMUX7236, including signal range and continuous current. The signal range for this design can be up to -15 V to +15 V and the maximum continuous current can be up to 330 mA for wide-range current measurement with a positive supply of 15 V on  $V_{DD}$  and negative supply of -15 V on  $V_{SS}$  (for more information, see 节 5.4). The TMUX7236 device is a bidirectional, single-pole double-throw (SPDT) switch that offers low on-resistance, low leakage, and low power. These features make this device suitable for precision and power sensitive applications.

## 8.2.3 Application Curve

The low on-resistance of TMUX7236 and ultra-low charge injection performance make this device ideal for implementing high precision systems. 图 8-2 shows the plot for the on-resistance versus temperature. Additionally, the TMUX7236 features a very low mismatch between channels, which is important for this application because it reduces the difference between the calibration and non-calibration paths. The TMUX7236 features mismatch between channels <180 m $\Omega$  and 100 m $\Omega$  typically.

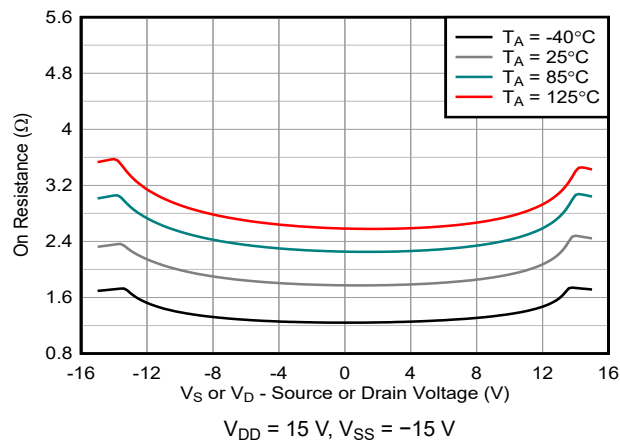


图 8-2. On-Resistance vs Temperature

### 8.2.3.1 On-Resistance Mismatch Between Channels

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$  (unless otherwise noted)

Typical at  $V_{DD} = +15\text{ V}$ ,  $V_{SS} = -15\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT
$\Delta R_{ON}$	On-resistance mismatch between channels	$V_S = -10\text{ V to }+10\text{ V}$ $I_D = -10\text{ mA}$ Refer to <a href="#">On-Resistance</a>	25°C		0.1	0.18	$\Omega$
			-40°C to +85°C			0.19	$\Omega$
			-40°C to +125°C			0.21	$\Omega$

### 8.3 Power Supply Recommendations

The TMUX7236 operates across a wide supply range of  $\pm 4.5\text{ V}$  to  $\pm 22\text{ V}$  (4.5 V to 44 V in single-supply mode). The device also performs well with asymmetrical supplies such as  $V_{DD} = 12\text{ V}$  and  $V_{SS} = -5\text{ V}$ .

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from  $0.1\text{ }\mu\text{F}$  to  $10\text{ }\mu\text{F}$  at both the  $V_{DD}$  and  $V_{SS}$  pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes. Always ensure the ground (GND) connection is established before supplies are ramped.

## 8.4 Layout

### 8.4.1 Layout Guidelines

When a PCB trace turns a corner at a  $90^\circ$  angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 8-3 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

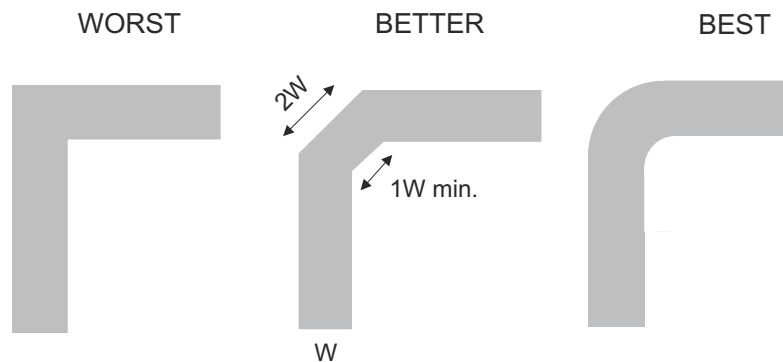


图 8-3. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Some key considerations are as follows:

- For reliable operation, connect a decoupling capacitor ranging from  $0.1\text{ }\mu\text{F}$  to  $10\text{ }\mu\text{F}$  between  $V_{DD}/V_{SS}$  and GND. TI recommends a  $0.1\text{-}\mu\text{F}$  and  $1\text{-}\mu\text{F}$  capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.



- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

#### 8.4.2 Layout Example

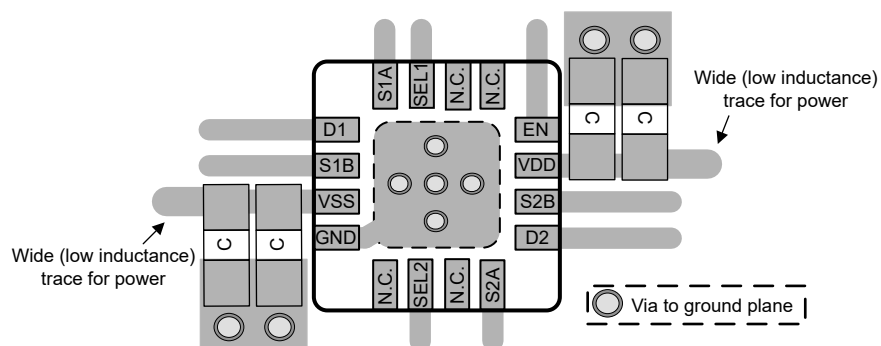


图 8-4. TMUX7236RUM Layout Example

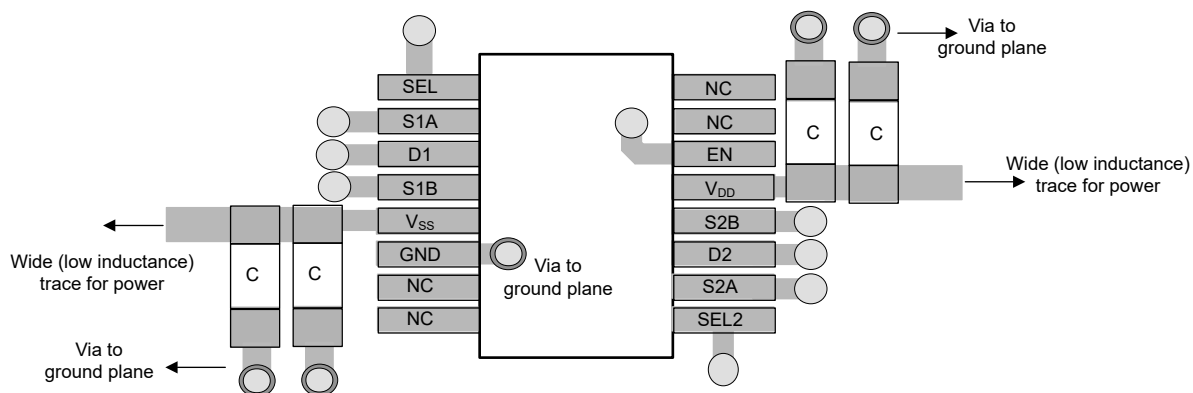


图 8-5. TMUX7236PW Layout Example

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Eliminate Power Sequencing with Powered-off Protection Signal Switches](#)
- Texas Instruments, [Improve Stability Issues with Low CON Multiplexers](#)
- Texas Instruments, [QFN/SON PCB Attachment](#)
- Texas Instruments, [Quad Flatpack No-Lead Logic Packages](#)
- Texas Instruments, [Simplifying Design with 1.8 V logic Muxes and Switches](#)
- Texas Instruments, [System-Level Protection for High-Voltage Analog Multiplexers](#)
- Texas Instruments, [True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit](#)

#### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 9.3 支持资源

**TI E2E™ 中文支持论坛** 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

#### 9.4 Trademarks

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#### 9.5 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

#### 9.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (July 2022) to Revision B (December 2023)	Page
• 添加了 <i>PW</i> 封装信息.....	1
Changes from Revision * (March 2022) to Revision A (July 2022)	Page
• 将数据表的状态从 <i>预告信息</i> 更改为 “ <i>量产数据</i> ” .....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">TMUX7236PWR</a>	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T236
TMUX7236PWR.B	Active	Production	TSSOP (PW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T236
<a href="#">TMUX7236RUMR</a>	Active	Production	WQFN (RUM)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX T236
TMUX7236RUMR.B	Active	Production	WQFN (RUM)   16	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX T236

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7236PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX7236RUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7236PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
TMUX7236RUMR	WQFN	RUM	16	3000	367.0	367.0	35.0

## GENERIC PACKAGE VIEW

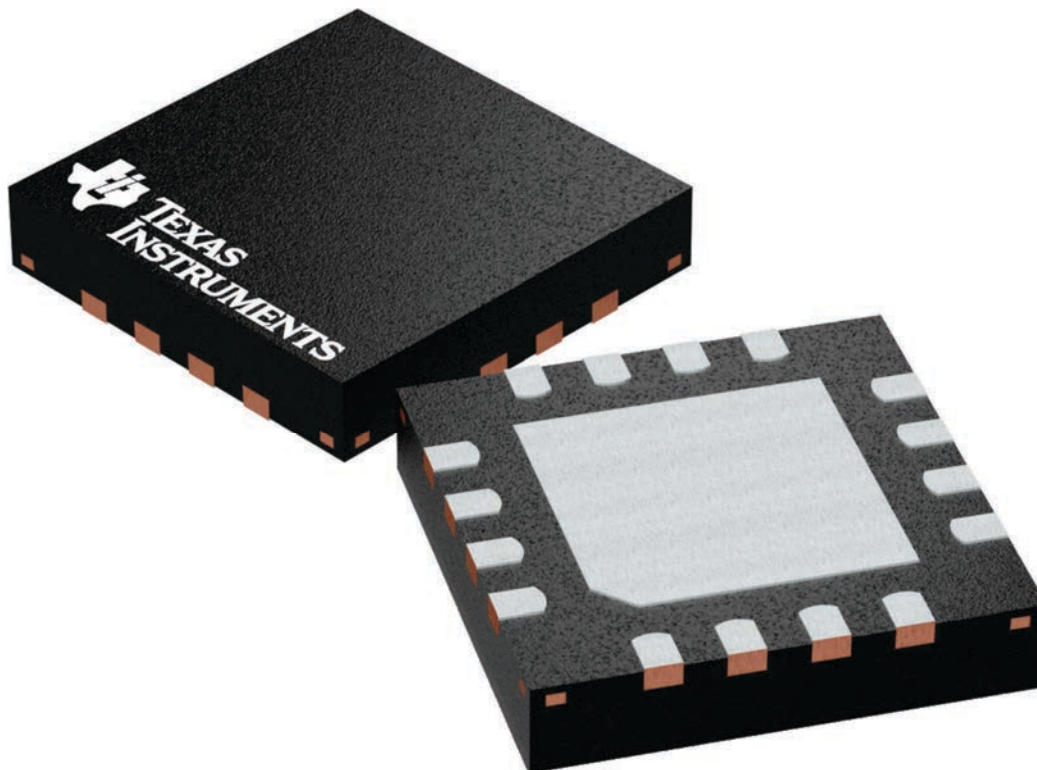
**RUM 16**

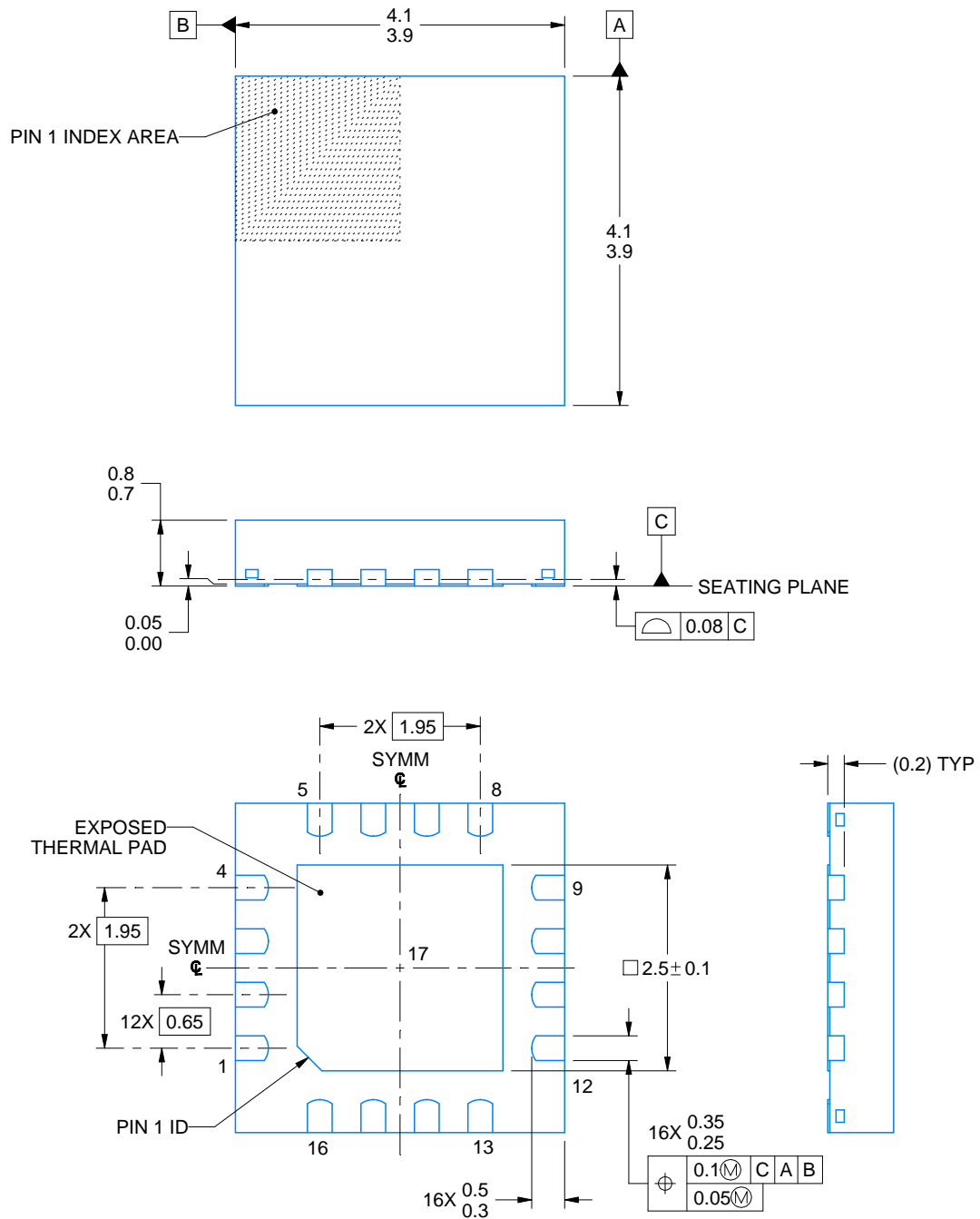
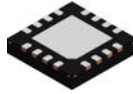
**WQFN - 0.8 mm max height**

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





4224815/A 02/2019

## NOTES:

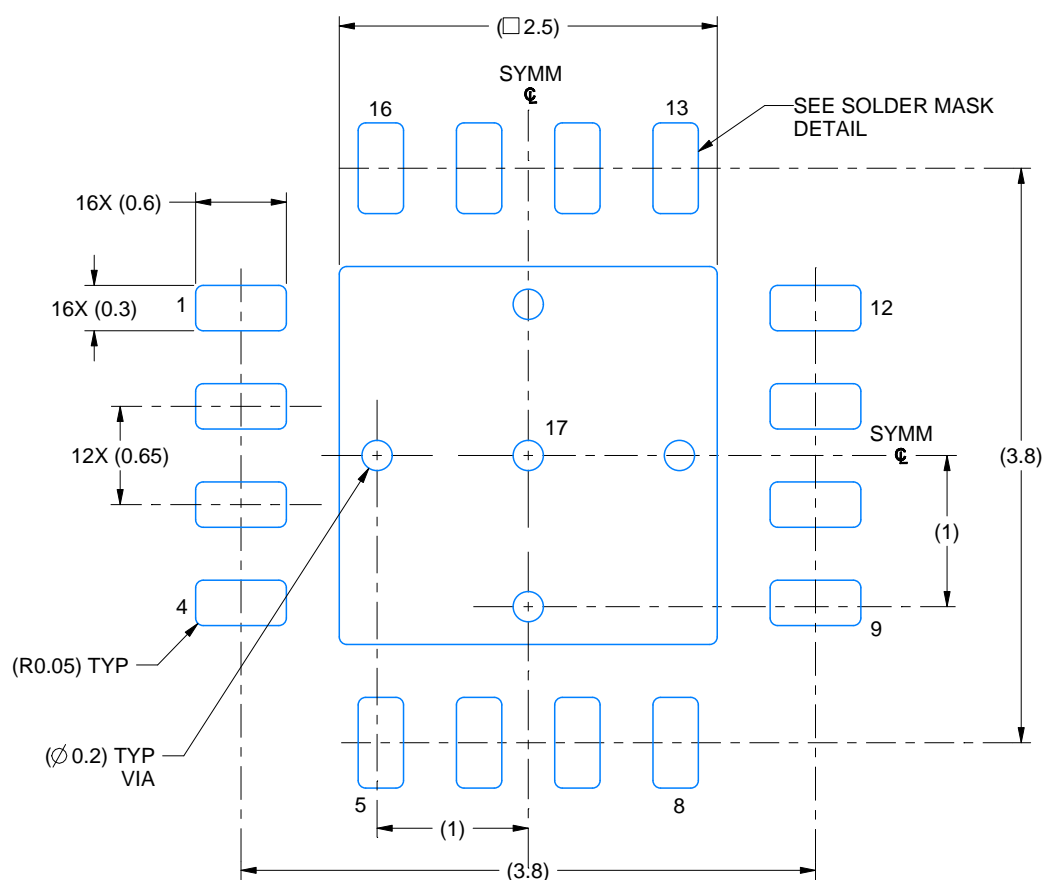
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



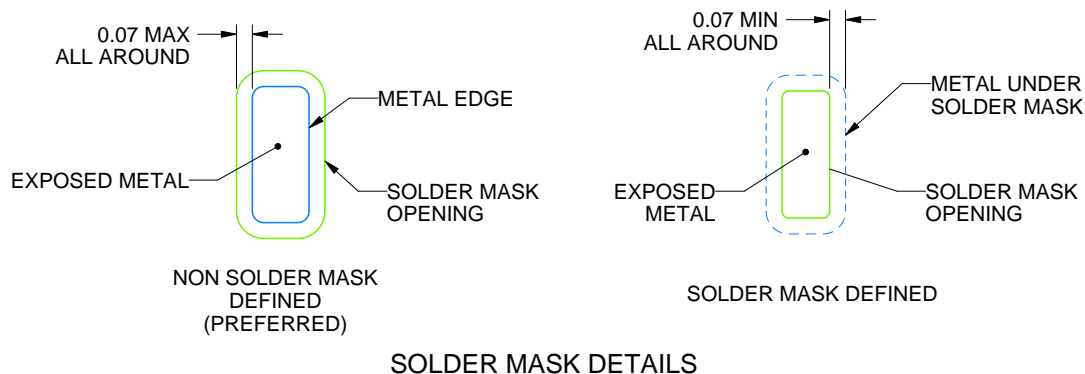
**RUM0016E**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224815/A 02/2019

NOTES: (continued)

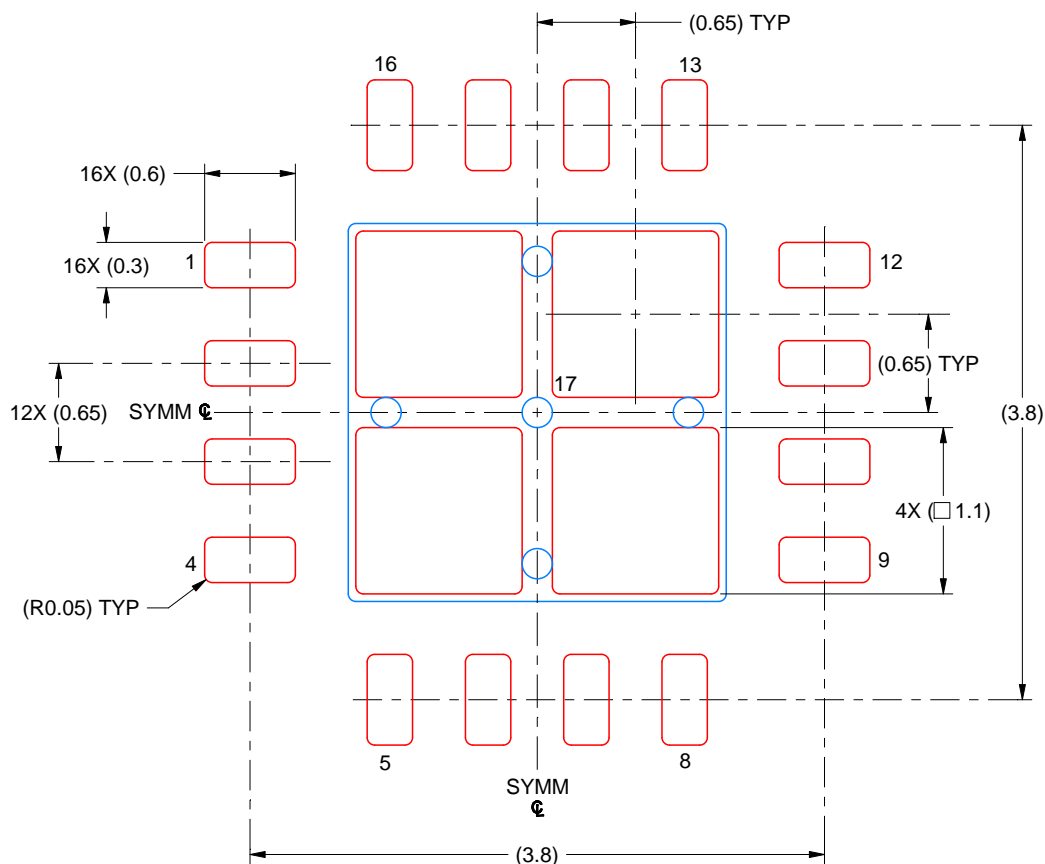
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RUM0016E

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
 BASED ON 0.125 MM THICK STENCIL  
 SCALE: 20X

EXPOSED PAD 17  
 77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224815/A 02/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/B 12/2023

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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