# 具有 1.8V 逻辑电平的 TMUX6219-Q136V、低 Ron、2:1 (SPDT) 开关

## 1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：–40°C 至 125°C 的工作环境温度范围
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 双电源电压范围：±4.5V 至 ±18V
- 单电源电压范围：4.5V 至 36V
- 低导通电阻：2.1Ω
- 低电荷注入：-10pC
- 高电流支持：330mA（最大值）
- 兼容 1.8V 逻辑电平
- 失效防护逻辑
- 轨至轨运行
- 双向信号路径
- 先断后合开关

## 2 应用

- 电动汽车充电站电源模块
- 高级驾驶辅助系统 (ADAS)
- 汽车网关
- 模拟和数字多路复用/多路信号分离
- 汽车音响主机
- 远程信息处理控制单元
- 紧急呼叫 (eCall)
- 信息娱乐系统
- 车身控制模块 (BCM)
- 车身电子装置和照明
- 电池管理系统 (BMS)
- HVAC 控制器模块
- ADAS 域控制器

## 3 说明

TMUX6219-Q1 是一款互补金属氧化物半导体 (CMOS) 开关，采用单通道 2:1 (SPDT) 配置。此器件在单电源（4.5V 至 36V）、双电源（±4.5V 至 ±18V）或非对称电源（例如 $V_{DD}$ = 8V，$V_{SS}$ = -12V）供电时均能正常运行。TMUX6219-Q1 可在源极 (Sx) 和漏极 (D) 引脚上支持从 $V_{SS}$ 到 $V_{DD}$ 范围的双向模拟和数字信号。

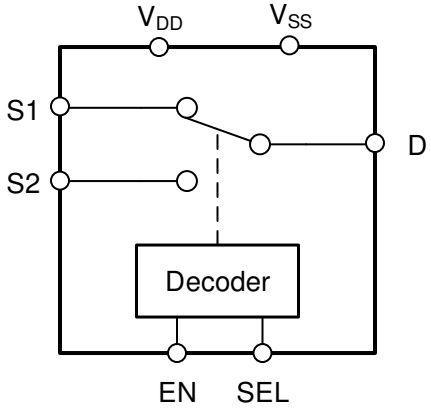
可以通过控制 EN 引脚来启用或禁用 TMUX6219-Q1。当禁用时，两个信号路径开关都断开。当启用时，SEL 引脚可用于导通信号路径 1（S1 至 D）或信号路径 2（S2 至 D）。所有逻辑控制输入均支持 1.8V 到 $V_{DD}$ 的逻辑电平，因此，当器件在有效电源电压范围内运行时，可确保 TTL 和 CMOS 逻辑兼容性。失效防护逻辑电路允许先在控制引脚上施加电压，然后在电源引脚上施加电压，从而保护器件免受潜在的损害。

TMUX6219-Q1 是精密开关和多路复用器系列器件。这些器件具有非常低的导通和关断泄漏电流以及较低的电荷注入，因此可用于高精度测量应用。

**器件信息**(1)

| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| TMUX6219-Q1 | VSSOP (8) (DGK) | 3.00mm × 3.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




**TMUX6219-Q1 方框图**

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

# Table of Contents

**1 特性** ..... 1
**2 应用** ..... 1
**3 说明** ..... 1
**4 Revision History** ..... 2
**5 Pin Configuration and Functions** ..... 3
**6 Specifications** ..... 4
6.1 Absolute Maximum Ratings ..... 4
6.2 ESD Ratings ..... 4
6.3 Thermal Information ..... 4
6.4 Recommended Operating Conditions ..... 5
6.5 Source or Drain Continuous Current ..... 5
6.6 ±15 V Dual Supply: Electrical Characteristics ..... 6
6.7 ±15 V Dual Supply: Switching Characteristics ..... 7
6.8 36 V Single Supply: Electrical Characteristics ..... 9
6.9 36 V Single Supply: Switching Characteristics ..... 10
6.10 12 V Single Supply: Electrical Characteristics ..... 12
6.11 12 V Single Supply: Switching Characteristics ..... 13
6.12 ±5 V Dual Supply: Electrical Characteristics ..... 15
6.13 ±5 V Dual Supply: Switching Characteristics ..... 16
6.14 Typical Characteristics ..... 18
**7 Parameter Measurement Information** ..... 23
7.1 On-Resistance ..... 23
7.2 Off-Leakage Current ..... 23
7.3 On-Leakage Current ..... 24
7.4 Transition Time ..... 24
7.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$ ..... 25
7.6 Break-Before-Make ..... 25
7.7 $t_{ON (VDD)}$ Time ..... 26
7.8 Propagation Delay ..... 26
7.9 Charge Injection ..... 27
7.10 Off Isolation ..... 27
7.11 Crosstalk ..... 28
7.12 Bandwidth ..... 28
7.13 THD + Noise ..... 29
7.14 Power Supply Rejection Ratio (PSRR) ..... 29
**8 Detailed Description** ..... 30
8.1 Overview ..... 30
8.2 Functional Block Diagram ..... 30
8.3 Feature Description ..... 30
8.4 Device Functional Modes ..... 32
8.5 Truth Tables ..... 32
**9 Application and Implementation** ..... 33
9.1 Application Information ..... 33
9.2 Typical Application ..... 33
**10 Power Supply Recommendations** ..... 34
**11 Layout** ..... 35
11.1 Layout Guidelines ..... 35
11.2 Layout Example ..... 35
**12 Device and Documentation Support** ..... 36
12.1 Documentation Support ..... 36
12.2 Receiving Notification of Documentation Updates ..... 36
12.3 支持资源 ..... 36
12.4 Trademarks ..... 36
12.5 Electrostatic Discharge Caution ..... 36
12.6 Glossary ..... 36
**13 Mechanical, Packaging, and Orderable Information** ..... 36

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (January 2021) to Revision A (June 2021) | Page |
|---|---|


Copyright © 2021 Texas Instruments Incorporated

# 5 Pin Configuration and Functions

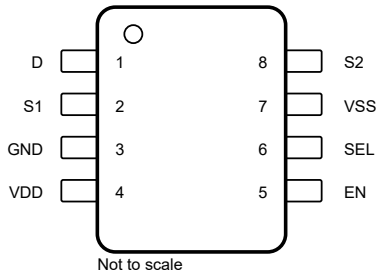



**图 5-1. DGK Package**
**8-Pin VSSOP**
**Top View**

**Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION(2) |
|---|---|---|---|
| NAME | DGK | | |
| D | 1 | I/O | Drain pin. Can be an input or output. |
| EN | 5 | I | Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the SEL logic input determine which switch is turned on. |
| GND | 3 | P | Ground (0 V) reference |
| S1 | 2 | I/O | Source pin 1. Can be an input or output. |
| S2 | 8 | I/O | Source pin 2. Can be an input or output. |
| SEL | 6 | I | Logic control input, has internal pull-down resistor. Controls the switch connection as shown in 表 8-1. |
| $V_{DD}$ | 4 | P | Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{DD}$ and GND. |
| $V_{SS}$ | 7 | P | Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{SS}$ and GND. |

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to 节 8.4 for what to do with unused pins.

Copyright © 2021 Texas Instruments Incorporated

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ – $V_{SS}$ | Power supply voltage differential | | 38 | V |
| $V_{DD}$ | Supply voltage | – 0.5 | 38 | V |
| $V_{SS}$ | Supply voltage | – 38 | 0.5 | V |
| $V_{SEL}$ or $V_{EN}$ | Logic control input pin voltage (SEL, EN)(3) | – 0.5 | 38 | V |
| $I_{SEL}$ or $I_{EN}$ | Logic control input pin current (SEL, EN)(3) | – 30 | 30 | mA |
| $V_S$ or $V_D$ | Source or drain voltage (Sx, D)(3) | $V_{SS}$ – 0.5 | $V_{DD}$+0.5 | V |
| $I_{IK}$ | Diode clamp current(3) | – 30 | 30 | mA |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, D) | | $I_{DC}$ + 10 %(4) | mA |
| $T_A$ | Ambient temperature | – 55 | 150 | °C |
| $T_{stg}$ | Storage temperature | – 65 | 150 | °C |
| $T_J$ | Junction temperature | | 150 | °C |
| $P_{tot}$ | Total power dissipation(5) | | 460 | mW |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for $I_{DC}$ specifications.
(5) For DGK package: $P_{tot}$ derates linearly above $T_A$ = 70°C by 6.7mW/°C.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2) | ±500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Thermal Information

| THERMAL METRIC(1) | | TMUX6219-Q1 DGK (VSSOP) 8 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 152.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 73.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 4.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 71.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.


Copyright © 2021 Texas Instruments Incorporated

## 6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ - $V_{SS}$ (1) | Power supply voltage differential | 4.5 | | 36 | V |
| $V_{DD}$ | Positive power supply voltage | 4.5 | | 36 | V |
| $V_S$ or $V_D$ | Signal path input/output voltage (source or drain pin) (Sx, D) | $V_{SS}$ | | $V_{DD}$ | V |
| $V_{SEL}$ or $V_{EN}$ | Address or enable pin voltage | 0 | | 36 | V |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, D) | | | $I_{DC}$ (2) | mA |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |

(1) $V_{DD}$ and $V_{SS}$ can be any value as long as 4.5 V ⩽ ($V_{DD}$ – $V_{SS}$) ⩽ 36 V, and the minimum $V_{DD}$ is met.
(2) Refer to *Source or Drain Continuous Current* table for $I_{DC}$ specifications.

## 6.5 Source or Drain Continuous Current

at supply voltage of $V_{DD}$ ± 10%, $V_{SS}$ ± 10 % (unless otherwise noted)

| CONTINUOUS CURRENT PER CHANNEL ($I_{DC}$) | | $T_A$ = 25°C | $T_A$ = 85°C | $T_A$ = 125°C | UNIT |
|---|---|---|---|---|---|
| PACKAGE | TEST CONDITIONS | | | | |
| DGK (VSSOP) | ±15 V Dual Supply | 330 | 210 | 120 | mA |
| | +36 V Single Supply(1) | 300 | 190 | 110 | mA |
| | +12 V Single Supply | 240 | 160 | 100 | mA |
| | ±5 V Dual Supply | 240 | 160 | 100 | mA |
| | +5 V Single Supply | 180 | 120 | 80 | mA |

(1) Specified for nominal supply voltage only.

Copyright © 2021 Texas Instruments Incorporated

## 6.6 ±15 V Dual Supply: Electrical Characteristics

$V_{DD}$ = +15 V ± 10%, $V_{SS}$ = – 15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +15 V, $V_{SS}$ = – 15 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = – 10 V to +10 V<br>$I_D$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 2.1 | 2.9 | Ω |
| | | | – 40°C to +85°C | | | 3.8 | Ω |
| | | | – 40°C to +125°C | | | 4.5 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = – 10 V to +10 V<br>$I_D$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 0.05 | 0.25 | Ω |
| | | | – 40°C to +85°C | | | 0.3 | Ω |
| | | | – 40°C to +125°C | | | 0.35 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = – 10 V to +10 V<br>$I_S$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 0.5 | 0.6 | Ω |
| | | | – 40°C to +85°C | | | 0.7 | Ω |
| | | | – 40°C to +125°C | | | 0.85 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 0 V, $I_S$ = – 10 mA<br>Refer to On-Resistance | – 40°C to +125°C | | 0.01 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Switch state is off<br>$V_S$ = +10 V / – 10 V<br>$V_D$ = – 10 V / + 10 V<br>Refer to Off-Leakage Current | 25°C | – 0.3 | 0.1 | 0.3 | nA |
| | | | – 40°C to +85°C | – 3 | | 3 | nA |
| | | | – 40°C to +125°C | – 50 | | 50 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Switch state is off<br>$V_S$ = +10 V / – 10 V<br>$V_D$ = – 10 V / + 10 V<br>Refer to Off-Leakage Current | 25°C | – 2 | 0.1 | 2 | nA |
| | | | – 40°C to +85°C | – 5 | | 5 | nA |
| | | | – 40°C to +125°C | – 70 | | 70 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Switch state is on<br>$V_S$ = $V_D$ = ±10 V<br>Refer to On-Leakage Current | 25°C | – 2 | 0.1 | 2 | nA |
| | | | – 40°C to +85°C | – 5 | | 5 | nA |
| | | | – 40°C to +125°C | – 70 | | 70 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | – 40°C to +125°C | 1.3 | | 36 | V |
| $V_{IL}$ | Logic voltage low | | – 40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | – 40°C to +125°C | | 0.005 | 1 | µA |
| $I_{IL}$ | Input leakage current | | – 40°C to +125°C | – 1 | – 0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | – 40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 30 | 40 | µA |
| | | | – 40°C to +85°C | | | 48 | µA |
| | | | – 40°C to +125°C | | | 62 | µA |
| $I_{SS}$ | $V_{SS}$ supply current | $V_{DD}$ = 16.5 V, $V_{SS}$ = – 16.5 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 3 | 10 | µA |
| | | | – 40°C to +85°C | | | 15 | µA |
| | | | – 40°C to +125°C | | | 25 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.


Copyright © 2021 Texas Instruments Incorporated

## 6.7 ±15 V Dual Supply: Switching Characteristics

$V_{DD}$ = +15 V ± 10%, $V_{SS}$ = – 15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +15 V, $V_{SS}$ = – 15 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Transition Time | 25°C | | 120 | 175 | ns |
| | | | – 40°C to +85°C | | | 190 | ns |
| | | | – 40°C to +125°C | | | 210 | ns |
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 100 | 170 | ns |
| | | | – 40°C to +85°C | | | 185 | ns |
| | | | – 40°C to +125°C | | | 200 | ns |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 10 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 100 | 180 | ns |
| | | | – 40°C to +85°C | | | 195 | ns |
| | | | – 40°C to +125°C | | | 210 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 10 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Break-Before-Make | 25°C | | 50 | | ns |
| | | | – 40°C to +85°C | 1 | | | ns |
| | | | – 40°C to +125°C | 1 | | | ns |
| $T_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 100ns<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on (VDD) Time | 25°C | | 0.19 | | ms |
| | | | – 40°C to +85°C | | 0.2 | | ms |
| | | | – 40°C to +125°C | | 0.2 | | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>Refer to Propagation Delay | 25°C | | 700 | | ps |
| $Q_{INJ}$ | Charge injection | $V_D$ = 0 V, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | – 10 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 100 kHz<br>Refer to Off Isolation | 25°C | | – 75 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1 MHz<br>Refer to Off Isolation | 25°C | | – 55 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 100 kHz<br>Refer to Crosstalk | 25°C | | – 117 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1MHz<br>Refer to Crosstalk | 25°C | | – 106 | | dB |
| BW | – 3dB Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V<br>Refer to Bandwidth | 25°C | | 40 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1 MHz | 25°C | | – 0.18 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62 V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 50 Ω, $C_L$ = 5 pF,<br>f = 1 MHz<br>Refer to ACPSRR | 25°C | | – 64 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 15 V, $V_{BIAS}$ = 0 V<br>$R_L$ = 10 kΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.0005 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 33 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 48 | | pF |

Copyright © 2021 Texas Instruments Incorporated

$V_{DD}$ = +15 V ± 10%, $V_{SS}$ = – 15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +15 V, $V_{SS}$ = – 15 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 148 | | pF |


Copyright © 2021 Texas Instruments Incorporated

## 6.8 36 V Single Supply: Electrical Characteristics

$V_{DD}$ = +36 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +36 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to 30 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 2.5 | 3.2 | Ω |
| | | | –40°C to +85°C | | | 4.2 | Ω |
| | | | –40°C to +125°C | | | 4.9 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0 V to 30 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 0.1 | 0.2 | Ω |
| | | | –40°C to +85°C | | | 0.25 | Ω |
| | | | –40°C to +125°C | | | 0.3 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V to 30 V<br>$I_S$ = –10 mA<br>Refer to On-Resistance | 25°C | | 0.3 | 1 | Ω |
| | | | –40°C to +85°C | | | 1.5 | Ω |
| | | | –40°C to +125°C | | | 2 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 18 V, $I_S$ = –10 mA<br>Refer to On-Resistance | –40°C to +125°C | | 0.009 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 39.6 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 30 V / 1 V<br>$V_D$ = 1 V / 30 V<br>Refer to Off-Leakage Current | 25°C | –0.5 | 0.1 | 0.5 | nA |
| | | | –40°C to +85°C | –5 | | 5 | nA |
| | | | –40°C to +125°C | –70 | | 70 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 39.6 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 30 V / 1 V<br>$V_D$ = 1 V / 30 V<br>Refer to Off-Leakage Current | 25°C | –2 | 0.1 | 2 | nA |
| | | | –40°C to +85°C | –10 | | 10 | nA |
| | | | –40°C to +125°C | –80 | | 80 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 39.6 V, $V_{SS}$ = 0 V<br>Switch state is on<br>$V_S$ = $V_D$ = 30 V or 1 V<br>Refer to On-Leakage Current | 25°C | –2 | 0.1 | 2 | nA |
| | | | –40°C to +85°C | –10 | | 10 | nA |
| | | | –40°C to +125°C | –80 | | 80 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 36 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | –40°C to +125°C | | 0.005 | 1 | µA |
| $I_{IL}$ | Input leakage current | | –40°C to +125°C | –1 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 39.6 V, $V_{SS}$ = 0 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 28 | 50 | µA |
| | | | –40°C to +85°C | | | 58 | µA |
| | | | –40°C to +125°C | | | 70 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

Copyright © 2021 Texas Instruments Incorporated

## 6.9 36 V Single Supply: Switching Characteristics

$V_{DD}$ = +36 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +36 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 18 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Transition Time | 25°C | | 110 | 170 | ns |
| | | | –40°C to +85°C | | | 185 | ns |
| | | | –40°C to +125°C | | | 200 | ns |
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 18 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 110 | 180 | ns |
| | | | –40°C to +85°C | | | 190 | ns |
| | | | –40°C to +125°C | | | 200 | ns |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 18 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 90 | 180 | ns |
| | | | –40°C to +85°C | | | 195 | ns |
| | | | –40°C to +125°C | | | 200 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 18 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Break-Before-Make | 25°C | | 44 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $T_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 100ns<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on (VDD) Time | 25°C | | 0.17 | | ms |
| | | | –40°C to +85°C | | 0.19 | | ms |
| | | | –40°C to +125°C | | 0.19 | | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>Refer to Propagation Delay | 25°C | | 920 | | ps |
| $Q_{INJ}$ | Charge injection | $V_D$ = 18 V, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | –13 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Off Isolation | 25°C | | –75 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz<br>Refer to Off Isolation | 25°C | | –55 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Crosstalk | 25°C | | –117 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1MHz<br>Refer to Crosstalk | 25°C | | –106 | | dB |
| BW | –3dB Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V,<br>Refer to Bandwidth | 25°C | | 38 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz | 25°C | | –0.19 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62 V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 50 Ω, $C_L$ = 5 pF,<br>f = 1 MHz<br>Refer to ACPSRR | 25°C | | –60 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ =18 V, $V_{BIAS}$ = 18 V<br>$R_L$ = 10 kΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.0004 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 6 V, f = 1 MHz | 25°C | | 35 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 6 V, f = 1 MHz | 25°C | | 49 | | pF |


Copyright © 2021 Texas Instruments Incorporated

$V_{DD}$ = +36 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +36 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 6 V, f = 1 MHz | 25°C | | 146 | | pF |

Copyright © 2021 Texas Instruments Incorporated

## 6.10 12 V Single Supply: Electrical Characteristics

$V_{DD}$ = +12 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +12 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to 10 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 4.6 | 6 | Ω |
| | | | –40°C to +85°C | | | 7.5 | Ω |
| | | | –40°C to +125°C | | | 8.4 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = 0 V to 10 V<br>$I_D$ = –10 mA<br>Refer to On-Resistance | 25°C | | 0.08 | 0.2 | Ω |
| | | | –40°C to +85°C | | | 0.32 | Ω |
| | | | –40°C to +125°C | | | 0.35 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V to 10 V<br>$I_S$ = –10 mA<br>Refer to On-Resistance | 25°C | | 1.2 | 2 | Ω |
| | | | –40°C to +85°C | | | 2.2 | Ω |
| | | | –40°C to +125°C | | | 2.4 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 6 V, $I_S$ = –10 mA<br>Refer to On-Resistance | –40°C to +125°C | | 0.017 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 13.2 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 10 V / 1 V<br>$V_D$ = 1 V / 10 V<br>Refer to Off-Leakage Current | 25°C | –1 | 0.1 | 1 | nA |
| | | | –40°C to +85°C | –5 | | 5 | nA |
| | | | –40°C to +125°C | –50 | | 50 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = 13.2 V, $V_{SS}$ = 0 V<br>Switch state is off<br>$V_S$ = 10 V / 1 V<br>$V_D$ = 1 V / 10 V<br>Refer to Off-Leakage Current | 25°C | –2 | 0.1 | 2 | nA |
| | | | –40°C to +85°C | –5 | | 5 | nA |
| | | | –40°C to +125°C | –70 | | 70 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = 13.2 V, $V_{SS}$ = 0 V<br>Switch state is on<br>$V_S$ = $V_D$ = 10 V or 1 V<br>Refer to On-Leakage Current | 25°C | –2 | 0.1 | 2 | nA |
| | | | –40°C to +85°C | –5 | | 5 | nA |
| | | | –40°C to +125°C | –70 | | 70 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | –40°C to +125°C | 1.3 | | 36 | V |
| $V_{IL}$ | Logic voltage low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | –40°C to +125°C | | 0.005 | 1 | µA |
| $I_{IL}$ | Input leakage current | | –40°C to +125°C | –1 | –0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = 13.2 V, $V_{SS}$ = 0 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 10 | 35 | µA |
| | | | –40°C to +85°C | | | 45 | µA |
| | | | –40°C to +125°C | | | 55 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.


Copyright © 2021 Texas Instruments Incorporated

## 6.11 12 V Single Supply: Switching Characteristics

$V_{DD}$ = +12 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +12 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 8 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Transition Time | 25°C | | 180 | 185 | ns |
| | | | –40°C to +85°C | | | 215 | ns |
| | | | –40°C to +125°C | | | 235 | ns |
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 8 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 120 | 180 | ns |
| | | | –40°C to +85°C | | | 210 | ns |
| | | | –40°C to +125°C | | | 230 | ns |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 8 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 130 | 210 | ns |
| | | | –40°C to +85°C | | | 235 | ns |
| | | | –40°C to +125°C | | | 250 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 8 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Break-Before-Make | 25°C | | 40 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $T_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 100ns<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on (VDD) Time | 25°C | | 0.19 | | ms |
| | | | –40°C to +85°C | | 0.2 | | ms |
| | | | –40°C to +125°C | | 0.2 | | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>Refer to Propagation Delay | 25°C | | 740 | | ps |
| $Q_{INJ}$ | Charge injection | $V_D$ = 6 V, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | –6 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Charge Injection | 25°C | | –75 | | dB |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz<br>Refer to Off Isolation | 25°C | | –55 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 100 kHz<br>Refer to Crosstalk | 25°C | | –117 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1MHz<br>Refer to Crosstalk | 25°C | | –106 | | dB |
| BW | –3dB Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V<br>Refer to Bandwidth | 25°C | | 42 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 6 V, f = 1 MHz | 25°C | | –0.3 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62 V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 50 Ω, $C_L$ = 5 pF,<br>f = 1 MHz<br>Refer to ACPSRR | 25°C | | –65 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 6 V, $V_{BIAS}$ = 6 V<br>$R_L$ = 10 kΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.0009 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 6 V, f = 1 MHz | 25°C | | 38 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 6 V, f = 1 MHz | 25°C | | 56 | | pF |

Copyright © 2021 Texas Instruments Incorporated

$V_{DD}$ = +12 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +12 V, $V_{SS}$ = 0 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 6 V, f = 1 MHz | 25°C | | 150 | | pF |


Copyright © 2021 Texas Instruments Incorporated

## 6.12 ±5 V Dual Supply: Electrical Characteristics

$V_{DD}$ = +5 V ± 10%, $V_{SS}$ = – 5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +5 V, $V_{SS}$ = – 5 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_{DD}$ = +4.5 V, $V_{SS}$ = – 4.5 V<br>$V_S$ = – 4.5 V to +4.5 V<br>$I_D$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 4 | 7.2 | Ω |
| | | | – 40°C to +85°C | | | 8.6 | Ω |
| | | | – 40°C to +125°C | | | 10 | Ω |
| $\Delta R_{ON}$ | On-resistance mismatch between channels | $V_S$ = – 4.5 V to +4.5 V<br>$I_D$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 0.1 | 0.3 | Ω |
| | | | – 40°C to +85°C | | | 0.35 | Ω |
| | | | – 40°C to +125°C | | | 0.4 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = – 4.5 V to +4.5 V<br>$I_D$ = – 10 mA<br>Refer to On-Resistance | 25°C | | 1.3 | 2.2 | Ω |
| | | | – 40°C to +85°C | | | 2.5 | Ω |
| | | | – 40°C to +125°C | | | 2.8 | Ω |
| $R_{ON\ DRIFT}$ | On-resistance drift | $V_S$ = 0 V, $I_S$ = – 10 mA<br>Refer to On-Resistance | – 40°C to +125°C | | 0.019 | | Ω/°C |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = +5.5 V, $V_{SS}$ = – 5.5 V<br>Switch state is off<br>$V_S$ = +4.5 V / – 4.5 V<br>$V_D$ = – 4.5 V / + 4.5 V<br>Refer to Off-Leakage Current | 25°C | – 1 | 0.1 | 1 | nA |
| | | | – 40°C to +85°C | – 4 | | 4 | nA |
| | | | – 40°C to +125°C | – 50 | | 50 | nA |
| $I_{D(OFF)}$ | Drain off leakage current(1) | $V_{DD}$ = +5.5 V, $V_{SS}$ = – 5.5 V<br>Switch state is off<br>$V_S$ = +4.5 V / – 4.5 V<br>$V_D$ = – 4.5 V / + 4.5 V<br>Refer to Off-Leakage Current | 25°C | – 2 | 0.1 | 2 | nA |
| | | | – 40°C to +85°C | – 5 | | 5 | nA |
| | | | – 40°C to +125°C | – 50 | | 50 | nA |
| $I_{S(ON)}$<br>$I_{D(ON)}$ | Channel on leakage current(2) | $V_{DD}$ = +5.5 V, $V_{SS}$ = – 5.5 V<br>Switch state is on<br>$V_S$ = $V_D$ = ±4.5 V<br>Refer to On-Leakage Current | 25°C | – 2 | 0.1 | 2 | nA |
| | | | – 40°C to +85°C | – 5 | | 5 | nA |
| | | | – 40°C to +125°C | – 50 | | 50 | nA |
| **LOGIC INPUTS (SEL / EN pins)** | | | | | | | |
| $V_{IH}$ | Logic voltage high | | – 40°C to +125°C | 1.3 | | 36 | V |
| $V_{IL}$ | Logic voltage low | | – 40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$ | Input leakage current | | – 40°C to +125°C | | 0.005 | 1 | µA |
| $I_{IL}$ | Input leakage current | | – 40°C to +125°C | – 1 | – 0.005 | | µA |
| $C_{IN}$ | Logic input capacitance | | – 40°C to +125°C | | 3 | | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | $V_{DD}$ = +5.5 V, $V_{SS}$ = – 5.5 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 20 | 35 | µA |
| | | | – 40°C to +85°C | | | 40 | µA |
| | | | – 40°C to +125°C | | | 50 | µA |
| $I_{SS}$ | $V_{SS}$ supply current | $V_{DD}$ = +5.5 V, $V_{SS}$ = – 5.5 V<br>Logic inputs = 0 V, 5 V, or $V_{DD}$ | 25°C | | 0.001 | 5 | µA |
| | | | – 40°C to +85°C | | | 8 | µA |
| | | | – 40°C to +125°C | | | 15 | µA |

(1) When $V_S$ is positive, $V_D$ is negative, or when $V_S$ is negative, $V_D$ is positive.
(2) When $V_S$ is at a voltage potential, $V_D$ is floating, or when $V_D$ is at a voltage potential, $V_S$ is floating.

Copyright © 2021 Texas Instruments Incorporated

## 6.13 ±5 V Dual Supply: Switching Characteristics

$V_{DD}$ = +5 V ± 10%, $V_{SS}$ = – 5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +5 V, $V_{SS}$ = – 5 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{TRAN}$ | Transition time from control input | $V_S$ = 3 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Transition Time | 25°C | | 300 | 400 | ns |
| | | | – 40°C to +85°C | | | 490 | ns |
| | | | – 40°C to +125°C | | | 550 | ns |
| $t_{ON\ (EN)}$ | Turn-on time from enable | $V_S$ = 3 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 220 | 300 | ns |
| | | | – 40°C to +85°C | | | 350 | ns |
| | | | – 40°C to +125°C | | | 380 | ns |
| $t_{OFF\ (EN)}$ | Turn-off time from enable | $V_S$ = 3 V<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Turn-on and Turn-off Time | 25°C | | 210 | 280 | ns |
| | | | – 40°C to +85°C | | | 330 | ns |
| | | | – 40°C to +125°C | | | 350 | ns |
| $t_{BBM}$ | Break-before-make time delay | $V_S$ = 3 V,<br>$R_L$ = 300 Ω, $C_L$ = 35 pF<br>Refer to Break-Before-Make | 25°C | | 50 | | ns |
| | | | – 40°C to +85°C | 1 | | | ns |
| | | | – 40°C to +125°C | 1 | | | ns |
| $T_{ON\ (VDD)}$ | Device turn on time ($V_{DD}$ to output) | $V_{DD}$ rise time = 100ns<br>$R_L$ = 300 Ω, $C_L$ = 35pF<br>Refer to Turn-on (VDD) Time | 25°C | | 0.19 | | ms |
| | | | – 40°C to +85°C | | 0.19 | 1 | ms |
| | | | – 40°C to +125°C | | 0.19 | 1 | ms |
| $t_{PD}$ | Propagation delay | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>Refer to Propagation Delay | 25°C | | 650 | | ps |
| $Q_{INJ}$ | Charge injection | $V_D$ = 0 V, $C_L$ = 1 nF<br>Refer to Charge Injection | 25°C | | – 5 | | pC |
| $O_{ISO}$ | Off-isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1 MHz<br>Refer to Off Isolation | 25°C | | – 55 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 100 kHz<br>Refer to Crosstalk | 25°C | | – 117 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1MHz<br>Refer to Crosstalk | 25°C | | – 106 | | dB |
| BW | – 3dB Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V,<br>Refer to Bandwidth | 25°C | | 43 | | MHz |
| $I_L$ | Insertion loss | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>$V_S$ = 0 V, f = 1 MHz | 25°C | | – 0.35 | | dB |
| ACPSRR | AC Power Supply Rejection Ratio | $V_{PP}$ = 0.62 V on $V_{DD}$ and $V_{SS}$<br>$R_L$ = 50 Ω, $C_L$ = 5 pF,<br>f = 1 MHz<br>Refer to ACPSRR | 25°C | | – 68 | | dB |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 5 V, $V_{BIAS}$ = 0 V<br>$R_L$ = 10 kΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.001 | | % |
| THD+N | Total Harmonic Distortion + Noise | $V_{PP}$ = 5 V, $V_{BIAS}$ = 0 V<br>$R_L$ = 10 MΩ, $C_L$ = 5 pF,<br>f = 20 Hz to 20 kHz<br>Refer to THD + Noise | 25°C | | 0.0006 | | % |
| $C_{S(OFF)}$ | Source off capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 40 | | pF |
| $C_{D(OFF)}$ | Drain off capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 60 | | pF |


Copyright © 2021 Texas Instruments Incorporated

$V_{DD}$ = +5 V ± 10%, $V_{SS}$ = – 5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at $V_{DD}$ = +5 V, $V_{SS}$ = – 5 V, $T_A$ = 25℃ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $T_A$ | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{S(ON)}$, $C_{D(ON)}$ | On capacitance | $V_S$ = 0 V, f = 1 MHz | 25°C | | 150 | | pF |

Copyright © 2021 Texas Instruments Incorporated

## 6.14 Typical Characteristics

at $T_A$ = 25°C

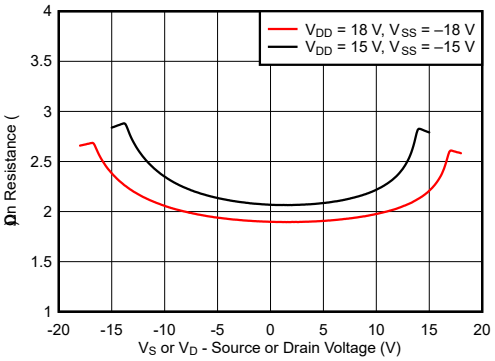



图 6-1. On-Resistance vs Source or Drain Voltage – Dual Supply

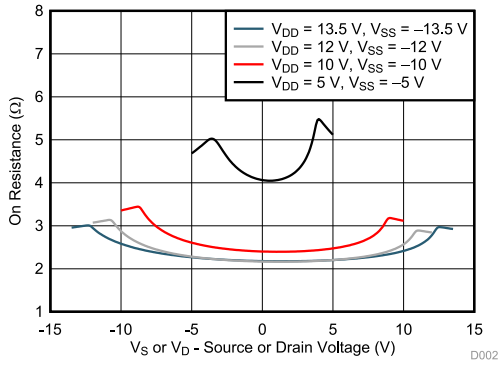



图 6-2. On-Resistance vs Source or Drain Voltage – Dual Supply

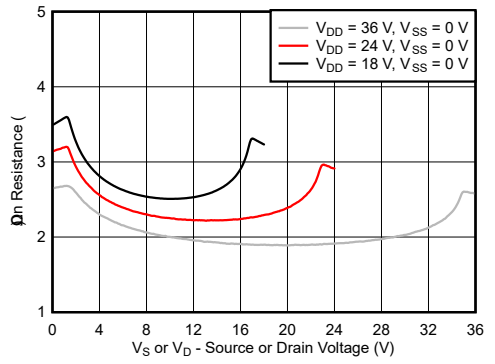



图 6-3. On-Resistance vs Source or Drain Voltage – Single Supply

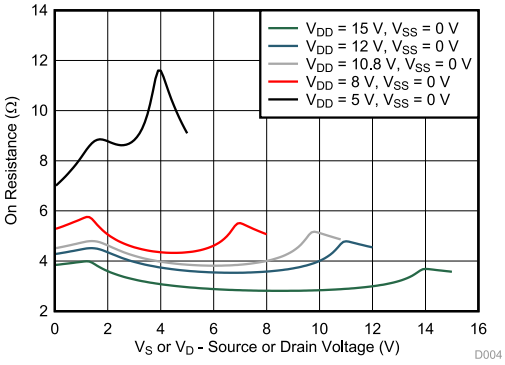
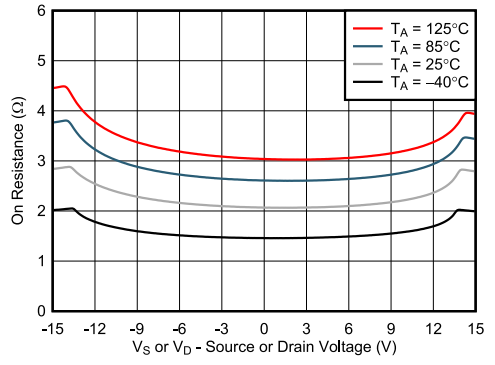
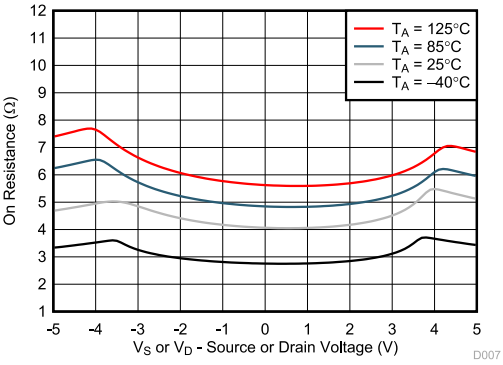



图 6-4. On-Resistance vs Source or Drain Voltage – Single Supply




$V_{DD}$ = 15 V, $V_{SS}$ = -15 V

图 6-5. On-Resistance vs Temperature



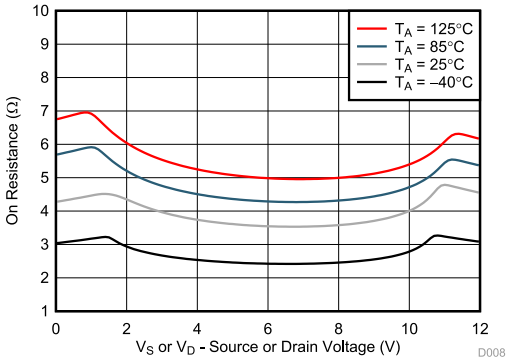

$V_{DD}$ = 5 V, $V_{SS}$ = -5 V

图 6-6. On-Resistance vs Temperature


Copyright © 2021 Texas Instruments Incorporated

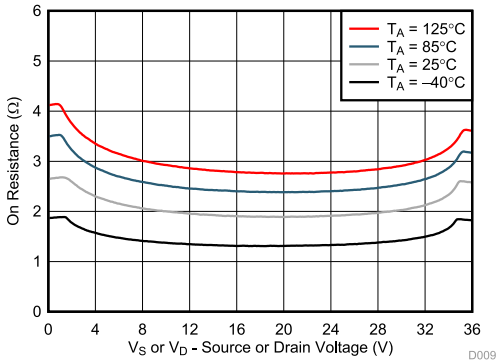
## 6.14 Typical Characteristics (continued)

at $T_A$ = 25°C



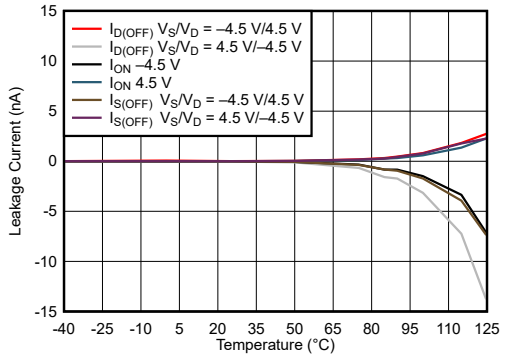

$V_{DD}$ = 12 V, $V_{SS}$ = 0 V

**图 6-7. On-Resistance vs Temperature**



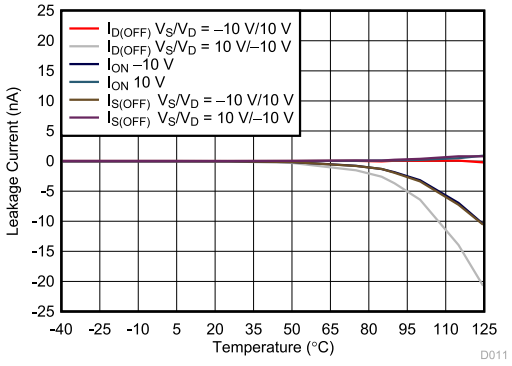

$V_{DD}$ = 36 V, $V_{SS}$ = 0 V

**图 6-8. On-Resistance vs Temperature**



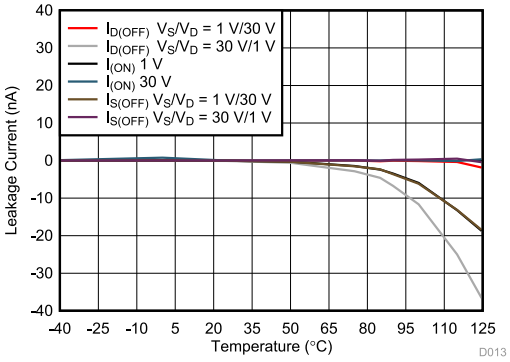

$V_{DD}$ = 5 V, $V_{SS}$ = -5 V

**图 6-9. Leakage Current vs Temperature**



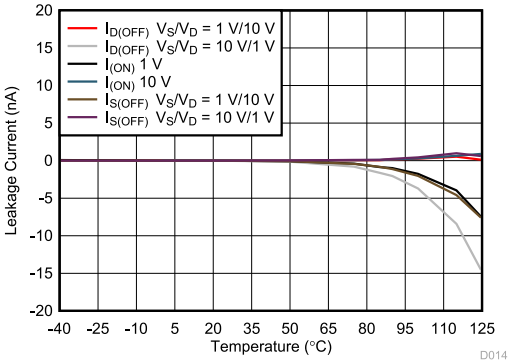

$V_{DD}$ = 15 V, $V_{SS}$ = -15 V

**图 6-10. Leakage Current vs Temperature**




$V_{DD}$ = 36 V, $V_{SS}$ = 0 V

**图 6-11. Leakage Current vs Temperature**




$V_{DD}$ = 12 V, $V_{SS}$ = 0 V

**图 6-12. Leakage Current vs Temperature**

Copyright © 2021 Texas Instruments Incorporated

## 6.14 Typical Characteristics (continued)

at $T_A$ = 25°C

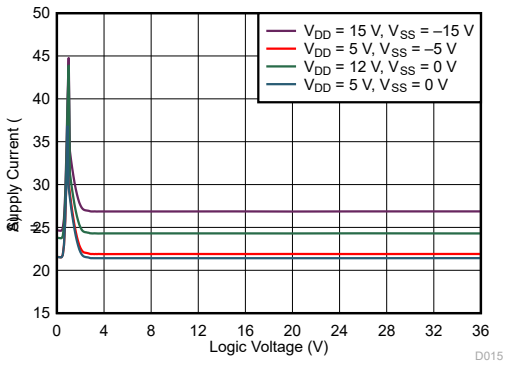



图 6-13. Supply Current vs Logic Voltage

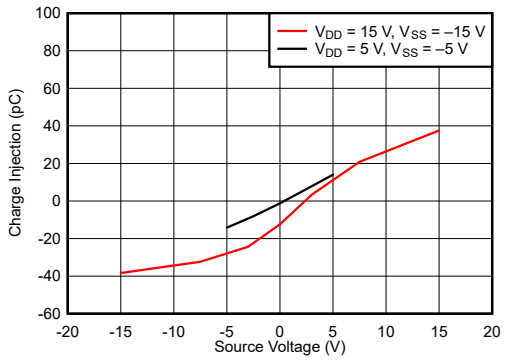



图 6-14. Charge Injection vs Source Voltage – Dual Supplies

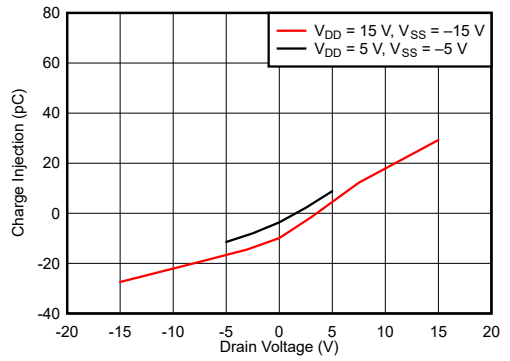



图 6-15. Charge Injection vs Drain Voltage – Dual Supplies

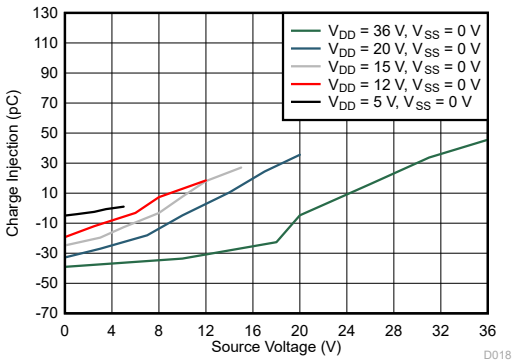



图 6-16. Charge Injection vs Source Voltage – Single Supplies

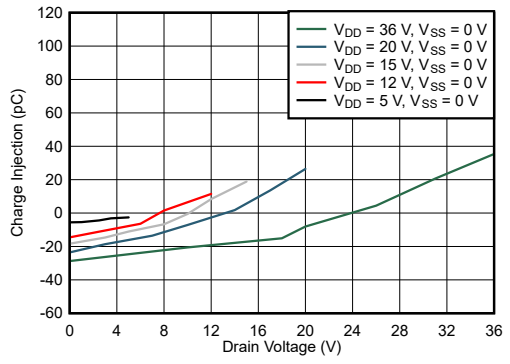
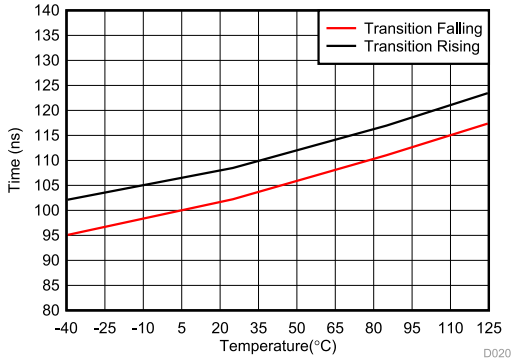



图 6-17. Charge Injection vs Drian Voltage – Single Supplies



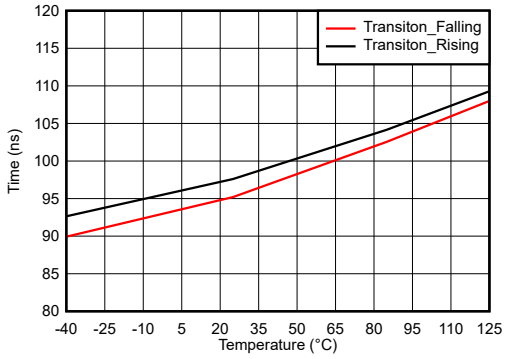

$V_{DD}$ = 15 V, $V_{SS}$ = -15 V

图 6-18. $T_{TRANSITION}$ vs Temperature


Copyright © 2021 Texas Instruments Incorporated

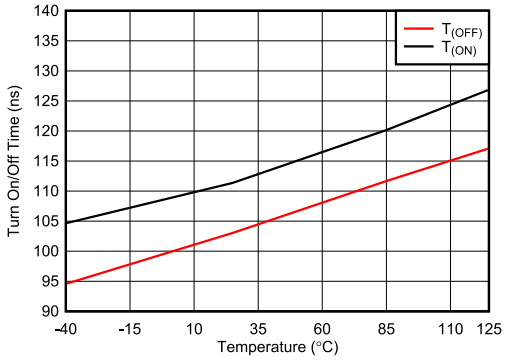
## 6.14 Typical Characteristics (continued)

at $T_A$ = 25°C



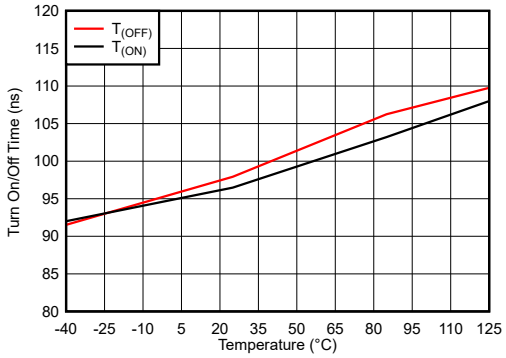

$V_{DD}$ = 36 V, $V_{SS}$ = 0 V

**图 6-19. $T_{TRANSITION}$ vs Temperature**




$V_{DD}$ = 15 V, $V_{SS}$ = -15 V

**图 6-20. $T_{ON}$ and $T_{OFF}$ vs Temperature**




$V_{DD}$ = 36 V, $V_{SS}$ = 0 V

**图 6-21. $T_{ON}$ and $T_{OFF}$ vs Temperature**

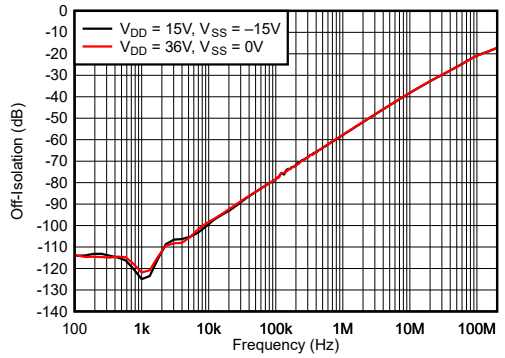
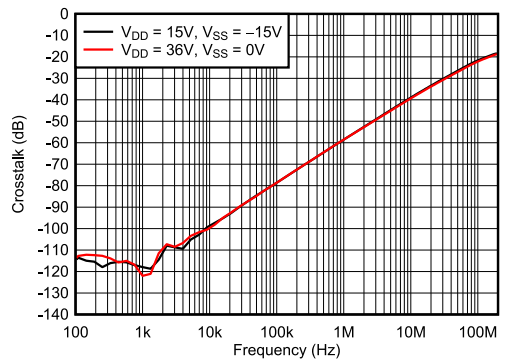
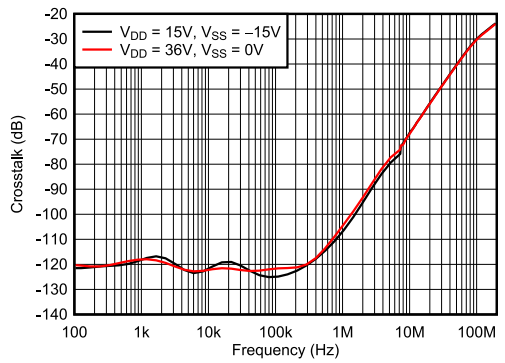



**图 6-22. Off-Isolation vs Frequency**




Switch *ON* (EN = 1)

**图 6-23. Crosstalk vs Frequency**




Switch *OFF* (EN = 0)

**图 6-24. Crosstalk vs Frequency**

Copyright © 2021 Texas Instruments Incorporated

## 6.14 Typical Characteristics (continued)

at $T_A$ = 25°C

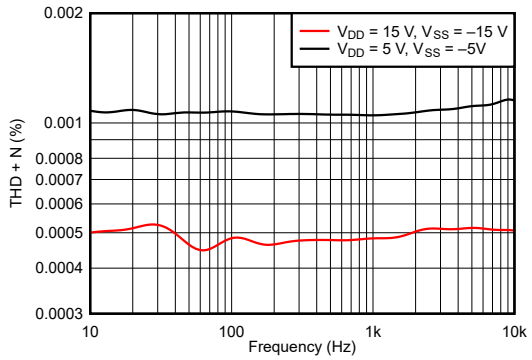



**图 6-25. THD+N vs Frequency (Dual Supplies)**

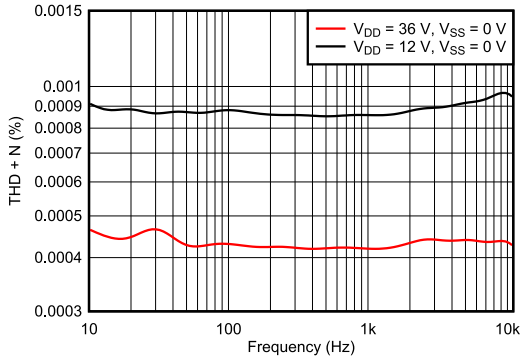
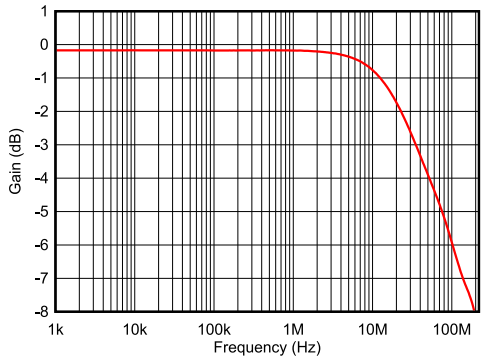
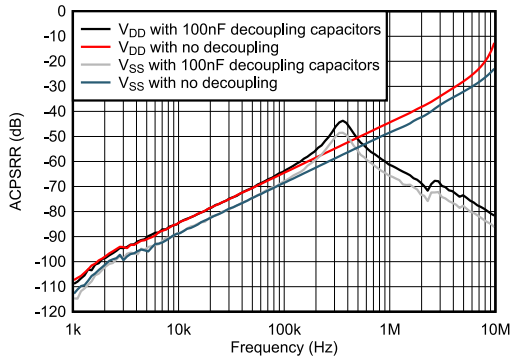



**图 6-26. THD+N vs Frequency (Single Supplies)**



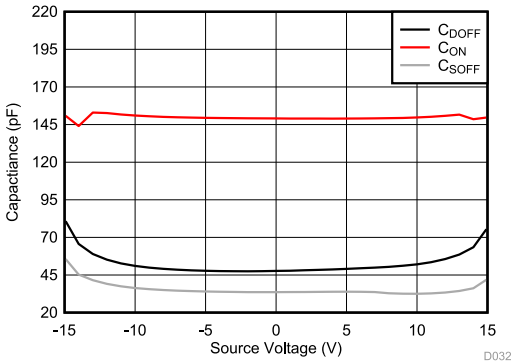

$V_{DD}$ = 15 V, $V_{SS}$ = -15 V

**图 6-27. On Response vs Frequency**



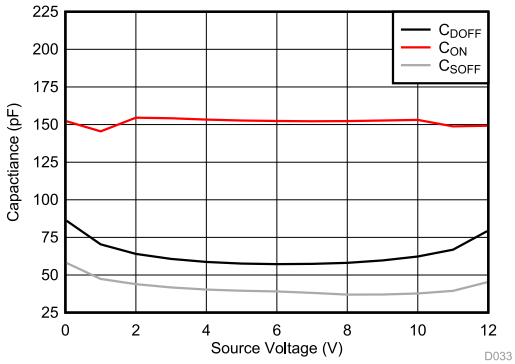

$V_{DD}$ = +15 V, $V_{SS}$ = -15 V

**图 6-28. ACPSRR vs Frequency**




$V_{DD}$ = +15 V, $V_{SS}$ = -15 V

**图 6-29. Capacitance vs Source Voltage or Drain Voltage**




$V_{DD}$ = 12 V, $V_{SS}$ = 0 V

**图 6-30. Capacitance vs Source Voltage or Drain Voltage**


Copyright © 2021 Texas Instruments Incorporated

# 7 Parameter Measurement Information

## 7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol $R_{ON}$ is used to denote on-resistance. 图 7-1 shows the measurement setup used to measure $R_{ON}$. Voltage (V) and current ($I_{SD}$) are measured using the following setup, where $R_{ON}$ is computed as $R_{ON} = V / I_{SD}$:

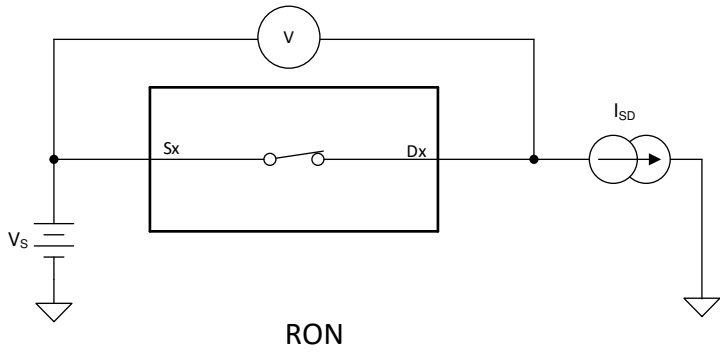



图 7-1. On-Resistance

## 7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current.
2. Drain off-leakage current.

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

图 7-2 shows the setup used to measure both off-leakage currents.

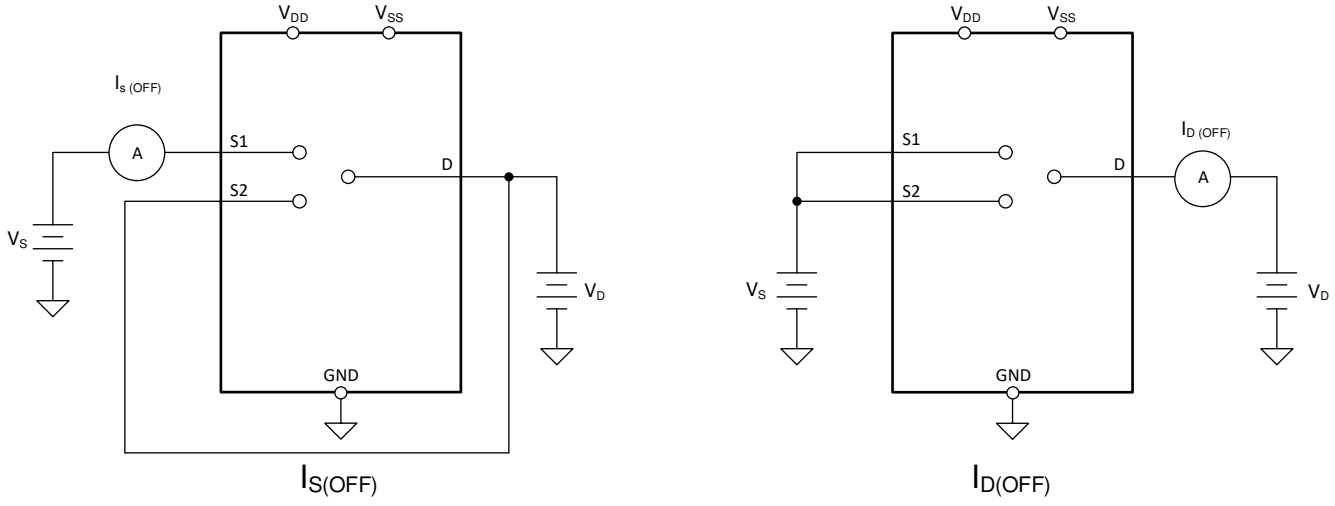



图 7-2. Off-Leakage Measurement Setup

## 7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

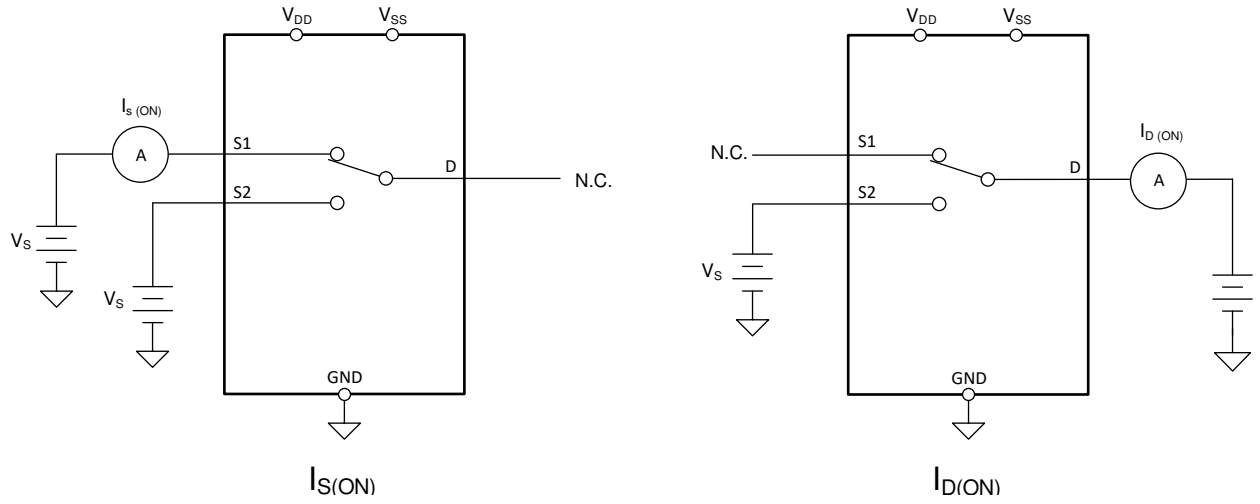



图 7-3. On-Leakage Measurement Setup

## 7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

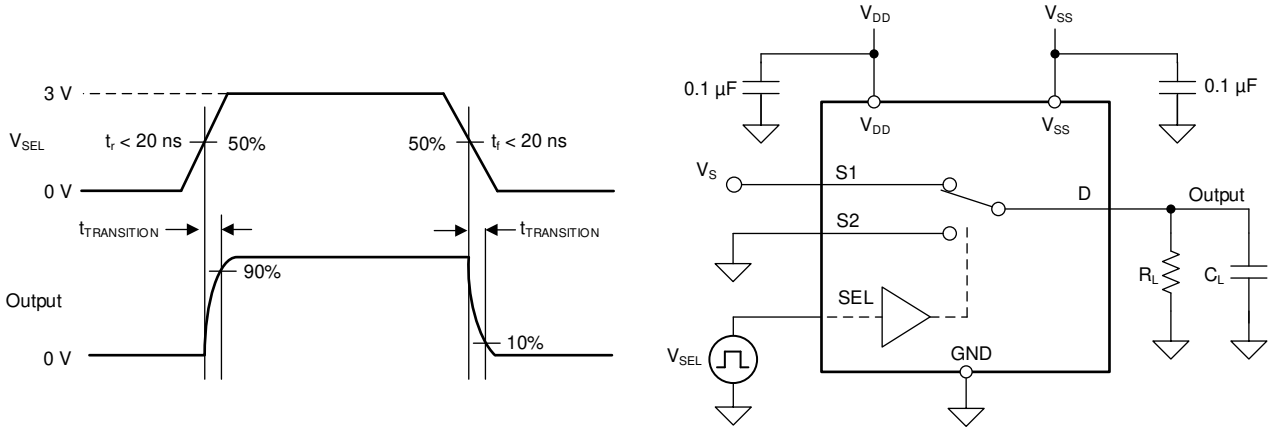



图 7-4. Transition-Time Measurement Setup


Copyright © 2021 Texas Instruments Incorporated

## 7.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-5 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-5 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

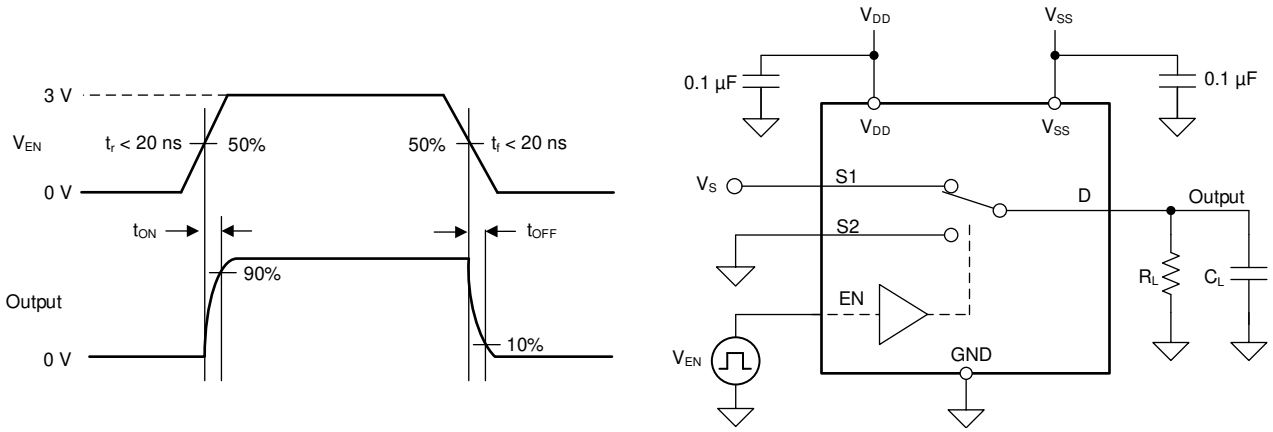



**图 7-5. Turn-On and Turn-Off Time Measurement Setup**

## 7.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 7-6 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

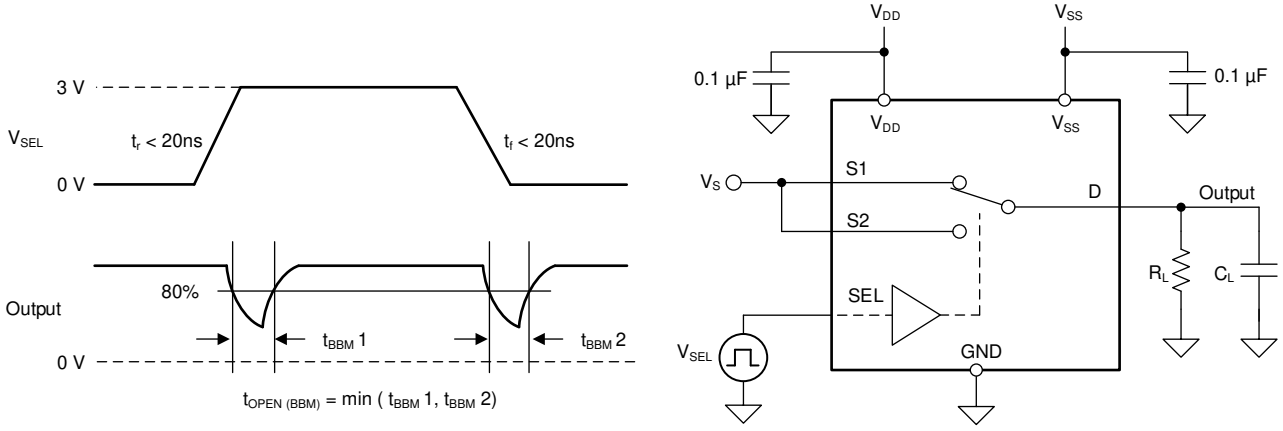



**图 7-6. Break-Before-Make Delay Measurement Setup**

## 7.7 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. 图 7-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

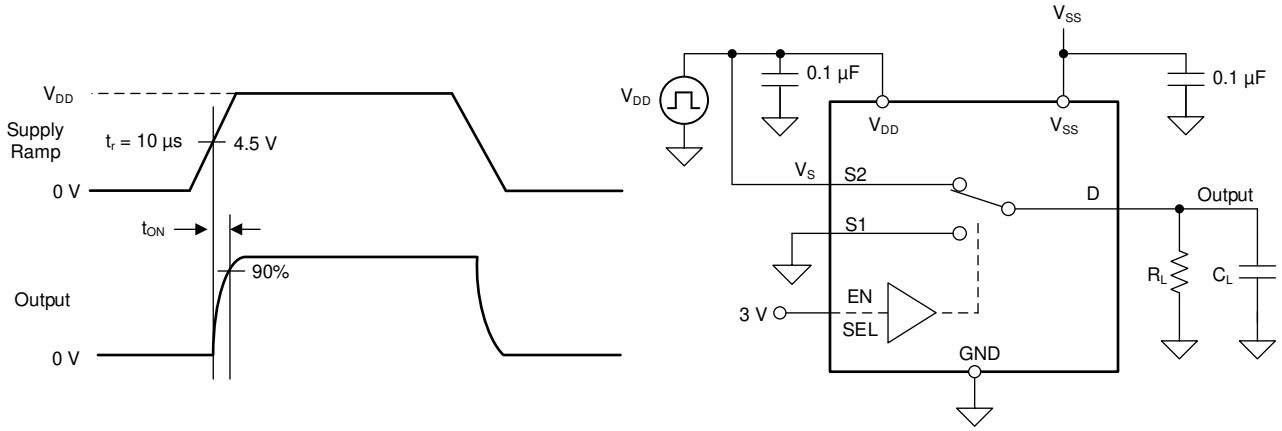



图 7-7. $t_{ON\ (VDD)}$ Time Measurement Setup

## 7.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. 图 7-8 shows the setup used to measure propagation delay, denoted by the symbol $t_{PD}$.

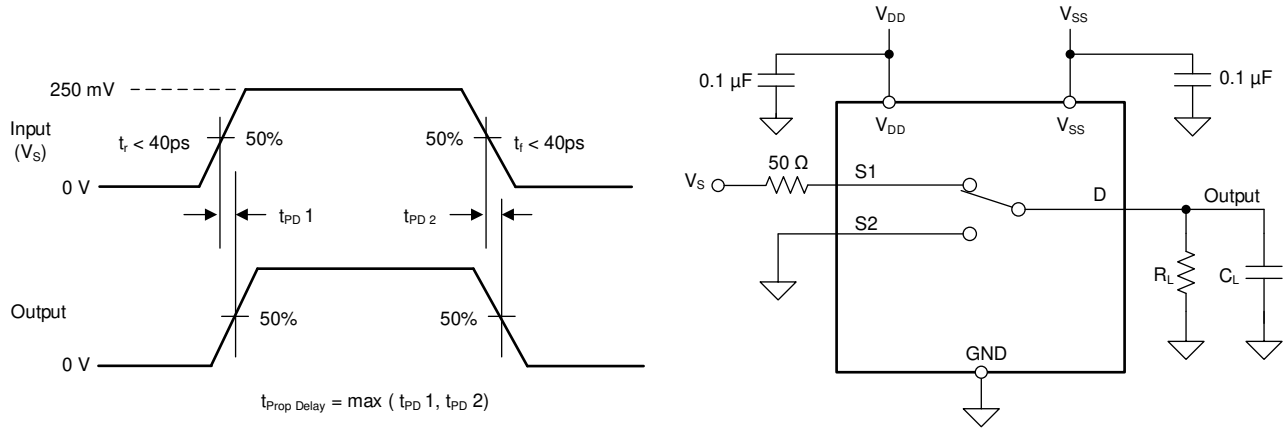



图 7-8. Propagation Delay Measurement Setup


Copyright © 2021 Texas Instruments Incorporated

## 7.9 Charge Injection

The TMUX6219-Q1 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol $Q_C$. 图 7-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

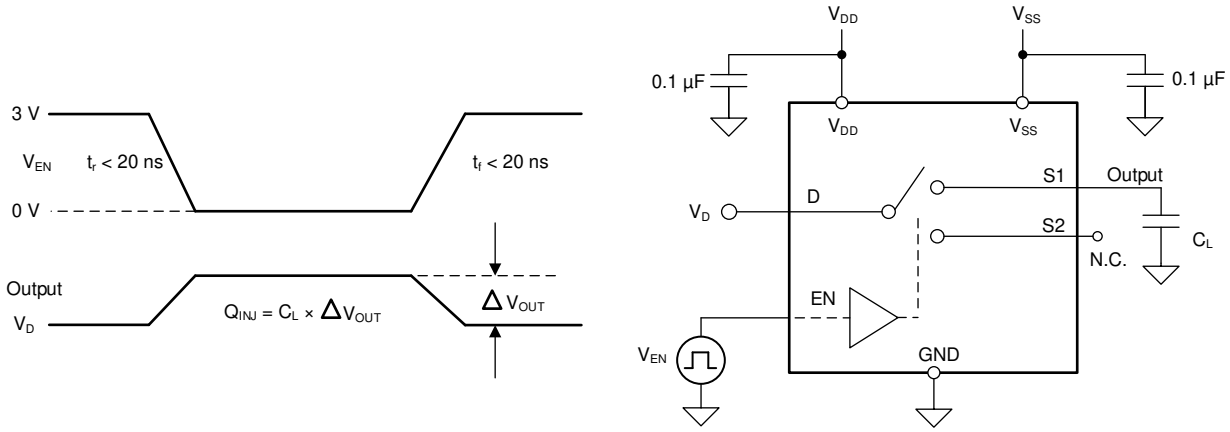
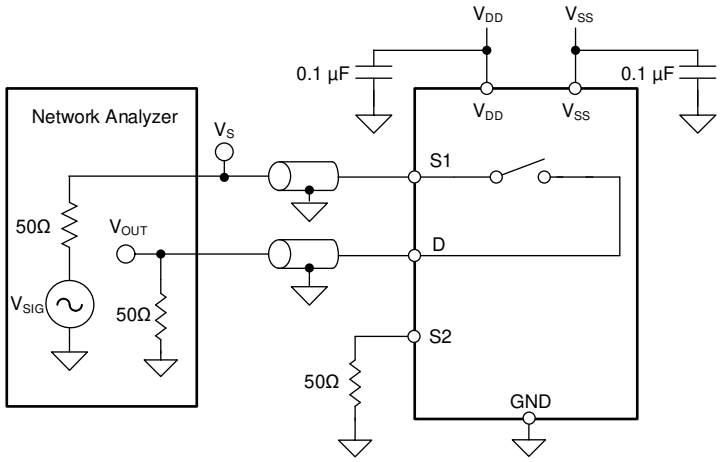



**图 7-9. Charge-Injection Measurement Setup**

## 7.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 7-10 shows the setup used to measure, and the equation used to calculate off isolation.



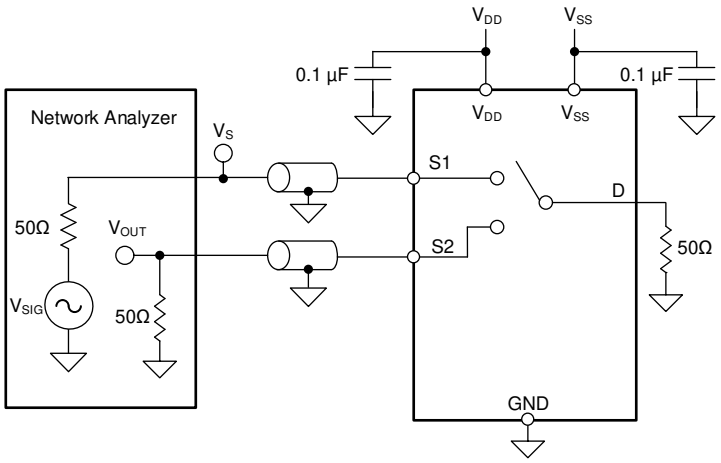

$$Off\ Isolation = 20 \times Log \frac{V_{OUT}}{V_S}$$

**图 7-10. Off Isolation Measurement Setup**

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

## 7.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 7-11 shows the setup used to measure, and the equation used to calculate crosstalk.

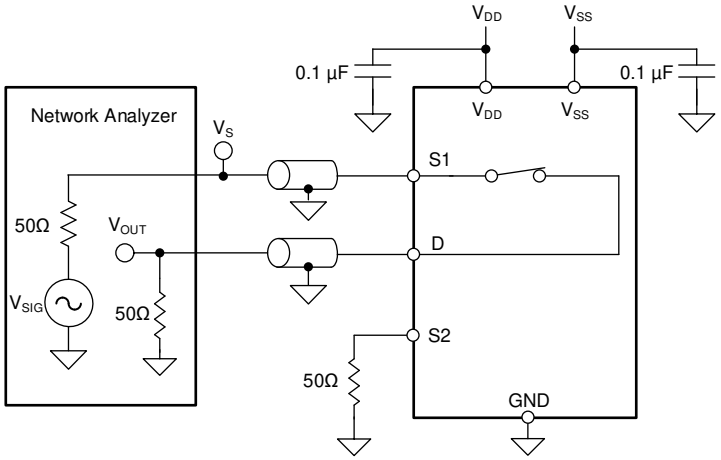



$$Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

**图 7-11. Crosstalk Measurement Setup**

## 7.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 7-12 shows the setup used to measure bandwidth.




$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

**图 7-12. Bandwidth Measurement Setup**


Copyright © 2021 Texas Instruments Incorporated

## 7.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output.

The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD + N.

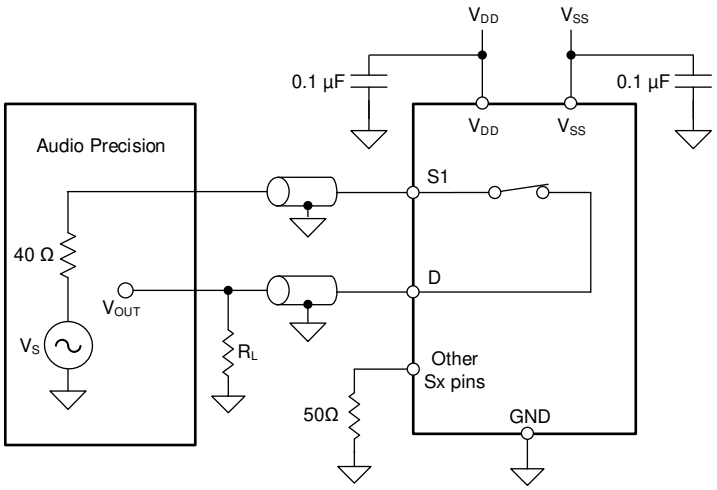
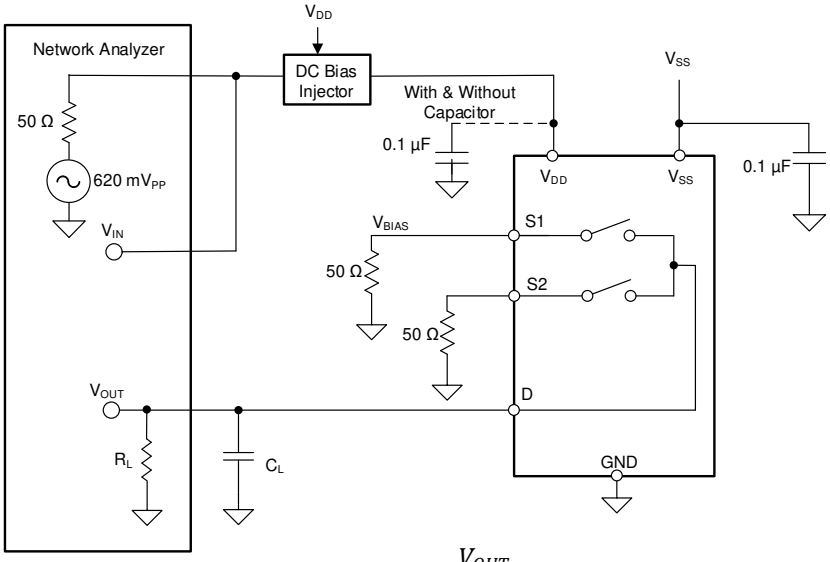



**图 7-13. THD + N Measurement Setup**

## 7.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620 $mV_{PP}$. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

This helps stabilize the supply and immediately filter as much of the supply noise as possible.




$$PSRR = 20 \times Log \frac{V_{OUT}}{V_{IN}}$$

**图 7-14. ACPSRR Measurement Setup**

# 8 Detailed Description

## 8.1 Overview

The TMUX6219-Q1 is a 2:1, 1-channel switch. Each input is turned on or turned off based on the state of the select line and enable pin.

## 8.2 Functional Block Diagram

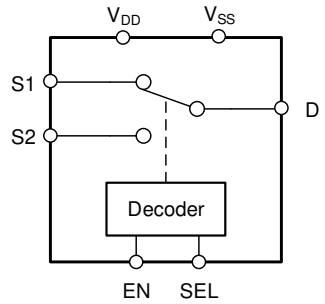



**图 8-1. TMUX6219-Q1 Functional Block Diagram**

## 8.3 Feature Description

### 8.3.1 Bidirectional Operation

The TMUX6219-Q1 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

### 8.3.2 Rail to Rail Operation

The valid signal path input or output voltage for TMUX6219-Q1 ranges from $V_{SS}$ to $V_{DD}$.

### 8.3.3 1.8 V Logic Compatible Inputs

The TMUX6219-Q1 has 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the TMUX6219-Q1 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*.

### 8.3.4 Fail-Safe Logic

The TMUX6219-Q1 supports Fail-Safe Logic on the control input pins (EN, SEL) allowing for operation up to 36 V above ground, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the logic input pins of the TMUX6219-Q1 to be ramped to +36 V while $V_{DD}$ and $V_{SS}$ = 0 V. The logic control inputs are protected against positive faults of up to +36 V in powered-off condition, but do not offer protection against negative overvoltage conditions.


Copyright © 2021 Texas Instruments Incorporated

### 8.3.5 Latch-Up Immune

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX62xx family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX62xx family of switches and multiplexers to be used in harsh environments.

### 8.3.6 Ultra-Low Charge Injection

The TMUX6219-Q1 has a transmission gate topology, as shown in 图 8-2. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

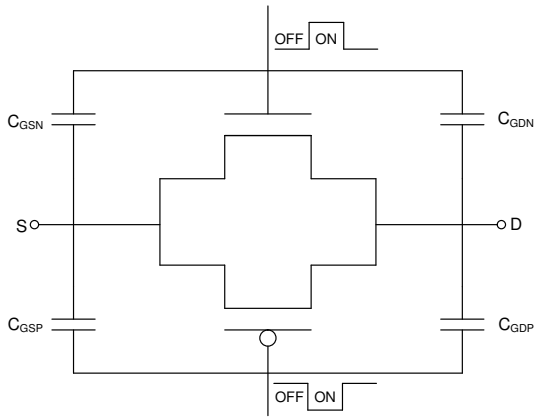



**图 8-2. Transmission Gate Topology**

The TMUX6219-Q1 contains specialized architecture to reduce charge injection on the source (Sx). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the drain (D). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the drain (D) instead of the source (Sx). As a general rule of thumb, Cp should be 20× larger than the equivalent load capacitance on the source (Sx). 图 8-3 shows charge injection variation with source voltage with different compensation capacitors on the Drain side.

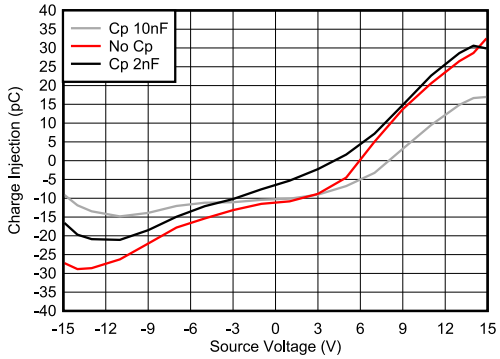



**图 8-3. Charge Injection Compensation**

Copyright © 2021 Texas Instruments Incorporated

## 8.4 Device Functional Modes

When the EN pin of the TMUX6219-Q1 is pulled high, one of the switches is closed based on the state of the SEL pin. When the EN pin is pulled low, both of the switches are in an open state regardless of the state of the SEL pin. The control pins can be as high as 36 V.

The TMUX6219-Q1 can be operated without any external components except for the supply decoupling capacitors. The EN pin has an internal pull-up resistor of 4 MΩ and SEL pin has internal pull-down resistor of 4 MΩ. If unused, EN pin must be tied to $V_{DD}$ and SEL pin must be tied to GND in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (S1, S2, or D) should be connected to GND.

## 8.5 Truth Tables

表 8-1 show the truth tables for the TMUX6219-Q1.

**表 8-1. TMUX6219-Q1 Truth Table**

| EN | SEL | Selected Source Connected To Drain (D) Pin |
|---|---|---|
| 0 | X(1) | All sources are off (HI-Z) |
| 1 | 0 | S1 |
| 1 | 1 | S2 |

(1) X denotes *don't care*.


Copyright © 2021 Texas Instruments Incorporated

# 9 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Application Information

TMUX6219-Q1 is part of the precision switches and multiplexers family of devices. TMUX6219-Q1 offers low RON, low on and off leakage currents and ultra-low charge injection performance. These properties make TMUX6219-Q1 ideal for implementing high precision industrial systems requiring selection of one of two inputs or outputs.

## 9.2 Typical Application

### 9.2.1 PWM Signal Generation (EV Charging Station)

One application of the TMUX6219-Q1 is in Electric Vehicle Service Equipment (EVSE). The EVSE is a system that monitors and controls the high voltage power path from the grid to the vehicle. One key feature of an EVSE is the pilot signal wire communication support that requires a 1-kHz, ±12-V PWM signal to be transmitted down the length of the charger cable to the vehicle.

The TMUX6219-Q1 can be used to generate 1kHz ±12V PWM signal for EVSE control pilot. A 1 kHz square wave at ±12 V generated by the EVSE on the control pilot line is used to detect the presence of the vehicle, communicate the maximum allowable charging current, and control charging.

图 9-1 shows the TMUX6219-Q1 configured for PWM signal generation for EVSE control pilot.

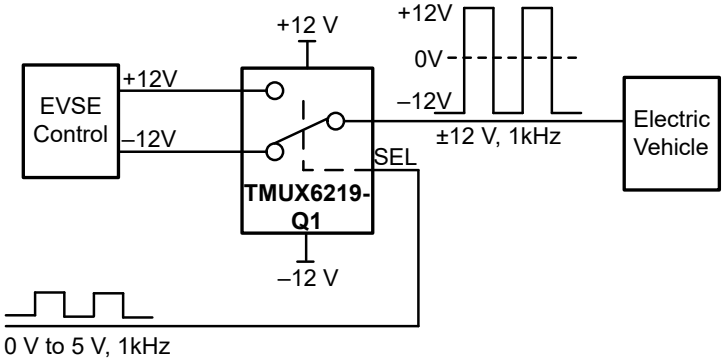



**图 9-1. PWM Signal Generation (EV Charging Station)**

### 9.2.2 Design Requirements

For the design example, use the parameters listed in 表 9-1 .

**表 9-1. Design Parameters**

| PARAMETERS | VALUES |
|---|---|
| Supply ($V_{DD}$) | 12 V |
| Supply ($V_{SS}$) | -12 V |
| MUX I/O signal range | -12 V to 12 V (Rail-to-Rail) |
| Control logic thresholds | 1.8 V compatiable (up to $V_{DD}$) |
| EN | EN pulled high to enable the switch |

Copyright © 2021 Texas Instruments Incorporated

### 9.2.3 Detailed Design Procedure

The application shown in 图 9-1 demonstrates how to generate a ±12V PWM signal that is created by toggling the TMUX6219-Q1. This PWM signal generated by the EVSE on the control pilot line signals to the car the available current of the charger, and the car will respond with a charging status. This handshake results in a safe method for supplying power to vehicle. The TMUX6219-Q1 can support 1.8 V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX6219-Q1 can be operated without any external components except for the supply decoupling capacitors. The select pin has an internal pull-down resistor to prevent floating input logic. All inputs to the switch must fall within the recommend operating conditions of the TMUX6219-Q1 including signal range and continuous current. For this design with a positive supply of 12 V on $V_{DD}$, and negative supply of -12 V on $V_{SS}$, the signal range can be 12 V to -12 V. The max continuous current ($I_{DC}$) can be up to 330 mA as shown in the *Recommended Operating Conditions table* for wide-range current measurement.

## 10 Power Supply Recommendations

The TMUX6219-Q1 operates across a wide supply range of of ±4.5 V to ±18 V (4.5 V to 36 V in single-supply mode). It also performs well with asymmetrical supplies such as $V_{DD}$ = 8 V and $V_{SS}$ = – 12 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF at both the $V_{DD}$ and $V_{SS}$ pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to power and ground planes. Always ensure the ground (GND) connection is established before supplies are ramped.


Copyright © 2021 Texas Instruments Incorporated

# 11 Layout

## 11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self – inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

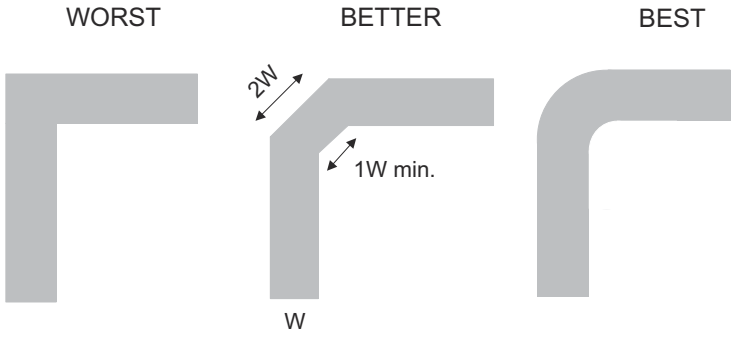



**图 11-1. Trace Example**

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 11-2 illustrates an example of a PCB layout with the TMUX6219-Q1. Some key considerations are:

- Decouple the supply pins with a 0.1-µF and 1 µF capacitor, placed lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

## 11.2 Layout Example

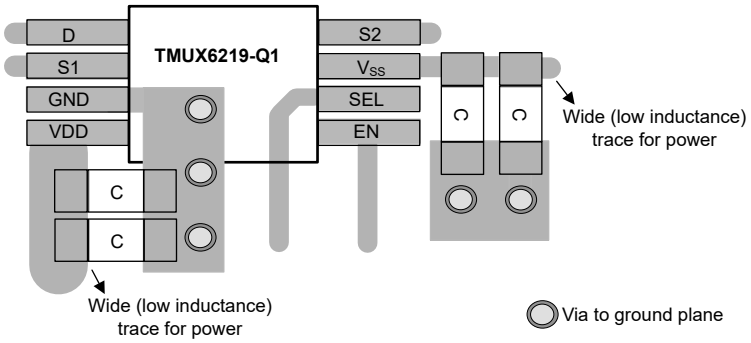



**图 11-2. TMUX6219-Q1 Layout Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Multiplexers and Signal Switches Glossary* application report
- Texas Instruments, *QFN/SON PCB Attachment* application report
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application report
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application report
- Texas Instruments, *TMUX6219-Q1 Functional Safety, FIT Rate, Failure Mode Distribution and Pin FMA* functional safety FIT rate, FMD and Pin-FMA

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


Copyright © 2021 Texas Instruments Incorporated

# 重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

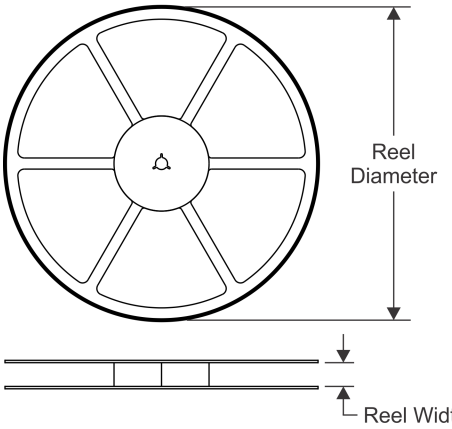
这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com/legal/termsofsale.html) 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

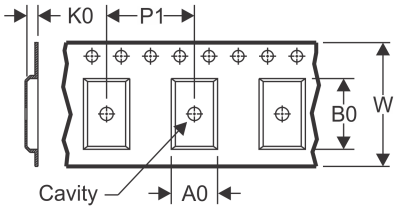
邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2021，德州仪器 (TI) 公司

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

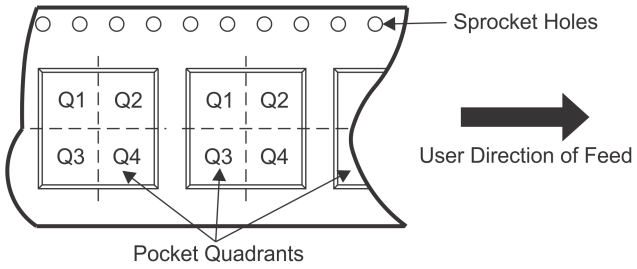



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

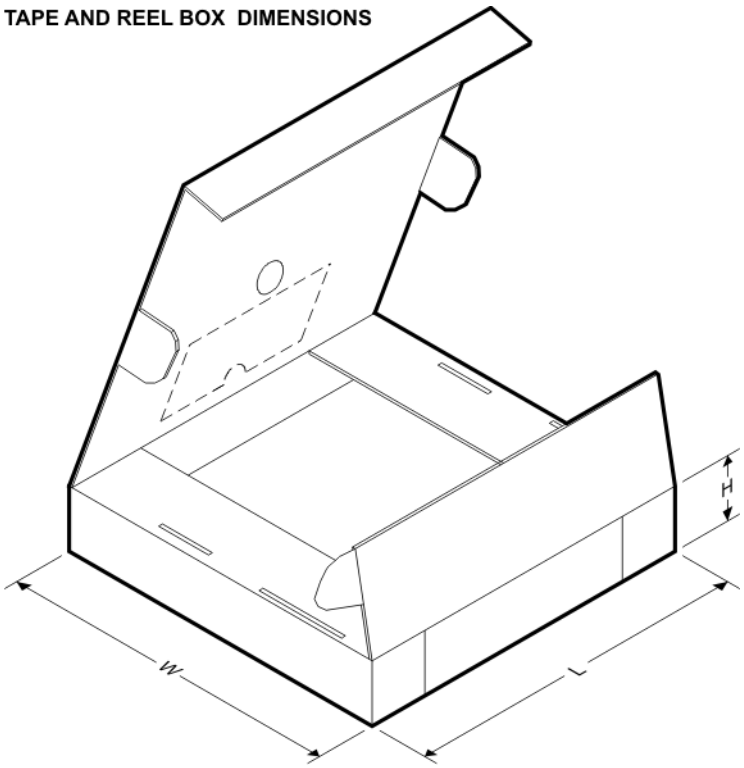
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX6219DGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |

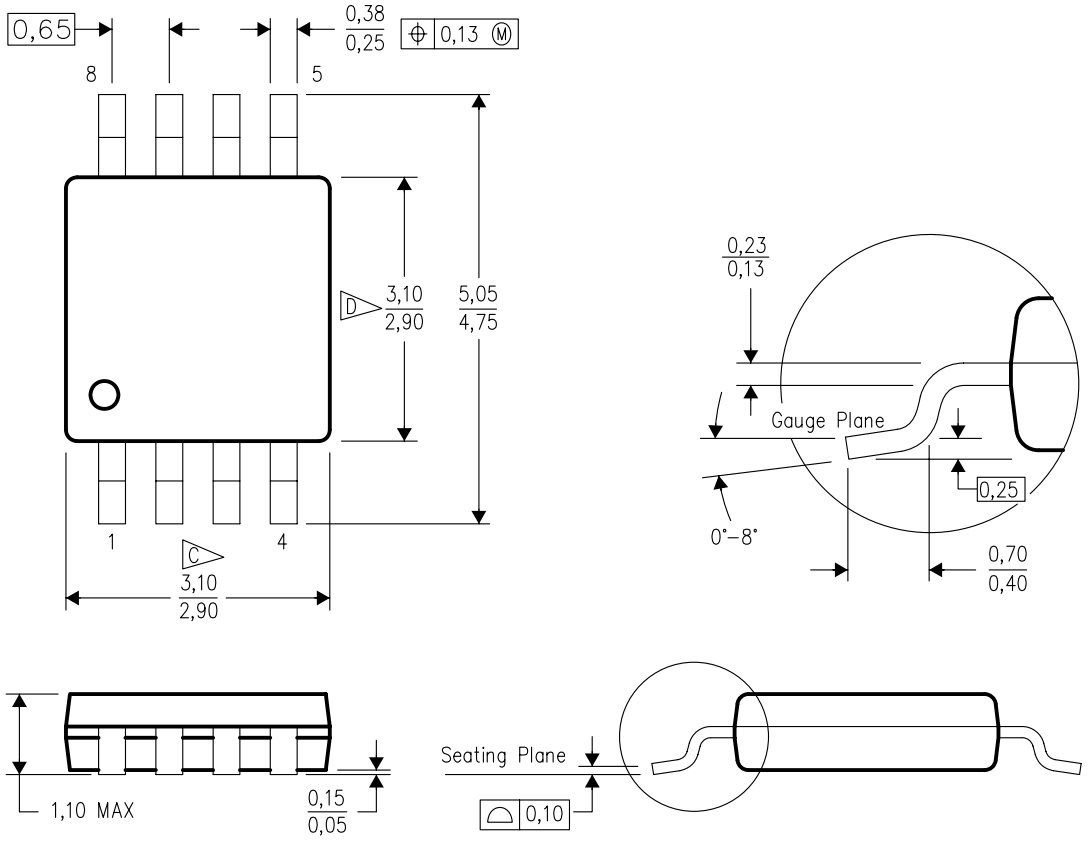
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMUX6219DGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |

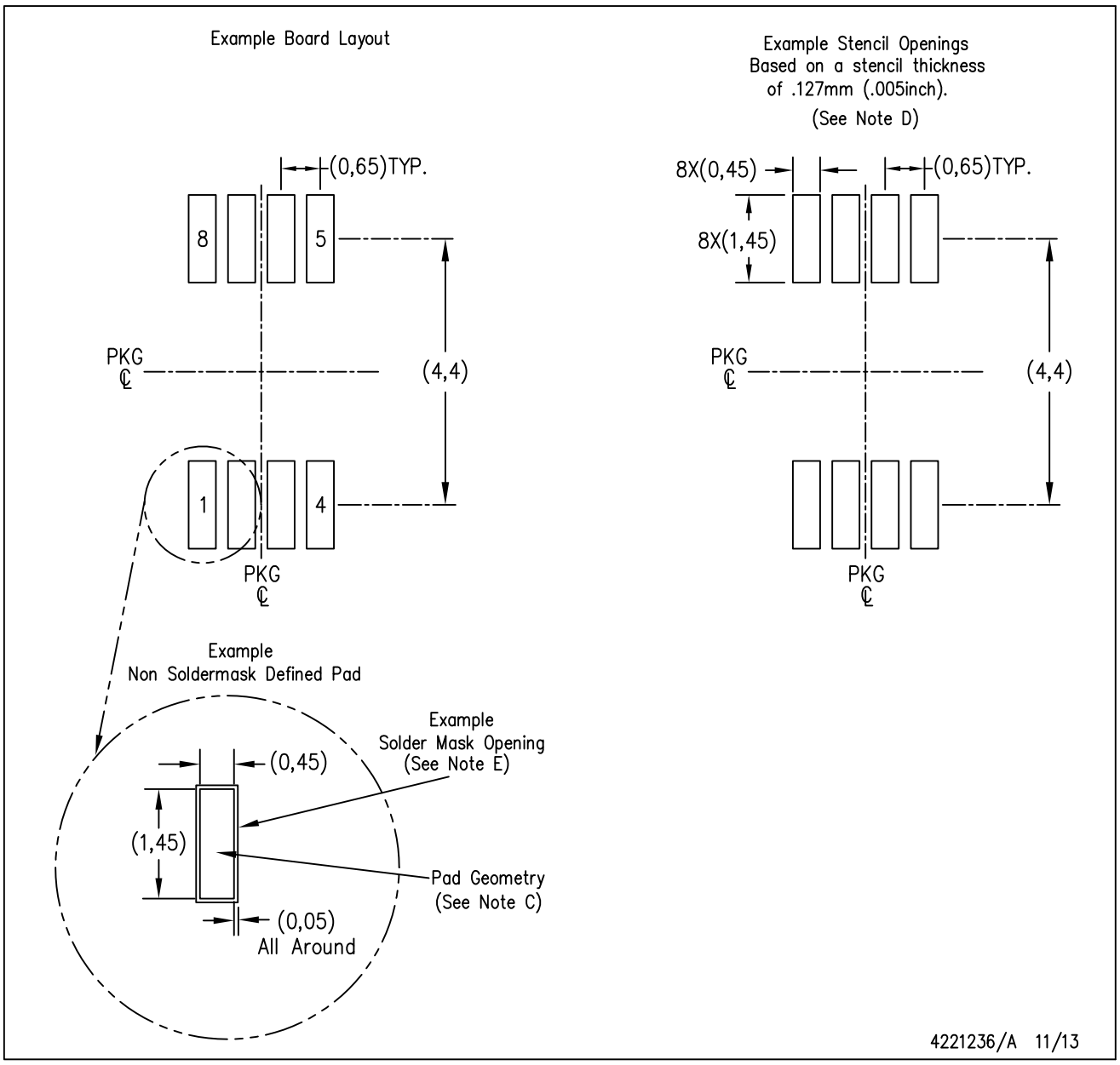
## DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE




4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

# DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# 重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com.cn/zh-cn/legal/termsofsale.html) 或 ti.com.cn 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122
Copyright © 2021 德州仪器半导体技术（上海）有限公司