具有 1.8V 逻辑电平的 TMUX620x 36V、低 Ron、8:1 单通道和 4:1 双通道精密多路复用器

1 特性

- 单电源电压范围：4.5V 至 36V
- 双电源电压范围：±4.5V 至 ±18V
- 低导通电阻：4Ω
- 低电荷注入：3pC
- 高电流支持：400mA（最大值）(WQFN)
- 高电流支持：300mA（最大值）(TSSOP)
- –40°C 至 +125°C 工作温度
- 1.8V 逻辑兼容输入
- 逻辑引脚上的集成下拉电阻器
- 失效防护逻辑
- 轨到轨运行
- 双向信号路径
- 先断后合开关

2 应用

- 工厂自动化和控制
- 可编程逻辑控制器 (PLC)
- 模拟输入模块
- 半导体测试设备
- 电池测试设备
- 超声波扫描仪
- 患者监护和诊断
- 光纤网络
- 光学测试设备
- 有线网络
- 数据采集系统 (DAQ)

3 说明

TMUX6208 是一款 8:1 单通道精密多路复用器；TMUX6209 是一款 4:1 双通道多路复用器，具有低导通电阻和电荷注入。该器件支持单电源（4.5V 至 36V）、双电源（±4.5V 至 18V）或非对称电源（例如，VDD = 12V，VSS = –5V）。TMUX620x 可在源极 (Sx) 和漏极 (D) 引脚上支持从 V_{SS} 到 V_{DD} 范围的双向模拟和数字信号。

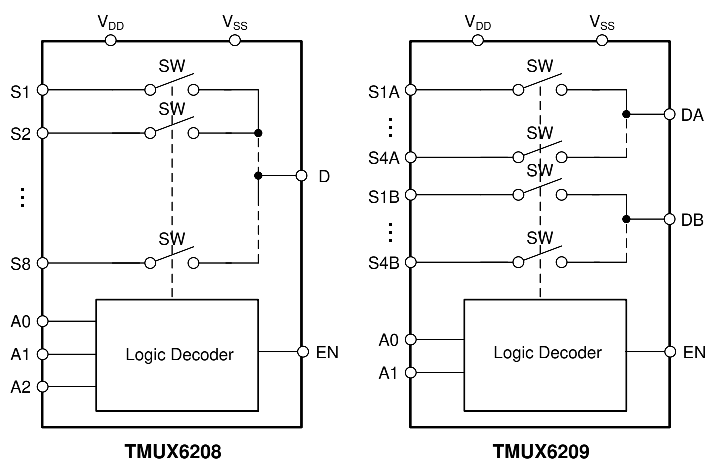
所有逻辑控制输入均支持 1.8V 至 V_{DD} 的逻辑高电平，因此，当器件在有效电源电压范围内运行时，可确保 TTL 和 CMOS 逻辑兼容性。 Fail-Safe Logic 电路允许在电源引脚之前的控制引脚上施加电压，从而保护器件免受潜在的损害。

TMUX620x 是精密开关和多路复用器系列器件。这些器件具有非常低的导通和关断漏电流以及低电荷注入，因此可用于高精度测量应用。

表 3-1. 器件信息

器件型号	配置	封装 (1)
TMUX6208	单通道 8:1 多路复用器	TSSOP (16) (PW) WQFN (16) (RUM)
TMUX6209	双通道 4:1 多路复用器	

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



TMUX6208 和 TMUX6209 方框图

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4 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX6208	Low-Leakage-Current, Precision, 8:1, 1-Ch. multiplexer
TMUX6209	Low-Leakage-Current, Precision, 4:1, 2-Ch. multiplexer

5 Pin Configuration and Functions

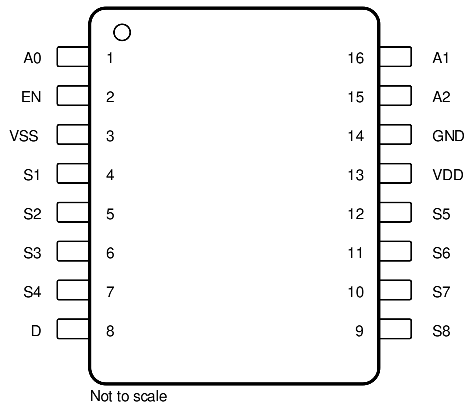


图 5-1. TMUX6208: PW Package 16-Pin TSSOP Top View

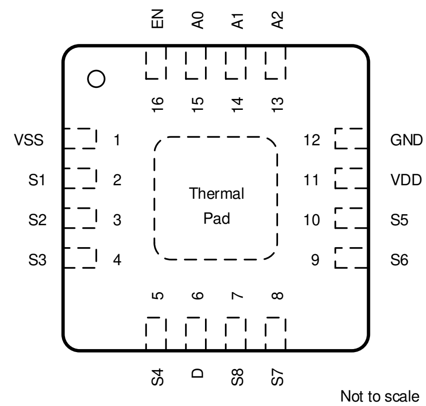


图 5-2. TMUX6208: RUM Package 16-Pin WQFN Top View

表 5-1. TMUX6208 Pin Functions

NAME	PW NO.	RUM NO.	TYPE(1)	DESCRIPTION(2)
A0	1	15	I	Logic control input, has internal 4 MΩ pull-down resistor. Controls the switch configuration as shown in 节 8.5.
A1	16	14	I	Logic control input, has internal 4 MΩ pull-down resistor. Controls the switch configuration as shown in 节 8.5.
A2	15	13	I	Logic control input, has internal 4 MΩ pull-down resistor. Controls the switch configuration as shown in 节 8.5.
D	8	6	I/O	Drain pin. Can be an input or output.
EN	2	16	I	Active high logic enable, has internal 4 MΩ pull-down resistor. When this pin is low, all switches are turned off. When this pin is high, the Ax logic input determines which switch is turned on.
GND	14	12	P	Ground (0 V) reference.
S1	4	2	I/O	Source pin 1. Can be an input or output.
S2	5	3	I/O	Source pin 2. Can be an input or output.
S3	6	4	I/O	Source pin 3. Can be an input or output.
S4	7	5	I/O	Source pin 4. Can be an input or output.
S5	12	10	I/O	Source pin 5. Can be an input or output.
S6	11	9	I/O	Source pin 6. Can be an input or output.
S7	10	8	I/O	Source pin 7. Can be an input or output.
S8	9	7	I/O	Source pin 8. Can be an input or output.
VDD	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
VSS	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
Thermal Pad			—	The thermal pad is not connected internally. It is recommended that the pad be tied to GND or VSS for best performance.

(1) I = input, O = output, I/O = input and output, P = power.

(2) Refer to 节 8.4 for what to do with unused pins.

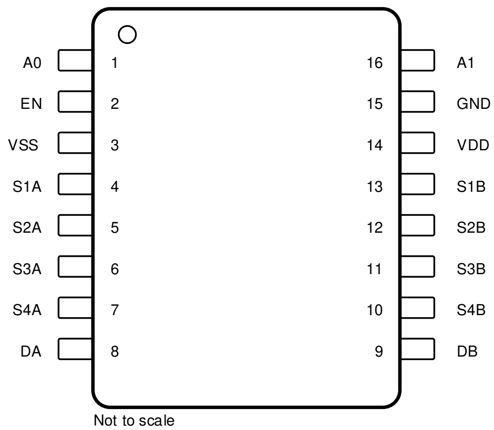


图 5-3. TMUX6209: PW Package 16-Pin TSSOP Top View

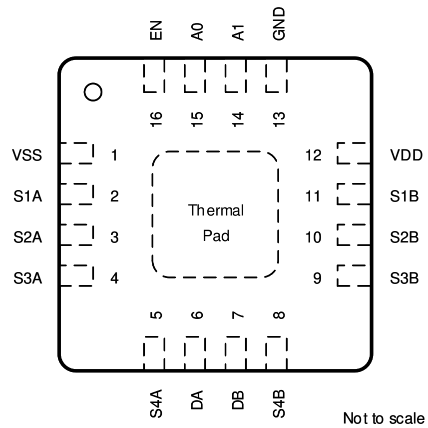


图 5-4. TMUX6209: RUM Package 16-Pin WQFN Top View

表 5-2. TMUX6209 Pin Functions

NAME	PW NO.	RUM NO.	TYPE(1)	DESCRIPTION(2)
A0	1	15	I	Logic control input, has internal pull-down resistor. Controls the switch configuration as shown in 节 8.5.
A1	16	14	I	Logic control input, has internal pull-down resistor. Controls the switch configuration as shown in 节 8.5.
DA	8	6	I/O	Drain Terminal A. Can be an input or an output.
DB	9	7	I/O	Drain Terminal B. Can be an input or an output.
EN	2	16	I	Active high logic enable, has internal pull-up resistor. When this pin is low, all switches are turned off. When this pin is high, the Ax logic input determines which switch is turned on.
GND	15	13	P	Ground (0 V) reference.
S1A	4	2	I/O	Source pin 1A. Can be an input or output.
S1B	13	11	I/O	Source pin 1B. Can be an input or output.
S2A	5	3	I/O	Source pin 2A. Can be an input or output.
S2B	12	10	I/O	Source pin 2B. Can be an input or output.
S3A	6	4	I/O	Source pin 3A. Can be an input or output.
S3B	11	9	I/O	Source pin 3B. Can be an input or output.
S4A	7	5	I/O	Source pin 4A. Can be an input or output.
S4B	10	8	I/O	Source pin 4B. Can be an input or output.
VDD	14	12	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
VSS	3	1	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
Thermal Pad			—	The thermal pad is not connected internally. It is recommended that the pad be tied to GND or VSS for best performance.

(1) I = input, O = output, I/O = input and output, P = power.
(2) Refer to 节 8.4 for what to do with unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
$V_{DD} - V_{SS}$	Supply voltage		38	V
V_{DD}		–0.5	38	V
V_{SS}		–38	0.5	V
$V_{ADDRESS}$ or V_{EN}	Logic control input pin voltage (EN, A0, A1, A2)	–0.5	38	V
$I_{ADDRESS}$ or I_{EN}	Logic control input pin current (EN, A0, A1, A2)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS} – 0.5	V_{DD}+0.5	V
I_{IK}	Diode clamp current[(3)]	–30	30	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)		I_{DC} + 10 %[(4)]	mA
T_A	Ambient temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C
P_{tot}	Total power dissipation (QFN package)[(5)]		1650	mW
	Total power dissipation (TSSOP package)[(5)]		700	mW

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
(4) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.
(5) For QFN package: P_{tot} derates linearily above T_A = 70°C by 24.4mW/°C.
For TSSOP package: P_{tot} derates linearily above T_A = 70°C by 10.8mW/°C.

6.2 ESD Ratings

			VALUE	UNIT
TMUX620x				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TMUX620x PW (TSSOP) 16 PINS	TMUX620x RUM (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.5	41.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.9	24.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.0	16.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.4	16.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	2.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} - V_{SS}$ [1]	Power supply voltage differential	4.5		36	V
V_{DD}	Positive power supply voltage	4.5		36	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	V_{SS}		V_{DD}	V
$V_{ADDRESS}$ or V_{EN}	Address or enable pin voltage	0		36	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)			I_{DC} [2]	mA
T_A	Ambient temperature	–40		125	°C

(1) V_{DD} and V_{SS} can be any value as long as 4.5 V ≤ (V_{DD} – V_{SS}) ≤ 36 V, and the minimum V_{DD} is met.
(2) Refer to *Source or Drain Continuous Current* table for I_{DC} specifications.

6.5 Source or Drain Continuous Current

at supply voltage of V_{DD} ± 10%, V_{SS} ± 10 % (unless otherwise noted)

CONTINUOUS CURRENT PER CHANNEL (I_{DC}) PACKAGE	TEST CONDITIONS	T_A = 25°C	T_A = 85°C	T_A = 125°C	UNIT
PW (TSSOP)	±15 V Dual Supply	300	190	110	mA
	+36 V Single Supply[1]	280	170	100	mA
	+12 V Single Supply	220	150	90	mA
	±5 V Dual Supply	210	140	90	mA
	+5 V Single Supply	170	110	70	mA
RUM (WQFN)	±15 V Dual Supply	400	230	120	mA
	+36 V Single Supply[1]	380	220	110	mA
	+12 V Single Supply	310	190	100	mA
	±5 V Dual Supply	300	190	100	mA
	+5 V Single Supply	230	150	90	mA

(1) Specified for nominal supply voltage only.

6.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		4	5.9	Ω
			–40°C to +85°C			7.4	Ω
			–40°C to +125°C			8.7	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = –10 V to +10 V I_S = –10 mA Refer to On-Resistance	25°C		0.4	1.5	Ω
			–40°C to +85°C			1.7	Ω
			–40°C to +125°C			1.8	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.02		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to 节 7.2	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–1		1	nA
			–40°C to +125°C	–5		5	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is off V_S = +10 V / –10 V V_D = –10 V / + 10 V Refer to 节 7.2	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–6		6	nA
			–40°C to +125°C	–42		42	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 16.5 V, V_{SS} = –16.5 V Switch state is on V_S = V_D = ±10 V Refer to 节 7.3	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–40		40	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	μA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		μA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		35	57	μA
			–40°C to +85°C			60	μA
			–40°C to +125°C			75	μA
I_{SS}	V_{SS} supply current	V_{DD} = 16.5 V, V_{SS} = –16.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		3	14	μA
			–40°C to +85°C			15	μA
			–40°C to +125°C			22	μA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.7 ±15 V Dual Supply: Switching Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		140	195	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			240	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to 节 7.5	25°C		140	195	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			240	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 10 V R_L = 300 Ω, C_L = 35 pF Refer to 节 7.5	25°C		200	268	ns
			–40°C to +85°C			285	ns
			–40°C to +125°C			298	ns
t_{BBM}	Break-before-make time delay	V_S = 10 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		60		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.17		ms
			–40°C to +125°C		0.17		ms
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF Refer to 节 7.8	25°C		1.8		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF Refer to 节 7.9	25°C		3		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth (TMUX6208)	R_L = 50 Ω, C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		30		MHz
BW	–3dB Bandwidth (TMUX6209)	R_L = 50 Ω, C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		52		MHz
I_L	Insertion loss	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.35		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω, C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–74		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 15 V, V_{BIAS} = 0 V R_L = 10 kΩ, C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		15		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6208)	V_S = 0 V, f = 1 MHz	25°C		135		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6209)	V_S = 0 V, f = 1 MHz	25°C		68		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6208)	V_S = 0 V, f = 1 MHz	25°C		185		pF

6.7 ±15 V Dual Supply: Switching Characteristics （续）

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ± 10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6209)	V_S = 0 V, f = 1 MHz	25°C		115		pF

6.8 36 V Single Supply: Electrical Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 30 V I_D = –10 mA Refer to On-Resistance	25°C		4	6.2	Ω
			–40°C to +85°C			7.9	Ω
			–40°C to +125°C			9.4	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 30 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 30 V I_S = –10 mA Refer to On-Resistance	25°C		0.4	1.8	Ω
			–40°C to +85°C			2.5	Ω
			–40°C to +125°C			3.1	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 18 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.015		Ω/°C
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V Refer to 节 7.2	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–2		2	nA
			–40°C to +125°C	–10		10	nA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is off V_S = 30 V / 1 V V_D = 1 V / 30 V Refer to 节 7.2	25°C	–0.5	0.05	0.5	nA
			–40°C to +85°C	–12		12	nA
			–40°C to +125°C	–85		85	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current(2)	V_{DD} = 39.6 V, V_{SS} = 0 V Switch state is on V_S = V_D = 30 V or 1 V Refer to 节 7.3	25°C	–0.5	0.05	0.5	nA
			–40°C to +85°C	–11		11	nA
			–40°C to +125°C	–78		78	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 39.6 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		55	86	µA
			–40°C to +85°C			90	µA
			–40°C to +125°C			105	µA

(1) When V_S is positive, V_D is negative, and vice versa.
(2) When V_S is at a voltage potential, V_D is floating, and vice versa.

6.9 36 V Single Supply: Switching Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		105	200	ns
			–40°C to +85°C			225	ns
			–40°C to +125°C			240	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to 节 7.5	25°C		115	200	ns
			–40°C to +85°C			220	ns
			–40°C to +125°C			240	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 18 V R_L = 300 Ω, C_L = 35 pF Refer to 节 7.5	25°C		90	290	ns
			–40°C to +85°C			305	ns
			–40°C to +125°C			315	ns
t_{BBM}	Break-before-make time delay	V_S = 18 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		40		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.14		ms
			–40°C to +85°C		0.15		ms
			–40°C to +125°C		0.15		ms
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF Refer to 节 7.8	25°C		2.5		ns
Q_{INJ}	Charge injection	V_S = 18 V, C_L = 100 pF Refer to 节 7.9	25°C		2		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth (TMUX6208)	R_L = 50 Ω, C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		30		MHz
BW	–3dB Bandwidth (TMUX6209)	R_L = 50 Ω, C_L = 5 pF V_S = 6 V	25°C		50		MHz
I_L	Insertion loss	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.35		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω, C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–70		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} =18 V, V_{BIAS} = 18 V R_L = 10 kΩ, C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0003		%
$C_{S(OFF)}$	Source off capacitance	V_S = 18 V, f = 1 MHz	25°C		15		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6208)	V_S = 18 V, f = 1 MHz	25°C		138		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6209)	V_S = 18 V, f = 1 MHz	25°C		68		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6208)	V_S = 18 V, f = 1 MHz	25°C		185		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6209)	V_S = 18 V, f = 1 MHz	25°C		115		pF

6.10 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		7	11.8	Ω
			–40°C to +85°C			14.2	Ω
			–40°C to +125°C			16.5	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 10 V I_D = –10 mA Refer to On-Resistance	25°C		0.2	0.7	Ω
			–40°C to +85°C			0.8	Ω
			–40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = 0 V to 10 V I_S = –10 mA Refer to On-Resistance	25°C		1.7	3.4	Ω
			–40°C to +85°C			3.8	Ω
			–40°C to +125°C			4.6	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 6 V, I_S = –10 mA Refer to On-Resistance	–40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to 节 7.2	25°C	–0.4	0.04	0.4	nA
			–40°C to +85°C	–1		1	nA
			–40°C to +125°C	–8		8	nA
$I_{D(OFF)}$	Drain off leakage current[1]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is off V_S = 10 V / 1 V V_D = 1 V / 10 V Refer to 节 7.2	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–5		5	nA
			–40°C to +125°C	–30		30	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[2]	V_{DD} = 13.2 V, V_{SS} = 0 V Switch state is on V_S = V_D = 10 V or 1 V Refer to 节 7.3	25°C	–0.4	0.05	0.4	nA
			–40°C to +85°C	–4		4	nA
			–40°C to +125°C	–28		28	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		–40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		–40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		–40°C to +125°C		0.4	2	µA
I_{IL}	Input leakage current		–40°C to +125°C	–0.1	–0.005		µA
C_{IN}	Logic input capacitance		–40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = 13.2 V, V_{SS} = 0 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		30	48	µA
			–40°C to +85°C			54	µA
			–40°C to +125°C			65	µA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.11 12 V Single Supply: Switching Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		180	210	ns
			–40°C to +85°C			245	ns
			–40°C to +125°C			276	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to 节 7.5	25°C		115	202	ns
			–40°C to +85°C			235	ns
			–40°C to +125°C			265	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 8 V R_L = 300 Ω, C_L = 35 pF Refer to 节 7.5	25°C		290	318	ns
			–40°C to +85°C			350	ns
			–40°C to +125°C			370	ns
t_{BBM}	Break-before-make time delay	V_S = 8 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.17	1	ms
			–40°C to +125°C		0.17	1	ms
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF Refer to 节 7.8	25°C		2.5		ns
Q_{INJ}	Charge injection	V_S = 6 V, C_L = 100 pF Refer to 节 7.9	25°C		2		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 100 kHz	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 100 kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth (TMUX6208)	R_L = 50 Ω, C_L = 5 pF V_S = 6 V Refer to Bandwidth	25°C		28		MHz
BW	–3dB Bandwidth (TMUX6209)	R_L = 50 Ω, C_L = 5 pF V_S = 6 V	25°C		55		MHz
I_L	Insertion loss	R_L = 50 Ω, C_L = 5 pF V_S = 6 V, f = 1 MHz	25°C		–0.6		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω, C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–74		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 6 V, V_{BIAS} = 6 V R_L = 10 kΩ, C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0007		%
$C_{S(OFF)}$	Source off capacitance	V_S = 6 V, f = 1 MHz	25°C		17		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6208)	V_S = 6 V, f = 1 MHz	25°C		155		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6209)	V_S = 6 V, f = 1 MHz	25°C		78		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6208)	V_S = 6 V, f = 1 MHz	25°C		200		pF

6.11 12 V Single Supply: Switching Characteristics （续）

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6209)	V_S = 6 V, f = 1 MHz	25°C		122		pF

6.12 ±5 V Dual Supply: Electrical Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = – 5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = – 5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_{DD} = +4.5 V, V_{SS} = – 4.5 V V_S = – 4.5 V to +4.5 V I_D = – 10 mA	25°C		7	13.5	Ω
			– 40°C to +85°C			16.2	Ω
			– 40°C to +125°C			18.5	Ω
Δ R_{ON}	On-resistance mismatch between channels	V_S = – 4.5 V to +4.5 V I_D = – 10 mA	25°C		0.2	0.7	Ω
			– 40°C to +85°C			0.8	Ω
			– 40°C to +125°C			0.9	Ω
$R_{ON\ FLAT}$	On-resistance flatness	V_S = – 4.5 V to +4.5 V I_D = – 10 mA	25°C		2	3.8	Ω
			– 40°C to +85°C			4.2	Ω
			– 40°C to +125°C			4.9	Ω
$R_{ON\ DRIFT}$	On-resistance drift	V_S = 0 V, I_S = – 10 mA	– 40°C to +125°C		0.03		Ω/°C
$I_{S(OFF)}$	Source off leakage current[(1)]	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Switch state is off V_S = +4.5 V / – 4.5 V V_D = – 4.5 V / + 4.5 V	25°C	– 0.5	0.02	0.5	nA
			– 40°C to +85°C	– 1.5		1.5	nA
			– 40°C to +125°C	– 8		8	nA
$I_{D(OFF)}$	Drain off leakage current[(1)]	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Switch state is off V_S = +4.5 V / – 4.5 V V_D = – 4.5 V / + 4.5 V	25°C	– 0.5	0.04	0.5	nA
			– 40°C to +85°C	– 3.5		3.5	nA
			– 40°C to +125°C	– 28		28	nA
$I_{S(ON)}$ $I_{D(ON)}$	Channel on leakage current[(2)]	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Switch state is on V_S = V_D = ±4.5 V	25°C	– 0.5	0.04	0.5	nA
			– 40°C to +85°C	– 3		3	nA
			– 40°C to +125°C	– 26		26	nA
LOGIC INPUTS (EN, A0, A1, A2)							
V_{IH}	Logic voltage high		– 40°C to +125°C	1.3		36	V
V_{IL}	Logic voltage low		– 40°C to +125°C	0		0.8	V
I_{IH}	Input leakage current		– 40°C to +125°C		0.4	2	μA
I_{IL}	Input leakage current		– 40°C to +125°C	– 0.1	– 0.005		μA
C_{IN}	Logic input capacitance		– 40°C to +125°C		3.5		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		25	38	μA
			– 40°C to +85°C			44	μA
			– 40°C to +125°C			55	μA
I_{SS}	V_{SS} supply current	V_{DD} = +5.5 V, V_{SS} = – 5.5 V Logic inputs = 0 V, 5 V, or V_{DD}	25°C		2	6.2	μA
			– 40°C to +85°C			7	μA
			– 40°C to +125°C			15	μA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.
(2) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.13 ±5 V Dual Supply: Switching Characteristics

V_{DD} = +5 V ± 10%, V_{SS} = –5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = –5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{TRAN}	Transition time from control input	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to Transition Time	25°C		125	250	ns
			–40°C to +85°C			280	ns
			–40°C to +125°C			305	ns
$t_{ON\ (EN)}$	Turn-on time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to 节 7.5	25°C		128	245	ns
			–40°C to +85°C			278	ns
			–40°C to +125°C			305	ns
$t_{OFF\ (EN)}$	Turn-off time from enable	V_S = 3 V R_L = 300 Ω, C_L = 35 pF Refer to 节 7.5	25°C		300	372	ns
			–40°C to +85°C			400	ns
			–40°C to +125°C			420	ns
t_{BBM}	Break-before-make time delay	V_S = 3 V, R_L = 300 Ω, C_L = 35 pF Refer to Break-Before-Make	25°C		50		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
$T_{ON\ (VDD)}$	Device turn on time (V_{DD} to output)	V_{DD} rise time = 1 µs R_L = 300 Ω, C_L = 35 pF Refer to Turn-on (VDD) Time	25°C		0.16		ms
			–40°C to +85°C		0.17	1	ms
			–40°C to +125°C		0.17	1	ms
t_{PD}	Propagation delay	R_L = 50 Ω, C_L = 5 pF Refer to 节 7.8	25°C		2		ns
Q_{INJ}	Charge injection	V_S = 0 V, C_L = 100 pF Refer to 节 7.9	25°C		1.2		pC
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Off Isolation	25°C		–82		dB
O_{ISO}	Off-isolation	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 1 MHz Refer to Off Isolation	25°C		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 100 kHz Refer to Crosstalk	25°C		–85		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 1MHz Refer to Crosstalk	25°C		–65		dB
BW	–3dB Bandwidth (TMUX6208)	R_L = 50 Ω, C_L = 5 pF V_S = 0 V Refer to Bandwidth	25°C		28		MHz
BW	–3dB Bandwidth (TMUX6209)	R_L = 50 Ω, C_L = 5 pF V_S = 0 V	25°C		54		MHz
I_L	Insertion loss	R_L = 50 Ω, C_L = 5 pF V_S = 0 V, f = 1 MHz	25°C		–0.7		dB
ACPSRR	AC Power Supply Rejection Ratio	V_{PP} = 0.62 V on V_{DD} and V_{SS} R_L = 50 Ω, C_L = 5 pF, f = 1 MHz Refer to ACPSRR	25°C		–76		dB
THD+N	Total Harmonic Distortion + Noise	V_{PP} = 5 V, V_{BIAS} = 0 V R_L = 10 kΩ, C_L = 5 pF, f = 20 Hz to 20 kHz Refer to THD + Noise	25°C		0.0017		%
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V, f = 1 MHz	25°C		18		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6208)	V_S = 0 V, f = 1 MHz	25°C		160		pF
$C_{D(OFF)}$	Drain off capacitance (TMUX6209)	V_S = 0 V, f = 1 MHz	25°C		80		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6208)	V_S = 0 V, f = 1 MHz	25°C		205		pF

6.13 ±5 V Dual Supply: Switching Characteristics （续）

V_{DD} = +5 V ± 10%, V_{SS} = –5 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +5 V, V_{SS} = –5 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance (TMUX6209)	V_S = 0 V, f = 1 MHz	25°C		124		pF

6.14 Typical Characteristics

at T_A = 25°C (unless otherwise noted)

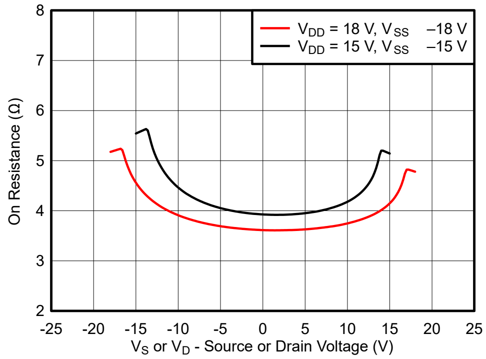


图 6-1. On-Resistance vs Source or Drain Voltage – Dual Supply

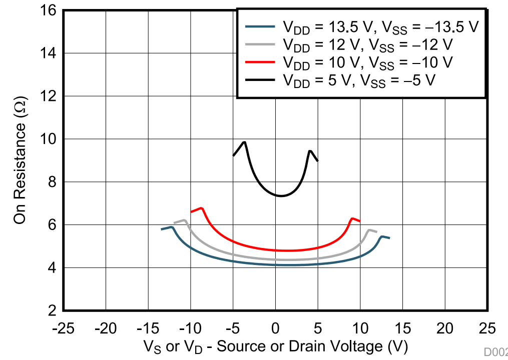


图 6-2. On-Resistance vs Source or Drain Voltage – Dual Supply

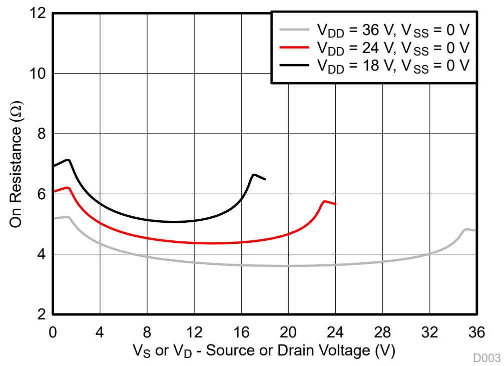


图 6-3. On-Resistance vs Source or Drain Voltage – Single Supply

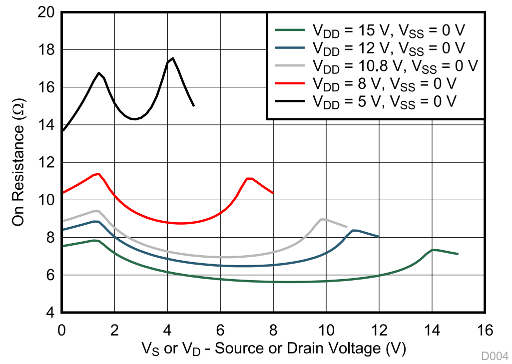
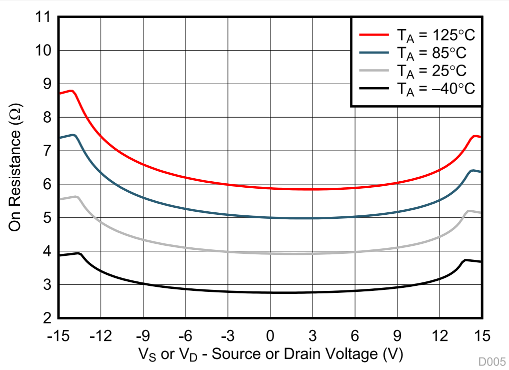
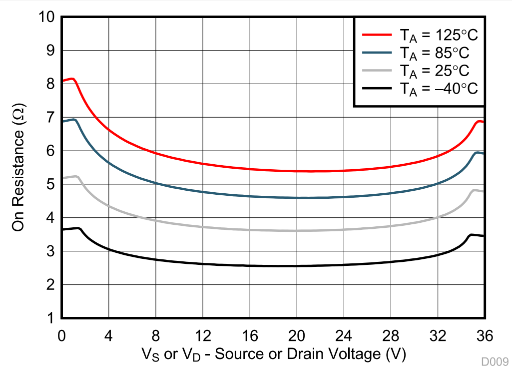


图 6-4. On-Resistance vs Source or Drain Voltage – Single Supply



V_{DD} = 15 V, V_{SS} = -15 V

图 6-5. On-Resistance vs Temperature

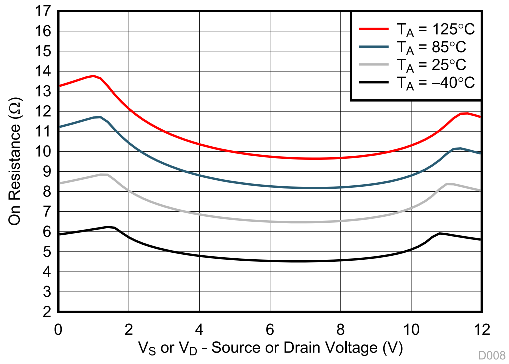


V_{DD} = 36 V, V_{SS} = 0 V

图 6-6. On-Resistance vs Temperature

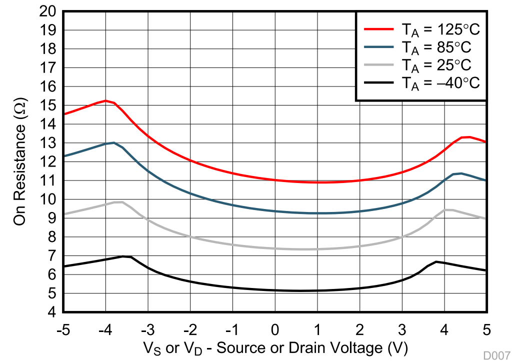
6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



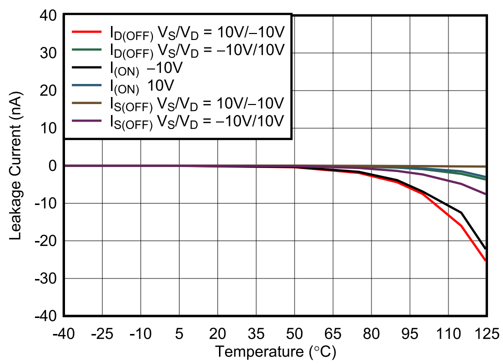
V_{DD} = 12 V, V_{SS} = 0 V

图 6-7. On-Resistance vs Temperature



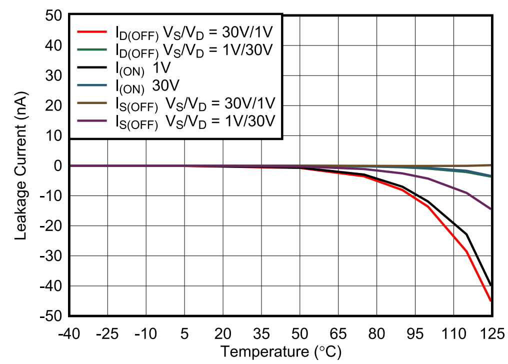
V_{DD} = 5 V, V_{SS} = -5 V

图 6-8. On-Resistance vs Temperature



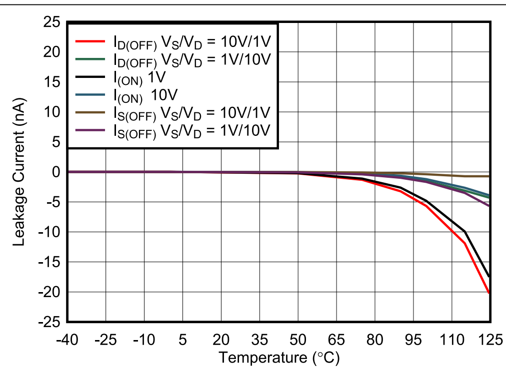
V_{DD} = 15 V, V_{SS} = -15 V

图 6-9. Leakage Current vs Temperature



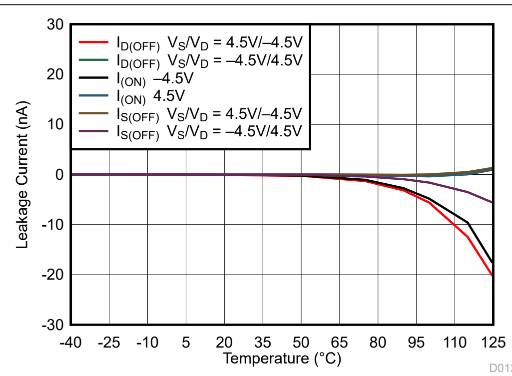
V_{DD} = 36 V, V_{SS} = 0 V

图 6-10. Leakage Current vs Temperature



V_{DD} = 12 V, V_{SS} = 0 V

图 6-11. Leakage Current vs Temperature



V_{DD} = 5 V, V_{SS} = -5 V

图 6-12. Leakage Current vs Temperature

6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)

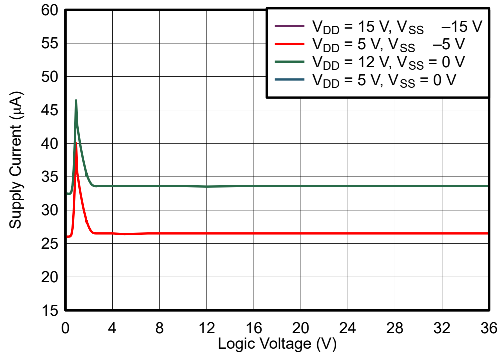


图 6-13. Supply Current vs Logic Voltage

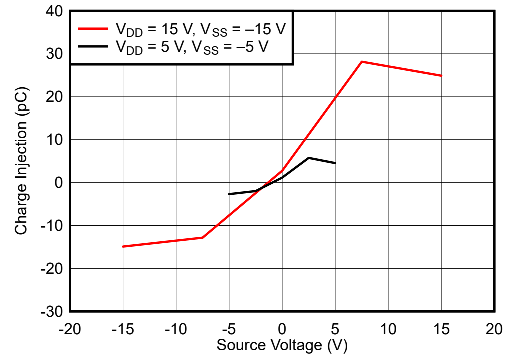


图 6-14. Charge Injection vs Source Voltage – Dual Supply

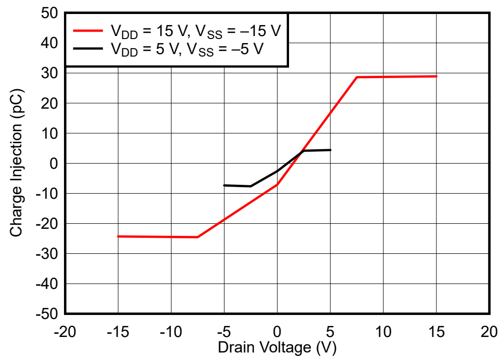


图 6-15. Charge Injection vs Drain Voltage – Dual Supply

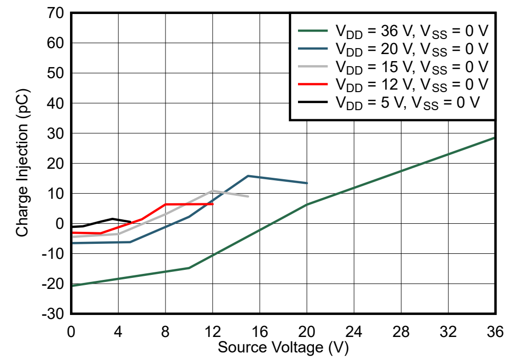


图 6-16. Charge Injection vs Source Voltage – Single Supply

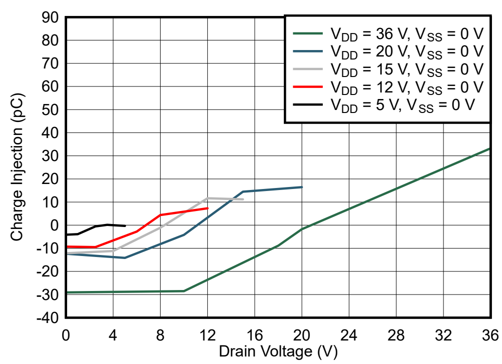


图 6-17. Charge Injection vs Drain Voltage – Single Supply

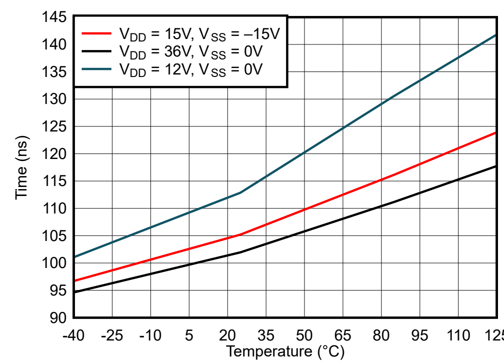
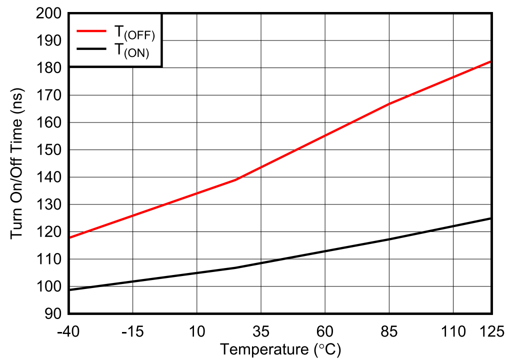


图 6-18. $T_{TRANSITION}$ vs Temperature

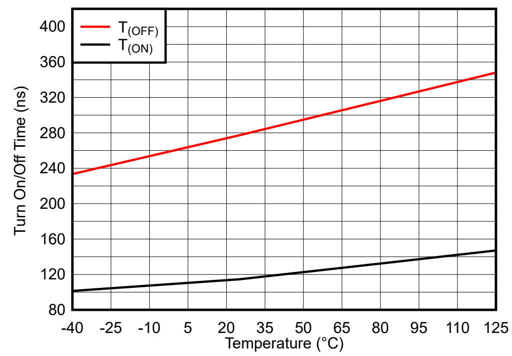
6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



V_{DD} = 15 V, V_{SS} = -15 V

图 6-19. T_{ON} and T_{OFF} vs Temperature



V_{DD} = 36 V, V_{SS} = 0 V

图 6-20. T_{ON} and T_{OFF} vs Temperature

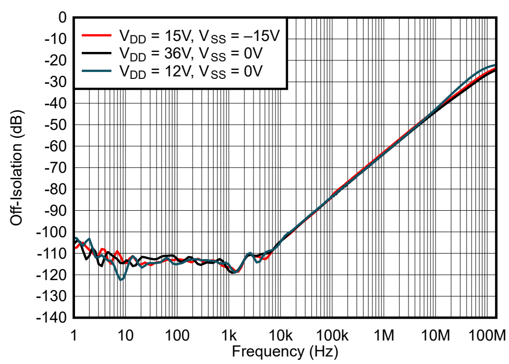
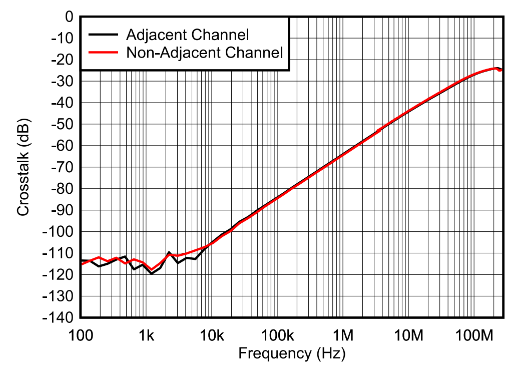


图 6-21. Off-Isolation vs Frequency



V_{DD} = 15 V, V_{SS} = -15 V

图 6-22. Crosstalk vs Frequency

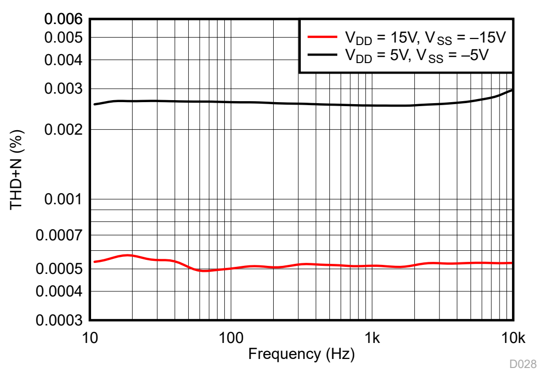


图 6-23. THD+N vs Frequency (Dual Supply)

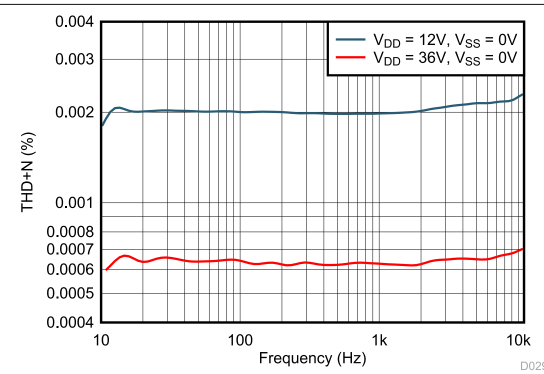
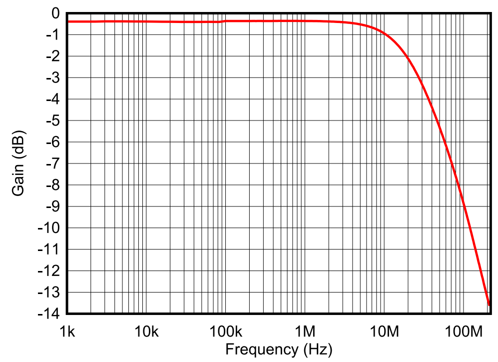


图 6-24. THD+N vs Frequency (Single Supply)

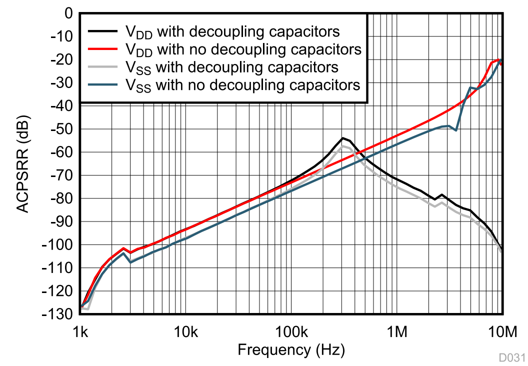
6.14 Typical Characteristics (continued)

at T_A = 25°C (unless otherwise noted)



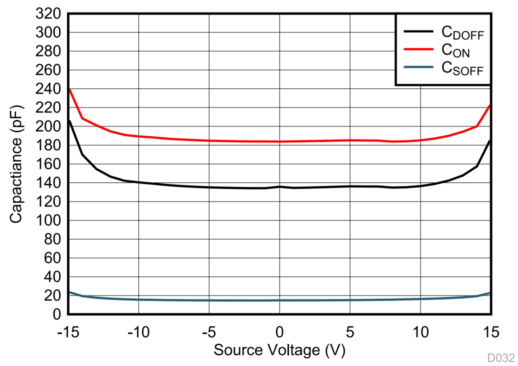
V_{DD} = +15 V, V_{SS} = -15 V

图 6-25. On Response vs Frequency



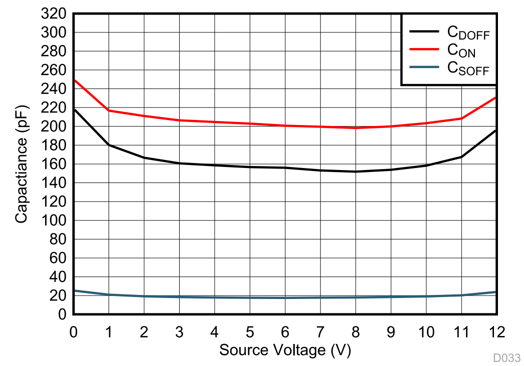
V_{DD} = +15 V, V_{SS} = -15 V

图 6-26. ACPSRR vs Frequency



V_{DD} = +15 V, V_{SS} = -15 V

图 6-27. Capacitance vs Source Voltage or Drain Voltage



V_{DD} = 12 V, V_{SS} = 0 V

图 6-28. Capacitance vs Source Voltage or Drain Voltage

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. 图 7-1 shows the measurement setup used to measure R_{ON}. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$.

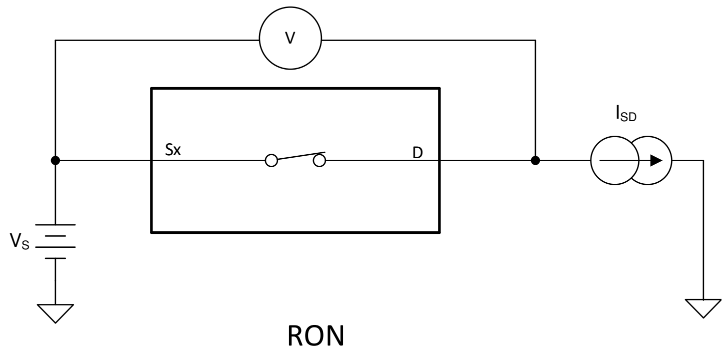


图 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

- Source off-leakage current
- Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

图 7-2 shows the setup used to measure both off-leakage currents.

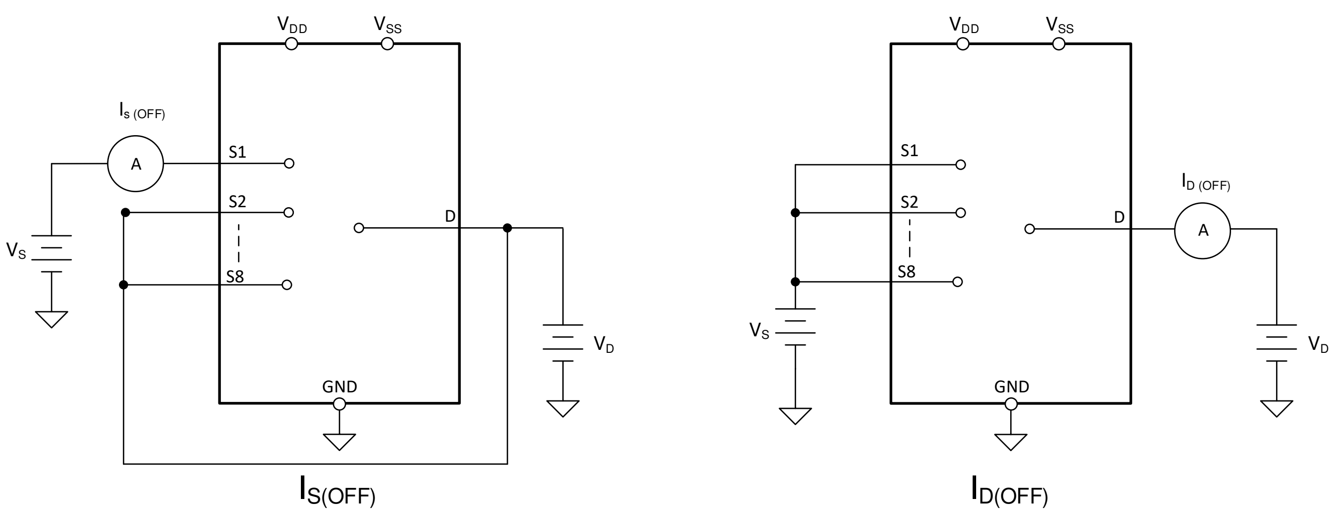


图 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

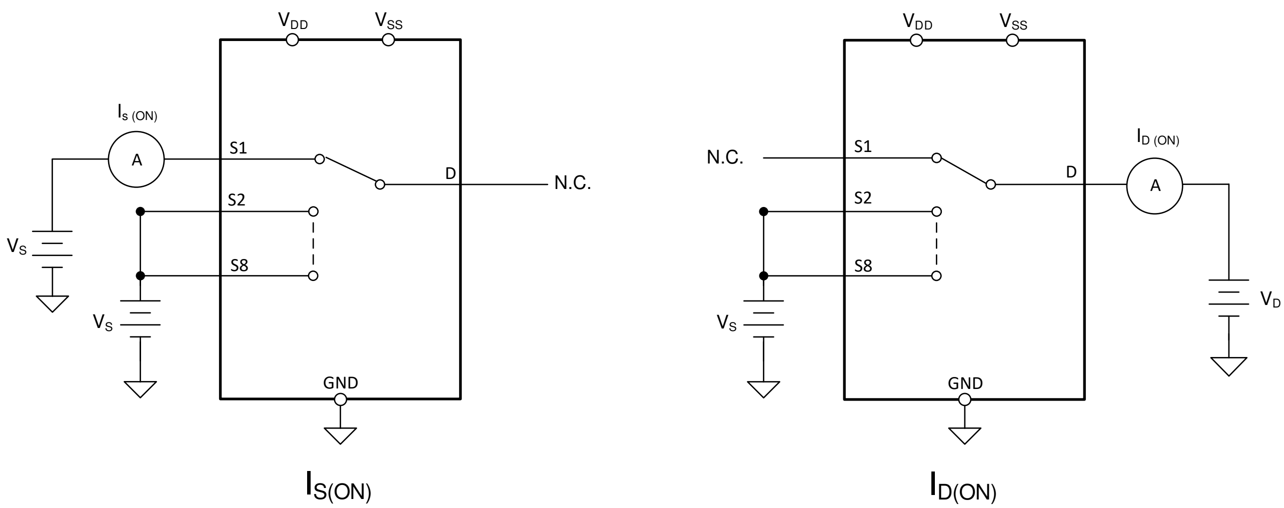


图 7-3. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 90% after the address signal has risen or fallen past the logic threshold. The 90% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

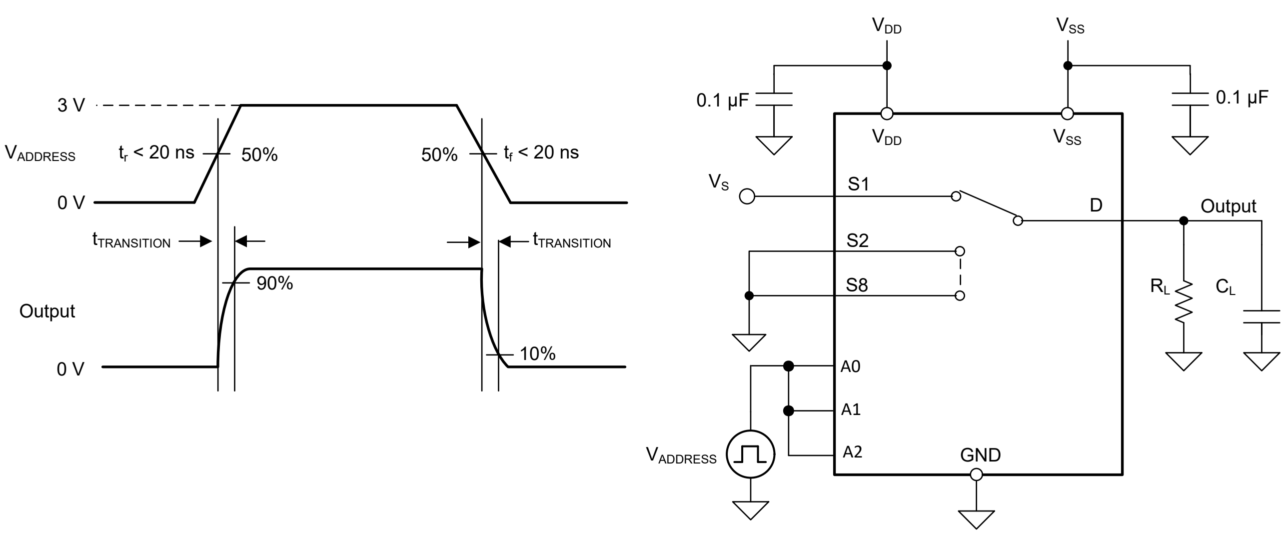


图 7-4. Transition-Time Measurement Setup

7.5 $t_{ON(EN)}$ and $t_{OFF(EN)}$

Turn-on time is defined as the time taken by the output of the device to rise to 90% after the enable has risen past the logic threshold. The 90% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-5 shows the setup used to measure turn-on time, denoted by the symbol $t_{ON(EN)}$.

Turn-off time is defined as the time taken by the output of the device to fall to 10% after the enable has fallen past the logic threshold. The 10% measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 图 7-5 shows the setup used to measure turn-off time, denoted by the symbol $t_{OFF(EN)}$.

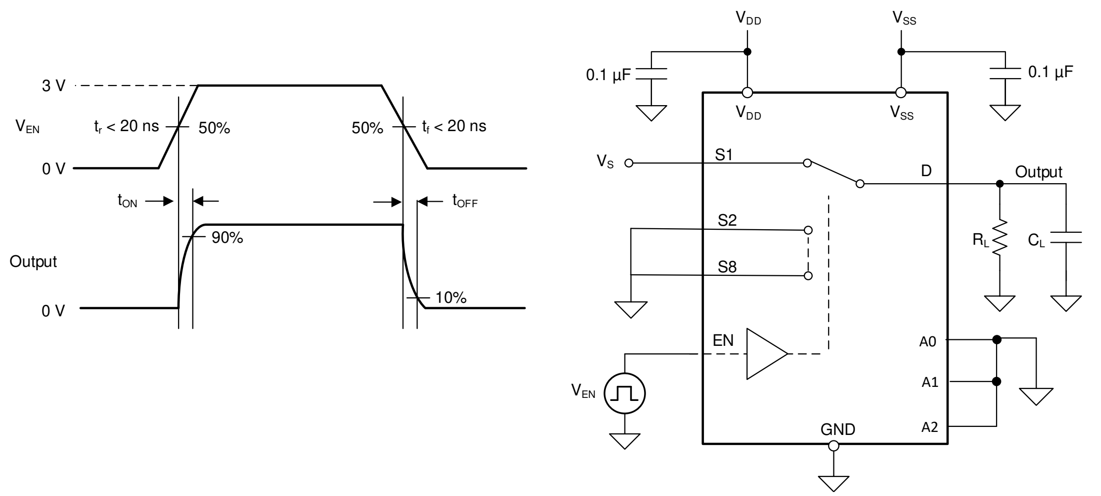


图 7-5. Turn-On and Turn-Off Time Measurement Setup

7.6 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 7-6 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

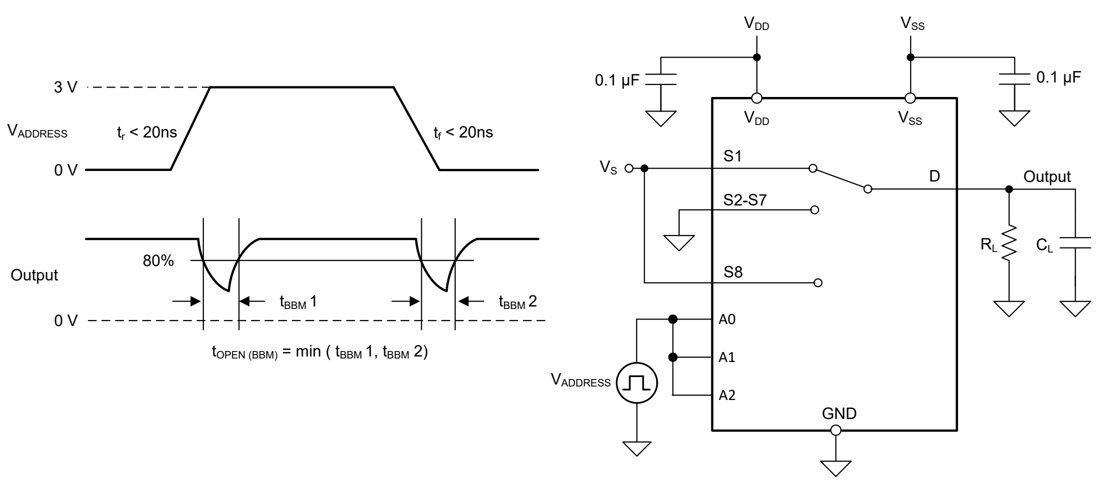


图 7-6. Break-Before-Make Delay Measurement Setup

7.7 $t_{ON\ (VDD)}$ Time

The $t_{ON\ (VDD)}$ time is defined as the time taken by the output of the device to rise to 90% after the supply has risen past the supply threshold. The 90% measurement is used to provide the timing of the device turning on in the system. 图 7-7 shows the setup used to measure turn on time, denoted by the symbol $t_{ON\ (VDD)}$.

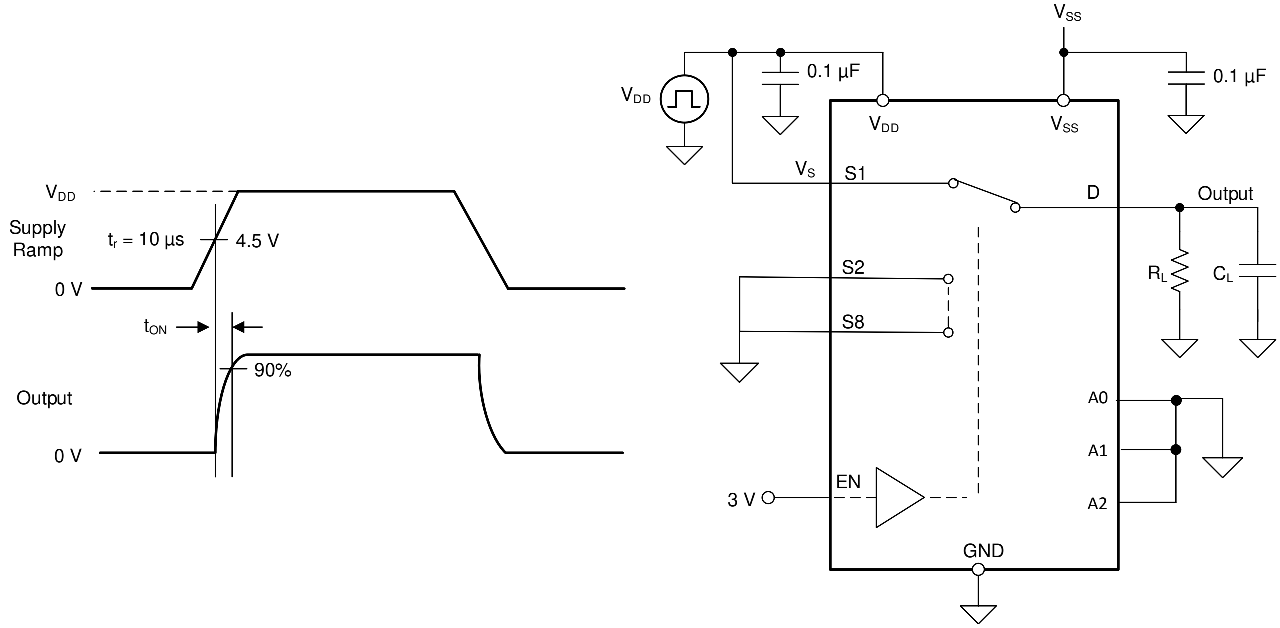


图 7-7. $t_{ON\ (VDD)}$ Time Measurement Setup

7.8 Propagation Delay

Propagation delay is defined as the time taken by the output of the device to rise or fall 50% after the input signal has risen or fallen past the 50% threshold. 图 7-8 shows the setup used to measure propagation delay, denoted by the symbol t_{PD}.

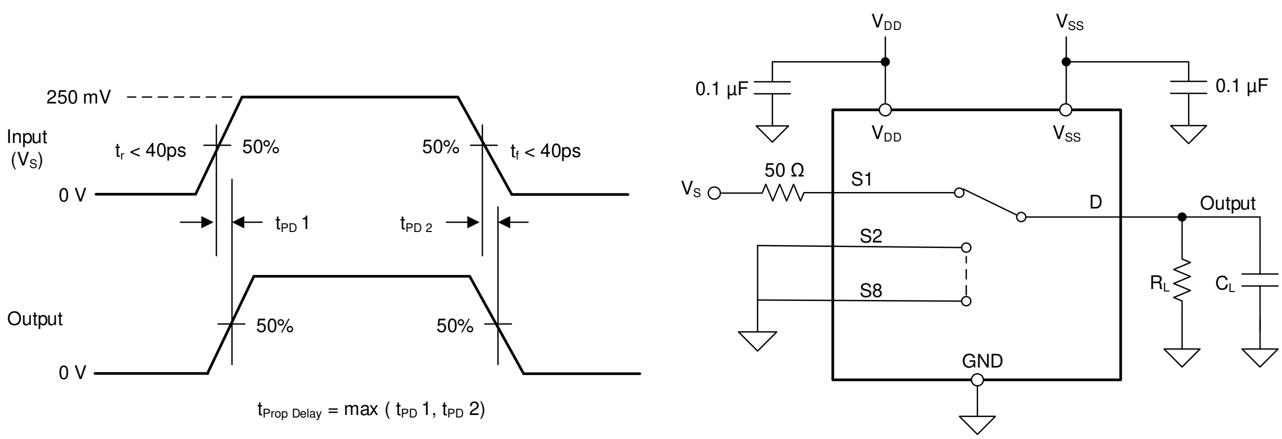


图 7-8. Propagation Delay Measurement Setup

7.9 Charge Injection

The TMUX6208 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 图 7-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

The TMUX6208 and have a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 图 7-9 shows the setup used to measure charge injection from source (Sx) to drain (D).

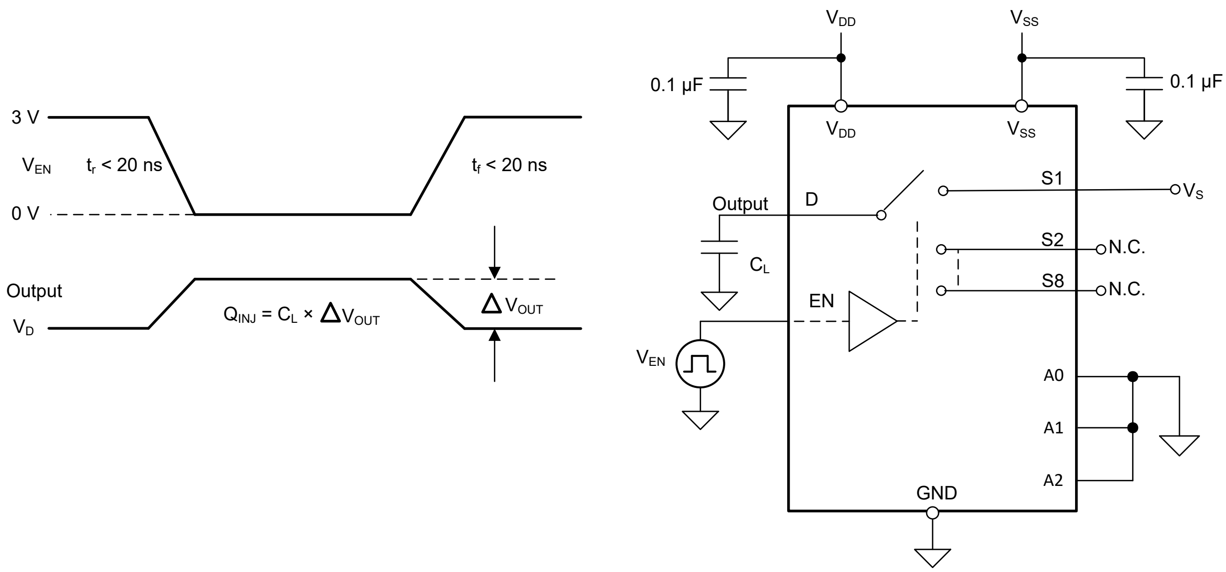
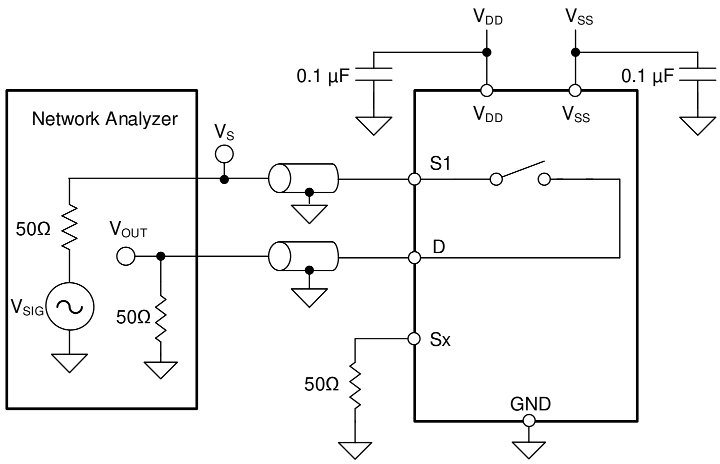


图 7-9. Charge-Injection Measurement Setup

7.10 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 图 7-10 shows the setup used to measure, and the equation used to calculate off isolation.

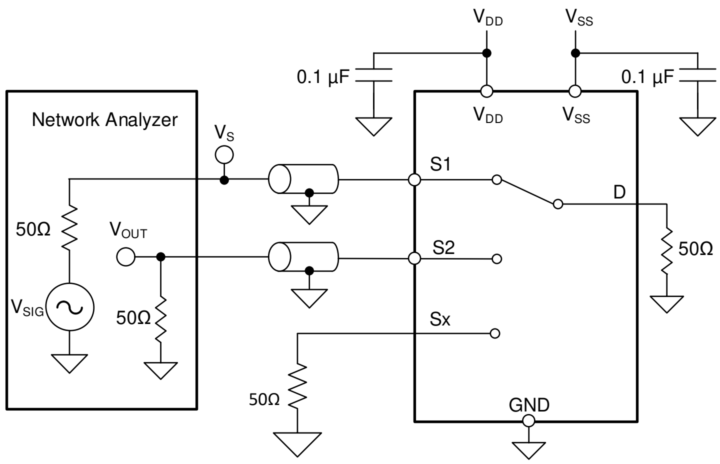


$$Off\ Isolation = 20 \times Log\frac{V_{OUT}}{V_S}$$

图 7-10. Off Isolation Measurement Setup

7.11 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 图 7-11 shows the setup used to measure and the equation used to calculate crosstalk.

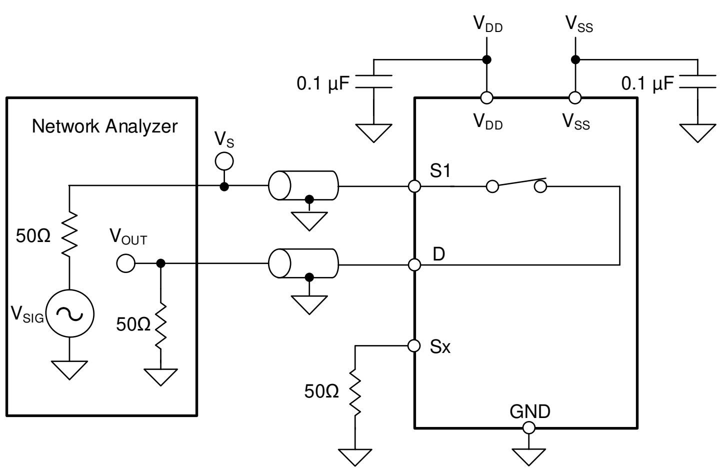


$$Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S}$$

图 7-11. Crosstalk Measurement Setup

7.12 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 图 7-12 shows the setup used to measure bandwidth.



$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S}$$

图 7-12. Bandwidth Measurement Setup

7.13 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the device varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD.

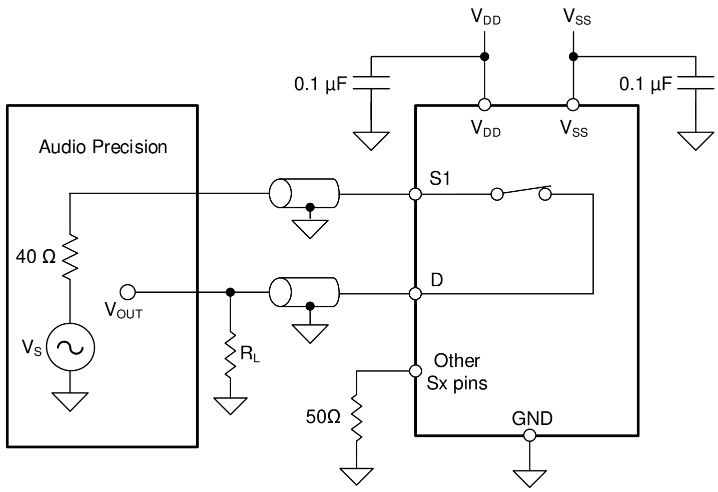
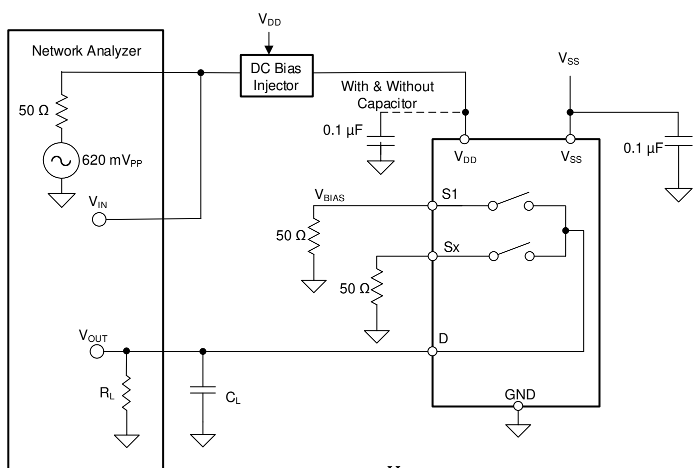


图 7-13. THD Measurement Setup

7.14 Power Supply Rejection Ratio (PSRR)

PSRR measures the ability of a device to prevent noise and spurious signals that appear on the supply voltage pin from coupling to the output of the switch. The DC voltage on the device supply is modulated by a sine wave of 620mVPP. The ratio of the amplitude of signal on the output to the amplitude of the modulated signal is the ACPSRR. A high ratio represents a high degree of tolerance to supply rail variation.

The below shows how the decoupling capacitors reduce high frequency noise on the supply pins. This helps stabilize the supply and immediately filter as much of the supply noise as possible.



$$PSRR = 20 \times Log\frac{V_{OUT}}{V_{IN}}$$

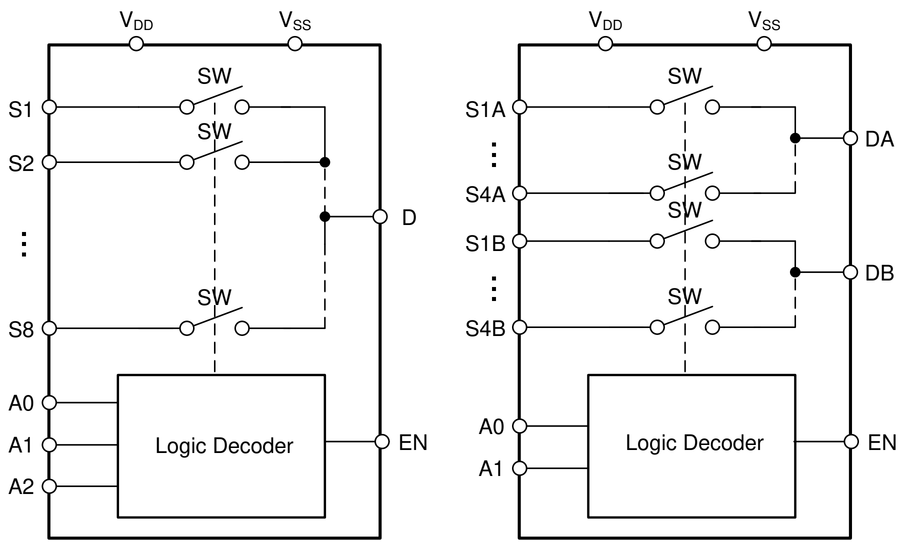
图 7-14. ACPSRR Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX6208 is an 8:1, 1-channel multiplexer and the TMUX6209 is a 4:1, 2 channel multiplexer. Each input is turned on or turned off based on the state of the address lines and enable pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX6208 and TMUX6209 conduct equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail-to-Rail Operation

The valid signal path input or output voltage for TMUX6208 and TMUX6209 ranges from V_{SS} to V_{DD}.

8.3.3 1.8 V Logic Compatible Inputs

TMUX6208 and TMUX6209 support 1.8-V logic compatible control for all logic control inputs. 1.8-V logic level inputs allows the to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches* .

8.3.4 Integrated Pull-Down Resistor on Logic Pins

The TMUX620x has internal weak pull-down resistors to GND to ensure the logic pins are not left floating. The value of this pull-down resistor is approximatly 4 MΩ, but is clamped to about 1 µA at higher voltages. This feature integrates up to four external components and reduces system size and cost.

8.3.5 Fail-Safe Logic

TMUX6208 and TMUX6209 support Fail-Safe Logic on the control input pins (EN and Ax) allowing it to operate up to 36 V, regardless of the state of the supply pins. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the TMUX6208 and TMUX6209 logic input pins to ramp up to +36 V while V_{DD} and

V_{SS} = 0 V. The logic control inputs are protected against positive faults of up to +36 V in powered-off condition, but do not offer protection against negative overvoltage conditions.

8.3.6 Latch-Up Immune

Latch-Up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-Up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX62xx family of devices are constructed on Silicon on Insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage or current injections. The latch-up immunity feature allows the TMUX62xx family of switches and multiplexers to be used in harsh environments. For more information on latch-up immunity refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability* .

8.3.7 Ultra-Low Charge Injection

图 8-1 shows that the TMUX620x have a transmission gate topology. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed.

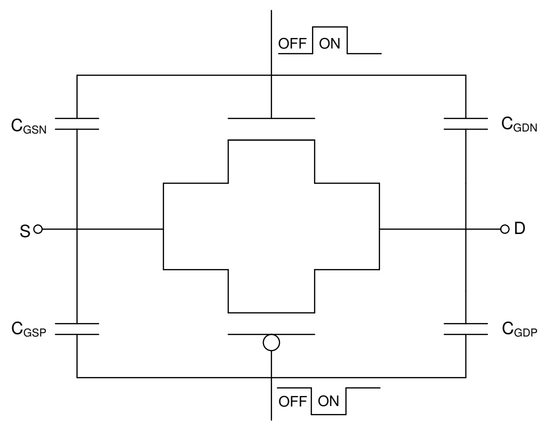


图 8-1. Transmission Gate Topology

The TMUX620x contain specialized architecture to reduce charge injection on the Drain (D). To further reduce charge injection in a sensitive application, a compensation capacitor (Cp) can be added on the Source (Sx). This will ensure that excess charge from the switch transition will be pushed into the compensation capacitor on the Source (Sx) instead of the Drain (D). As a general rule of thumb, Cp should be 20x larger than the equivalent load capacitance on the Drain (D). 图 8-2 shows charge injection variation with different compensation capacitors on the Source side. This plot was captured on the TMUX6219 as part of the TMUX62xx family with a 100pF load capacitance.

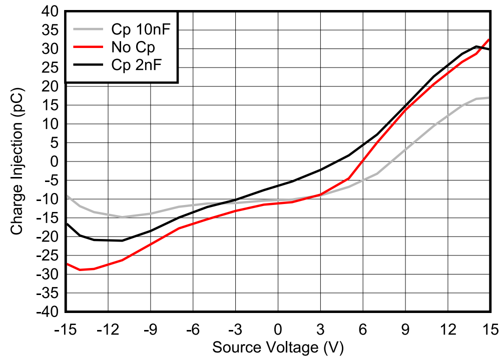


图 8-2. Charge Injection Compesation

8.4 Device Functional Modes

When the EN pin of the TMUX6208 is pulled high, one of the switches is closed based on the state of the Ax pin. Similarly, when the EN pin of the TMUX6209 is pulled high, two of the switches are closed based on the state of the address lines. When the EN pin is pulled low, all of the switches are in an open state regardless of the state of the Ax pin. The control pins can be as high as 36V.

The TMUX6208 and TMUX6209 can be operated without any external components except for the supply decoupling capacitors. The EN and Ax pins have internal pull-down resistors of 4 MΩ. If unused, Ax and EN pins must be tied to GND in order to ensure the device does not consume additional current as highlighted in Implications of Slow or Floating CMOS Inputs. Unused signal path inputs (Sx or D) should be connected to GND.

8.5 Truth Tables

表 8-1 shows the truth tables for the TMUX6208.

表 8-1. TMUX6208 Truth Table

EN	A2	A1	A0	Selected Source Connected To Drain (D) Pin
0	X(1)	X	X	All sources are off (HI-Z)
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1) X denotes *do not care*.

表 8-2 show the truth tables for the TMUX6209.

表 8-2. TMUX6209 Truth Table

EN	A1	A0	Selected Source Connected To Drain (D) Pin
0	X(1)	X	All sources are off (HI-Z)
1	0	0	S1x
1	0	1	S2x
1	1	0	S3x

表 **8-2. TMUX6209 Truth Table（续）**

EN	A1	A0	Selected Source Connected To Drain (D) Pin
1	1	1	S4x

(1) X denotes *do not care*.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TMUX6208 and TMUX6209 are part of the precision switches and multiplexers family of devices. These devices operate with dual supplies (±4.5 V to ±18 V), a single supply (4.5 V to 36 V), or asymmetric supplies (such as VDD = 12 V, VSS = –5 V), and offer true rail-to-rail input and output. The TMUX6208 and TMUX6209 offer low RON, low on and off leakage currents and ultra-low charge injection performance. These features make the TMUX62xx a family of precision, robust, high-performance analog multiplexers for high-voltage, industrial applications.

9.2 Typical Application

One example to take advantage of TMUX6208 performance is the implementation of multiplexed data aquisition front end for multiple input sensors. Applications such as analog input modules for programmable logic controllers (PLCs), data aquisition (DAQ), and seminconducter test systems commonly need to monitor multiple signals into a single ADC channel. The multiple inputs can come from different system voltages being montitored, or environemental sensors such as temperature or humidity. 图 9-1 shows a simplified example of monitoring multiple inputs into a single ADC using a multiplexer.

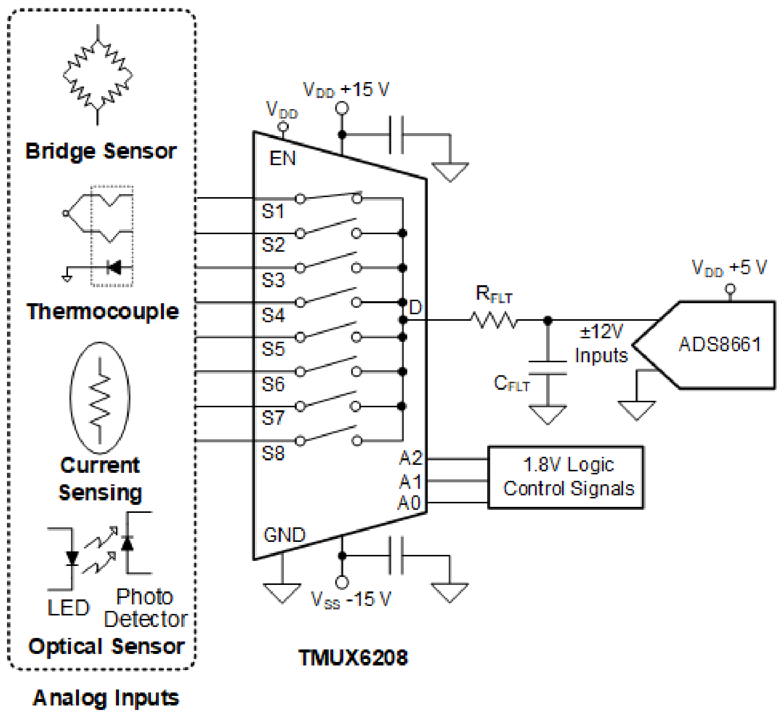


图 9-1. Multiplexed Data Aqcuisition Front End

9.2.1 Design Requirements

表 9-1. Design Parameters

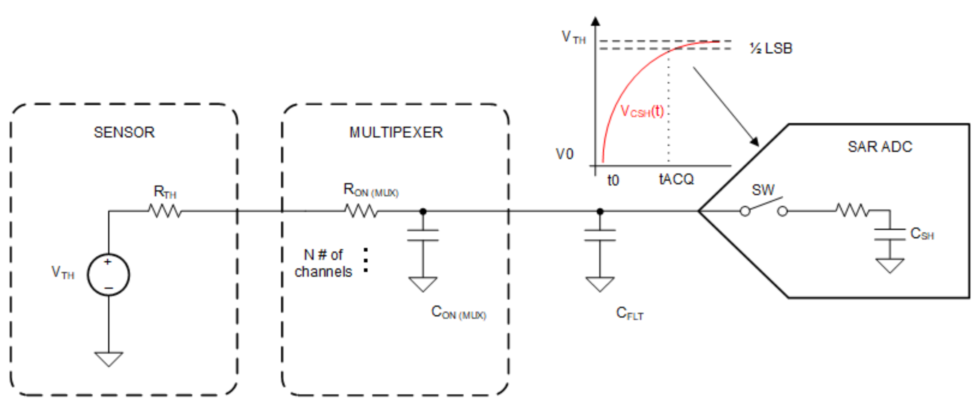
PARAMETER	VALUE
Positive supply (VDD)	+15 V
Negative supply (V_{SS})	-15 V
Input / output signal range	-12 V to 12 V (limit of ADC)
Control logic thresholds	1.8 V compatible
Temperature range	-40°C to +125°C

9.2.2 Detailed Design Procedure

The application shown in 图 9-1 demonstrates how a multiplexer can be used to simplfy the signal chain and monitor multiple input signals to a single ADC channel. In this example the ADC (ADS8661) has software programmable input ranges up to ±12.288 V. The ADC also has overvotlage protection up to ±20 V which allows for the multiplexer to be powered with wider supply voltages than the input signal range to maximize on-resistance performance of the multiplxer, while still maintaining system level overvotlage protection beyond the usuable signal range. Both the multiplexer and the ADC are capable of operation in extended industrial temperature range of -40°C to +125°C allowing for use in a wider array of industrial systems.

Many SAR ADCs have an analog input structure that consists of a sampling switch and a sampling capacitor. Many signal chains will have a driver amplifier to help charge the input of the ADC to meet a fast system aquisition time. However a driver amplifier is not always needed to drive SAR ADCs. 图 9-2 shows a typical diagram of a sensor driving the SAR ADC input directly after being passed through the multiplxer. A filter capacitor (C_{FLT}) is connected to the input of the ADC to reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitor of the ADC.

The sensor block simplifies the device into a Thevenin equivalant voltage source (V_{TH}) and resistance (R_{TH}) which can be extracted from the device datasheets. Similarly the multixplexer can be thought of as a series resistance ($R_{ON(MUX)}$) and capacitance ($C_{ON(MUX)}$). To ensure maximum precison of the signal chain the system should be able to settle within 1/2 of an LSB within the acquisition time of the ADC. 图 9-2 shows the time constant can be calculated. This equation highlights the importance of selecting a multiplexer with low on-resistance to further reduce the system time constant. Additionaly low charge injection performance of the multiplexer is helpful to reduce conversion errors and improve accuracy of the measurements.



$t_{ACQ} > k \times \tau_{FLT}$

- $\tau_{FLT} = (R_{TH} + R_{ON\,(MUX)})\ X\ (C_{FLT} + C_{ON\,(MUX)})$
- k is single pole time constant for N bit ADC

图 9-2. Driving SAR ADC

9.2.3 Application Curve

The low on and off leakage currents of TMUX620x and ultra-low charge injection performance make this device ideal for implementing high precision industrial systems. 图 9-3 shows the plot for the charge injection versus source voltage for the TMUX6208.

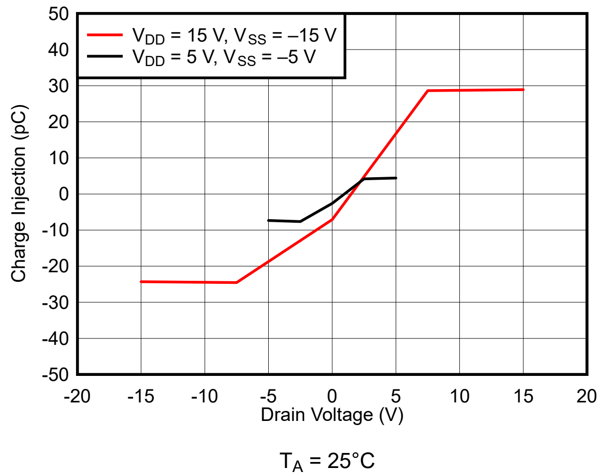


图 9-3. Charge Injection vs Drain Voltage

9.3 Power Supply Recommendations

The TMUX6208 and TMUX6209 operate across a wide supply range of of ±4.5 V to ±18 V (4.5 V to 36 V in single-supply mode). The device also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS} = –5 V.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the supply rails to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF at both the V_{DD} and V_{SS} pins to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground and power planes. Always ensure the ground (GND) connection is established before supplies are ramped.

9.4 Layout

9.4.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 9-4 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

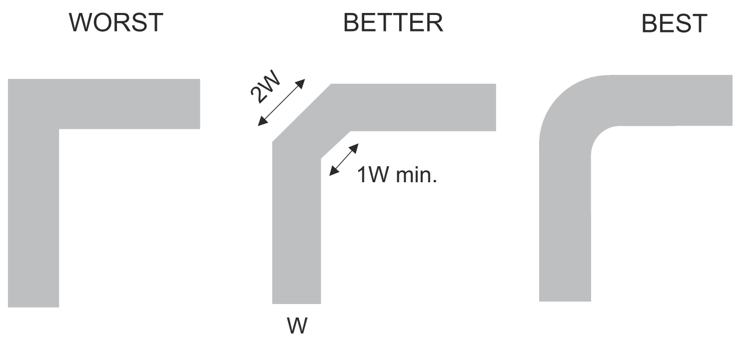


图 9-4. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

图 9-5 and 图 9-6 illustrate an example of a PCB layout with the TMUX6208. Some key considerations are:

- For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between VDD/VSS and GND. We recommend a 0.1 µF and 1 µF capacitor, placing the lowest value capacitor as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
- Using multiple vias in parallel will lower the overall inductance and is beneficial for connection to ground planes.

9.4.2 Layout Example

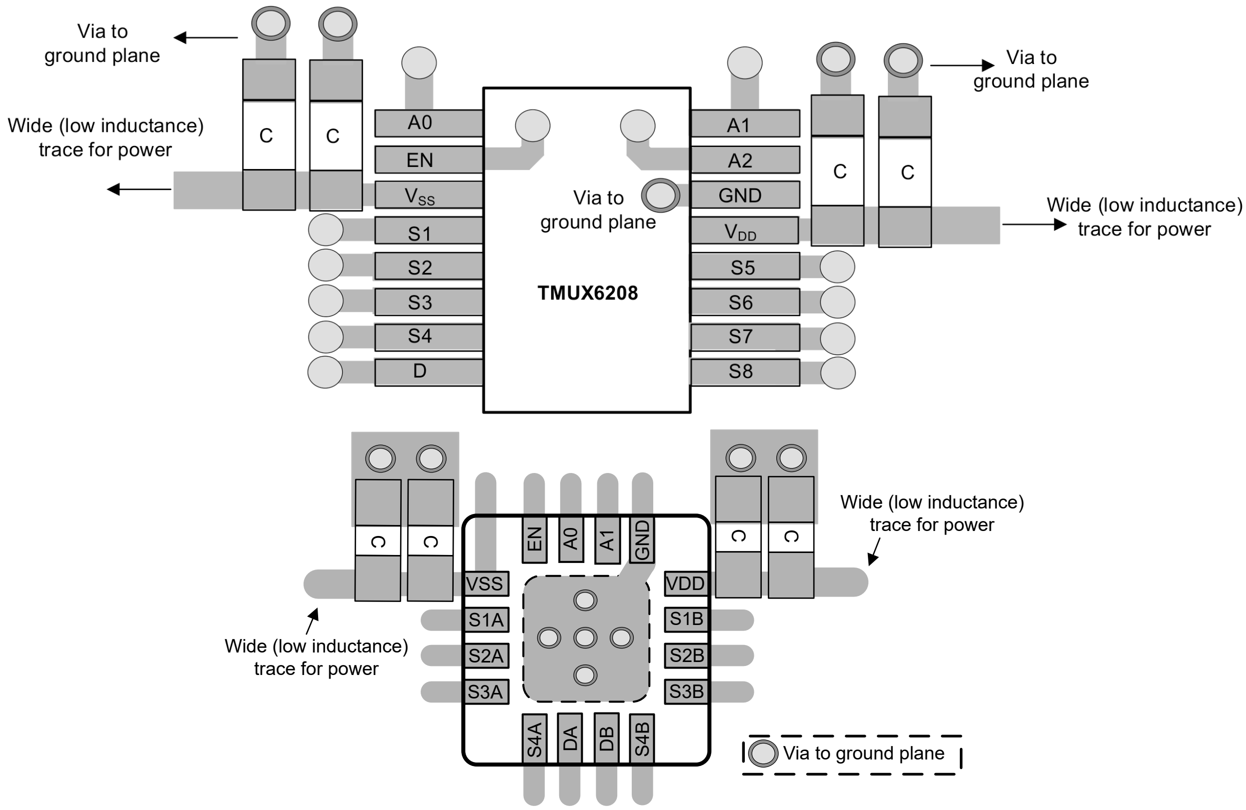
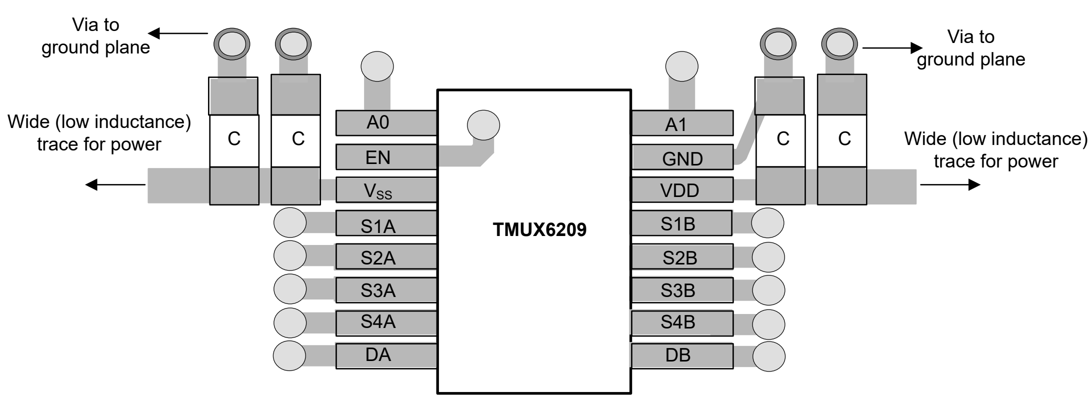


图 9-5. TMUX6208 Layout Example



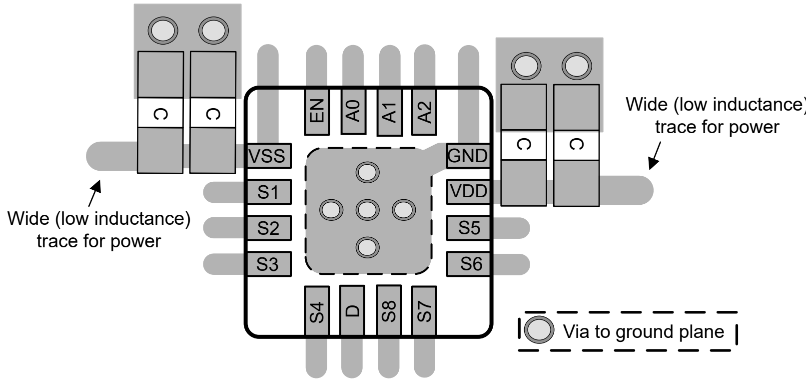


图 9-6. TMUX6209 Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Improve Stability Issues with Low CON Multiplexers* application brief.
- Texas Instruments, *Improving Signal Measurement Accuracy in Automated Test Equipment* application brief
- Texas Instruments, *Sample & Hold Glitch Reduction for Precision Outputs Reference Design* reference guide.
- Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches* application brief.
- Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers* application reports.
- Texas Instruments, *True Differential, 4 x 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit* application reports.
- Texas Instruments, *QFN/SON PCB Attachment* application reports.
- Texas Instruments, *Quad Flatpack No-Lead Logic Packages* application reports.
- Texas Instruments, *Using Latch Up Immune Multiplexers to Help Improve System Reliability* application reports.

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (January 2022) to Revision E (July 2024)	Page
• Updated HBM ESD for all packages	5
• Updated IIH max specification	7

Changes from Revision C (August 2021) to Revision D (January 2022) **Page**

Changes from Revision B (April 2021) to Revision C (August 2021) **Page**

Changes from Revision A (January 2021) to Revision B (April 2021) **Page**

Changes from Revision * (November 2020) to Revision A (January 2021) **Page**

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX6208PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X208	Samples
TMUX6208RUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X208	Samples
TMUX6209PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	X209	Samples
TMUX6209RUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TMUX X209	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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