采用 WCSP 封装并具有 1.2V 逻辑的 TMUX1575 2:1 (SPDT) 4 通道断电保护开关

1 特性

- 宽电源电压范围：1.08V 至 3.6V
- 低导通电容：5pF
- 高带宽：1.8GHz
- -40°C 至 +125°C 工作温度
- 兼容 1.2V 逻辑
- 支持超出电源电压范围的输入电压
- 逻辑引脚上带有集成下拉电阻器
- 双向信号路径
- 失效防护逻辑
- 断电保护

2 应用

- 闪存存储器共享
- JTAG 多路复用
- SPI 多路复用
- eMMC 多路复用
- 智能手表
- 智能追踪器
- 手机
- PC 和笔记本电脑
- 网络接口卡 (NIC)
- 服务器
- 数据中心交换机和路由器
- 无线基础设施
- 楼宇自动化
- ePOS

3 说明

TMUX1575 是一款采用 2:1 (SPDT) 配置的 4 通道互补金属氧化物半导体 (CMOS) 开关。此器件的体积小巧，工作电源电压为 1.08V 至 3.6V，可用于从服务器和通信设备到个人电子设备的广泛应用。此器件可在源极（SxA、SxB）和漏极 (Dx) 引脚上支持双向模拟和数字信号，并且能够传递最高 V_{DD} x 2 的信号，最大输入/输出电压为 3.6V。

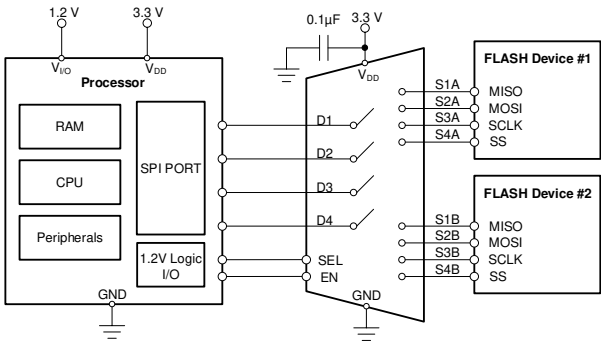
TMUX1575 信号路径上的断电保护功能可在移除电源电压 (V_{DD} = 0V) 时提供隔离。如果没有该保护功能，开关可通过内部 ESD 二极管为电源轨进行反向供电，从而对系统造成潜在损坏。

失效防护逻辑电路允许在电源引脚上施加电压之前，先在逻辑控制引脚上施加电压，从而保护器件免受潜在的损害。所有控制输入都具有兼容 1.2V 逻辑的阈值，因此无需外部逻辑转换。逻辑引脚上带有集成下拉电阻器，无需外部组件，可减小系统尺寸、降低系统成本。

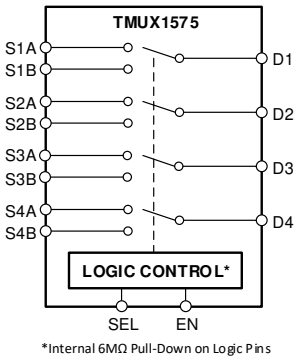
器件信息 (1)

器件型号	封装	封装尺寸（标称值）
TMUX1575	WCSP (16)	1.34mm × 1.34mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。



应用示例



方框图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
October 2020	*	Initial Release

5 Pin Configuration and Functions

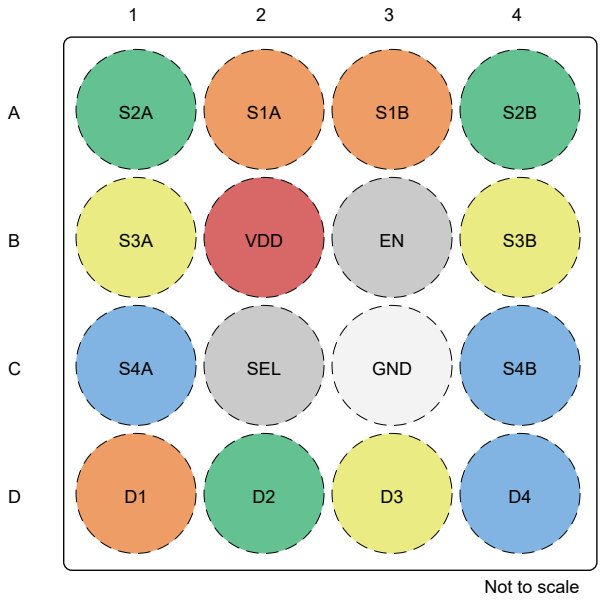


图 5-1. WCSP Package 16-Pin Top View

Pin Functions

PIN		TYPE(1)	DESCRIPTION(2)
NAME	NO.		
S2A	A1	I/O	Source pin 2A. Can be an input or output.
S1A	A2	I/O	Source pin 1A. Can be an input or output.
S1B	A3	I/O	Source pin 1B. Can be an input or output.
S2B	A4	I/O	Source pin 2B. Can be an input or output.
S3A	B1	I/O	Source pin 3A. Can be an input or output.
VDD	B2	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
EN	B3	I	Active high enable: Internal 6 MΩ pull-down to GND.
S3B	B4	I/O	Source pin 3B. Can be an input or output.
S4A	C1	I/O	Source pin 4A. Can be an input or output.
SEL	C2	I	Select pin: controls state of switches according to 表 8-1. Internal 6 MΩ pull-down to GND.
GND	C3	P	Ground (0 V) reference
S4B	C4	I/O	Source pin 4B. Can be an input or output.
D1	D1	I/O	Drain pin 1. Can be an input or output.
D2	D2	I/O	Drain pin 2. Can be an input or output.
D3	D3	I/O	Drain pin 3. Can be an input or output.
D4	D4	I/O	Drain pin 4. Can be an input or output.

(1) I = input, O = output, I/O = input and output, P = power.

(2) Refer to 节 8.4 for what to do with unused pins.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	– 0.5	4	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SEL or EN)	– 0.5	4	V
I_{SEL} or I_{EN}	Logic control input pin current (SEL or EN)	– 30	30	mA
V_S or V_D	Source or drain pin voltage	– 0.5	4	V
I_S or $I_{D\ (CONT)}$	Source and drain pin continuous current: (SxA, SxB, Dx)	– 20	20	mA
T_{stg}	Storage temperature	– 65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{DD}	Supply voltage	1.08	3.6	V
V_S or V_D	Signal path input/output voltage (source or drain pin), $V_{DD} \geqslant 1.08$ V(1)	0	V_{DD} x 2	V
V_{S_off} or V_{D_off}	Signal path input/output voltage (source or drain pin), V_{DD} =0 V	0	3.6	V
V_{SEL} or V_{EN}	Logic control input voltage (EN, SEL)	0	3.6	V
T_A	Ambient temperature	– 40	125	ºC

(1) Device input/output can operate up to V_{DD} x 2, with a maximum input/output voltage of 3.6 V.

6.4 Thermal Information

THERMAL METRIC(1)		DEVICE YCJ (WCSP) 16 PINS	UNIT
$R_{\theta\ JA}$	Junction-to-ambient thermal resistance	89.4	°C/W
$R_{\theta\ JC(top)}$	Junction-to-case (top) thermal resistance	21.4	°C/W
$R_{\theta\ JB}$	Junction-to-board thermal resistance	0.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	21.3	°C/W
$R_{\theta\ JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

V_{DD} = 1.08 V to 3.6 V, GND = 0V, T_A = –40°C to +125°C
Typical values are at V_{DD} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_{DD}	Active supply current	V_{SEL} = 0 V, 1.2V or V_{DD} V_S = 0 V to 3.6 V T_A = –40°C to +85°C		7	10	µA
I_{DD}	Active supply current	V_{SEL} = 0 V, 1.2V or V_{DD} V_S = 0 V to 3.6 V T_A = –40°C to +125°C		7	14	µA
DC CHARACTERISTICS						
R_{ON}	ON-state resistance	V_S = 0 V to V_{DD} I_{SD} = 8 mA		1.7	6.5	Ω
R_{ON}	On-resistance	V_S = 0 V to V_{DD} * 2 $V_{S(max)}$ = 3.6 V I_{SD} = 8 mA		3	8	Ω
ΔR_{ON}	On-resistance match between channels	V_S = V_{DD} I_{SD} = 8 mA		0.1	0.4	Ω
$R_{ON(FLAT)}$	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 8 mA		1	3.5	Ω
I_{POFF}	Powered-off I/O pin leakage current	V_{DD} = 0 V V_S = 0 V to 3.6 V V_D = 0 V	–2	0.01	2	µA
$I_{S(OFF)}$ $I_{D(OFF)}$	OFF leakage current	Switch Off V_D = 0.8*V_{DD} / 0.2*V_{DD} V_S = 0.2*V_{DD} / 0.8*V_{DD} T_A = –40°C to +85°C	–10	0.01	10	nA
$I_{S(OFF)}$ $I_{D(OFF)}$	OFF leakage current	Switch Off V_D = 0.8*V_{DD} / 0.2*V_{DD} V_S = 0.2*V_{DD} / 0.8*V_{DD} T_A = –40°C to +125°C	–100	0.01	100	nA
$I_{D(ON)}$ $I_{S(ON)}$	ON leakage current	Switch On V_D = 0.8 x V_{DD} / 0.2 x V_{DD}, S pins floating or V_S = 0.8 x V_{DD} / 0.2 x V_{DD}, D pins floating T_A = –40°C to +85°C	–10	0.01	10	nA
$I_{D(ON)}$ $I_{S(ON)}$	ON leakage current	Switch On V_D = 0.8*V_{DD} / 0.2*V_{DD}, S pins floating or V_S = 0.8*V_{DD} / 0.2*V_{DD}, D pins floating T_A = –40°C to +125°C	–160	0.01	160	nA
LOGIC INPUTS						
V_{IH}	Input logic high		0.8		3.6	V
V_{IL}	Input logic low		0		0.45	V
I_{IH}	Input high leakage current	V_{SEL} = 1.8 V, V_{DD}		0.5	2.5	µA
I_{IL}	Input low leakage current	V_{SEL} = 0 V	–1	0.1		µA
R_{PD}	Internal pull-down resistor on logic pins			6		MΩ
C_I	Logic input capacitance	V_{SEL} = 0 V, 1.8 V or V_{DD} f = 1 MHz		3		pF

6.6 Dynamic Characteristics

V_{DD} = 1.08 V to 3.6 V, GND = 0V, T_A = –40°C to +125°C
Typical values are at V_{DD} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
C_{OFF}	Source and drain off capacitance	V_S = 2.5 V V_{SEL}= 0 V f = 1 MHz	Switch OFF		3.5		pF
C_{ON}	Source and drain on capacitance	V_S = 2.5 V V_{SEL}= 0 V f = 1 MHz	Switch ON		10		pF
Q_C	Charge Injection	V_S = V_{DD}/2 R_S = 0 Ω, C_L =1 nF	Switch ON		5		pC
O_{ISO}	Off isolation	R_L = 50 Ω f = 100 kHz	Switch OFF		–95		dB
		R_L = 50 Ω f = 1 MHz	Switch OFF		–70		dB
X_{TALK}	Channel to Channel crosstalk	R_L = 50 Ω f = 100 kHz	Switch ON		–90		dB
BW	Bandwidth	R_L = 50 Ω	Switch ON		1.8		GHz
I_{LOSS}	Insertion loss	R_L = 50 Ω f = 1 MHz	Switch ON		–0.15		dB

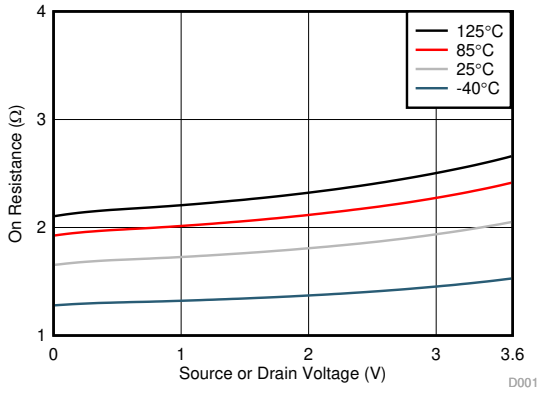
6.7 Timing Requirements

V_{DD} = 1.08 V to 3.6 V, GND = 0V, T_A = –40°C to +125°C
Typical values are at V_{DD} = 3.3 V, T_A = 25°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{TRAN}	Transition time from control input	V_{DD} = 1.8 V to 3.6 V V_S = V_{DD} R_L = 200 Ω, C_L = 15pF		35	80	ns
t_{TRAN}	Transition time from control input	V_{DD} < 1.8 V V_S = V_{DD} R_L = 200 Ω, C_L = 15pF		40	115	ns
$t_{ON(EN)}$	Device turn on time from enable pin	V_S = V_{DD} R_L = 200 Ω, C_L = 15pF		55	130	ns
$t_{OFF(EN)}$	Device turn off time from enable pin	V_S = V_{DD} R_L = 200 Ω, C_L = 15pF		30	60	ns
$t_{ON(VDD)}$	Device turn on time (V_{DD} to output)	V_S = V_{DD} V_{DD} rise time = 1us R_L = 200 Ω, C_L = 15pF		300	990	µs
$t_{OFF(VDD)}$	Device turn off time (V_{DD} to output)	V_S = V_{DD} V_{DD} fall time = 1us R_L = 200 Ω, C_L = 15pF		1	12	µs
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15pF	1			ns
$t_{SK(P)}$	Inter - channel skew			6		ps
t_{PD}	Propagation delay			60		ps

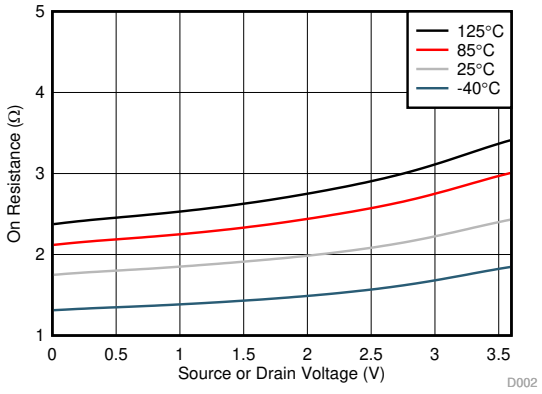
6.8 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted).



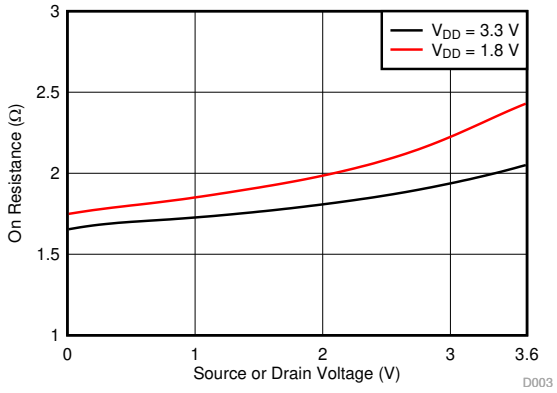
V_{DD} = 3.3 V

图 6-1. On-Resistance vs Temperature



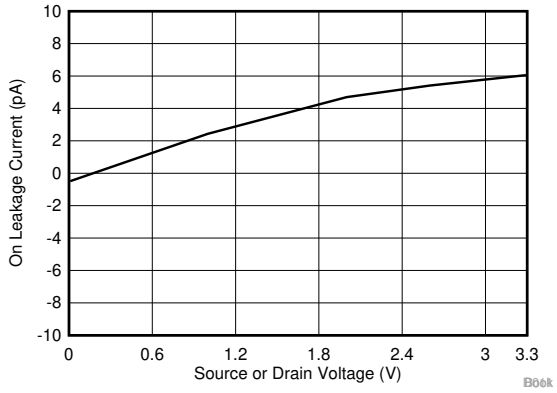
V_{DD} = 1.8 V

图 6-2. On-Resistance vs Temperature



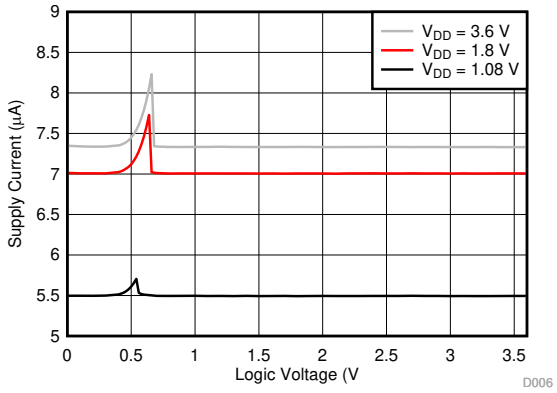
T_A = 25°C

图 6-3. On-Resistance vs Source or Drain Voltage



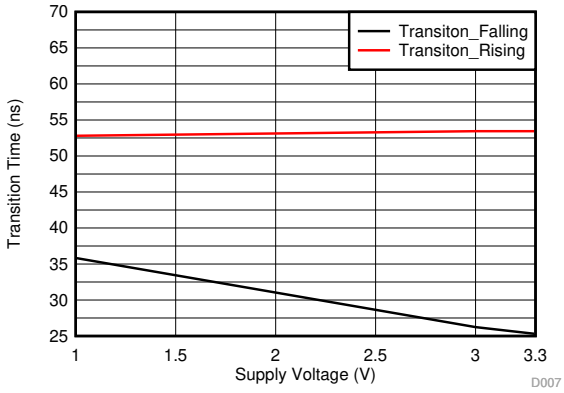
V_{DD} = 3.3 V

图 6-4. On-Leakage vs Source or Drain Voltage



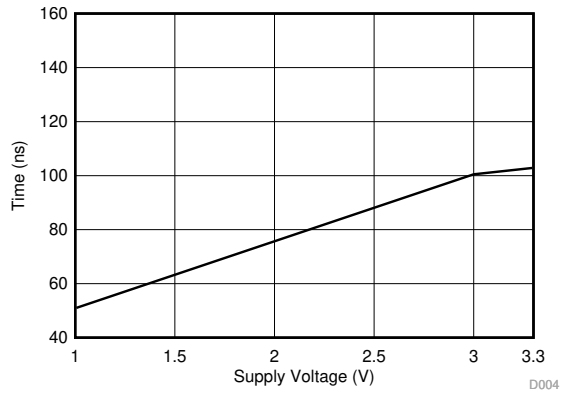
T_A = 25°C

图 6-5. Supply Current vs Logic Voltage



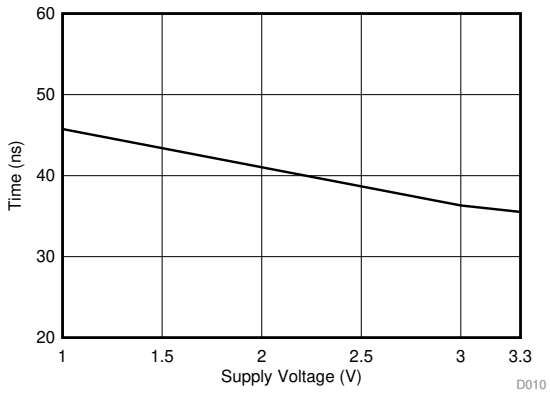
T_A = 25°C

图 6-6. $T_{TRANSITION}$ vs Supply Voltage



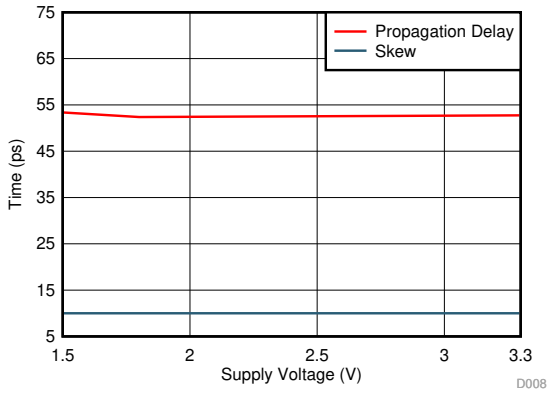
T_A = 25°C

图 6-7. $T_{ON\ (EN)}$ vs Supply Voltage



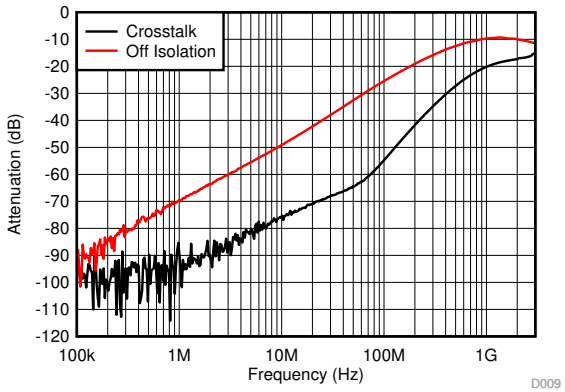
T_A = 25°C

图 6-8. $T_{OFF\ (EN)}$ vs Supply Voltage



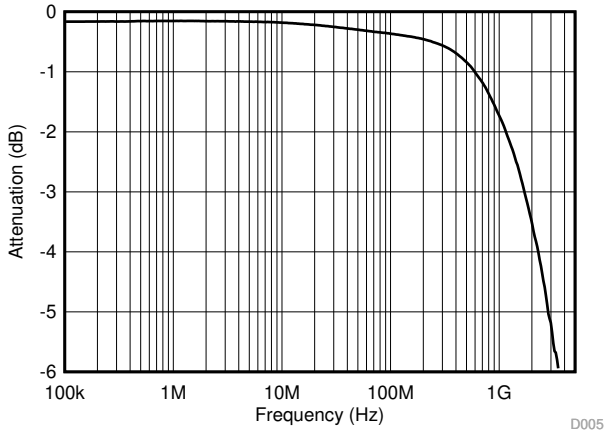
T_A = 25°C

图 6-9. Skew and Propagation Delay vs Supply Voltage



T_A = 25°C

图 6-10. Off Isolation and Crosstalk vs Frequency



T_A = 25°C

图 6-11. On-Response vs Frequency

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 图 7-1. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed as shown below with R_{ON} = V / I_{SD}:

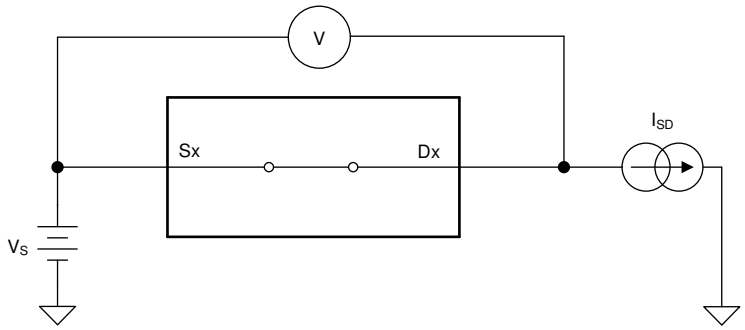


图 7-1. On-Resistance Measurement Setup

7.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S\ (OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D\ (OFF)}$.

The setup used to measure both off-leakage currents is shown in 图 7-2.

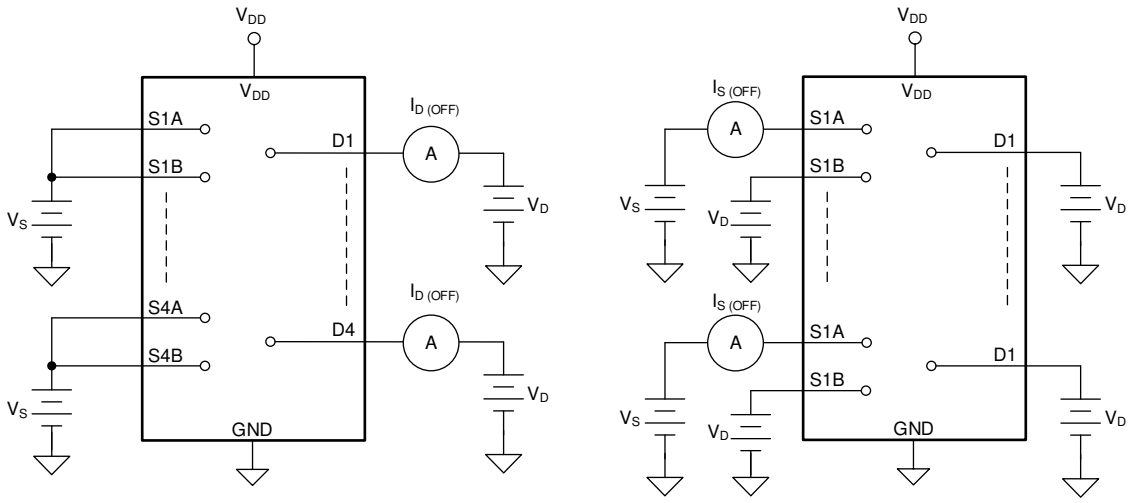


图 7-2. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S\ (ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D\ (ON)}$.

Either the source pin or drain pin is left floating during the measurement. 图 7-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

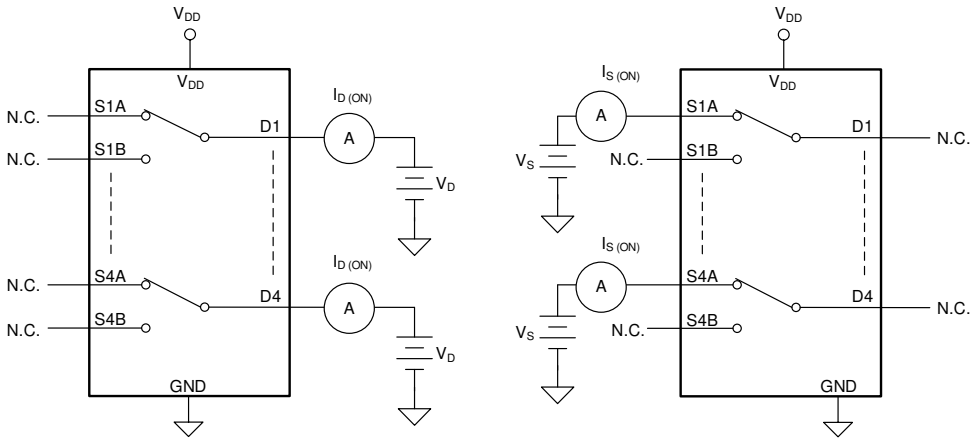


图 7-3. On-Leakage Measurement Setup

7.4 I_{POFF} Leakage Current

I_{POFF} leakage current is defined as the leakage current flowing into or out of the source pin when the device is powered off. This current is denoted by the symbol I_{POFF}.

The setup used to measure both I_{POFF} leakage current is shown in 图 7-4.

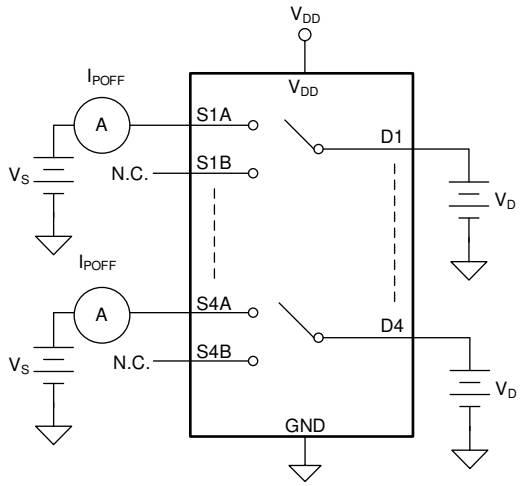


图 7-4. I_{POFF} Leakage Measurement Setup

7.5 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the select signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. The time constant from the load resistance and load capacitance can be added to the transition time to calculate system level timing. 图 7-5 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

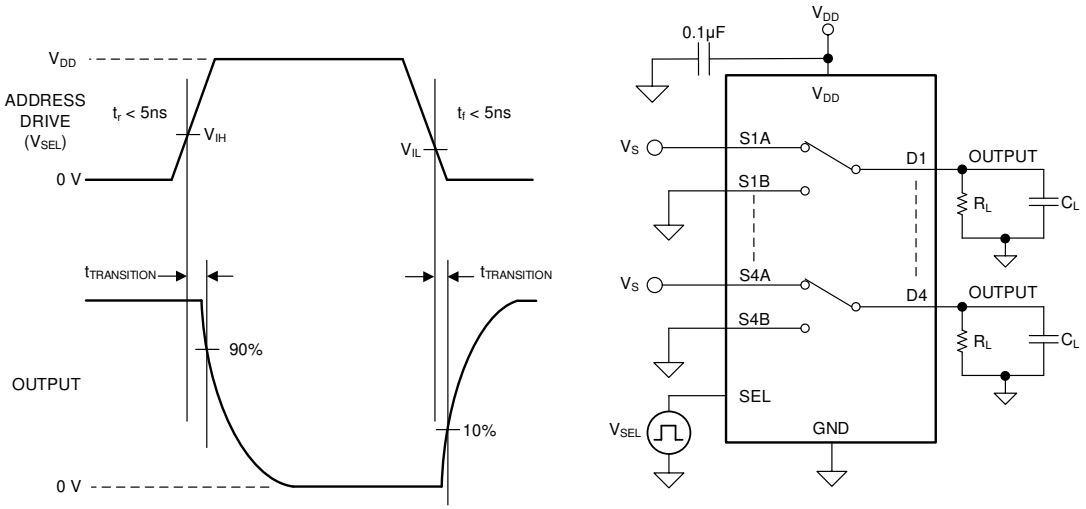


图 7-5. Transition-Time Measurement Setup

7.6 $t_{ON\ (EN)}$ and $t_{OFF\ (EN)}$ Time

The $t_{ON\ (EN)}$ time is defined as the time taken by the output of the device to rise to 90% after the enable has fallen past the logic threshold. The 90% measurement is used to provide the timing of the device being enabled in the system. 图 7-6 shows the setup used to measure the enable time, denoted by the symbol $t_{ON\ (EN)}$.

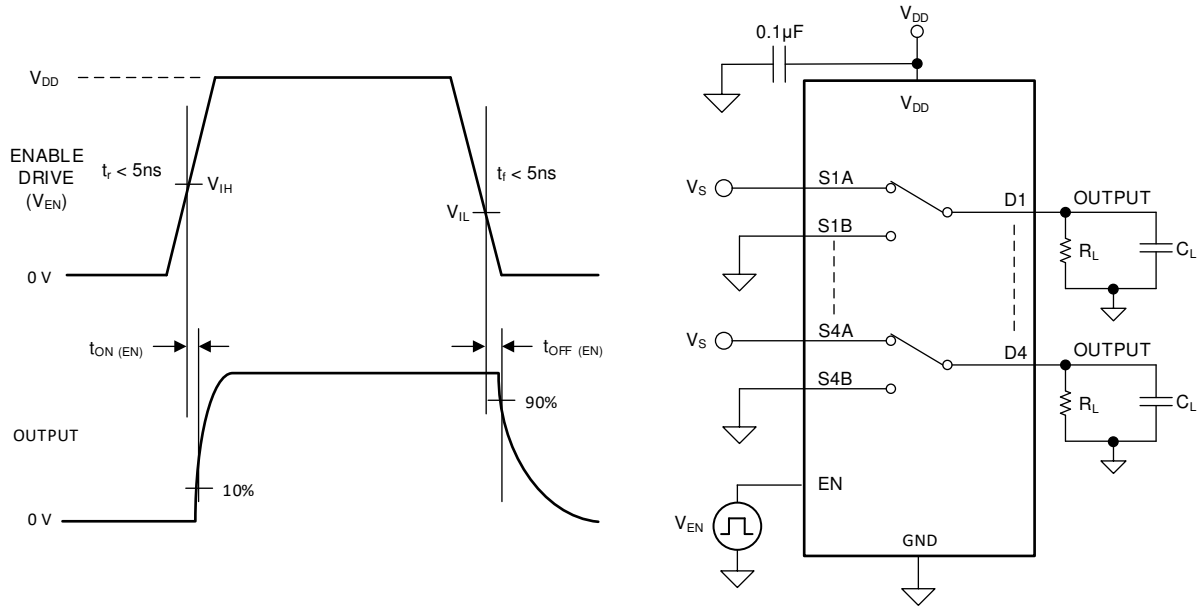


图 7-6. $t_{ON\ (EN)}$ and $t_{OFF\ (EN)}$ Time Measurement Setup

7.7 Break-Before-Make Delay

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 图 7-7 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

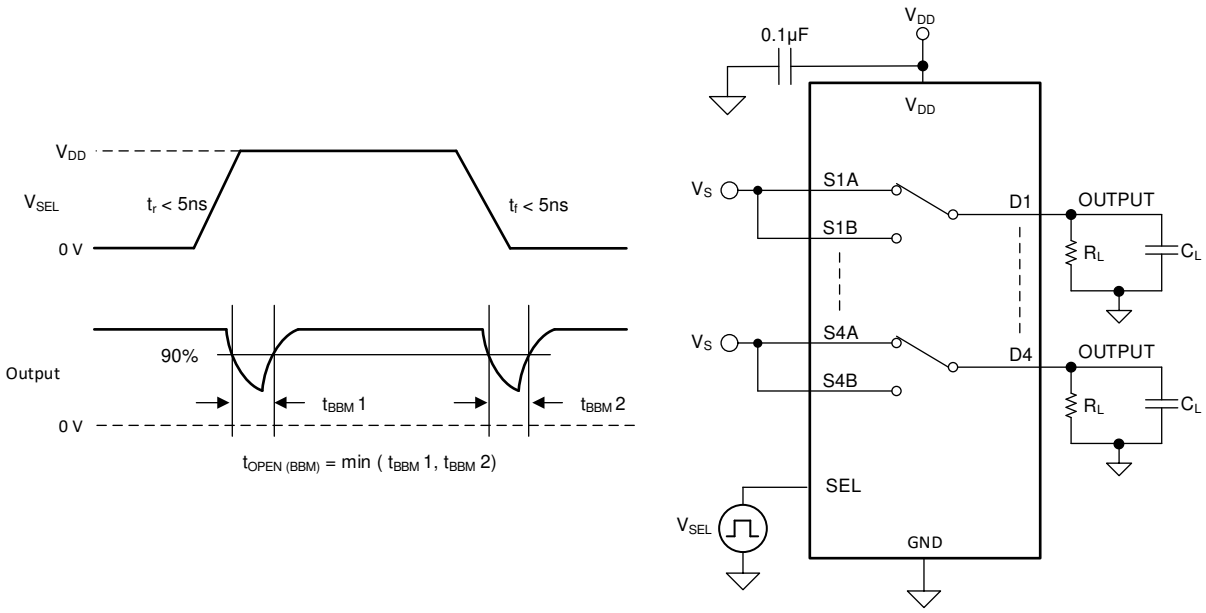


图 7-7. Break-Before-Make Delay Measurement Setup

7.8 Charge Injection

The amount of charge injected into the source or drain of the device during the falling or rising edge of the gate signal is known as charge injection, and is denoted by the symbol Q_C. 图 7-8 shows the setup used to measure charge injection from source (Sx) to drain (Dx).

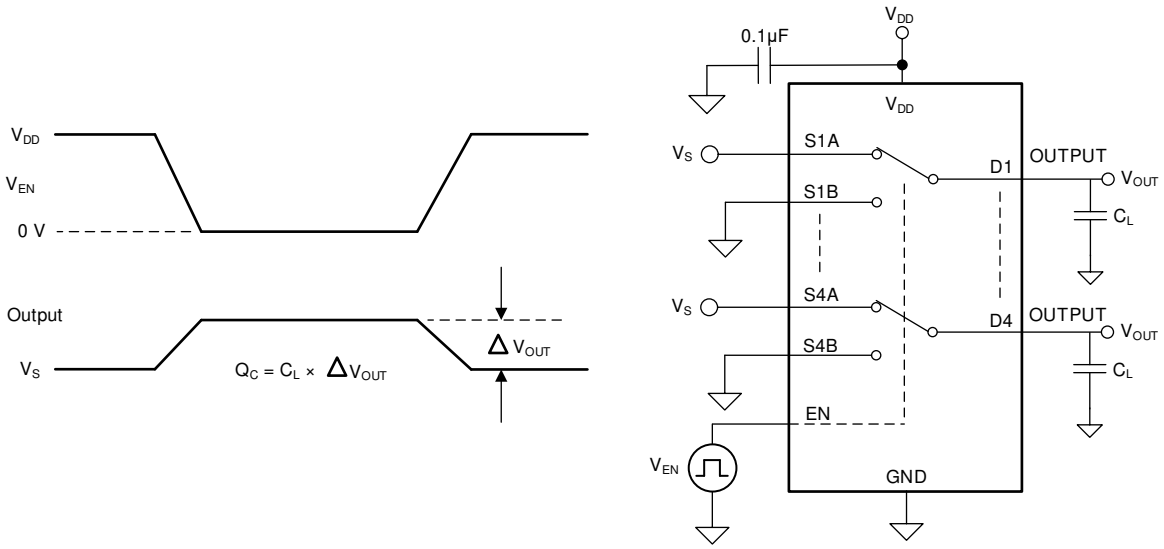


图 7-8. Charge-Injection Measurement Setup

7.9 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. 图 7-9 shows the setup used to measure off isolation. Use off isolation equation to compute off isolation.

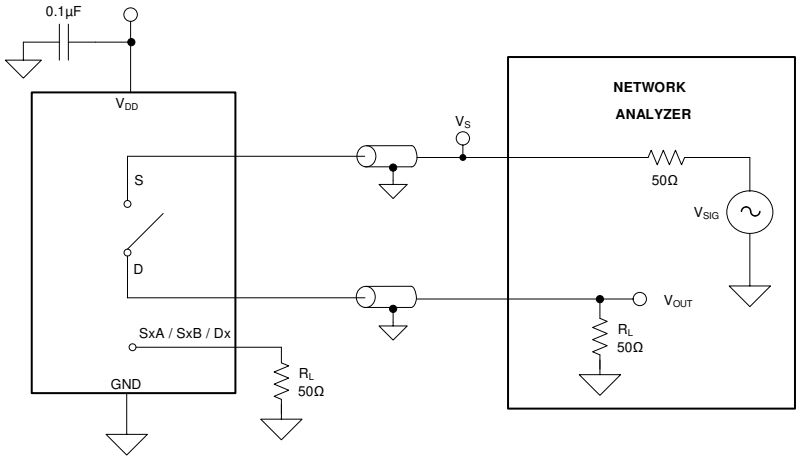


图 7-9. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

7.10 Channel-to-Channel Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (Dx) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. The characteristic impedance, Z_0, for the measurement is 50 Ω. 图 7-10 shows the setup used to measure, and the equation used to compute crosstalk.

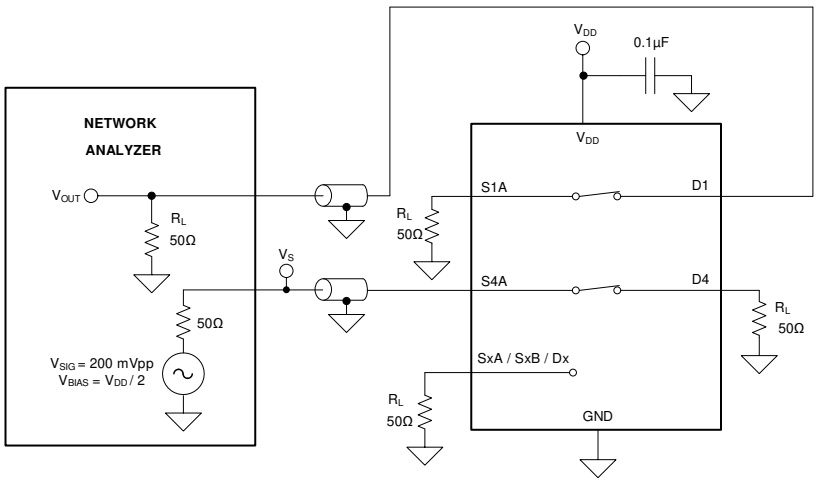


图 7-10. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.11 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the device. The characteristic impedance, Z_0, for the measurement is 50 Ω. 图 7-11 shows the setup used to measure bandwidth.

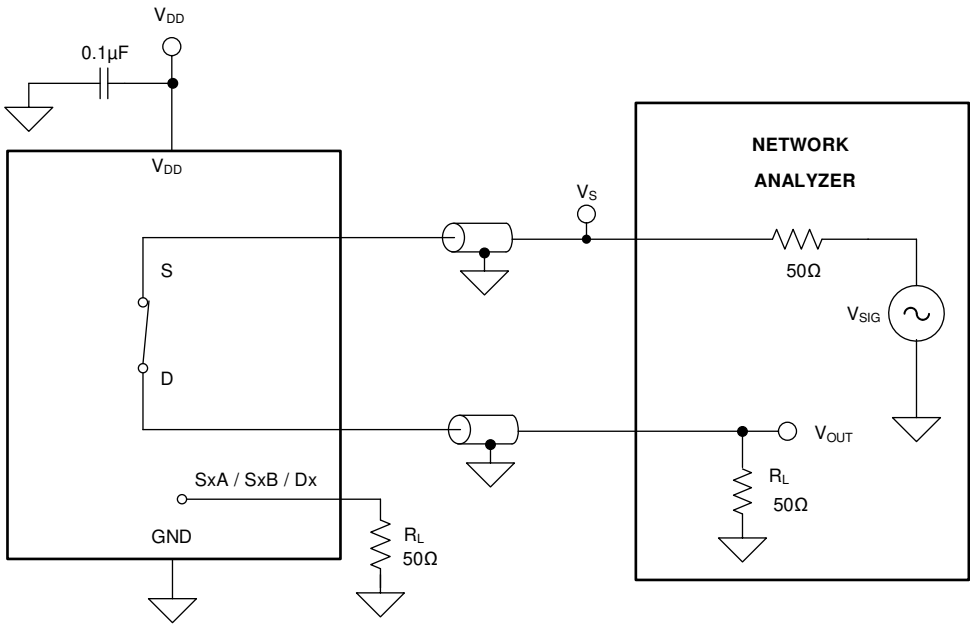


图 7-11. Bandwidth Measurement Setup

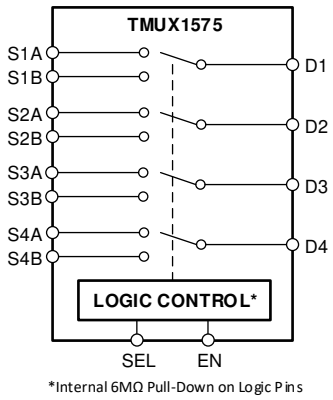
$$Attenuation = 20 \times Log\left(\frac{V_{OUT}}{V_S}\right) \quad (3)$$

8 Detailed Description

8.1 Overview

The TMUX1575 is a high speed 2:1 (SPDT) 4-ch. switch with powered-off protection. Wide operating supply of 1.08 V to 3.6 V allows for use in a wide array of applications from servers and communication equipment to personal electronics. The device supports bidirectional analog and digital signals on the source (SxA, SxB) and drain (Dx) pins. The wide bandwidth of this switch allows little or no attenuation of high-speed signals at the outputs to pass with minimum edge and phase distortion as well as propagation delay.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX1575 conducts equally well from source (SxA, SxB) to drain (Dx) or from drain (Dx) to source (SxA, SxB). Each channel has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Beyond Supply Operation

When the TMUX1575 is powered from 1.08 V to 3.6 V, the valid signal path input and output voltage ranges from GND to V_{DD} x 2, with a maximum input/output voltage of 3.6 V.

Example 1: If the TMUX1575 is powered at 1.2 V, the signal range is 0 V to 2.4 V.

Example 2: If the TMUX1575 is powered at 1.8 V, the signal range is 0 V to 3.6 V.

Example 3: If the TMUX1575 is powered at 3.6 V, the signal range is 0 V to 3.6 V.

Other voltage levels not mentioned in the examples support Beyond Supply Operation as long as the supply voltage falls within the recommended operation conditions of 1.08 V to 3.6 V.

8.3.3 1.2 V Logic Compatible Inputs

The TMUX1575 has 1.2-V logic compatible control inputs. Regardless of the V_{DD} voltage, the control input thresholds remain fixed, allowing a 1.8-V processor GPIO to control the TMUX1575 without the need for an external translator. This saves both space and BOM cost. For more information on 1.2 V and 1.8 V logic implementations, refer to *Simplifying Design with 1.8 V logic Muxes and Switches.*

8.3.4 Powered-off Protection

Powered-off protection up on the signal path of the TMUX1575 provides isolation when the supply voltage is removed (V_{DD} = 0 V). When the TMUX1575 is powered-off, the I/Os of the device remain in a high-Z state. Powered-off protection minimizes system complexity by removing the need for power supply sequencing on the signal path. The device performance remains within the leakage performance mentioned in the Electrical Specifications. For more information on powered-off protection, refer to *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

8.3.5 Fail-Safe Logic

The TMUX1575 has Fail-Safe Logic on the control input pins (SELx) which allows for operation up to 3.6 V, regardless of the state of the supply pin. This feature allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pins of the TMUX1575 to be ramped to 3.6 V while V_{DD} = 0 V. Additionally, the feature enables operation of the TMUX1575 with V_{DD} = 1.08 V while allowing the select pins to interface with a logic level of another device up to 3.6 V.

8.3.6 Integrated Pull-Down Resistors

The TMUX1575 has internal weak pull-down resistors (6 MΩ) to GND to ensure the logic pins are not left floating. This feature integrates external components and reduces system size and cost.

8.4 Device Functional Modes

The enable (EN) pin is an active-high logic pin that controls the connection between the source (SxA, SxB) and drain (Dx) pins of the device. When the enable pin is pulled low, all switches are turned off. When the enable is pulled high, the select pin controls the signal path selection. The select pin (SEL) controls the state of all four channels of the TMUX1575 and determines which source pin is connected to the drain pins. When the select pin is pulled low, the SxA pin conducts to the corresponding Dx pins. When the select pin is pulled high, the SxB pin conducts to the corresponding Dx pins. The TMUX1575 logic pins have internal weak pull-down resistors (6 MΩ) to GND so that it powers-on in a known state.

The TMUX1575 can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or V_{DD} in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (SxA, SxB, or Dx) should be connected to GND.

8.4.1 Truth Tables

表 8-1. TMUX1575 Truth Table

INPUTS		Selected Source Pins Connected To Drain Pins (Dx)
EN	SEL	
1	0	S1A connected to D1 S2A connected to D2 S3A connected to D3 S4A connected to D4
1	1	S1B connected to D1 S2B connected to D2 S3B connected to D3 S4B connected to D4
0	X(1)	Hi-Z (OFF)

(1) X denotes *don't care*.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

Common applications that require the features of the TMUX1575 include multiplexing various protocols from a possessor or MCU such as SPI, JTAG, eMMC, or standard GPIO signals. The TMUX1575 provides superior isolation performance when the device is powered. The added benefit of powered-off protection allows a system to minimize complexity by eliminating the need for power sequencing in hot-swap and live insertion applications. The example shown in 图 9-1 illustrates the use of the TMUX1575 to multiplex an SPI bus to multiple flash memory devices.

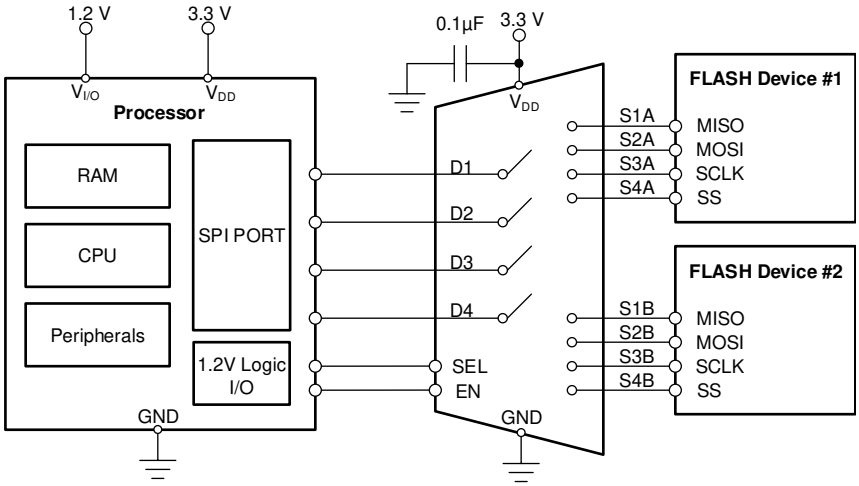


图 9-1. Multiplexing Flash Memory

9.1.1 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETERS	VALUES
Supply (V_{DD})	3.3 V
Input / Output signal range	0 V to 3.3 V
Control logic thresholds	1.2 V compatible

9.1.2 Detailed Design Procedure

The TMUX1575 can be operated without any external components except for the supply decoupling capacitors. The TMUX1575 has internal weak pull-down resistors (6 MΩ) to GND so that it powers-on with the switches in a known state. All inputs signals passing through the switch must fall within the recommend operating conditions of the TMUX1575 including signal range and continuous current. For this design example, with a supply of 3.3 V, the signals can range from 0 V to 3.3 V when the device is powered. This example can also utilize the Powered-off protection feature where the inputs can range from 0 V to 3.6 V when V_{DD} = 0 V. Due to the voltage range and high speed capability, the TMUX1575 example is suitable for use in SPI, JTAG, eMMC, and I2S

applications. Refer to *Enabling SPI-based flash memory expansion by using multiplexers* for more information on using switches and multiplexers for SPI protocol expansion.

10 Power Supply Recommendations

The TMUX1575 operates across a wide supply range of 1.08 V to 3.6 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 μF to 10 μF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

11 Layout

11.1 Layout Guidelines

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self‐inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 图 11-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

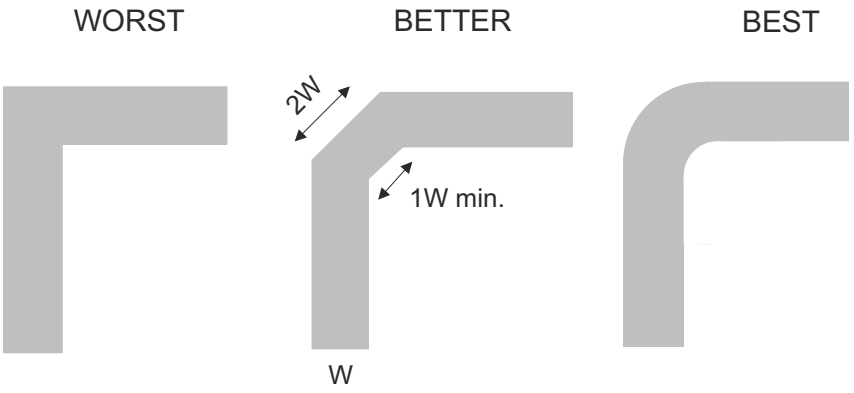


图 11-1. Trace Example

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal’s transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Do not route high speed signal traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or ICs that use or duplicate clock signals.

Avoid stubs on the high-speed signals traces because they cause signal reflections.

Route all high-speed signal traces over continuous GND planes, with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

When working with high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 图 11-2.

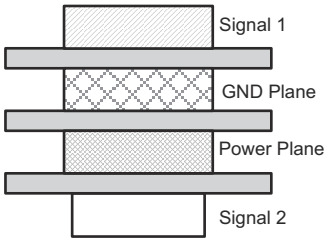


图 11-2. Example Layout

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies. 图 11-3 illustrates an example of a PCB layout with the TMUX1575. Some key considerations are:

Decouple the V_{DD} pin with a 0.1-μF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.

High-speed switches require proper layout and design procedures for optimum performance.

Keep the input lines as short as possible.

Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.

Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

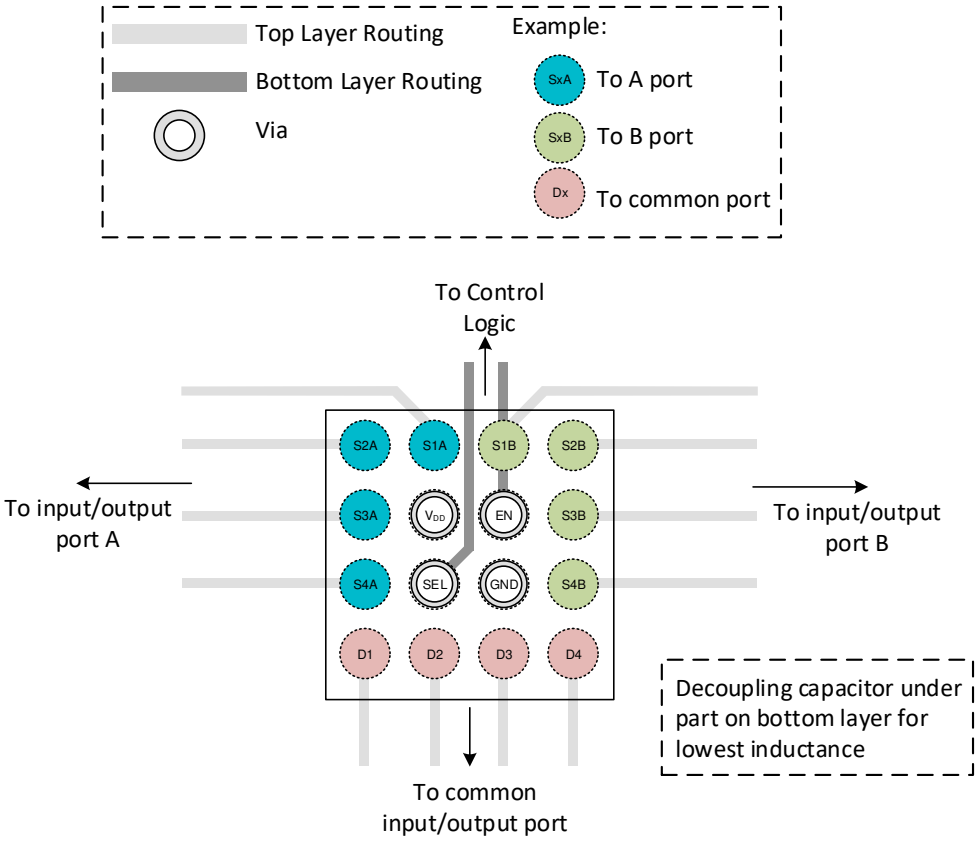


图 11-3. Example Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.

Texas Instruments, *Enabling SPI-based flash memory expansion by using multiplexers*.

Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.

Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.

Texas Instruments, *High-Speed Interface Layout Guidelines*.

Texas Instruments, *High-Speed Layout Guidelines*.

Texas Instruments, *QFN/SON PCB Attachment*.

Texas Instruments, *Quad Flatpack No-Lead Logic Packages*.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

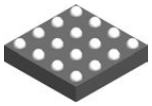
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

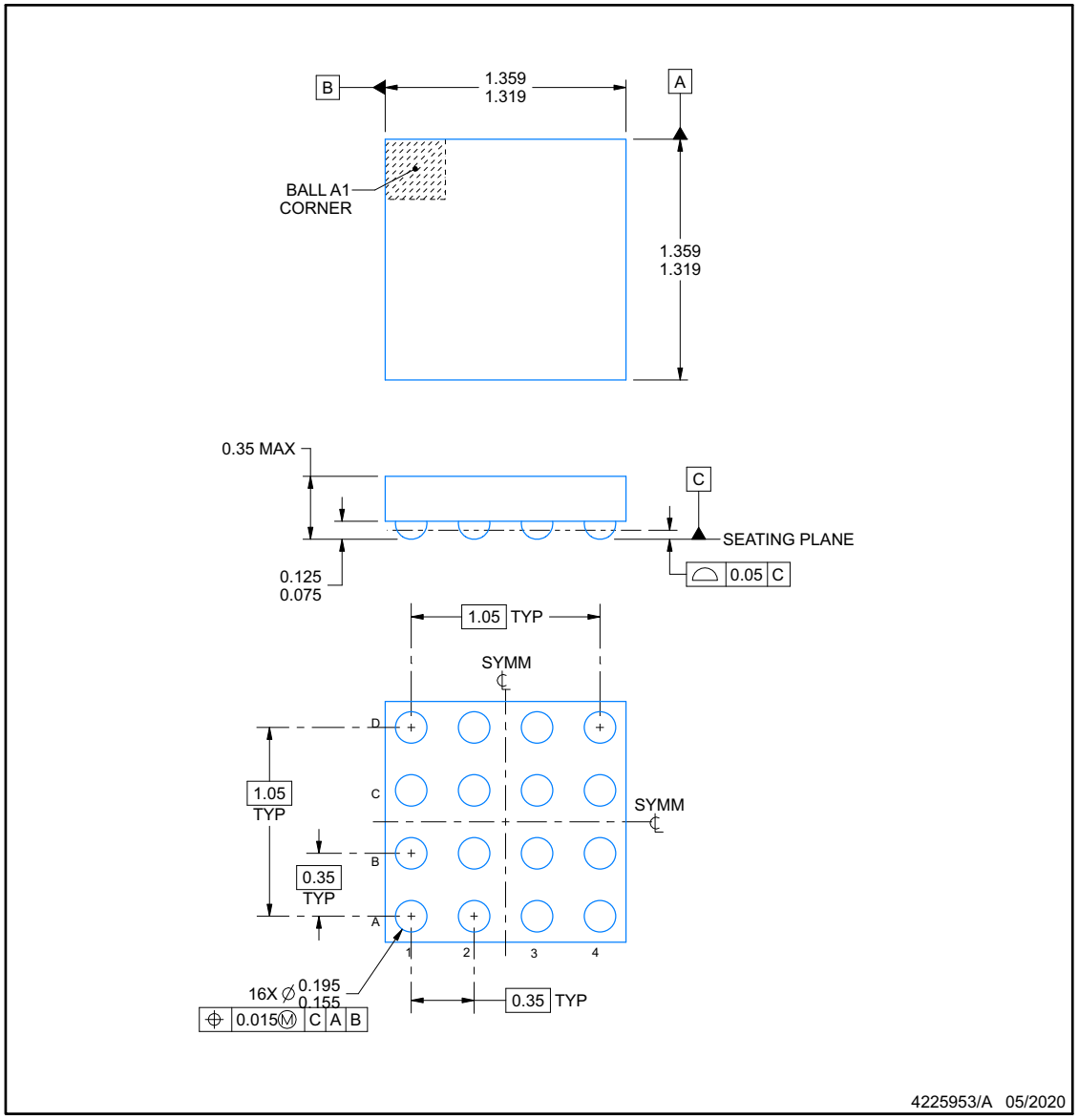


PACKAGE OUTLINE

YCJ0016-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

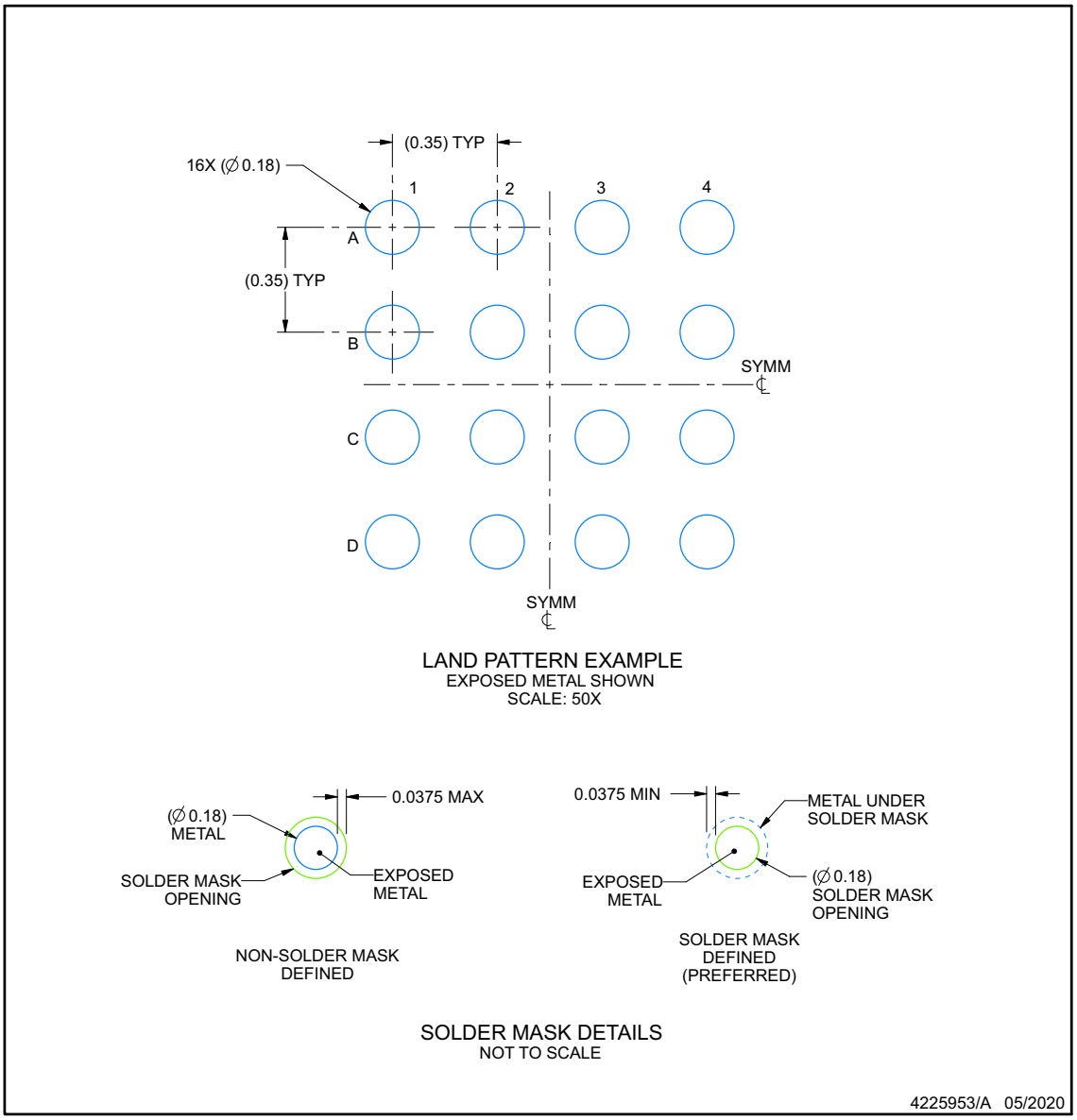
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YCJ0016-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



NOTES: (continued)

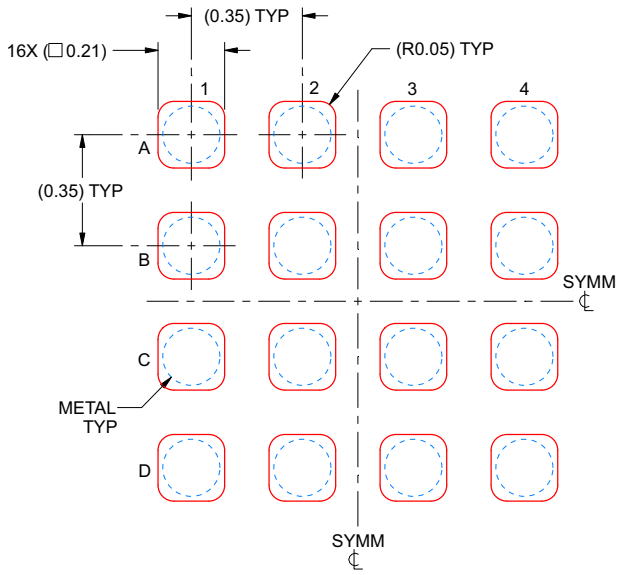
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCJ0016-C01

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4225953/A 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX1575YCJR	ACTIVE	DSBGA	YCJ	16	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	1575	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

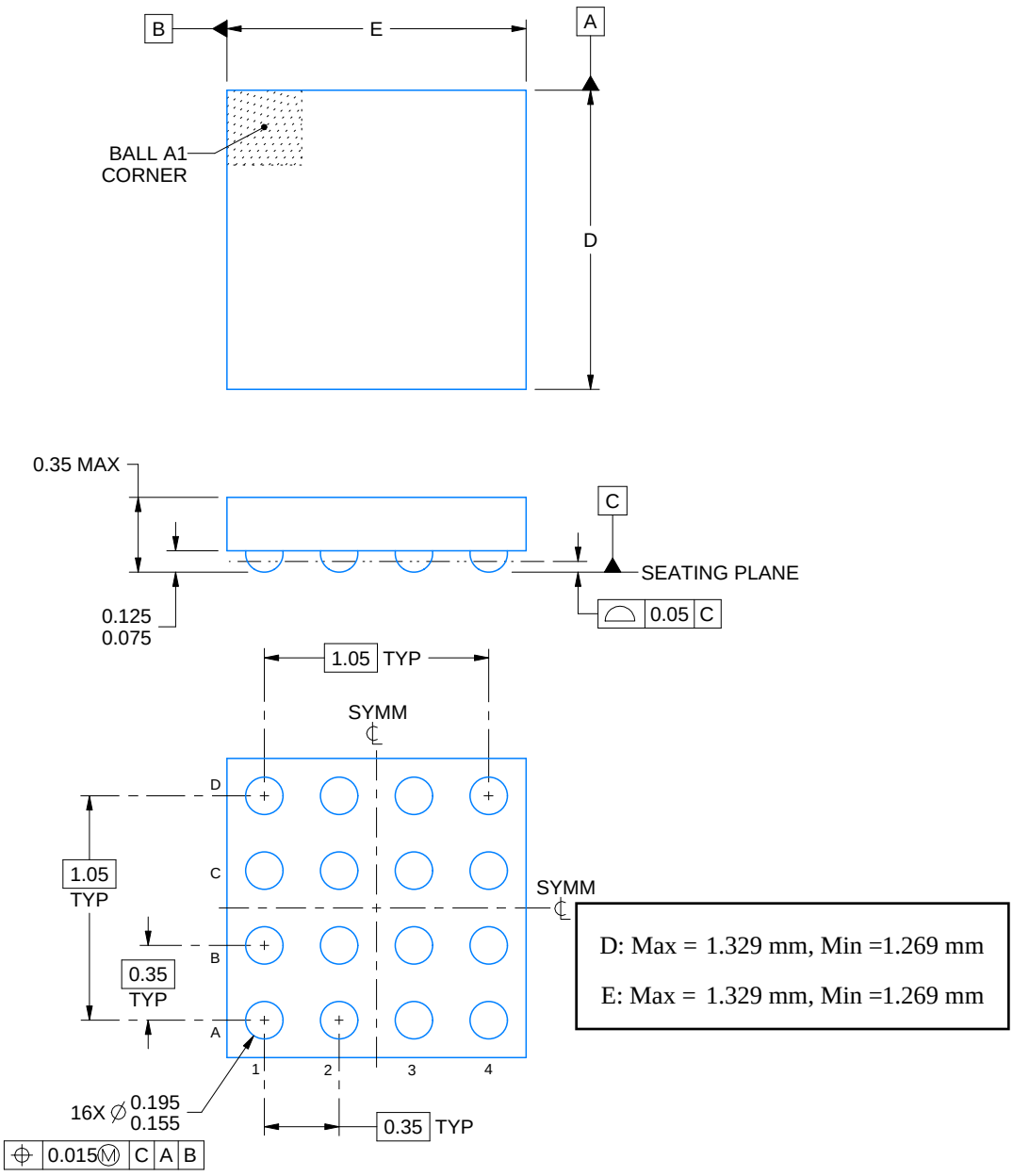
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

YCJ0016

PACKAGE OUTLINE

DSBGA - 0.35 mm max height

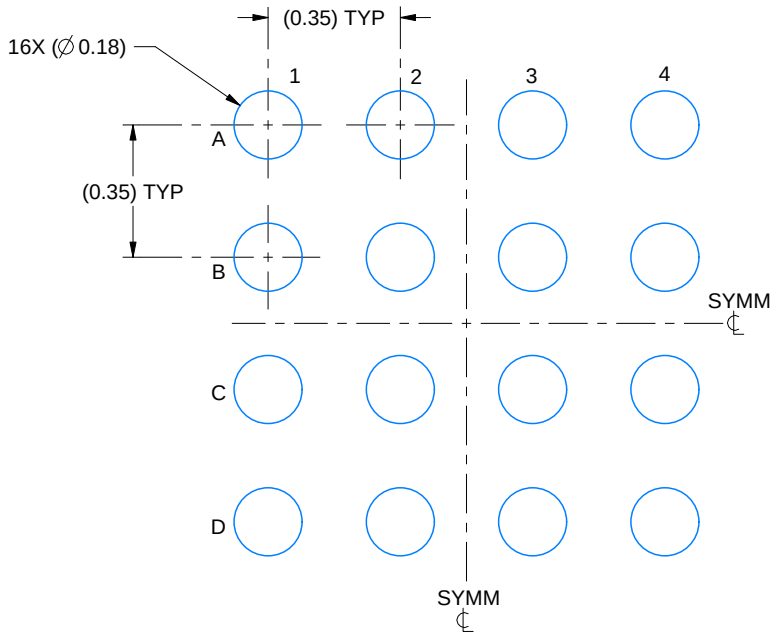
DIE SIZE BALL GRID ARRAY



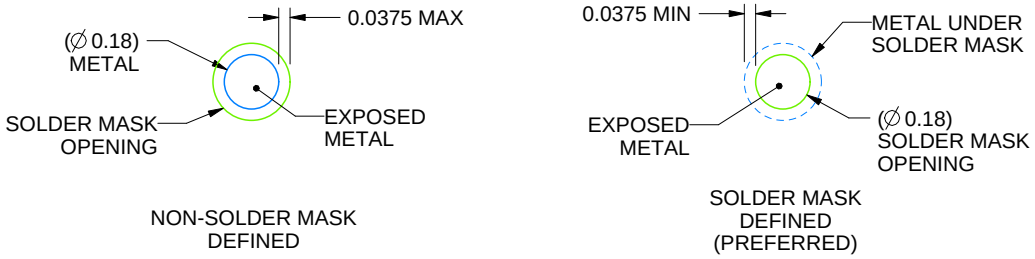
4226577/A 02/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X



SOLDER MASK DETAILS
NOT TO SCALE

4226577/A 02/2021

NOTES: (continued)

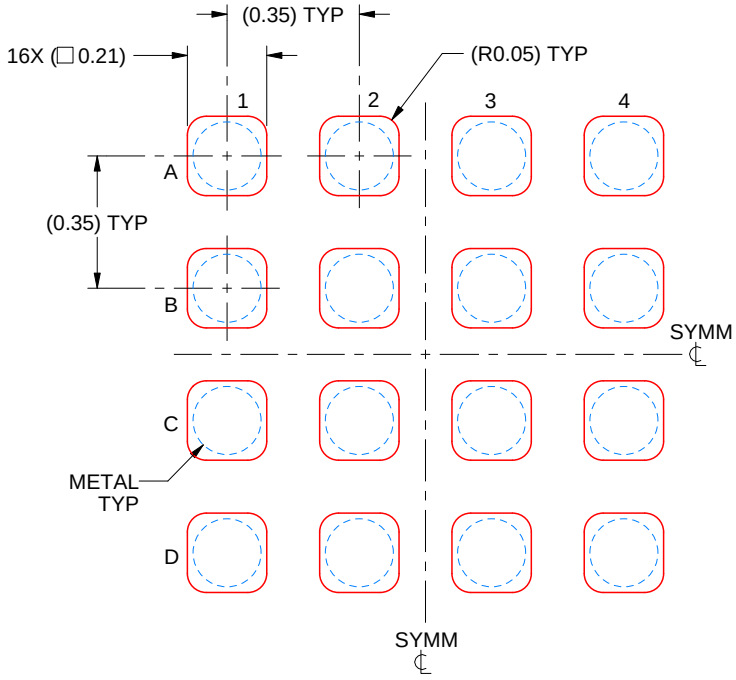
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YCJ0016

DSBGA - 0.35 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

4226577/A 02/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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