TEXAS INSTRUMENTS

**TMDS1204**

ZHCSQV9A – AUGUST 2022 – REVISED APRIL 2024

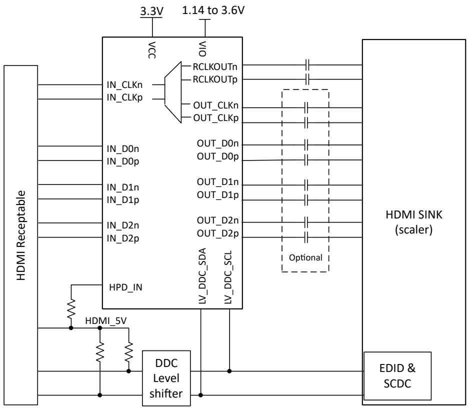
# TMDS1204 12Gbps 直流或交流耦合型 TMDS® 和 FRL HDMI™ 混合转接驱动器

## 1 特性

- 支持高达 12Gbps HDMI 2.1 数据速率的交流耦合或直流耦合输入和输出
  - 向后兼容 HDMI 1.4b 和 HDMI 2.0b
  - HDMI 2.1 固定速率链路 (FRL) 为 3Gbps、6Gbps、8Gbps、10Gbps 和 12Gbps
  - 支持 HDMI 2.1 三通道和四通道 FRL
- 已针对 HDMI 接收器应用进行优化
- 6GHz 时高达 12dB 的自适应和固定均衡器
- $I^2C$ 或引脚搭接可编程
- 集成的 HPD 电平转换器同时支持 1.8V 和 3.3V LVCMOS 电平
- 主通道上全通道交换
- 集成扇出缓冲器，适用于需要单独时钟和数据路径的应用
- 信号检测输出指示器
- 用于链路配置的数字显示控制 (DDC) 监控功能
- 低功耗：
  - 12G FRL 四通道有源限制：575mW
  - 12G FRL 四通道有源线性：220mW
  - 断电：0.6mW
- 可用于商业级和工业级温度范围
- 单个 3.3V 电源
- 40 引脚 0.4mm 间距 4mm × 6mm WQFN 封装

## 2 应用

- 笔记本电脑和台式机
- 电视
- 家庭影院和娱乐系统
- 游戏系统
- 扩展坞
- 专业音频、视频和标牌



简化版原理图

## 3 说明

TMDS1204 是一款 HDMI 2.1 转接驱动器，支持高达 12Gbps 的数据速率，向后兼容 HDMI 1.4b 和 HDMI 2.0b。高速差分输入和输出可以是交流耦合或直流耦合，支持将 TMDS1204 用作 DP++ 转 HDMI 电平转换器或 HDMI 转接驱动器。TMDS1204 可支持 3Gbps、6Gbps、8Gbps、10Gbps 和 12Gbps 的三通道和四通道 HDMI 2.1 FRL。

TMDS1204 是一款混合转接驱动器，同时支持源端和接收端应用。混合转接驱动器可用作线性转接驱动器，也可用作限幅转接驱动器。配置为限幅转接驱动器时，TMDS1204 的差分输出电压电平独立于图形处理单元 (GPU) 的输出电平，从而确保插座的 HDMI 电平符合要求。限幅转接驱动器模式推荐用于 HDMI 源端应用。配置为线性转接驱动器时，TMDS1204 的差分输出电平是 GPU 输出电平的线性函数，从而支持将 TMDS1204 用于透明呈现链路训练或用作通道缩短器。建议将线性转接驱动器模式用于 HDMI 接收端应用。

TMDS1204 有一个集成的 HPD 电平转换器，此 HPD 电平转换器将 5V HPD 信号转换为 1.8V 或 3.3V。电平转换器输出还可以配置为推挽式或开漏式。集成电平转换器后，无需分立式解决方案，因此节省了系统成本。

TMDS1204 支持 3.3V $V_{CC}$ 单电源轨，可用于商业级温度范围 (TMDS1204) 和工业级温度范围 (TMDS1204I)。

器件信息

| 器件型号(1) | 温度 | 封装 |
|---|---|---|
| TMDS1204 | Ta = 0°C 至 70°C | RNQ（WQFN，40） |
| TMDS1204I | Ta = -40°C 至 85°C | |

(1) 有关更多信息，请参阅节 11。

English Data Sheet: SLLSF57

## Table of Contents

# 4 Pin Configuration and Functions

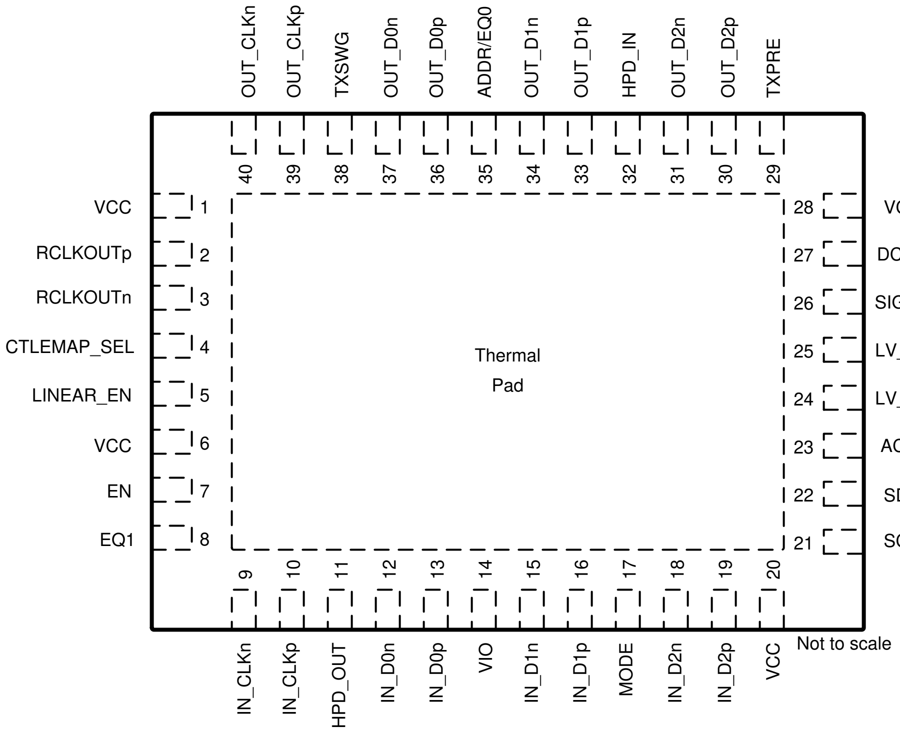


图 4-1. RNQ Package, 40-Pin WQFN (Top View)

表 4-1. Pin Functions

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| VCC | 1 | P | 3.3V power supply |
| RCLKOUTp | 2 | O | HDMI 1.4/2.0 clock differential positive output when not operating in HDMI 2.1 FRL mode with Fan-out buffer feature enabled. External AC coupling required. If not used, then this pin can be left unconnected. |
| RCLKOUTn | 3 | O | HDMI 1.4/2.0 clock differential negative output when not operating in HDM I2.1 FRL mode with Fan-out buffer feature enabled. External AC coupling required. If not used, then this pin can be left unconnected. |
| CTLEMAP_SEL | 4 | I<br>4 Level<br>(PU/PD) | CTLE Map select. When TMDS1204 is configured in pin-strap mode, this pin selects the CTLE Map used. 表 7-8 provides more details. Also in pin-strap this pin will control whether or not AEQ is enabled. 表 7-9 provides more details. In I$^2$C mode, CTLE Map and AEQ enable is determined by registers. |
| LINEAR_EN | 5 | I<br>4-Level<br>(PU/PD) | In pin-strap mode, selects whether TMDS1204 operates in linear or limited redriver mode. 表 7-5 provides more details. |
| VCC | 6 | P | 3.3V power supply |
| EN | 7 | I<br>2-Level (PU) | When low, TMDS1204 will be held in reset. The IN_D[2:0], IN_CLK, OUT_D[2:0] and OUT_CLK pins will be held in high impedance while EN is low. On rising edge of EN, device will sample four-level inputs and function based on the sampled state of the pins. This pin has a internal 250 k pull-up to VIO. |

### 表 4-1. Pin Functions （续）

| PIN | | TYPE[(1)] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| EQ1 | 8 | I<br>4 Level<br>(PU/PD) | EQ1 Pin Setting when TMDS1204 is configured for pin strap mode; Works in conjunction with EQ0; 表 7-6 provides the settings. In $I^2C$ mode, EQ settings are controlled through registers. |
| IN_CLKn | 9 | I | Clock differential negative input. |
| IN_CLKp | 10 | I | Clock differential positive input. |
| HPD_OUT | 11 | O | Hot plug detect output to source side. If not used, then this pin can be left floating. |
| IN_D0n | 12 | I | Channel 0 differential negative input. |
| IN_D0p | 13 | I | Channel 0 differential positive input. |
| VIO | 14 | P | Voltage supply for I/Os. 表 7-2 provides more information. |
| IN_D1n | 15 | I | Channel 1 differential negative input. |
| IN_D1p | 16 | I | Channel 1 differential positive input. |
| MODE | 17 | I<br>4 Level<br>(PU/PD) | Mode control pin. Selects between pin-strap and $I^2C$ mode. For more information, refer to 节 7.3.1. |
| IN_D2n | 18 | I | Channel 2 differential negative input. |
| IN_D2p | 19 | I | Channel 2 differential positive input. |
| VCC | 20 | P | 3.3V power supply. |
| SCL/CFG0 | 21 | I | $I^2C$ Clock/CFG0: when TMDS1204 is configured for $I^2C$ mode, this pin will function as the $I^2C$ clock. Otherwise, this pin will function as CFG0. 表 7-18 provides more details. |
| SDA/CFG1 | 22 | I/O | $I^2C$ Data / CFG1: When TMDS1204 is configured for $I^2C$ mode, this pin will function as the $I^2C$ clock. Otherwise, this pin will function as CFG1. 表 7-19 provides more details. |
| AC_EN | 23 | I<br>2-Level (PD) | In pin-strap mode, selects whether high speed transmitters are externally AC or DC coupled.<br>0: DC-coupled<br>1: AC-coupled |
| LV_DDC_SCL | 24 | I/O | Low voltage side DDC clock line. Internally pulled-up to VIO. |
| LV_DDC_SDA | 25 | I/O | Low voltage side DDC data line. Internally pulled-up to VIO. |
| SIGDET_OUT | 26 | O | SIGDET_OUT. Open drain output asserted low when signal is detected on IN_CLK or IN_D2 when HPD_IN is high. Otherwise signal is de-asserted. When used requires 10k or greater pull-up resistor. |
| DCGAIN | 27 | I<br>4 Level<br>(PU/PD) | DC Gain.<br>"0": −3dB<br>"R": −3dB<br>"F": 0dB<br>"1": +1dB |
| VCC | 28 | P | 3.3V power supply |
| TXPRE | 29 | I<br>4 Level<br>(PU/PD) | TX pre-emphasis control: in pin-strap mode with limited enabled, this pin controls TX EQ. In pin-strap with linear and AEQ enabled, this pin will adjust the adapted value. 表 7-15 provides the available TXPRE settings when operating in pin strap mode. In $I^2C$ mode, Tx pre-emphasis is controlled through registers. |
| OUT_D2p | 30 | O | TMDS data 2 differential positive output |
| OUT_D2n | 31 | O | TMDS data 2 differential negative output |
| HPD_IN | 32 | I<br>2-Level (PD) | Hot plug detect input from sink side. This pin has an internal pull-down resistor and is fail-safe. |
| OUT_D1p | 33 | O | TMDS data 1 differential positive output |
| OUT_D1n | 34 | O | TMDS data 1 differential negative output |

### 表 4-1. Pin Functions （续）

| PIN |  | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. |  |  |
| ADDR/EQ0 | 35 | I<br>4 Level<br>(PU/PD) | Address bit for $I^2C$ programming when TMDS1204 is configured for $I^2C$ mode. 表 7-22 provides more details.<br>EQ0 pin setting when TMDS1204 is configured for pin strap mode; works in conjunction with EQ1; 表 7-6 lists the settings. In $I^2C$ mode, EQ settings are controlled through registers. |
| OUT_D0p | 36 | O | TMDS data 0 differential positive output |
| OUT_D0n | 37 | O | TMDS data 0 differential negative output |
| TXSWG | 38 | I<br>4 Level<br>(PU/PD) | TX output swing control: 4 settings. This pin is only used in pin strap mode. 表 7-17 provides the available TX swing settings. In $I^2C$ mode, TX output swing is controlled through registers. |
| OUT_CLKp | 39 | O | TMDS data clock differential positive output |
| OUT_CLKn | 40 | O | TMDS data clock differential negative output |
| Thermal Pad |  | — | Thermal pad. Connect to a solid ground plane. |

(1) I = input, O = output, P = power, G = ground

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ and $V_{IO}$ | -0.5 | 4 | V |
| Input Voltage | Differential Inputs (IN_D[2:0], IN_CLK) | -0.3 | 4 | V |
| Output voltage | RCLKOUTp/n, HPD_OUT, SIGDET_OUT outputs | –0.3 | 4 | V |
| Output voltage | Differential outputs (OUT_D[2:0], OUT_CLK) | –0.3 | 4 | V |
| Control pins | LV_DDC_SDA, LV_DDC_SCL, SCL/CFG0, SDA/CFG1, MODE, CLTEMAP_SEL, TXSWG, TXPRE, EQ1, ADDR/EQ0, EN, AC_EN, LINEAR_EN, DCGAIN | –0.5 | 4 | V |
| | HPD_IN | –0.5 | 6 | V |
| $T_J$ | TMDS1204 Junction temperature | | 105 | °C |
| $T_J$ | TMDS1204I Junction temperature | | 125 | °C |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Rating* may cause permanent damage to the device. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under the *Recommended Operating Condition*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

## 5.2 ESD and Latch-Up Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±4000 | V |
| | | Charged-device model (CDM), per JEDEC specification JS-002(2) | ±1500 | |
| $V_{(Supply)}$ | Supply Test | Supply test, per JESD78F class II(3) | 1.5 x $V_{CC}$ | V |
| $I_{(signal+)}$ | Positive signal pin latch-up | Signal pin test, per JESD78F class II, immunity level A (all signal pins)(3) | +100 | mA |
| $I_{(signal-)}$ | Negative signal pin latch-up | Signal pin test, per JESD78F class II, immunity level A (all signal pins except pin 2 and pin 3)(3) | –100 | mA |
| | | Signal pin test, per JESD78F class II, immunity level B, annex A flow 1F (pin 2 and pin 3 are connected through 10 nF capacitors)(3)(4) | –100 | mA |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) JESD78F at maximum ambient temperature
(4) Per annex A flow 1F, negative pulse immunity on pin 2 and pin 3 is –15 mA without 10 nF series capacitors. Care should be given during ICT to limit test current to less than –15 mA.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage when high-speed RX pins (IN_D[2:0] and IN_CLK) is AC-coupled to a DP++ TX | 3.0 | 3.3 | 3.6 | V |
| $V_{CC}$ | Supply voltage when high-speed RX pins (IN_D[2:0] and IN_CLK) is DC-coupled to a HDMI TX | 3.135 | 3.3 | 3.465 | V |
| $V_{IO}$ | VIO supply when 1.2V LVCMOS level used. | 1.14 | 1.2 | 1.26 | V |
| $V_{IO}$ | VIO supply when 1.8V LVCMOS level used. | 1.7 | 1.8 | 1.9 | V |
| $V_{IO}$ | VIO supply when 3.3V LVCMOS level used. | 3 | 3.3 | 3.6 | V |
| $V_{PSN}$ | Peak to peak Power supply noise on $V_{CC}$ pins (less than 4MHz). | | | 100 | mV |

## 5.3 Recommended Operating Conditions （续）

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CTL3}$ | DC input voltage for SCL/CFG0, SDA/CFG1, MODE, AC_EN, LINEAR_EN, EN, CTLEMAP_SEL, TXSWG, TXPRE, EQ1, ADDR1/EQ0, DCGAIN, LV_DDC_SCL, LV_DDC_SDA | –0.3 | | 3.6 | V |
| $V_{CTL5}$ | DC input voltage for HPD_IN pins | –0.3 | | 5.5 | V |
| $C_{ACRX}$ | Optional external AC-coupling capacitor on IN_Dx and IN_CLK. | 85 | | 253 | nF |
| $C_{ACTX}$ | External AC-coupling capacitor on OUT_Dx and OUT_CLK when AC_EN = H. | 85 | | 253 | nF |
| $T_A$ | TMDS1204 Ambient temperature | 0 | | 70 | °C |
| $T_A$ | TMDS1204I Ambient temperature | –40 | | 85 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | TMDS1204 | UNIT |
|---|---|---|---|
| | | RNQ (WQFN) | |
| | | 40 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 30.9 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 21.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 11.7 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.3 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 11.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 3.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER** | | | | | | |
| $P_{ACTIVE\text{-}H14\text{-}LT\text{-}ARX\text{-}DTX}$ | Power dissipation in HDMI 1.4 3.4Gbps active operation | Pin Strap mode; DR = 3.4Gbps; HPD_IN = H; No de-emphasis/pre-emphasis; Limited redriver mode; DC-coupled TX; AC-coupled RX; 3Gbps CTLE; | | 190 | 265 | mW |
| $P_{ACTIVE\text{-}H20\text{-}LT\text{-}ARX\text{-}DTX}$ | Power dissipation in HDMI 2.0 6Gbps active operation | Pin Strap mode; DR = 6Gbps; HPD_IN = H; No de-emphasis/pre-emphasis; Limited redriver mode; DC-coupled TX; AC-coupled RX; 6Gbps CTLE; | | 215 | 305 | mW |
| $P_{ACTIVE\text{-}FRL\text{-}LT\text{-}DRX\text{-}DTX}$ | Power dissipation in FRL 12Gbps active operation when TX is DC-coupled (AC_EN = L) and RX is DC-coupled; | Pin Strap mode; DR = 12Gbps; HPD_IN = H; TXFFE0; Limited redriver mode; DC-coupled TX; DC-coupled RX to 3.3V Vicm; 12Gbps CTLE; | | 540 | 775 | mW |
| $P_{ACTIVE\text{-}FRL\text{-}LT\text{-}ARX\text{-}ATX}$ | Power dissipation in FRL 12Gbps active operation when TX is AC-coupled (AC_EN = H) | Pin Strap mode; DR = 12Gbps; HPD_IN = H; TXFFE0; Limited redriver mode; AC-coupled TX; AC-coupled RX;12Gbps CTLE; | | 840 | 1220 | mW |
| $P_{ACTIVE\text{-}FRL\text{-}LT\text{-}ARX\text{-}DTX}$ | Power dissipation in FRL 12Gbps active operation when TX is DC-coupled (AC_EN = L) | Pin Strap mode; DR = 12Gbps; HPD_IN = H; TXFFE0; Limited redriver mode; DC-coupled TX; AC-coupled RX; 12Gbps CTLE; | | 575 | 785 | mW |

## 5.5 Electrical Characteristics （续）

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_{ACTIVE\text{-}FRL\text{-}LR\text{-}ARX\text{-}DTX}$ | Power dissipation in FRL 12Gbps active operation when TX is DC-coupled (AC_EN = L) | Pin Strap mode; DR = 12Gbps; HPD_IN = H; Highest linearity setting; Linear redriver mode; DC-coupled TX; AC-coupled RX; 12Gbps CTLE; | | 220 | 310 | mW |
| $P_{ACTIVE\text{-}FRL\text{-}LR\text{-}ARX\text{-}ATX}$ | Power dissipation in FRL 12Gbps active operation when TX is AC-coupled (AC_EN = H) | Pin Strap mode; DR = 12Gbps; HPD_IN = H; Highest linearity setting; Linear redriver mode; AC-coupled TX; AC-coupled RX; 12Gbps CTLE | | 660 | 990 | mW |
| $P_{PD}$ | Power in power-down (HPD_IN = L) | Pin Strap mode; HPD_IN = L; EN = L or H; High-speed outputs are disconnected; | | 0.6 | 2 | mW |
| $P_{SD}$ | Power in standby (HPD_IN = H) but no incoming signal | Pin Strap mode; HPD_IN = H; No incoming signal; EN = H; DC-coupled TX; AC-coupled RX; Limited redriver mode; High-speed outputs are connected; | | 1.0 | 1.85 | mW |
| $I_{VIOQ}$ | VIO quiescent current | HPD_IN = H;VCC = VIO = 3.6V; LV_DDC_SDA/SCL = H; | | | 16 | µA |
| $I_{VIOA}$ | VIO active instantaneous current | VCC = VIO = 3.6V; HPD_IN = H; | | | 1 | mA |
| **2-LEVEL CONTROL PINS (EN, SCL/CFG0, SDA/CFG1, AC_EN)** | | | | | | |
| $V_{IO\_TRSHD}$ | Threshold for selecting between 1.2V LVCMOS / 1.8V LVCMOS | | | 1.5 | | V |
| $V_{IO\_TRSHD}$ | Threshold for selecting between 1.8V LVCMOS / 3.3V LVCMOS | | | 2.5 | | V |
| $V_{IL\_1p2V}$ | Low-level input voltage for SCL/CFG0, SDA/CFG1 | VIO = 1.26V; VCC = 3.0V; | -0.3 | | 0.360 | V |
| $V_{IH\_1p2V}$ | High-level input voltage for SCL/CFG0, SDA/CFG1 | VIO = 1.14V; VCC = 3.6V; | 0.8 | | 3.6 | V |
| $V_{IL\_1p8V}$ | Low-level input voltage for SCL/CFG0, SDA/CFG1 | VIO = 1.9V; VCC = 3.0V; | -0.3 | | 0.57 | V |
| $V_{IH\_1p8V}$ | High-level input voltage for SCL/CFG0, SDA/CFG1 | VIO = 1.7V; VCC = 3.6V; | 1.19 | | 3.6 | V |
| $V_{IL\_3p3V}$ | Low-level input voltage for SCL/CFG0, SDA/CFG1 | VIO = 3.6V; VCC = 3.0V; | -0.3 | | 0.8 | V |
| $V_{IL\_3p3V}$ | Low-level input voltage for AC_EN | VIO = 3.6V; VCC = 3.0V; | -0.3 | | 0.8 | V |
| $V_{IH\_3p3V}$ | High-level input voltage for SCL/CFG0, SDA/CFG1 | VIO = 3.0V; VCC = 3.6V; | 2.2 | | 3.6 | V |
| $V_{IH\_3p3V}$ | High-level input voltage for AC_EN | VIO = 3.0V; VCC = 3.6V; | 2.2 | | 3.6 | V |
| $V_{OL\_1p2V}$ | Low-level output voltage SDA/CFG1 | $V_{CC}$ = 3.0V; VIO = 1.2V; | -0.3 | | 0.3 | V |
| $I_{OL\_1p2V}$ | Low-level output current SDA/CFG1 | $V_{CC}$ = 3.0V; VIO = 1.2V; | 2 | | | mA |
| $V_{OL}$ | Low-level output voltage SDA/CFG1 | $V_{CC}$ = 3.0V; VIO = 1.8V or 3.3V; | -0.3 | | 0.4 | V |
| $I_{OL}$ | Low-level output current SDA/CFG1 | $V_{CC}$ = 3.0V; VIO = 1.8V or 3.3V; | 4 | | | mA |
| $I_{IL\_I2C}$ | Low-level input current SCL/CFG0, SDA/CFG1 | $V_{IN}$ = 0V; VIO = 1.8V or 3.3V; | –1 | | 1 | µA |
| $I_{LEAK}$ | Fail-safe input current for SCL/CFG0, SDA/CFG1 | $V_{IN}$ = 3.6V; VCC = 0V; | –25 | | 25 | µA |
| $V_{IL\_EN}$ | Low-level input voltage for EN pin. | VIO = 1.14V; VCC = 3.3V; | -0.3 | | 0.4 | V |
| $V_{IH\_EN}$ | High-level input voltage for EN pin. | VIO = 3.6V; VCC = 3.3V; | 0.8 | | 3.6 | V |
| $I_{IL}$ | Low-level input current EN | $V_{IN}$ = 0V; VIO = 1.8V or 3.3V; VCC = 3.6V | –20 | | 20 | µA |
| $I_{IL}$ | Low-level input current AC_EN | $V_{IN}$ = 0V; VIO = 1.8V or 3.3V; | –1 | | 1 | µA |
| $I_{IH\_EN}$ | High-level input current for EN | $V_{IN}$ = 3.6V; VIO = 1.8V or 3.3V; | –1 | | 1 | µA |
| $I_{IH\_ACEN}$ | High-level input current for AC_EN | $V_{IN}$ = 3.6V; VIO = 1.8V or 3.3V; | –24 | | 24 | µA |

## 5.5 Electrical Characteristics （续）

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{PU\_EN}$ | Internal Pull-up resistance on EN. | | 125 | 250 | 350 | kΩ |
| $R_{PD\_ACEN}$ | Internal Pull-down resistance on AC_EN | | 125 | 250 | 350 | kΩ |
| $C_{I2C\text{-}PINS}$ | Capacitance for SCL/CFG0 and SDA/CFG1 | f = 100 kHz; | | | 5 | pF |
| $C_{(I2C\_FM+\_BUS)}$ | I2C bus capacitance for FM+ (1MHz) | | | | 150 | pF |
| $C_{(I2C\_FM\_BUS)}$ | I2C bus capacitance for FM (400 kHz) | | | | 150 | pF |
| $R_{(EXT\_I2C\_FM+)}$ | External resistors on both SDA and SCL when operating at FM+ (1MHz) | $C_{(I2C\_FM+\_BUS)}$ = 150pF | 620 | 820 | 910 | Ω |
| $R_{(EXT\_I2C\_FM)}$ | External resistors on both SDA and SCL when operating at FM (400 kHz) | $C_{(I2C\_FM\_BUS)}$ = 150pF | 620 | 1500 | 2200 | Ω |
| **LV_DDC_SDA and LV_DDC_SCL** | | | | | | |
| $V_{IL\_1p2V}$ | Low-level input voltage | VCC = 3.0V; | -0.3 | | 0.360 | V |
| $V_{IH\_1p2V}$ | High-level input voltage | VCC = 3.6V; | 0.8 | | 3.6 | V |
| $V_{IL\_1p8V}$ | Low-level input voltage | VCC = 3.0V; | -0.3 | | 0.57 | V |
| $V_{IH\_1p8V}$ | High-level input voltage | VCC = 3.6V; | 1.19 | | 3.6 | V |
| $V_{IL\_3p3V}$ | Low-level input voltage | VCC = 3.0V; | -0.3 | | 0.8 | V |
| $V_{IH\_3p3V}$ | High-level input voltage | VCC = 3.6V; | 2.2 | | 3.6 | V |
| $R_{PULV}$ | Internal pull-up resistor to VIO | | 7450 | 10000 | 13000 | Ω |
| $\Delta V_{LV\_HYST\_3p3V}$ | Hysteresis on LV side for 3.3V LVCMOS | VIO = 3.3V; VCC = 3.3V | | 50 | | mV |
| **SIGDET_OUT** | | | | | | |
| $V_{OL}$ | Low level output voltage | $V_{CC}$ = 3.0V; | -0.3 | | 0.4 | V |
| $I_{OL}$ | Low level output current | $V_{CC}$ = 3.0V; | 4 | | | mA |
| $I_{HIZ}$ | Leakage current when output disabled | $V_{CC}$ = 3.6V; Pulled up to 3.6V through 10kΩ | -5 | | 5 | µA |
| **HPD_IN** | | | | | | |
| $V_{IL\text{-}HPDIN}$ | Low-level input voltage for HPD_IN | $V_{CC}$ = 3.6V; | -0.3 | | 0.8 | V |
| $V_{IH\text{-}HPDIN}$ | High-level input voltage for HPD_IN | $V_{CC}$ = 3.6V | 2.0 | | 5.5 | V |
| $I_{H\text{-}HPDIN}$ | High-level input current for HPD_IN | Device powered; $V_{IH}$ = 5.5V; Includes internal pull-down resistor | -50 | | 50 | µA |
| $I_{L\text{-}HPDIN}$ | Low-level input current for HPD_IN | Device powered; $V_{IL}$ = 0V; Includes internal pull-down resistor | -1 | | 1 | µA |
| $R_{PD\text{-}HPDIN}$ | Internal Pull-down resistance on HPD_IN | $V_{CC}$ = 3.3V; HPD_IN = 5.5V | 110 | 150 | 210 | kΩ |
| $I_{LEAK\text{-}HPDIN}$ | Fail-safe condition leakage current for HPD_IN | $V_{CC}$ = 0V; HPD_IN = 5.5V | -50 | | 50 | µA |
| **HPD_OUT** | | | | | | |
| $V_{OH\_3p3V}$ | High level output voltage when configured for 3.3V LVCMOS push/pull. | $V_{CC}$ = 3.0V; | 2.4 | | 3.465 | V |
| $V_{OH\_1p8V}$ | High level output voltage when configured for 1.8V LVCMOS push/pull. | $V_{CC}$ = 3.0V; | 1.3 | | 1.95 | V |
| $V_{OL\_PP}$ | Low level output voltage when configured for push/pull. | $V_{CC}$ = 3.0V; | -0.3 | | 0.4 | V |
| $V_{OL\_OD}$ | Low level output voltage when configured for open drain. | $V_{CC}$ = 3.0V; 0.5 kΩ to 3.6V load; | -0.3 | | 0.4 | V |

## 5.5 Electrical Characteristics（续）

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{OH\_3p3V}$ | High level output current for 3.3V LVCMOS | HPD_IN = $V_{IH-HPDIN}$; | | | -4 | mA |
| $I_{OL\_3p3V}$ | Low level output current for 3.3V LVCMOS | HPD_IN = $V_{IL-HPDIN}$; $I_2C$ mode; | 4 | | | mA |
| $I_{OH\_1p8V}$ | High level output current for 1.8V LVCMOS | HPD_IN = $V_{IH-HPDIN}$; | | | -1.1 | mA |
| $I_{OL\_1p8V}$ | Low level output current for 1.8V LVCMOS | HPD_IN = $V_{IL-HPDIN}$; $I_2C$ mode; | 1.2 | | | mA |
| **4-LEVEL CONTROL (MODE, LINEAR_EN, EQ1, ADDR/EQ0, TXSLEW, TXPRE, TXSWG, DCGAIN)** | | | | | | |
| $V_{TH}$ | Threshold "0" / "R" | $V_{CC}$ = 3.3V | | 0.55 | | V |
| $V_{TH}$ | Threshold "R" / "F" | $V_{CC}$ = 3.3V | | 1.65 | | V |
| $V_{TH}$ | Threshold "F" / "1" | $V_{CC}$ = 3.3V | | 2.7 | | V |
| $I_{IH}$ | High-level input current | $V_{IH}$ = 3.6V; $V_{CC}$ = 3.6V; | 20 | | 60 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0V; $V_{CC}$ = 3.6V; | －100 | | -40 | µA |
| $R_{4PU}$ | Internal pullup resistance | | | 48 | | kΩ |
| $R_{4PD}$ | Internal pull-down resistance | | | 98 | | kΩ |
| **HDMI HIGH SPEED INPUTS** | | | | | | |
| $D_{R\_RX\_DATA}$ | Data lanes data rate | | 0.25 | | 12 | Gbps |
| $D_{R\_RX\_CLK}$ | Clock lane data rate | | 0.25 | | 12 | Gbps |
| $V_{ID(DC)}$ | DC differential input swing | At pins; LINEAR_EN = L; | 400 | | 1200 | mVpp |
| $V_{ID(EYE)}$ | Differential input swing eye opening | At pins; | 75 | | | mVpp |
| $V_{RX\_ASSERT}$ | Signal detect assert level. | PRBS7 pattern; 12Gbps; | | 180 | | mVpp |
| $V_{RX\_DEASSERT}$ | Signal detect deassert level. | PRBS7 pattern; 12Gbps; | | 110 | | mVpp |
| $V_{ICM-DC}$ | Input DC common mode voltage bias | At pins; | 2.5 | 3.3 | VCC | V |
| $E_{EQ\_12Gbs\_MAX\_LT}$ | Maximum Fixed EQ gain (AC - DC) | At 6GHz; 12Gbps CTLE; EQ15; DC Gain = 0dB; Limited Mode; At output of RX; | | 12 | | dB |
| $E_{EQ\_12Gbps\_MIN\_LT}$ | Minimum Fixed EQ gain (AC - DC) | At 6GHz; 12Gbps CTLE; EQ0; DC Gain = 0dB; Limited Mode; At output of RX; | | 1.0 | | dB |
| $E_{EQ\_12Gbps\_BYPASS\_LT}$ | Maximum Fixed EQ Gain when EQ is bypassed. (AC - DC) | At 6GHz; 12Gbps CTLE; DC Gain = 0dB; Limited Mode; At output of RX; | | -1.5 | | dB |
| $E_{EQ\_6Gbs\_MAX\_LT}$ | Maximum Fixed EQ gain (AC - DC) | At 3GHz; 6Gbps CTLE; EQ15; DC Gain = 0dB; Limited Mode; At output of RX; | | 12.0 | | dB |
| $E_{EQ\_6Gbps\_MIN\_LT}$ | Minimum Fixed EQ gain (AC - DC) | At 3GHz; 6Gbps CTLE; EQ0; DC Gain = 0dB; Limited Mode; At output of RX; | | 0.6 | | dB |
| $E_{EQ\_3Gbs\_MAX\_LT}$ | Maximum Fixed EQ gain (AC - DC) | At 1.5GHz; 3Gbps CTLE; EQ15; DC Gain = 0dB; Limited Mode; At output of RX; | | 12 | | dB |
| $E_{EQ\_3Gbps\_MIN\_LT}$ | Minimum Fixed EQ gain (AC - DC) | At 1.5GHz; 3Gbps CTLE; EQ0; DC Gain = 0dB; Limited Mode; At output of RX; | | 0.8 | | dB |
| $R_{INT}$ | Input differential impedance when termination is enabled | At TTP2; HPD_IN = H; 0℃ $\leqslant T_A \leqslant$ 70℃ | 90 | 100 | 110 | Ω |
| $R_{INT}$ | Input differential impedance when termination is enabled | At TTP2; HPD_IN = H; －20℃ $\leqslant T_A \leqslant$ 85℃ | 85 | 100 | 115 | Ω |
| **HDMI HIGH SPEED OUTPUTS (Limited Mode)** | | | | | | |

## 5.5 Electrical Characteristics（续）

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OL\_open}$ | Single-ended low-level output voltage for DR ⩽ 1.65Gbps data rate | DR = 270 Mbps; HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000mV); TXPRE = "F" (0dB); TX termination open; VCC_EXT = 3.3V; 25℃ ⩽ $T_A$ ⩽ 85℃; | 2.7 | | 2.9 | V |
| $V_{OL\_300}$ | Single-ended low-level output voltage 1.65Gbps < DR ⩽ 3.4Gbps. | DR = 3.4Gbps; HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000mV); TXPRE = "F" (0dB); TX termination 300Ω; VCC_EXT = 3.3V; 25℃ ⩽ $T_A$ ⩽ 85℃; | 2.6 | | 2.9 | V |
| $V_{OL\_DAT20}$ | Data lane single-ended low-level output voltage 3.4Gbps < DR ⩽ 6Gbps. | DR = 5.94Gbps; HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000mV); TXPRE = "F" (0dB); VCC_EXT = 3.3V; 25℃ ⩽ $T_A$ ⩽ 85℃; | 2.3 | | 2.9 | V |
| $V_{SWING\_DA\_14}$ | Single-ended output voltage swing on data lanes with TX term set to open. | DR = 1.5Gbps; HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000mV); TXPRE = "F" (0dB); VCC_EXT = 3.3V; 25℃ ⩽ $T_A$ ⩽ 85℃; | 400 | 500 | 600 | mV |
| $V_{SWING\_DA\_14}$ | Single-ended output voltage swing on data lanes with TX term set to 300Ω. | DR = 3.4Gbps;HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000mV); TXPRE = "F" (0dB); VCC_EXT = 3.3V; 25℃ ⩽ $T_A$ ⩽ 85℃; | 400 | 500 | 600 | mV |
| $V_{SWING\_DA\_20}$ | Single-ended output voltage swing on data lanes for HDMI2.0 operation. | DR = 5.94Gbps;HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000mV); TXPRE = "F" (0dB); VCC_EXT = 3.3V; 25℃ ⩽ $T_A$ ⩽ 85℃; | 400 | 500 | 600 | mV |
| $V_{SWING\_CLK\_14\_OPEN}$ | Single-ended output voltage swing on clock lane for DR ⩽ 3.4Gbps datarate | HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000mV); TXPRE = "F" (0dB); VCC_EXT = 3.3V; 25℃ ⩽ $T_A$ ⩽ 85℃; TERM set to open; | 400 | 500 | 600 | mV |
| $V_{SWING\_CLK\_20}$ | Single-ended output voltage swing on clock lane for HDMI 2.0 | HPD_IN = H; AC_EN = L (DC-coupled); TXSWG = "F" (1000mV); TXPRE = "F" (0dB); VCC_EXT = 3.3V; 25℃ ⩽ $T_A$ ⩽ 85℃; | 300 | 400 | 600 | mV |
| $V_{OCM\text{-}DC\text{-}ON}$ | FRL DC common mode voltage when actively transmitting | At TTP4; AC_EN = L or H; LTP5, 6, 7 or 8; TXFFE0; 25℃ ⩽ $T_A$ ⩽ 85℃; | 2.335 | | 3.495 | V |
| $V_{OCM\text{-}DC\text{-}OFF}$ | FRL DC common mode voltage when lane 3 is disabled | At TTP4; FRL 3 lane mode; AC_EN = L or H; 25℃ ⩽ $T_A$ ⩽ 85℃; | 2.335 | | 3.495 | V |
| $V_{OD\_3G}$ | Data lanes Differential output swing | At TTP4; 2.97Gbps; HPD_IN = H; AC_EN = L or H; TXSWG = "F" (1000mV); TXPRE = "F" (0dB); 25℃ ⩽ $T_A$ ⩽ 85℃; | 400 | | 1560 | mV |
| $V_{OD\_6G}$ | Data lanes Differential output swing | At TTP4_EQ; 5.94Gbps; HPD_IN = H; AC_EN = L or H; TXSWG = "F" (1000mV); TXPRE = "F" (0dB); 25℃ ⩽ $T_A$ ⩽ 85℃; | 150 | | 1560 | mV |
| $V_{OD\_12G\_FRL}$ | Data lanes Differential output swing at 12 G FRL. | At TTP4_EQ; 12Gbps; HPD_IN = H; AC_EN = L or H; TXSWG = "F" (1000mV); TXFFE0; 25℃ ⩽ $T_A$ ⩽ 85℃; | 100 | | 1560 | mV |
| $I_{LEAK}$ | Failsafe condition leakage current | $V_{CC}$ = 0V; DC-coupled; TMDS output pulled to 3.465V with 50 Ω resistors | | | 35 | µA |
| $I_{OS}$ | Short circuit current limit | OUT_CLK, OUT_D[2:0] outputs P or N shorted to GND | | | 70 | mA |

## 5.5 Electrical Characteristics （续）

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $R_{TERM14}$ | Internal termination for DR ⩽ 3.4Gbps when DC-coupled | TERM = 1h; AC_EN = L (DC-coupled);HPD_IN=H; Active state; –20℃ ⩽ $T_A$ ⩽ 85℃; | 235 | 295 | 375 | Ω |
| $R_{TERM14}$ | Internal termination for DR ⩽ 3.4Gbps when AC-coupled | TERM = 1h; AC_EN = H (AC-coupled); HPD_IN=H; Active state; –20℃ ⩽ $T_A$ ⩽ 85℃; | 235 | 295 | 375 | Ω |
| $R_{TERM2+}$ | Internal termination for DR > 3.4Gbps when DC-coupled. | TERM = 3h; AC_EN = L (DC-coupled); HPD_IN=H; Active state; –20℃ ⩽ $T_A$ ⩽ 85℃; | 85 | 100 | 115 | Ω |
| $R_{TERM2+}$ | Internal termination for DR > 3.4Gbps when AC-coupled. | TERM = 3h; AC_EN = H (AC-coupled); HPD_IN=H; Active state; –20℃ ⩽ $T_A$ ⩽ 85℃; | 85 | 100 | 115 | Ω |
| $V_{TXPRE0\text{-}RATIO}$ | Transmitter FFE pre-emphasis ratio for 0dB. | TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 0h; CLK_VOD = 3h; D0_TXFFE = 0h; D0_VOD = 3h; D1_TXFFE = 0h; D1_VOD = 3h; D2_TXFFE = 0h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones; | | 0 | | dB |
| $V_{TXPRE1\text{-}RATIO}$ | Transmitter FFE pre-emphasis ratio for 3.5dB for data lanes | At 5.94Gbps HDMI 2.0; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 0h; CLK_VOD = 3h; D0_TXFFE = 1h; D0_VOD = 3h; D1_TXFFE = 1h; D1_VOD = 3h; D2_TXFFE = 1h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones; | | 4.0 | | dB |
| $V_{TXPRE2\text{-}RATIO}$ | Transmitter FFE pre-emphasis ratio for 6dB for data lanes | At 5.94Gbps HDMI 2.0; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 0h; CLK_VOD = 3h; D0_TXFFE = 2h; D0_VOD = 3h; D1_TXFFE = 2h; D1_VOD = 3h; D2_TXFFE = 2h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones; | | 6.5 | | dB |
| $V_{TXFFE0\text{-}RATIO}$ | Transmitter FRL TXFFE0 de-emphasis ratio | At 12Gbps FRL; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 4h; CLK_VOD = 3h; D0_TXFFE = 4h; D0_VOD = 3h; D1_TXFFE = 4h; D1_VOD = 3h; D2_TXFFE = 4h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones; | | -2.5 | | dB |
| $V_{TXFFE1\text{-}RATIO}$ | Transmitter FRL TXFFE1 de-emphasis ratio | At 12Gbps FRL; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 5h; CLK_VOD = 3h; D0_TXFFE = 5h; D0_VOD = 3h; D1_TXFFE = 5h; D1_VOD = 3h; D2_TXFFE = 5h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones; | | -3.2 | | dB |
| $V_{TXFFE2\text{-}RATIO}$ | Transmitter FRL TXFFE2 de-emphasis ratio. | At 12Gbps FRL; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 6h; CLK_VOD = 3h; D0_TXFFE = 6h; D0_VOD = 3h; D1_TXFFE = 6h; D1_VOD = 3h; D2_TXFFE = 6h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones; | | -3.5 | | dB |

## 5.5 Electrical Characteristics （续）

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{TXFFE3-RATIO}$ | Transmitter FRL TXFFE3 de-emphasis ratio | At 12Gbps FRL; TERM = 3h; HPD_IN = H; TX_AC_EN = 0; CLK_TXFFE = 7h; CLK_VOD = 3h; D0_TXFFE = 7h; D0_VOD = 3h; D1_TXFFE = 7h; D1_VOD = 3h; D2_TXFFE = 7h; D2_VOD = 3h; 20 * log (Vp/Vn); 128 zeros followed by 128 ones; | | -4.5 | | dB |
| **HDMI HIGH SPEED OUTPUTS (Linear Mode)** | | | | | | |
| $CP_{LF-TXSWG-0}$ | Low-frequency 1dB compression point Dx_VOD = 0. | At 10MHz; 200mVpp < $V_{ID}$ < 1200mVpp; EQ0; DCGAIN = 0dB; 12Gbps CTLE; CTLEBYP_EN = 0; BERT TX 100MHz clock starting at 200mV to 1200mV in 50mV steps;TX DC coupled to VCC_EXT; | | 900 | | mVpp |
| $CP_{HF-TXSWG-0}$ | High-frequency 1dB compression point Dx_VOD = 0. | At 6GHz; 200mVpp < $V_{ID}$ < 1200mVpp; EQ0; DCGAIN = 0dB; 12Gbps CTLE; CTLEBYP_EN = 0; TX DC coupled to VCC_EXT; | | 750 | | mVpp |
| $CP_{LF-TXSWG-R}$ | Low-frequency 1dB compression point Dx_VOD = 1. | At 10MHz; 200mVpp < $V_{ID}$ < 1200mVpp; EQ0; DCGAIN = 0dB; 12Gbps CTLE; CTLEBYP_EN = 0; BERT TX 100MHz clock starting at 200mV to 1200mV in 50mV steps; TX DC coupled to VCC_EXT; | | 1000 | | mVpp |
| $CP_{HF-TXSWG-R}$ | High-frequency 1dB compression point Dx_VOD = 1. | At 6GHz; 200mVpp < $V_{ID}$ < 1200mVpp; EQ0; DCGAIN = 0dB; 12Gbps CTLE; CTLEBYP_EN = 0;TX DC coupled to VCC_EXT; | | 800 | | mVpp |
| $CP_{LF-TXSWG-F}$ | Low-frequency 1dB compression point Dx_VOD = 2. | At 10MHz; 200mVpp < $V_{ID}$ < 1200mVpp; EQ0; DCGAIN = 0dB; 12Gbps CTLE; CTLEBYP_EN = 0; BERT TX 100MHz clock starting at 200mV to 1200mV in 50mV steps; TX DC coupled to VCC_EXT; | | 1100 | | mVpp |
| $CP_{HF-TXSWG-F}$ | High-frequency 1dB compression point Dx_VOD = 2. | At 6GHz; 200mVpp < $V_{ID}$ < 1200mVpp; EQ0; DCGAIN = 0dB; 12Gbps CTLE; CTLEBYP_EN = 0; TX DC coupled to VCC_EXT; | | 875 | | mVpp |
| $CP_{LF-TXSWG-1}$ | Low-frequency 1dB compression point Dx_VOD = 3. | At 10MHz; 200mVpp < $V_{ID}$ < 1200mVpp; EQ0; DCGAIN = 0dB; 12Gbps CTLE; CTLEBYP_EN = 0; BERT TX 100MHz clock starting at 200mV to 1200mV in 50mV steps; TX DC coupled to VCC_EXT; | | 1200 | | mVpp |
| $CP_{HF-TXSWG-1}$ | High-frequency 1dB compression point Dx_VOD = 3. | At 6GHz; 200mVpp < $V_{ID}$ < 1200mVpp; EQ0; DCGAIN = 0dB; 12Gbps CTLE; CTLEBYP_EN = 0; TX DC coupled to VCC_EXT; | | 950 | | mVpp |
| **RCLKOUT** | | | | | | |
| $V_{TX-CM}$ | Output common mode voltage | | 2.4 | 2.8 | 3.465 | V |
| $V_{ODPP}$ | Peak-to-peak output voltage swing | | 600 | 700 | 1100 | mV |
| $R_{TERM}$ | Differential output impedance | | 70 | 100 | 120 | Ω |
| $t_{RF}$ | Rise and fall time | 20% to 80% | 100 | | 370 | ps |
| $C_{TX\_AC}$ | Required external AC capacitor | | 8 | 10 | 12 | nF |

## 5.6 Timing Requirements

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Local I2C (SCL/CFG0, SDA/CFG1). Refer to 图 6-9.** | | | | | |
| $f_{SCL}$ | $I^2C$ clock frequency | | | 1 | MHz |
| $t_{BUF}$ | Bus free time between START and STOP conditions | 0.5 | | | μs |
| $t_{HD\_STA}$ | Hold time after repeated START condition. After this period, the first clock pulse is generated | 0.26 | | | μs |
| $t_{LOW}$ | Low period of the $I^2C$ clock | 0.5 | | | μs |
| $t_{HIGH}$ | High period of the $I^2C$ clock | 0.26 | | | μs |
| $t_{SU\_STA}$ | Setup time for a repeated START condition | 0.26 | | | μs |
| $t_{HD\_DAT}$ | Data hold time | 0 | | | μs |
| $t_{SU\_DAT}$ | Data setup time | 50 | | | ns |
| $t_R$ | Rise time of both SDA and SCL signals | | | 120 | ns |
| $t_F$ | Fall time of both SDA and SCL signals | 4 | | 120 | ns |
| $t_{SU\_STO}$ | Setup time for STOP condition | 0.26 | | | μs |
| **DDC Snoop I2C Timings. Refer to 图 6-9.** | | | | | |
| $f_{SCL}$ | $I^2C$ DDC clock frequency | | | 100 | kHz |
| $t_{BUF}$ | Bus free time between START and STOP conditions | 4.7 | | | μs |
| $t_{HD\_STA}$ | Hold time after repeated START condition. After this period, the first clock pulse is generated | 4 | | | μs |
| $t_{LOW}$ | Low period of the $I^2C$ clock | 4.7 | | | μs |
| $t_{HIGH}$ | High period of the $I^2C$ clock | 4 | | | μs |
| $t_{SU\_STA}$ | Setup time for a repeated START condition | 4.7 | | | μs |
| $t_{HD\_DAT}$ | Data hold time | 0 | | | μs |
| $t_{SUDAT}$ | Data setup time | 250 | | | ns |
| $t_R$ | Rise time of both SDA and SCL signals. Measured from 30% to 70%. | | | 1000 | ns |
| $t_F$ | Fall time of both SDA and SCL signals  Measured from 70% to 30%. | | | 300 | ns |
| $t_{SU\_STO}$ | Setup time for STOP condition | 4 | | | μs |
| $C_{b\_LV}$ | Capacitive load for each bus line on LV side | | | 50 | pF |
| **Power-On. Refer to 图 6-1.** | | | | | |
| $t_{VCC\_RAMP}$ | $V_{CC}$ supply ramp. Measured from 10% to 90%. | 0.10 | | 50 | ms |
| $t_{D\_PG}$ | Internal POR de-assertion delay | | | 5 | ms |
| $t_{VIO\_SU}$ | $V_{IO}$ supply stable before reset(2) high. | 100 | | | μs |
| $t_{CFG\_SU}$ | Configuration pins(1) setup before reset(2) high. | 0 | | | μs |
| $t_{CFG\_HD}$ | Configuration pins(1) hold after reset(2)high. | 500 | | | μs |

(1) Follow comprise the configuration pins:  MODE,  ADDR/EQ0, EQ1, TXSWG, TXSLEW, TXPRE, AC_EN, HPDOUT_SEL, DCGAIN
(2) Reset is the logical AND of internal POR and EN pin.

## 5.7 Switching Characteristics

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Redriver** | | | | | | |
| $f_{HDMI14\_open}$ | Maximum HDMI 1.4 clock frequency at which TX termination is assured to be open | HDMI1.4; 25MHz ⩽ IN_CLK ⩽ 340MHz; TXTERM_AUTO_HDMI14 = 0h; TERM = 2h; TX is DC-coupled; | 165 | | | MHz |

## 5.7 Switching Characteristics （续）

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $f_{HDMI14\_300}$ | Minimum HDMI 1.4 clock frequency at which TX termination is assured to be 300Ω | HDMI1.4; 25MHz ≤ IN_CLK ≤ 340MHz; TXTERM_AUTO_HDMI14 = 0h; TERM = 2h; TX is DC-coupled; | | | 250 | MHz |
| $t_{AEQ\_DONE}$ | Time from start of FRL link training to AEQ complete for 3Gbps. | | | | 0.7 | ms |
| $t_{AEQ\_DONE}$ | Time from start of FRL link training to AEQ complete for 6Gbps, 8Gbps, 10Gbps, and 12Gbps | | | | 0.5 | ms |
| $t_{PD}$ | Propagation delay time | At TTP4; | 90 | | 220 | ps |
| $t_{SK1(T)}$ | Clock lane Intra-pair output skew with worse case skew at inputs | At TTP4; With 0.15 UI skew at input; At 6Gbps with 150MHz clock; TX termination 100 Ω; Linear mode; | | | 0.15 | UI |
| $t_{SK1(T)}$ | Data lane Intra-pair output skew with worse case skew at inputs | At TTP4; With 0.15 UI skew at input; At 12Gbps; LTP5, 6, 7, or 8; TXFFE0; TX termination 100 Ω; Linear mode; | | | 0.15 | UI |
| $t_{SK1(T)}$ | Clock lane Intra-pair output skew with zero intra-pair skew at inputs | At TTP4; No intra-pair skew at input; 6Gbps with 150MHz clock; TX termination 100 Ω; Limited mode; | | 0.10 | 0.15 | UI |
| $t_{SK1(T)}$ | Data lane Intra-pair output skew with zero intra-pair skew at inputs | At TTP4; No intra-pair skew at input; At 12Gbps; LTP5, 6, 7, or 8; TXFFE0; TX termination 100 Ω; Limited mode; | | 0.053 | 0.11 | UI |
| $t_{SK2(T)}$ | Inter-pair output skew | At TTP4; At 12Gbps; LTP5, 6, 7, or 8; TXFFE0; | | | 30 | ps |
| $t_{RF\text{-}CLK\text{-}14}$ | Transition time (rise and fall time) for clock lane when operating at HDMI1.4 | At TTP4; 20% to 80%; Clock Frequency = 300MHz; | 75 | | 600 | ps |
| $t_{RF\text{-}CLK\text{-}20}$ | Transition time (rise and fall time) for clock lane when operating at HDMI 2.0 | At TTP4; 20% to 80%; Clock Frequency = 150MHz; | 75 | | 600 | ps |
| $t_{RF\_14}$ | Transition time (rise and fall time) for data lanes when operating at HDMI 1.4 | At TTP4; 20% to 80%; DR = 3Gbps; SLEW_HDMI14 = default; PRBS7 pattern; Clock Frequency = 300MHz; | 75 | | 195 | ps |
| $t_{RFDAT\_20}$ | Transition time (rise and fall time) for data lanes when operating at HDMI 2.0 | At TTP4; 20% to 80%; DR = 6Gbps; SLEW_HDMI20 = default; PRBS7 pattern; Clock Frequency = 150MHz; | 42.5 | | 115 | ps |
| $t_{SLEW\_FRL}$ | Single-ended TX slew rate for data lanes when operating at HDMI 2.1 FRL | At TTP4; Slope at 50% level; All FRL DR up to 12Gbps; SLEW_HDMI21 = Default; clock pattern of 128 zeros and 128 ones; | | | 16 | mV/ps |
| $t_{TRANS\_3G}$ | Transition bit duration when de-emphasis/ pre-emphasis is enabled | At TTP4; DR = 3Gbps; Clock pattern of 128 zeros followed by 128 ones; | 0.4 | | 1 | UI |
| $t_{TRANS\_6G}$ | Transition bit duration when de-emphasis/ pre-emphasis is enabled | At TTP4; DR = 6Gbps; Clock pattern of 128 zeros followed by 128 ones; | 0.4 | | 1 | UI |
| $t_{TRANS\_8G}$ | Transition bit duration when de-emphasis/ pre-emphasis is enabled | At TTP4; DR = 8Gbps; Clock pattern of 128 zeros followed by 128 ones; | 0.4 | | 1 | UI |
| $t_{TRANS\_10G}$ | Transition bit duration when de-emphasis/ pre-emphasis is enabled | At TTP4; DR = 10Gbps; Clock pattern of 128 zeros followed by 128 ones; | 0.5 | | 1.1 | UI |
| $t_{TRANS\_12G}$ | Transition bit duration when de-emphasis/ pre-emphasis is enabled | At TTP4; DR = 12Gbps; Clock pattern of 128 zeros followed by 128 ones; | 0.6 | | 1.3 | UI |
| **HPD** | | | | | | |
| $t_{HPD\_PD}$ | HPD_IN to HPD_OUT propagation delay | Refer to 图 6-7 | | | 100 | µs |
| $t_{HPD\_PWRDOWN}$ | HPD_IN debounce time before declaring Powerdown. Enter Powerdown if HPD_IN is low after debounce time. | Refer to 图 6-7 | 2 | | 4 | ms |

## 5.7 Switching Characteristics （续）

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{HPD\_STANDBY}$ | HPD_IN debounce time required for exiting Powerdown to Standby. Exit Powerdown if HPD_IN is high after debounce time. | Refer to 图 6-8 | 2 | | 4 | ms |
| **Standby** | | | | | | |
| $t_{STANDBY\_ENTRY}$ | Detection of electrical idle to entry into Standby. | HPD_IN = H; | | | 300 | µs |
| $t_{SIGDET\_DB}$ | Maximum differential signal glitch time rejected during debounce before transitioning from standby to active | HPD_IN = H; | | | 25 | µs |
| $t_{SIGDET\_DB}$ | Maximum differential signal glitch time rejected during debounce before transitioning from active to standby | HPD_IN = H; | | | 50 | ns |
| $t_{STANDBY\_EXIT}$ | Detection of differential signal to exit from Standby to Active state when SIGDET_OUT low. | HPD_IN = H; Does not include AEQ time if AEQ_TX_DELAY_EN = 1; | | | 200 | µs |
| $f_{SCL}$ | DDC buffer frequency | | | | 100 | kHz |
| $t_{PLH1}$ | Propagation delay time. Low-to-high-level output. VIO set to 1.2V LVCMOS levels. | LV to HV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 1400 | ns |
| | Propagation delay time. Low-to-high-level output. VIO set to 1.8V LVCMOS levels. | LV to HV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 1400 | ns |
| | Propagation delay time. Low-to-high-level output. VIO set to 3.3V LVCMOS levels. | LV to HV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 1400 | ns |
| $t_{PLH2}$ | Propagation delay time. Low-to-high-level output. VIO set to 1.2V LVCMOS levels. | HV to LV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 410 | ns |
| | Propagation delay time. Low-to-high-level output. VIO set to 1.8V LVCMOS levels. | HV to LV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 410 | ns |
| | Propagation delay time. Low-to-high-level output. VIO set to 3.3V LVCMOS levels. | HV to LV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 410 | ns |
| $t_{PHL1}$ | Propagation delay time. High to low-level output. VIO set to 1.2V LVCMOS. | LV to HV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 1200 | ns |
| | Propagation delay time. High to low-level output. VIO set to 1.8V LVCMOS. | LV to HV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 1200 | ns |
| | Propagation delay time. High to low-level output. VIO set to 3.3V LVCMOS. | LV to HV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 1200 | ns |
| $t_{PHL2}$ | Propagation delay time. High to low-level output. VIO set to 1.2V LVCMOS. | HV to LV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 535 | ns |
| | Propagation delay time. High to low-level output. VIO set to 1.8V LVCMOS. | HV to LV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 535 | ns |
| | Propagation delay time. High to low-level output. VIO set to 3.3V LVCMOS. | HV to LV; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; DDC_LV_DCC_EN = 1'b1; | | | 535 | ns |
| $t_{LV\_FALL}$ | LV side fall time for 1.2V LVCMOS | 70% to 30%; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; | 75 | | 260 | ns |
| | LV side fall time for 1.8V LVCMOS | 70% to 30%; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; | 75 | | 260 | ns |
| | LV side fall time for 3.3V LVCMOS | 70% to 30%; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; | 75 | | 260 | ns |
| $t_{HV\_FALL}$ | HV side fall time | 70% to 30%; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; | 75 | | 260 | ns |
| $t_{LV\_RISE}$ | LV side rise time for 1.2V LVCMOS | 30% to 70%; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; Pulled up to VIO using $R_{PULV}$; | 300 | | 670 | ns |
| | LV side rise time for 1.8V LVCMOS | 30% to 70%; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; Pulled up to VIO using $R_{PULV}$; | 300 | | 670 | ns |
| | LV side rise time for 3.3V LVCMOS | 30% to 70%; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; Pulled up to VIO using $R_{PULV}$; | 300 | | 670 | ns |

## 5.7 Switching Characteristics （续）

over recommended voltage and operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{HV\_RISE\_50pF}$ | HV side rise time (50pF load) | 30% to 70%; $C_{LV\_BUS}$ = $C_{HV\_BUS}$ = 50pF; VCC = 3.0V; HDMI5V = 5.3V; Pulled up to HDMI5V using $R_{PUHV}$; | | | 225 | ns |
| $t_{HV\_RISE\_750pF}$ | HV side rise time (750pF load) | 30% to 70%; $C_{LV\_BUS}$ = 50pF; $C_{HV\_BUS}$ = 750pF; VCC = 3.0V; HDMI5V = 5.3V; Pulled up to HDMI5V using $R_{PUHV}$; | | | 1250 | ns |

## 5.8 Typical Characteristics

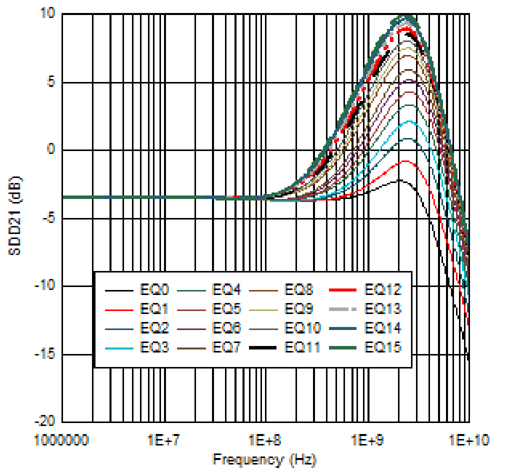


图 5-1. 3Gbps CTLE EQ Curves with GLOBAL_DCG = 0x2 in Limited Mode

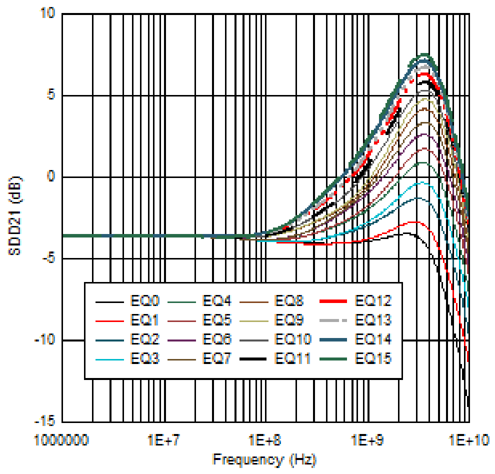


图 5-2. 6Gbps CTLE EQ Curves with GLOBAL_DCG = 0x2 in Limited Mode

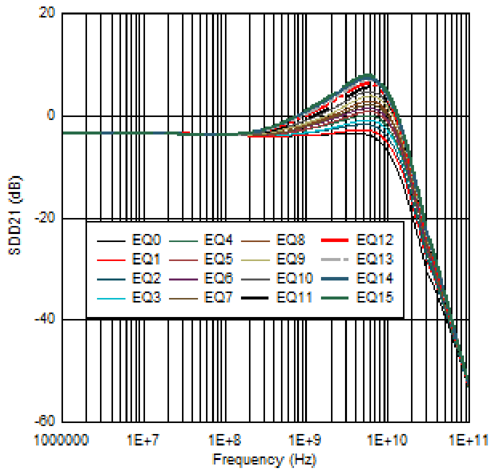


图 5-3. 12Gbps CTLE EQ Curves with GLOBAL_DCG =0x2 in Limited Mode

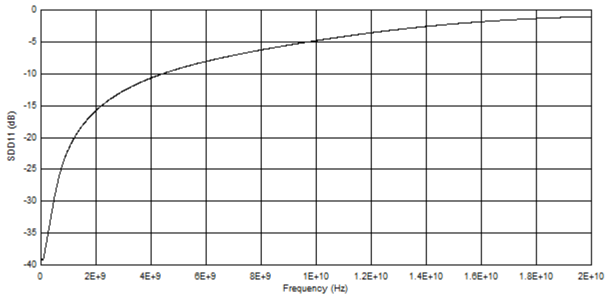


图 5-4. Input Differential Return Loss (SDD11)

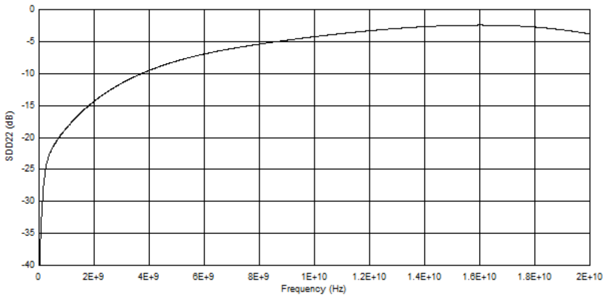


图 5-5. Output Differential Return Loss (SDD22)

# 6 Parameter Measurement Information

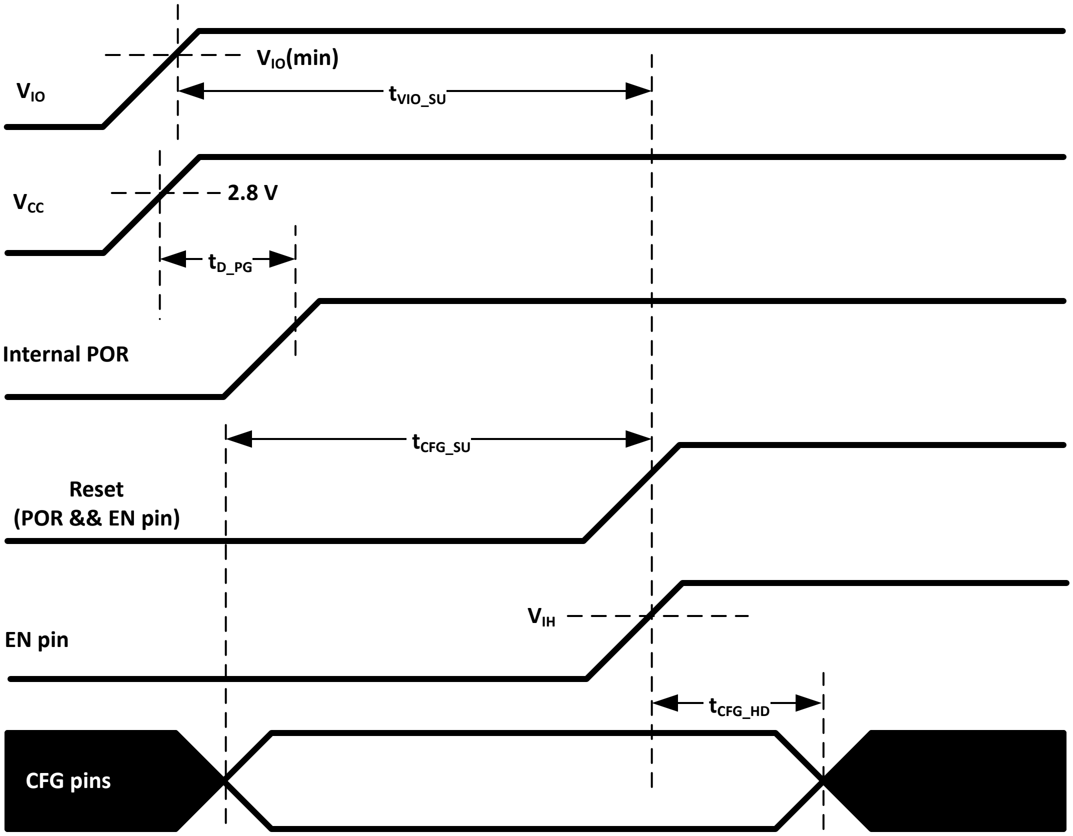


图 6-1. Power-On Timing Requirements

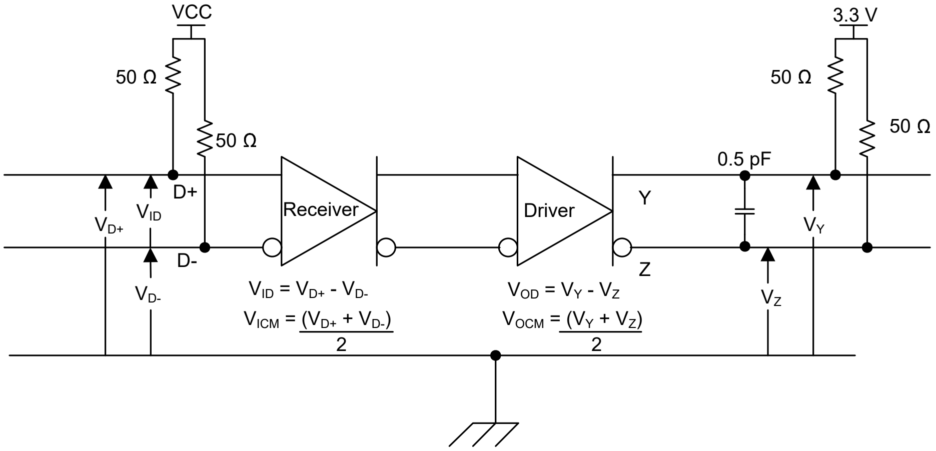


图 6-2. TMDS Main Link Test Circuit

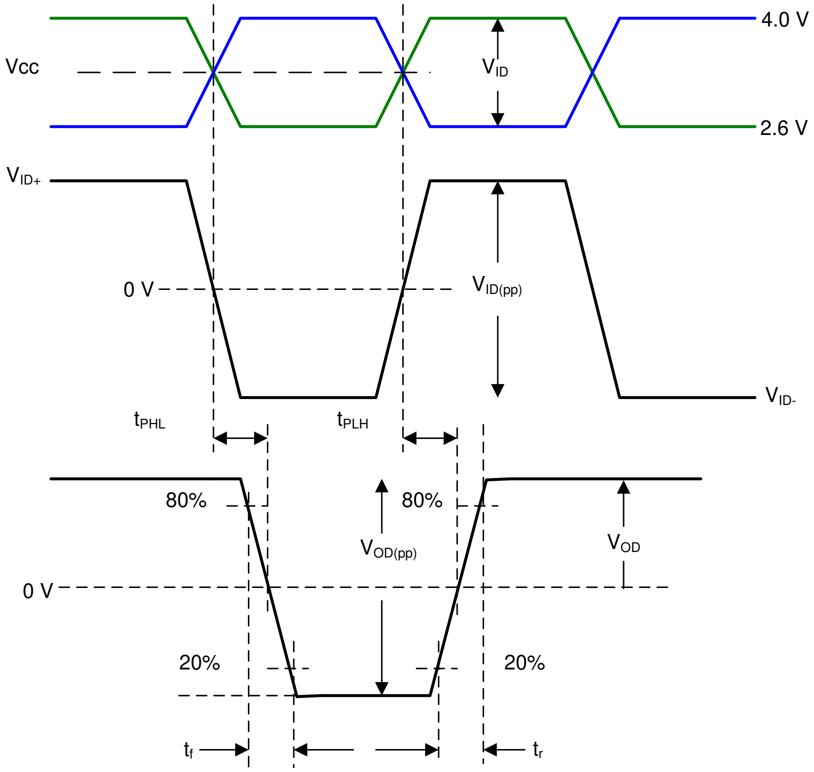


图 6-3. Input or Output Timing Measurements

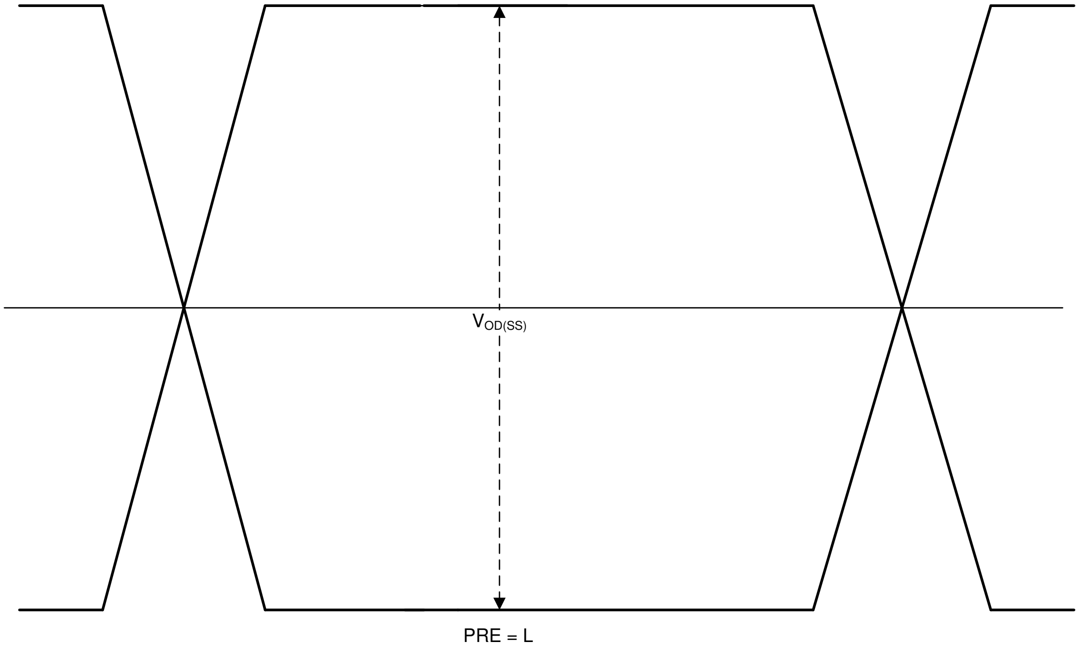


图 6-4. Output Differential Waveform

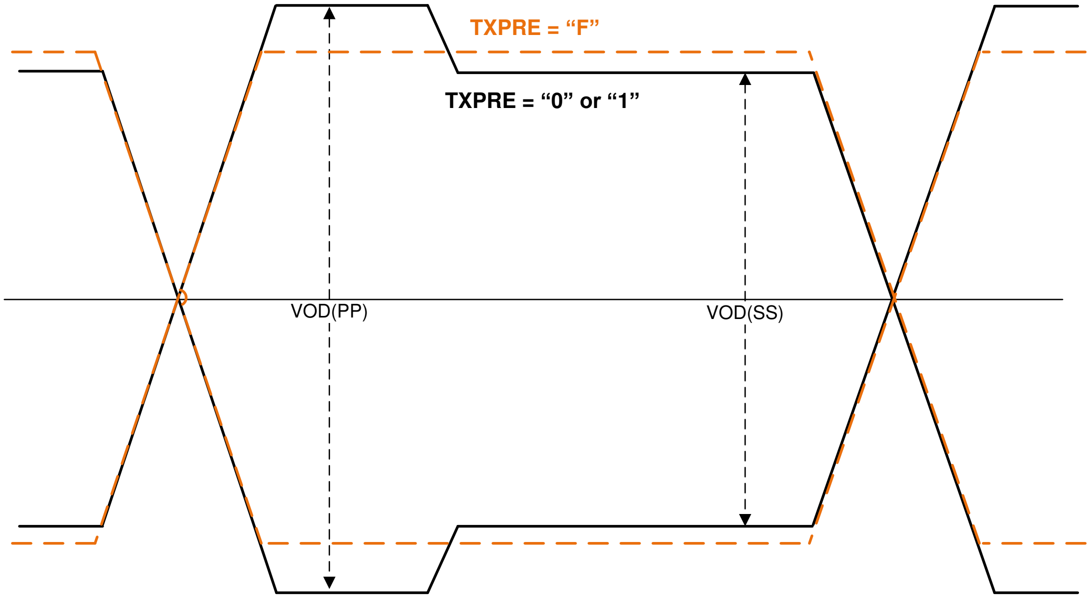
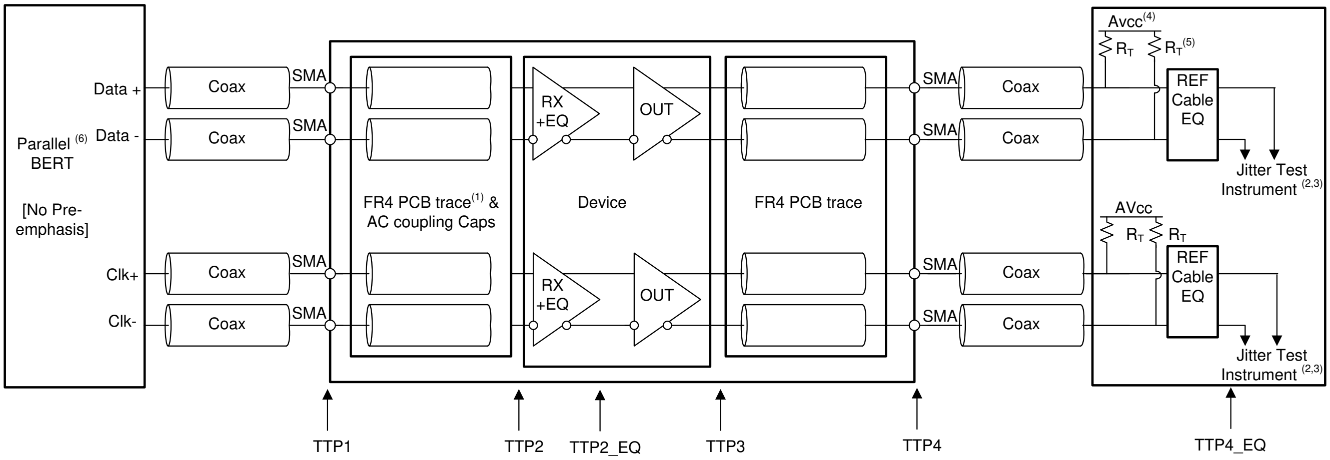


图 6-5. Output Differential Waveform with De-Emphasis



(1) The FR4 trace between TTP1 and TTP2 is designed to emulate 1-12” of FR4, AC-coupling capacitor, connector and another 2” of FR4. Trace width – 4 mils. 100 Ω differential impedance.

(2) All Jitter is measured at a BER of $10^9$. HDMI 2.1 jitter measured at BER $10^{-10}$.

(3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP

(4) AVCC = 3.3V.

(5) $R_T$ = 50 Ω.

(6) For HDMI 1.4 or 2.0, the input signal from parallel Bert does not have any pre-emphasis or de-emphasis. For HDMI 2.1 FRL, the input signal from BERT will have 2.18dB pre-shoot and −3.1dB de-emphasis. Refer to *Recommended Operating Conditions*.

图 6-6. HDMI Output Jitter Measurement

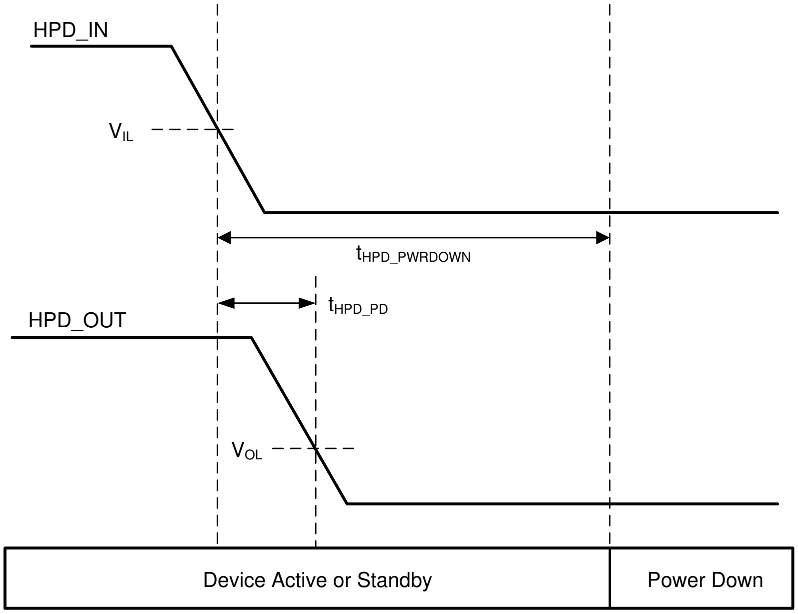


图 6-7. HPD Logic Shutdown and Propagation Timing

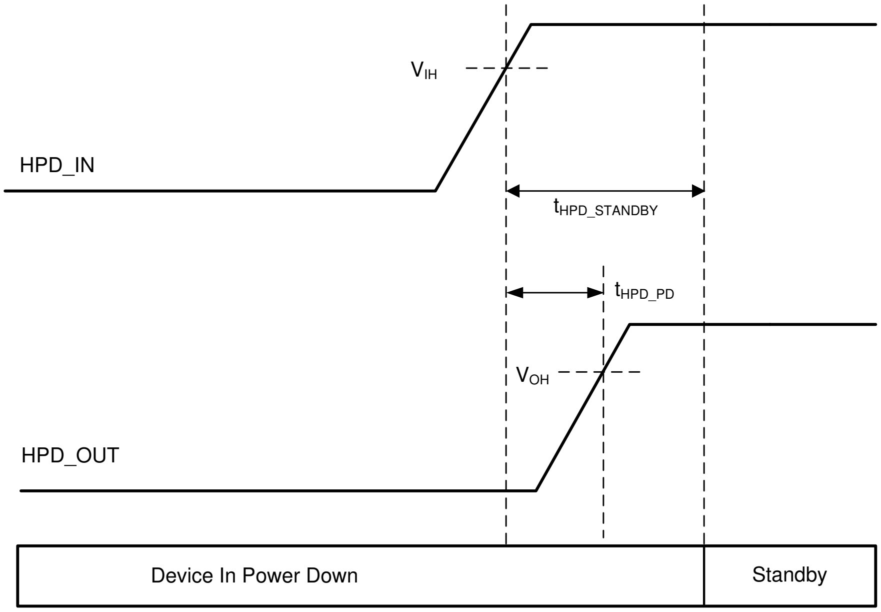


图 6-8. HPD Logic Standby and Propagation Timing

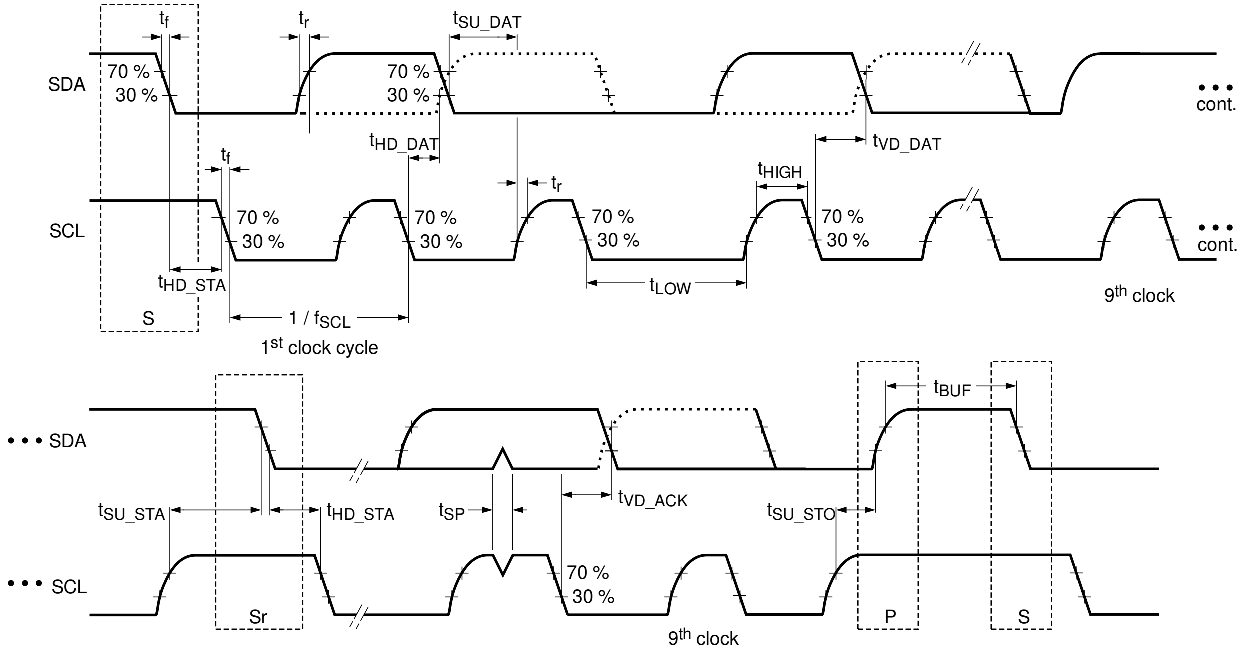


图 6-9. I$^2$C SCL and SDA Timing

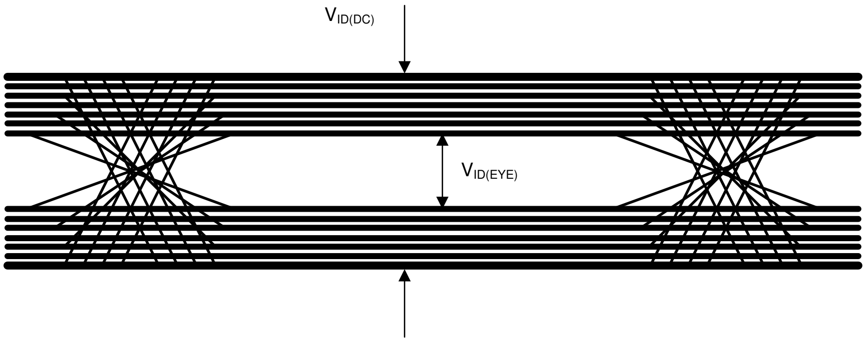
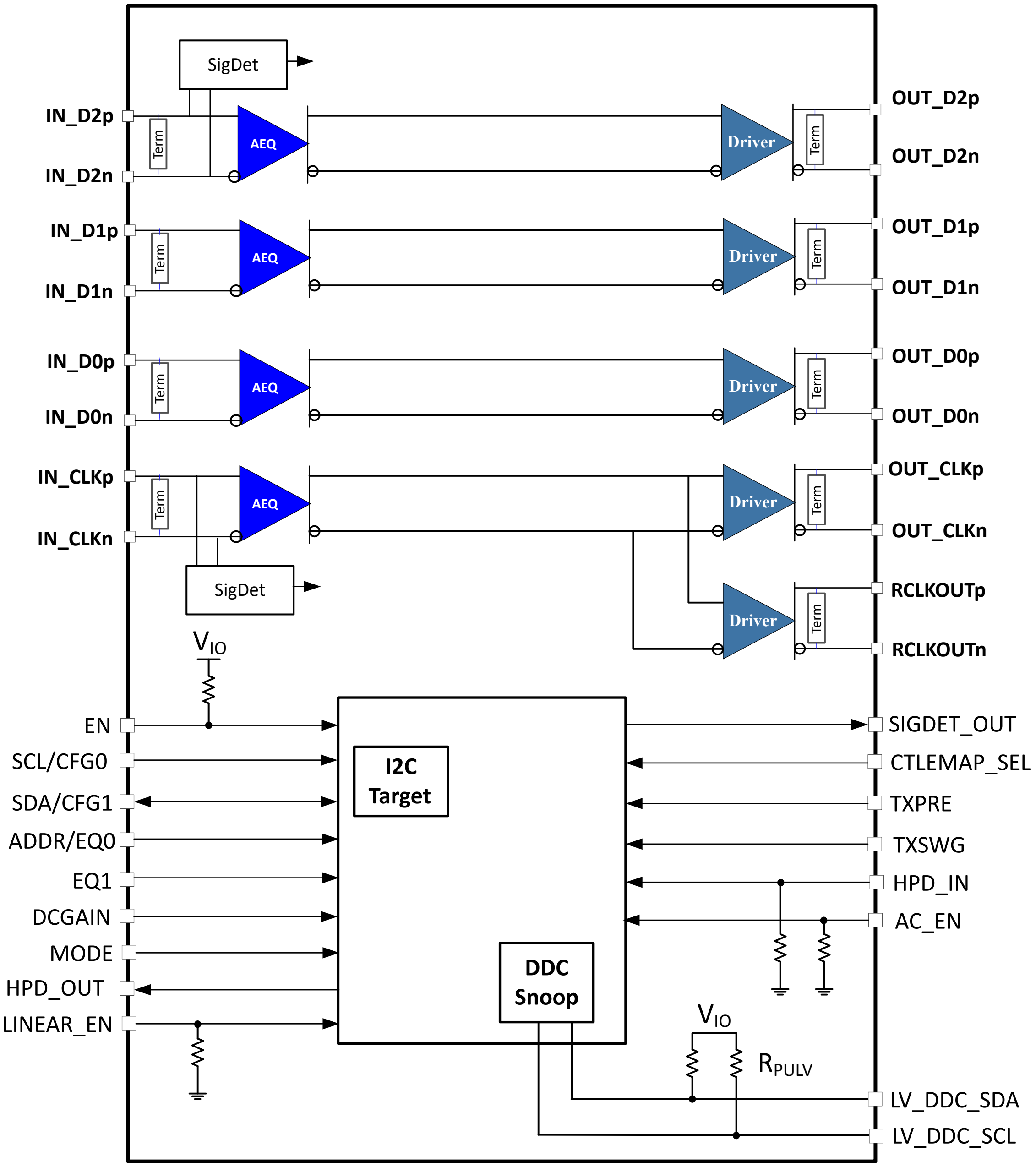


图 6-10. $V_{ID(DC)}$ and $V_{ID(EYE)}$

# 7 Detailed Description

## 7.1 Functional Block Diagram



## 7.2 Feature Description

### 7.2.1 4-Level Inputs

The TMDS1204 has 4-level inputs pins that control the receiver equalization gain, transmitter voltage swing, and pre-emphasis, and place TMDS1204 into different modes of operation. These 4-level inputs utilize a resistor divider to help set the 4 valid levels and provide a wider range of control settings. There are internal pull-up and a pull-down resistors. These resistors are combined with the external resistor connection to achieve the desired voltage level.

**表 7-1. 4-Level Control Pin Settings**

| LEVEL | SETTINGS |
|---|---|
| 0 | Tie 1kΩ 5% to GND. |
| R | Tie 20kΩ 5% to GND. |
| F | Float (leave pin open) |
| 1 | Tie 1kΩ 5% to $V_{CC}$. |

---

备注

图 6-1 shows how all 4-level inputs are latched after the rising edge of the EN pin. After these pins are sampled, the internal pull-up and pull-down resistors will be isolated to save power.

---

### 7.2.2 I/O Voltage Level Selection

The TMDS1204 supports 1.2V, 1.8V, and 3.3V LVCMOS levels. The VIO pin is used to select which voltage level is used for the following 2-level control pins: LV_DDC_SDA, LV_DDC_SCL, SCL/CFG0, and SDA/CFG1.

The AC_EN pin threshold is fixed at 3.3V LVCMOS levels. EN pin threshold is fixed at 1.2V LVCMOS threshold.

**表 7-2. Selection of LVCMOS Signaling Level**

| VIO pin | LVCMOS Signaling Level |
|---|---|
| VALUE < 1.5V | 1.2V |
| 1.5V < VALUE < 2.5V | 1.8V |
| VALUE > 2.5V | 3.3V |

### 7.2.3 HPD_OUT

The TMDS1204 will level shift the 5V signaling level present on the HPD_IN pin to a lower voltage such as 1.8V or 3.3V levels on the HPD_OUT pin. The HPD_OUT supports both push-pull and open drain. The default operation is push-pull. Selection between push-pull and open drain is done through the HPDOUT_SEL register.

表 7-2 lists how the VIO determines the output level of HPD_OUT when HPD_OUT is configured for push-pull operation. Please note push-pull operation is not supported for VIO less than 1.7V.

---

备注

Open-drain operation is only supported when TMDS1204 is configured for I2C mode.

When EN pin is low, the HPD_OUT pin will be in a high impedance state. It is recommended to have a weak pull-down resistor (such as 220k) on HPD_OUT.

---

### 7.2.4 Lane Control

The TMDS1204 has various lane control features. Pin strapping globally controls features like receiver equalization, DC Gain, $V_{OD}$ swing, slew rate, and pre-emphasis or de-emphasis. Through $I^2C$ receiver equalization, transmitter swing, and pre-emphasis for each lane can be independently controlled.

### 7.2.5 Swap

图 7-1 shows how TMDS1204 incorporates a swap function which can swap the lanes. The RX EQ, pre-emphasis, termination, and slew configurations will follow the new mapping. This function is supported in pin strap mode as well as when TMDS1204 is configured for $I^2C$ mode. A register controls the swap function in $I^2C$ mode.

**表 7-3. Swap Functions**

| Normal Operation<br>CFG1 pin = L or LANE_SWAP Register is 0h | CFG1 = H or LANE_SWAP Register is 1h |
|---|---|
| IN_D2 → OUT_D2 | IN_CLK → OUT_CLK |
| IN_D1 → OUT_D1 | IN_D0 → OUT_D0 |
| IN_D0 → OUT_D0 | IN_D1 → OUT_D1 |
| IN_CLK → OUT_CLK | IN_D2 → OUT_D2 |

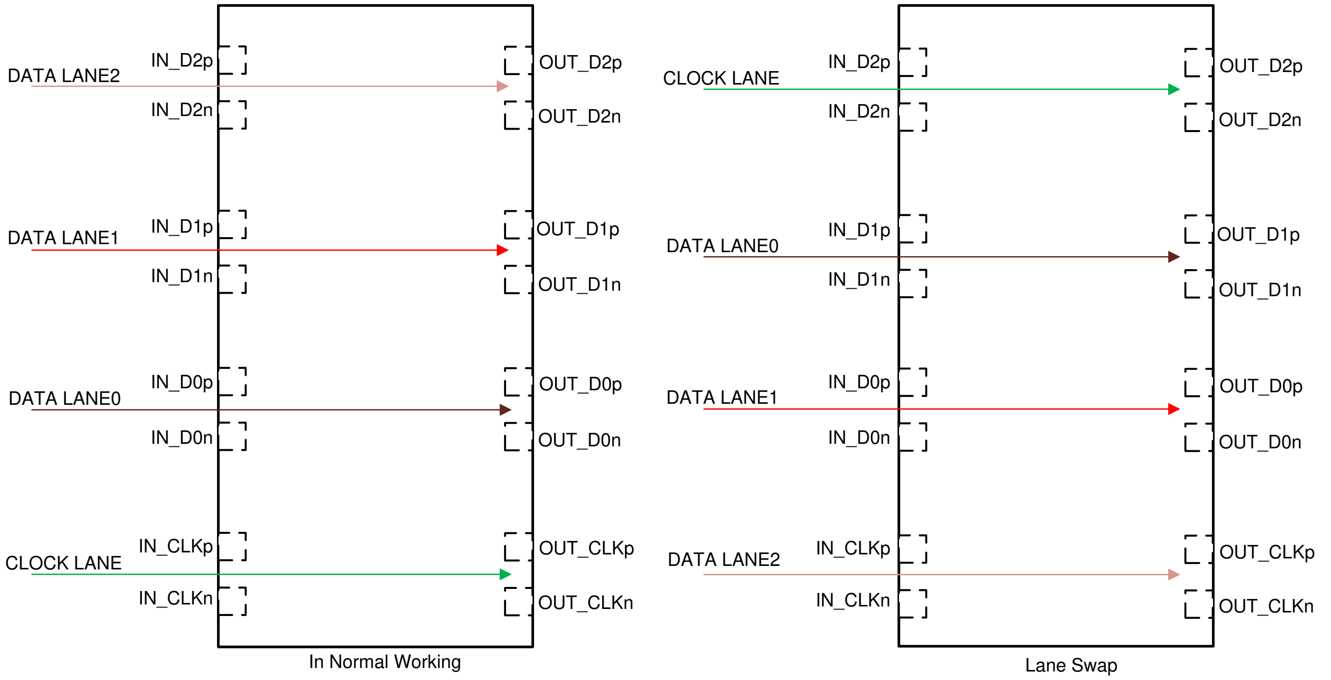


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**图 7-1. TMDS1204 Swap Function**

### 7.2.6 Linear and Limited Redriver

The TMDS1204 supports both linear and limited redriver. Selection between linear and limited can be done from the LINEAR_EN pin in pin-strap mode or through GLOBAL_LINR_EN register in $I^2C$ mode.

The limited redriver mode will decouple TMDS1204 transmitter's voltage swing, pre-emphasis or de-emphasis, and slew rate from the GPUs transmitter. This allows the GPU to use a lower power TX setting and depends on the TMDS1204 transmitter to meet TX compliance requirements. For source applications, it is recommended to configure TMDS1204 as a limited redriver. It is not recommended to use limited redriver mode in sink applications.

Unlike limited redriver mode, in linear redriver mode the TMDS1204 transmitter's output is not decoupled from the GPU's transmitter. In linear redriver mode, the TMDS1204 transmitter's output is a linear function of its input. The linear redriver mode offers transparency to link training which makes it perfect for HDMI 2.1 applications. For HDMI sink applications, it is recommended to configure TMDS1204 as a linear redriver.

表 7-4 lists the requirements that the GPU transmitter must meet if linear redriver mode is used in an HDMI 2.1 source application. Linear redriver mode should only be used for HDMI 2.1 data rates. For HDMI 1.4 and 2.0, the TMDS1204 should be configured for limited mode (LINEAR_EN = "0" or "1").

**表 7-4. Linear Redriver Mode: GPU TX Requirements for HDMI Source Applications**

| GPU TX Parameter | Min | Max | Units |
|---|---|---|---|
| Single-ended TX swing for HDMI 2.1 | 400 | 500 | mV |
| TX rise/fall time for 3, 6, 8, 10, and 12Gbps FRL | | 16 | mV/ps |

The TMDS1204 in pin-strap mode provides the option to dynamically switch between limited and linear based on the HDMI mode of operation. The feature is enabled by setting LINEAR_EN pin = "1".

**表 7-5. Pin-Strap Mode LINEAR_EN Pin Function**

| LINEAR_EN Pin Level | HDMI 1.4, 2.0, or DP | HDMI 2.1 FRL |
|---|---|---|
| 1 | Limited Enabled | Linear Enabled |
| F | Linear Enabled<br>Recommended for DP and HDMI sink application. | Linear Enabled<br>Recommended for DP and HDMI sink application. |
| R | Reserved | Reserved |
| 0 | Limited Enabled.<br>Recommended for HDMI source application | Limited Enabled<br>Recommended for HDMI source application |

### 7.2.7 Main Link Inputs

Each main link input (IN_D[2:0] and IN_CLK) is internally biased to 3.3V through approximately 100Ω (50Ω single-ended). When using TMDS1204 in DisplayPort++ applications, external AC-coupling capacitance should be used. When using TMDS1204 in an HDMI application such as in an HDMI monitor, the main link inputs can be DC-coupled to a compliant HDMI transmitter. Each input data channel contains an equalizer to compensate for cable or board losses.

### 7.2.8 Receiver Equalizer

The equalizer is used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. TMDS1204 supports fixed receiver equalizer by setting the EQ0 and EQ1 pins or through the I$^2$C register. 表 7-6 lists the pin strap settings and EQ values.

The TMDS1204 has three sets of CTLE curves (3Gbps CTLE, 6Gbps CTLE, and 12Gbps CTLE) with each curve having 16 AC gain settings and 3 DC gain settings. 表 7-6 provides details about the 16 AC gain settings with GLOBAL_DCG = 0x2.

The TMDS1204 in pin-strap mode has three CTLE HDMI Datarate Maps: Map A, Map B, and Map C. 表 7-7 provides details about these maps. The expectation is Map A and C should be used if TMDS1204 is used in a source application and Map B for a sink application.

表 7-8 lists how the sampled state of the CTLEMAP_SEL pin determines the default CTLE HDMI Datarate map when the TMDS1204 is configured for pin-strap mode.

In I$^2$C mode, the default CTLE (3Gbps, 6Gbps, or 12Gbps) used for each HDMI mode can be controlled from a register.

### 表 7-6. Receiver EQ Settings When GLOBAL_DCG = 0x2

| EQ Setting[1] | RX EQ Level for 3Gbps CTLE (Gain at 1.5GHz – Gain at 10-MHz) | RX EQ Level for 6Gbps CTLE (Gain at 3GHz – Gain at 10-MHz) | RX EQ Level for 12Gbps CTLE (Gain at 6GHz – Gain at 10-MHz) | EQ1 PIN | EQ0 PIN |
|---|---|---|---|---|---|
| 0[2] | 1.0 | 0.5 | 0 | 0 | 0 |
| 1 | 2.0 | 1.0 | 0.8 | 0 | R |
| 2 | 3.2 | 2.4 | 1.8 | 0 | F |
| 3 | 4.2 | 3.3 | 2.7 | 0 | 1 |
| 4 | 5.3 | 4.4 | 3.7 | R | 0 |
| 5 | 6.0 | 5.2 | 4.4 | R | R |
| 6 | 7.0 | 6.0 | 5.0 | R | F |
| 7 | 7.7 | 6.8 | 5.8 | R | 1 |
| 8 | 9.0 | 7.5 | 6.5 | F | 0 |
| 9 | 9.5 | 8.2 | 7.5 | F | R |
| 10 | 10.0 | 8.8 | 8.3 | F | F |
| 11 | 10.5 | 9.3 | 9.1 | F | 1 |
| 12 | 11.0 | 10.0 | 9.8 | 1 | 0 |
| 13 | 11.5 | 10.5 | 10.3 | 1 | R |
| 14 | 12.0 | 11.0 | 11.0 | 1 | F |
| 15 | 12.3 | 11.8 | 11.6 | 1 | 1 |

(1) CLK_EQ, D0_EQ, D1_EQ, and D2_EQ registers determine the receiver EQ setting in I2C mode.
(2) When CTLEBYP_EN = 1 and DCGAIN = 0dB, EQ settings 0 will be 0dB due to the CTLE is bypassed.

### 表 7-7. CTLE HDMI Datarate Map A, B, and C

| HDMI Mode | Map A | Map B | Map C |
|---|---|---|---|
| 1.4 | 12Gbps CTLE | 3Gbps CTLE | 6Gbps CTLE |
| 2.0 | 12Gbps CTLE | 6Gbps CTLE | 6Gbps CTLE |
| 3Gbps FRL | 12Gbps CTLE | 3Gbps CTLE | 6Gbps CTLE |
| 6Gbps FRL | 12Gbps CTLE | 6Gbps CTLE | 6Gbps CTLE |
| 8Gbps FRL | 12Gbps CTLE | 12Gbps CTLE | 12Gbps CTLE |
| 10Gbps FRL | 12Gbps CTLE | 12Gbps CTLE | 12Gbps CTLE |
| 12Gbps FRL | 12Gbps CTLE | 12Gbps CTLE | 12Gbps CTLE |

### 表 7-8. Pin-strap Mode CTLE HDMI Datarate Mapping

| | Sampled State of CTLEMAP_SEL pin | | | |
|---|---|---|---|---|
| | "0" | "R" | "F" | "1" |
| **CTLE HDMI Datarate Map** | Map B | Map C | Map B | Map A |

备注

The clock lane EQ when operating in HDMI 1.4 or 2.0 will use the 3Gbps CTLE and will be set to the zero EQ setting.

### 7.2.9 CTLE Bypass

The TMDS1204 will operate as a buffer when CTLE bypass is enabled. In pin-strap mode, this feature is disabled. In $I^2C$ mode, this feature is enabled when CTLEBYP_EN = 1h and GLOBAL_DCG = 2h. Any lane that has EQ setting of 0h will operate in CTLE bypass.

### 7.2.10 Adaptive Equalization in HDMI 2.1 FRL

The TMDS1204 supports adaptive equalization (AEQ) for HDMI 2.1 FRL. It does not support AEQ for HDMI 1.4 or 2.0. In HDMI 1.4 and HDMI 2.0 modes, TMDS1204 will use the sampled state of the EQ[1:0] pins or value programmed into the register. The AEQ is supported in some pin-strap modes as well as in I$^2$C mode. In I$^2$C mode, AEQ can be enabled by setting the AEQ_EN register. The TMDS1204 adaptation algorithm scans through available equalization settings searching for a setting for which the incoming high-speed signal is not over equalized.

The TMDS1204 will perform adaptive equalization when FRL link training begins. It will also re-adapt each time the data rate changes. The adaption will only occur during the TXFFE0 portion of FRL link training when LTP5, LTP6, LTP7, or LTP8 is being received. The TMDS1204 adaption will complete within $t_{AEQ\_DONE}$ from the time FRL link training begins. If the sink requests additional TXFFE levels (TXFFE1, 2, or 3), then the TMDS1204 will keep its equalizer settings fixed at the value adapted during TXFFE0. If for some reason the FRL link training fails and transitions to legacy mode (HDMI 1.4 or HDMI 2.0), then the EQ [1:0] pins sample the EQ settings that the TMDS1204 switches to if in pin-strap mode or programmed into the register (if in I2C mode).

The TMDS1204 will keep OUT_D[2:0] and OUT_CLK disabled until after adaptation completes. After adaptation completes, the appropriate lanes will be enabled. In I$^2$C mode, this behavior can be overridden by clearing the AEQ_TX_DELAY_EN field.

**表 7-9. Adaptive Equalization Enable and Disable**

| | CTLEMAP_SEL pin level | | | |
|---|---|---|---|---|
| **MODE pin level** | **0** | **R** | **F** | **1** |
| **0** | AEQ disabled | AEQ disable | AEQ disabled | AEQ disabled |
| **R** | AEQ disabled | AEQ disabled | AEQ enabled | AEQ enabled |
| **F** | I$^2$C register | I$^2$C register | I$^2$C register | I$^2$C register |
| **1** | AEQ disabled | AEQ disabled | AEQ enabled | AEQ enabled |

---

备注

The AEQ operates only on IN_D0 pins (pins 12 and 13). The EQ value determined by AEQ will be applied to the other FRL data lanes.

---

#### *7.2.10.1 HDMI 2.1 TX Compliance Testing with AEQ Enabled*

Care must be taken when performing HDMI 2.1 TX compliance testing with AEQ enabled. Because the TMDS1204 will only adapt to LTP5 through 8 during the TXFFE0 part of link training, it is important the test equipment initiate a FRL link training before performing any TX measurements, especially TX eye and jitter measurement. After completion of FRL link training, the test equipment can then switch the current pattern (LTP5, LTP6, LTP7, or LTP8) to the desired test pattern (LTP1, LTP2, LTP3, or LTP4). If the test equipment request LTP1, LTP2, LTP3, or LTP4 before initiating link training, the TMDS1204 will use the sampled state of EQ[1:0] pins.

The following HDMI 2.1 TX tests use LTP5, LTP6, LTP7, and LTP8 as the required pattern for the measurement: HFR1-1, HFR1-2, HFR1-4, HFR1-7, and HFR1-8. If the TMDS1204 AEQ adaption has not completed and instead uses sampled state of EQ[1:0] pins, then it is possible these tests may fail or inaccurately represent system performance.

### 7.2.11 HDMI 2.1 Link Training Compatible Rx EQ

This mode is recommended in source applications in which the GPU is unaware of the TMDS1204 presence and will adjust its transmitter levels (VOD, de-emphasis, and pre-shoot) during HDMI 2.1 FRL link training. This mode is only supported if the TMDS1204 is enabled for limited redriver. 表 7-10 lists the TXFFE levels that this mode assumes the GPU is using.

This feature is supported in I$^2$C mode and all pin-strap modes with the exception of MODE = "0".

In HDMI 2.1 with AEQ disabled, the TMDS1204 will initially set the RX EQ based on the EQ0 and EQ1 pins. The pins determine what value will be used when the TXFFE0 is snooped during FRL link training. 表 7-11 lists how TMDS1204 uses the EQ setting for each increase in TXFFE level (TXFFE1, 2, or 3) from the sampled state of the EQ [1:0] pins.

When HDMI 2.1 with AEQ is enabled, the TMDS1204 will adapt during the TXFFE0 portion of FRL link training. 表 7-11 lists how TMDS1204 uses the EQ setting for each increase in TXFFE level (TXFFE1, 2, or 3) from the adapted EQ value.

**表 7-10. Recommended GPU FRL TXFFE Levels**

| GPU FRL TXFFE Levels | Pre-Shoot (dB) | De-Emphasis (dB) |
|---|---|---|
| TXFFE0 | 2.18 | −3.10 |
| TXFFE1 | 2.50 | −4.43 |
| TXFFE2 | 2.92 | −6.02 |
| TXFFE3 | 3.52 | −7.96 |

**表 7-11. Link Training Compatible RX EQ Adjustments**

| Initial EQ Setting from sampled state of EQ[1:0] pins or adapted EQ value | EQ Setting Used for TXFFE1 | EQ Setting Used for TXFFE2 | EQ Setting Used for TXFFE3 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 2 | 1 | 0 | 0 |
| 3 | 1 | 0 | 0 |
| 4 | 2 | 1 | 0 |
| 5 | 2 | 1 | 0 |
| 6 | 3 | 1 | 0 |
| 7 | 3 | 1 | 0 |
| 8 | 4 | 2 | 1 |
| 9 | 5 | 3 | 1 |
| 10 | 6 | 4 | 1 |
| 11 | 7 | 5 | 1 |
| 12 | 8 | 6 | 2 |
| 13 | 9 | 7 | 3 |
| 14 | 10 | 8 | 4 |
| 15 | 11 | 9 | 5 |

### 7.2.12 Input Signal Detect

When standby is enabled and swap is disabled, the TMDS1204 waits for a signal on either IN_CLK (if HDMI 1.4 or 2.0) or IN_D2 (if HDMI 2.1). When standby is enabled and swap is enabled, the TMDS1204 looks for a signal on either IN_CLK (if HDMI 2.1) or IN_D2 (if HDMI 1.4 or 2.0). The TMDS1204 is fully functional when a signal is detected. If no signal is detected, then the device reenters standby state waiting for a signal again. In the standby state, all of the TMDS outputs are in high-Z status. In both pin-strap mode and I$^2$C mode, standby is enabled by default. In I$^2$C mode, standby can be disabled by setting the STANDBY_DISABLE register mode.

#### *7.2.12.1 SIGDET_OUT Indicator*

When standby state is enabled, the TMDS1204 will assert the SIGDET_OUT pin low whenever the TMDS1204 exits the standby state and will de-assert it when entering power down or standby state. If used, the SIGDET_OUT requires an external pull-up resistor of 10-kΩ or greater.

### 7.2.13 Main Link Outputs

#### *7.2.13.1 Transmitter Bias*

The TMDS1204 transmitter supports both external (DC-coupled) and internal bias (AC-coupled) to a receiver. Selection between DC and AC-coupled is done through use of the AC_EN pin in pin-strap mode and TX_AC_EN register in I$^2$C mode. The AC_EN pin informs the TMDS1204 whether or not an external AC-coupling capacitor is present. When AC_EN is greater than VIH, then TMDS1204 transmitters are internally biased to approximately $V_{CC}$. For DisplayPort, HDMI 2.1 FRL AC-coupled, or any other AC-coupled application, the AC_EN pin should be connected to greater than VIH and an external AC-coupling capacitor should be placed on each of the OUT_D[2:0] pins and the OUT_CLK pin. If the AC_EN pin is connected to less than VIL, then the AC_EN pin will inform TMDS1204 that AC_EN pin is DC-coupled (externally biased) to the far-end HDMI compliant receiver.

---

备注

图 7-3 shows that if using AC-coupled TX mode (AC_EN = high) in an HDMI source application, then an external 499 Ω pull-down to GND must be placed on each OUT pin (OUT_D2:0p/n and OUT_CLKp/n) between the AC-coupling capacitor and the HDMI receptacle. The purpose of the 499 Ω resistor is to set the common mode voltage to HDMI compliant levels.

---

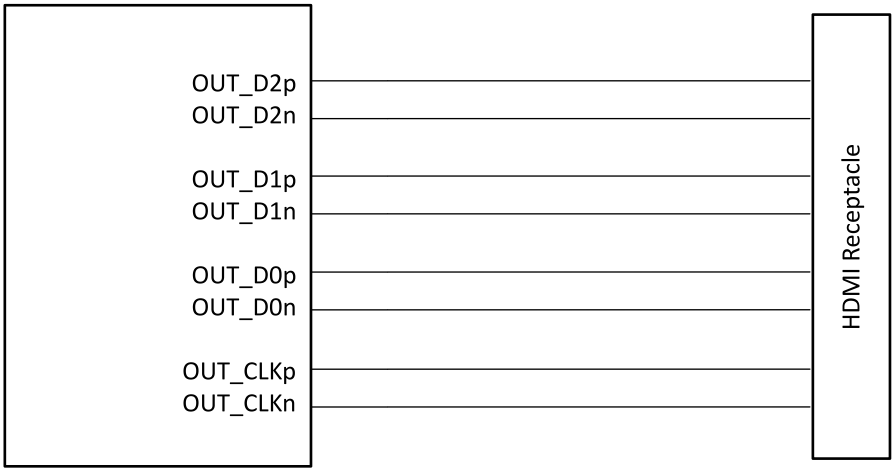

**图 7-2. DC-Coupled TX in HDMI Source Application (AC_EN = Low). External ESD is Not Shown.**

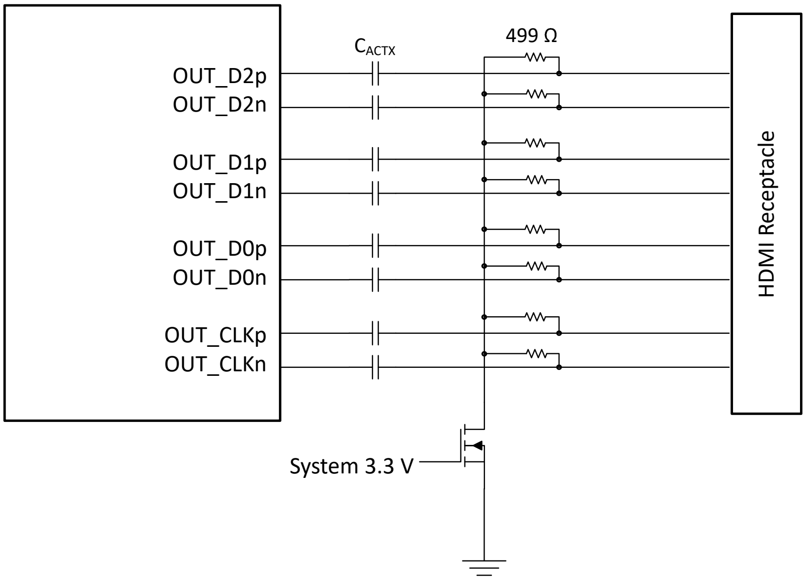

**图 7-3. AC-Coupled TX in HDMI Source Application (AC_EN = High). External ESD is Not Shown.**

#### *7.2.13.2 Transmitter Impedance Control*

HDMI 2.0 standards require a source termination impedance approximately 100 Ω for data rates > 3.4Gbps. HDMI 1.4b requires no source termination but has a provision for termination for higher data rates greater than 1.65Gbps. Enabling this termination is optional. 表 7-13 lists how the TMDS1204 terminations are controlled automatically when in pin strap mode. Depending on the MODE pin, the CFG0 pin can be used to select the HDMI 1.4 termination between open and 300 Ω .

The TMDS1204 supports automatic selection between open and 300 Ω termination when operating in HDMI 1.4. In pin-strap mode with CTL0 low, the TMDS1204 will enable open termination when HDMI clock frequency is less than $f_{HDMI14\_open}$ and will enable 300 Ω termination when HDMI clock frequency is greater than $f_{HDMI14\_300}$. TXTERM_AUTO_HDMI14 register controls this feature in I2C mode.

In $I^2C$ mode, termination is controlled through the registers as provided in 表 7-12.

**表 7-12. Source Termination Control in I2C mode**

| TX_AC_EN Register | TERM Register | TXTERM_AUTO_HDMI14 Register | Source Termination |
|---|---|---|---|
| 0 | 00 | X | None |
| 0 | 01 | X | Parallel ≅ 300 Ω across P and N |
| 0 | 10 | X | Automatic. HDMI 2.0 or HDM 2.1. parallel ≅ 100 Ω across P and N |
| 0 | 10 | 1 | Automatic. HDMI 1.4. parallel ≅ 300 Ω across P and N |
| 0 | 10 | 0 | Automatic. HDMI 1.4. No termination if HDMI clock frequency is ≤ $f_{HDMI14\_open}$. |
| 0 | 10 | 0 | Automatic. HDMI 1.4. Parallel ≅ 300 Ω across P and N termination if HDMI clock frequency is ≥ $f_{HDMI14\_300}$. |
| 0 | 11 | X | Parallel ≅ 100 Ω across P and N |
| 1 | 00 | X | ≅ 150 Ω to supply ($V_{CC}$) on both P and N |
| 1 | 01 | X | ≅ 150 Ω to supply ($V_{CC}$) on both P and N |
| 1 | 10 | X | Automatic. ≅ 150 Ω to supply ($V_{CC}$) on both P and N for HDMI 1.4. Otherwise ≅ 50 Ω to supply ($V_{CC}$) on both P and N. |

**表 7-12. Source Termination Control in I2C mode （续）**

| TX_AC_EN Register | TERM Register | TXTERM_AUTO_HDMI14 Register | Source Termination |
|---|---|---|---|
| 1 | 11 | X | ≅ 50 Ω to supply ($V_{CC}$) on both P and N |

**表 7-13. Automatic Source Termination Control in Pin-Strap Mode**

| HDMI Mode | AC_EN pin | Source Termination |
|---|---|---|
| HDMI 1.4 | 0 | None or parallel ≅ 300 Ω across P and N depending on state of SCL/CFG0 pin |
| HDMI 2.0 | 0 | Parallel ≅ 100 Ω across P and N |
| HDMI 1.4 | 1 | ≅ 150 Ω to supply ($V_{CC}$) on both P and N |
| HDMI 2.0 | 1 | ≅ 50 Ω to supply ($V_{CC}$) on both P and N |

### *7.2.13.3 TX Slew Rate Control*

The TMDS1204 has the ability to slow down the TMDS output edge rates. In pin-strap mode, the TX slew rate can not be controlled. In I$^2$C mode, both clock and data lanes slew rate can be controlled from a register. 表 7-14 lists the supported settings for each slew rate register based on HDMI data rate. The TMDS1204 must be configured in limited redriver mode to control the TX slew rate.

**表 7-14. I$^2$C Mode TX Slew Register Supported Settings**

| HDMI Datarate | SLEW_CLK Register | SLEW_3G Register | SLEW_6G Register | SLEW_8G10G12G Register |
|---|---|---|---|---|
| HDMI 1.4 | 3'b000 through 3'b011 | 3'b010 through 3'b101 | N/A | N/A |
| HDMI 2.0 | 3'b000 through 3'b011 | N/A | 3'b011 through 3'b110 | N/A |
| HDMI 2.1 3Gbps FRL | N/A | 3'b010 through 3'b101 | N/A | N/A |
| HDMI 2.1 6Gbps FRL | N/A | N/A | 3'b011 through 3'b110 | N/A |
| HDMI 2.1 8Gbps FRL | N/A | N/A | N/A | 3'b100 through 3'b111 |
| HDMI 2.1 10Gbps FRL | N/A | N/A | N/A | 3'b110 through 3'b111 |
| HDMI 2.1 12Gbps FRL | N/A | N/A | N/A | 3'b111 |

### *7.2.13.4 TX Pre-Emphasis and De-Emphasis Control*

The TMDS1204 provides pre-emphasis and de-emphasis on the data lanes allowing the output signal pre-conditioning to offset interconnect losses between the TMDS1204 outputs and a TMDS receiver. Pre-emphasis and de-emphasis is not implemented on the clock lane unless the TMDS1204 is in HDMI 2.1 FRL mode and at which time the clock lane becomes a data lane. There are two methods to implement pre-emphasis, pin strapping or through I$^2$C programming. TX pre-emphasis and de-emphasis control is only supported in limited mode.

When using pin strap mode, the TXPRE pin controls four different global pre-emphasis and de-emphasis values for all data lanes when TMDS1204 is operating in HDMI 1.4 or HDMI 2.0. 表 7-15 lists these pre-emphasis and de-emphasis values. In HDMI 2.1 FRL mode, the de-emphasis value used is based on the DDC TXFFE snooped value. 表 7-16 lists how the TMDS1204 uses the de-emphasis level for each TX FFE level.

**表 7-15. Pin-Strap TXPRE Pin Function**

|  | LINEAR_EN pin = "0" |  |  | LINEAR_EN pin = "F" or "1" | LINEAR_EN pin = "R" |
|---|---|---|---|---|---|
| **TXPRE pin** | **HDMI 1.4 or HDMI 2.0** | **HDMI 2.1 FRL TXFF0 Level** | **AEQ ADJUSTMENT** | **AEQ ADJUSTMENT** | **AEQ ADJUSTMENT** |
| 0 | 3.5dB pre-emphasis | Refer to 表 7-16. | 0 | +1 | 0 |
| R | -2.5dB de-emphasis | Refer to 表 7-16. | 0 | +4 | 0 |
| F | 0dB | Refer to 表 7-16. | 0 | 0 | 0 |

表 7-15. Pin-Strap TXPRE Pin Function （续）

| | LINEAR_EN pin = "0" | | | LINEAR_EN pin = "F" or "1" | LINEAR_EN pin = "R" |
|---|---|---|---|---|---|
| **TXPRE pin** | **HDMI 1.4 or HDMI 2.0** | **HDMI 2.1 FRL TXFF0 Level** | **AEQ ADJUSTMENT** | **AEQ ADJUSTMENT** | **AEQ ADJUSTMENT** |
| 1 | 6.0dB pre-emphasis | Refer to 表 7-16 | 0 | +2 | 0 |

表 7-16. HDMI 2.1 FRL TX FFE Levels

| FRL TX FFE Snooped Level | De-Emphasis (dB) |
|---|---|
| TXFFE0 | -2.5 |
| TXFFE1 | -3.5 |
| TXFFE2 | -3.7 |
| TXFFE3 | -4.6 |

### *7.2.13.5 TX Swing Control*

The TMDS1204 transmitter swing level can be adjusted in both pin strap and $I^2C$ mode. In $I^2C$ mode, TX swing settings are controlled independently for each lane (both clock and data) through registers.

In I2C mode, the TX swing used when operating in HDMI 1.4 and HDMI 2.0 can be independently controlled through HDMI14_VOD and HDMI20_VOD registers.

表 7-17 lists how the TXSWG pin adjusts the default 1000mV swing in pin strap mode with limited redeliver mode enabled. In HDMI 1.4 the TXSWG controls the swing for both the data and clock lanes. In HDMI 2.0, the TXSWG pin controls the data lanes while the clock lane will remain at the default value. In HDMI 2.1, the TXSWG pin controls data and clock lanes.

In pin-strap mode with linear enabled, the linearity range is fixed at the highest level (1200mVpp) and therefore TXSWG pin is not used. In $I^2C$ mode, the linearity range can be adjusted from a register.

表 7-17. Pin Strap TXSWG Control

| TXSWG pin | Limited Mode for HDMI 1.4 | Limited Mode for HDMI 2.0 | Limited Mode for HDMI 2.1 | Linear Mode |
|---|---|---|---|---|
| 0 | Default (1000mVpp) | Default (1000mVpp) | Default + 10% | 1200mVpp |
| R | Default − 5% | Default − 5% | Default − 5% | 1200mVpp |
| F | Default (1000mVpp) | Default (1000mVpp) | Default (1000mVpp) | 1200mVpp |
| 1 | Default (1000mVpp) | Default + 5% | Default + 5% | 1200mVpp |

### *7.2.13.6 Fan-out Buffer*

In some applications the HDMI clock and data must be on separate paths. The TMDS1204 implements a fan-out buffer feature to support such applications. When the fan-out buffer feature is enabled, the TMDS1204 will output the HDMI clock on RCLKOUTp/n when operating in HDMI 1.4 or HDMI 2.0. The OUT_CLKp/n will be disabled. When operating in HDMI 2.1 FRL mode, the TMDS1204 will output FRL data3 on OUT_CLKp/n. RCLKOUTp/n will be disabled.

The feature is enabled in pin-strap mode when MODE pin = "R" or it can be enable through FANOUT_EN register when TMDS1204 is configured for $I^2C$ mode.

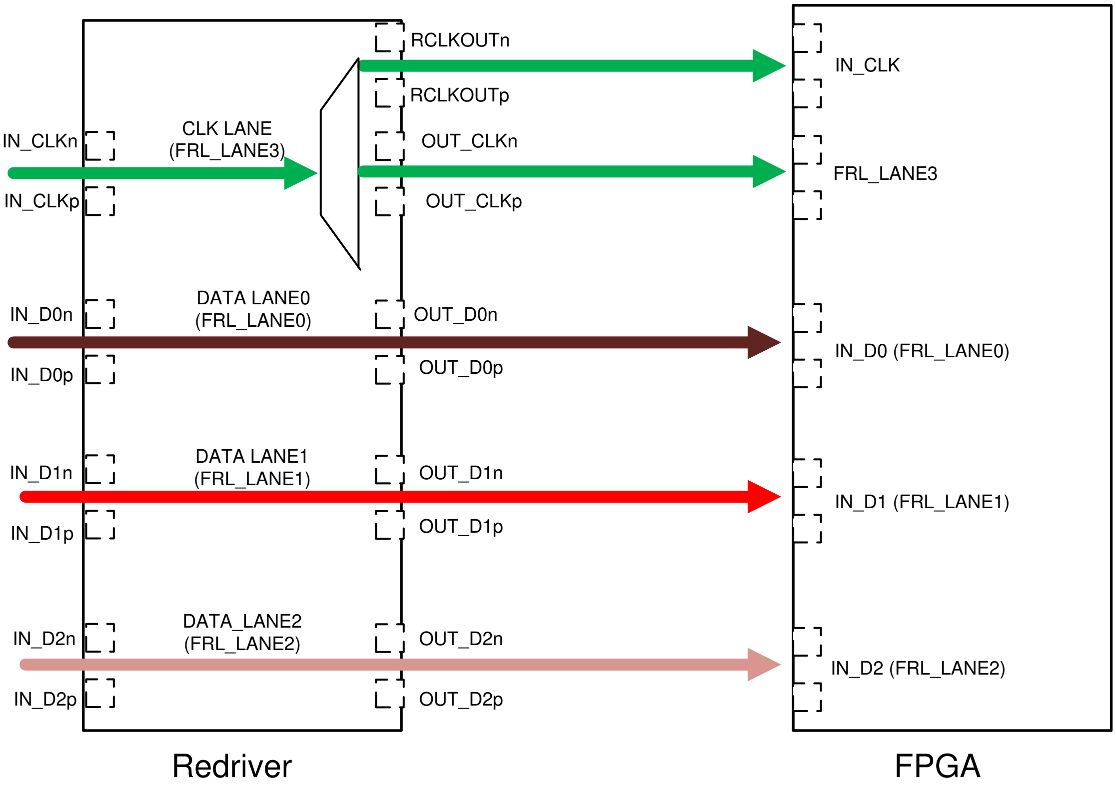

图 7-4. Fan-Out Buffer

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备注

Fan-out buffer feature will be disabled if SWAP is enabled.

---

### 7.2.14 HDMI DDC Capacitance

The HDMI specification limits the DDC bus capacitance to ≤ 50-pF for both an HDMI source and sink. Therefore, care must be taken to make sure the total capacitance of all components (TMDS1204, FR4 trace, ESD, source, and sink) is less than 50-pF.

If implementing a DDC level shifter using pass gates, then the total capacitance will include all components between source or sink and the HDMI receptacle. These components include and are not limited to Source or Sink, the FR4 trace, ESD components, and TMDS1204.

---

备注

Trace capacitance can be in the range of 2 to 5-pF per inch. A general rule is a 50 Ω FR4 trace will be around 3.3-pF per inch.

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### 7.2.15 DisplayPort

The TMDS1204 supports DisplayPort at datarates up to 8.1Gbps (HBR3) when configured for either pin-strap and I$^2$C mode. In pin-strap mode, DisplayPort mode is enabled as provided in 表 7-18. In I$^2$C mode, DisplayPort mode is enabled when FRL_RATE field (offset 0x31) is programmed to 0x6, RATE_SNOOP_CTRL (offset 0xA bit 2) is disabled, and TXFFE_SNOOP_CTLE (offset 0xA bits 1:0) is disabled.

备注

The TMDS1204 must be configured as a linear redriver when enabled for DisplayPort mode. The linear range should be programmed to highest level (Dx_VOD = 0x3 and CLK_VOD = 0x3). The TMDS1204 TX termination must be set to 100Ω (TERM = 0x3) and TX bias must be set to ac-coupled (TX_AC_EN = 0x1).

## 7.3 Device Functional Modes

### 7.3.1 MODE Control

The MODE pin provides four modes of operation. There are three pin-strap modes and one $I^2C$ mode. In all three pin strap modes, DDC snooping feature is enabled. In $I^2C$ mode, DDC snoop feature is enabled by default but can be disabled by a register.

#### *7.3.1.1 $I^2C$ Mode (MODE = "F")*

In $I^2C$ mode, all settings of the TMDS1204 can be controlled through the registers. The TMDS1204 7-bit I2C address is determined by the ADDR/EQ0 pin. All other 4-level and 2-level pins are not used in $I^2C$ mode since the functions exist in a register. The SCL/CFG0 pin will function as the $I^2C$ clock and the SDA/CFG1 pin will function as the $I^2C$ data.

The TMDS1204 defaults to power down in $I^2C$ mode. Upon completion of initialization of the TMDS1204, software must clear the PD_EN field to exit the power down state. The HPD_OUT pin will be asserted low while the PD_EN register is set.

The TMDS1204 supports 1.2V, 1.8V, and 3.3V $I^2C$ signaling levels. Selection of 1.2V, 1.8V, or 3.3V is determined by the VIO pin as provided in 表 7-2.

#### *7.3.1.2 Pin Strap Modes*

表 7-18 and 表 7-19 lists how the SCL/CFG0 and the SDA/CFG1 pins will be used to control the HDMI 1.4 termination, lane SWAP function, and the DisplayPort mode in pin-strap mode.

**表 7-18. SCL/CFG0 Pin in Pin-Strap Mode**

| SCL/CFG0 Pin | AC_EN Pin | TMDS1204 Function |
|---|---|---|
| 0 | 0 | HDMI 1.4 termination is open if HDMI clock frequency ≤ $f_{HDMI14\_open}$ |
| 0 | 0 | HDMI 1.4 termination is ≅300 Ω if HDMI clock frequency ≥ $f_{HDMI14\_300}$ |
| 1 | 0 | HDMI 1.4 termination is ≅300 Ω |
| 0 | 1 | Normal HDMI. Function determined by MODE pin. |
| 1 | 1 | DisplayPort mode. DDC snoop disabled. All four lanes enabled when HPD_IN is high. 12Gbps CTLE used. |

**表 7-19. SDA/CFG1 Pin in Pin-Strap Mode**

| SDA/CFG1 Pin | TMDS1204 Function |
|---|---|
| 0 | Normal Lane ordering |
| 1 | Lane Swap enabled |

备注

The SCL/CFG0 is the only two-level pin that is continuously sampled in pin-strap mode. AC_EN, HPDOUT_SEL, and SDA/CFG1 will not be continuously sampled in pin-strap mode unless indicated otherwise.

The TMDS1204 must be configured as a linear redriver when operating in DisplayPort mode.

#### 7.3.1.2.1 Pin-Strap: HDMI 1.4 and HDMI 2.0 Functional Description

The TMDS1204 will always use the sampled state of EQ[1:0] pins when operating in either HDMI 1.4 and HDMI 2.0. The amount of EQ applied is determined by the CTLE Map used (for more information, refer to 节 7.2.8).

If TMDS1204 is configured for limited redriver mode, then the OUT_D[2:0] and OUT_CLKP/N levels will be fixed based on the sampled state of TXSWG pin (表 7-17 provides more information) and TXPRE pin (表 7-15 provides more information).

If TMDS1204 is configured for linear redriver mode, then OUT_D[2:0] and OUT_CLK will be a linear function of the input signals.

备注

In source application, it is recommended to use limited redriver mode for both HDMI 1.4 and HDMI 2.0.

#### 7.3.1.2.2 Pin-Strap HDMI 2.1 Function (MODE = "0"): Fixed Rx EQ)

In this mode, the TMDS1204 will operate with a fixed RX EQ based on the value set by EQ0 and EQ1 pins.

As listed in 表 7-16, the outputs will be fixed to TXFFE0 in HDMI 2.1 FRL with limited redriver enabled. These outputs will not change based on the snooped value of TXFFE. This configuration is intended to be used in sink applications where the channel between sink and TMDS1204 is fixed.

备注

Adaptive EQ is not supported in this mode (for more information refer to 节 7.2.10). Link Training Compatible Rx EQ is not supported in this mode (for more information, refer to 节 7.2.11).

#### 7.3.1.2.3 Pin-Strap HDMI 2.1 Function (Mode = "1"): Flexible Rx EQ

In this mode, the TMDS1204 supports both Adaptive EQ (AEQ) (for more information, refer to 节 7.2.10) and Link Training Compatible Rx EQ (for more information, refer to 节 7.2.11).

If TMDS1204 is configured for limited redriver mode, the OUT_D[2:0] and OUT_CLK VOD level will be fixed based on the sampled state of TXSWG (表 7-17 provides more information). As provided in 表 7-16, the outputs will be fixed to TXFFE0 in HDMI 2.1 FRL. These outputs will not change based on the snooped value of TXFFE.

#### 7.3.1.2.4 Pin-Strap HDMI 2.1 Function (Mode = "R"): Flexible Rx EQ and Fan-Out Buffer

This pin strap mode is the same as MODE ="1"except that the Fan-Out buffer is supported.

As shown in 图 7-4, the fan-out buffer feature is supported in this mode. The TMDS1204 will output HDMI clock on RCLKOUTp/n when operating in HDMI 1.4 and HDMI 2.0, and OUT_CLKp/n will be disabled in HDMI 1.4 and HDMI 2.0. In HDMI 2.1 FRL mode, the RCLKOUTp/n will be disabled and FRL data lane 3 will be the output through the TMDS1204 clock lane.

备注

Fan-out buffer feature will be disabled if SWAP is enabled. In this pin strap mode, it is recommended to configure TMDS1204 in linear redriver mode.

### 7.3.2 DDC Snoop Feature

As part of discovery the source reads the sink E-EDID information to understand the sink’s capabilities. Part of this read is HDMI Forum Vendor Specific Data Block (HF-VSDB) located at target address 0xA8. From the LV_DDC_SDA and LV_DDC_SCL pins, the TMDS1204 DDC snoop function will monitor both reads and writes to specific offsets of the Status and Control Data Channel Structure (SCDCS) located within the HF-VSDB. The following SCDCS offsets are monitored: Update Flags at offset 10h, TMDS Configuration at offset 20h, Sink Configuration at offset 31h, Source Test Configuration at offset 35h, and Status Flags located at offsets 41h and 42h. The DDC snoop function resides on the LV_DDC_SDA and LV_DDC_SCL pins.

The TMDS1204 has similar SCDCS registers within its register space. Through TMDS1204 local I$^2$C interface, external microprocessor can control TMDS1204 to perform all the necessary functions required for each HDMI type.

#### *7.3.2.1 HDMI Type*

表 7-20 lists the TMDS1204 monitors offsets 20h and 31h to determine HDMI type as either HDMI 1.4, HDMI 2.0, or HDMI 2.1 FRL.

**表 7-20. HDMI Type Selection**

| HDMI Type | TMDS_CLK_RATIO SCDCS Offset 20h[1] | FRL_RATE SCDCS Offset 31h[3:0] |
|---|---|---|
| HDMI 1.4 (TMDS x10) | 0 | 0h |
| HDMI 2.0 (TMDS x40) | 1 | 0h |
| HDMI 2.1 FRL | X | Not 0h |

备注

TMDS1204 will default to HDMI 1.4 following a power-on reset or whenever it enters the power down state. Upon exiting standby, the TMDS1204 will hold data rate value (HDMI 1.4, 2.0, or 2.1) prior to entering the standby.

#### *7.3.2.2 HDMI 2.1 FRL Snoop*

In HDMI 2.1 FRL mode, the TMDS1204 monitors offset 31h, 35h, 41h, and 42h. Each offset contains information that the TMDS1204 uses during FRL link training or during TX compliance testing.

Offset 31h contains FRL lane count (3 or 4 lanes), data rate (3, 6, 8, 10, or 12Gbps), and maximum TXFFE levels supported. TMDS1204 enables the appropriate number of lanes based on the lane count. The TMDS1204 uses the data rate information to determine the duration of the TXFFE de-emphasis. The maximum number of supported TXFFE levels sets the number of TXFFE levels TMDS1204 uses during FRL link training. 表 7-16 lists the TMDS1204 does support all four possible TXFFE levels (TXFFE0 through TXFFE3).

Values snooped from offset 35h is used by TMDS1204 during TX FFE compliance testing.

### 7.3.3 Low Power States

The TMDS1204 has two low power states: Power Down and Standby. 表 7-21 lists both lower power states. Power down is entered when HPD_IN is low for $t_{HPD\_PWRDOWN}$ or in I$^2$C if PD_EN bit is set. Power down is also entered when the EN pin is low. The TMDS1204 will exit power down to the standby state when HPD_IN is high for $t_{HPD\_STANDBY}$.

The TMDS1204 implements a two stage standby power process when HPD_IN is high.

Stage 1: if there is no signal (electrical idle) on the IN_CLK lane, and if HDMI 1.4/2.0 or IN_D2 if HDMI 2.1, then the TMDS1204 will enter Standby State within $t_{STANDBY\_ENTRY}$.

Stage 2: if a signal is detected which last longer than $t_{SIGDET\_DB}$, then TMDS1204 will declare a valid signal and exit standby within $t_{STANDY\_EXIT}$.

- If a signal is detected, then the TMDS1204 will go into normal active operation and signals present at IN_CLK and IN_D[2:0] inputs will be passed through to the OUT_CLK and OUT_D[2:0] outputs.
- If it is determined that no signal is present, then the TMDS1204 will reenter stage 1.

The TMDS1204 will exit standby state and immediately enter active state if LTP1, LTP2, LTP3, or LTP4 is snooped while monitoring status flags at SCDCS offset 41h or 42h.

The TMDS1204 will exit normal operation and return to the standby state within $t_{STANDBY\_ENTRY}$ anytime electrical idle is detected.

**表 7-21. Power States**

| | **INPUTS** | | | | | **STATUS** | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **EN pin** | **HPD_IN pin** | **STANDBY_DISABLE register** | **HPD_PWRDWN_DISABLE register** | **PD_EN register** | **HDMI 1.4/2.0: IN_CLK pin HDMI 2.1: IN_D2 pins** | **HPD_OUT pin** | **IN_Dx pins** | **SDA/SCL** | **OUT_Dx OUT_CLK** | **DDC** | **State** |
| L | X | X | X | X | X | High-Z | High-Z | Disabled | High-Z | Disabled | Power Down State |
| H | L | X | 0 | 0 | X | L | High-Z | Active | High-Z | Disabled | Power Down State |
| H | X | X | X | 1 | X | L | High-Z | Active | High-Z | Disabled | Power Down State |
| H | H | 1 | X | 0 | X | HPD_IN | All RX Active | Active | TX Active | Active | Normal operation |
| H | X | 1 | 1 | 0 | X | H | All RX Active | Active | TX Active | Active | Normal operation |
| H | H | 0 | X | 0 | No signal | HPD_IN | HDMI 1.4/2.0: IN_CLK Active HDMI 2.1: IN_D2 Active | Active | High-Z | Active | Standby State (Squelch waiting) |
| H | H | 0 | X | 0 | Valid signal detected | HPD_IN | All RX Active | Active | TX Active | Active | Normal operation |
| H | X | 0 | 1 | 0 | No signal | H | HDMI 1.4/2.0: IN_CLK Active HDMI 2.1: IN_D2 Active | Active | High-Z | Active | Standby State (Squelch waiting) |
| H | X | 0 | 1 | 0 | Valid signal detected | H | All RX Active | Active | TX Active | Active | Normal operation |

## 7.4 Programming

### 7.4.1 Pseudocode Examples

These are examples of configuring TMDS1204 when it is configured for I2C mode.

#### *7.4.1.1 HDMI 2.1 Source Example with DDC Snoop Disabled and DDC Buffer Disabled*

When using an external discrete DDC buffer with snooping disabled, this example can be used. In this example, adaptive EQ for HDMI 2.1 is disabled. Also, this example assumes the source only wants to support TXFFE0 level when operating in HDMI 2.1 FRL mode.

This example will initialize the following:

- Limited redriver mode with DC-coupled output
- TX slew rate for each data rate
- CTLE used for each data rate

```
// (address, data)
// Initial power-on configuration.
(0x0A, 0x05), // Rate snoop disabled and TXFFE controlled by 35h, 41h, and 42h
(0x0B, 0x23), // 3G and 6G tx slew rate control
(0x0C, 0x70), // HDMI clock and 8G10G12G TX slew rate control
(0x0E, 0x97), // HDMI 1.4, 2.0 and 2.1 CTLE selection
(0x11, 0x00), // Disable all four lanes.
(0x09, 0x00), // Take out of PD state. Should be done after initialization is complete.

// Selection between HDMI modes (1.4, 2.0, and 2.1)
switch (HDMI_MODE) {
    case 'HDMI14_165' : // HDMI 1.4 configuration for less than 1.65Gbps
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x20), // Limited mode, DC-coupled TX, 0dB DCG, Term open, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x00), // Disable FRL
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI14_340' : // HDMI 1.4 configuration for greater than 1.65Gbps
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x21), // Limited mode, DC-coupled TX, 0dB DCG, Term 300, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x00), // Disable FRL
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI20' :  // HDMI 2.0 configuration
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x02), // Set TMDS_CLK_RATIO
        (0x31, 0x00), // Disable FRL
```

```
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_3G' : // HDMI 2.1 3Gbps FRL
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x01), // Set to 3G FRL. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_6G_3lane' : // HDMI 2.1 6Gbps FRL 3 lanes
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x00), // Clock lane EQ.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x02), // Set to 6G FRL and 3 lanes. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_6G_4lane' : // HDMI 2.1 6Gbps FRL 4 lanes
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x0Y), // Clock lane EQ. Set to "Y" to desired value.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x03), // Set to 6G FRL and 4 lanes. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_8G' : //HDMI 2.1 8Gbps FRL
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x0Y), // Clock lane EQ. Set "Y" to desired value.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x04), // Set to 8G FRL and 4 lanes. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_10G' : //HDMI 2.1 10Gbps FRL
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x0Y), // Clock lane EQ. Set "Y" to desired value.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x05), // Set to 10G FRL and 4 lanes. Only TXFFE0 supported.
```

```
        (0x11, 0x0F), // Enable all four lanes.
        break;
    case 'HDMI21_12G' : //HDMI 2.1 12Gbps FRL
        (0x11, 0x00), // Disable all four lanes.
        (0x0D, 0x23), // Limited mode, DC-coupled TX, 0dB DCG, Term 100, disable CTLE bypass
        (0x12, 0x03), // Clock lane VOD and TXFFE
        (0x13, 0x0Y), // Clock lane EQ. Set "Y" to desired value.
        (0x14, 0x03), // D0 lane VOD and TXFFE.
        (0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
        (0x16, 0x03), // D1 lane VOD and TXFFE.
        (0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
        (0x18, 0x03), // D2 lane VOD and TXFFE.
        (0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
        (0x20, 0x00), // Clear TMDS_CLK_RATIO
        (0x31, 0x06), // Set to 12G FRL and 4 lanes. Only TXFFE0 supported.
        (0x11, 0x0F), // Enable all four lanes.
        break;
}
```

#### *7.4.1.2 Sink Example*

This example assumes TMDS1204 transmitters are DC-coupled to the HDMI sink. In this example, TMDS1204 will be configured for linear mode with adaptive EQ enabled and TMDS1204 will automatically determine HDMI data rate by snooping DDC traffic between the HDMI source and sink.

```
// (address, data)
// Initial power-on configuration.
(0x0A, 0x00), // Rate snoop and TXFFE snoop enabled.
(0x0B, 0x23), // 3G and 6G slew rate control
(0x0C, 0x00), // HDMI clock tx slew rate control
(0x0D, 0xA3), // Linear mode, DC-coupled TX, 0dB DCG, Term fixed at 100Ω, disable CTLE bypass
(0x0E, 0x97), // HDMI14, 2.0 and 2.1 CTLE selection
(0x12, 0x03), // Clock lane VOD and TXFFE
(0x13, 0x00), // Clock lane EQ.
(0x14, 0x03), // D0 lane VOD and TXFFE.
(0x15, 0x0Y), // D0 lane EQ. Set "Y" to desired value.
(0x16, 0x03), // D1 lane VOD and TXFFE.
(0x17, 0x0Y), // D1 lane EQ. Set "Y" to desired value.
(0x18, 0x03), // D2 lane VOD and TXFFE.
(0x19, 0x0Y), // D2 lane EQ. Set "Y" to desired value.
(0x1E, 0x40), // Enable AEQ
(0x09, 0x00), // Take out of PD state. Should be done after initialization is complete.
```

### 7.4.2 TMDS1204 I$^2$C Address Options

For further programmability, the TMDS1204 can be controlled using I$^2$C. The SCL/CFG0 and SDA/CFG1 terminals are used for I$^2$C clock and I$^2$C data respectively.

**表 7-22. TMDS1204 I$^2$C Device Address Description**

| ADDR/EQ0 pin | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (W/R) | HEX |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0/1 | BC/BD |
| R | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0/1 | BA/BB |
| F | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0/1 | B8/B9 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0/1 | B6/B7 |

### 7.4.3 I$^2$C Target Behavior

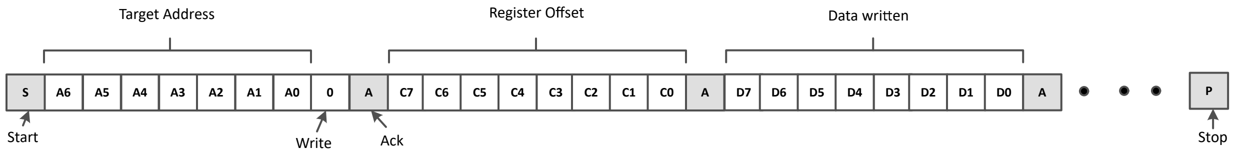


**图 7-5. I$^2$C Write with Data**

The following procedure should be followed to write data to TMDS1204 $I^2C$ registers (refer to 图 7-5):

1. The controller initiates a write operation by generating a start condition (S), followed by the TMDS1204 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TMDS1204 acknowledges the address cycle.
3. The controller presents the register offset within TMDS1204 to be written, consisting of one byte of data, MSB-first.
4. The TMDS1204 acknowledges the sub-address cycle.
5. The controller presents the first byte of data to be written to the $I^2C$ register.
6. The TMDS1204 acknowledges the byte transfer.
7. The controller may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TMDS1204.
8. The controller terminates the write operation by generating a stop condition (P).

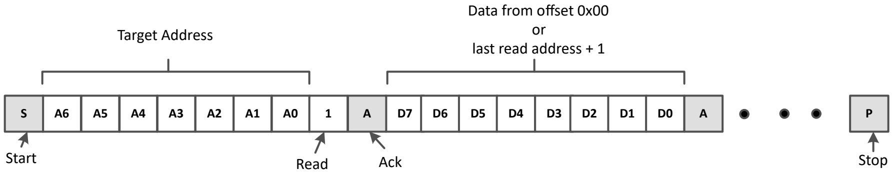


图 7-6. I2C Read Without Repeated Start

The following procedure should be followed to read the TMDS1204 $I^2C$ registers without a repeated Start (refer to 图 7-6).

1. The controller initiates a read operation by generating a start condition (S), followed by the TMDS1204 7-bit address and a zero-value “W/R” bit to indicate a read cycle.
2. The TMDS1204 acknowledges the 7-bit address cycle.
3. Following the acknowledge the controller continues sending clock.
4. The TMDS1204 transmit the contents of the memory registers MSB-first starting at register 00h or last read register offset+1. If a write to the $I^2C$ register occurred prior to the read, then the TMDS1204 shall start at the register offset specified in the write.
5. The TMDS1204 waits for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the $I^2C$ controller acknowledges reception of each data byte transfer.
6. If an ACK is received, then the TMDS1204 transmits the next byte of data as long as controller provides the clock. If a NAK is received, then the TMDS1204 stops providing data and waits for a stop condition (P).
7. The controller terminates the write operation by generating a stop condition (P).

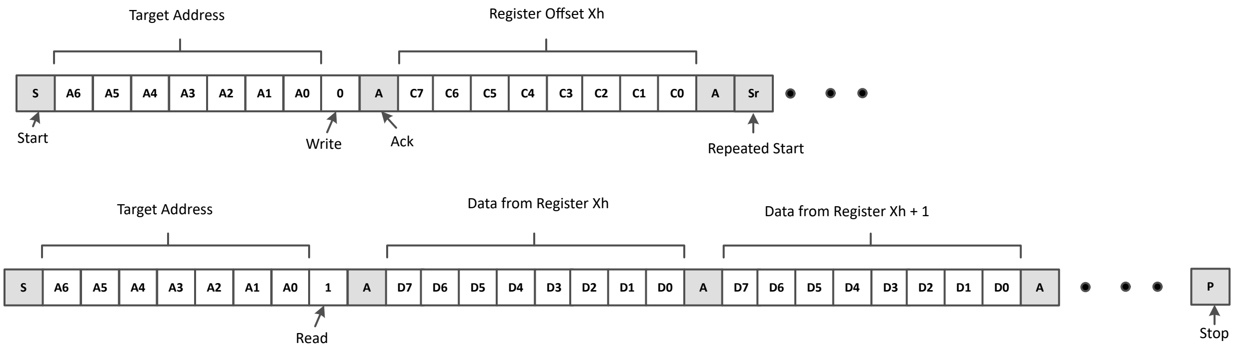


图 7-7. I2C Read with Repeated Start

The following procedure should be followed to read the TMDS1204 $I^2C$ registers with a repeated Start (refer to 图 7-7).

1. The controller initiates a read operation by generating a start condition (S), followed by the TMDS1204 7-bit address and a zero-value “W/R” bit to indicate a write cycle.

2. The TMDS1204 acknowledges the 7-bit address cycle.
3. The controller presents the register offset within TMDS1204 to be written, consisting of one byte of data, MSB-first.
4. The TMDS1204 acknowledges the register offset cycle.
5. The controller presents a repeated start condition (Sr).
6. The controller initiates a read operation by generating a start condition (S), followed by the TMDS1204 7-bit address and a one-value “W/R” bit to indicate a read cycle.
7. The TMDS1204 acknowledges the 7-bit address cycle.
8. The TMDS1204 transmit the contents of the memory registers MSB-first starting at the register offset.
9. The TMDS1204 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the controller after each byte transfer; the I$^2$C controller acknowledges reception of each data byte transfer.
10. If an ACK is received, then the TMDS1204 transmits the next byte of data as long as controller provides the clock. If a NAK is received, then the TMDS1204 stops providing data and waits for a stop condition (P).
11. The controller terminates the read operation by generating a stop condition (P).

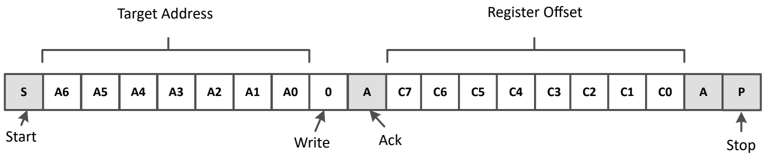


**图 7-8. I2C Write Without Data**

The following procedure should be followed for setting a starting sub-address for I$^2$C reads (refer to 图 7-8).

1. The controller initiates a write operation by generating a start condition (S), followed by the TMDS1204 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TMDS1204 acknowledges the address cycle.
3. The controller presents the register offset within TMDS1204 to be written, consisting of one byte of data, MSB-first.
4. The TMDS1204 acknowledges the register offset cycle.
5. The controller terminates the write operation by generating a stop condition (P).

备注

图 7-6 that if no register offset is included for the read procedure after initial power-up, then reads start at register offset 00h and continue byte by byte through the registers until the I2C controller terminates the read operation. During a read operation, the TMDS1204 auto-increments the I$^2$C internal register address of the last byte transferred independent of whether or not an ACK was received from the I2C controller.

## 7.5 Register Maps

### 7.5.1 TMDS1204 Registers

表 7-23 lists the memory-mapped registers for the TMDS1204 registers. All register offset addresses not listed in 表 7-23 should be considered as reserved locations and the register contents should not be modified.

**表 7-23. TMDS1204 Registers**

| Offset | Acronym | Register Name | Section |
|---|---|---|---|
| 8h | REV_ID | Revision ID | Go |
| 9h | PD_RST | Power Down and Reset control | Go |
| Ah | MISC_CONTROL | Misc Control | Go |
| Bh | GBL_SLEW_CTRL | Global TX Slew control for data lanes in HDMI1.4 and 2.0 | Go |
| Ch | GBL_SLEW_CTRL2 | Global TX Slew control for data and clock | Go |
| Dh | GBL_CTRL1 | Global control | Go |

表 7-23. TMDS1204 Registers （续）

| Offset | Acronym | Register Name | Section |
|---|---|---|---|
| Eh | GBL_CTLE_CTRL | Global CTLE control | Go |
| 11h | LANE_ENABLE | Lane enables | Go |
| 12h | CLK_CONFIG1 | CLK lane TX swing and FFE control | Go |
| 13h | CLK_CONFIG2 | CLK lane RX EQ control | Go |
| 14h | D0_CONFIG1 | D0 lane TX swing and FFE control | Go |
| 15h | D0_CONFIG2 | D0 lane RX EQ control | Go |
| 16h | D1_CONFIG1 | D1 lane TX swing and FFE control | Go |
| 17h | D1_CONFIG2 | D1 lane RX EQ control | Go |
| 18h | D2_CONFIG1 | D2 lane TX swing and FFE control | Go |
| 19h | D2_CONFIG2 | D2 lane RX EQ control | Go |
| 1Ah | SIGDET_TH_CFG | SIGDET voltage threshold control | Go |
| 1Ch | GBL_STATUS | Global Powerdown and Standby Status | Go |
| 1Dh | AEQ_CONTROL1 | Adaptive EQ control1 | Go |
| 1Eh | AEQ_CONTROL2 | Adaptive EQ control2 | Go |
| 20h | SCDC_TMDS_CONFIG | SCDC TMDS Clock Ratio | Go |
| 31h | SCDC_SINK_CONFIG | SCDC SNK FRL FFE and Rate | |
| 35h | SCDC_SRC_TEST | SCDC Test | Go |
| 41h | SCDC_STATUS10 | Lanes 0 and 1 FRL Training Status | Go |
| 42h | SCDC_STATUS32 | Lanes 2 and 3 FRL Training Status | Go |
| 50h | AEQ_STATUS | Adaptive EQ Status | Go |
| 51h | AEQ_STATUS2 | Adaptive EQ Status | Go |

Complex bit access types are encoded to fit into small table cells. 表 7-24 shows the codes that are used for access types in this section.

表 7-24. TMDS1204 Access Type Codes

| Access Type | Code | Description |
|---|---|---|
| **Read Type** | | |
| R | R | Read |
| RH | R<br>H | Read<br>Set or cleared by hardware |
| **Write Type** | | |
| W | W | Write |
| W1S | W<br>1S | Write<br>1 to set |
| WtoPH | W<br>toPH | Write<br>Pulse high |
| **Reset or Default Value** | | |
| -*n* | | Value after reset or the default value |

### 7.5.1.1 REV_ID Register (Offset = 8h) [Reset = 03h]

REV_ID is shown in 表 7-25.

Return to the Summary Table.

表 7-25. REV_ID Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | REV_ID | RH | 3h | Device revision. |

### 7.5.1.2 PD_RST Register (Offset = 9h) [Reset = 01h]

PD_RST is shown in 表 7-26.

Return to the Summary Table.

表 7-26. PD_RST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SOFT_RST | WtoPH | 0h | Writing a 1 to this field resets all fields |
| 6 | SCDC_SOFT_RST | WtoPH | 0h | Writing a 1 to this field resets the fields in the SCDC registers 20h, 31h, 35h, 41h and 42h. |
| 5 | RESERVED | R | 0h | Reserved |
| 4 | RESERVED | R/W | 0h | Reserved |
| 3 | RESERVED | R | 0h | Reserved |
| 2 | HPD_PWRDWN_DISABLE | R/W | 0h | Mode to ignore HPD pin and always enter active state unless PD_EN is high<br>0h = Automatically enter power down based on HPD_IN<br>1h = Always remain in active state or Standby |
| 1 | STANDBY_DISABLE | R/W | 0h | When high, standby state is disabled and the device will immediately enter active state with all lanes enabled when not in power down. When low, the device will enter standby state when exiting power down and wait for incoming data before entering active state.<br>0h = Standby state enabled<br>1h = Standby state disabled |
| 0 | PD_EN | R/W | 1h | I2C power down. Software should clear this field after it has completed initialization. HPD_OUT will be asserted low when this field is set.<br>0h = Normal operation<br>1h = Forced power down by I2C |

### 7.5.1.3 MISC_CONTROL Register (Offset = Ah) [Reset = 08h]

MISC_CONTROL is shown in 表 7-27.

Return to the Summary Table.

表 7-27. MISC_CONTROL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LANE_SWAP | R/W | 0h | This field swaps the input and output lanes.<br>0h = No lanes swapped<br>1h = Both input and output lanes swapped |
| 6 | FANOUT_EN | R/W | 0h | Selects whether or not fan-out buffer feature is enabled or not. When enabled, hardware will enable RCLKOUT when operating in HDMI1.4 and HDMI2.0. When operating in HDMI 2.1 mode, OUT_CLK will be enabled for FRL lane 3.<br>0h = Fan-out buffer feature disabled.<br>1h = Fan-out buffer feature enabled. |
| 5 | RX_TERM_DISABLE | R/W | 0h | When set will disable Rx termination.<br>0h = Enabled when HPD_IN high.<br>1h = Disable |
| 4 | HPD_OUT_SEL | R/W | 0h | Selects whether HPD_OUT is push/pull or open-drain.<br>0h = Push Pull<br>1h = Open Drain |

表 7-27. MISC_CONTROL Register Field Descriptions （续）

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3 | EQ_SNOOP_CTRL | R/W | 1h | Control whether Rx EQ is adjusted in response to snooped TXFFE when TXFFE snooping is enabled through registers 41h and 42h.<br>0h = Rx EQ automatically adjusted for TXFFE<br>1h = Rx EQ is fixed |
| 2 | RATE_SNOOP_CTRL | R/W | 0h | Control snooping of HDMI rates. When snooping is disabled, correct HDMI rate must be written through I2C to registers 20h and 31h.<br>0h = Snooping enabled<br>1h = Snooping disabled |
| 1-0 | TXFFE_SNOOP_CTRL | R/W | 0h | Control snooping of TXFFE<br>0h = DDC snooping through registers 35h, 41h and 42h<br>1h = DDC snooping disabled. TXFFE controlled through I2C writes to 35h, 41h and 42h<br>2h = DDC snooping disabled. TXFFE controlled through writes to CLK_TXFFE, D0_TXFFE, D1_TXFFE, and D2_TXFFE<br>3h = DDC snooping disabled. TXFFE controlled through writes to CLK_TXFFE, D0_TXFFE, D1_TXFFE, and D2_TXFFE |

#### 7.5.1.4 GBL_SLEW_CTRL Register (Offset = Bh) [Reset = 34h]

GBL_SLEW_CTRL is shown in 表 7-28.

Return to the Summary Table.

表 7-28. GBL_SLEW_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0h | Reserved |
| 6-4 | SLEW_3G | R/W | 3h | Field controls slew rate for HDMI 1.4 data lane and HDMI 2.1 3Gbps FRL data lanes.<br>0h = slowest edge rate<br>7h = fastest edge rate |
| 3 | RESERVED | R | 0h | Reserved |
| 2-0 | SLEW_6G | R/W | 4h | Field controls slew rate for HDMI 2.0 data lanes and HDMI 2.1 6Gbps FRL data lanes.<br>0h = slowest edge rate<br>7h = fastest edge rate |

#### 7.5.1.5 GBL_SLEW_CTRL2 Register (Offset = Ch) [Reset = 71h]

GBL_SLEW_CTRL2 is shown in 表 7-29.

Return to the Summary Table.

表 7-29. GBL_SLEW_CTRL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0h | Reserved |
| 6-4 | SLEW_8G10G12G | R/W | 7h | Field controls slew rate for data lanes for 8Gbps, 10Gbps and 12Gbps FRL datarates<br>0h = slowest edge rate<br>7h = fastest edge rate |
| 3 | RESERVED | R | 0h | Reserved |
| 2-0 | SLEW_CLK | R/W | 1h | Field control slew rate of clock lane in HDMI 1.4b and HDMI 2.0 modes.<br>0h = slowest edge rate<br>7h = fastest edge rate |

### 7.5.1.6 GBL_CTRL1 Register (Offset = Dh) [Reset = 22h]

GBL_CTRL1 is shown in 表 7-30.

Return to the Summary Table.

表 7-30. GBL_CTRL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | GLOBAL_LINR_EN | R/W | 0h | Global control for selecting between linear redriver or limited redriver.<br>0h = Limited<br>1h = Linear |
| 6 | TX_AC_EN | R/W | 0h | Controls selection of ac-coupled or dc-coupled TX termination. When AC-coupled is enabled, 50 Ω termination on both P and N to VCC will be enabled.<br>0h = dc-coupled<br>1h = ac-coupled |
| 5-4 | GLOBAL_DCG | R/W | 2h | CTLE DCGain for all lane.<br>0h = -3dB<br>1h = -3dB<br>2h = 0dB<br>3h = +1dB |
| 3 | TXTERM_AUTO_HDMI14 | R/W | 0h | Selects between no termination and 300 Ωs when TERM = 2h and operating in HDMI1.4.<br>0h = No termination for clock less than or equal to 165MHz and 300 Ω for clock greater than 225MHz<br>1h = 300 Ω |
| 2 | CTLEBYP_EN | R/W | 0h | Selects whether or not CTLE bypass is enabled or not when GLOBAL_DCG is set to 2h and EQ set to 0h.<br>0h = CTLE bypass disabled<br>1h = CTLE bypass enabled |
| 1-0 | TERM | R/W | 2h | TX termination control<br>0h = No termination<br>1h = 300 Ω<br>2h = Automatic based HDMI mode<br>3h = 100 Ω |

### 7.5.1.7 GBL_CTLE_CTRL Register (Offset = Eh) [Reset = 3Fh]

GBL_CTLE_CTRL is shown in 表 7-31.

Return to the Summary Table.

表 7-31. GBL_CTLE_CTRL Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | GLOBAL_CTLEBW | R/W | 0h | CTLE bandwidth control. 0 is lowest and 3h is highest. |
| 5-4 | HDMI14_CTLE_SEL | R/W | 3h | Selects the CTLE used when datarate is HDMI 1.4. Value programmed into this field will apply to data lanes only. Clock lane will always use 3Gbps CTLE.<br>0h = 3Gbps CTLE<br>1h = 6Gbps CTLE<br>2h = Auto select based on snoop datarate<br>3h = 12Gbps CTLE |
| 3-2 | HDMI20_CTLE_SEL | R/W | 3h | Selects the CTLE used when datarate is HDMI 2.0. Value programmed into this field will apply to data lanes only. Clock lane will always use 3Gbps CTLE.<br>0h = 3Gbps CTLE<br>1h = 6Gbps CTLE<br>2h = Auto select based on snoop datarate<br>3h = 12Gbps CTLE |

表 7-31. GBL_CTLE_CTRL Register Field Descriptions （续）

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 1-0 | HDMI21_CTLE_SEL | R/W | 3h | Selects the CTLE used when datarate is HDMI 2.1. Value programmed into this field will apply to all four lanes.<br>0h = 3Gbps CTLE<br>1h = 6Gbps CTLE<br>2h = Auto select based on snoop datarate<br>3h = 12Gbps CTLE |

### 7.5.1.8 LANE_ENABLE Register (Offset = 11h) [Reset = 5Fh]

LANE_ENABLE is shown in 表 7-32.

Return to the Summary Table.

表 7-32. LANE_ENABLE Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | HDMI20_VOD | R/W | 1h | VOD control for limited redriver in HDMI 2.0<br>0h = Use values in CLK_VOD, D0_VOD, D1_VOD and D2_VOD<br>1h = Default (1000mV)<br>2h = Default - 5%<br>3h = Default + 5% |
| 5-4 | HDMI14_VOD | R/W | 1h | VOD control for limited redriver in HDMI 1.4<br>0h = Use values in CLK_VOD, D0_VOD, D1_VOD and D2_VOD<br>1h = Default (1000mV)<br>2h = Default - 5%<br>3h = Default - 10% |
| 3 | CLK_LANE_EN | R/W | 1h | Enable for CLK lane<br>0h = Disabled<br>1h = Enabled |
| 2 | D0_LANE_EN | R/W | 1h | Enable for D0 lane<br>0h = Disabled<br>1h = Enabled |
| 1 | D1_LANE_EN | R/W | 1h | Enable for D0 lane<br>0h = Disabled<br>1h = Enabled |
| 0 | D2_LANE_EN | R/W | 1h | Enable for D0 lane<br>0h = Disabled<br>1h = Enabled |

### 7.5.1.9 CLK_CONFIG1 Register (Offset = 12h) [Reset = 03h]

CLK_CONFIG1 is shown in 表 7-33.

Return to the Summary Table.

表 7-33. CLK_CONFIG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0h | Reserved |
| 6-4 | CLK_TXFFE | R/W | 0h | TXFFE control for CLK lane. This field is only honored in HDMI 2.1.<br>0h = 0.0dB<br>1h = 3.5dB<br>2h = 6.0dB<br>3h = Reserved<br>4h = -1.5dB<br>5h = -2.5dB<br>6h = -3.5dB<br>7h = -4.8dB |
| 3 | RESERVED | R | 0h | Reserved |

表 7-33. CLK_CONFIG1 Register Field Descriptions （续）

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 2-0 | CLK_VOD | R/W | 3h | Differential Swing control for CLK lane.<br>0h = Limited -15% Linear 800mV<br>1h = Limited -10% Linear 900mV<br>2h = Limited - 5% Linear 1000mV<br>3h = Limited 800mV Linear 1200mV<br>4h = Limited +5% Linear Reserved<br>5h = Limited +10% Linear Reserved<br>6h = Limited +15% Linear Reserved<br>7h = Limited +20% Linear Reserved |

#### 7.5.1.10 CLK_CONFIG2 Register (Offset = 13h) [Reset = 00h]

CLK_CONFIG2 is shown in 表 7-34.

Return to the Summary Table.

表 7-34. CLK_CONFIG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0h | Reserved |
| 3-0 | CLK_EQ | R/W | 0h | EQ control for CLK lane. This field is only honored in HDMI 2.1.<br>0h = Min EQ<br>Fh = Max EQ |

#### 7.5.1.11 D0_CONFIG1 Register (Offset = 14h) [Reset = 03h]

D0_CONFIG1 is shown in 表 7-35.

Return to the Summary Table.

表 7-35. D0_CONFIG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0h | Reserved |
| 6-4 | D0_TXFFE | R/W | 0h | TXFFE control for D0 lane.<br>0h = 0.0dB<br>1h = 3.5dB<br>2h = 6.0dB<br>3h = Reserved<br>4h = -1.5dB<br>5h = -2.5dB<br>6h = -3.5dB<br>7h = -4.8dB |
| 3 | RESERVED | R | 0h | Reserved |
| 2-0 | D0_VOD | R/W | 3h | Differential Swing control for D0 lane.<br>0h = Limited -15% Linear 800mV<br>1h = Limited -10% Linear 900mV<br>2h = Limited - 5% Linear 1000mV<br>3h = Limited 1000mV Linear 1200mV<br>4h = Limited +5% Linear Reserved<br>5h = Limited +10% Linear Reserved<br>6h = Limited +15% Linear Reserved<br>7h = Limited +20% Linear Reserved |

#### 7.5.1.12 D0_CONFIG2 Register (Offset = 15h) [Reset = 00h]

D0_CONFIG2 is shown in 表 7-36.

Return to the Summary Table.

表 7-36. D0_CONFIG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0h | Reserved |
| 3-0 | D0_EQ | R/W | 0h | EQ control for D0 lane.<br>0h = Min EQ<br>Fh = Max EQ |

#### 7.5.1.13 D1_CONFIG1 Register (Offset = 16h) [Reset = 03h]

D1_CONFIG1 is shown in 表 7-37.

Return to the Summary Table.

表 7-37. D1_CONFIG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0h | Reserved |
| 6-4 | D1_TXFFE | R/W | 0h | TXFFE control for D1 lane.<br>0h = 0.0dB<br>1h = 3.5dB<br>2h = 6.0dB<br>3h = Reserved<br>4h = -1.5dB<br>5h = -2.5dB<br>6h = -3.5dB<br>7h = -4.8dB |
| 3 | RESERVED | R | 0h | Reserved |
| 2-0 | D1_VOD | R/W | 3h | Differential Swing control for D1 lane.<br>0h = Limited -15% Linear 800mV<br>1h = Limited -10% Linear 900mV<br>2h = Limited - 5% Linear 1000mV<br>3h = Limited 1000mV Linear 1200mV<br>4h = Limited +5% Linear Reserved<br>5h = Limited +10% Linear Reserved<br>6h = Limited +15% Linear Reserved<br>7h = Limited +20% Linear Reserved |

#### 7.5.1.14 D1_CONFIG2 Register (Offset = 17h) [Reset = 00h]

D1_CONFIG2 is shown in 表 7-38.

Return to the Summary Table.

表 7-38. D1_CONFIG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0h | Reserved |
| 3-0 | D1_EQ | R/W | 0h | EQ control for D1 lane<br>0h = Min EQ<br>Fh = Max EQ |

#### 7.5.1.15 D2_CONFIG1 Register (Offset = 18h) [Reset = 03h]

D2_CONFIG1 is shown in 表 7-39.

Return to the Summary Table.

表 7-39. D2_CONFIG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0h | Reserved |
| 6-4 | D2_TXFFE | R/W | 0h | TXFFE control for D2 lane<br>0h = 0.0dB<br>1h = 3.5dB<br>2h = 6.0dB<br>3h = Reserved<br>4h = -1.5dB<br>5h = -2.5dB<br>6h = -3.5dB<br>7h = -4.8dB |
| 3 | RESERVED | R | 0h | Reserved |
| 2-0 | D2_VOD | R/W | 3h | Differential Swing control for D2 lane.<br>0h = Limited -15% Linear 800mV<br>1h = Limited -10% Linear 900mV<br>2h = Limited - 5% Linear 1000mV<br>3h = Limited 1000mV Linear 1200mV<br>4h = Limited +5% Linear Reserved<br>5h = Limited +10% Linear Reserved<br>6h = Limited +15% Linear Reserved<br>7h = Limited +20% Linear Reserved |

#### 7.5.1.16 D2_CONFIG2 Register (Offset = 19h) [Reset = 00h]

D2_CONFIG2 is shown in 表 7-40.

Return to the Summary Table.

表 7-40. D2_CONFIG2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R | 0h | Reserved |
| 3-0 | D2_EQ | R/W | 0h | EQ control for D2 lane.<br>0h = Min EQ<br>Fh = Max EQ |

#### 7.5.1.17 SIGDET_TH_CFG Register (Offset = 1Ah) [Reset = 44h]

SIGDET_TH_CFG is shown in 表 7-41.

Return to the Summary Table.

表 7-41. SIGDET_TH_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0h | Reserved |
| 6-4 | CFG_SIGDET_HYST | R/W | 4h | Controls the SIGDET hysteresis. Value programmed into this field plus value programmed into CFG_SIGDET_VTH field defines the SIGDET assert threshold.<br>0h = 0mV<br>1h = 12mV<br>2h = 25mV<br>3h = 37mV<br>4h = 55mV<br>5h = 63mV<br>6h = 75mV<br>7h = 90mV |
| 3 | RESERVED | R | 0h | Reserved |

表 7-41. SIGDET_TH_CFG Register Field Descriptions （续）

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 2-0 | CFG_SIGDET_VTH | R/W | 4h | Controls the SIGDET de-assert voltage threshold.<br>0h = 58mV<br>1h = 60mV<br>2h = 72mV<br>3h = 84mV<br>4h = 95mV<br>5h = 108mV<br>6h = 120mV<br>7h = 135mV |

### 7.5.1.18 GBL_STATUS Register (Offset = 1Ch) [Reset = 00h]

GBL_STATUS is shown in 表 7-42.

Return to the Summary Table.

表 7-42. GBL_STATUS Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PD_STATUS | RH | 0h | Power Down status |
| 6 | STANDBY_STATUS | RH | 0h | Standby Status |
| 5-0 | RESERVED | R | 0h | Reserved |

### 7.5.1.19 AEQ_CONTROL1 Register (Offset = 1Dh) [Reset = F3h]

AEQ_CONTROL1 is shown in 表 7-43.

Return to the Summary Table.

表 7-43. AEQ_CONTROL1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | FULLAEQ_UPPER_EQ | R/W | Fh | Maximum EQ value to check for full AEQ mode |
| 3-2 | AEQ_PATTERN_CTRL | R/W | 0h | Control how link training pattern snooping for EQ adaptation<br>0h = Require a read of pattern register 41h/42h after a rate change. Allow eq adaptation for patterns 0, 5, 6, 7, and 8.<br>1h = Require a read of pattern register 41h/42h after a rate change. Allow eq adaptation for patterns 5, 6, 7, and 8.<br>2h = Allow eq adaptation for patterns 0, 5, 6, 7, and 8. No need for read after rate change<br>3h = Allow eq adaptation for patterns 5, 6, 7, and 8. No need for read after rate change. |
| 1 | AEQ_START_CTRL | R/W | 1h | Control whether starts based on signal detect or both signal detect and FLT_UPDATE cleared<br>0h = Only require signal detect<br>1h = Require signal detect and clearing of FLT_UPDATE |
| 0 | AEQ_TX_DELAY_EN | R/W | 1h | Control whether TX remains disabled during EQ adaptation<br>0h = TX active during adaptation<br>1h = TX disabled during adaptation |

### 7.5.1.20 AEQ_CONTROL2 Register (Offset = 1Eh) [Reset = 00h]

AEQ_CONTROL2 is shown in 表 7-44.

Return to the Summary Table.

表 7-44. AEQ_CONTROL2 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | AEQ_MODE | R/W | 0h | Selects between two Adaption modes<br>0h = AEQ with hits counted at mideye for every EQ.<br>1h = AEQ with hits counted at mideye only for EQ equal 0. |
| 6 | AEQ_EN | R/W | 0h | Controls whether or not adaptive EQ is enabled.<br>0h = AEQ disabled<br>1h = AEQ enabled |
| 5-4 | RESERVED | R/W | 0h | Reserved |
| 3 | OVER_EQ_SIGN | R/W | 0h | Selects the sign for OVER_EQ_CTRL field.<br>0h = positive<br>1h = negative |
| 2-0 | OVER_EQ_CTRL | R/W | 0h | This field will increase or decrease the AEQ by value programmed into this field. For example, full AEQ value is 6 and this field is programmed to 2 and OVER_EQ_SIGN = 0, then EQ value used will be 8. This field is only used in Full AEQ mode.<br>0h = 0 or -8<br>1h = 1 or -7<br>2h = 2 or -6<br>3h = 3 or -5<br>4h = 4 or -4<br>5h = 5 or -3<br>6h = 6 or -2<br>7h = 7 or -1 |

### 7.5.1.21 SCDC_TMDS_CONFIG Register (Offset = 20h) [Reset = 00h]

SCDC_TMDS_CONFIG is shown in 表 7-45.

Return to the Summary Table.

表 7-45. SCDC_TMDS_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | RESERVED | R | 0h | Reserved |
| 1 | TMDS_CLK_RATIO | RH/W | 0h | TMDS Bit Period to TMDS Clock Period Ratio. Reads last value snooped through DDC read/write or I2C write.<br>0h = 1/10 (HDMI 1.4b)<br>1h = 1/40 (HDMI 2.0) |
| 0 | RESERVED | R | 0h | Reserved |

### 7.5.1.22 SCDC_SINK_CONFIG Register (Offset = 31h) [Reset = 00h]

SCDC_SINK_CONFIG is shown in 表 7-46.

Return to the Summary Table.

表 7-46. SCDC_SINK_CONFIG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | FFE_LEVELS | RH/W | 0h | Indicates the maximum TXFFE level supported for the current FRL rate. Read last value snooped through DDC read/write or I2C write.<br>0h = Only TXFFE0 supported<br>1h = TXFFE0-1 supported<br>2h = TXFFE0-2 supported<br>3h = TXFFE0-3 supported |

表 7-46. SCDC_SINK_CONFIG Register Field Descriptions （续）

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 3-0 | FRL_RATE | RH/W | 0h | Selects FRL rate and lane count. Read last value snooped through DDC read/write or I2C write.<br>0h = Disable FRL<br>1h = 3Gbps on 3 lanes<br>2h = 6Gbps on 3 lanes<br>3h = 6Gbps on 4 lanes<br>4h = 8Gbps on 4 lanes<br>5h = 10Gbps on 4 lanes<br>6h = 12Gbps on 4 lanes |

#### 7.5.1.23 SCDC_SRC_TEST Register (Offset = 35h) [Reset = 00h]

SCDC_SRC_TEST is shown in 表 7-47.

Return to the Summary Table.

表 7-47. SCDC_SRC_TEST Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R | 0h | Reserved |
| 5 | FLT_NO_TIMEOUT | RH/W | 0h | Set by sink test equipment to have source not time out during FRL link training<br>0h = Normal operation<br>1h = Source does not timeout |
| 4 | RESERVED | R | 0h | Reserved |
| 3 | TX_NO_FFE | RH/W | 0h | Test mode to disable FFE. Read last value snooped through DDC read/write or I2C write.<br>0h = Normal TXFFE<br>1h = TX sent with no FFE |
| 2 | TX_DEEMPH_ONLY | RH/W | 0h | Test mode to enable de-emphasis only. Read last value snooped through DDC read/write or I2C write.<br>0h = Normal TXFFE<br>1h = TX sent de-emphasis only |
| 1 | TX_PRESHOOT_ONLY | RH/W | 0h | Test mode to enable pre-shoot only. Read last value snooped through DDC read/write or I2C write.<br>0h = Normal TXFFE<br>1h = TX sent with pre-shoot only |
| 0 | RESERVED | R | 0h | Reserved |

#### 7.5.1.24 SCDC_STATUS10 Register (Offset = 41h) [Reset = 00h]

SCDC_STATUS10 is shown in 表 7-48.

Return to the Summary Table.

表 7-48. SCDC_STATUS10 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | LN1_LTP_REQ | RH/W | 0h | Link training pattern request for lane 1. Reads last value read through DDC or written through I2C. A DDC read/I2C write of Eh advances the current FFE level for this lane saturating at the value of FFE_LEVELS. A DDC read/I2C write of Fh clears for FFE level for all lanes to TXFFE0. |
| 3-0 | LN0_LTP_REQ | RH/W | 0h | Link training pattern request for lane 0. Reads last value read through DDC or written through I2C. A DDC read/I2C write of Eh advances the current FFE level for this lane saturating at the value of FFE_LEVELS. A DDC read/I2C write of Fh clears for FFE level for all lanes to TXFFE0. |

### 7.5.1.25 SCDC_STATUS32 Register (Offset = 42h) [Reset = 00h]

SCDC_STATUS32 is shown in 表 7-49.

Return to the Summary Table.

**表 7-49. SCDC_STATUS32 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | LN3_LTP_REQ | RH/W | 0h | Link training pattern request for lane 3. Reads last value read through DDC or written through I2C. A DDC read/I2C write of Eh advances the current FFE level for this lane saturating at the value of FFE_LEVELS. A DDC read/I2C write of Fh clears for FFE level for all lanes to TXFFE0. |
| 3-0 | LN2_LTP_REQ | RH/W | 0h | Link training pattern request for lane 2. Reads last value read through DDC or written through I2C. A DDC read/I2C write of Eh advances the current FFE level for this lane saturating at the value of FFE_LEVELS. A DDC read/I2C write of Fh clears for FFE level for all lanes to TXFFE0. |

### 7.5.1.26 AEQ_STATUS Register (Offset = 50h) [Reset = 80h]

AEQ_STATUS is shown in 表 7-50.

Return to the Summary Table.

**表 7-50. AEQ_STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | AEQDONE_STAT | RH | 1h | This field is low while AEQ is active and high when it is done. It is valid when FRL training and AEQ_EN = 1 or when FORCE_AEQ_EN = 1 and HW has reset FORCE_AEQ back to 0.<br>0h = AEQ is running<br>1h = AEQ is done |
| 6 | AEQ_HC_OVERFLOW | RH | 0h | 13-bit AEQ hit counter overflow status |
| 5 | RESERVED | R | 0h | Reserved |
| 4 | RXD1_DONE_STAT | RH | 0h | This flag is set after DAC wait timer expires. |
| 3-0 | RXD1_AEQ_STAT | RH | 0h | Optimal EQ determined by FSM after the completion of Full AEQ. This field will include the value programmed into OVER_EQ_CTRL field. |

### 7.5.1.27 AEQ_STATUS2 Register (Offset = 51h) [Reset = 00h]

AEQ_STATUS2 is shown in 表 7-51.

Return to the Summary Table.

**表 7-51. AEQ_STATUS2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0h | Reserved |
| 6-4 | VOD_RANGE_STAT | RH | 0h | VOD range selected by the last AEQ run |
| 3-0 | AEQ_EYE_STAT | RH | 0h | EYE status from the last AEQ run. Relative to the max limit of 15. |

# 8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

TMDS1204 is designed to accept AC or DC-coupled HDMI input signals. The device provides signal conditioning and level shifting functions to drive a compliant HDMI source connector. The device can be used in an HDMI sink application such as monitor or TV. The TMDS1204 can also be used as an DP/HDMI redriver in an embedded application. In many major PC or gaming systems APU/GPU will provide AC-coupled HDMI signals. TMDS1204 is suitable for such platforms.

## 8.1 Application Information

The TMDS1204 features are optimized for sink applications such as TV or monitors, but TMDS1204 can also support source applications such as Blu-ray™ DVD player, gaming system, desktops, and notebooks. The following sections provide design considerations for the various types of applications.

## 8.2 Typical Source-Side Application

图 8-1 shows a schematic representation of what is considered a standard source implementation.

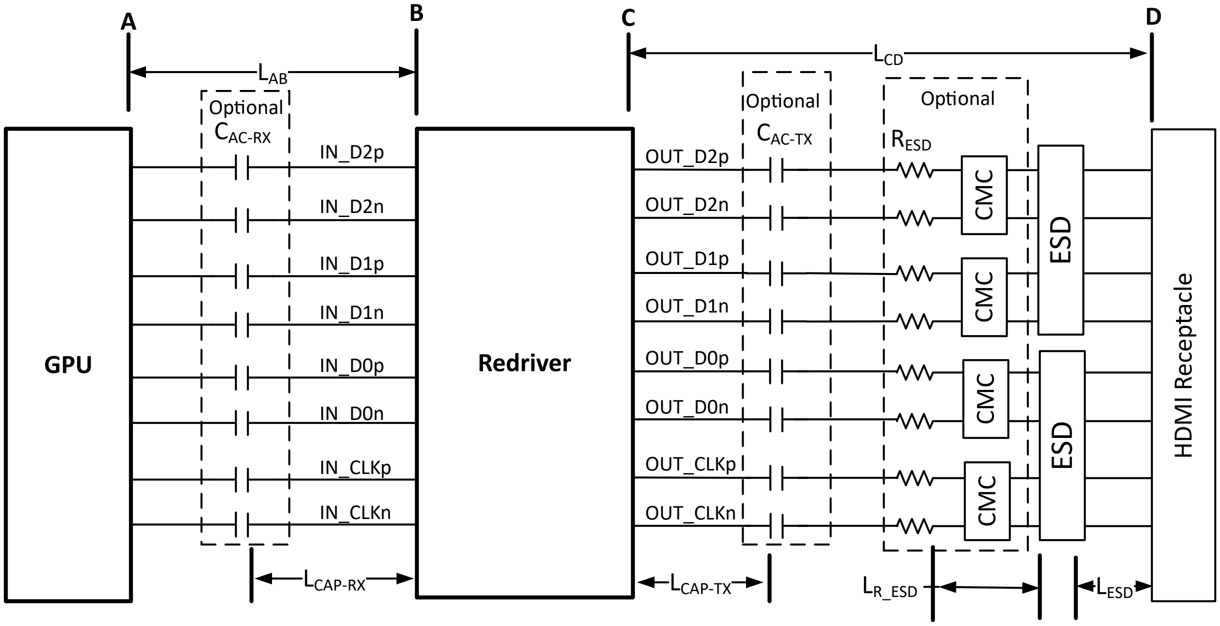


图 8-1. TMDS1204 in Source Side Application

### 8.2.1 Design Requirements

The TMDS1204 can be designed into many different applications. In all the applications there are certain requirements for the system to work properly. The EN pin must have a 0.1-µF capacitor to ground. The processor can drive the EN pin, but the EN pin needs to change states (low to high) after the voltage rails have stabilized. Using $I^2C$ is the best way to configure the device, but pin strapping is also provided as $I^2C$ and is not available in all cases. As sources may have many different naming conventions, it is necessary to confirm that the link between the source and the TMDS1204 are correctly mapped. A Swap function is provided for the input pins in case signaling is reversed between the source and receptacle. 表 8-1 lists information on expected values to perform properly.

For this design example, the TMDS1204 is assumed to be configured for pin-strap mode. If I2C mode is desired, the MODE pin should be set to "F" and software must configure TMDS1204. For how to configure TMDS1204, refer to 节 7.4.1.

表 8-1. Design Parameters

| Design Parameter | Value |
|---|---|
| $V_{CC}$ | 3.3V |
| $V_{IO}$ (1.2V, 1.8V, or 3.3V LVCMOS levels) | 1.8V |
| Maximum HDMI 2.1 FRL Datarate (3, 6, 8, 10, or 12Gbps) | 12Gbps |
| Pin-strap or I2C mode (if I2C, then MODE = "F"). | Pin-strap |
| Pin Strap Mode.(MODE = "0", "R" or "1"). | Mode = "0" (Fixed EQ) |
| DDC Snoop Feature. (Y/N). Required when in pin strap. Optional in I2C mode. | Yes |
| SWAP function (Y / N). In pin strap mode controlled by SDA/CFG1 pin. | Yes. SDA/CFG1 pin = H. |
| HPD_IN to HPD_OUT Level Shifter Support (Y / N) | Yes, HPD_OUT is used. If no, then HPD_OUT can be left floating. |
| Pre-Channel Length (表 8-2 provides the length restrictions) | Length = 8 inches (≅ 7.2dB at 6GHz insertion loss) |
| Post-Channel Length (表 8-2 provides the length restrictions) | Length = 2 inches (≅ 1.8dB at 6GHz insertion loss) |
| Limited or linear redriver mode? | Limited redriver (LINEAR_EN pin = "0"). |
| TX is DC or AC-coupled to HDMI receptacle? | DC-coupled. AC_EN pin = Low. |
| GPU Launch Voltage (500mV to 1200mV) if using limited redriver mode. If using linear redriver mode, then refer to the GPU requirements listed in 表 7-4. | 500mV |
| GPU HDMI 2.1 pre-shoot and de-emphasis levels used if using redriver in limited mode | If MODE = "0" or "R", GPU's TX FFE pre-shoot and de-emphasis levels shall be set to 0dB for all four TXFFE levels<br>If MODE = "1", then GPU TXFFE pre-shoot and de-emphasis levels shall meet the requirements listed in 表 7-4. |
| RX EQ (16 possible values. Value chosen based on pre-channel length). | EQ1 pin: "R"<br>ADDR/EQ0 pin: "R"<br>(7.5dB) |
| TX Pre-emphasis. In pre-strap mode controlled by TXPRE pin. | Default 0dB of pre-emphasis. Float TXPRE pin. |
| TX Swing. In pre-strap mode controlled by TXSWG pin. | Default TX swing level. Float TXSWG pin. |

表 8-2. Source Layout and Component Placement Constraints

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{ESD}$ | External series resistor between ESD component and TMDS1204 | | 0 | | 2.5 | Ω |
| $L_{AB}$ (1) (2) | PCB trace length from GPU to TMDS1204 | At 12Gbps | 1 | | 10 | inches |
| $L_{INTRA\text{-}AB}$ | Intra-pair skew from GPU to TMDS1204 | | | | 5 | mil |
| $L_{CD}$ (1) | PCB trace length from TMDS1204 to receptacle | At 12Gbps | 0.75 | | 2 | inches |
| $L_{INTRA\text{-}CD}$ | Intra-pair skew from TMDS1204 to receptacle | | | | 5 | mil |
| $L_{CAP\text{-}RX}$ | PCB trace length from TMDS1204 to optional external $C_{AC\text{-}RX}$ capacitor | | 0.3 | | | inches |
| $L_{CAP\text{-}TX}$ | PCB trace length from TMDS1204 to optional external $C_{AC\text{-}TX}$ capacitor | | 0.3 | | | inches |
| $L_{ESD}$ | PCB trace length from ESD component to receptacle | | | | 0.5 | inches |
| $L_{R\_ESD}$ | PCB trace length from $R_{ESD}$ to ESD component | | | | 0.25 | inches |
| $L_{INTER\text{-}PAIR}$ (3) | Inter-pair skew between all four channels (D0, D1, D2, and CLK) | | | | 1 | inches |
| $IL_{PCB}$ | PCB trace insertion loss | | 0.1 | | 0.17 | dB / inch /GHz |
| $Z_{PCB\_AB}$ | Differential impedance of $L_{AB}$ | | 75 | | 110 | Ω |
| $Z_{PCB\_CD}$ | Differential impedance of $L_{CD}$ | | 90 | | 110 | Ω |
| $VIA_{AB}$ | Number of vias between GPU and TMDS1204 | | | | 2 | VIA |
| $VIA_{CD}$ | Number of vias between HDMI connector and TMDS1204 | | | | 1 | VIA |
| XTALK | Differential crosstalk between adjacent differential pairs on PCB. | ≦ 3GHz | | | −24 | dB |

(1) Maximum distance assumes PCB trace insertion loss meets $IL_{PCB}$ requirement. If PCB trace insertion loss exceeds the maximum limit, then distance needs be reduced.
(2) Minimum distance assumes PCB trace insertion loss meets $IL_{PCB}$ requirement. If PCB trace insertion loss is less than the minimum limit, then distance needs to be increased.
(3) Calculation of channel length is the sum of $L_{AB}$ and $L_{CD}$.

### 8.2.2 Detailed Design Procedure

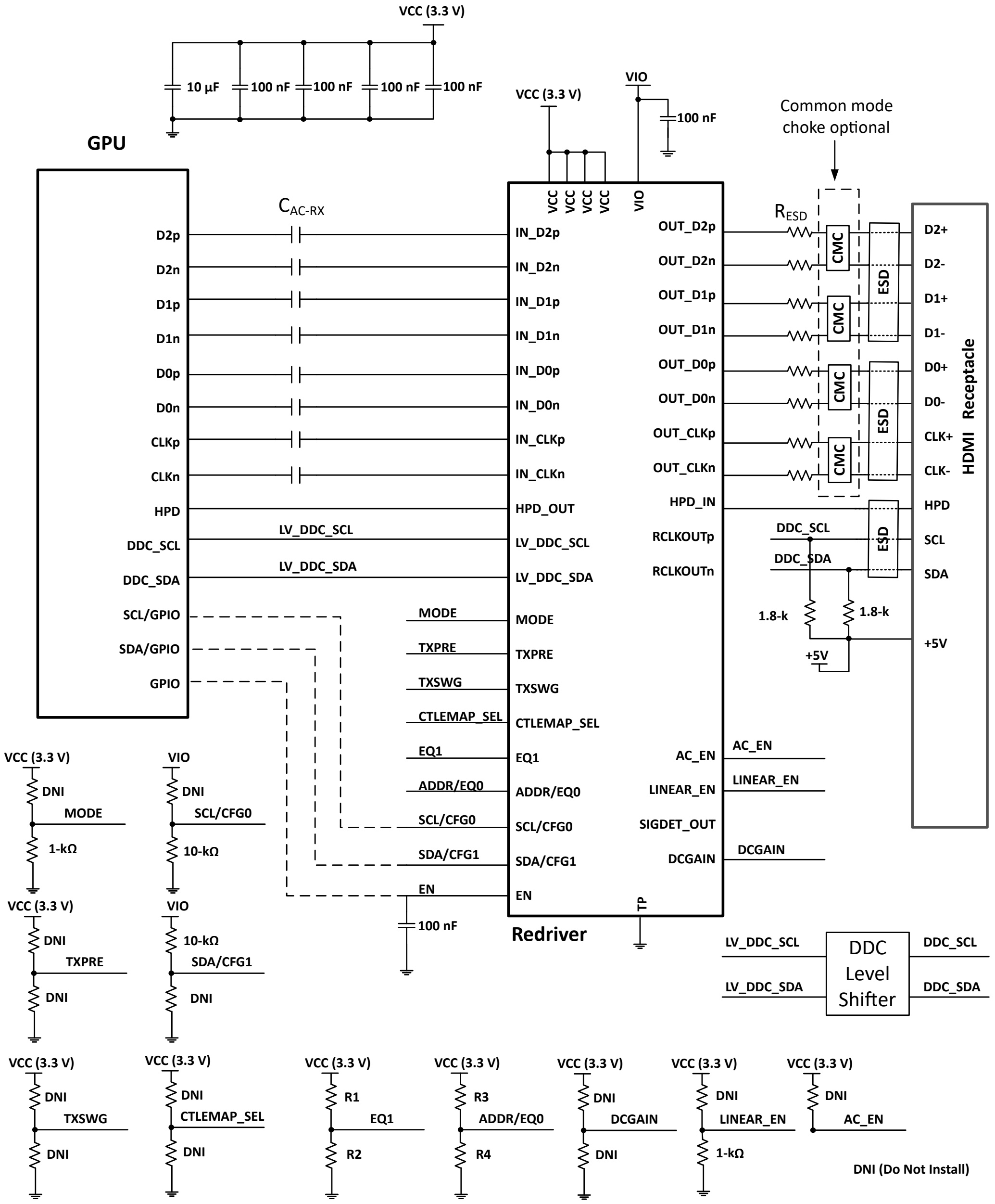


图 8-2. TMDS1204 in Source Application Schematics

#### 8.2.2.1 Pre-Channel ($L_{AB}$)

The TMDS1204 can support up to 12dB at 6GHz of insertion loss. The loss profile between the GPU and the TMDS1204 input (referred to the pre-channel as shown in 图 8-1) should be less than the TMDS1204 maximum receiver equalization. 图 8-3 shows the loss profile of FR4 trace at different lengths. The TMDS1204 EQ0 and EQ1 pins should be configured to match the pre-channel insertion loss. 表 7-6 lists the EQ0 and EQ1 configuration options.

The GPU transmitter differential output voltage swing must be large enough so that the TMDS1204's $V_{ID(DC)}$ and $V_{ID(EYE)}$ requirements are met. The $V_{ID(EYE)}$ is the eye height after the contribution of ISI jitter only. Because a redriver can only compensate for ISI jitter, all non-ISI sources of jitter (random, sinusoidal, and so forth) will be passed through TMDS1204. If the system designer requires the worse case channel length of 10 inches, then the GPU transmitter differential voltage swing without de-emphasis should be at least 1000mVpp to meet the $V_{ID(DC)}$ and $V_{ID(EYE)}$ requirements of the TMDS1204. A GPU transmitter, which incorporates de-emphasis, can meet the requirement with less than 1000mVpp.

#### 8.2.2.2 Post-Channel ($L_{CD}$)

图 8-1 shows the post-channel, which should be 2 inches or less. If ESD devices are used, then it may be necessary to overcome the insertion loss of the ESD device by increasing the TMDS1204 transmitter voltage swing. 表 7-17 lists how this is done by configuring the TXSWG pin to the appropriate value.

If post-channel is greater than 2 inches, then transmitter pre-emphasis may need to be employed. 表 7-15 lists how this is done by configuring the TMDS1204 TXPRE pin to the appropriate setting. Adjusting the TMDS1204 transmitter voltage swing may also be necessary.

#### 8.2.2.3 Common Mode Choke

It may be necessary to incorporate a common mode choke (CMC) to reduce EMI. The purpose of a CMC is to have a minimal impact to the differential signal while attenuating common mode noise thereby reducing radiated emissions. The CMC should be placed between the TMDS1204 and the ESD device.

**表 8-3. Recommended Common Mode Chokes**

| Manufacturer | Part Number |
|---|---|
| Murata | DLM0QSB120HY2 |
| Murata | DLM0NSB120HY2 |
| Murata | NFG0QHB542HS2 |

#### 8.2.2.4 ESD Protection

It may be necessary to incorporate an ESD component to protect the TMDS1204 from electrostatic discharge (ESD). It is recommended that the ESD protection component has a breakdown voltage of ⩾4.5V and a clamp voltage of ⩽4.3V. A clamp voltage greater than 4.3V will require a $R_{ESD}$ on each high-speed differential pin. The ESD component should be placed near the HDMI connector.

**表 8-4. Recommended ESD Protection Component**

| Manufacturer | Part Number |
|---|---|
| NXP | PUSB3FR4 |

### 8.2.3 Application Curves

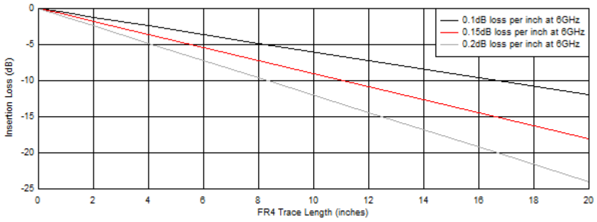


图 8-3. FR4 Trace Insertion Loss at 6GHz

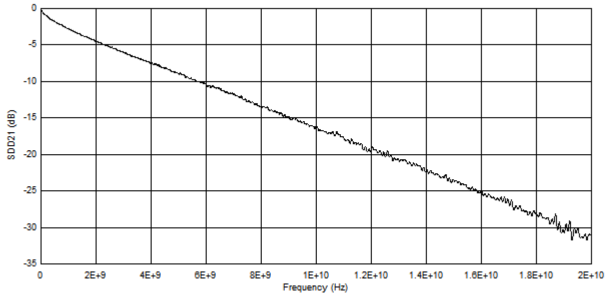


图 8-4. Pre-Channel Insertion Loss at TTP2

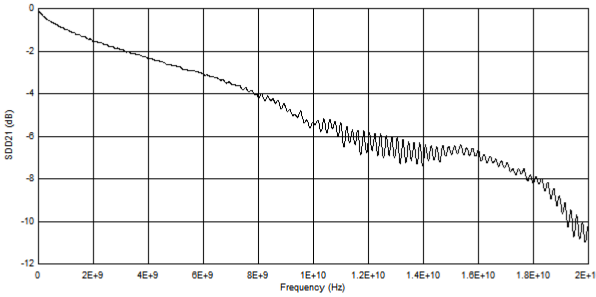


图 8-5. Post-Channel Insertion Loss at TTP4

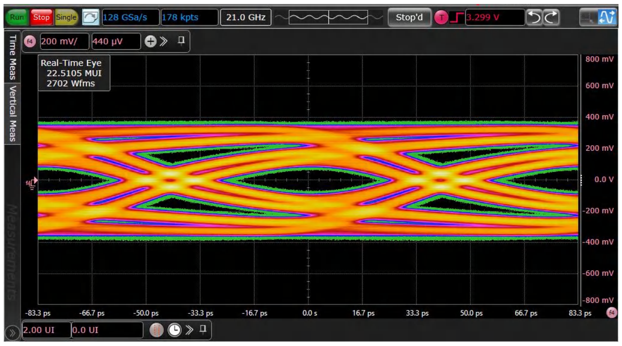


图 8-6. 12Gbps Input Eye at TTP2 After Pre-channel

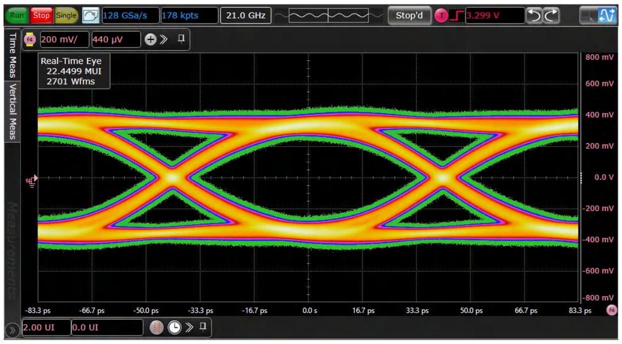


图 8-7. 12Gbps Output Eye at TTP4 After Pre and Post Channels

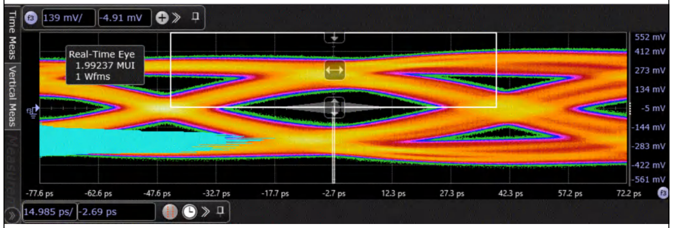


图 8-8. 12Gbps Output Eye at TTP4_EQ After Pre and Post Channels

## 8.3 Typical Sink-Side Application

图 8-9 shows a schematic representation of what is considered a standard sink implementation.

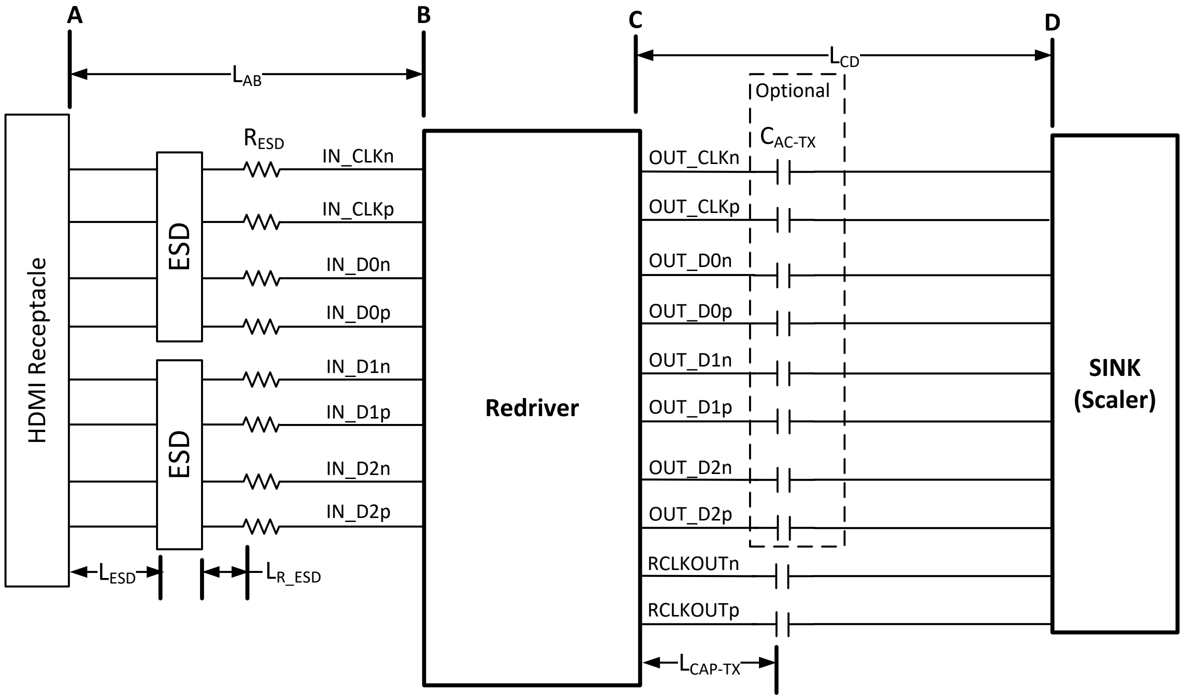


图 8-9. TMDS1204 in Sink Side Application

### 8.3.1 Design Requirements

表 8-5. Design Parameters

| Design Parameter | Value |
|---|---|
| $V_{CC}$ | 3.3V (±5%) |
| $V_{IO}$ (1.2V, 1.8V, or 3.3V LVCMOS levels) | 3.3V |
| Maximum HDMI 2.1 FRL Datarate (6, 8, 10, or 12Gbps) | 12Gbps |
| Pin-strap or I2C mode (if I2C, then MODE = "F"). | Pin-strap |
| Pin Strap Mode.(MODE = "0", "R" or "1"). | Mode = "1" (Adaptive EQ) |
| DDC Snoop Feature. (Y/N). Required when in pin strap. Optional in I2C mode. | Yes |
| SWAP function (Y / N). In pin strap mode controlled by SDA/CFG1 pin. | No. SDA/CFG1 pin = L. |
| HPD_IN to HPD_OUT Level Shifter Support (Y / N) | No, then HPD_OUT can be left floating. |
| Pre-Channel Length (表 8-6 lists the length restrictions) | Length = 1 inches; Width = 4 mil. (≅ 1dB at 6GHz insertion loss) |
| Post-Channel Length (表 8-6 lists the length restrictions) | Length = 6 inches; Width = 4 mil (≅ 6dB at 6GHz insertion loss) |
| Limited or linear redriver mode? | Linear redriver (LINEAR_EN pin = "F") recommended in sink application |
| TX is DC or AC-coupled to HDMI receptacle? | AC-coupled. AC_EN pin = High. |
| RX EQ (16 possible values. Value chosen based on pre-channel length). | EQ1 pin: "0"<br>ADDR/EQ0 pin: "1"<br>(2.7dB) |
| CTLE Map (Map A, Map B or Map C). In pre-strap controlled by CTLEMAP_SEL pin. | For Sink application recommend Map B or C. |
| TX pre-emphasis. In pre-strap mode controlled by TXPRE pin. TX pre-emphasis control not supported in linear redriver mode. | Float TXPRE pin. |
| TX Swing. In pre-strap mode controlled by TXSWG pin. | Default TX swing level. Float TXSWG pin. |

### 表 8-5. Design Parameters （续）

| Design Parameter | Value |
|---|---|
| Fan-out Buffer support (Y / N) | Typically only used with a FPGA. If feature needed in pin-strap mode, then MODE must be set to "R". |

### 表 8-6. Sink Layout and Component Placement Constraints

| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{ESD}$ | External series resistor between ESD component and TMDS1204 | | 0 | | 2.5 | Ω |
| $L_{AB}$ (1) (2) | PCB trace length from receptacle to TMDS1204 | | 0.75 | | 2 | inches |
| $L_{INTRA\text{-}AB}$ | Intra-pair skew from receptacle to TMDS1204 | | | | 2 | mil |
| $L_{CD}$ (1) | PCB trace length from TMDS1204 to sink | | 1 | | 6 | inches |
| $L_{INTRA\text{-}CD}$ | Intra-pair skew from TMDS1204 to sink | | | | 2 | mil |
| $L_{CAP\text{-}TX}$ | PCB trace length from TMDS1204 to external $C_{AC\text{-}TX}$ capacitor | | 0.3 | | | inches |
| $L_{ESD}$ | PCB trace length from ESD component to receptacle | | | | 0.5 | inches |
| $L_{R\_ESD}$ | PCB trace length from $R_{ESD}$ to ESD component | | | | 0.25 | inches |
| $L_{INTER\text{-}PAIR}$ (3) | Inter-pair skew between all four channels (D0, D1, D2, and CLK) | | | | 0.10 | inches |
| $IL_{PCB}$ | PCB trace insertion loss | | 0.1 | | 0.17 | dB / inch /GHz |
| $Z_{PCB\_AB}$ | Differential impedance of $L_{AB}$ | | 90 | | 110 | Ω |
| $Z_{PCB\_CD}$ | Differential impedance of $L_{CD}$ | | 90 | | 110 | Ω |
| $VIA_{AB}$ | Number of vias between receptacle and TMDS1204 | | | | 1 | VIA |
| $VIA_{CD}$ | Number of vias between sink and TMDS1204 | | | | 2 | VIA |
| XTALK | Differential crosstalk between adjacent differential pairs on PCB. | ≦ 3GHz | | | −24 | dB |

(1) Maximum distance assumes PCB trace insertion loss meets $IL_{PCB}$ requirement. If PCB trace insertion loss exceeds the maximum limit, then distance needs to be reduced.
(2) Minimum distance assumes PCB trace insertion loss meets $IL_{PCB}$ requirement. If PCB trace insertion loss is less than the minimum limit, then distance needs to be increased.
(3) Calculation of channel length is the sum of $L_{AB}$ and $L_{CD}$.

### 8.3.2 Detailed Design Procedures

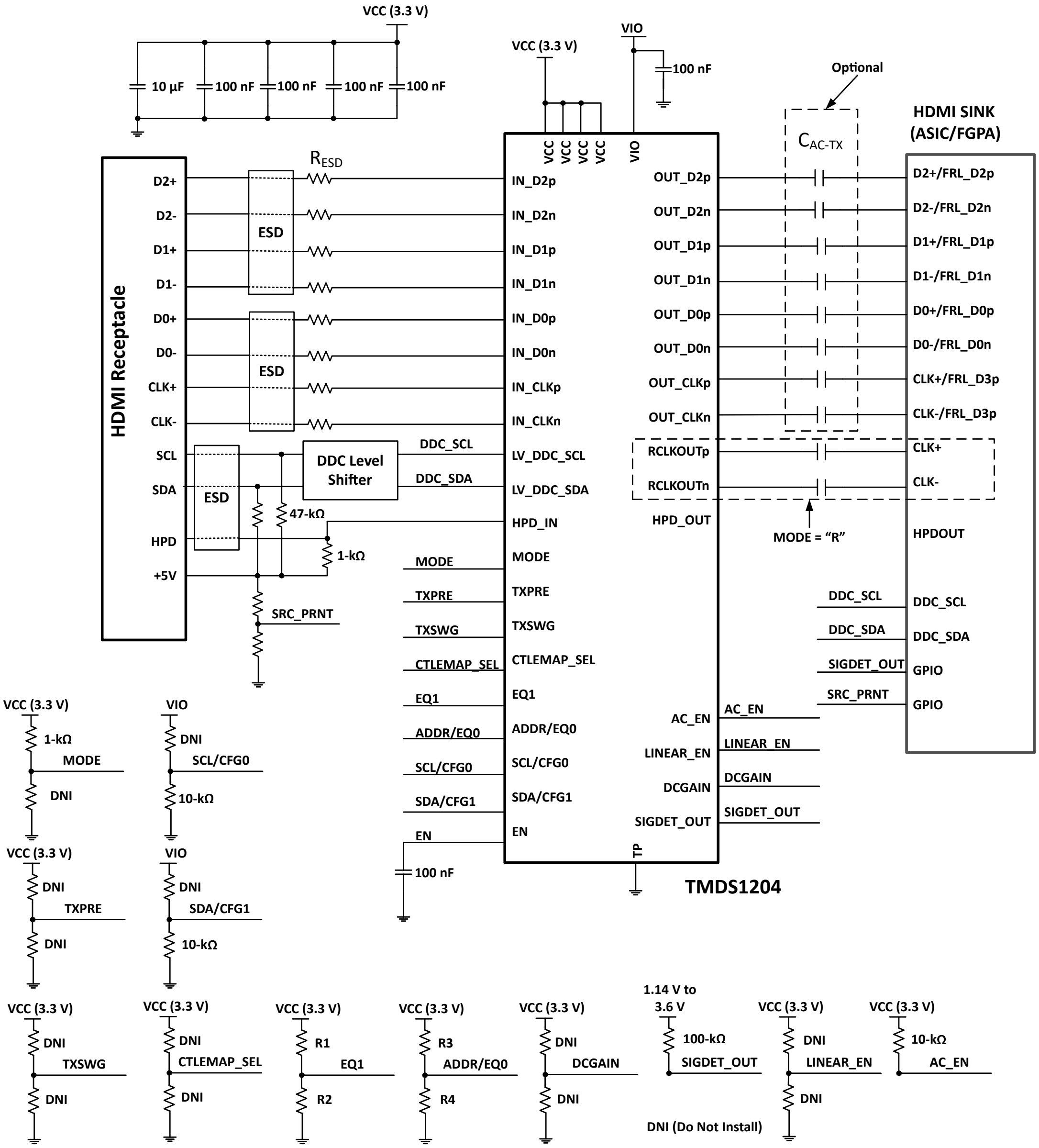


图 8-10. TMDS1204 in Sink Application Schematics

## 8.4 Power Supply Recommendations

### 8.4.1 Supply Decoupling

Texas Instruments recommends a single bulk capacitor of 10-µF on the $V_{CC}$ supply. Along with the bulk capacitor, Texas Instruments recommends a 0.1-µF decoupling capacitor on each TMDS1204 $V_{CC}$ pin that is placed as close to the $V_{CC}$ pin as possible. 图 8-10 shows an example.

## 8.5 Layout

### 8.5.1 Layout Guidelines

For the TMDS1204 on a high-K board, it is required to solder the PowerPAD™ onto the thermal land to ground. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. On a high-K board, the TMDS1204 can operate over the full temperature range by soldering the PowerPAD onto the thermal land. For the device to operate across the temperature range on a low-K board, a 1-oz Cu trace connecting the GND pins to the thermal land must be used. A simulation shows $R_{\theta JA}$ = 30.9°C/W allowing 950-mW power dissipation at 70°C ambient temperature. For information about a general PCB design guide for PowerPAD packages, refer to the *PowerPAD Thermally Enhanced Package* application report. TI recommends using a four layer stack up at a minimum to accomplish a low-EMI PCB design. TI recommends four layers as the TMDS1204 is a single voltage rail device.

- Routing the high-speed TMDS traces on the top layer avoids the use of vias (and the introduction of their inductance) and allows for clean interconnects from the HDMI connectors to the Redriver inputs and outputs. It is important to match the electrical length of these high speed traces to minimize both inter-pair and intra-pair skew.
- Placing a solid ground plane next to the high-speed single layer establishes controlled impedance for transmission link interconnects and provides an excellent low-inductance path for the return current flow.
- Placing a power plane next to the ground plane creates an additional high-frequency bypass capacitance.
- Routing slower seed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep symmetry. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high frequency bypass capacitance significantly.
- To minimize crosstalk between adjacent differential pairs, the distance between the differential pairs should be at least five times longer than the trace width (5W rule). For the clock differential pair, the distance should be increased to 8W or 10W.

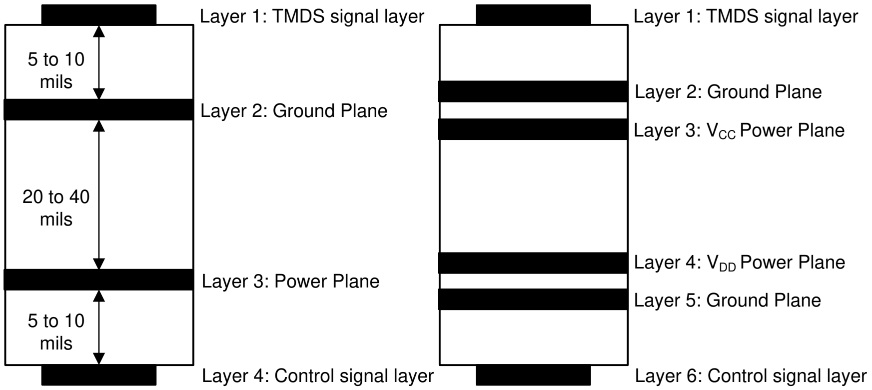
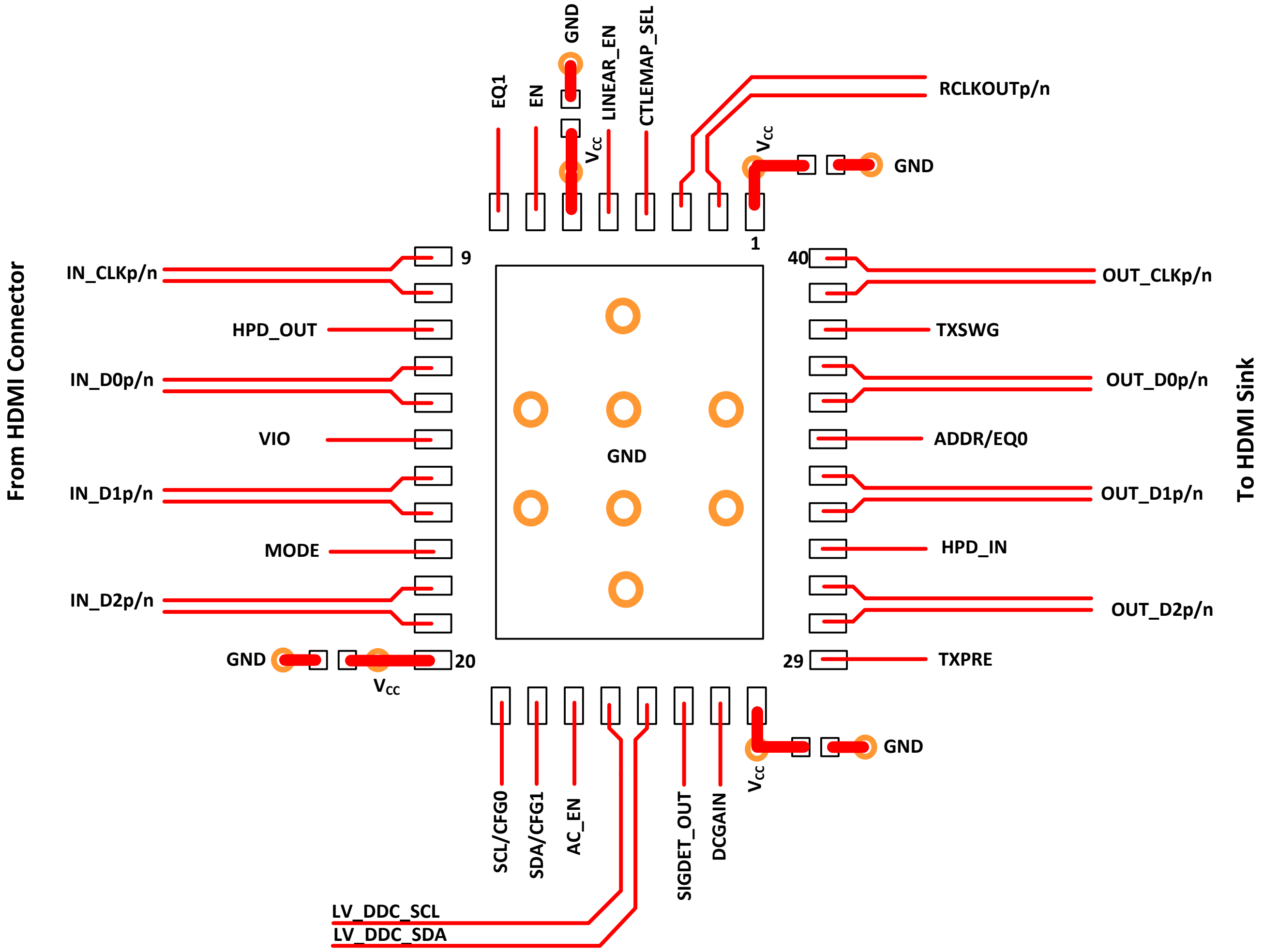


图 8-11. Recommended 4 or 6-Layer PCB Stack

### 8.5.2 Layout Example



The differential input lanes and differential output lanes should be separated as close to the TMDS1204 as feasible to minimize crosstalk. Adding a ground flood plain between each differential lane further reduces crosstalk and thus improves signal integrity at high speed data rates.

图 8-12. Sink Example Layout

## 9 器件和文档支持

### 9.1 文档支持

#### 9.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*PowerPAD 热增强型封装* 应用报告

### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

### 9.4 商标

HDMI™ is a trademark of HDMI Licensing, LLC.
Blu-ray™ is a trademark of Blu-ray Disc Association (BDA).
PowerPAD™ and TI E2E™ are trademarks of Texas Instruments.
TMDS® is a registered trademark of Silicon Image, Inc.
所有商标均为其各自所有者的财产。

### 9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision * (August 2022) to Revision A (April 2024) | Page |
|---|---|
| • 更新了*器件信息* 表以包含环境温度 | 1 |
| • Corrected swap of R and F in EQ1 pin column in *Receiver EQ Settings When GLOBAL_DCG = 0x2* table | 27 |
| • Added *DisplayPort* section | 35 |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TMDS1204IRNQR | Active | Production | WQFN (RNQ) \| 40 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TMD04 |
| TMDS1204IRNQR.B | Active | Production | WQFN (RNQ) \| 40 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TMD04 |
| TMDS1204IRNQT | Active | Production | WQFN (RNQ) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TMD04 |
| TMDS1204IRNQT.B | Active | Production | WQFN (RNQ) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TMD04 |
| TMDS1204RNQR | Active | Production | WQFN (RNQ) \| 40 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TMD04 |
| TMDS1204RNQR.B | Active | Production | WQFN (RNQ) \| 40 | 3000 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TMD04 |
| TMDS1204RNQT | Active | Production | WQFN (RNQ) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TMD04 |
| TMDS1204RNQT.B | Active | Production | WQFN (RNQ) \| 40 | 250 \| SMALL T&R | Yes | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | TMD04 |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

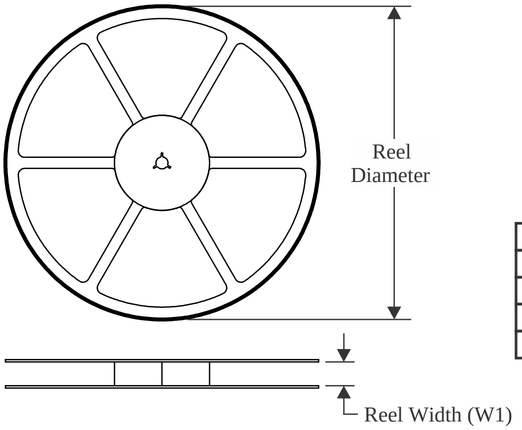
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

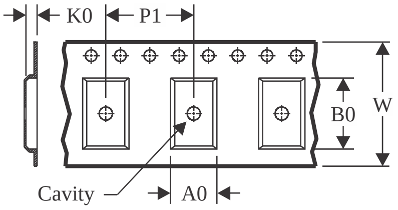
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

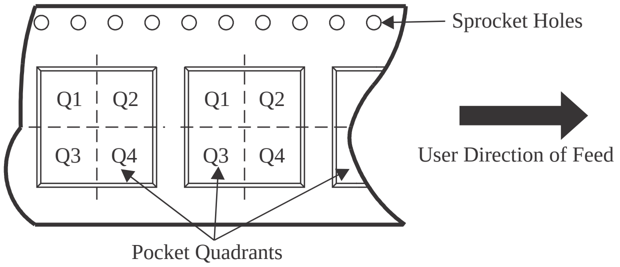


TAPE DIMENSIONS



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

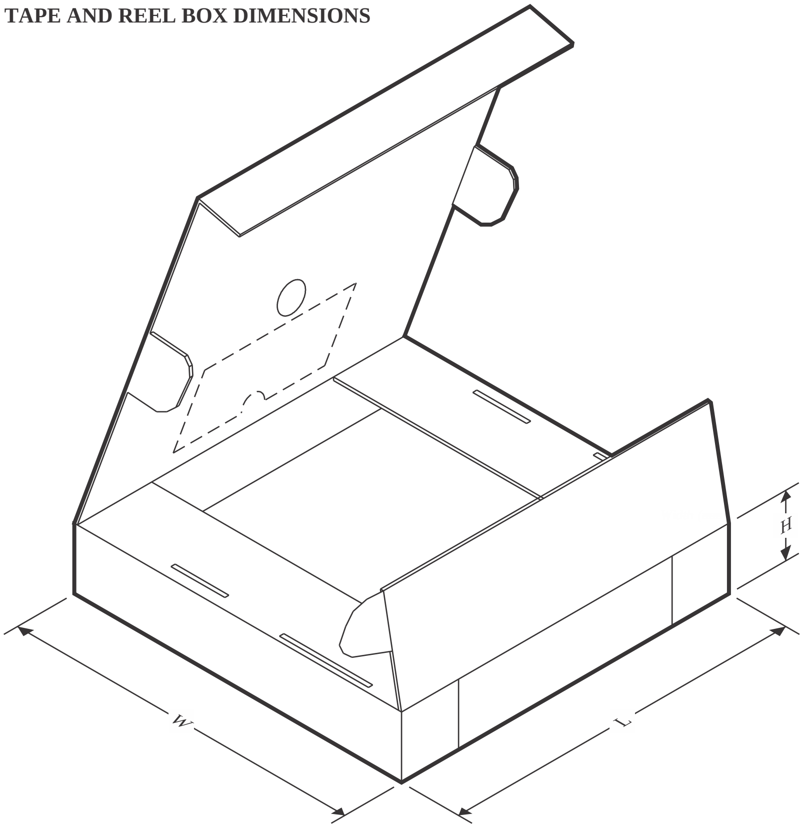
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

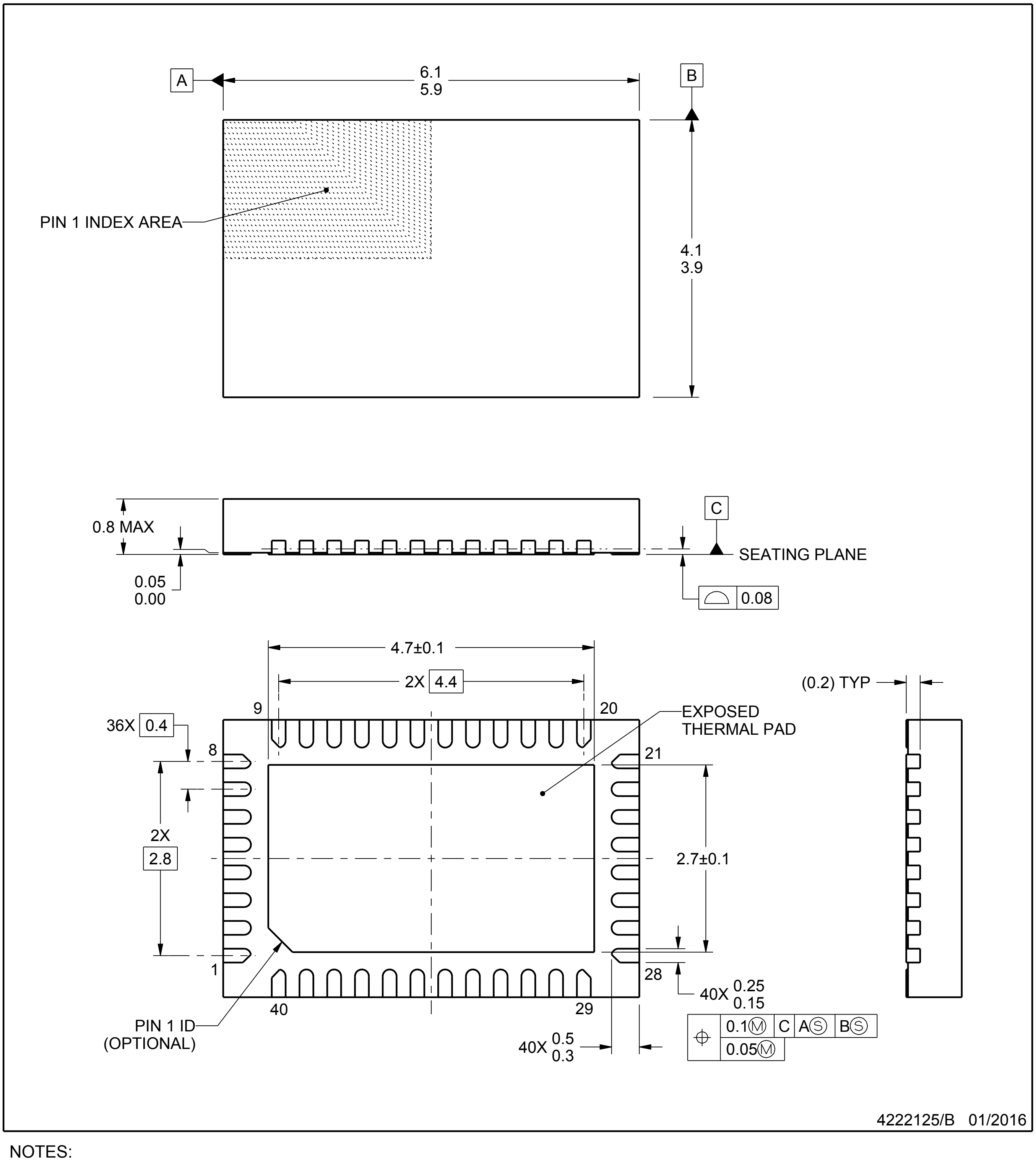
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMDS1204IRNQR | WQFN | RNQ | 40 | 3000 | 330.0 | 12.4 | 4.3 | 6.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TMDS1204IRNQT | WQFN | RNQ | 40 | 250 | 180.0 | 12.4 | 4.3 | 6.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TMDS1204RNQR | WQFN | RNQ | 40 | 3000 | 330.0 | 12.4 | 4.3 | 6.3 | 1.1 | 8.0 | 12.0 | Q2 |
| TMDS1204RNQT | WQFN | RNQ | 40 | 250 | 180.0 | 12.4 | 4.3 | 6.3 | 1.1 | 8.0 | 12.0 | Q2 |

## TAPE AND REEL BOX DIMENSIONS



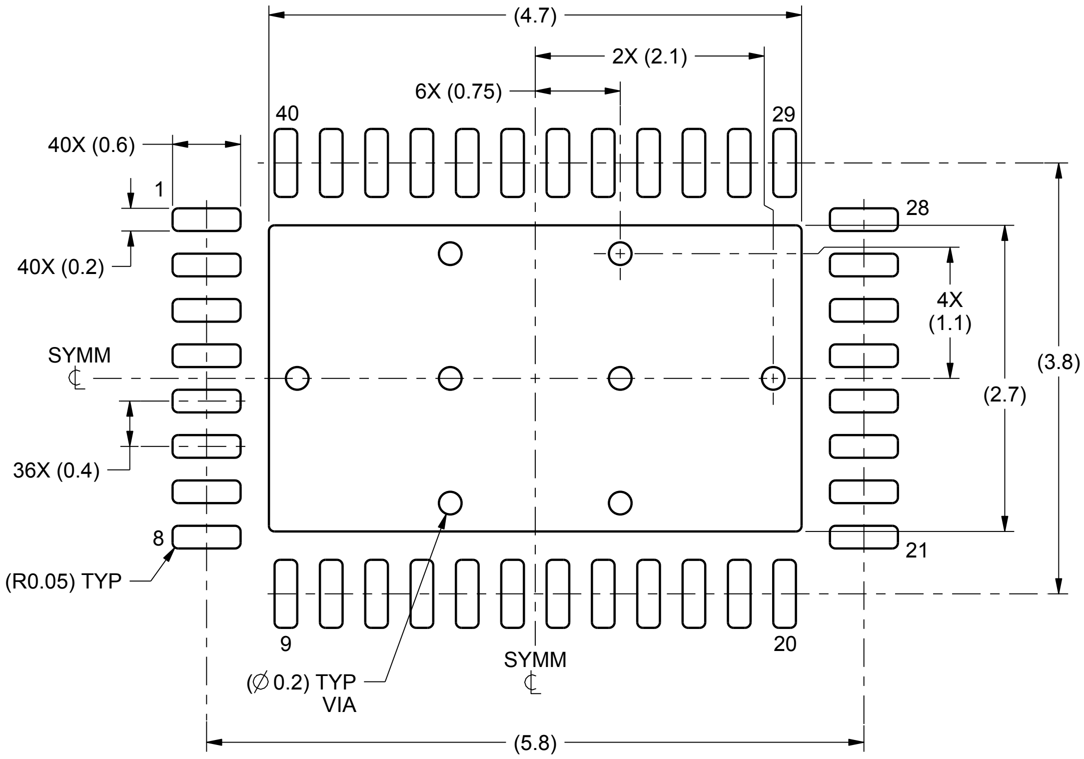
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TMDS1204IRNQR | WQFN | RNQ | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| TMDS1204IRNQT | WQFN | RNQ | 40 | 250 | 210.0 | 185.0 | 35.0 |
| TMDS1204RNQR | WQFN | RNQ | 40 | 3000 | 367.0 | 367.0 | 35.0 |
| TMDS1204RNQT | WQFN | RNQ | 40 | 250 | 210.0 | 185.0 | 35.0 |

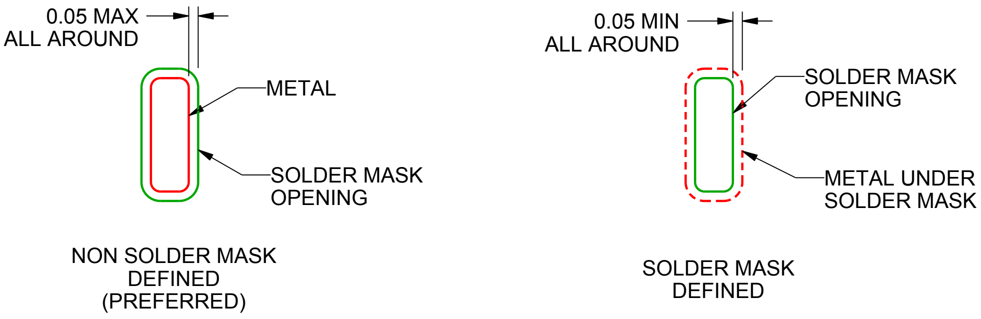


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

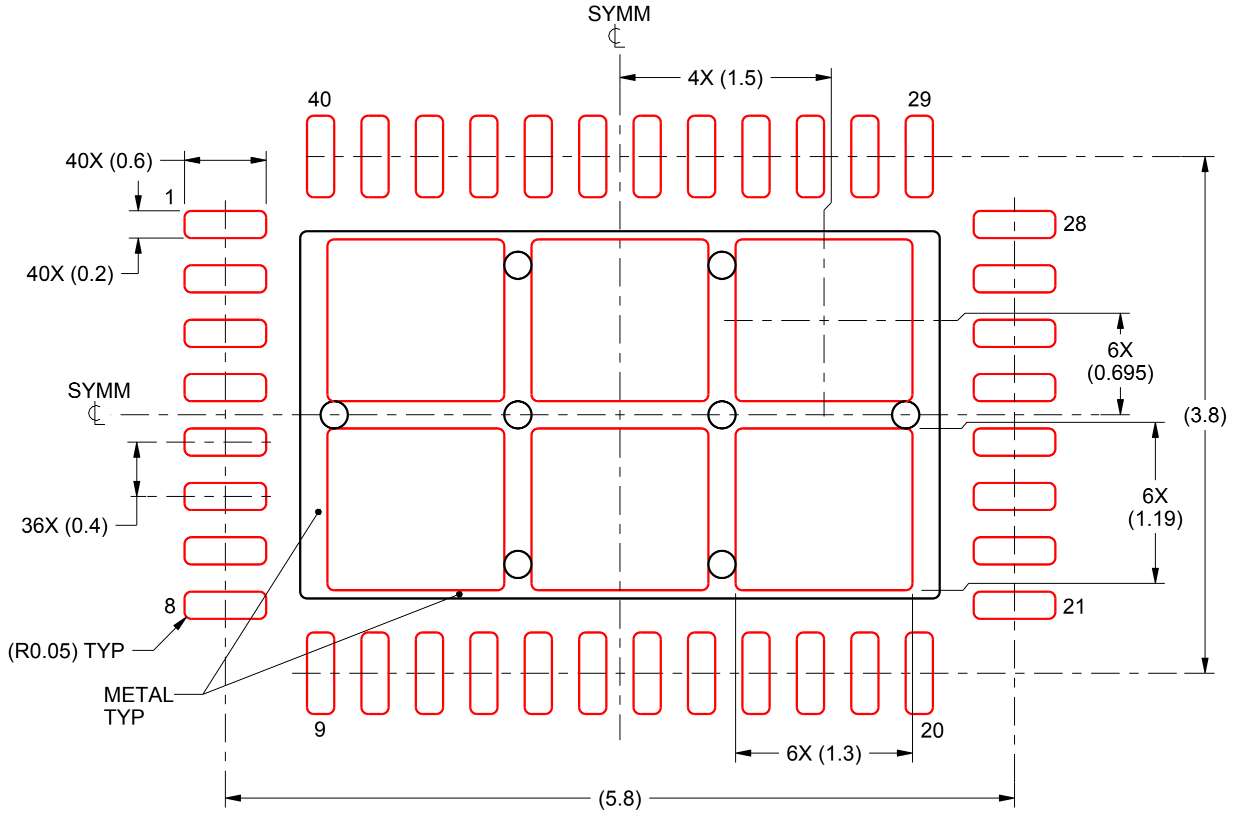


SOLDER MASK DETAILS

4222125/B 01/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
73% PRINTED SOLDER COVERAGE BY AREA
SCALE:18X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要通知和免责声明

最后更新日期：2025 年 10 月