具有轨对轨输入和推挽输出的 CMOS 比较器

1 特性

- 在 2.7V、5V 和 15V 电源下指定的参数
- 5V 时的电源电流 7 μ A（典型值）
- 5V 时的响应时间为 420ns
- 推挽输出
- 输入共模范围超过 V_{CC-} 和 V_{CC+}
- 低输入电流

2 应用

- 由电池供电的产品
- 笔记本电脑和 PDA
- 移动通信
- 警报和安防电路
- 直接传感器接口
- 取代了用作比较器的具有更好性能及更低电流的放大器

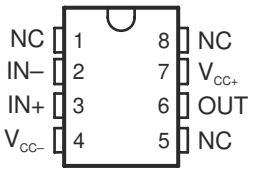
3 说明

TLV7211 和 TLV7211A 是一款微功耗 CMOS 比较器，采用节省空间的 SOT-23-5 封装。这使得比较器专为空间和重量关键的设计而设计。TLV7211A 具有 5mV 的输入偏移电压，TLV7211 具有 15mV 的输入偏移电压。

SOT-23-5 封装的主要优势在小型便携式电子设备（如手机、寻呼机、笔记本电脑、个人数字助理和 PCMCIA 卡）中尤为明显。轨到轨输入电压使得 TLV7211 或 TLV7211A 成为光检测器电路、光学与磁传感器以及警报与状态电路等传感器连接的理想选择。

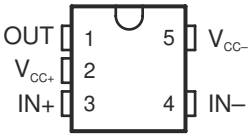
SOT-23-5 封装的尺寸较小，使得该器件能够适配于 PC 板上的狭小空间。

D PACKAGE (TOP VIEW)

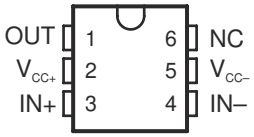


NC – No internal connection

DBV PACKAGE (TOP VIEW)



DCK PACKAGE (TOP VIEW)



本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

内容

1 特性.....1
2 应用.....1
3 说明.....1
4 订购信息.....2
5 规格.....3
5.1 绝对最大额定值.....3
5.2 ESD 保护.....3
5.3 建议运行条件.....3
5.4 2.7V 电气特性.....4
5.5 5V 电气特性.....5
5.6 15V 电气特性.....6
5.7 开关特性.....7
5.8 典型特性.....8
6 详细说明.....10
6.1 概述.....10
6.2 功能方框图.....10
6.3 特性说明.....10
7 器件和文档支持.....12
7.1 接收文档更新通知.....12
7.2 支持资源.....12
7.3 商标.....12
7.4 静电放电警告.....12
7.5 术语表.....12
8 修订历史记录.....12
9 机械、封装和可订购信息.....12

4 订购信息

T_A	V_{OS}（最大值）	封装(1)		可订购器件型号	正面标识(2)
-40°C 至 85°C	5mV	SOIC – D	卷 (2500)	TLV7211AIDR	7211AI
			75 管	TLV7211AID	
		SOT-23-5 – DBV	卷 (3000)	TLV7211AIDBVR	YBN_
		SOT (SC-70) – DCK	卷 (3000)	TLV7211AIDCKR	Y8_
	15mV	SOIC – D	卷 (2500)	TLV7211IDR	TY7211
			75 管	TLV7211ID	
		SOT-23-5 – DBV	卷 (3000)	TLV7211IDBVR	YBK_
		SOT (SC-70) – DCK	卷 (3000)	TLV7211IDCKR	Y7_

(1) 封装图、标准包装数量、热数据、符号和 PCB 设计指南可从 www.ti.com/sc/package 获取。
(2) DBV/DCK：实际正面标识有一个用于标明封测场所的附加字符。

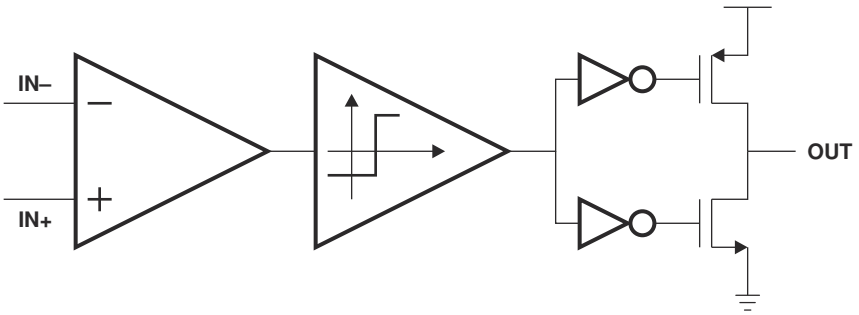


图 4-1. 功能方框图

Copyright © 2025 Texas Instruments Incorporated

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）

			最小值	最大值	单位
V_{CC+} – V_{CC-}	电源电压(1)			16	V
V_{ID}	差动输入电压(2)			正负电源电压	V
V_I	输入电压范围（任何输入）		V_{CC-} – 0.3	V_{CC+} + 0.3	V
V_O	输出电压范围		V_{CC-} – 0.3	V_{CC+} + 0.3	V
I_{CC}	电源电流			40	mA
I_I	输入电流			±5	mA
I_O	输出电流			±30	mA
θ_{JA}	封装热阻抗(3) (4)	D 封装		97	°C/W
		DBV 封装		206	
		DCK 封装		259	
T_J	工作虚拟结温			150	°C
T_{stg}	贮存温度范围		-65	150	°C

(1) 所有电压值（差分电压和为 I_{OS} 测量指定的 V_{CC} 除外）都是相对于网络 GND 的值。
(2) 差分电压是相对于 IN – 的 IN+ 上的值。
(3) 最大功耗是与 T_J(max)、θ_{JA} 和 T_A 相关的函数。在任何允许的环境温度下，允许的最大功耗为 $P_D = (T_J(max) – T_A)/\theta_{JA}$。在 150°C 的绝对最大 T_J 下运行可能会影响可靠性。
(4) 封装热阻抗根据 JESD 51-7 计算。

5.2 ESD 保护

	典型值	单位
人体放电模型	2000	V

5.3 建议运行条件

		最小值	最大值	单位
V_{CC+} – V_{CC-}	电源电压	2.7	15	V
T_J	工作虚拟结温	-40	85	°C

5.4 2.7V 电气特性

V_{CC+} = 2.7V，V_{CC-} = GND，V_{CM} = V_O = V_{CC+}/2 和 R_L > 1MΩ（除非另有说明）

参数		测试条件	T_J	TLV7211A			TLV7211			单位
				最小值	典型值	最大值	最小值	典型值	最大值	
V_{OS}	输入偏移电压		25°C		3	5		3	15	mV
			-40°C 至 85°C			8			18	
TCV_{OS}	输入失调电压温漂		25°C		1			1		μV/°C
I_B	输入电流		25°C		0.04			0.04		pA
I_{OS}	输入失调电流		25°C		0.02			0.02		pA
CMRR	共模抑制比	0 ≤ V_{CM} ≤ 2.7V	25°C		75			75		dB
PSRR	电源抑制比	2.7V ≤ V_{CC+} ≤ 15 V	25°C		80			80		dB
A_V	电压增益		25°C		100			100		dB
CMVR	输入共模电压范围	CMRR > 55dB	25°C	2.9	3		2.9	3		V
			-40°C 至 85°C	2.7			2.7			
		CMRR > 55dB	25°C		-0.3	-0.2		-0.3	-0.2	
			-40°C 至 85°C			0			0	
V_{OH}	高电平输出电压	I_{load} = 2.5mA	25°C	2.4	2.5		2.4	2.5		V
			-40°C 至 85°C	2.3			2.3			
V_{OL}	低电平输出电压	I_{load} = 2.5mA	25°C		0.2	0.3		0.2	0.3	V
			-40°C 至 85°C			0.4			0.4	
I_{CC}	电源电流	V_{OUT} = 低	25°C		7	12		7	12	μA
			-40°C 至 85°C			14			14	
		V_{OUT} = 高-空闲	25°C		5	10		5	10	
			-40°C 至 85°C			12			12	

Copyright © 2025 Texas Instruments Incorporated

5.5 5V 电气特性

V_{CC+} = 5V，V_{CC-} = GND，V_{CM} = V_O = V_{CC+}/2 和 R_L > 1MΩ（除非另有说明）

参数		测试条件	T_J	TLV7211A			TLV7211			单位
				最小值	典型值	最大值	最小值	典型值	最大值	
V_{OS}	输入偏移电压		25°C		3	5		3	15	mV
			-40°C 至 85°C			8			18	
TCV_{OS}	输入失调电压温漂		25°C		1			1		μV/°C
I_B	输入电流		25°C		0.04			0.04		pA
I_{OS}	输入失调电流		25°C		0.02			0.02		pA
CMRR	共模抑制比		25°C		75			75		dB
PSRR	电源抑制比	5V ≤ V_{CC+} ≤ 10 V	25°C		80			80		dB
A_V	电压增益		25°C		100			100		dB
CMVR	输入共模电压范围	CMRR > 55dB	25°C	5.2	5.3		5.2	5.3		V
			-40°C 至 85°C	5			5			
		CMRR > 55dB	25°C		-0.3	-0.2		-0.3	-0.2	
			-40°C 至 85°C			0			0	
V_{OH}	高电平输出电压	I_{load} = 5mA	25°C	4.6	4.8		4.6	4.8		V
			-40°C 至 85°C	4.45			4.45			
V_{OL}	低电平输出电压	I_{load} = 5mA	25°C		0.2	0.4		0.2	0.4	V
			-40°C 至 85°C			0.55			0.55	
I_{CC}	电源电流	V_{OUT} = 低	25°C		7	14		7	14	μA
			-40°C 至 85°C			18			18	
		V_{OUT} = 高-空闲	25°C		5	10		5	10	
			-40°C 至 85°C			13			13	
I_{OH}	短路输出电流	I_{source}	25°C	30			30			mA
I_{OL}	短路输出电流	I_{sink}，V_O < 12V(1)	25°C	45			45			mA

(1) 如果 V+ 大于 12V，请勿使输出短路至 V+。

5.6 15V 电气特性

V_{CC+} = 15V，V_{CC-} = GND，V_{CM} = V_O = V_{CC+}/2 和 R_L > 1MΩ（除非另有说明）

参数		测试条件	T_J	TLV7211A			TLV7211			单位
				最小值	典型值	最大值	最小值	典型值	最大值	
V_{OS}	输入偏移电压		25°C		3	5		3	15	mV
			-40°C 至 85°C			8			18	
TCV_{OS}	输入失调电压温漂		25°C		4			4		μV/°C
I_B	输入电流		25°C		0.04			0.04		pA
I_{OS}	输入失调电流		25°C		0.02			0.02		pA
CMRR	共模抑制比		25°C		82			82		dB
PSRR	电源抑制比	5V ≤ V_{CC+} ≤ 10 V	25°C		80			80		dB
A_V	电压增益		25°C		100			100		dB
CMVR	输入共模电压范围	CMRR > 55dB	25°C	15.2	15.3		15.2	15.3		V
			-40°C 至 85°C	15			15			
		CMRR > 55dB	25°C		-0.3	-0.2		-0.3	-0.2	
			-40°C 至 85°C			0			0	
V_{OH}	高电平输出电压	I_{load} = 5mA	25°C	14.6	14.8		14.6	14.8		V
			-40°C 至 85°C	14.45			14.45			
V_{OL}	低电平输出电压	I_{load} = 5mA	25°C		0.2	0.4		0.2	0.4	V
			-40°C 至 85°C			0.55			0.55	
I_{CC}	电源电流	V_{OUT} = 低	25°C		7	14		7	14	μA
			-40°C 至 85°C			18			18	
		V_{OUT} = 高-空闲	25°C		5	12		5	12	
			-40°C 至 85°C			14			14	
I_{OH}	短路输出电流	I_{source}	25°C	30			30			mA
I_{OL}	短路输出电流	I_{sink}，V_O < 12V(1)	25°C	45			45			mA

(1) 如果 V+ 大于 12V，请勿使输出短路至 V+。

Copyright © 2025 Texas Instruments Incorporated

5.7 开关特性

T_J = 25°C、V_{CC+} = 5V、V_{CC-} = GND、V_{CM} = V_O = V_{CC+}/2 和 R_L > 1MΩ（除非另有说明）

参数		测试条件		典型值	单位
t_{rise}	上升时间	f = 10kHz，C_L = 50pF(1)，过驱 = 10mV		15	ns
t_{fall}	下降时间	f = 10kHz，C_L = 50pF(1)，过驱 = 10mV		15	ns
t_{PHL}	传播延迟时间，从低电平到高电平	f = 10kHz，C_L = 50pF(1)	10mV	900	ns
			100mV	450	
t_{PLH}	传播延迟时间，从低电平到高电平	f = 10kHz，C_L = 50pF(1)	10mV	900	ns
			100mV	420	

(1) C_L 包括探头和夹具电容。

5.8 典型特性

T_A = 25°C，V_S = 12V，R_{PULLUP} = 2.5k，C_L = 20pF，V_{CM} = 0V，$V_{UNDERDRIVE}$ = 100mV，$V_{OVERDRIVE}$ = 100mV（除非另有说明）。

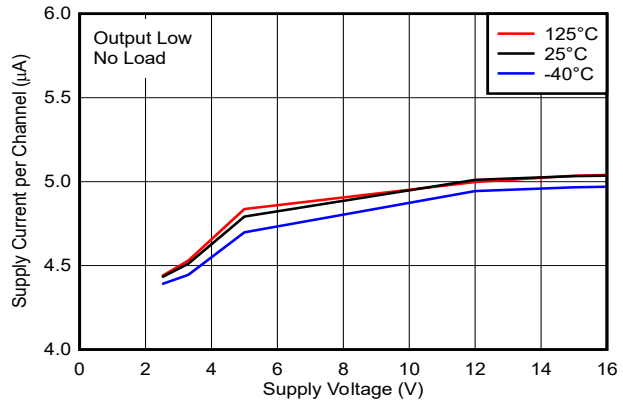


图 5-1. 每通道电源电流与电源电压间的关系，输出低电平

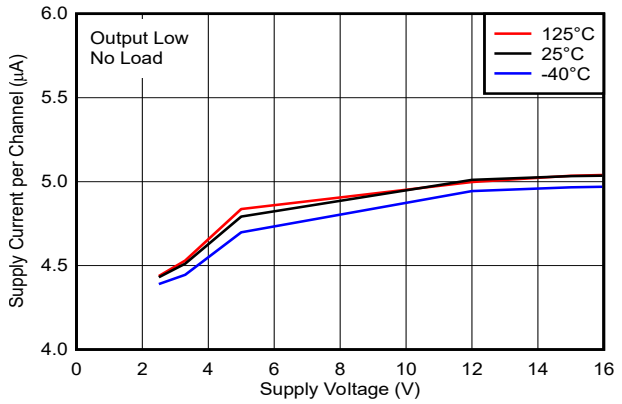


图 5-2. 每通道电源电流与电源电压间的关系，输出高电平

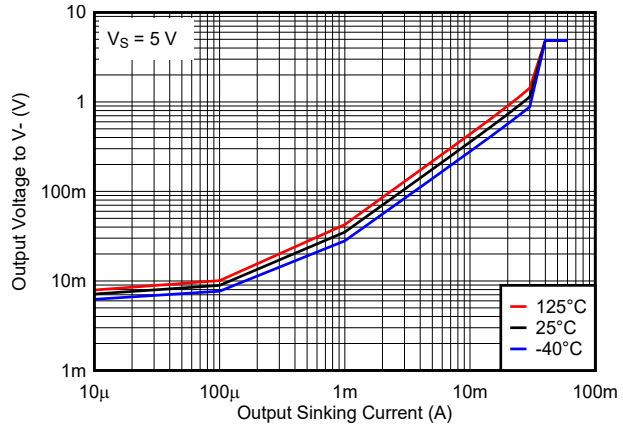


图 5-3. 输出电压与输出灌电流间的关系，5V

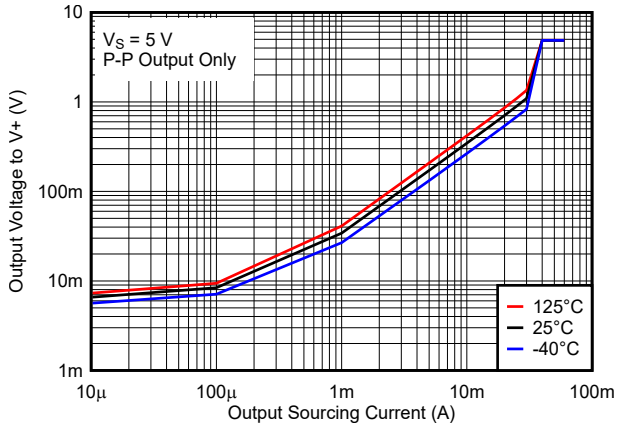


图 5-4. 输出电压与输出拉电流间的关系，5V

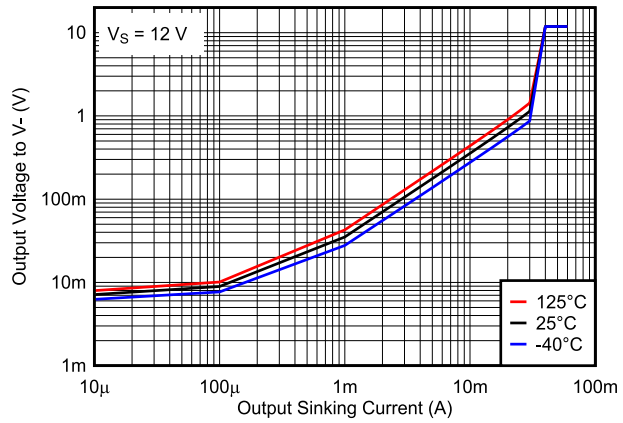


图 5-5. 输出电压与输出灌电流间的关系，12V

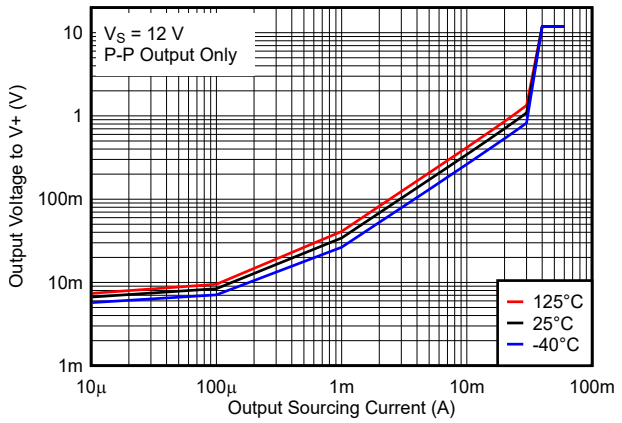


图 5-6. 输出电压与输出拉电流间的关系，12V

Copyright © 2025 Texas Instruments Incorporated

5.8 典型特性（续）

T_A = 25°C，V_S = 12V，R_{PULLUP} = 2.5k，C_L = 20pF，V_{CM} = 0V，$V_{UNDERDRIVE}$ = 100mV，$V_{OVERDRIVE}$ = 100mV（除非另有说明）。

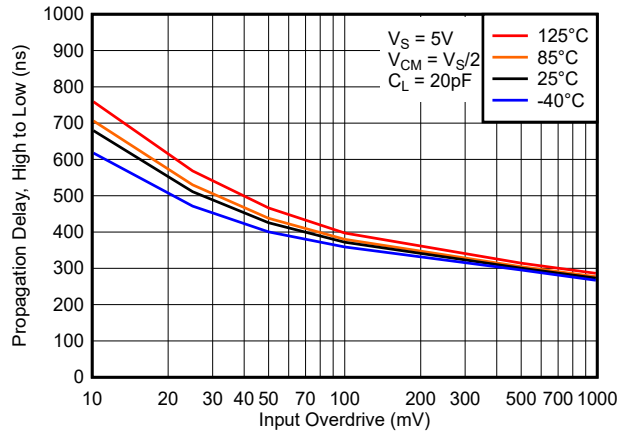


图 5-7. 传播延迟，从高电平到低电平，5V

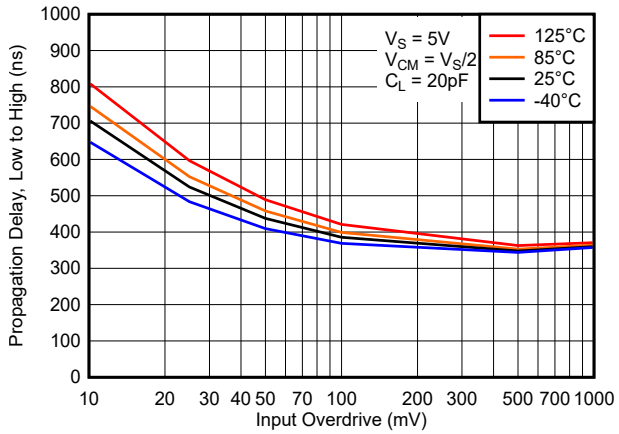


图 5-8. 传播延迟，从低电平到高电平，5V

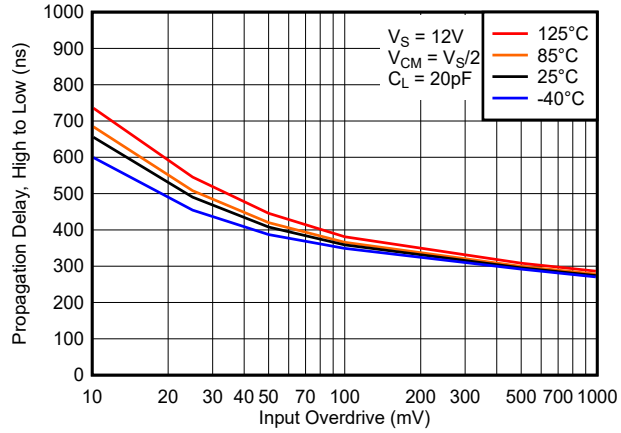


图 5-9. 传播延迟，从高电平到低电平，12V

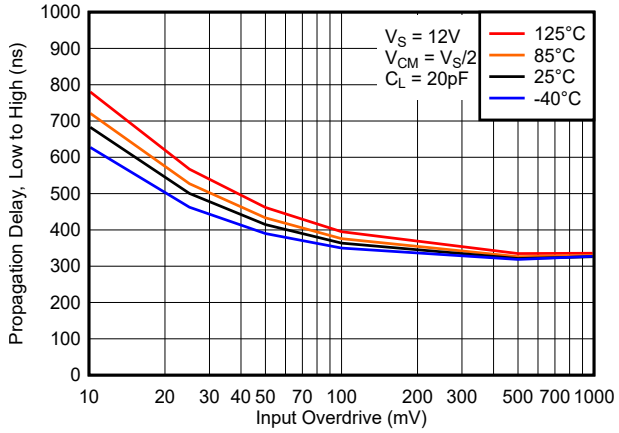


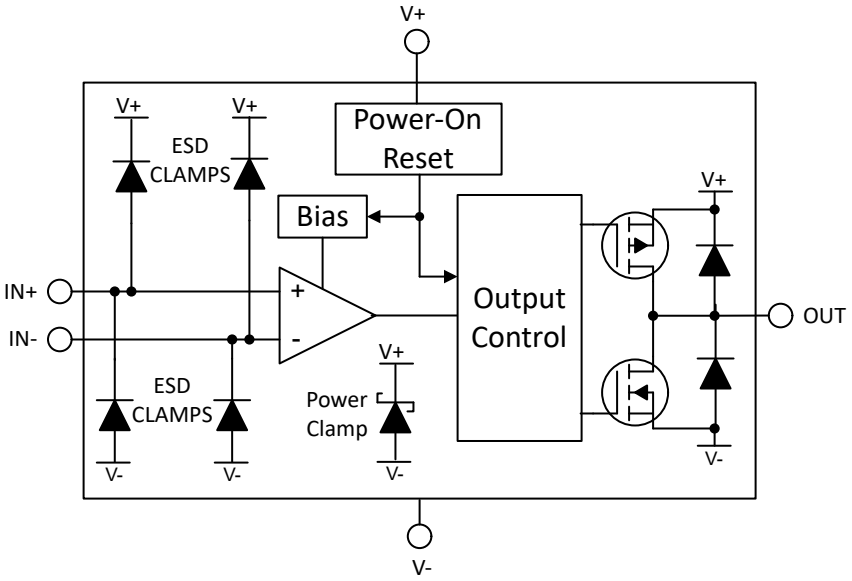
图 5-10. 传播延迟，从低电平到高电平，12V

6 详细说明

6.1 概述

TLV7211 推挽输出比较器具有 7uA 的低静态电流，并且可在 2.7V 至 15V 的电压范围内正常工作。推挽式 CMOS 输出级直接驱动容性负载，无需使用功耗上拉电阻器即可实现规定的响应时间。同样地，还集成了一个内部上电复位电路，这样在加电断电和时，输出端就会保持在已知的状态。

6.2 功能方框图



6.3 特性说明

6.3.1 器件功能模式

TLV7211 会在连接电源时通电。该器件可采用单电源或双电源供电，具体取决于应用需求。一旦电源电压高于建议值，器件便能发挥出最佳性能。

Copyright © 2025 Texas Instruments Incorporated

6.3.2 上电复位 (POR)

TLV7211 具有用于启动或断电条件已知的内部上电复位 (POR) 电路。当电源 (V+) 上升或下降时，当电压达到 1.7V 之后，POR 电路会激活长达 200µs，或者，在电源电压降至 1.7V 以下时立即激活。当电源电压大于等于最小电源电压时，经过延迟周期后，比较器输出将反映差分输入的状态 (V_{ID})。

对于 TLV7211 推挽输出器件，输出在 POR 期间 (t_{on}) 保持低电平。

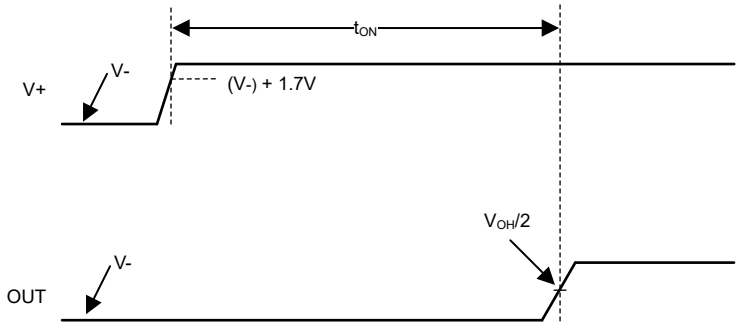


图 6-1. 上电复位时序图

7 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

7.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

7.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

7.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

8 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (January 2007) to Revision C (December 2025)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 通篇更新了传播延迟和上升/下降时间规范	1
• 删除了*电气特性* 表中典型的输入偏移电压平均漂移值	4
• 更新了典型性能特性曲线	8
• 添加了上电复位 (POR) 说明	11

9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

Copyright © 2025 Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV7211AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI
TLV7211AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI
TLV7211AIDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	YBNM
TLV7211AIDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	YBNM
TLV7211AIDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Y8A
TLV7211AIDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Y8A
TLV7211AIDCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLV7211AIDCKT	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 85	Y8A
TLV7211AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI
TLV7211AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	7211AI
TLV7211ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211IDBVR	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	YBKM
TLV7211IDBVR.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	YBKM
TLV7211IDCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Y7A
TLV7211IDCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	Y7A
TLV7211IDCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	-	Call TI	Call TI	-40 to 85	
TLV7211IDCKT	Obsolete	Production	SC70 (DCK) | 6	-	-	Call TI	Call TI	-40 to 85	Y7A
TLV7211IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211
TLV7211IDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TY7211

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

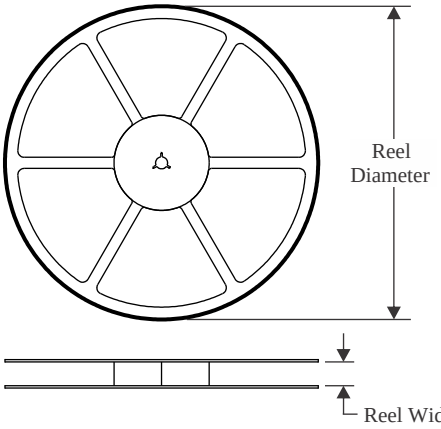
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

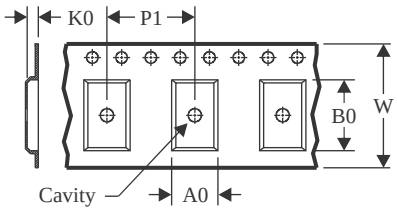
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

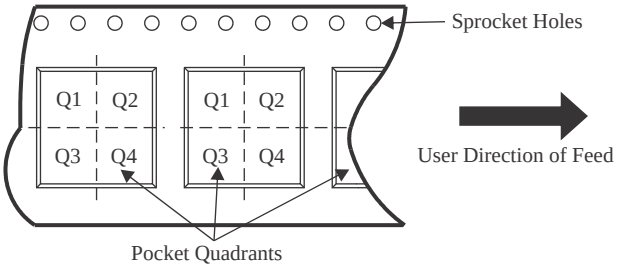


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

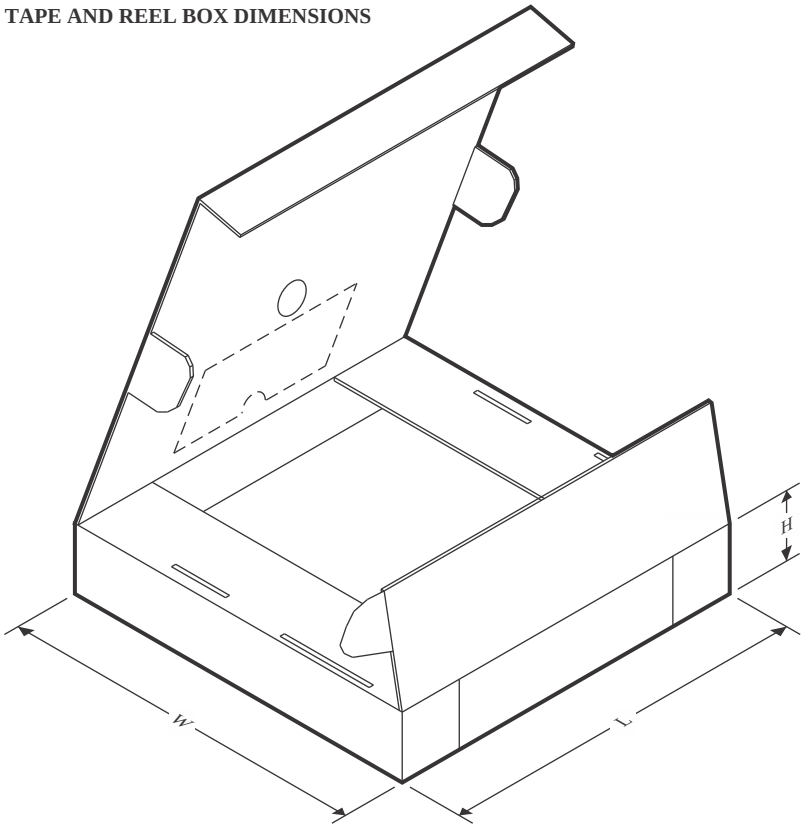
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV7211AIDBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7211AIDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7211AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV7211IDBVR	SOT-23	DBV	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7211IDCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV7211IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV7211IDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

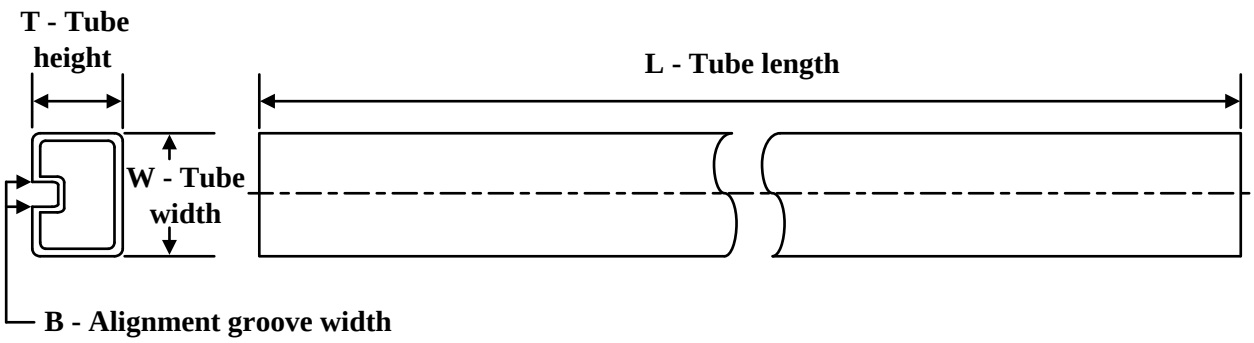
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

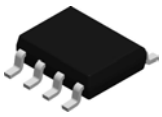
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV7211AIDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7211AIDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV7211AIDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV7211IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TLV7211IDCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TLV7211IDR	SOIC	D	8	2500	340.5	338.1	20.6
TLV7211IDRG4	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLV7211AID	D	SOIC	8	75	507	8	3940	4.32
TLV7211AID.A	D	SOIC	8	75	507	8	3940	4.32
TLV7211ID	D	SOIC	8	75	507	8	3940	4.32
TLV7211ID.A	D	SOIC	8	75	507	8	3940	4.32

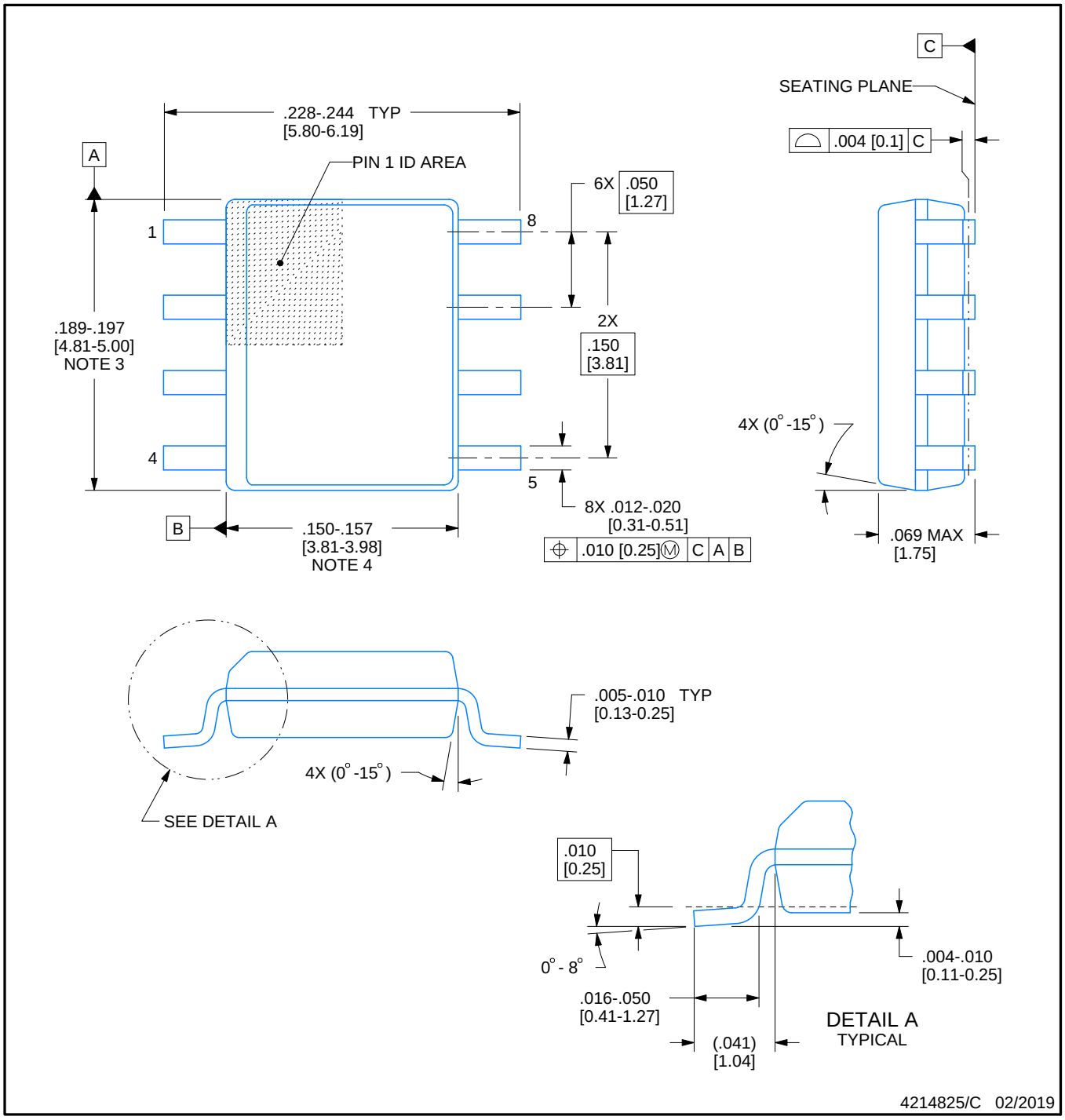


PACKAGE OUTLINE

D0008A

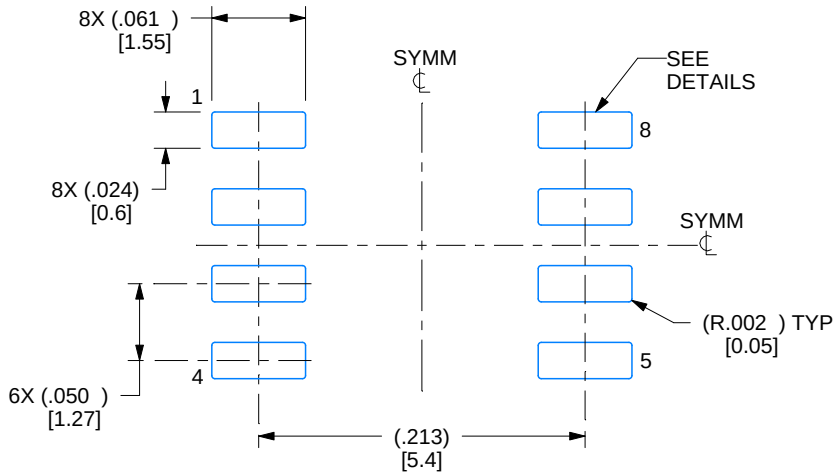
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

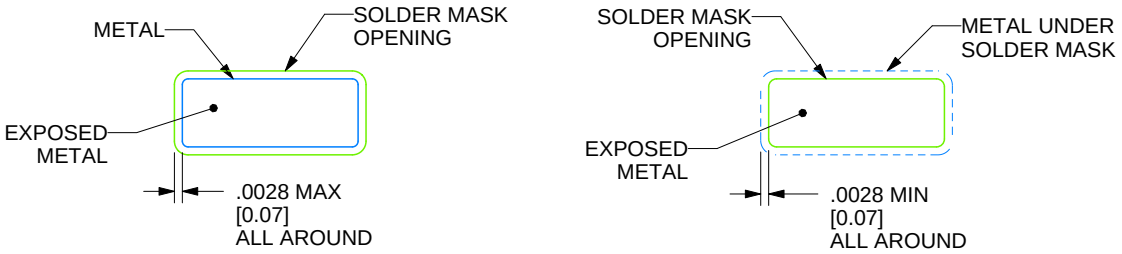


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

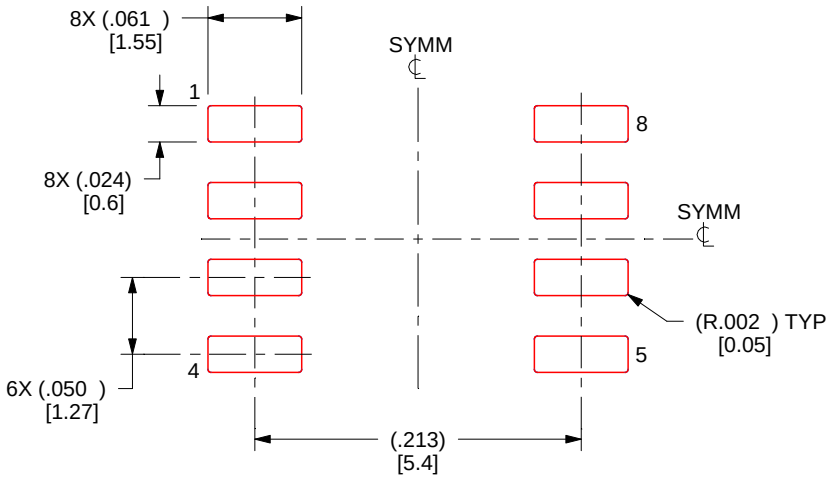


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

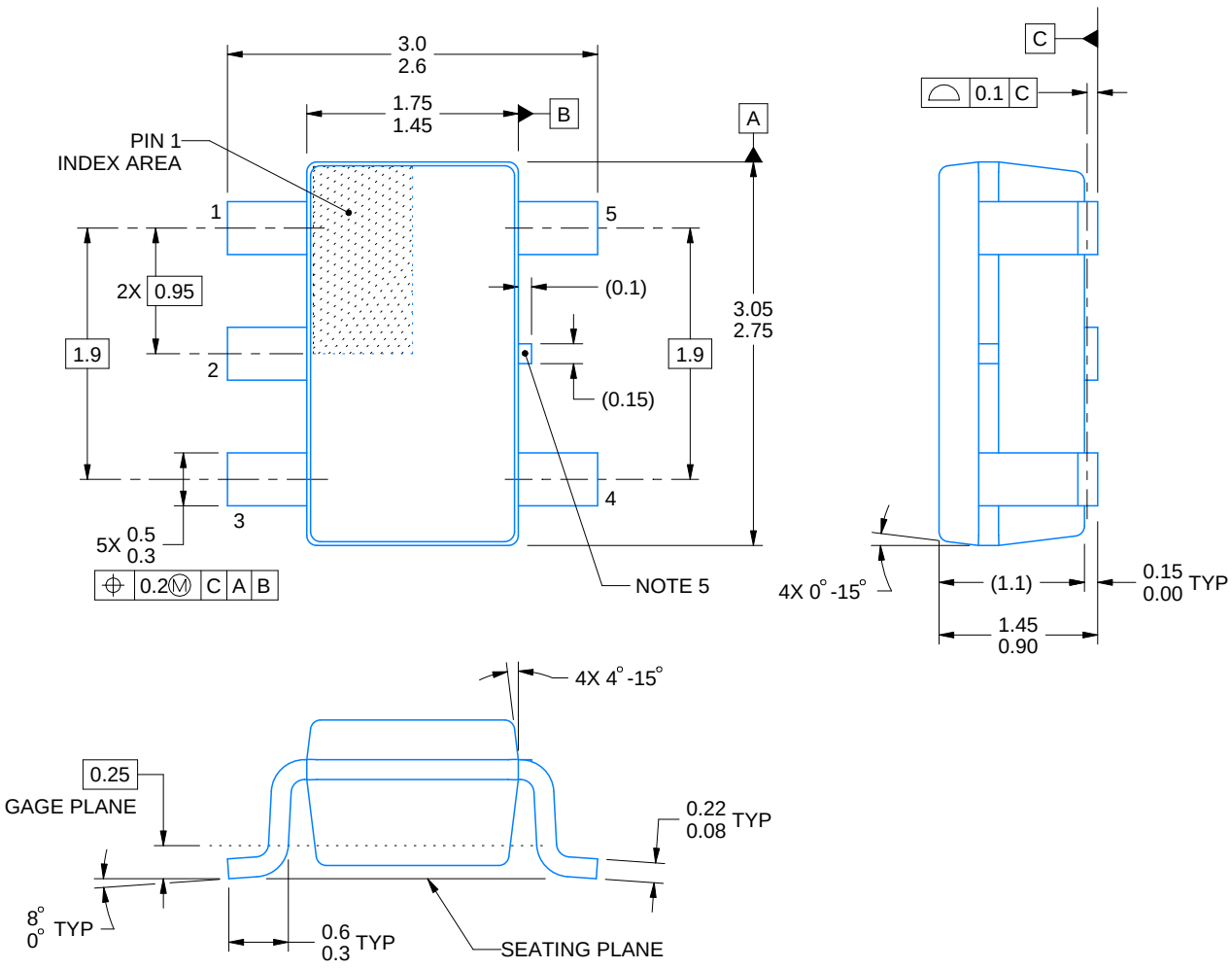


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

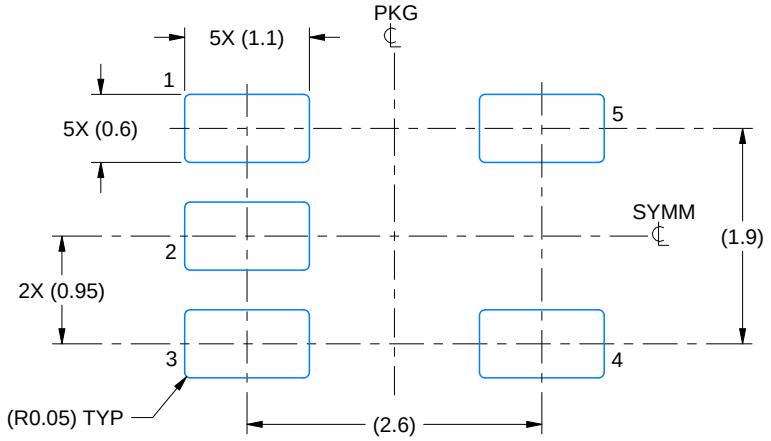
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



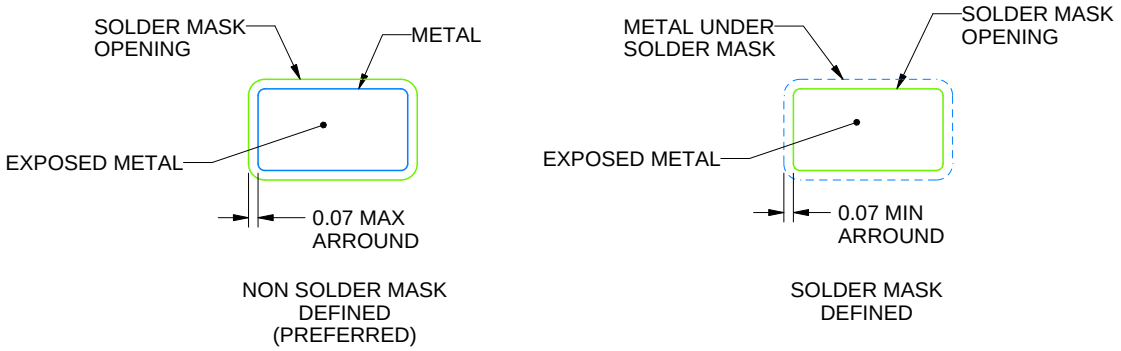
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

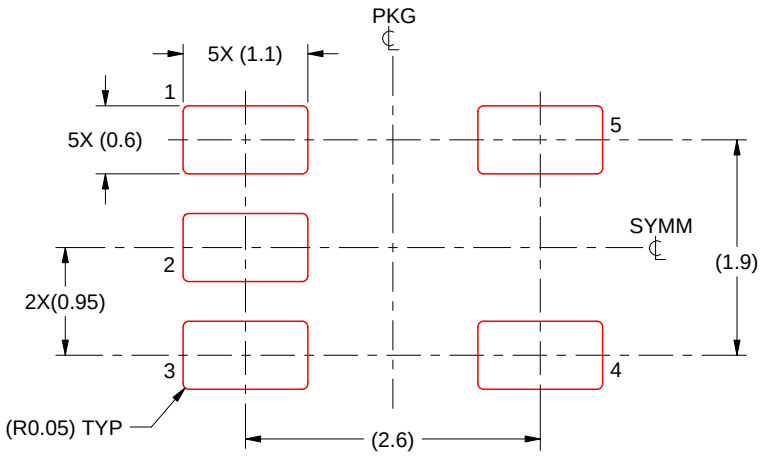


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

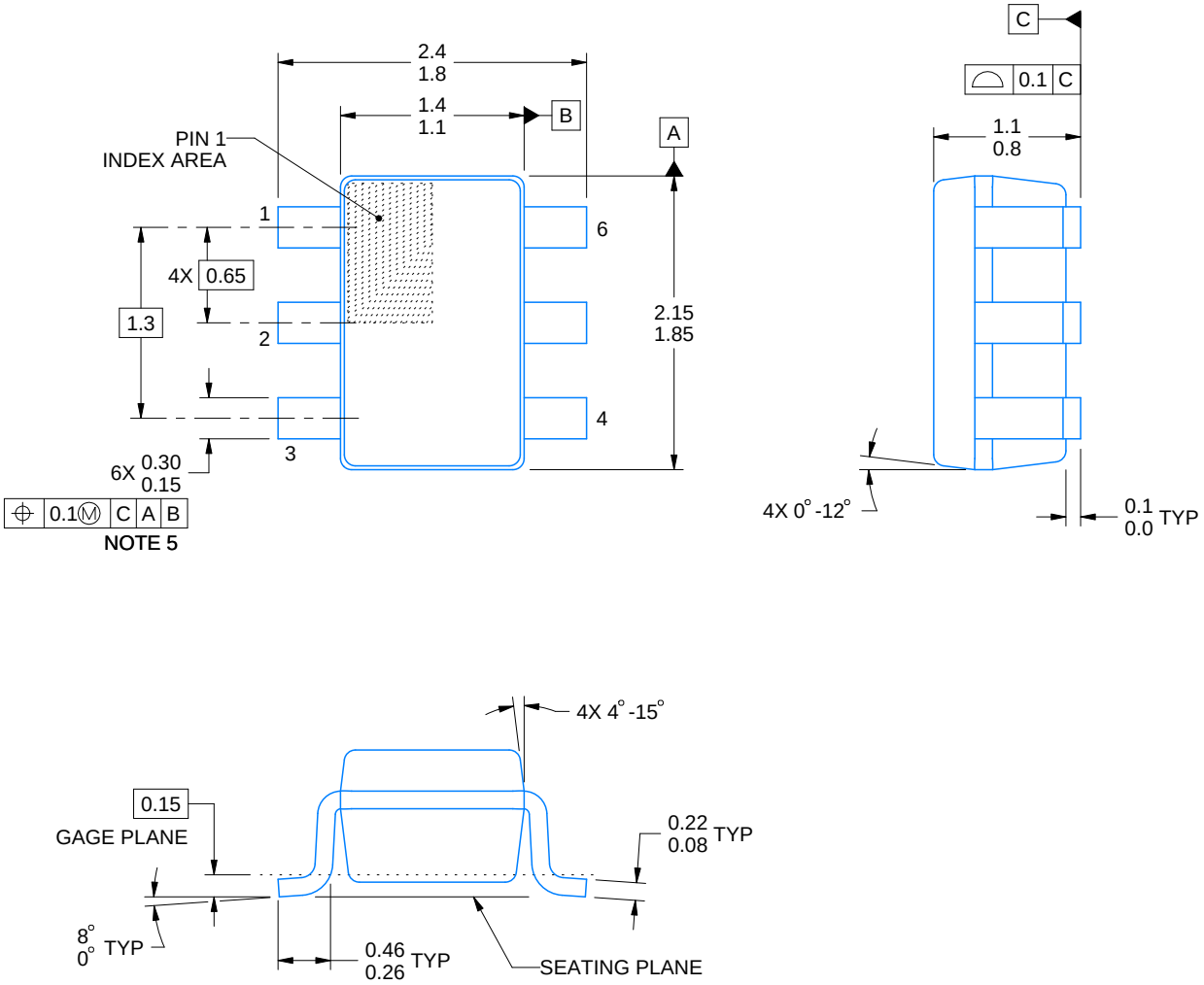


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

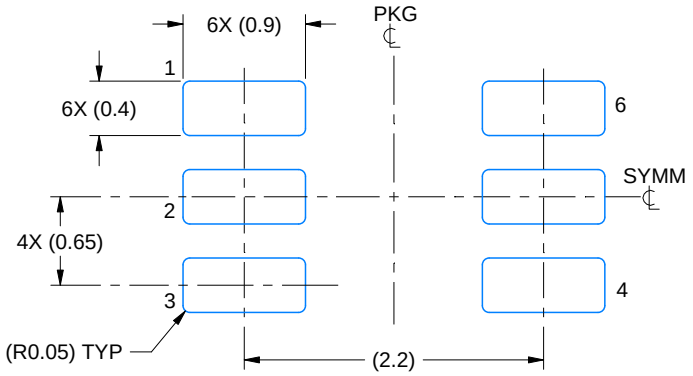
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



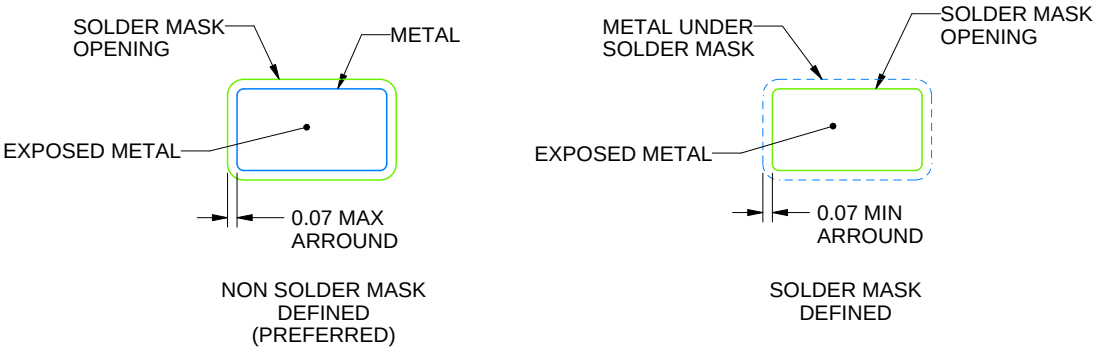
4214835/D 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

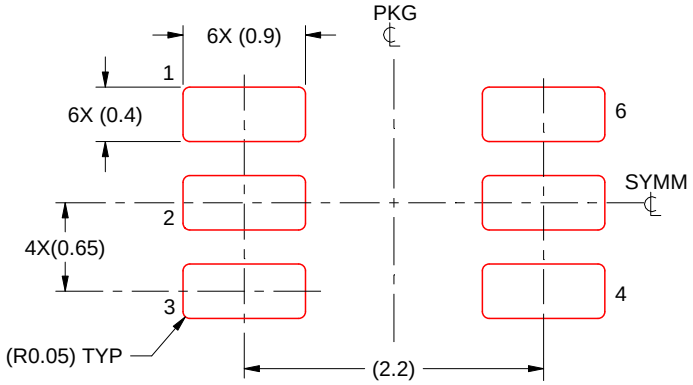


SOLDER MASK DETAILS

4214835/D 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 TI 销售条款)、TI 通用质量指南 或 ti.com 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。 除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月