TLV61070A 具有 0.5V 超低输入电压的 2.5A 升压转换器

1 特性

- 输入电压范围：0.5V 至 5.5V
- 启动时的最小输入电压为 1.3V
- 输出电压设置范围：2.2V 至 5.5V
- 两个 69mΩ (LS)/89mΩ (HS) MOSFET
- 2.5A 谷值开关电流限制
- V_{IN} = 3.6V、V_{OUT} = 5V 且 I_{OUT} = 1.0 A 时效率为 92.3%
- V_{IN} > 1.5V 时开关频率为 1MHz，V_{IN} < 1V 时开关频率为 0.55MHz
- V_{IN} 和 SW 关断电流典型值为 0.1μA
- 在 –40°C 至 +125°C 温度范围内，基准电压精度为 ±2.5%
- 轻负载下采用自动 PFM 运行模式
- V_{IN} > V_{OUT} 时切换为直通模式
- 在关断期间真正断开输入域输出之间的连接
- 输出过压和热关断保护
- 输出短路保护
- 2.9mm × 1.6mm SOT23-6 (DDC) 6 引脚封装

2 应用

- 电子货架标签
- 可视门铃
- 远程控制器

3 说明

TLV61070A 器件是一款具有 0.5V 超低输入电压的同步升压转换器。该器件可以为由多种电池和超级电容器供电的便携式设备和智能设备提供电源解决方案。在整个温度范围内，TLV61070A 具有 2.5A 的典型谷值开关电流限制。在 0.5V 至 5.5V 的宽输入电压范围内，TLV61070A 支持超级电容器备用电源应用，这可能导致超级电容器深度放电。

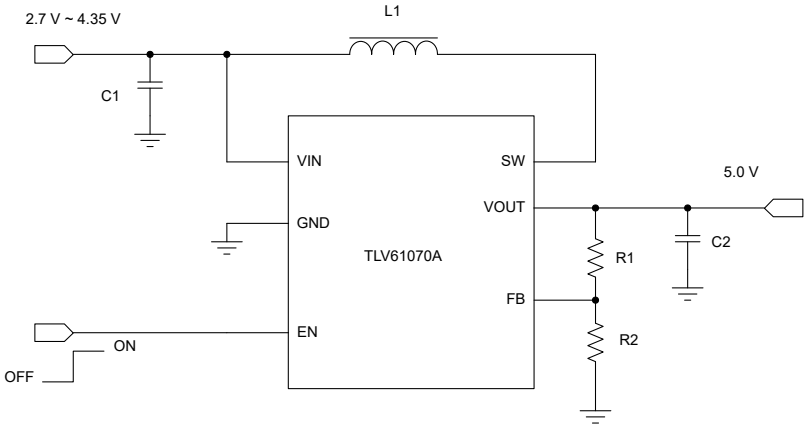
当输入电压高于 1.5V 时，TLV61070A 的工作频率为 1MHz。当输入电压低于 1.5V 甚至降至 1V 时，开关频率逐渐降至 0.55MHz。TLV61070A 在轻负载条件下会进入省电模式，以便在整个负载电流范围内保持高效率。在轻负载条件下，TLV61070A 在 V_{OUT} 处消耗 20μA 的静态电流。在关断期间，TLV61070A 与输入电源完全断开，仅消耗 0.1μA 的电流，从而能够实现较长的电池寿命。TLV61070A 具有 5.7V 输出过压保护、输出短路保护和热关断保护。

TLV61070A 采用 2.9mm × 1.6mm SOT23-6 (DBV) 封装，更大限度地减少了外部元件的数量，因而拥有非常小巧的解决方案尺寸。

器件信息

器件型号	封装(1)	封装尺寸（标称值）
TLV61070A	SOT-23 (6)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用电路

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4 Revision History

DATE	REVISION	NOTES
September 2022	*	Initial release

5 Pin Configuration and Functions

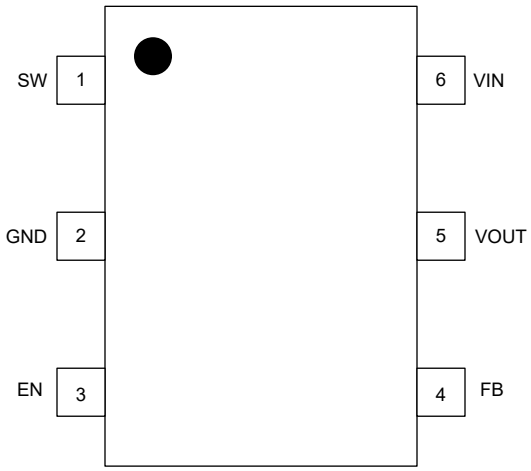


图 5-1. DBV Package 6-Pin SOT236 Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SW	PWR	The switch pin of the converter. It is connected to the drain of the internal low-side power MOSFET and the source of the internal high-side power MOSFET.
2	GND	PWR	Ground pin of the IC
3	EN	I	Enable logic input. Logic high voltage enables the device. Logic low voltage disables the device and turns it into shutdown mode.
4	FB	I	Voltage feedback of adjustable output voltage
5	VOUT	PWR	Boost converter output
6	VIN	I	IC power supply input

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage range at terminals(2)	VIN, EN, FB, SW, VOUT	–0.3	7	V
	SW spike at 10ns	–0.7	8	V
	SW spike at 1ns	–0.7	9	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	0.5		5.5	V
V_{OUT}	Output voltage setting range	2.2		5.5	V
L	Effective inductance range	0.7	1.0	6.1	µH
C_{IN}	Effective input capacitance range	1.0	4.7		µF
C_{OUT}	Effective output capacitance range	4	10	1000	µF
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV61070A DBV - 6 PINS Standard	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	139.1	°C/W
$R_{\theta JC}$	Junction-to-case thermal resistance	34.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	40.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

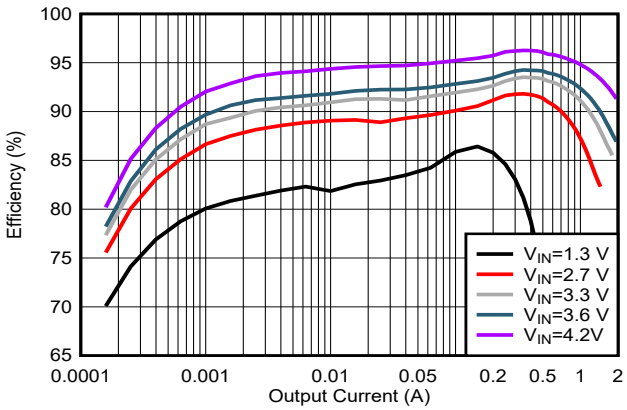
6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 3.6 V and V_{OUT} = 5.0 V. Typical values are at T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		0.5		5.5	V
V_{IN_UVLO}	Under-voltage lockout threshold	V_{IN} rising		1.0	1.3	V
		V_{IN} falling		0.4	0.5	V
I_Q	Quiescent current into VIN pin	IC enabled, No load, No switching V_{IN} = 1.3 V to 5.5 V, V_{FB} = V_{REF} + 0.1 V, T_J up to 85°C		0.9	3.0	µA
	Quiescent current into VOUT pin	IC enabled, No load, No switching V_{OUT} = 2.2 V to 5.5 V, V_{FB} = V_{REF} + 0.1 V, T_J up to 85°C		20	30	µA
I_{SD}	Shutdown current into VIN and SW pin	IC disabled, V_{IN} = V_{SW} = 3.6 V, T_J = 25°C		0.1	0.2	µA
OUTPUT						
V_{OUT}	Output voltage setting range		2.2		5.5	V
V_{REF}	Reference voltage at the FB pin	PWM mode	485	500	515	mV
		PFM mode		505		mV
V_{OVP}	Output over-voltage protection threshold	V_{OUT} rising	5.5	5.7	6.0	V
V_{OVP_HYS}	Over-voltage protection hysteresis			0.1		V
I_{FB_LKG}	Leakage current at FB pin			4	50	nA
I_{VOUT_LKG}	Leakage current into VOUT pin	IC disabled, V_{IN} = 0 V, V_{SW} = 0 V, V_{OUT} = 5.5 V, T_J = 25°C		1	3	µA
t_{SS}	Soft startup time	From active EN to VOUT regulation. V_{IN} = 2.5 V, V_{OUT} = 5.0 V, C_{OUT_EFF} = 10 µF, I_{OUT} = 0		750		µs
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on resistance	V_{OUT} = 5.0 V		89		mohm
	Low-side MOSFET on resistance	V_{OUT} = 5.0 V		69		mohm
f_{SW}	Switching frequency	V_{IN} = 3.6 V, V_{OUT} = 5.0 V, PWM mode		1.0		MHz
		V_{IN} = 1.0 V, V_{OUT} = 5.0 V, PWM mode		0.55		MHz
t_{ON_min}	Minimum on time		40	96	130	ns
t_{OFF_min}	Minimum off time			80	120	ns
I_{LIM_SW}	Valley current limit	V_{IN} = 3.6 V, V_{OUT} = 5.0 V,T_J = 25°C	2.00	2.45		A
I_{LIM_SW}	Valley current limit	V_{IN} = 3.6 V, V_{OUT} = 5.0 V,T_J = –40°C to 125°C	1.80	2.45		A
I_{LIM_CHG}	Pre-charge current	V_{IN} = 1.3 - 5.5 V, V_{OUT} < 0.4 V	100	185		mA
		V_{IN} = 2.4 V, V_{OUT} = 2.15 V	200	385		mA
LOGIC INTERFACE						
V_{EN_H}	EN logic high threshold	V_{IN} > 1.3 V or V_{OUT} > 2.2 V			1.2	V
V_{EN_L}	EN logic low threshold	V_{IN} > 1.3 V or V_{OUT} > 2.2 V	0.35	0.42	0.45	
PROTECTION						
T_{SD}	Thermal shutdown threshold	T_J rising		150		°C
T_{SD_HYS}	Thermal shutdown hysteresis	T_J falling below T_{SD}		20		°C

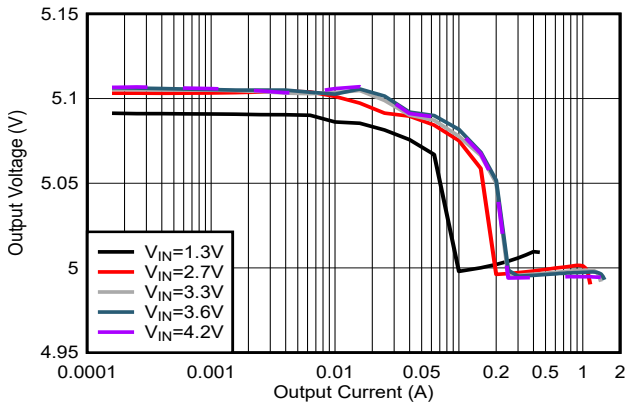
6.6 Typical Characteristics

V_{IN} = 3.6 V, V_{OUT} = 5 V, T_J = 25°C, unless otherwise noted



V_{IN} = 1.3 V, 2.7 V, 3.3 V, 3.6 V4.2 V; V_{OUT} = 5 V

图 6-1. Load Efficiency with Different Input



V_{IN} = 1.3 V, 2.7 V, 3.3 V, 3.6 V4.2 V; V_{OUT} = 5 V

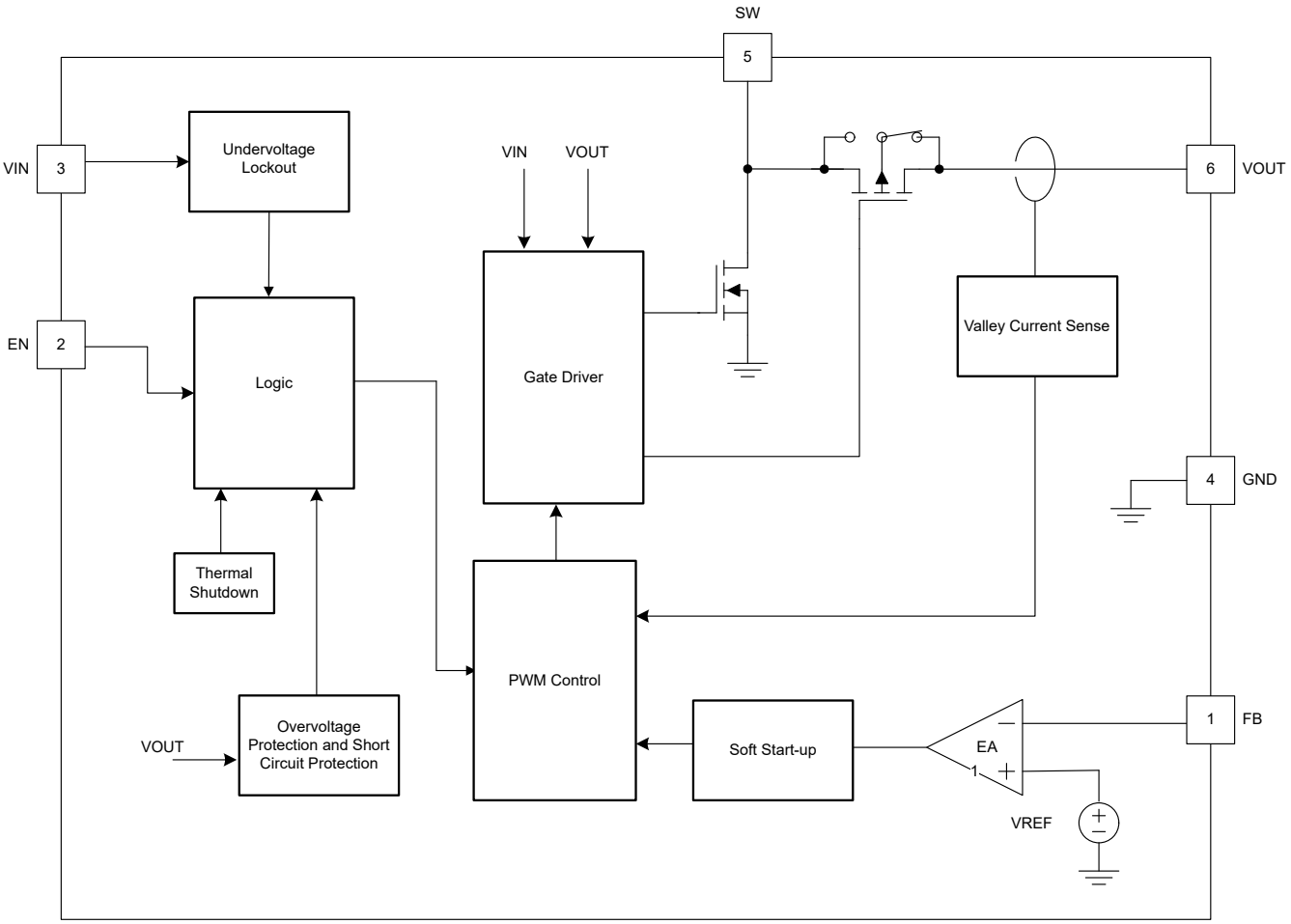
图 6-2. Load Regulation

7 Detailed Description

7.1 Overview

The TLV61070A synchronous step-up converter is designed to operate from an input voltage supply range between 0.5 V and 5.5 V with 2.5-A valley switch current limit. The TLV61070A typically operates at a quasi-constant frequency pulse width modulation (PWM) at moderate to heavy load currents. The switching frequency is 1 MHz when the input voltage is above 1.5 V. The switching frequency reduces down to 0.55 MHz gradually when the input voltage goes down from 1.5 V to 1 V and keeps at 0.55 MHz when the input voltage is below 1 V. At light load conditions, the TLV61070A converter operates in Power Save mode with pulse frequency modulation (PFM). During PWM operation, the converter uses adaptive constant on-time valley current mode control scheme to achieve excellent line regulation and load regulation and allows the use of a small inductor and ceramic capacitors. Internal loop compensation simplifies the design process while minimizing the number of external components.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout

The TLV61070A has a built-in undervoltage lockout (UVLO) circuit to ensure the device working properly. When the input voltage is above the UVLO rising threshold of 1.3 V, the TLV61070A can be enabled to boost the output voltage. After the TLV61070A starts up and the output voltage is above 2.2 V, the TLV61070A works with input voltage as low as 0.5 V.

7.3.2 Enable and Soft Start

When the input voltage is above the UVLO rising threshold and the EN pin is pulled to a voltage above 1.2 V, the TLV61070A is enabled and starts up. At the beginning, the TLV61070A charges the output capacitors with a current of about 185 mA when the output voltage is below 0.4 V. When the output voltage is charged above 0.4 V, the output current is changed to having output current capability to drive the 5-Ω resistance load. After the output voltage reaches the input voltage, the TLV61070A starts switching, and the output voltage ramps up further. The typical start-up time is 700 µs accounting from EN high to output, reaching target voltage for the application with input voltage is 2.5 V. Output voltage is 5 V, output effective capacitance is 10 µF, and no load. When the voltage at the EN pin is below 0.4 V, the internal enable comparator turns the device into Shutdown mode. In shutdown mode, the device is entirely turned off. The output is disconnected from the input power supply.

7.3.3 Switching Frequency

The TLV61070A switches at a quasi-constant 1-MHz frequency when the input voltage is above 1.5 V. When the input voltage is lower than 1.5 V, the switching frequency is reduced gradually to 0.55 MHz to improve the efficiency and get higher boost ratio. When the input voltage is below 1 V, the switching frequency is fixed at a quasi-constant 0.55 MHz.

7.3.4 Current Limit Operation

The TLV61070A uses a valley current limit sensing scheme. Current limit detection occurs during the off time by sensing of the voltage drop across the synchronous rectifier.

When the load current is increased such that the inductor current is above the current limit within the whole switching cycle time, the off-time is increased to allow the inductor current to decrease to this threshold before the next on time begins (so called frequency foldback mechanism). When the current limit is reached, the output voltage decreases during further load increase.

The maximum continuous output current ($I_{OUT(LC)}$) before entering current limit (CL) operation can be defined by 方程式 1.

$$I_{OUT(CL)} = (1-D) \times \left(I_{LIM} + \frac{1}{2} \Delta I_{L(P-P)} \right) \quad (1)$$

where

- D is the duty cycle
- $\Delta I_{L(P-P)}$ is the inductor ripple current

The duty cycle can be estimated by 方程式 2.

$$D = 1 - \frac{V_{IN} \times \eta}{V_{OUT}} \quad (2)$$

where

- V_{OUT} is the output voltage of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the efficiency of the converter, use 90% for most applications

The peak-to-peak inductor ripple current is calculated by 方程式 3.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \quad (3)$$

where

- L is the inductance value of the inductor
- f_{SW} is the switching frequency
- D is the duty cycle
- V_{IN} is the input voltage of the boost converter

7.3.5 Pass-Through Operation

When the input voltage is higher than the setting output voltage, the output voltage is higher than the target regulation voltage. When the output voltage is 101% of the setting target voltage, the TLV61070A stops switching and fully turns on the high-side PMOS FET. The device works in pass-through mode. The output voltage is the input voltage minus the voltage drop across the DCR of the inductor and the $R_{DS(on)}$ of the PMOS FET. When the output voltage drops below the 97% of the setting target voltage as the input voltage declines or the load current increases, the TLV61070A resumes switching again to regulate the output voltage.

7.3.6 Overvoltage Protection

The TLV61070A has an output overvoltage protection (OVP) to protect the device if the external feedback resistor divider is wrongly populated. When the output voltage is above 5.7 V typically, the device stops switching. Once the output voltage falls 0.1 V below the OVP threshold, the device resumes operating again.

7.3.7 Output Short-to-Ground Protection

The TLV61070A starts to limit the output current when the output voltage is below 1.8 V. The lower the output voltage reaches, the smaller the output current is. When the VOUT pin is short to ground, and the output voltage becomes less than 0.4 V, the output current is limited to approximately 185 mA. Once the short circuit is released, the TLV61070A goes through the soft start-up again to the regulated output voltage.

7.3.8 Thermal Shutdown

The TLV61070A goes into thermal shutdown once the junction temperature exceeds 150°C. When the junction temperature drops below the thermal shutdown recovery temperature, typically 130°C, the device starts operating again.

7.4 Device Functional Modes

The TLV61070A has two switching operation modes: PWM mode in moderate to heavy load conditions and power save mode with pulse frequency modulation (PFM) in light load conditions.

7.4.1 PWM Mode

The TLV61070A uses a quasi-constant 1.0-MHz frequency pulse width modulation (PWM) at moderate-to-heavy load current. Based on the input voltage to output voltage ratio, a circuit predicts the required on time. At the beginning of the switching cycle, the NMOS switching FET. The input voltage is applied across the inductor and the inductor current ramps up. In this phase, the output capacitor is discharged by the load current. When the on time expires, the main switch NMOS FET is turned off, and the rectifier PMOS FET is turned on. The inductor transfers its stored energy to replenish the output capacitor and supply the load. The inductor current declines because the output voltage is higher than the input voltage. When the inductor current hits the valley current threshold determined by the output of the error amplifier, the next switching cycle starts again.

The TLV61070A has a built-in compensation circuit that can accommodate a wide range of input voltage, output voltage, inductor value, and output capacitor value for stable operation.

7.4.2 Power Save Mode

The TLV61070A integrates a Power Save mode with PFM to improve efficiency at light load. When the load current decreases, the inductor valley current set by the output of the error amplifier no longer regulates the output voltage. When the inductor valley current hits the low limit, the output voltage exceeds the setting voltage as the load current decreases further. When the FB voltage hits the PFM reference voltage, the TLV61070A goes into the Power Save mode. In Power Save mode, when the FB voltage rises and hits the PFM reference voltage, the device continues switching for several cycles because of the delay time of the internal comparator, then it stops switching. The load is supplied by the output capacitor, and the output voltage declines. When the FB voltage falls below the PFM reference voltage, after the delay time of the comparator, the device starts switching again to ramp up the output voltage.

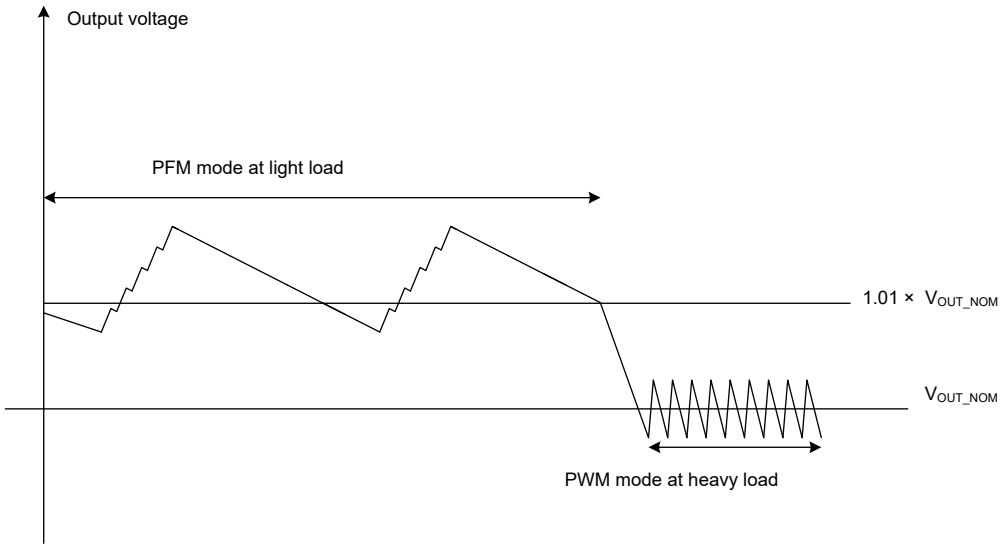


图 7-1. Output Voltage in PWM Mode and PFM Mode

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TLV61070A is a synchronous boost converter designed to operate from an input voltage supply range between 0.5 V and 5.5 V with a typical 2.5-A valley switch current limit. The TLV61070A typically operates at a quasi-constant 1-MHz frequency PWM at moderate-to-heavy load currents when the input voltage is above 1.5 V. The switching frequency changes to 0.55 MHz gradually with the input voltage changing from 1.5 V to 1 V for better efficiency and high step-up ratio. When the input voltage is below 1 V, the switching frequency is fixed at a quasi-constant 0.55 MHz. At light load currents, the TLV61070A converter operates in Power Save mode with PFM to achieve high efficiency over the entire load current range.

8.2 Typical Application

The TLV61070A provides a power supply solution for portable devices powered by batteries or backup applications powered by super-capacitors. The TLV61070A can output 5 V and 1.0 A from a single-cell Li-ion battery.

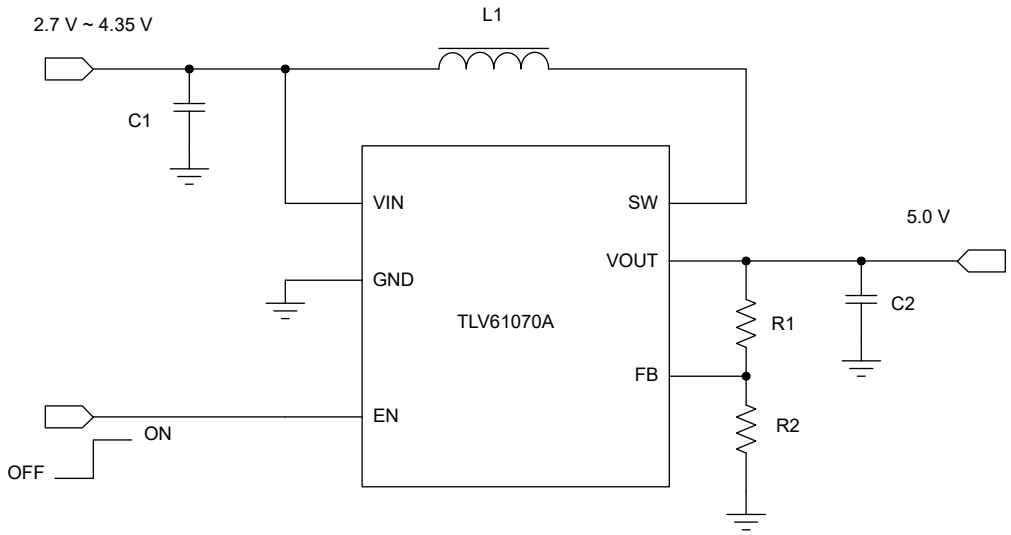


图 8-1. Li-ion Battery to 5-V Boost Converter

8.2.1 Design Requirements

The design parameters are listed in 表 8-1.

表 8-1. Design Parameters

PARAMETERS	VALUES
Input voltage	2.7 V to 4.35 V
Output voltage	5 V
Output current	1.0 A
Output voltage ripple	±50 mV

8.2.2 Detailed Design Procedure

8.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider (R1, R2 in 图 8-1). When the output voltage is regulated, the typical voltage at the FB pin is V_{REF}. Thus, the resistor divider is determined by 方程式 4.

$$R1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R2 \tag{4}$$

where

- V_{OUT} is the regulated output voltage
- V_{REF} is the internal reference voltage at the FB pin

For the best accuracy, keep R2 smaller than 100 kΩ to ensure the current flowing through R2 is at least 100 times larger than the FB pin leakage current. Changing R2 towards a lower value increases the immunity against noise injection. Changing the R2 towards a higher value reduces the quiescent current for achieving highest efficiency at low load currents.

8.2.2.2 Inductor Selection

Since the selection of the inductor affects steady-state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications: inductor value, saturation current, and DC resistance (DCR).

The TLV61070A is designed to work with inductor values between 2.2 µH and 4.7 µH. Follow 方程式 5 to 方程式 7 to calculate the inductor peak current for the application. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, and maximum load current of the application. To have enough design margins, choose the inductor value with –30% tolerances and low power-conversion efficiency for the calculation.

In a boost regulator, the inductor DC current can be calculated by 方程式 5.

$$I_{L(DC)} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{5}$$

where

- V_{OUT} is the output voltage of the boost converter
- I_{OUT} is the output current of the boost converter
- V_{IN} is the input voltage of the boost converter
- η is the power conversion efficiency, use 90% for most applications

The inductor ripple current is calculated by 方程式 6.

$$\Delta I_{L(P-P)} = \frac{V_{IN} \times D}{L \times f_{SW}} \tag{6}$$

where

- D is the duty cycle, which can be calculated by 方程式 2
- L is the inductance value of the inductor
- f_{SW} is the switching frequency
- V_{IN} is the input voltage of the boost converter

Therefore, the inductor peak current is calculated by 方程式 7.

$$I_{L(P)} = I_{L(DC)} + \frac{\Delta I_{L(P-P)}}{2} \quad (7)$$

Normally, it is advisable to work with an inductor peak-to-peak current of less than 40% of the average inductor current for maximum output current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. The saturation current of the inductor must be higher than the calculated peak inductor current. 表 8-2 lists the recommended inductors for the TLV61070A.

表 8-2. Recommended Inductors for the TLV61070A

PART NUMBER(1)	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (LxWxH)	VENDOR
XGL4030-222ME	2.2	15.0	7.0	4.0 × 4.0 × 3.1	Coilcraft
74438357022	2.2	13.5	7.0	4.1 x 4.1 x 3.1	Wurth Elecktronik

(1) See the *Third-party Products* disclaimer.

8.2.2.3 Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. The ripple voltage is related to capacitor capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple voltage can be calculated by 方程式 8.

$$C_{OUT} = \frac{I_{OUT} \times D_{MAX}}{f_{SW} \times V_{RIPPLE}} \quad (8)$$

where

- D_{MAX} is the maximum switching duty cycle
- V_{RIPPLE} is the peak-to-peak output ripple voltage
- I_{OUT} is the maximum output current
- f_{SW} is the switching frequency

The ESR impact on the output ripple must be considered if tantalum or aluminum electrolytic capacitors are used. The output peak-to-peak ripple voltage caused by the ESR of the output capacitors can be calculated by 方程式 9.

$$V_{RIPPLE(ESR)} = I_{L(P)} \times R_{ESR} \quad (9)$$

Take care when evaluating the derating of a ceramic capacitor under DC bias voltage, aging, and AC signal. For example, the DC bias voltage can significantly reduce capacitance. A ceramic capacitor can lose more than 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage. Increasing the output capacitor makes the output ripple voltage smaller in PWM mode.

TI recommends using the X5R or X7R ceramic output capacitor in the range of 4-µF to 1000-µF effective capacitance. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. Increasing the output capacitor makes the output ripple voltage smaller in PWM mode.

8.2.2.4 Loop Stability, Feedforward Capacitor Selection

When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop can be unstable.

The load transient response is another approach to check the loop stability. During the load transient recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the stability of the converters. Without any ringing, the loop has usually more than 45° of phase margin.

A feedforward capacitor (C3 in the 图 8-2) in parallel with R1 induces a pair of zero and pole in the loop transfer function. By setting the proper zero frequency, the feedforward capacitor can increase the phase margin to improve the loop stability. For large output capacitance more than 40 μF application, TI recommends a feedforward capacitor to set the zero frequency (f_{FFZ}) to 1 kHz. As for the input voltage lower than 1-V application, TI recommends to use the effective output capacitance is about 100 μF and set the zero frequency (f_{FFZ}) to 1 kHz. The value of the feedforward capacitor can be calculated by 方程式 10.

$$C3 = \frac{1}{2\pi \times f_{FFZ} \times R1} \tag{10}$$

where

- R1 is the resistor between the VOUT pin and FB pin
- f_{FFZ} is the zero frequency created by the feedforward capacitor

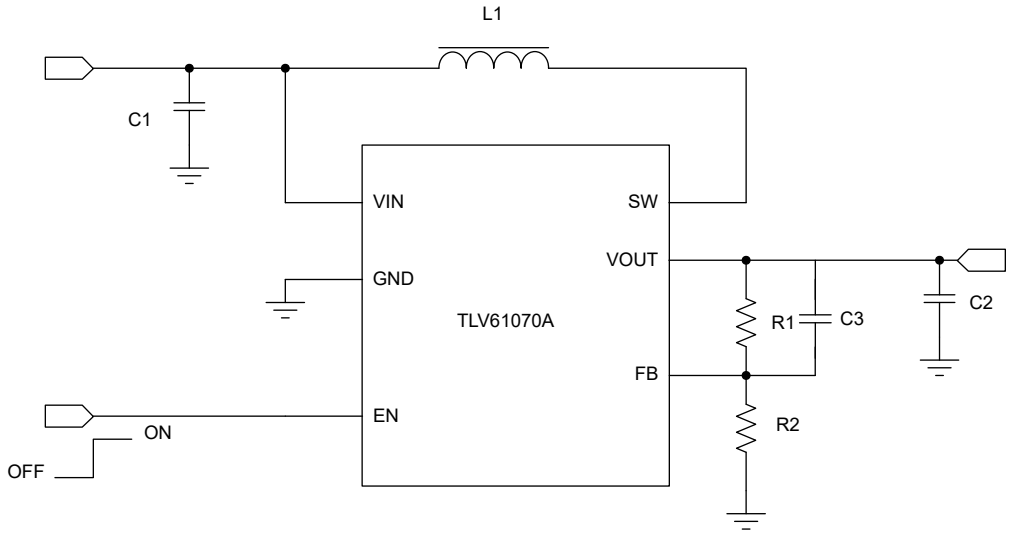
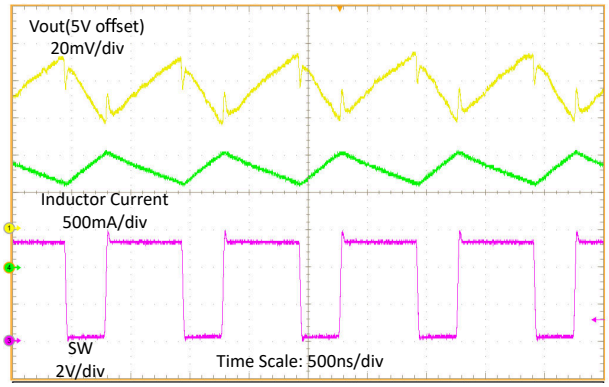


图 8-2. TLV61070A Circuit With Feedforward Capacitor

8.2.2.5 Input Capacitor Selection

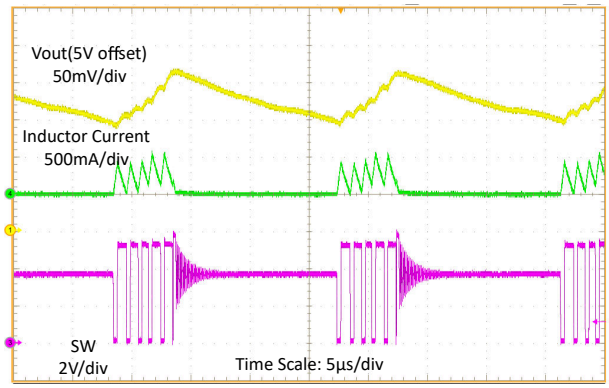
Multilayer X5R or X7R ceramic capacitors are excellent choices for the input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors must be located as close as possible to the device. While a 10- μF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations. Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. In this circumstance, place additional bulk capacitance (tantalum or aluminum electrolytic capacitor) between the ceramic input capacitor and the power source to reduce ringing that can occur between the inductance of the power source leads and ceramic input capacitor.

8.2.3 Application Curves



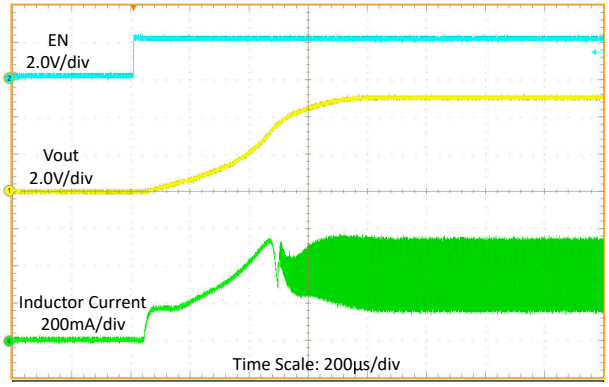
V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 1 A

图 8-3. Switching Waveform at Heavy Load



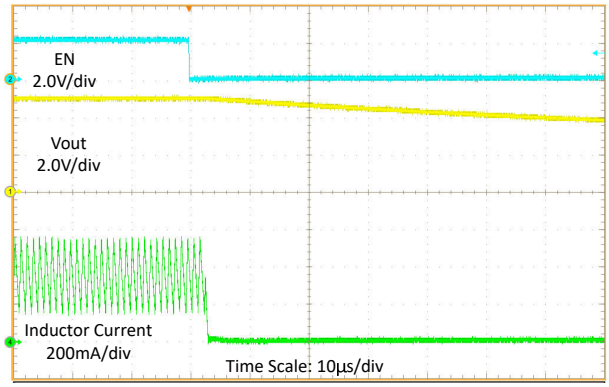
V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 50 mA

图 8-4. Switching Waveform at Light Load



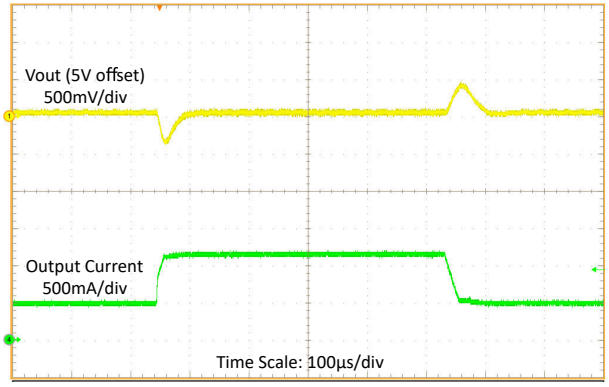
V_{IN} = 3.6 V, V_{OUT} = 5 V, 250 mA load current

图 8-5. Start-Up Waveform



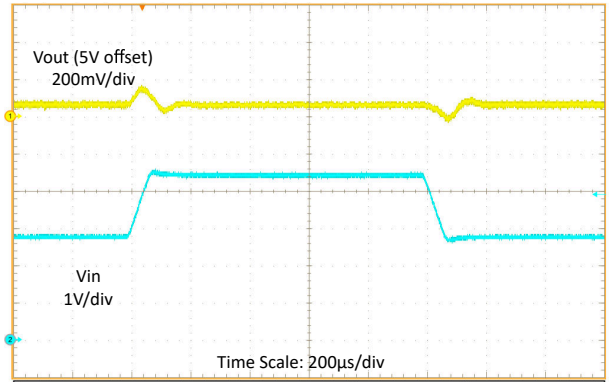
V_{IN} = 3.6 V, V_{OUT} = 5 V, 250 mA load current

图 8-6. Shutdown Waveform



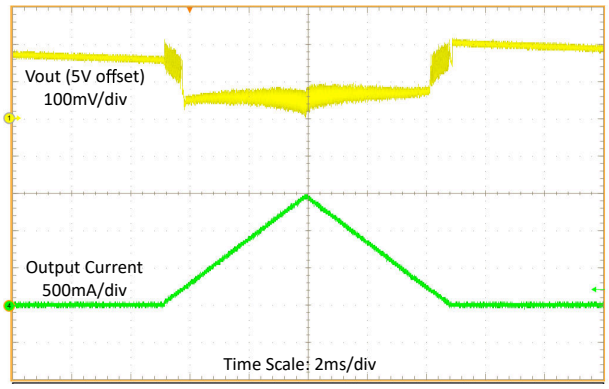
V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 800 mA to 1.5 A with 20- µ s slew rate

图 8-7. Load Transient



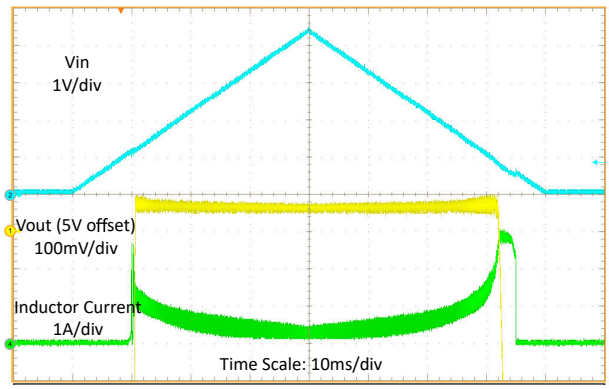
V_{IN} = 2.7 V to 4.35 V with 20- µ s slew rate, V_{OUT} = 5 V
I_{OUT} = 1 A

图 8-8. Line Transient



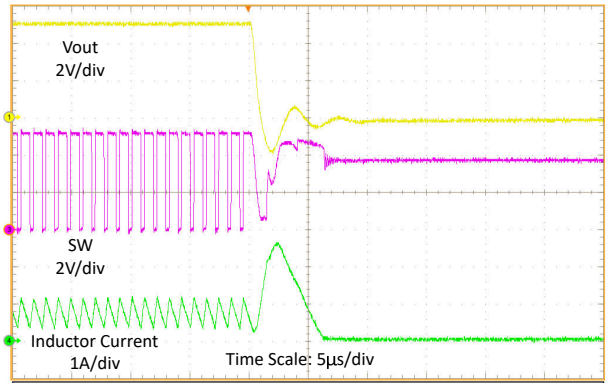
V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 0 A to 1.5 A Sweep

图 8-9. Load Sweep



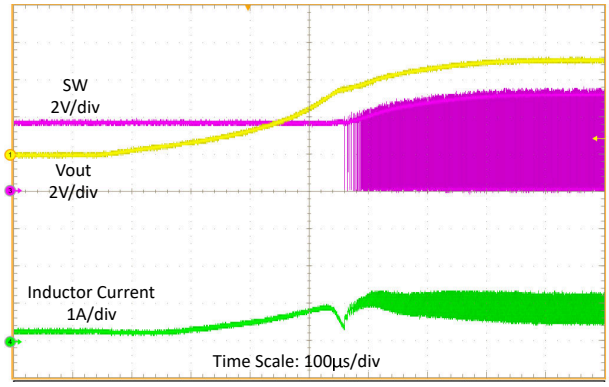
V_{IN} = 0 V to 4.35 V Sweep, V_{OUT} = 5 V, 250 mA load current

图 8-10. Line Sweep



V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 250 mA

图 8-11. Output Short Protection (Entry)



V_{IN} = 3.6 V, V_{OUT} = 5 V, I_{OUT} = 250 mA

图 8-12. Output Short Protection (Recover)

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 0.5 V to 5.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A typical choice is a tantalum or aluminum electrolytic capacitor with a value of 100 µF. Output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the TLV61070A.

8.4 Layout

8.4.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high-peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pin of the IC.

The feedback divider should be placed as close as possible to the ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

8.4.2 Layout Example

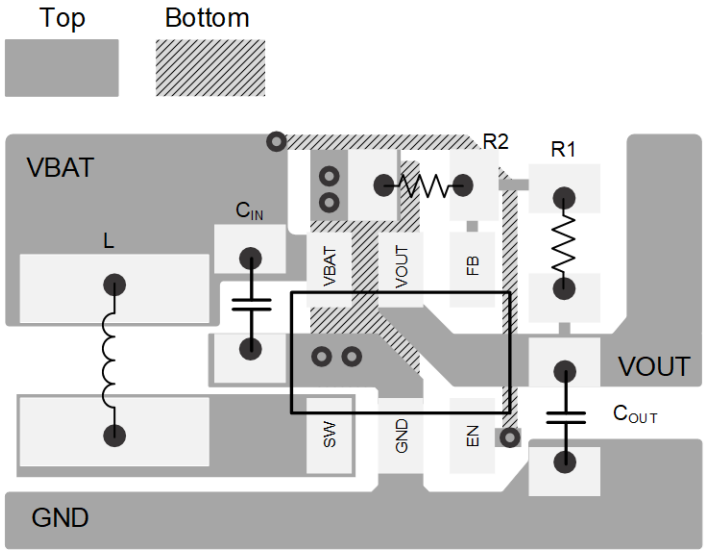


图 8-13. PCB Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 第三方产品免责声明

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9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV61070ADBVR	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	2N5F
TLV61070ADBVR.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2N5F

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

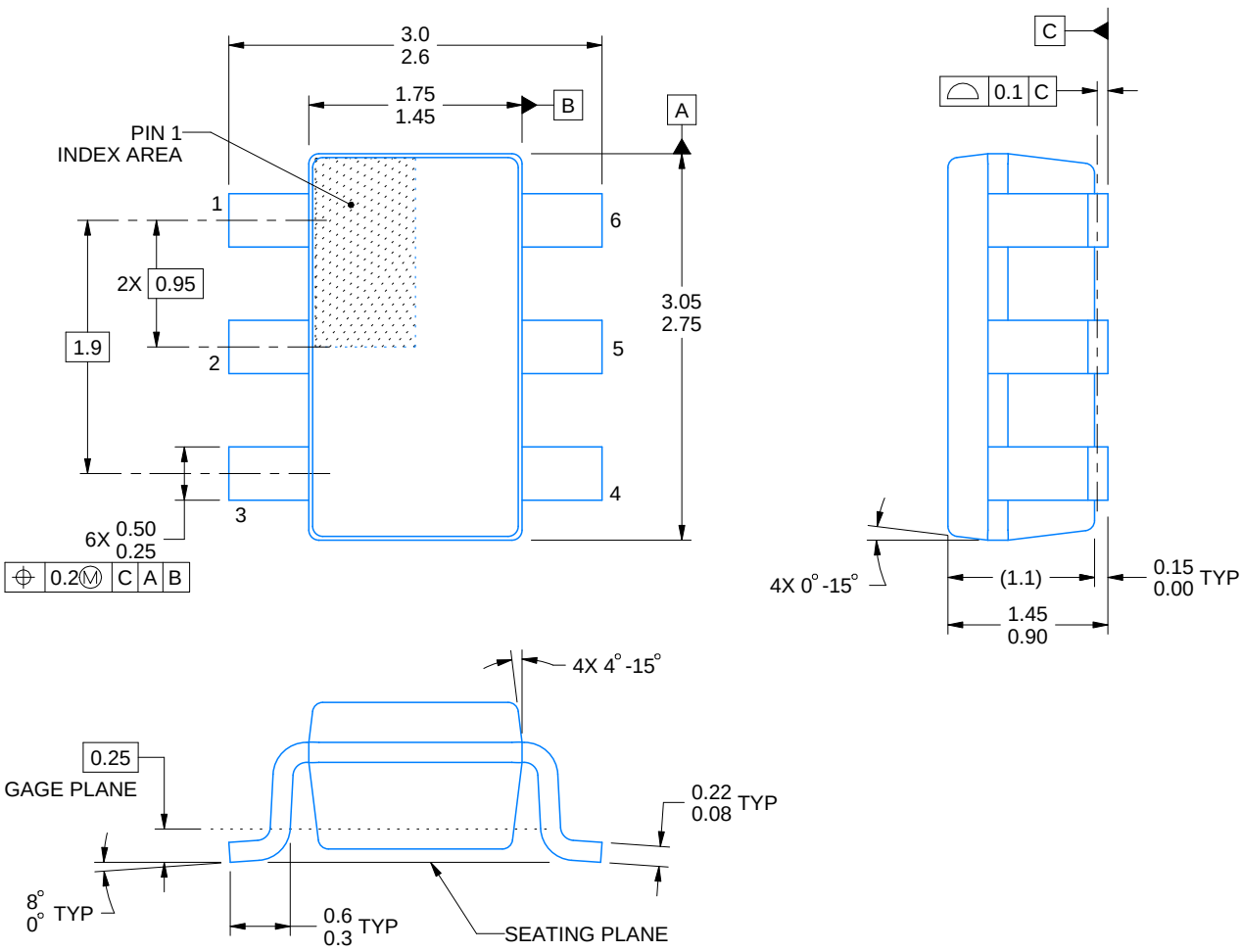
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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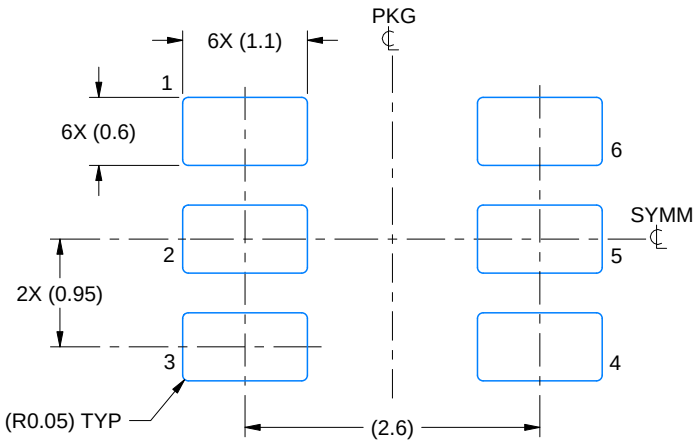
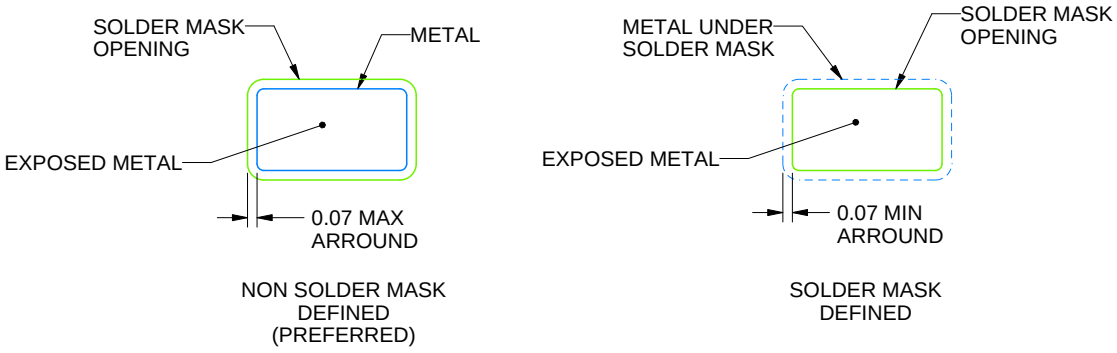
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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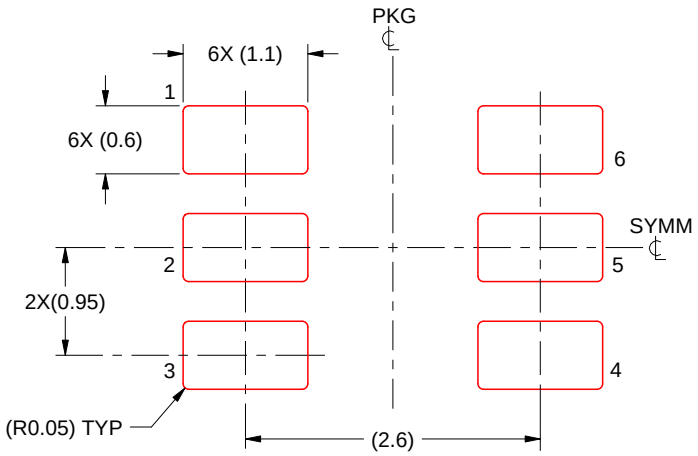
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月