- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 12 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Low Power . . . 500 μA Max**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **Low Input Offset Voltage**
  950 μV Max at T_A = 25°C (TLV226xA)
- **Wide Supply Voltage Range**
  2.7 V to 8 V
- **Macromodel Included**
- **Available in Q-Temp Automotive**
  HighRel Automotive Applications
  Configuration Control / Print Support
  Qualification to Automotive Standards

description

The TLV2262 and TLV2264 are dual and quad low voltage operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single or split supply applications. The TLV226x family offers a compromise between the micropower TLV225x and the ac performance of the TLC227x. It has low supply current for battery-powered applications, while still having adequate ac performance for applications that demand it. This family is fully characterized at 3 V and 5 V and is optimized for low-voltage applications. The noise performance has been dramatically improved over previous generations of CMOS amplifiers. Figure 1 depicts the low level of noise voltage for this CMOS amplifier, which has only 200 μA (typ) of supply current per amplifier.

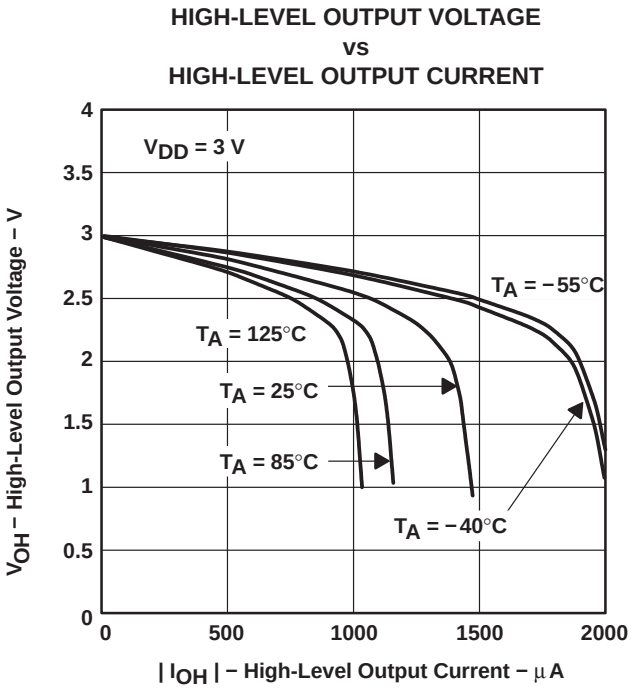


Figure 1

The TLV226x, exhibiting high input impedance and low noise, are excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micropower dissipation levels combined with 3-V operation, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature with single or split supplies makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLV226xA family is available and has a maximum input offset voltage of 950 μV.

The TLV2262/4 also makes great upgrades to the TLV2332/4 in standard designs. They offer increased output dynamic range, lower noise voltage and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications. For applications that require higher output drive and wider input voltage range, see the TLV2432 and TLV2442 devices. If your design requires single amplifiers, please see the TLV2211/21/31 family. These devices are single rail-to-rail operational amplifiers in the SOT-23 package. Their small size and low power consumption make them ideal for high density, battery-powered equipment.

TLV2262 AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	CERAMIC FLATPACK (U)
0°C to 70°C	2.5 mV	TLV2262CD	—	—	TLV2262CP	TLV2262CPWLE	—
−40°C to 125°C	950 µV 2.5 mV	TLV2262AID TLV2262ID	— —	— —	TLV2262AIP TLV2262IP	TLV2262AIPWLE —	— —
−40°C to 125°C	950 µV 2.5 mV	TLV2262AQD TLV2262QD	— —	— —	— —	— —	— —
−55°C to 125°C	950 µV 2.5 mV	— —	TLV2262AMFK TLV2262MFK	TLV2262AMJG TLV2262MJG	— —	— —	TLV2262AMU TLV2262MU

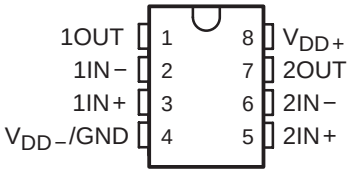
† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2262CDR).
‡ The PW package is available only left-end taped and reeled.
§ Chips are tested at 25°C.
¶ For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

TLV2264 AVAILABLE OPTIONS

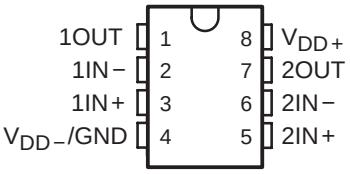
T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (J)	PLASTIC DIP (N)	TSSOP (PW)	CERAMIC FLATPACK (W)
−40°C to 125°C	950 µV 2.5 mV	TLV2264AID TLV2264ID	— —	— —	TLV2264AIN TLV2264IN	TLV2264AIPWLE —	— —
−40°C to 125°C	950 µV 2.5 mV	TLV2264AQD TLV2264QD	— —	— —	— —	— —	— —
−55°C to 125°C	950 µV 2.5 mV	— —	TLV2264AMFK TLV2264MFK	TLV2264AMJ TLV2264MJ	— —	— —	TLV2264AMW TLV2264MW

† The D packages are available taped and reeled. Add R suffix to device type (e.g., TLV2262IDR).
‡ The PW package is available only left-end taped and reeled.
§ Chips are tested at 25°C.
¶ For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

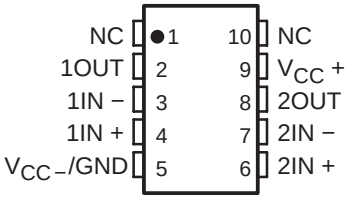
**TLV2262C, TLV2262AC
TLV2262I, TLV2262AI
TLV2262Q, TLV2262AQ
D, P, OR PW PACKAGE
(TOP VIEW)**



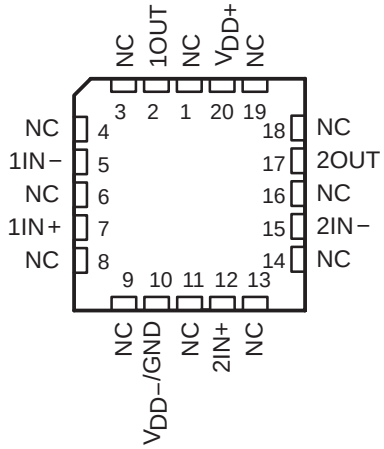
**TLV2262M, TLV2262AM
JG PACKAGE
(TOP VIEW)**



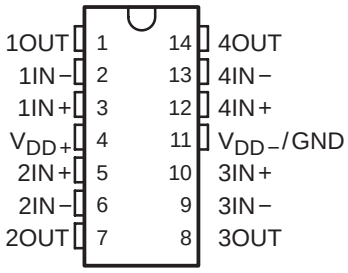
**TLV2662M, TLV2262AM
U PACKAGE
(TOP VIEW)**



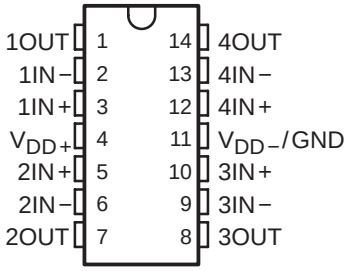
**TLV2262M, TLV2262AM
FK PACKAGE
(TOP VIEW)**



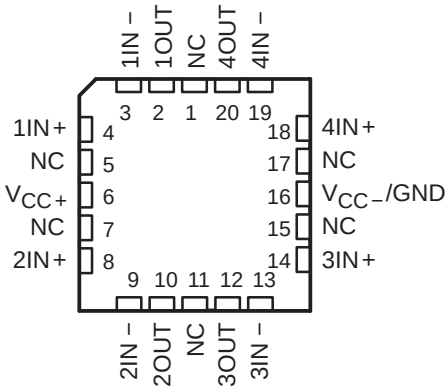
**TLV2264I, TLV2264AI
TLV2264Q, TLV2264AQ
D, N, OR PW PACKAGE
(TOP VIEW)**



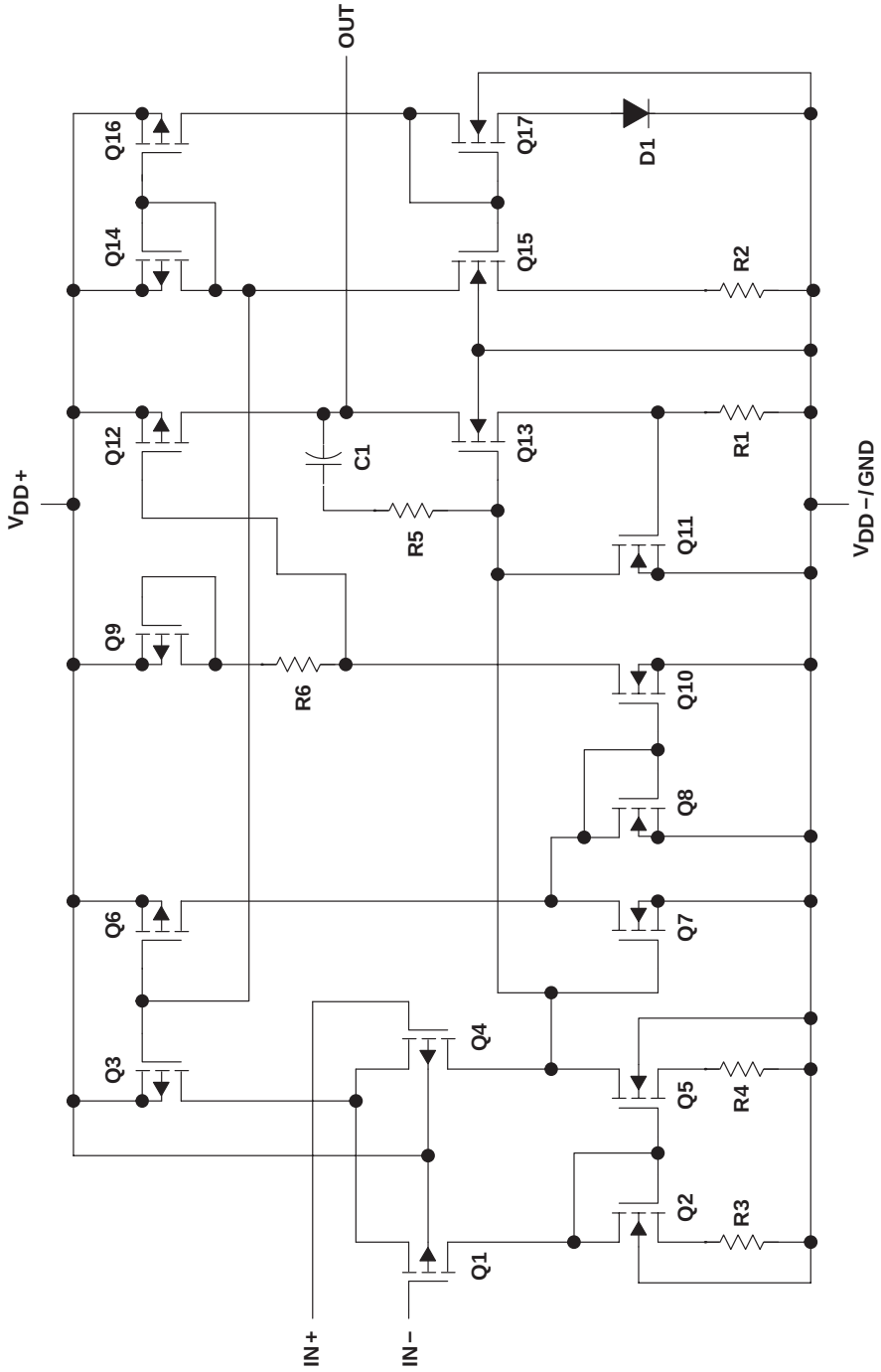
**TLV2264M, TLV2264AM
J OR W PACKAGE
(TOP VIEW)**



**TLV2264M, TLV2264AM
FK PACKAGE
(TOP VIEW)**



equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLV2252	TLV2254
Transistors	38	76
Resistors	28	54
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 16 V
Differential input voltage, V_{ID} (see Note 2) . . . . . $\pm V_{DD}$
Input voltage range, V_I (any input, see Note 1) . . . . . V_{DD-} −0.3 V to V_{DD+}
Input current, I_I (each input) . . . . . ±5 mA
Output current, I_O . . . . . ±50 mA
Total current into V_{DD+} . . . . . ±50 mA
Total current out of V_{DD-} . . . . . ±50 mA
Duration of short-circuit current (at or below) 25°C (see Note 3) . . . . . unlimited
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A: I suffix . . . . . −40°C to 125°C
Q suffix . . . . . −40°C to 125°C
M suffix . . . . . −55°C to 125°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to V_{DD-}.
2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows when input is brought below V_{DD-} − 0.3 V.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D−8	725 mW	5.8 mW/°C	377 mW	145 mW
D−14	950 mW	7.6 mW/°C	494 mW	190 mW
FK	1375 mW	11.0 mW/°C	715 mW	275 mW
J	1375 mW	11.0 mW/°C	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	—	210 mW
N	1150 mW	9.2 mW/°C	598 mW	—
P	1000 mW	8.0 mW/°C	520 mW	200 mW
PW−8	525 mW	4.2 mW/°C	273 mW	105 mW
PW−14	700 mW	5.6 mW/°C	364 mW	—
U	700 mW	5.5 mW/°C	—	150 mW
W	700 mW	5.5 mW/°C	370 mW	150 mW

recommended operating conditions

	I SUFFIX		Q SUFFIX		M SUFFIX		UNIT
	MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, $V_{DD\pm}$ (see Note 1)	2.7	8	2.7	8	2.7	8	V
Input voltage range, V_I	V_{DD-}	V_{DD+} −1.3	V_{DD-}	V_{DD+} −1.3	V_{DD-}	V_{DD+} −1.3	V
Common-mode input voltage, V_{IC}	V_{DD-}	V_{DD+} −1.3	V_{DD-}	V_{DD+} −1.3	V_{DD-}	V_{DD+} −1.3	V
Operating free-air temperature, T_A	−40	125	−40	125	−55	125	°C

NOTE 1: All voltage values, except differential voltages, are with respect to V_{DD-}.

TLV2262I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262I			TLV2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		2.99			2.99		V
		I_{OH} = −100 μA		25°C	2.85			2.85			
				Full range	2.825			2.825			
		I_{OH} = −400 μA		25°C	2.7			2.7			
				Full range	2.65			2.65			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 μA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 μA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	30			30			
			R_L = 1 MΩ‡	25°C		100			100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	100		dB
				Full range	80			80			

† Full range is − 40°C to 125°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2262I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2262I			TLV2262AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current	V_O = 1.5 V, No load	25°C		400	500		400	500	µA
			Full range			500			500	

† Full range is − 40°C to 125°C.

TLV2262I operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262I			TLV2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.1 V to 1.9 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		µV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		395			395		kHz
t_s	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		µs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		55°			55°		
	Gain margin			25°C		11			11		dB

† Full range is − 40°C to 125°C.
‡ Referenced to 1.5 V

TLV2262I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262I			TLV2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤5 mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.6			4.6			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
				Full range	55			55			
			R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2262I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2262I			TLV2262AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		400	500		400	500	µA
			Full range			500			500	

† Full range is − 40°C to 125°C.

TLV2262I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262I			TLV2262AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		µV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		µs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V

TLV2264I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264I			TLV2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		2.99			2.99		V
		I_{OH} = −100 µA		25°C	2.85			2.85			
				Full range	2.825			2.825			
		I_{OH} = −400 µA		25°C	2.7			2.7			
				Full range	2.65			2.65			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 µA	25°C		100			100		
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200			200		
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	30			30			
			R_L = 1 MΩ‡	25°C		100			100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	100		dB
				Full range	80			80			

† Full range is − 40°C to 125°C.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2264I electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2264I			TLV2264AI			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 1.5 V, No load	25°C		0.8	1		0.8	1	mA
			Full range			1			1	

† Full range is − 40°C to 125°C.

TLV2264I operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264I			TLV2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.7 V to 1.7 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		395			395		kHz
t_s	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		55°			55°		
	Gain margin			25°C		11			11		dB

† Full range is − 40°C to 125°C.
‡ Referenced to 1.5 V

TLV2264I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264I			TLV2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 85°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				85°C			150			150	
				Full range			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				85°C			150			150	
				Full range			800			800	
V_{ICR}	Common-mode input voltage range	$\|V_{IO}\|$ ≤5 mV, R_S = 50 Ω		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99			4.99		V
		I_{OH} = −100 µA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 µA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.6			4.6			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
				Full range	55			55			
			R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2264I electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264I			TLV2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is − 40°C to 125°C.

TLV2264I operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264I			TLV2264AI			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 1.4 V to 2.6 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.3			0.3			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is − 40°C to 125°C.
‡ Referenced to 2.5 V

TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_O = 0,	V_{IC} = 0, R_S = 50 Ω	25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert$ ≤5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		2.99			2.99		V
		I_{OH} = −100 µA		25°C	2.85			2.85			
				Full range	2.82			2.82			
		I_{OH} = −400 µA		25°C	2.7			2.7			
				Full range	2.55			2.55			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 µA	25°C		100	150		100	150	
				Full range			165			165	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200	300		200	300	
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	25			25			
			R_L = 1 MΩ‡	25°C		100			100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V,	R_S = 50 Ω	25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	100		dB
				Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V

NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current	V_O = 1.5 V, No load	25°C		400	500		400	500	µA
			Full range			500			500	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLV2262Q and TLV2262M operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 1.7 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/µs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		µV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		395			395		kHz
t_s	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		µs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		55°			55°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V

TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \le$5 mV, R_S = 50 Ω		25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		4.99			4.99		V
		I_{OH} = −100 µA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 µA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 µA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 µA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
				Full range	50			50			
			R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	P package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V,	R_S = 50 Ω	25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2262Q and TLV2262M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current	V_O = 2.5 V, No load	25°C		400	500		400	500	μA
			Full range			500			500	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLV2262Q and TLV2262M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2262Q, TLV2262M			TLV2262AQ, TLV2262AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±1.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	µV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		µV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		µV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	R_S = 50 Ω,	$\lvert V_{IO}\rvert \le$ 5 mV	25°C	0 to 2	−0.3 to 2.2		0 to 2	−0.3 to 2.2		V
				Full range	0 to 1.7			0 to 1.7			
V_{OH}	High-level output voltage	I_{OH} = −20 µA		25°C		2.99			2.99		V
		I_{OH} = −100 µA		25°C	2.85			2.85			
				Full range	2.82			2.82			
		I_{OH} = −400 µA		25°C	2.7			2.7			
				Full range	2.6			2.6			
V_{OL}	Low-level output voltage	V_{IC} = 1.5 V,	I_{OL} = 50 µA	25°C		10			10		mV
		V_{IC} = 1.5 V,	I_{OL} = 500 µA	25°C		100	150		100	150	
				Full range			150			150	
		V_{IC} = 1.5 V,	I_{OL} = 1 mA	25°C		200	300		200	300	
				Full range			300			300	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1.5 V, V_O = 1 V to 2 V	R_L = 50 kΩ‡	25°C	60	100		60	100		V/mV
				Full range	25			25			
			R_L = 1 MΩ‡	25°C		100			100		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		270			270		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 1.7 V, V_O = 1.5 V, R_S = 50 Ω		25°C	65	75		65	77		dB
				Full range	60			60			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 2.7 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	100		dB
				Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, V_{DD} = 3 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 1.5 V, No load	25°C		0.8	1		0.8	1	mA
			Full range			1			1	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLV2264Q and TLV2264M operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 1.7 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		43			43		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.6			0.6		μV
		f = 0.1 Hz to 10 Hz		25°C		1			1		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.03%			0.03%		
			A_V = 10			0.05%			0.05%		
	Gain-bandwidth product	f = 1 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.67			0.67		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 1 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		395			395		kHz
t_s	Settling time	A_V = −1, Step = 1 V to 2 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		5.6			5.6		μs
			To 0.01%			12.5			12.5		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		55°			55°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 1.5 V

TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{DD\pm}$ = ±2.5 V, V_{IC} = 0, V_O = 0, R_S = 50 Ω		25°C		300	2500		300	950	μV
				Full range			3000			1500	
α_{VIO}	Temperature coefficient of input offset voltage			25°C to 125°C		2			2		μV/°C
	Input offset voltage long-term drift (see Note 4)			25°C		0.003			0.003		μV/mo
I_{IO}	Input offset current			25°C		0.5	60		0.5	60	pA
				125°C			800			800	
I_{IB}	Input bias current			25°C		1	60		1	60	pA
				125°C			800			800	
V_{ICR}	Common-mode input voltage range	$|V_{IO}| \le$5 mV,	R_S = 50 Ω	25°C	0 to 4	−0.3 to 4.2		0 to 4	−0.3 to 4.2		V
				Full range	0 to 3.5			0 to 3.5			
V_{OH}	High-level output voltage	I_{OH} = −20 μA		25°C		4.99			4.99		V
		I_{OH} = −100 μA		25°C	4.85	4.94		4.85	4.94		
				Full range	4.82			4.82			
		I_{OH} = −400 μA		25°C	4.7	4.85		4.7	4.85		
				Full range	4.5			4.5			
V_{OL}	Low-level output voltage	V_{IC} = 2.5 V,	I_{OL} = 50 μA	25°C		0.01			0.01		V
		V_{IC} = 2.5 V,	I_{OL} = 500 μA	25°C		0.09	0.15		0.09	0.15	
				Full range			0.15			0.15	
		V_{IC} = 2.5 V,	I_{OL} = 1 mA	25°C		0.2	0.3		0.2	0.3	
				Full range			0.3			0.3	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 2.5 V, V_O = 1 V to 4 V	R_L = 50 kΩ‡	25°C	80	170		80	170		V/mV
				Full range	50			50			
			R_L = 1 MΩ‡	25°C		550			550		
$r_{i(d)}$	Differential input resistance			25°C		10^{12}			10^{12}		Ω
$r_{i(c)}$	Common-mode input resistance			25°C		10^{12}			10^{12}		Ω
$c_{i(c)}$	Common-mode input capacitance	f = 10 kHz,	N package	25°C		8			8		pF
z_o	Closed-loop output impedance	f = 100 kHz,	A_V = 10	25°C		240			240		Ω
CMRR	Common-mode rejection ratio	V_{IC} = 0 to 2.7 V, V_O = 2.5 V, R_S = 50 Ω		25°C	70	83		70	83		dB
				Full range	70			70			
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 4.4 V to 8 V, V_{IC} = V_{DD}/2,	No load	25°C	80	95		80	95		dB
				Full range	80			80			

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V
NOTE 4: Typical values are based on the input offset voltage shift observed through 500 hours of operating life test at T_A = 150°C extrapolated to T_A = 25°C using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLV2264Q and TLV2264M electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS		T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Supply current (four amplifiers)	V_O = 2.5 V,	No load	25°C		0.8	1		0.8	1	mA
				Full range			1			1	

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.

TLV2264Q and TLV2264M operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A†	TLV2264Q, TLV2264M			TLV2264AQ, TLV2264AM			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain	V_O = 0.5 V to 3.5 V, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C	0.35	0.55		0.35	0.55		V/μs
				Full range	0.25			0.25			
V_n	Equivalent input noise voltage	f = 10 Hz		25°C		40			40		nV/√Hz
		f = 1 kHz		25°C		12			12		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	f = 0.1 Hz to 1 Hz		25°C		0.7			0.7		μV
		f = 0.1 Hz to 10 Hz		25°C		1.3			1.3		
I_n	Equivalent input noise current			25°C		0.6			0.6		fA/√Hz
THD + N	Total harmonic distortion plus noise	V_O = 0.5 V to 2.5 V, f = 20 kHz, R_L = 50 kΩ‡	A_V = 1	25°C		0.017%			0.017%		
			A_V = 10			0.03%			0.03%		
	Gain-bandwidth product	f = 50 kHz, C_L = 100 pF‡	R_L = 50 kΩ‡,	25°C		0.71			0.71		MHz
B_{OM}	Maximum output-swing bandwidth	$V_{O(PP)}$ = 2 V, R_L = 50 kΩ‡,	A_V = 1, C_L = 100 pF‡	25°C		185			185		kHz
t_s	Settling time	A_V = −1, Step = 0.5 V to 2.5 V, R_L = 50 kΩ‡, C_L = 100 pF‡	To 0.1%	25°C		6.4			6.4		μs
			To 0.01%			14.1			14.1		
ϕ_m	Phase margin at unity gain	R_L = 50 kΩ‡,	C_L = 100 pF‡	25°C		56°			56°		
	Gain margin			25°C		11			11		dB

† Full range is −40°C to 125°C for Q level part, −55°C to 125°C for M level part.
‡ Referenced to 2.5 V

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode voltage	2 − 5 6, 7
α_{VIO}	Input offset voltage temperature coefficient	Distribution	8 − 11
I_{IB}/I_{IO}	Input bias and input offset currents	vs Free-air temperature	12
V_I	Input voltage	vs Supply voltage vs Free-air temperature	13 14
V_{OH}	High-level output voltage	vs High-level output current	15, 18
V_{OL}	Low-level output voltage	vs Low-level output current	16, 17, 19
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency	20
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature	21 22
V_{ID}	Differential input voltage	vs Output voltage	23, 24
A_{VD}	Differential voltage amplification	vs Load resistance	25
A_{VD}	Large-signal differential voltage amplification	vs Frequency vs Free-air temperature	26, 27 28, 29
z_o	Output impedance	vs Frequency	30, 31
CMRR	Common-mode rejection ratio	vs Frequency vs Free-air temperature	32 33
k_{SVR}	Supply-voltage rejection ratio	vs Frequency vs Free-air temperature	34, 35 36, 37
I_{DD}	Supply current	vs Free-air temperature	38, 39
SR	Slew rate	vs Load capacitance vs Free-air temperature	40 41
V_O	Inverting large-signal pulse response		42, 43
V_O	Voltage-follower large-signal pulse response		44, 45
V_O	Inverting small-signal pulse response		46, 47
V_O	Voltage-follower small-signal pulse response		48, 49
V_n	Equivalent input noise voltage	vs Frequency	50, 51
	Input noise voltage	Over a 10-second period	52
	Integrated noise voltage	vs Frequency	53
THD + N	Total harmonic distortion plus noise	vs Frequency	54
	Gain-bandwidth product	vs Supply voltage vs Free-air temperature	55 56
ϕ_m	Phase margin	vs Frequency vs Load capacitance	26, 27 57
	Gain margin	vs Load capacitance	58
B_1	Unity-gain bandwidth	vs Load capacitance	59
	Overestimation of phase margin	vs Load capacitance	60

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

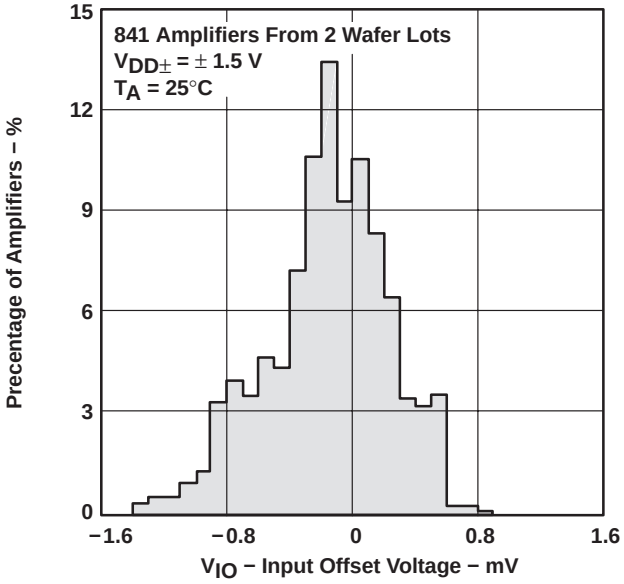


Figure 2

DISTRIBUTION OF TLV2262
INPUT OFFSET VOLTAGE

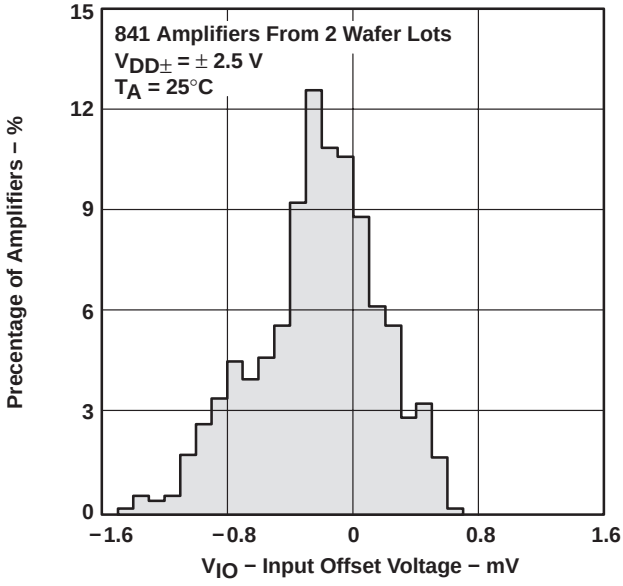


Figure 3

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE

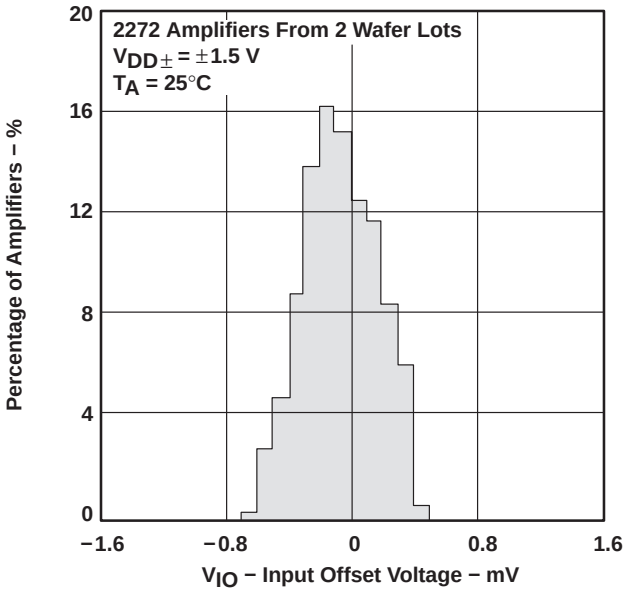


Figure 4

DISTRIBUTION OF TLV2264
INPUT OFFSET VOLTAGE

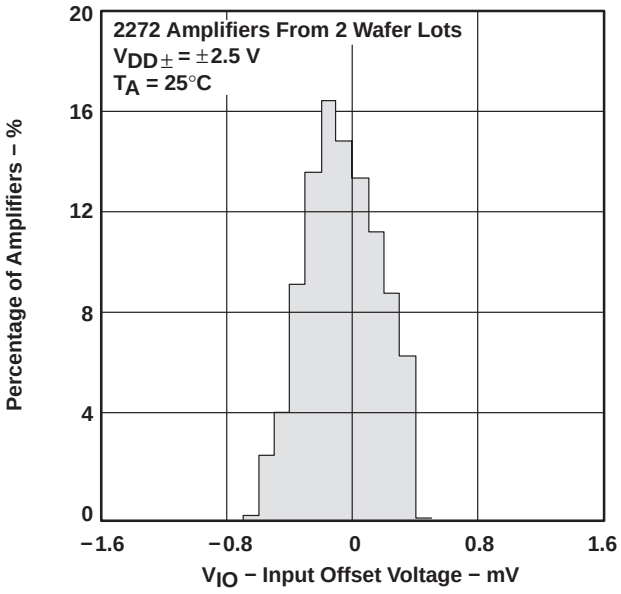


Figure 5

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE† vs COMMON-MODE INPUT VOLTAGE

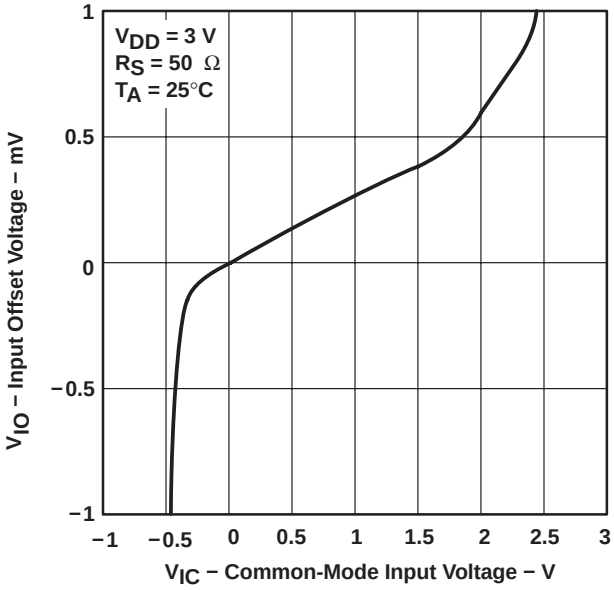


Figure 6

INPUT OFFSET VOLTAGE† vs COMMON-MODE INPUT VOLTAGE

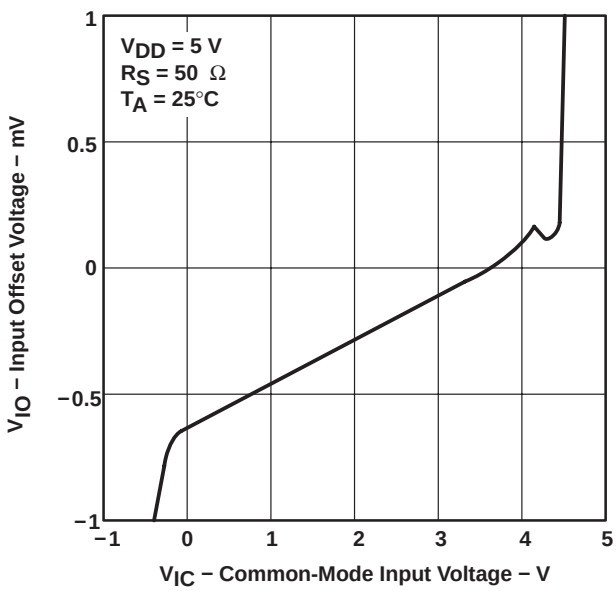


Figure 7

DISTRIBUTION OF TLV2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

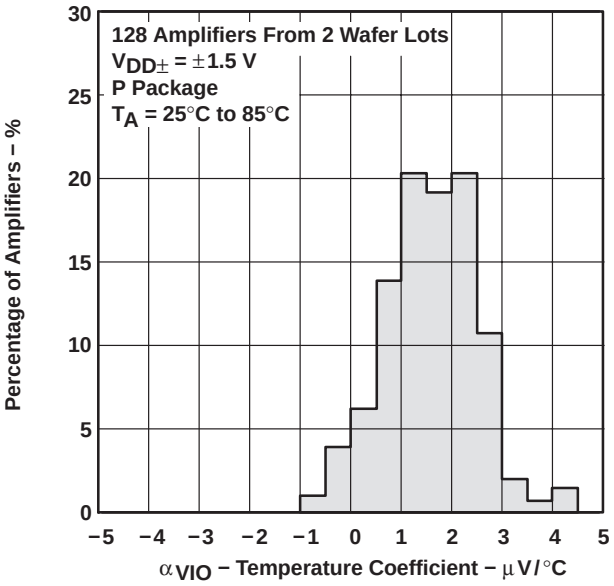


Figure 8

DISTRIBUTION OF TLV2262 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

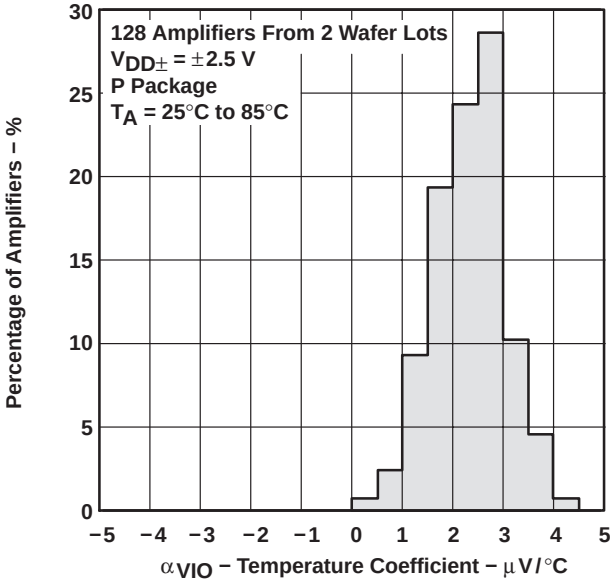


Figure 9

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

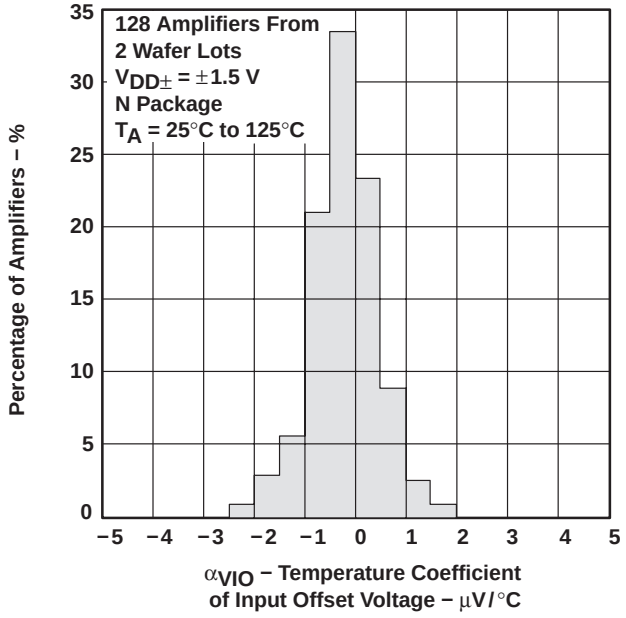


Figure 10

DISTRIBUTION OF TLV2264 INPUT OFFSET VOLTAGE TEMPERATURE COEFFICIENT

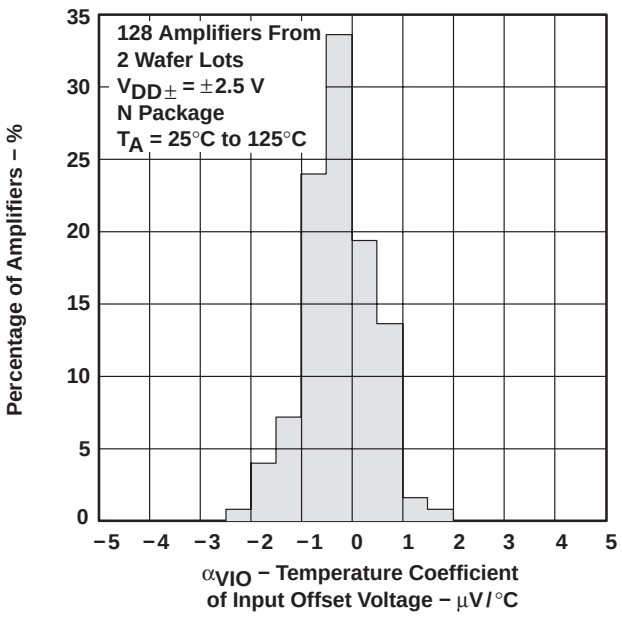


Figure 11

INPUT BIAS AND INPUT OFFSET CURRENTS† vs FREE-AIR TEMPERATURE

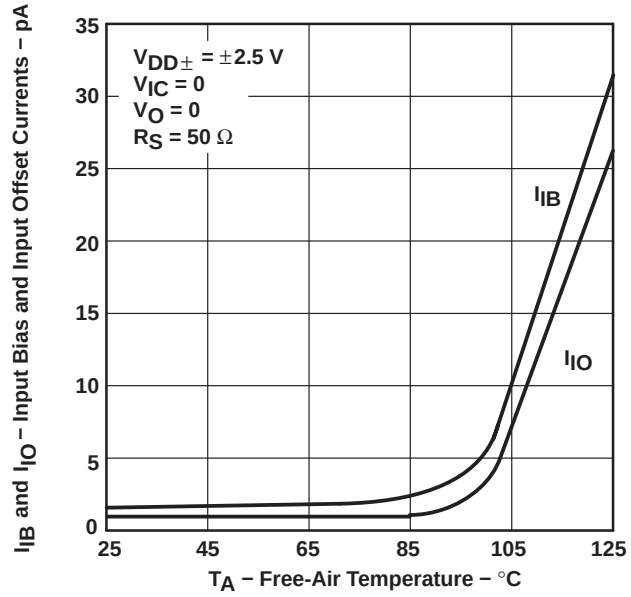


Figure 12

INPUT VOLTAGE vs SUPPLY VOLTAGE

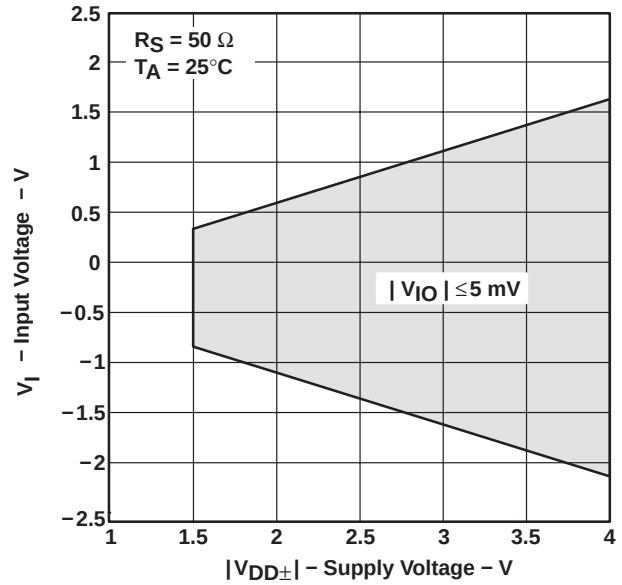


Figure 13

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

INPUT VOLTAGE†‡ vs FREE-AIR TEMPERATURE

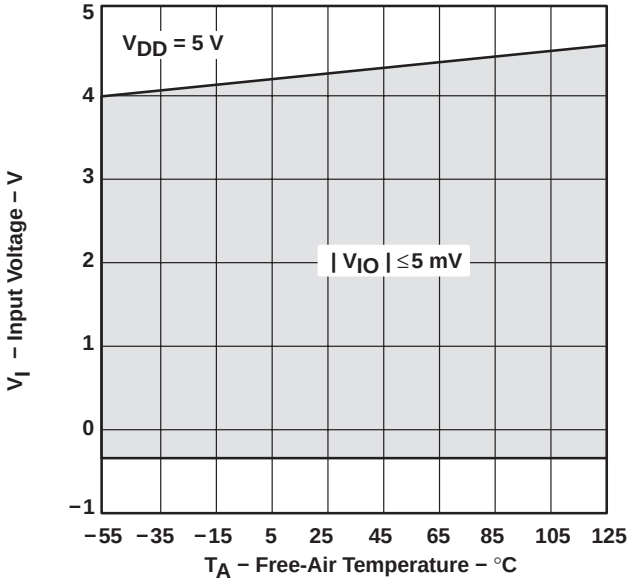


Figure 14

HIGH-LEVEL OUTPUT VOLTAGE†‡ vs HIGH-LEVEL OUTPUT CURRENT

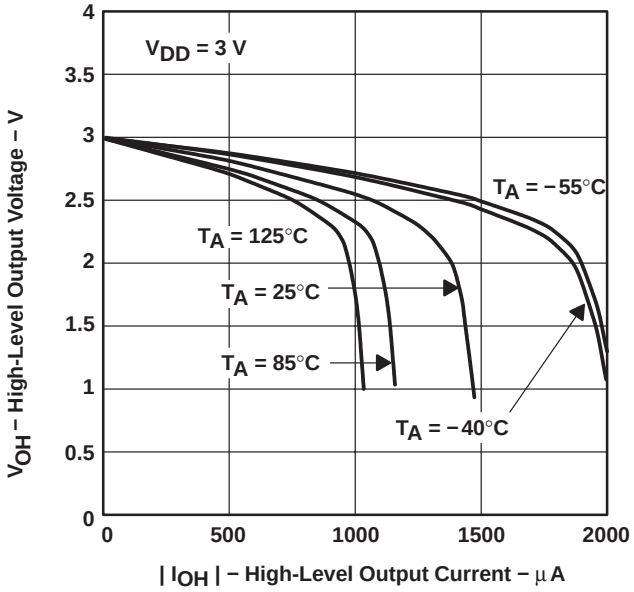


Figure 15

LOW-LEVEL OUTPUT VOLTAGE‡ vs LOW-LEVEL OUTPUT CURRENT

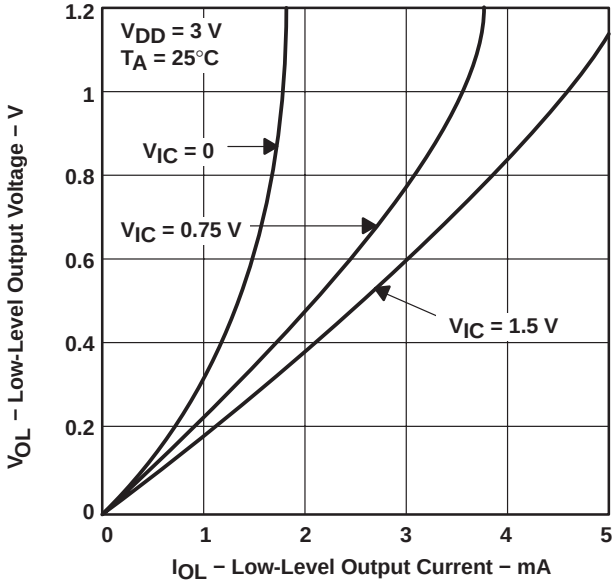


Figure 16

LOW-LEVEL OUTPUT VOLTAGE†‡ vs LOW-LEVEL OUTPUT CURRENT

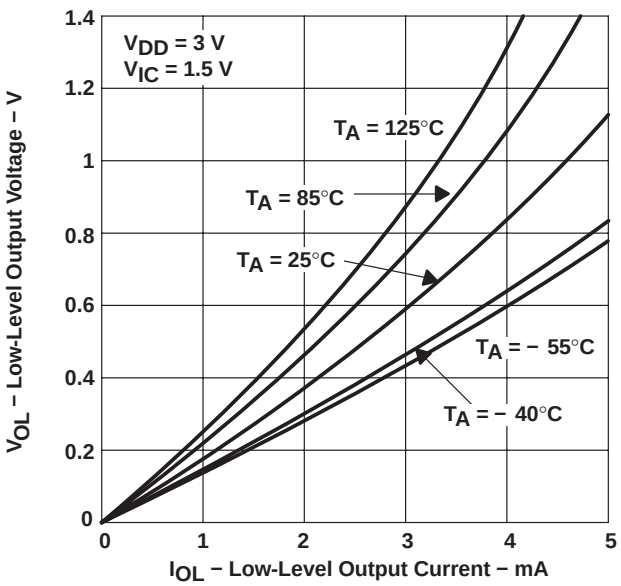


Figure 17

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE†‡ vs HIGH-LEVEL OUTPUT CURRENT

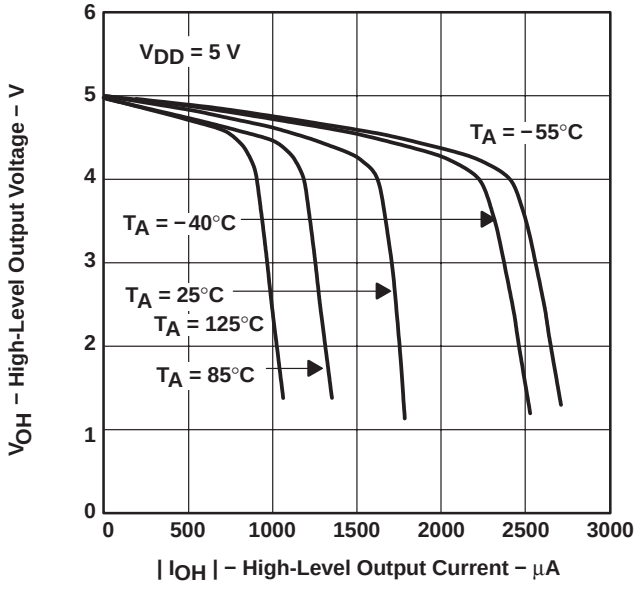


Figure 18

LOW-LEVEL OUTPUT VOLTAGE†‡ vs LOW-LEVEL OUTPUT CURRENT

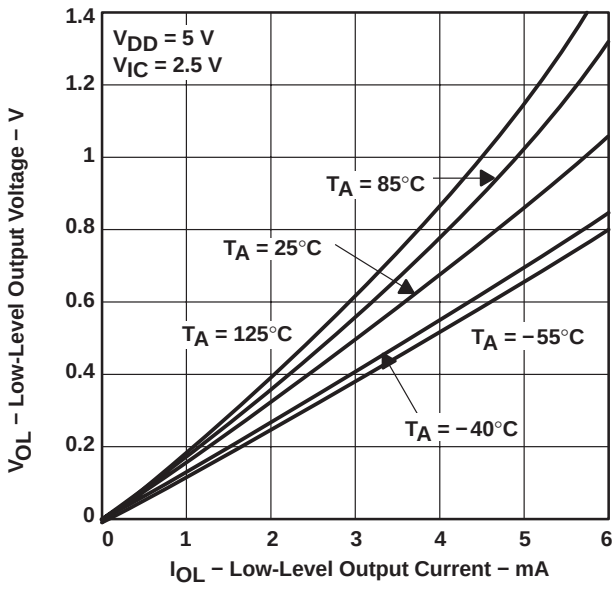


Figure 19

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE‡ vs FREQUENCY

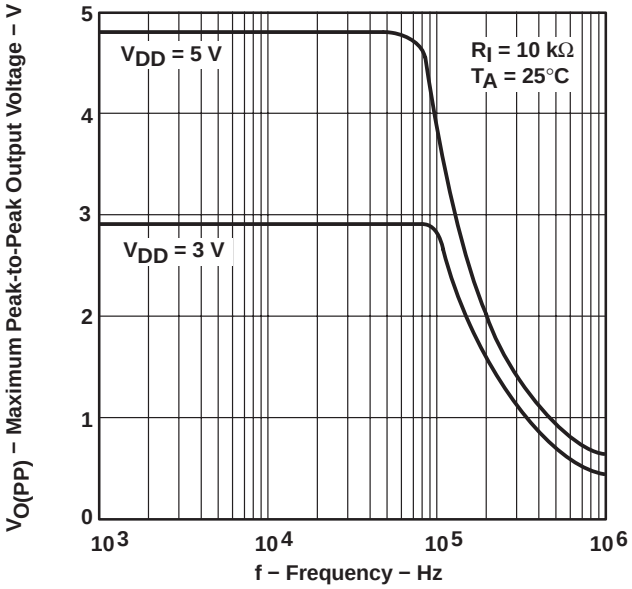


Figure 20

SHORT-CIRCUIT OUTPUT CURRENT vs SUPPLY VOLTAGE

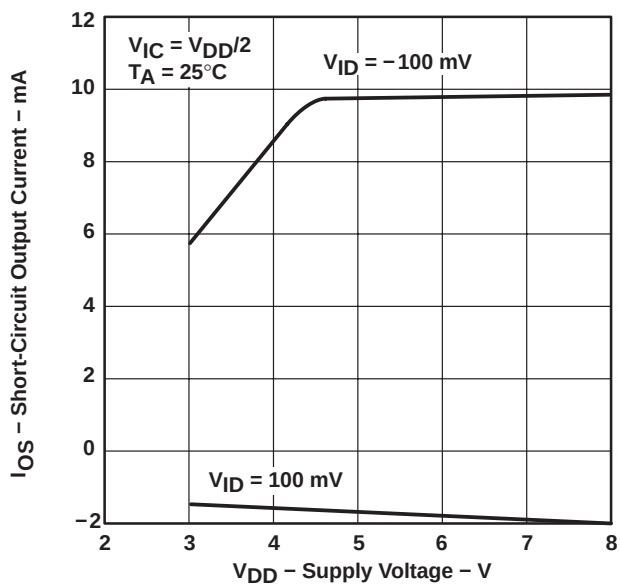


Figure 21

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

SHORT-CIRCUIT OUTPUT CURRENT† vs FREE-AIR TEMPERATURE

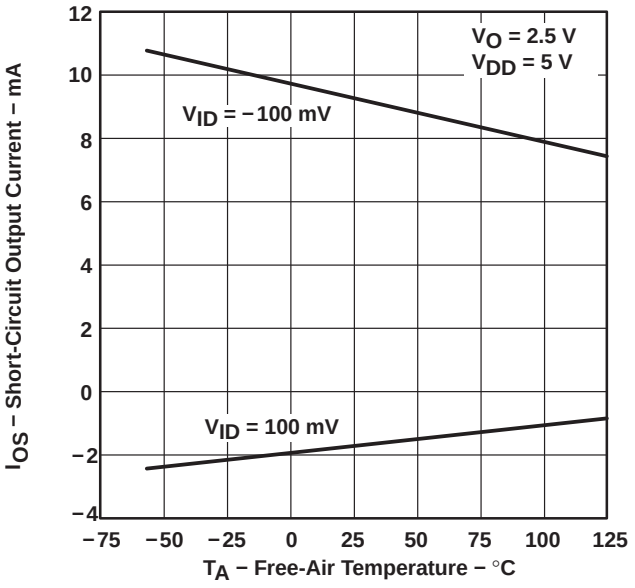


Figure 22

DIFFERENTIAL INPUT VOLTAGE‡ vs OUTPUT VOLTAGE

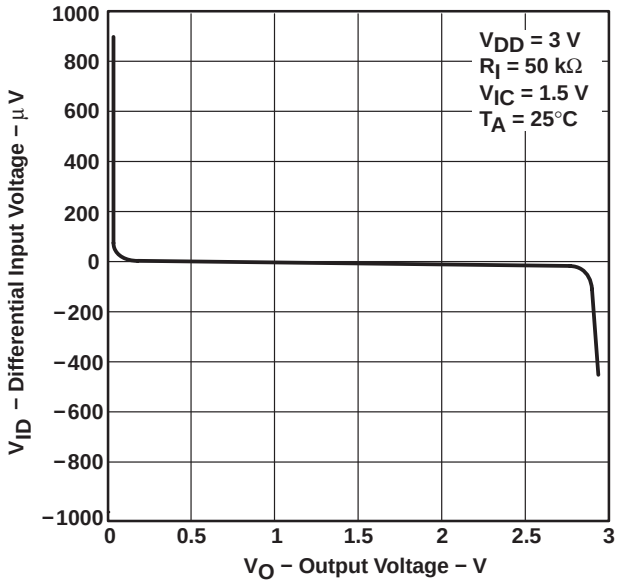


Figure 23

DIFFERENTIAL INPUT VOLTAGE‡ vs OUTPUT VOLTAGE

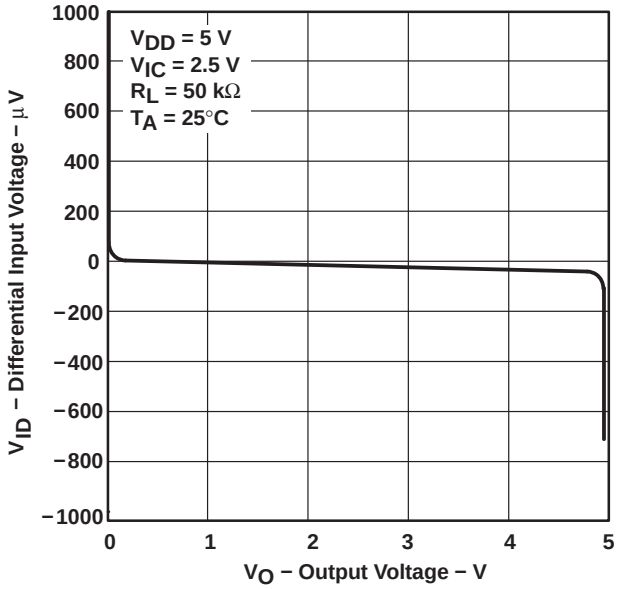


Figure 24

DIFFERENTIAL VOLTAGE AMPLIFICATION‡ vs LOAD RESISTANCE

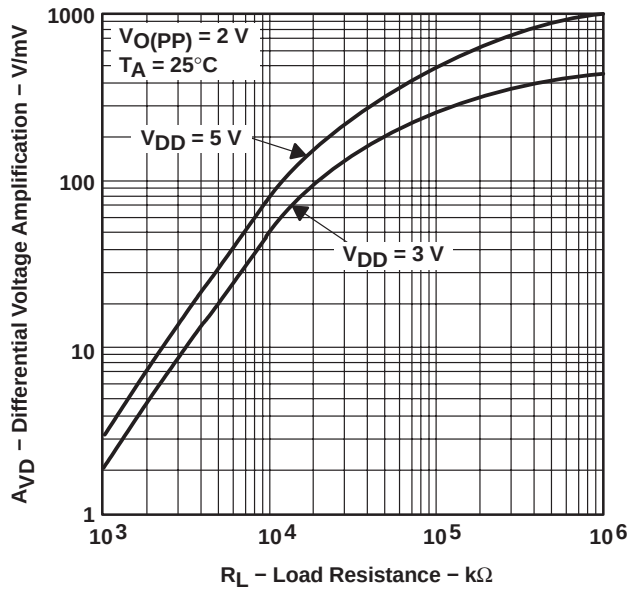


Figure 25

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN† vs FREQUENCY

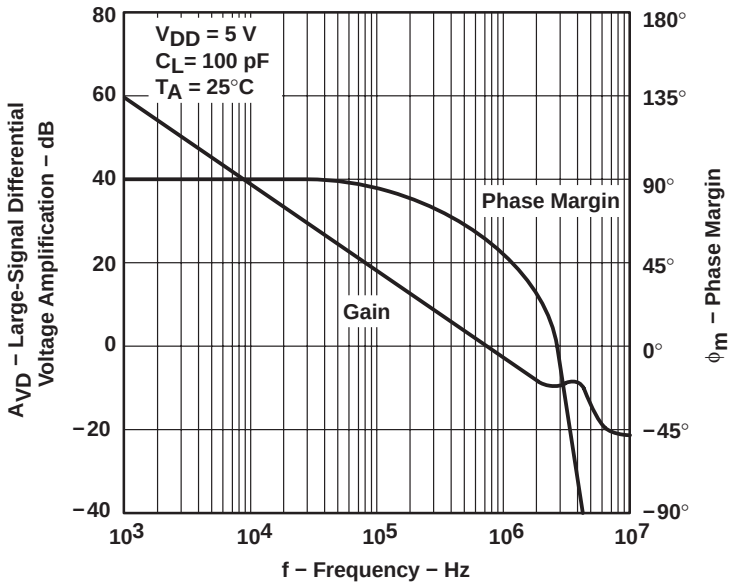


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE MARGIN† vs FREQUENCY

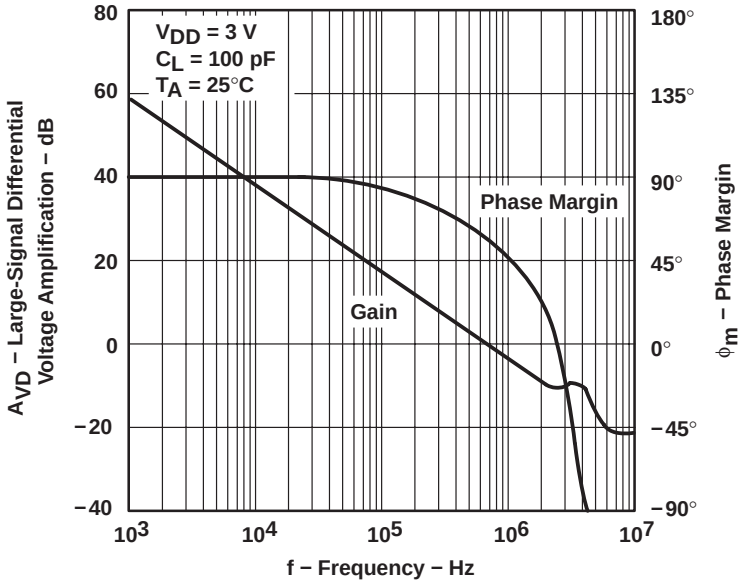


Figure 27

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡ vs FREE-AIR TEMPERATURE

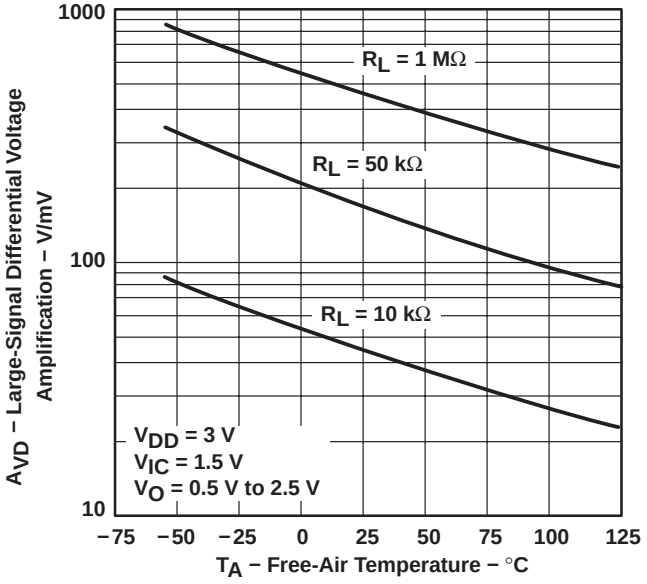


Figure 28

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION†‡ vs FREE-AIR TEMPERATURE

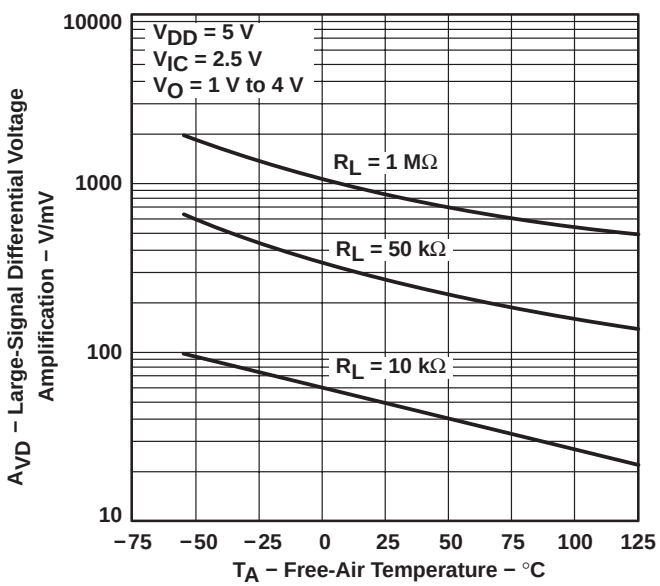


Figure 29

OUTPUT IMPEDANCE‡ vs FREQUENCY

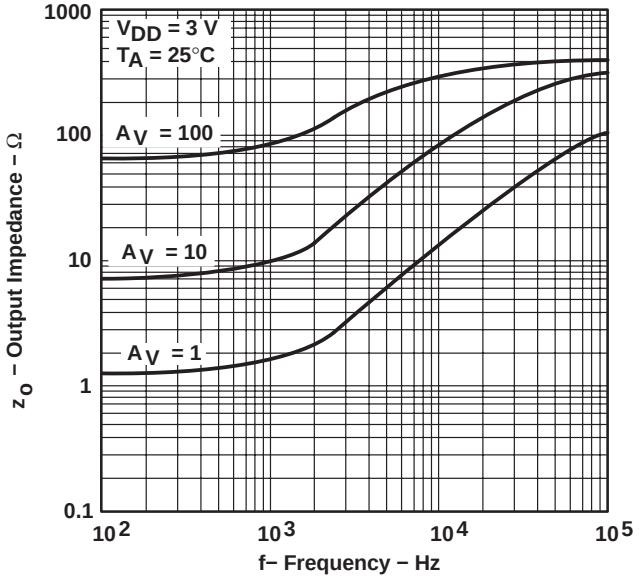


Figure 30

OUTPUT IMPEDANCE‡ vs FREQUENCY

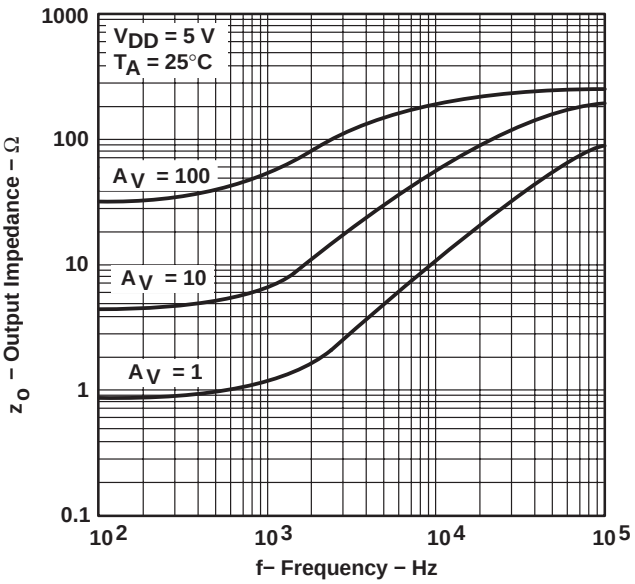


Figure 31

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

COMMON-MODE REJECTION RATIO† vs FREQUENCY

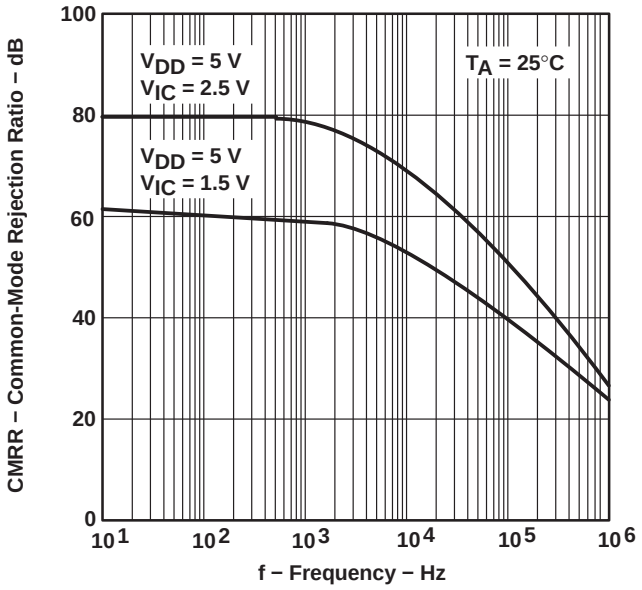


Figure 32

COMMON-MODE REJECTION RATIO†‡ vs FREE-AIR TEMPERATURE

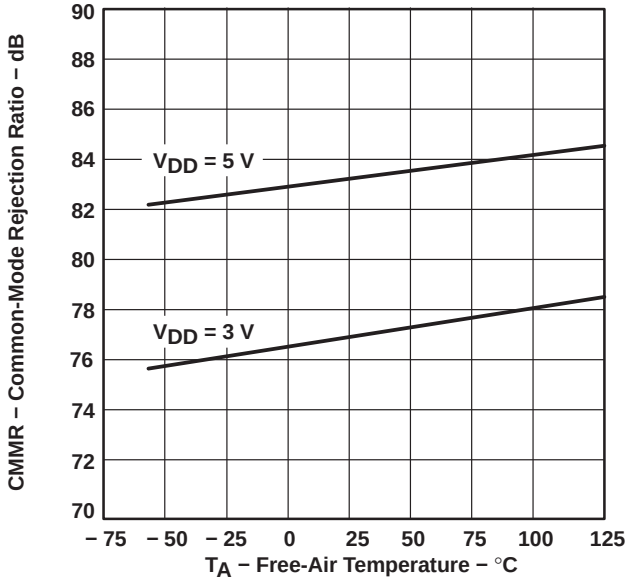


Figure 33

SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY

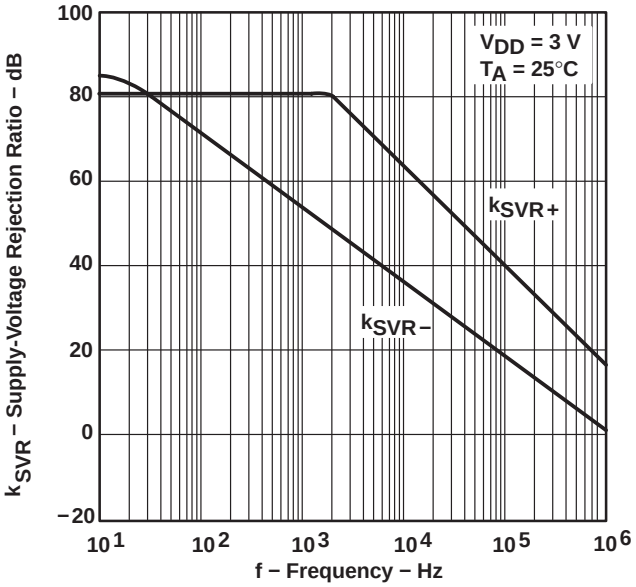


Figure 34

SUPPLY-VOLTAGE REJECTION RATIO† vs FREQUENCY

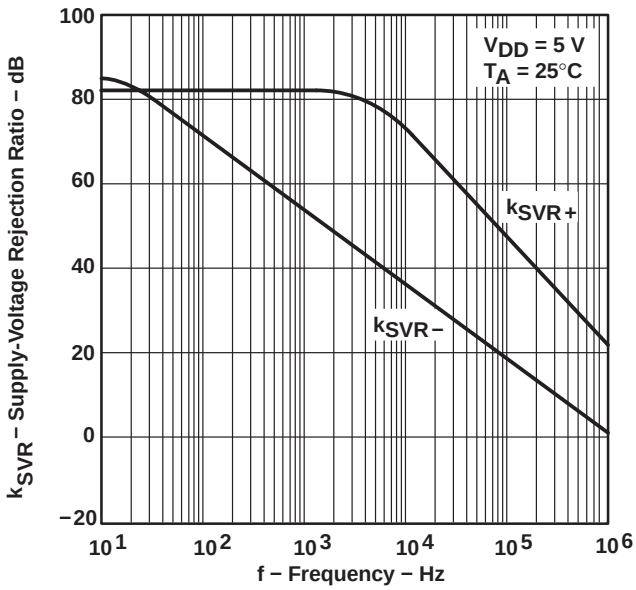


Figure 35

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

TLV2262
SUPPLY-VOLTAGE REJECTION RATIO† vs FREE-AIR TEMPERATURE

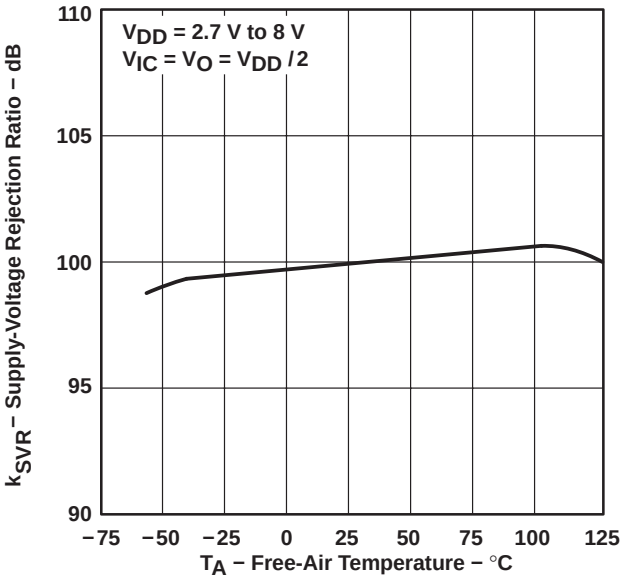


Figure 36

TLV2264
SUPPLY-VOLTAGE REJECTION RATIO† vs FREE-AIR TEMPERATURE

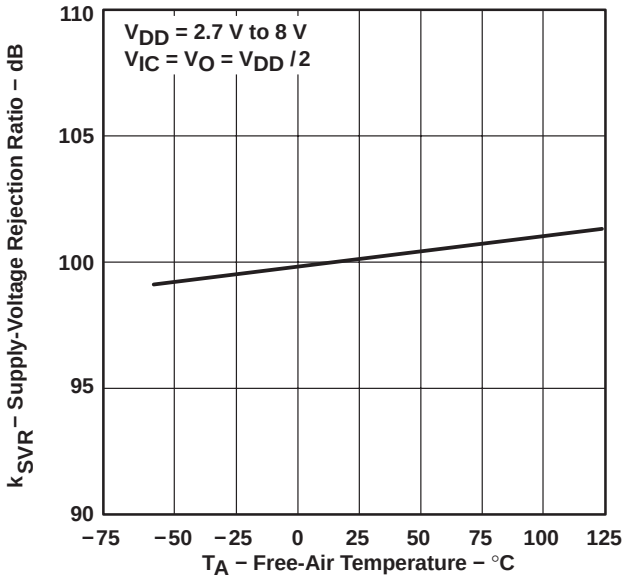


Figure 37

TLV2262
SUPPLY CURRENT†‡ vs FREE-AIR TEMPERATURE

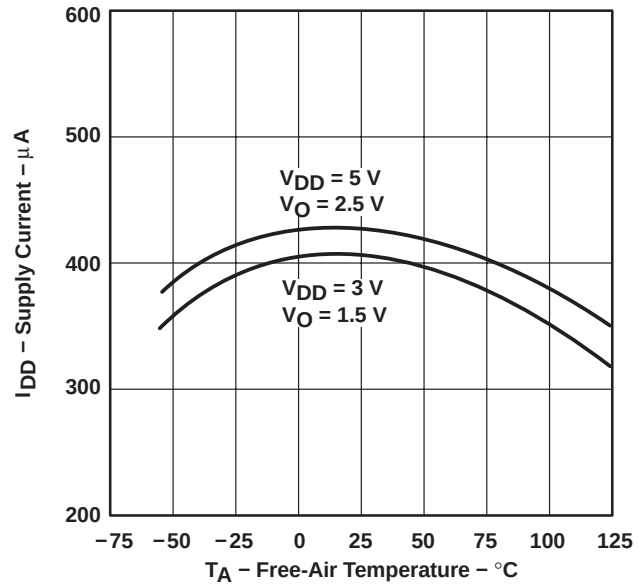


Figure 38

TLV2264
SUPPLY CURRENT†‡ vs FREE-AIR TEMPERATURE

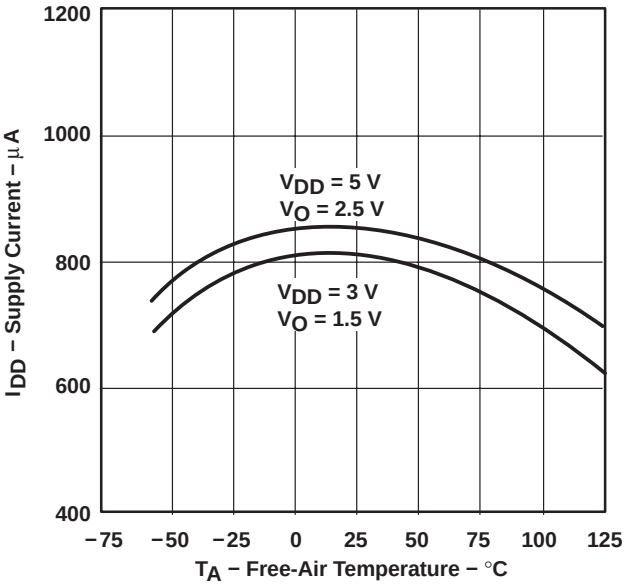


Figure 39

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.
‡ For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

SLEW RATE† vs LOAD CAPACITANCE

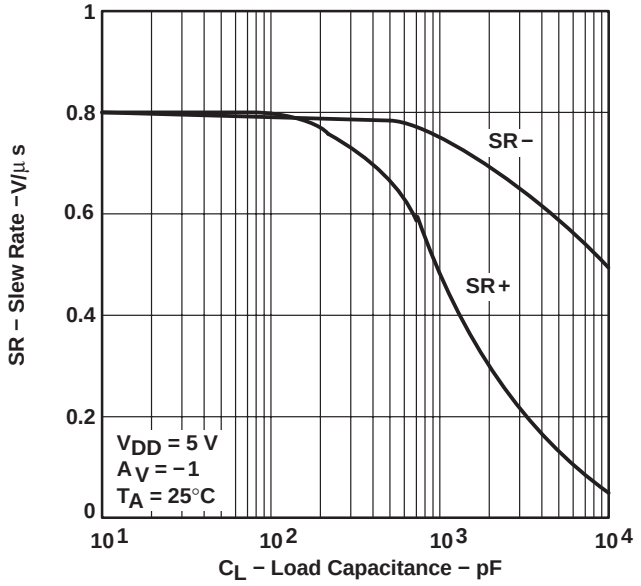


Figure 40

SLEW RATE†‡ vs FREE-AIR TEMPERATURE

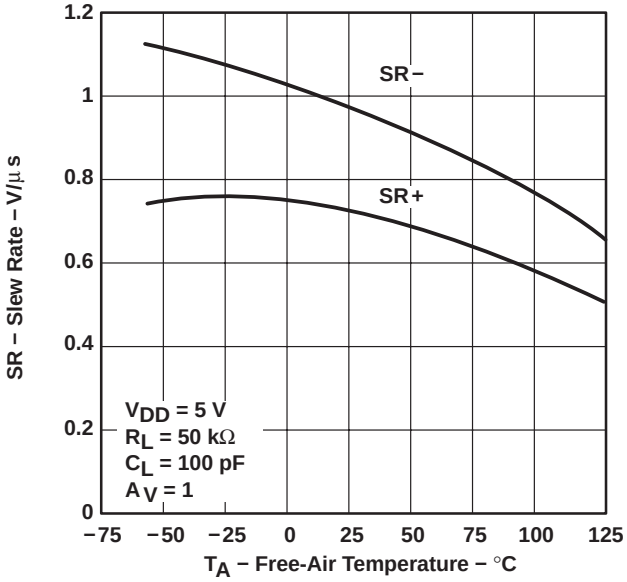


Figure 41

INVERTING LARGE-SIGNAL PULSE RESPONSE†

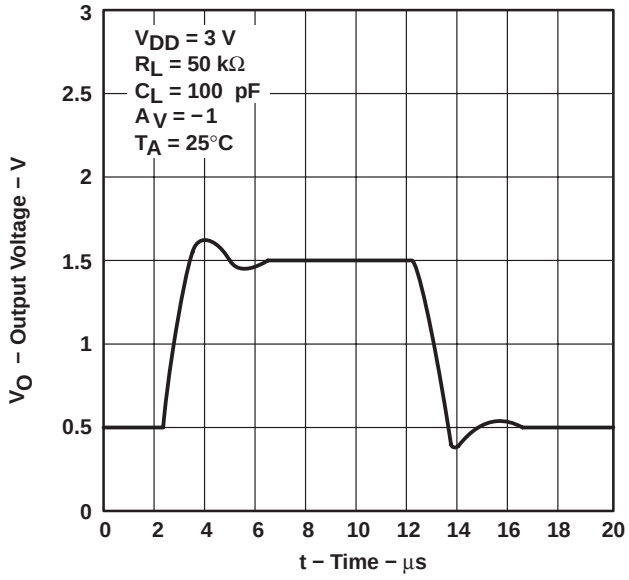


Figure 42

INVERTING LARGE-SIGNAL PULSE RESPONSE†

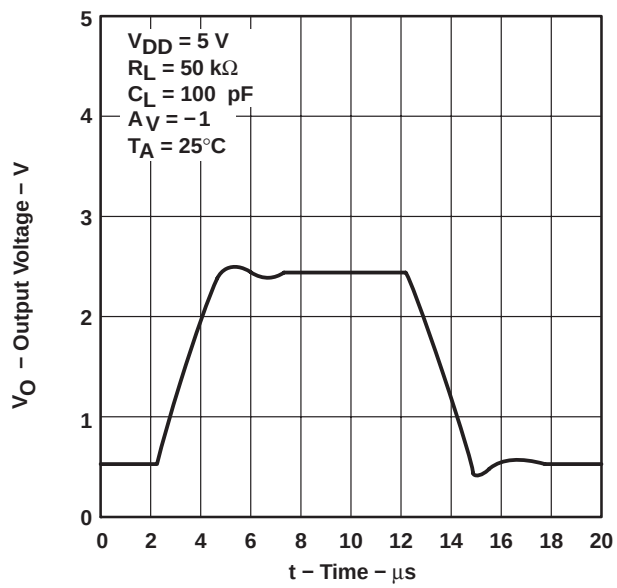


Figure 43

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE†

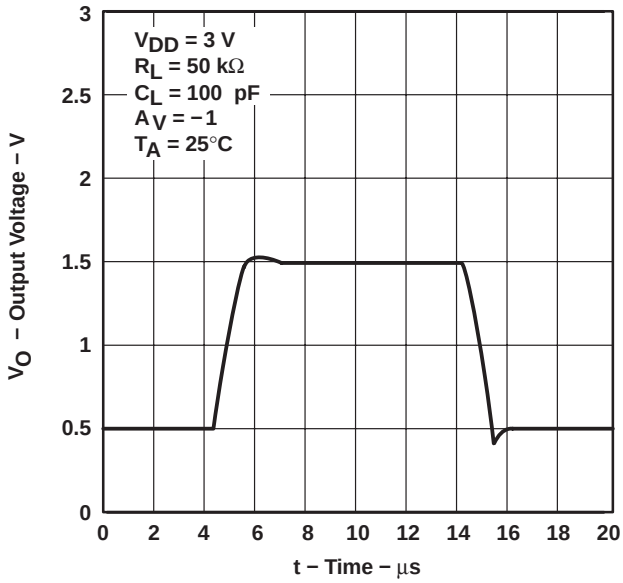


Figure 44

VOLTAGE-FOLLOWER LARGE-SIGNAL
PULSE RESPONSE†

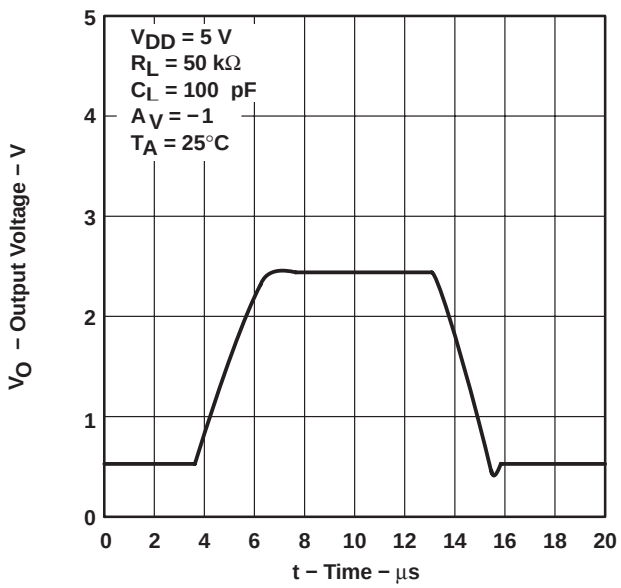


Figure 45

INVERTING SMALL-SIGNAL
PULSE RESPONSE†

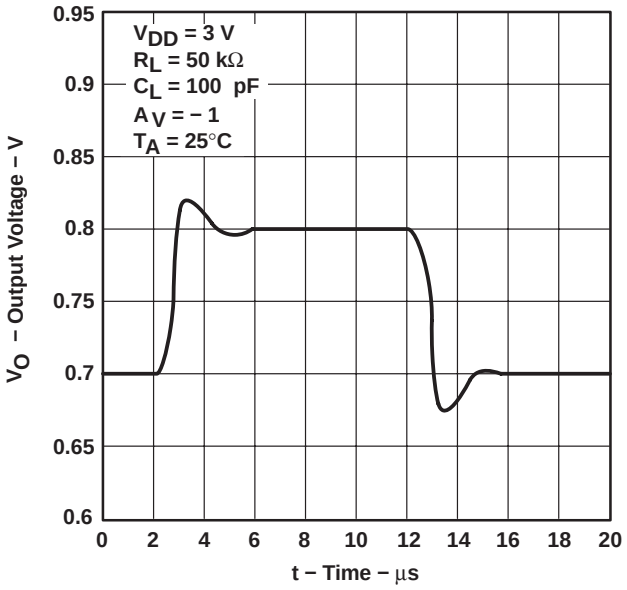


Figure 46

INVERTING SMALL-SIGNAL
PULSE RESPONSE†

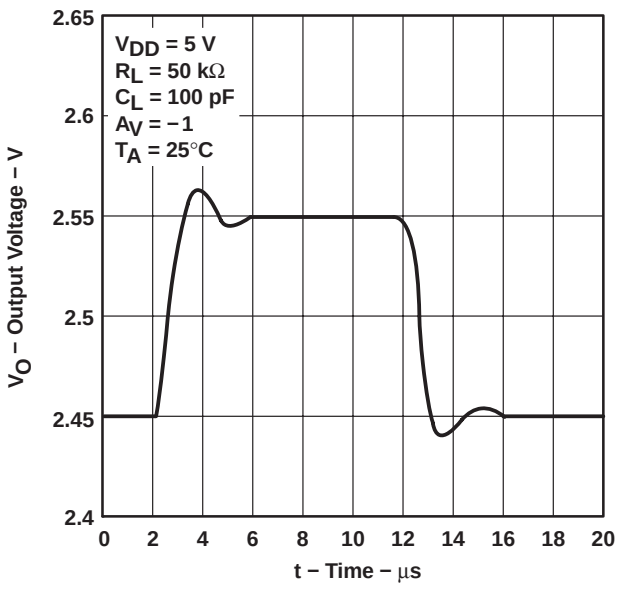


Figure 47

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE†

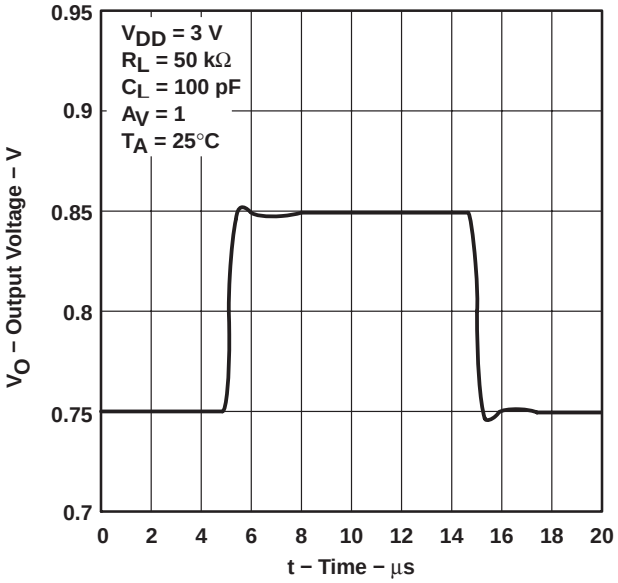


Figure 48

VOLTAGE-FOLLOWER SMALL-SIGNAL
PULSE RESPONSE†

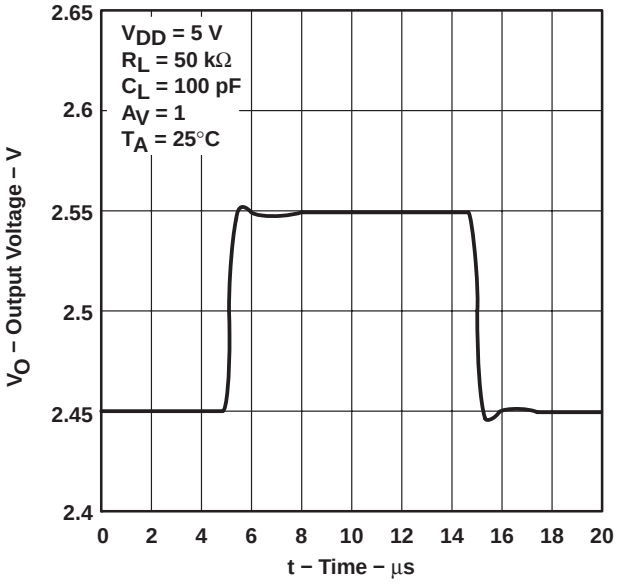


Figure 49

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

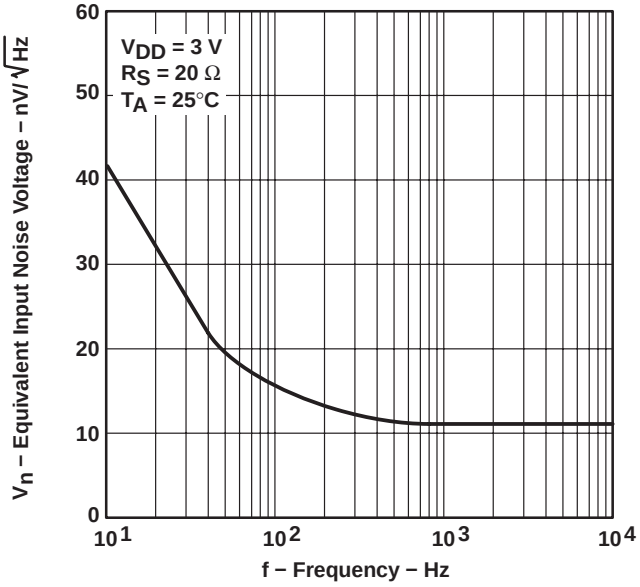


Figure 50

EQUIVALENT INPUT NOISE VOLTAGE†
vs
FREQUENCY

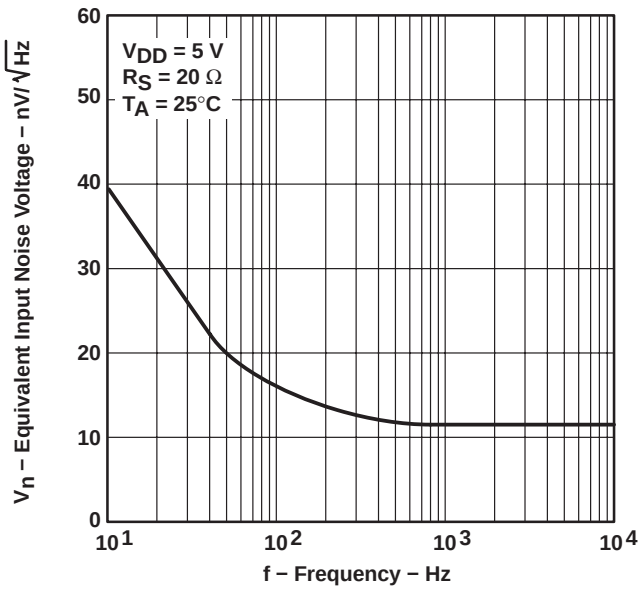


Figure 51

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

INPUT NOISE VOLTAGE OVER A 10-SECOND PERIOD†

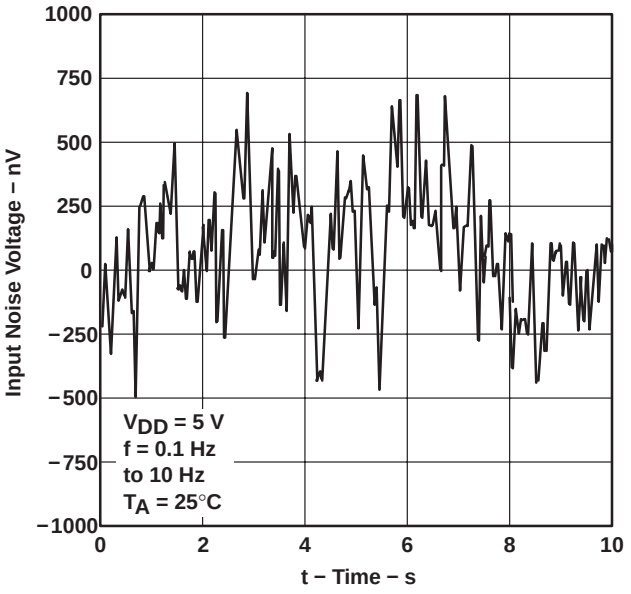


Figure 52

INTEGRATED NOISE VOLTAGE vs FREQUENCY

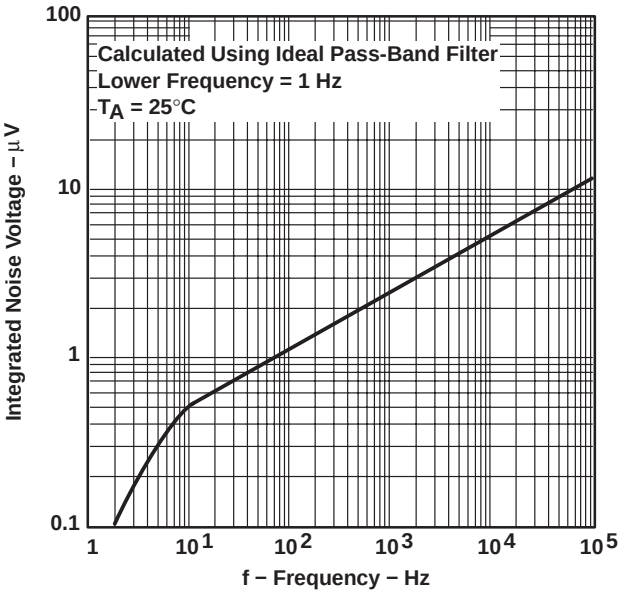


Figure 53

TOTAL HARMONIC DISTORTION PLUS NOISE† vs FREQUENCY

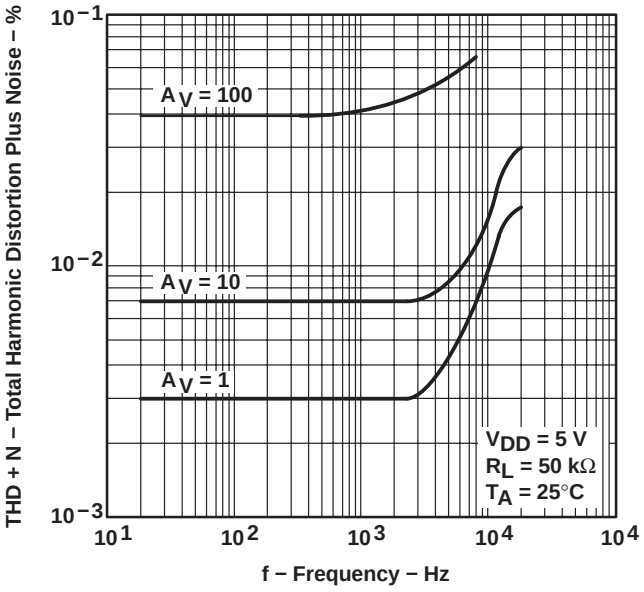


Figure 54

GAIN-BANDWIDTH PRODUCT vs SUPPLY VOLTAGE

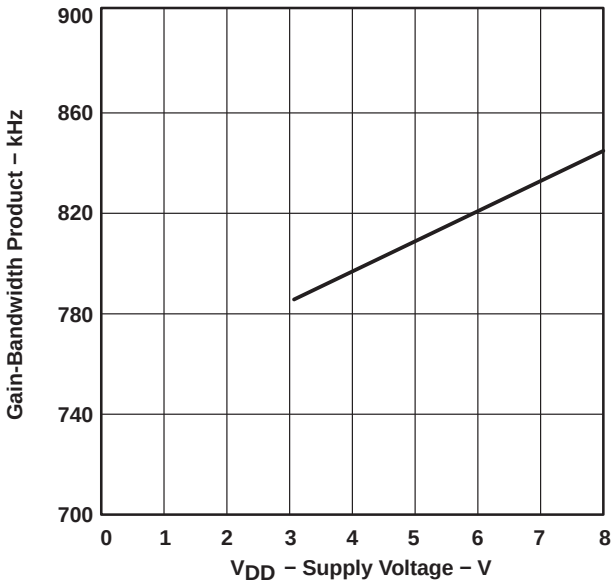


Figure 55

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT† ‡ vs FREE-AIR TEMPERATURE

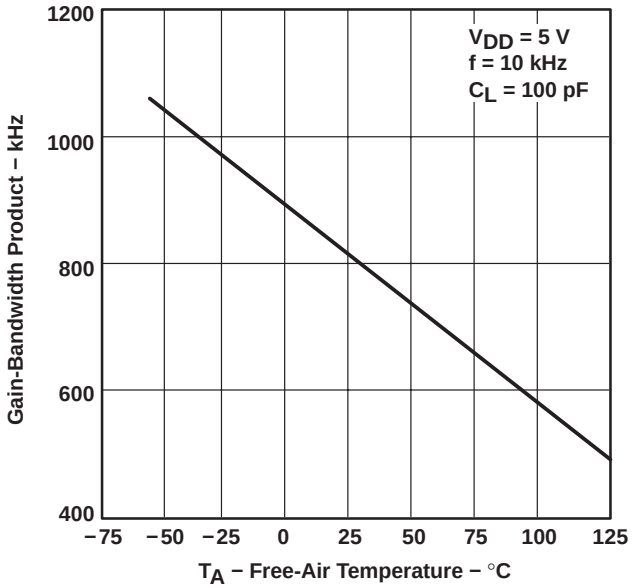


Figure 56

PHASE MARGIN vs LOAD CAPACITANCE

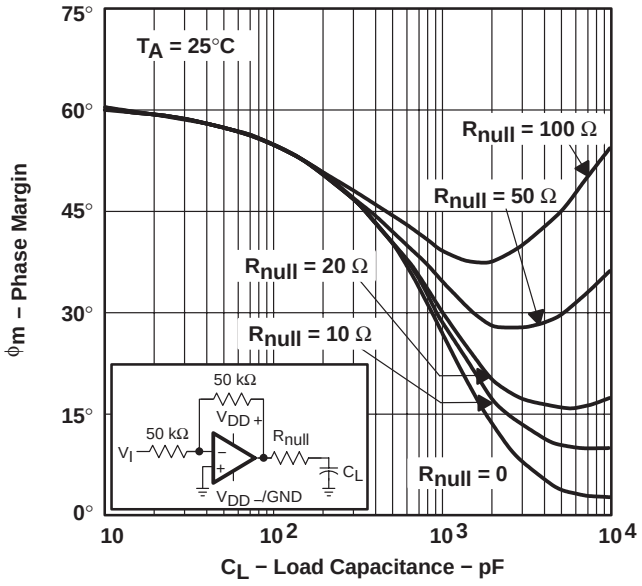


Figure 57

GAIN MARGIN vs LOAD CAPACITANCE

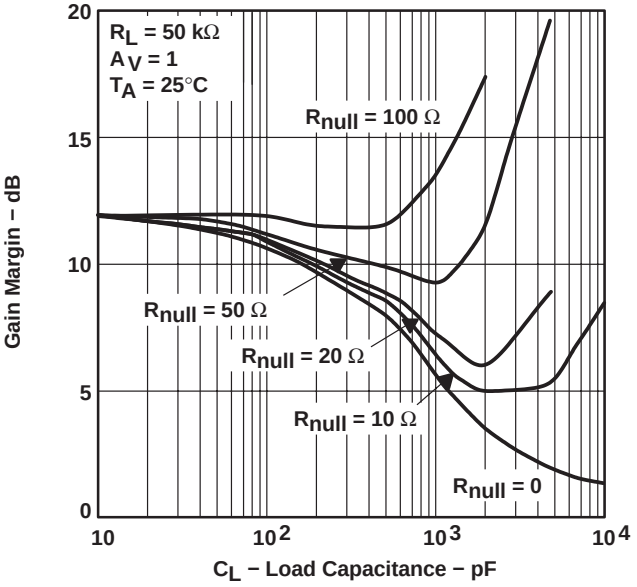


Figure 58

UNITY-GAIN BANDWIDTH vs LOAD CAPACITANCE

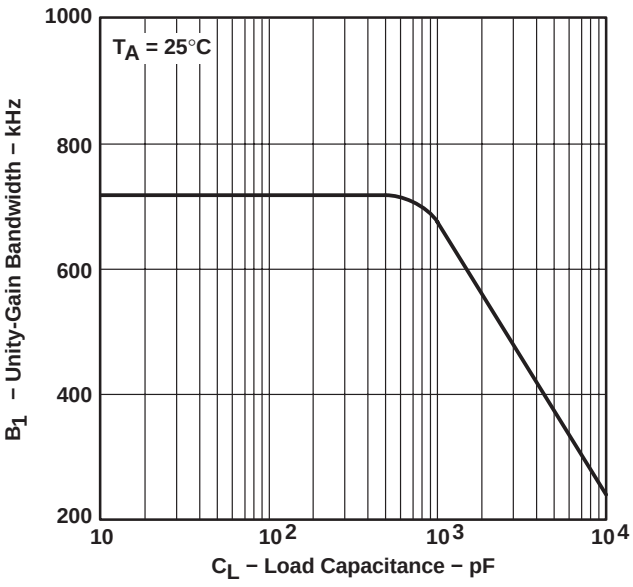
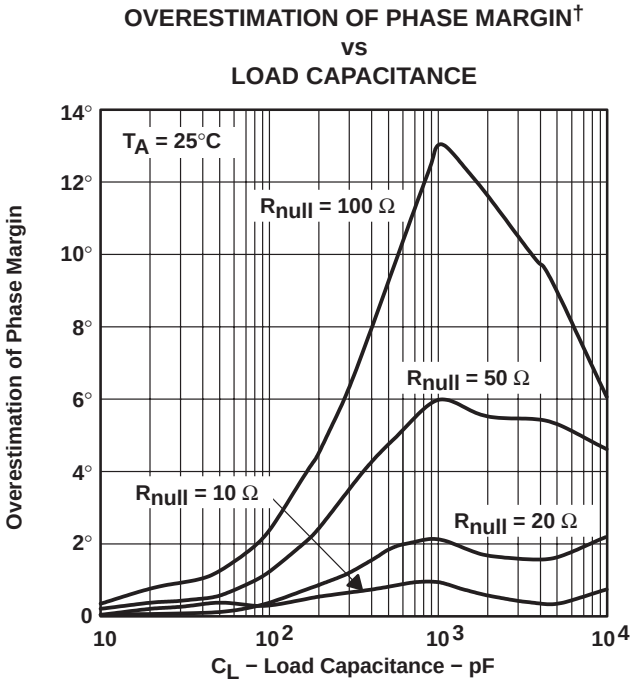


Figure 59

† For all curves where V_{DD} = 5 V, all loads are referenced to 2.5 V. For all curves where V_{DD} = 3 V, all loads are referenced to 1.5 V.
‡ Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS



† See application information

Figure 60

APPLICATION INFORMATION

driving large capacitive loads

The TLV226x is designed to drive larger capacitive loads than most CMOS operational amplifiers. Figure 51 and Figure 52 illustrate its ability to drive loads greater than 400 pF while maintaining good gain and phase margins (R_{null} = 0).

A smaller series resistor (R_{null}) at the output of the device (see Figure 61) improves the gain and phase margins when driving large capacitive loads. Figure 51 and Figure 52 show the effects of adding series resistances of 10 Ω, 20 Ω, 50 Ω, and 100 Ω. The addition of this series resistor has two effects: the first is that it adds a zero to the transfer function and the second is that it reduces the frequency of the pole associated with the output load in the transfer function.

The zero introduced to the transfer function is equal to the series resistance times the load capacitance. To calculate the improvement in phase margin, equation (1) can be used.

$$\Delta\theta_{m1} = \tan^{-1}\left(2 \times \pi \times \text{UGBW} \times R_{null} \times C_L\right) \quad (1)$$

Where :

$\Delta\theta_{m1}$ = improvement in phase margin
UGBW = unity-gain bandwidth frequency
R_{null} = output series resistance
C_L = load capacitance

The unity-gain bandwidth (UGBW) frequency decreases as the capacitive load increases (see Figure 53). To use equation 1, UGBW must be approximated from Figure 53.

Using equation 1 alone overestimates the improvement in phase margin as illustrated in Figure 59. The overestimation is caused by the decrease in the frequency of the pole associated with the load, providing additional phase shift and reducing the overall improvement in phase margin. The pole associated with the load is reduced by the factor calculated in equation 2.

$$F = \frac{1}{1 + g_m \times R_{null}} \quad (2)$$

Where :

F = factor reducing frequency of pole
g_m = small-signal output transconductance (typically 4.83×10^{-3} mhos)
R_{null} = output series resistance

For the TLV226x, the pole associated with the load is typically 7 MHz with 100-pF load capacitance. This value varies inversely with C_L: at C_L = 10 pF, use 70 MHz, at C_L = 1000 pF, use 700 kHz, and so on.

Reducing the pole associated with the load introduces phase shift, thereby reducing phase margin. This results in an error in the increase in phase margin expected by considering the zero alone (equation 1). Equation 3 approximates the reduction in phase margin due to the movement of the pole associated with the load. The result of this equation can be subtracted from the result of the equation 1 to better approximate the improvement in phase margin.

APPLICATION INFORMATION

driving large capacitive loads (continued)

$$\Delta\theta_{m2} = \tan^{-1}\left[\frac{UGBW}{(F \times P_2)}\right] - \tan^{-1}\left(\frac{UGBW}{P_2}\right) \quad (3)$$

Where :

$\Delta\theta_{m2}$ = reduction in phase margin
UGBW = unity-gain bandwidth frequency
F = factor from equation (2)
P_2 = unadjusted pole (70 MHz @ 10 pF, 7 MHz @ 100 pF, etc.)

Using these equations with Figure 60 and Figure 61 enables the designer to choose the appropriate output series resistance to optimize the design of circuits driving large capacitive loads.

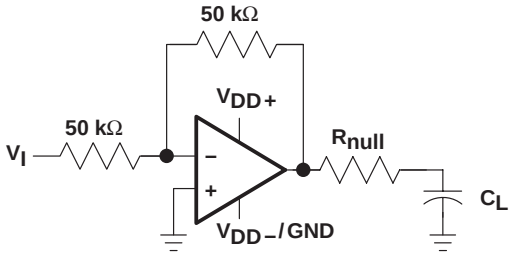


Figure 61. Series-Resistance Circuit

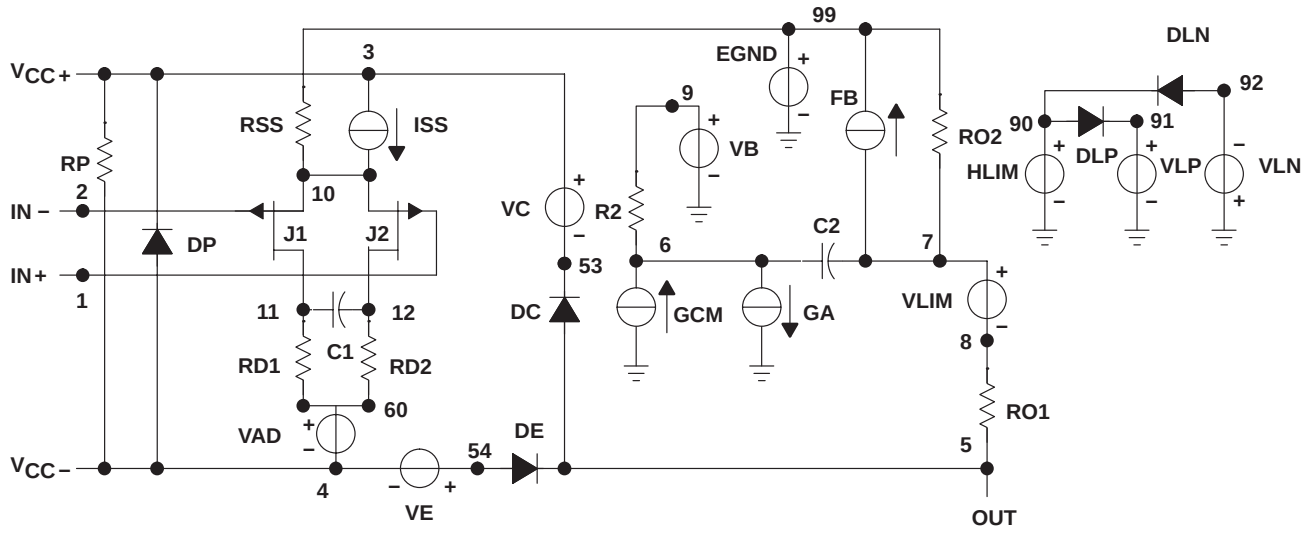
APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 5) and subcircuit in Figure 62 are generated using the TLV226x typical electrical and operating characteristics at T_A = 25°C. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity-gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 5: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, “Macromodeling of Intergrated Circuit Operational Amplifiers,” *IEEE Journal of Solid-State Circuits,* SC-9, 353 (1974).




```
.SUBCKT TLV226x 1 2 3 4 5
C1      11      12      5.5E−12
C2      6       7       20.00E−12
DC      5       53      DX
DE      54      5       DX
DLP     90      91      DX
DLN     92      90      DX
DP      4       3       DX
EGND    99      0       POLY (2) (3,0) (4,0) 0 .5 .5
FB      7       99      POLY (5) VB VC VE VLP
+ VLN 0 8.84E6 −10E6 10E6 10E6 −10E6
GA      6       0       11      12 62.83E−6
GCM     0       6       10      99 12.34E−9
ISS     3       10      DC 11.05E−6
HLIM    90      0       VLIM 1K
J1      11      2       10 JX
J2      12      1       10 JX
R2      6       9       100.0E3
RD1     60      11      15.92E3
RD2     60      12      15.92E3
R01     8       5       135
R02     7       99      135
RP      3       4       15.87E3
RSS     10      99      18.18E6
VAD     60      4       −.5
VB      9       0       DC 0
VC      3       53      DC .615
VE      54      4       DC .615
VLIM    7       8       DC 0
VLP     91      0       DC 1
VLN     0       92      DC 5.1
.MODEL DX D (IS=800.0E−18)
.MODEL JX PJF (IS=500.0E−15 BETA=325E−6
+ VTO=−.08)
.ENDS
```

Figure 62. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9550401QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9550401QPA TLV2262M
5962-9550403QHA	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9550403QHA TLV2262AM
5962-9550403QPA	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9550403QPA TLV2262AM
5962-9550404QCA	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9550404QCA TLV2264AMJB
5962-9550404QDA	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9550404QDA TLV2264AMWB
TLV2262AID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262A
TLV2262AID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262A
TLV2262AIDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262A
TLV2262AIDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262A
TLV2262AIP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2262AI
TLV2262AIP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2262AI
TLV2262AIPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 125	TY262A
TLV2262AIPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY262A
TLV2262AIPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY262A
TLV2262AMJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9550403QPA TLV2262AM
TLV2262AMJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9550403QPA TLV2262AM
TLV2262AMUB	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9550403QHA TLV2262AM
TLV2262AMUB.A	Active	Production	CFP (U) | 10	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9550403QHA TLV2262AM
TLV2262ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262I
TLV2262ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262I
TLV2262IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262I

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2262IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2262I
TLV2262IDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV2262IP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2262IP
TLV2262IP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2262IP
TLV2262IPW	Obsolete	Production	TSSOP (PW) | 8	-	-	Call TI	Call TI	-40 to 125	TY2262
TLV2262IPWR	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2262
TLV2262IPWR.A	Active	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TY2262
TLV2262MJGB	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9550401QPA TLV2262M
TLV2262MJGB.A	Active	Production	CDIP (JG) | 8	50 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	9550401QPA TLV2262M
TLV2264AID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2264AI
TLV2264AID.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2264AI
TLV2264AIDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2264AI
TLV2264AIDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	V2264AI
TLV2264AIDRG4	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	-	Call TI	Call TI	-40 to 125	
TLV2264AIN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2264AIN
TLV2264AIN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2264AIN
TLV2264AIPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264AI
TLV2264AIPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264AI
TLV2264AMJB	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9550404QCA TLV2264AMJB
TLV2264AMJB.A	Active	Production	CDIP (J) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9550404QCA TLV2264AMJB
TLV2264AMWB	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9550404QDA TLV2264AMWB
TLV2264AMWB.A	Active	Production	CFP (W) | 14	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9550404QDA TLV2264AMWB
TLV2264AQD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264A

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TLV2264AQD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264A
TLV2264AQD.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264A
TLV2264ID	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264I
TLV2264ID.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264I
TLV2264IDR	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264I
TLV2264IDR.B	Active	Production	SOIC (D) | 14	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264I
TLV2264IN	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2264IN
TLV2264IN.A	Active	Production	PDIP (N) | 14	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	TLV2264IN
TLV2264IPWR	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264I
TLV2264IPWR.B	Active	Production	TSSOP (PW) | 14	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P2264I
TLV2264QD	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264
TLV2264QD.A	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264
TLV2264QD.B	Active	Production	SOIC (D) | 14	50 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TLV2264

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TLV2262, TLV2262A, TLV2262AM, TLV2262M, TLV2264A, TLV2264AM :

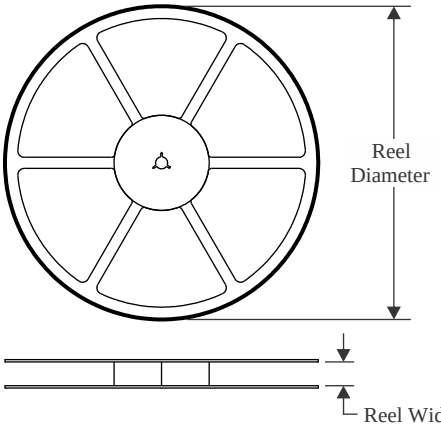
- Catalog : TLV2262A, TLV2262, TLV2264A
- Automotive : TLV2262A-Q1, TLV2262A-Q1, TLV2264A-Q1, TLV2264A-Q1
- Military : TLV2262M, TLV2262AM, TLV2264AM

NOTE: Qualified Version Definitions:

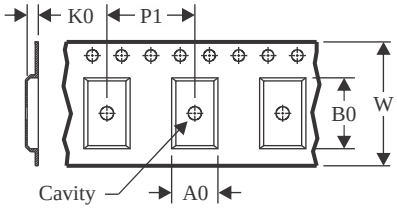
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

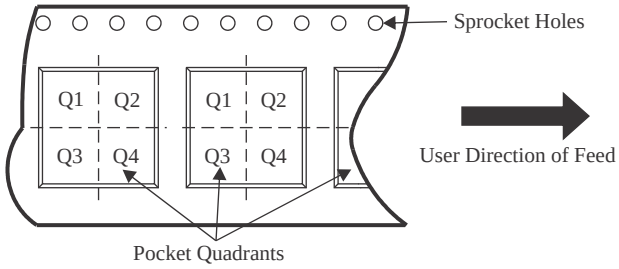


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

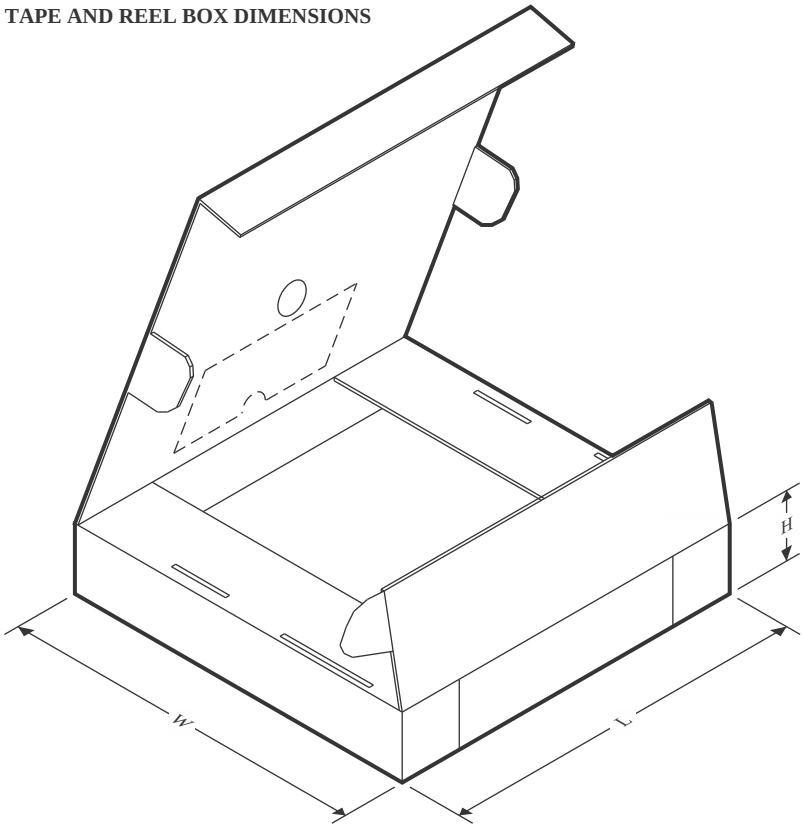
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV2262AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2262AIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2262IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV2262IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV2264AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2264AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV2264IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV2264IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

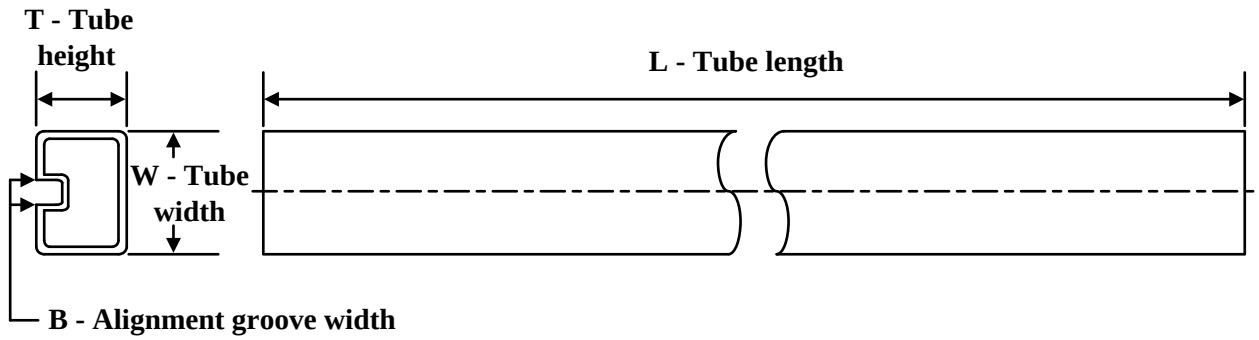
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

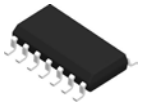
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV2262AIDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2262AIPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV2262IDR	SOIC	D	8	2500	353.0	353.0	32.0
TLV2262IPWR	TSSOP	PW	8	2000	353.0	353.0	32.0
TLV2264AIDR	SOIC	D	14	2500	340.5	336.1	32.0
TLV2264AIPWR	TSSOP	PW	14	2000	353.0	353.0	32.0
TLV2264IDR	SOIC	D	14	2500	353.0	353.0	32.0
TLV2264IPWR	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9550403QHA	U	CFP	10	25	506.98	26.16	6220	NA
5962-9550404QDA	W	CFP	14	25	506.98	26.16	6220	NA
TLV2262AID	D	SOIC	8	75	507	8	3940	4.32
TLV2262AID.A	D	SOIC	8	75	507	8	3940	4.32
TLV2262AIP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2262AIP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLV2262AMUB	U	CFP	10	25	506.98	26.16	6220	NA
TLV2262AMUB.A	U	CFP	10	25	506.98	26.16	6220	NA
TLV2262ID	D	SOIC	8	75	507	8	3940	4.32
TLV2262ID.A	D	SOIC	8	75	507	8	3940	4.32
TLV2262IP	P	PDIP	8	50	506	13.97	11230	4.32
TLV2262IP.A	P	PDIP	8	50	506	13.97	11230	4.32
TLV2264AID	D	SOIC	14	50	507	8	3940	4.32
TLV2264AID.B	D	SOIC	14	50	507	8	3940	4.32
TLV2264AIN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2264AIN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLV2264AMWB	W	CFP	14	25	506.98	26.16	6220	NA
TLV2264AMWB.A	W	CFP	14	25	506.98	26.16	6220	NA
TLV2264AQD	D	SOIC	14	50	507	8	3940	4.32
TLV2264AQD.A	D	SOIC	14	50	507	8	3940	4.32
TLV2264AQD.B	D	SOIC	14	50	507	8	3940	4.32
TLV2264ID	D	SOIC	14	50	507	8	3940	4.32
TLV2264ID.B	D	SOIC	14	50	507	8	3940	4.32
TLV2264IN	N	PDIP	14	25	506	13.97	11230	4.32
TLV2264IN.A	N	PDIP	14	25	506	13.97	11230	4.32
TLV2264QD	D	SOIC	14	50	505.46	6.76	3810	4
TLV2264QD.A	D	SOIC	14	50	505.46	6.76	3810	4
TLV2264QD.B	D	SOIC	14	50	505.46	6.76	3810	4

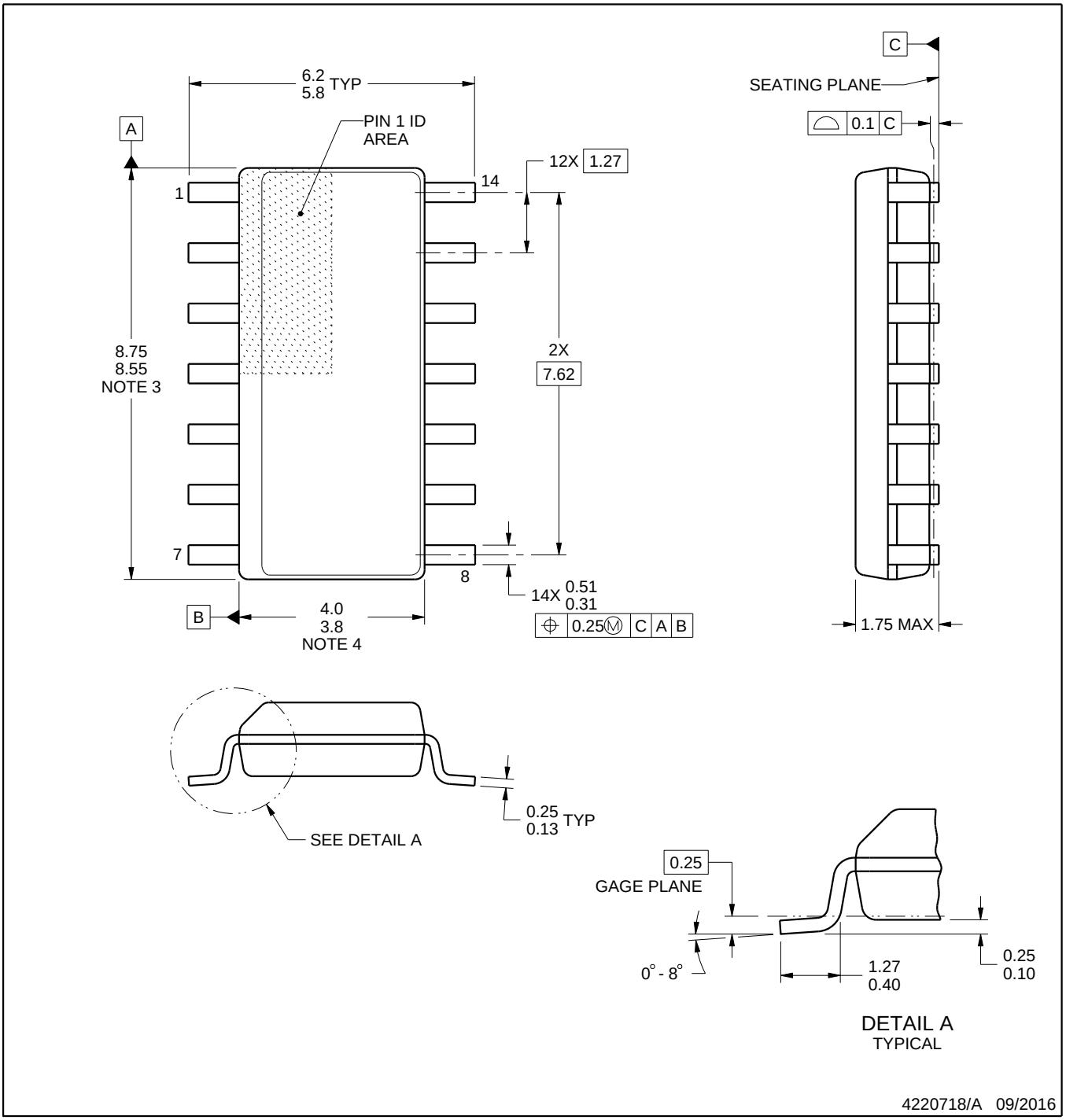


PACKAGE OUTLINE

D0014A

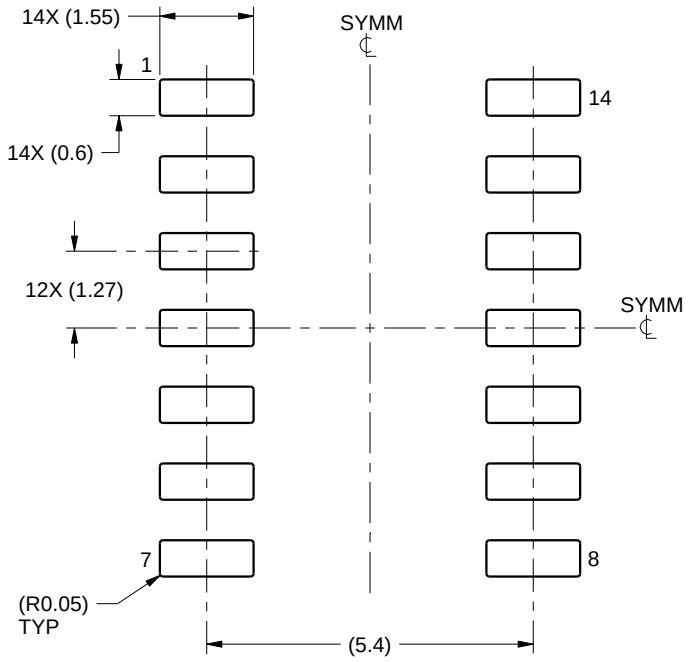
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

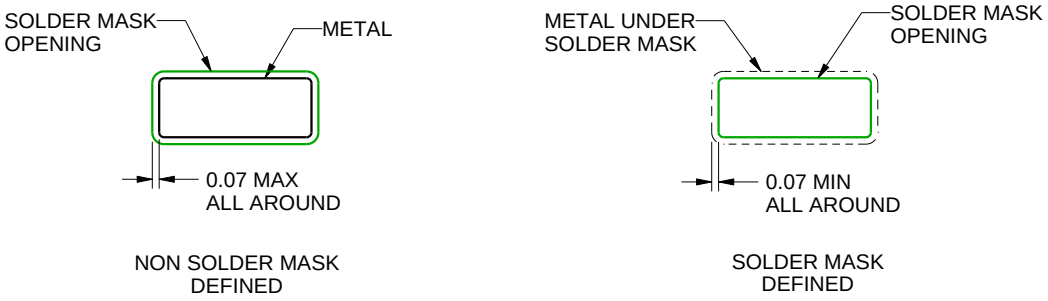


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

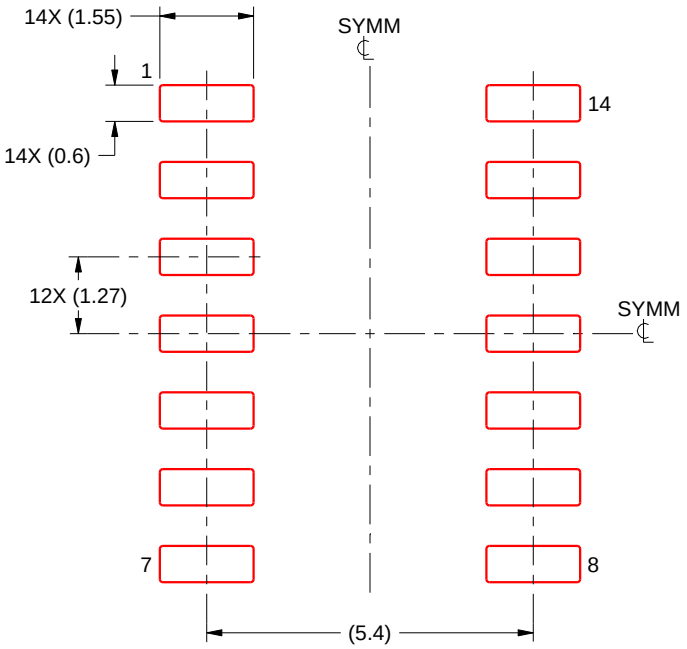
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



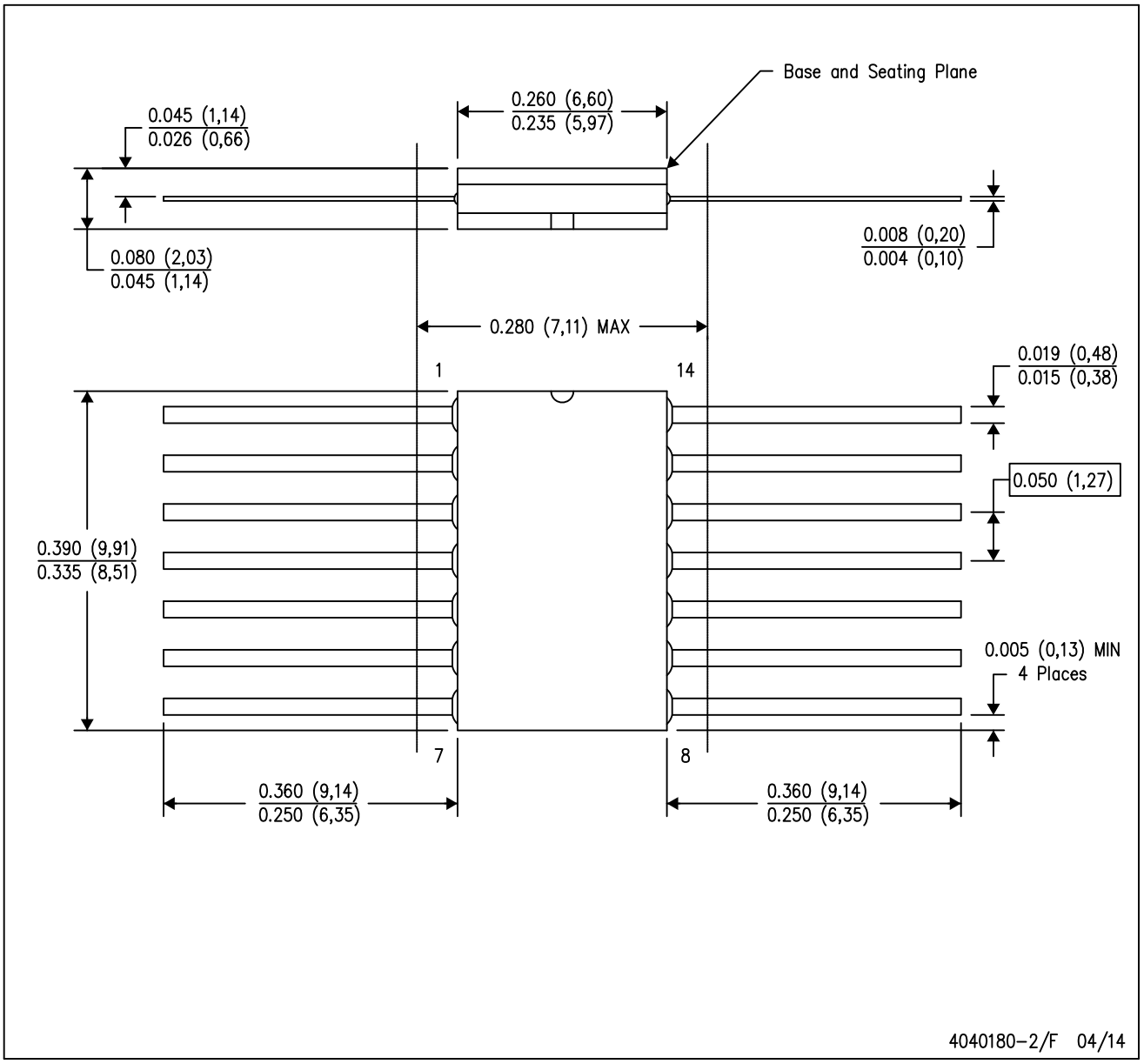
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK

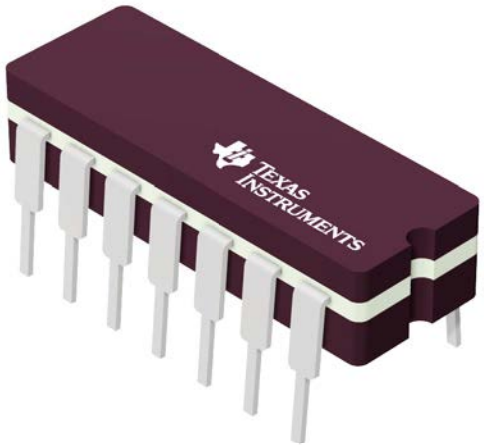


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

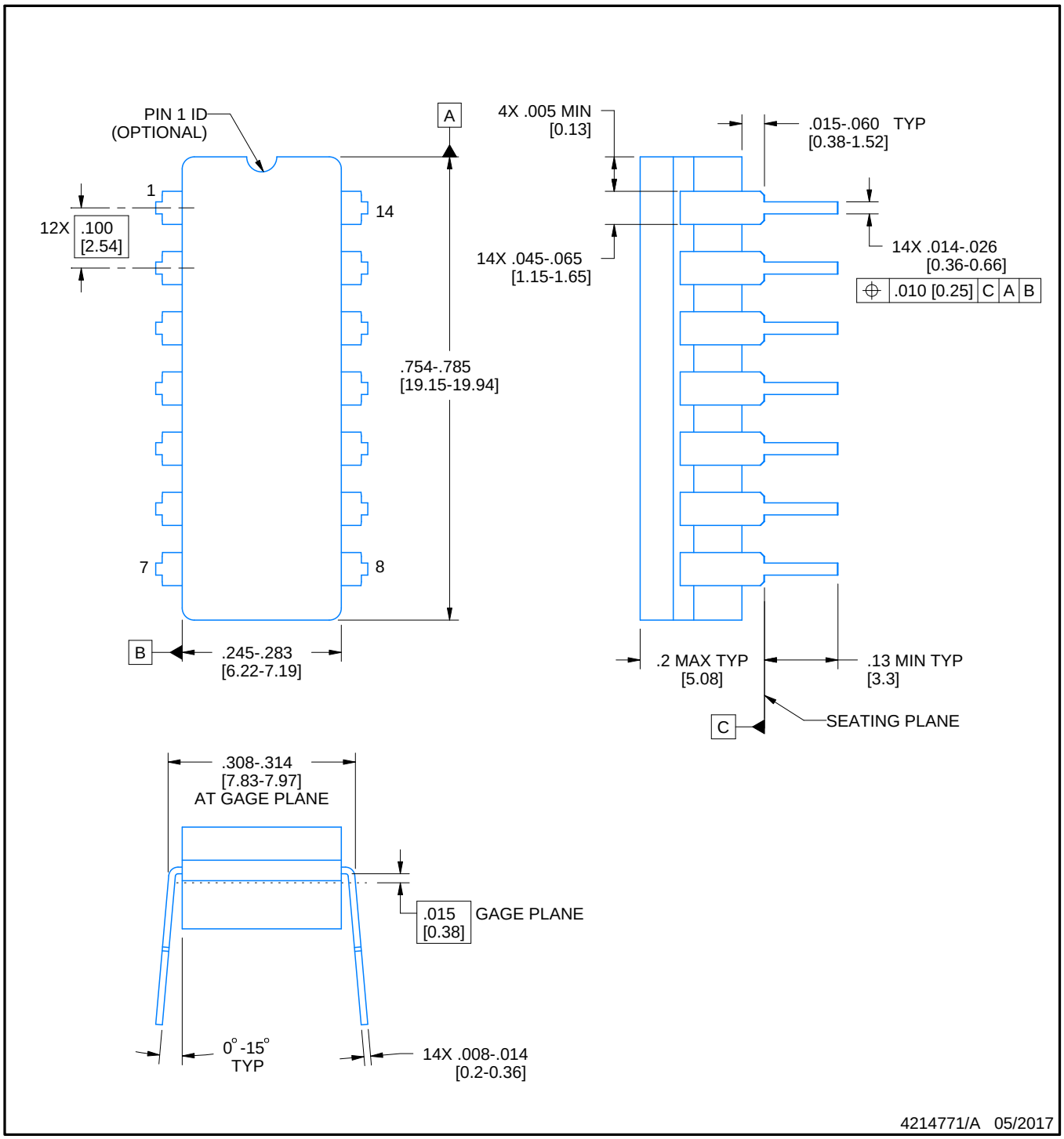
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

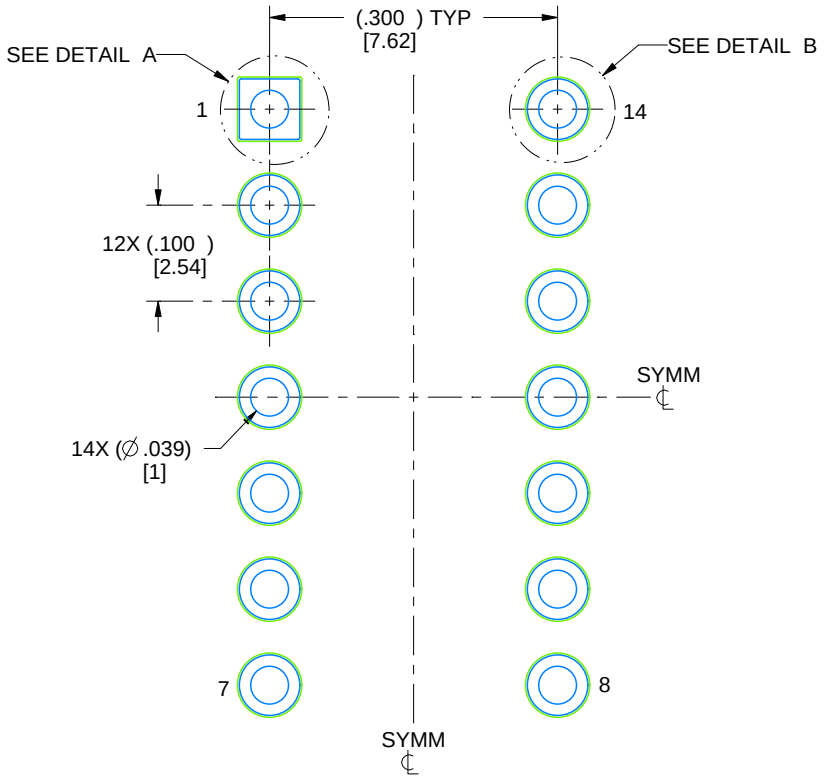
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

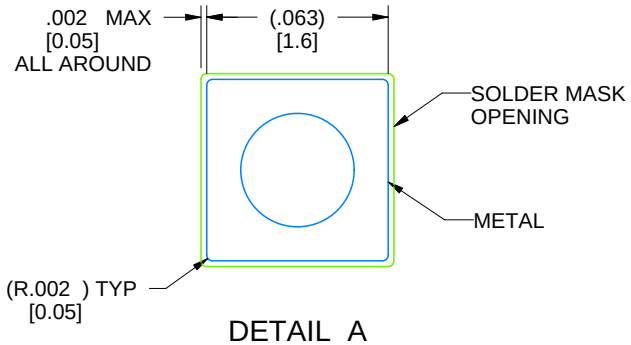
J0014A

CDIP - 5.08 mm max height

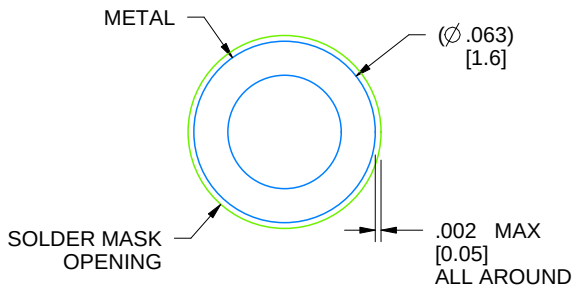
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

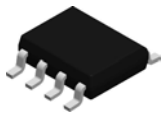


DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

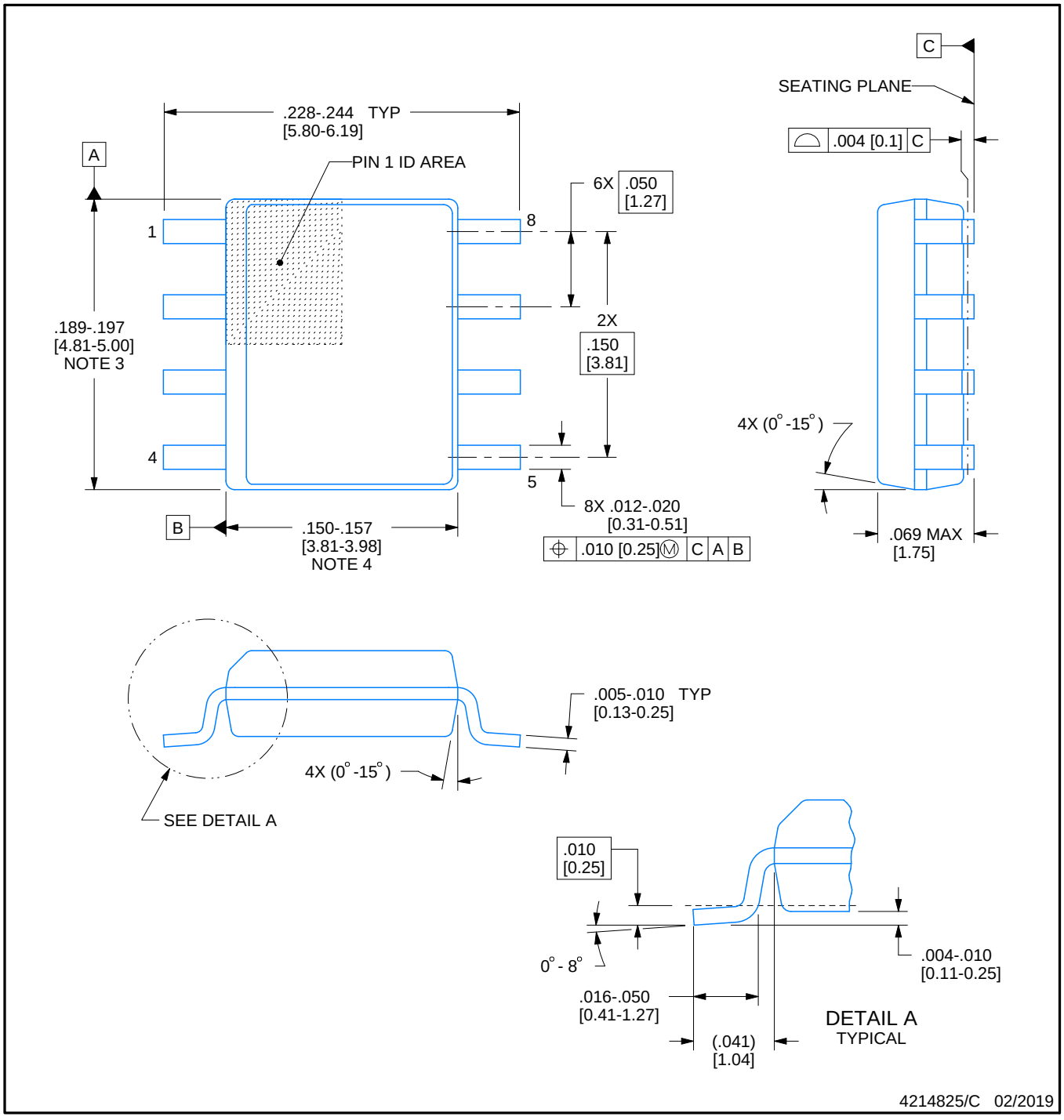


PACKAGE OUTLINE

D0008A

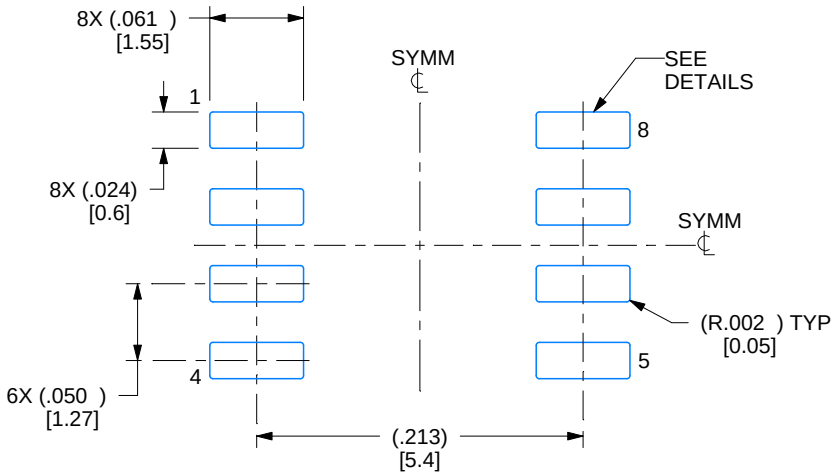
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

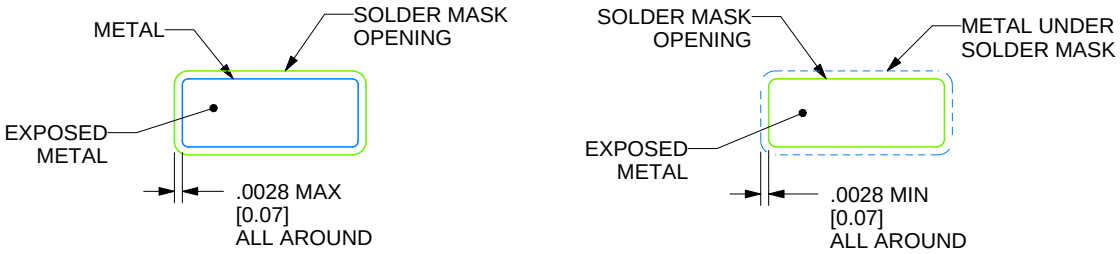


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

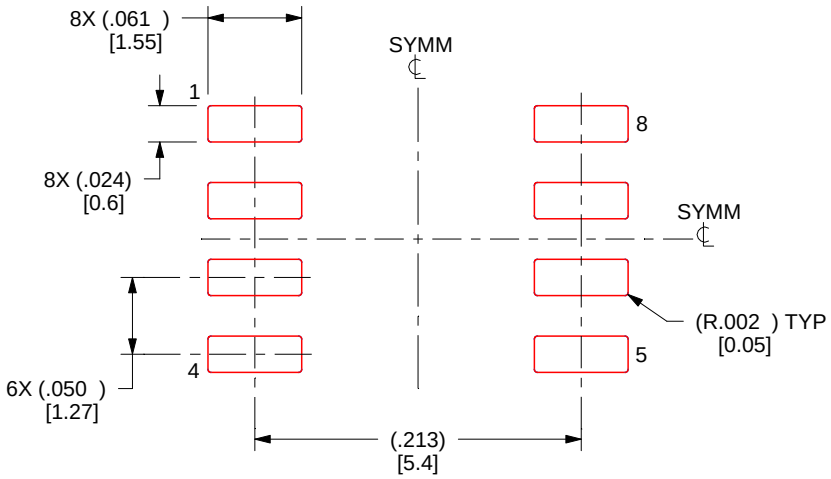
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



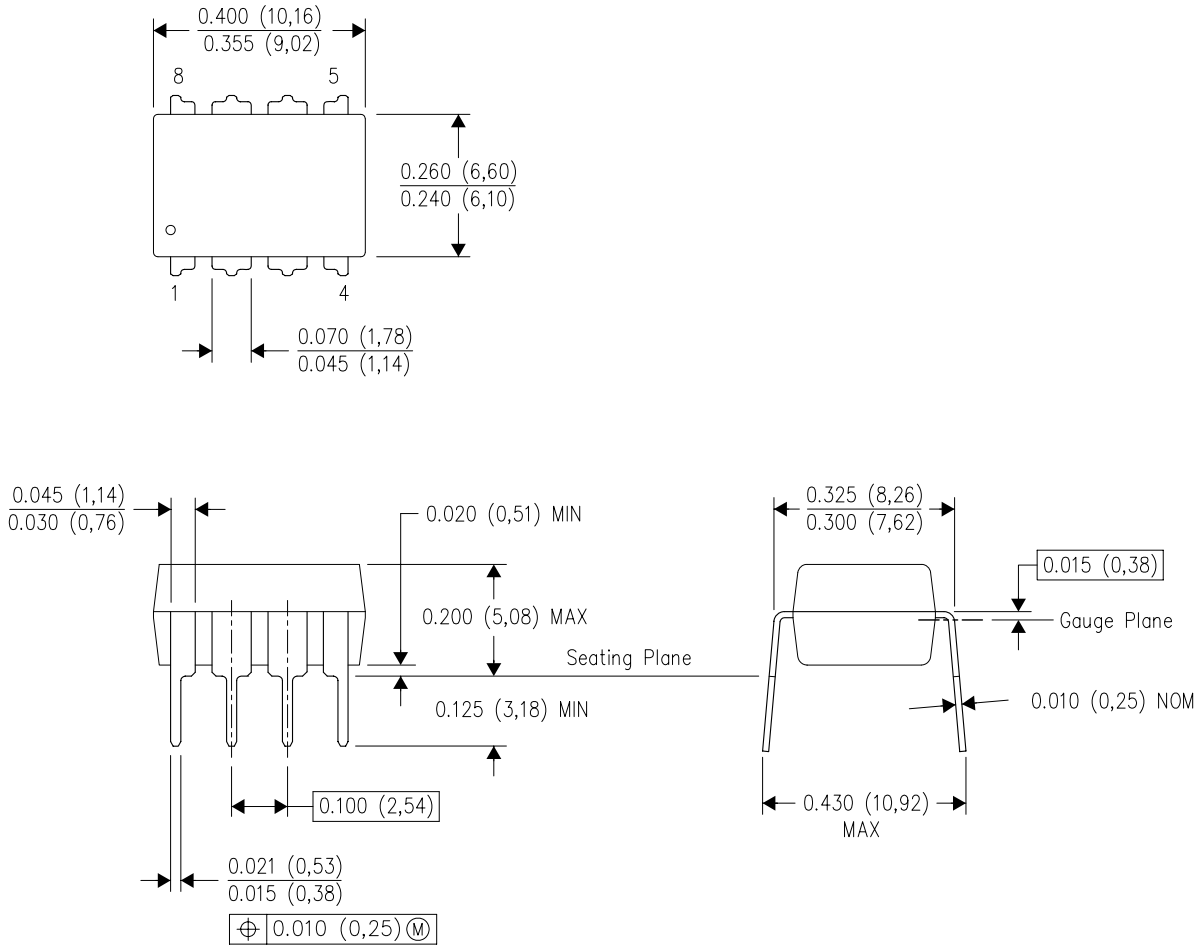
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

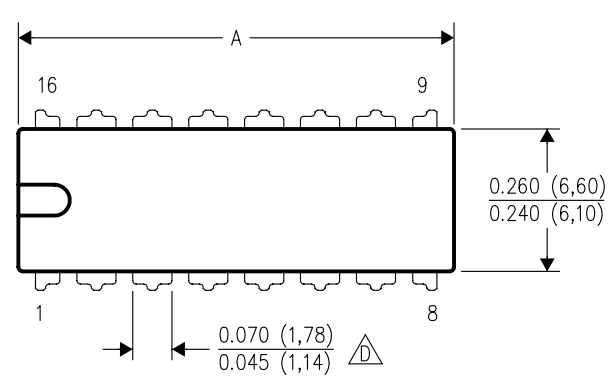


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

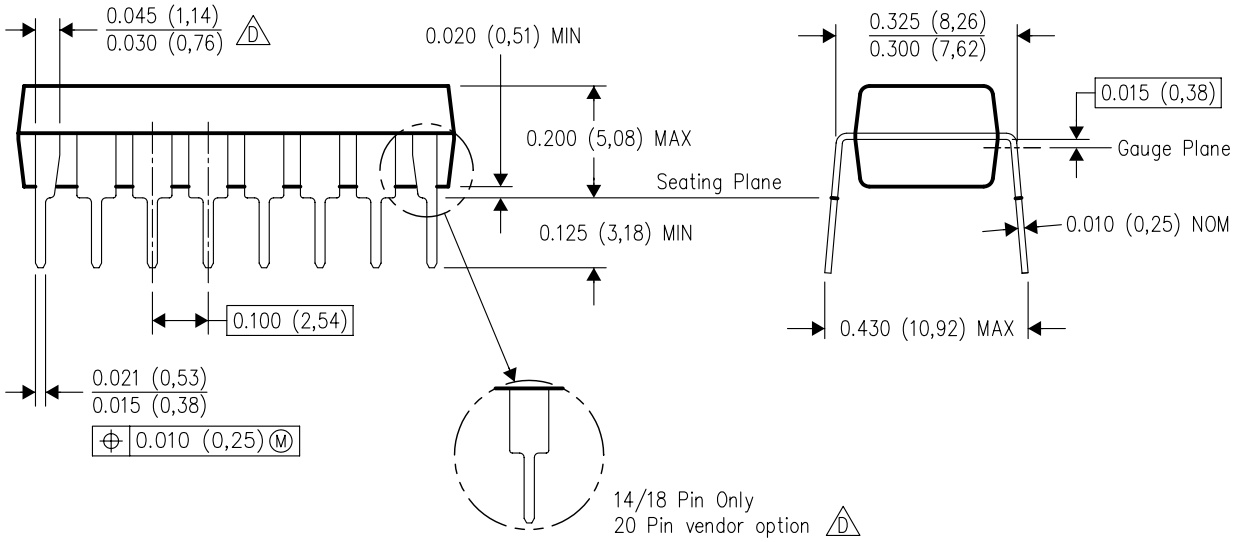
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

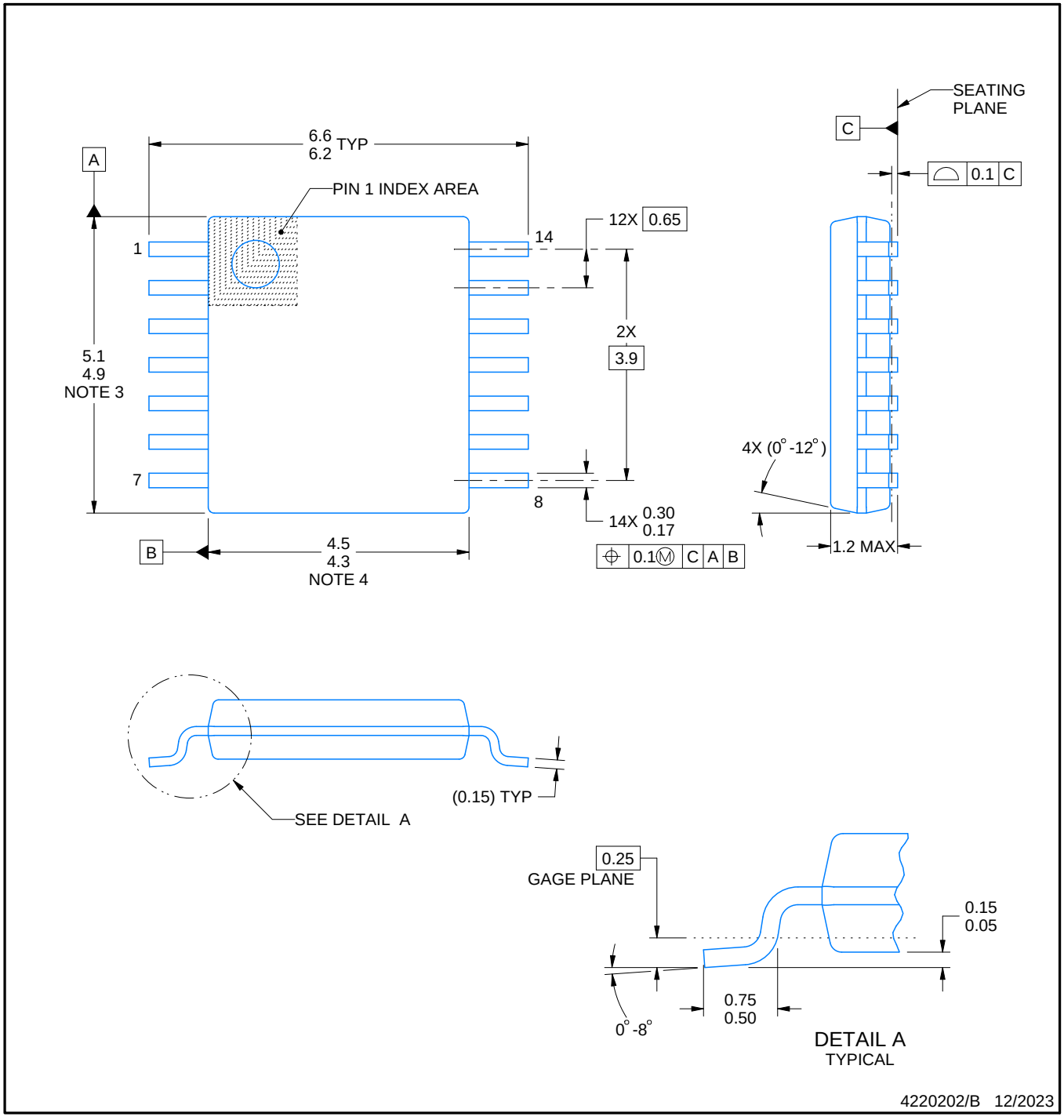
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

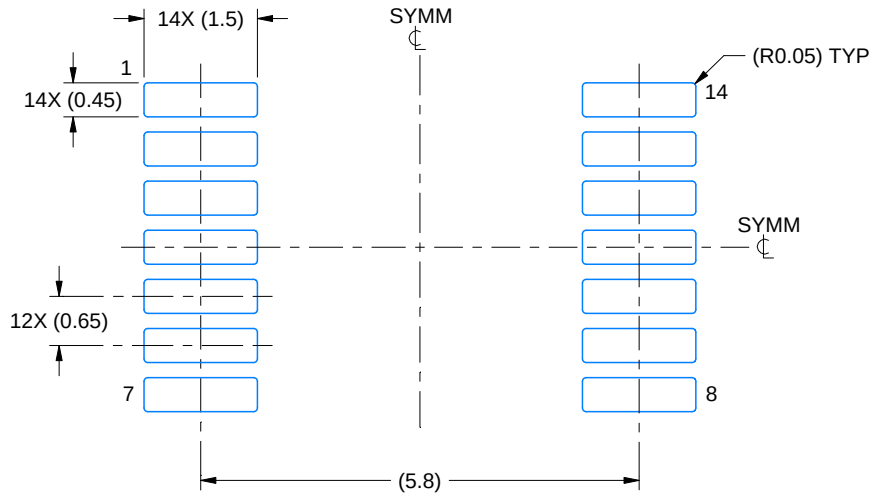
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

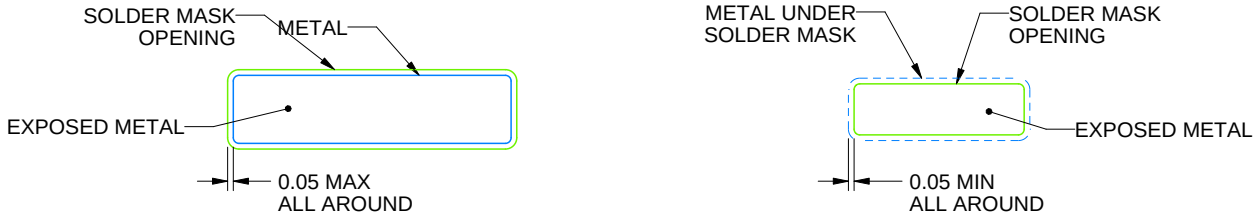


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

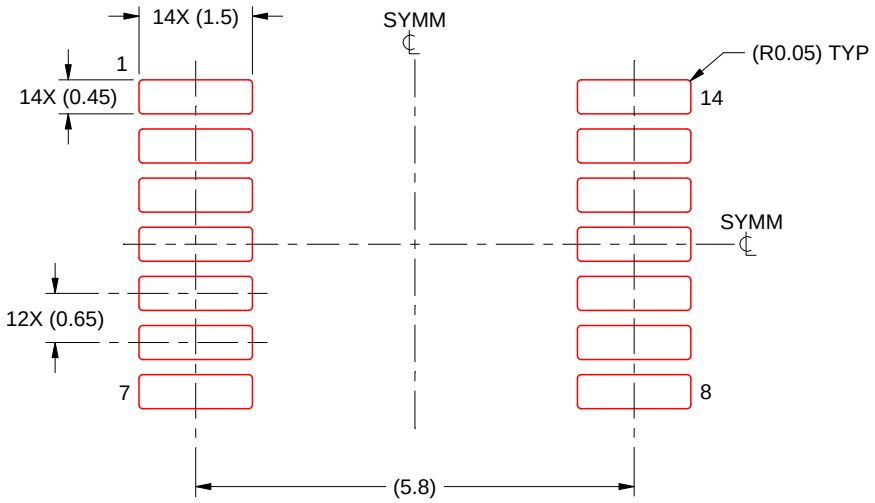


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

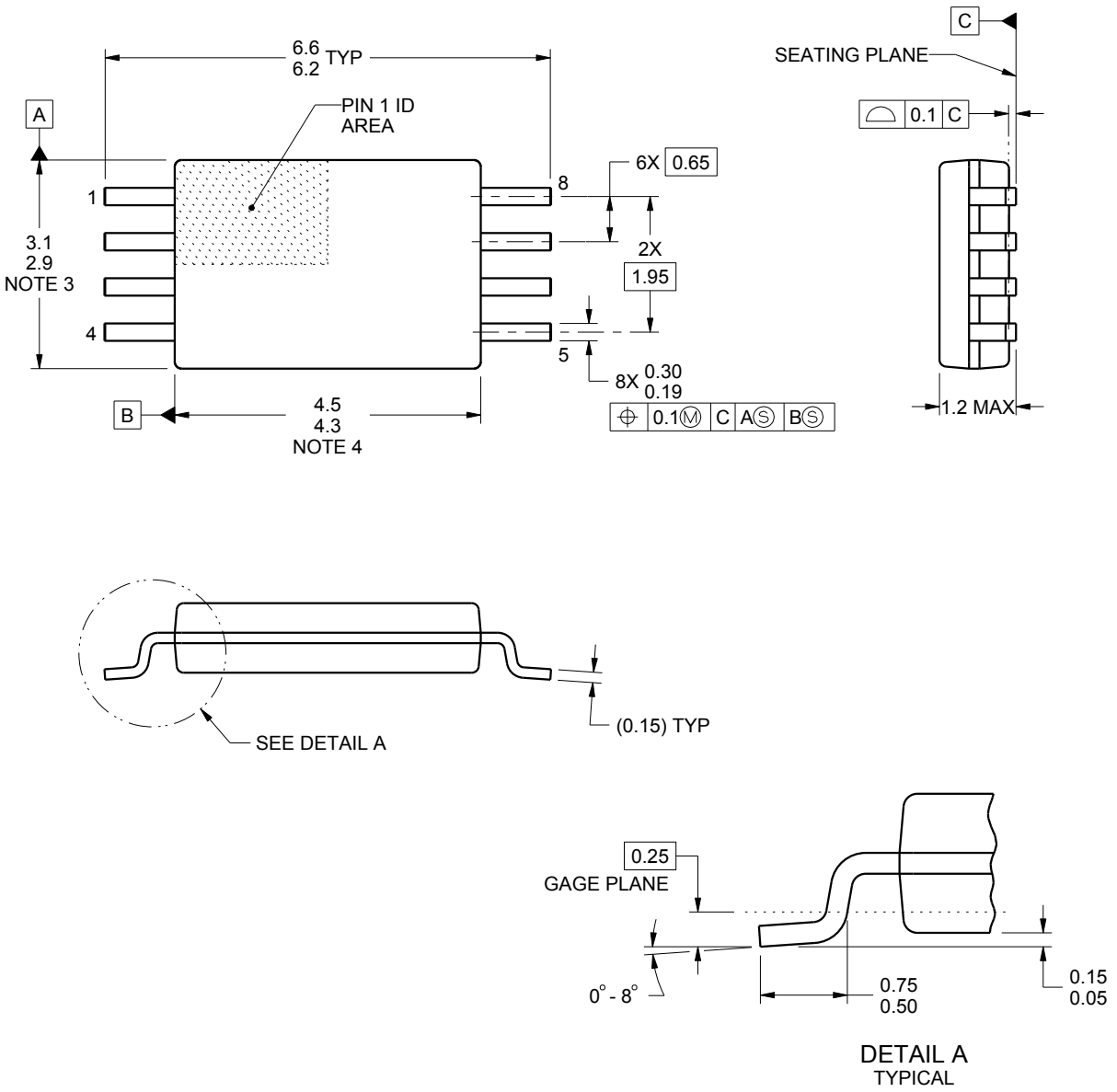
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0008A

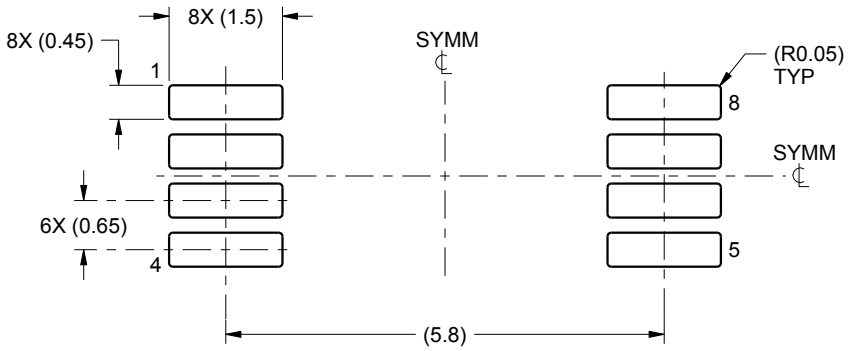
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

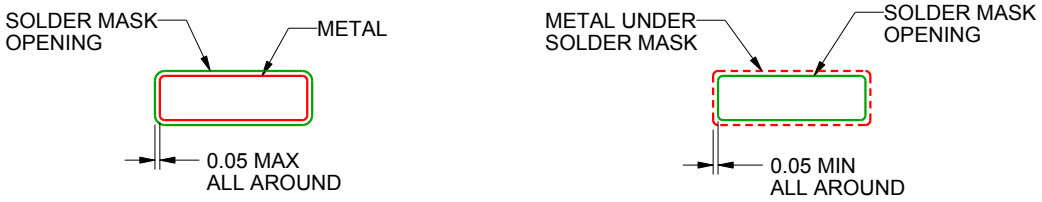


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

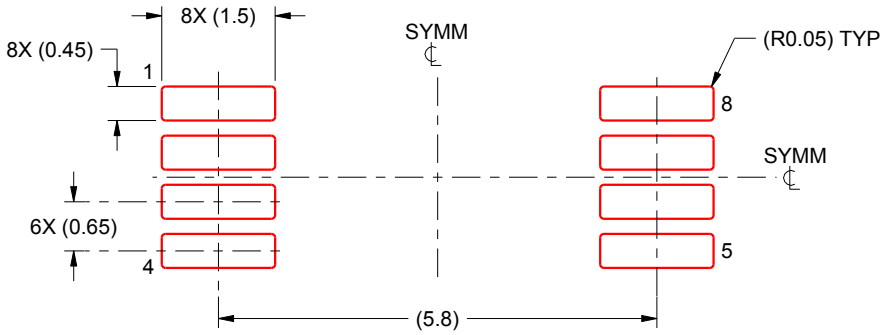


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

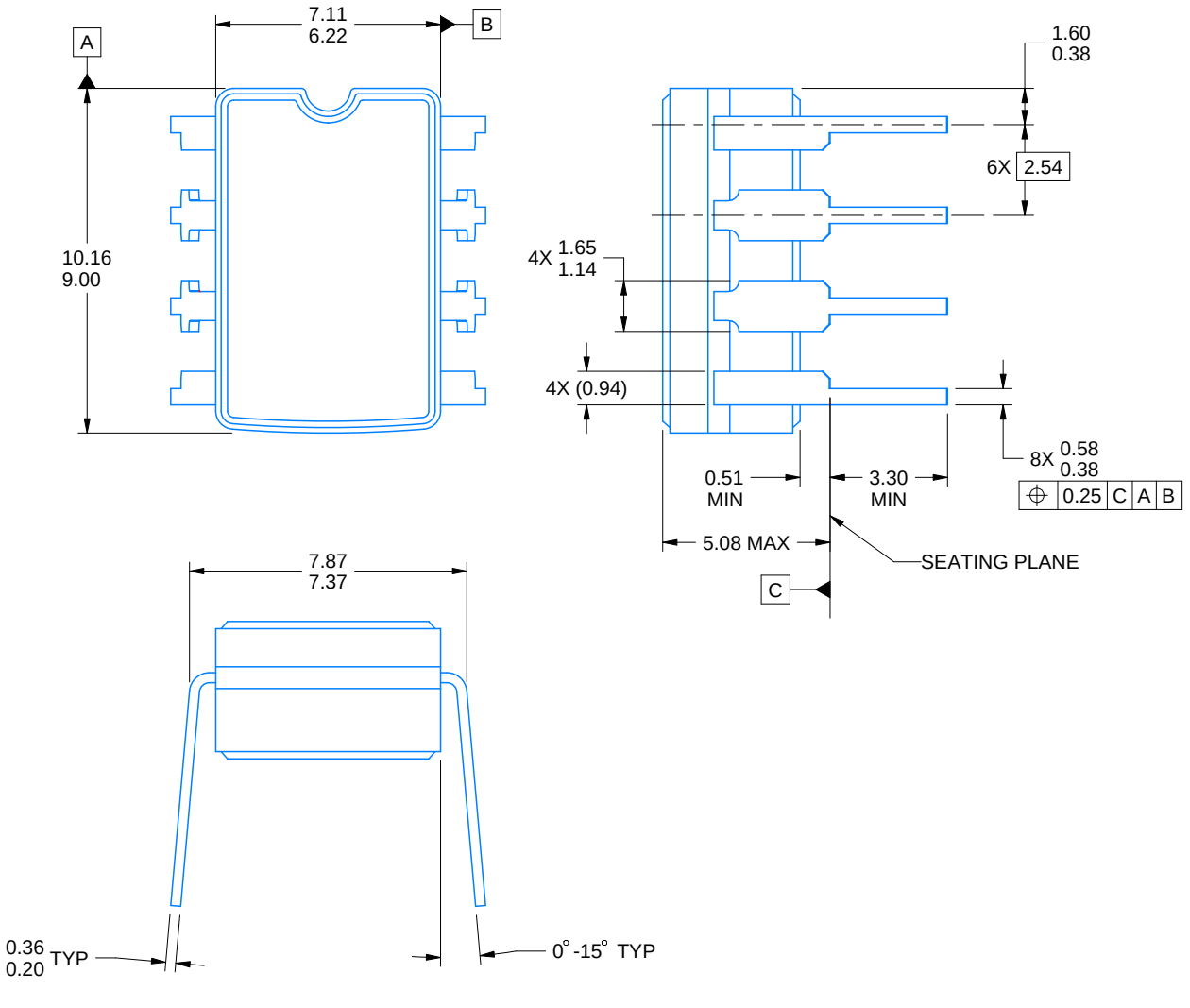
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



4230036/A 09/2023

NOTES:

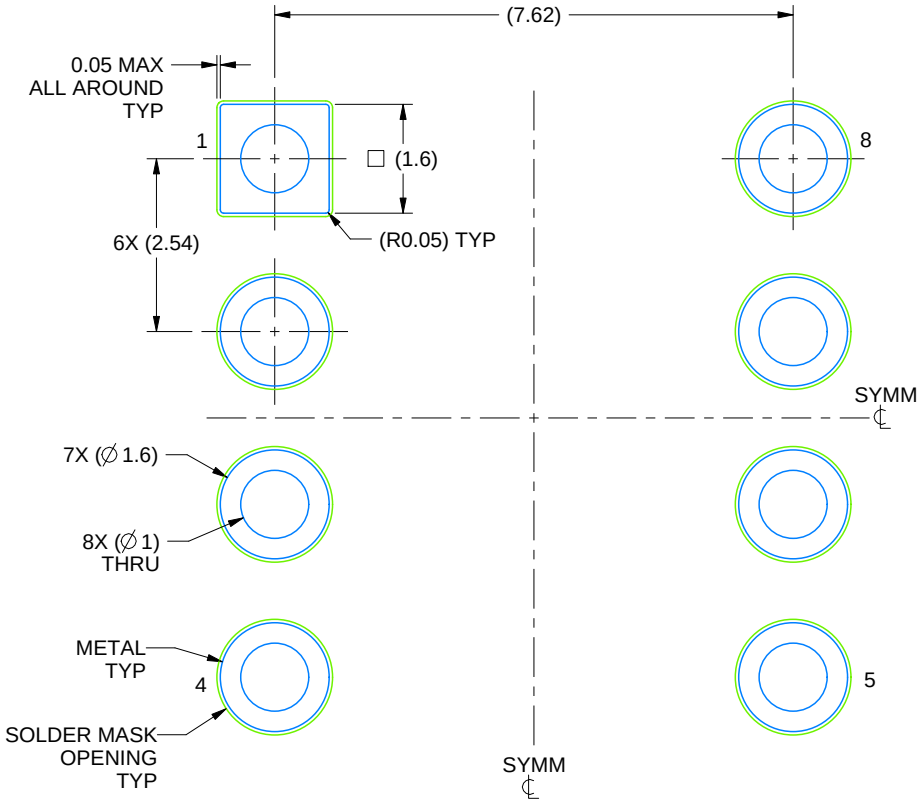
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

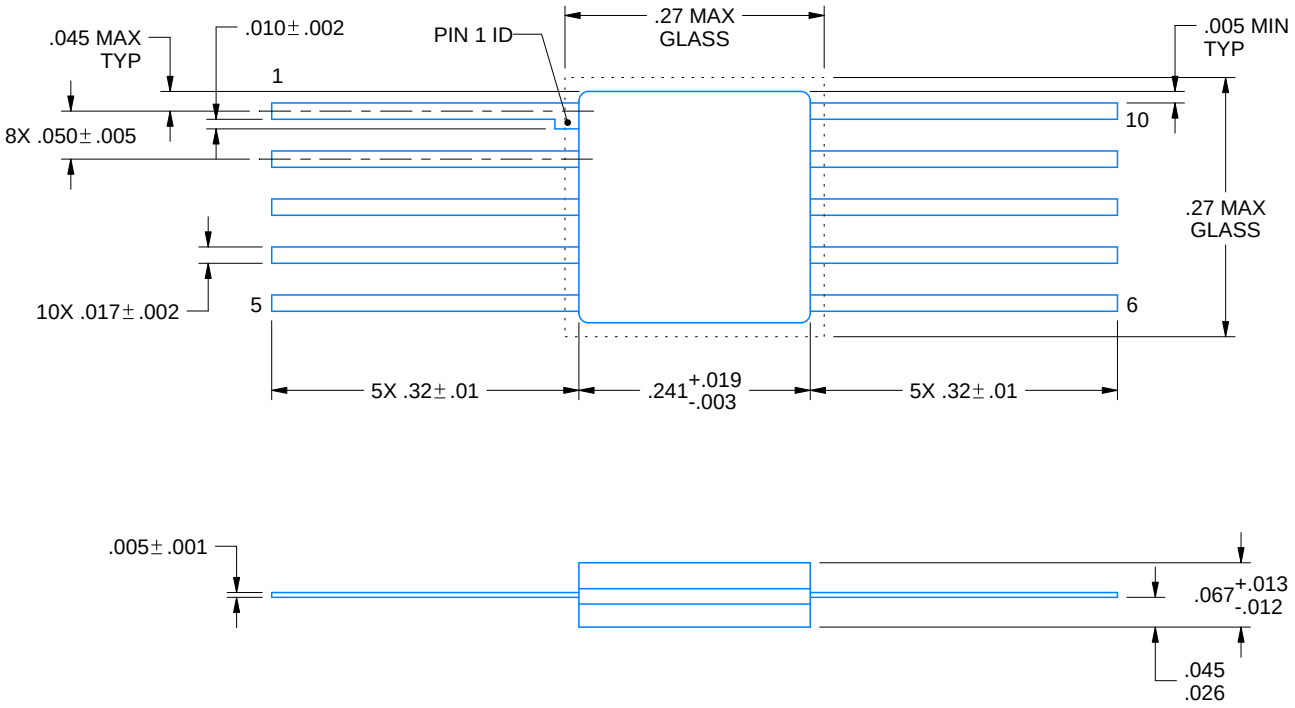
4230036/A 09/2023

U0010A

PACKAGE OUTLINE

CFP - 2.03 mm max height

CERAMIC FLATPACK



4225582/A 01/2020

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale, TI’s General Quality Guidelines, or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Last updated 10/2025